High Power/High Bandwidth GaN MMICs and Hybrid Amplifiers: Design and Characterization

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***Abstract* — Broadband microstrip and coplanar MMIC amplifiers featuring beyond 10W for X-band radar applications are realized in a AlGaN/GaN HEMT technology on 2" s.i. SiC substrate. Single-stage and dual-stage demonstrators with flat gain from 1 GHz to 2.7 GHz and up to 40 W peak power in hybrid microstrip technology for basestation applications are presented. The performance illustrates the potential of this technology with very high bandwidth and superior power density in comparison to GaAs.**

I. Introduction

In recent years, GaN based electronic devices and technologies are rapidly moving from research towards various applications, especially in the area of high-power amplifiers. GaN FETs turned out to be very promising for broadband applications due to the advantageous high voltage operation yielding several times higher impedance levels and power densities in comparison to GaAs and silicon devices. These expectations have been confirmed by outstanding hybrid and MMIC power amplifier results in the last years, e.g. [1,2].

For radar applications, microstrip MMIC realizations of the high power amplifiers (HPAs) are preferred due to their compatibility to module technology [2]. For GaN devices on s.i. SiC substrate, backside processing and microstrip MMIC amplifier realization have been demonstrated in recent years [2]. High-resistivity silicon has been recently proposed as an alternative substrate material for GaN devices e.g. in [3] and for X-Band MMIC amplifiers [5].

Furthermore, GaN on SiC and Si technologies focus on devices for mobile communication applications, especially HPAs for base stations in the 2 GHz range with power densities up to 12 W/mm [4]. Recently, promising hybrid microstrip HPA realizations for 2.1 GHz and more than 200 W output power have been published, using Doherty or push-pull configurations [6].

In this paper, examples of X-band HPA MMICs and hybrid microstrip amplifiers for base station applications are presented with emphasis on power and bandwidth capabilities of GaN devices on s.i. SiC substrate.

II. Processing Overview

A. MMIC Process

The active device structures are fabricated with multi-wafer MOCVD and CAIBE mesa isolation. For different application frequency ranges described here, 0.3 µm and 0.5 µm gate lengths are defined by e-beam lithography. For passive MMIC structures, a two-level metallization with airbridges, MIM capacitors with breakdown voltage beyond 200 V, and thin-film resistors are available. The backside processing includes wafer thinning to 100 µm, etching of 50 µm square via holes, and backside galvanic metallization. Typical DC and RF ratings of the active devices are: $f_T \geq 36$ GHz for 0.3 µm gate length, a maximum transconductance of ≥ 230 mS/mm, a drain-source breakdown voltage of ≥ 65V, a knee voltage of ≤ 5V, and a saturated drain current of ≥ 1100mA/mm.

B. Hybrid Amplifiers

For L-band and S-band hybrid amplifier realization, standard SMD technology with gold plating is applied on microwave laminates of Rogers Corp.. The HEMT power bars of up to 8 mm or 16 mm total gate width are mounted into standard LDMOS packages using an in-house soldering process and wire-bonded to the package leads. Special precautions are taken to avoid odd-mode oscillations within the packaged large power FET cells without bandwidth reduction.

III. Characterization

For device modelling, a comprehensive measurement data base comprising DC data at different temperatures, broadband S-parameter measurements at more than 400 bias points, and pulsed-DC data is used. From this database, equivalent-circuit based large-signal models are extracted [8]. The models are scalable with respect to total gatewidth. For base station amplifiers in the range from 1 GHz to 3 GHz, a flexible modelling of packaged power FET cells with 16 mm total gatewidth and more is required. For this purpose, a scalable large-signal model of a "base cell" chip is embedded in a distributed package model. The latter is extracted from package and FET measurements in the hybrid microstrip environment. Taking into consideration the low input and output impedance levels of the packaged high power cells, a microstrip test fixture was realized which enables calibrated S-parameter measurement in a low-impedance system up to 10 GHz using tapered microstrip lines.

For model verification, RF load-pull and power sweep waveform measurements are used on the on-wafer (chip) level, as well as for packaged high-power HEMT cells. For packaged devices, the load-pull and waveform measurement data are error-corrected to the package reference planes in the hybrid microstrip environment using the above-mentioned "low-impedance" test fixture. As an example, fig. 1 illustrates a power sweep on a packaged 8 mm device at 2.1 GHz under tuning conditions for maximum output power. At 3 dB gain compression, a CW output power of 43.2 dBm (2.6 W/mm) was achieved at $V_{DS} = 35$ V, while the maximum PAE was 42 %. The DC current increases from 0.6 A at 21 dBm net input power to 1.4 A at 31.5 dBm due to the class-AB biasing.

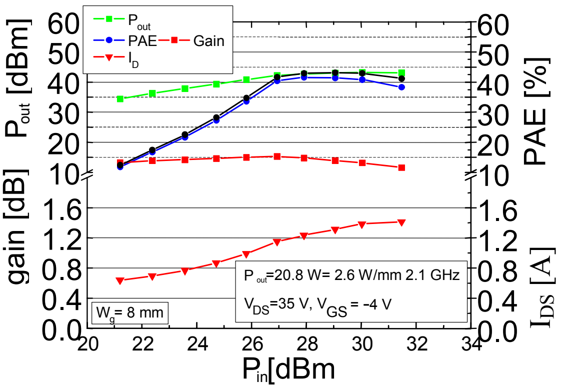

Fig. 1. Output power, gain and PAE vs. input power for a packaged 8 mm device at 2.1 GHz and $V_{DS} = 35$ V under optimum load tuning conditions.

Fig. 2 presents an on-wafer power sweep measurement of a 8x60 µm device, again at 2 GHz with load reflection coefficient tuned to maximum output power. The DC drain voltage is 40 V in this case. The maximum output power is 3.27 W, or 6.9 W/mm, respectively, while the maximum PAE amounts to 46 %. The maximum small-signal net gain is 22 dB, and the maximum output power is obtained with approx. 5 dB of gain compression. The power density of the 8 mm device is significantly lower than for the 0.48 mm cell, which is clearly due to the different thermal configuration, i.e. the heat spreading of a 2" wafer in comparison to an air-cooled hybrid module.

The time-domain load trajectory (I_{DS} vs. V_{DS}) for a power sweep measurement of the 0.48 mm FET at $V_{DS} = 35$ V is depicted in fig. 3 for input power levels from 14 dBm to 24 dBm with 1 dB step. Near maximum power, the trajectory circulates between the knee voltage at saturation drain current and pinch-off just below the drain breakdown voltage. The two different slopes below and beyond the DC bias point are typical for operation around a class-AB DC bias point. The reference plane of the measurement is at the wafer probe tips, so the blow-up in the trajectory is due to parasitic reactive effects, such as output and feedback capacitances. With respect to the intrinsic drain current source of the FET, the loadline will be approximately a straight line without reactive blow-up in the case of proper load tuning. Of course, this plane is not accessible in a practical measurement, because the nonlinear charge currents within the FET can not be de-embedded.

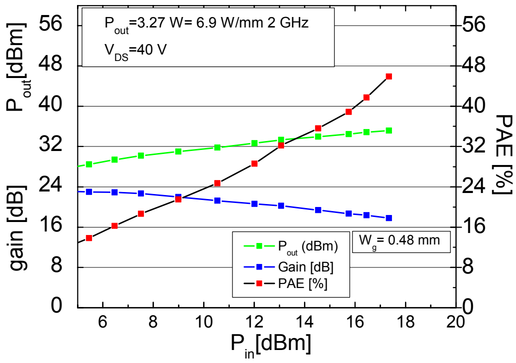

Fig. 2. Output power, gain and PAE vs. input power for a 0.48 mm device at 2 GHz under optimum load tuning conditions.

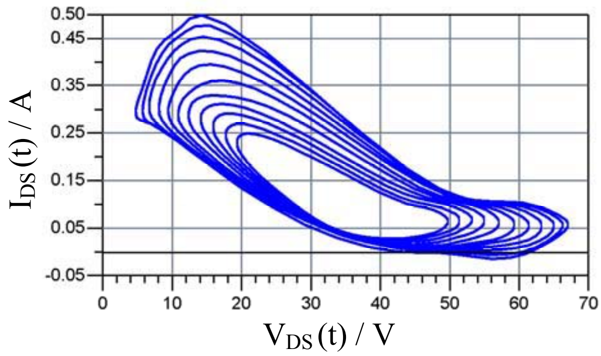

Fig. 3. Waveform measurement: I_{DS} vs. V_{DS} trajectory of the 8x60 µm HEMT at 2 GHz. Input power is 14 dBm to 24 dBm with 1 dB step.

IV. MMIC CIRCUIT DESIGN EXAMPLES

A. Design

For X-band applications, microstrip and coplanar MMIC amplifiers were designed. The microstrip design is targeted directly at pulsed-radar applications, while the coplanar one was developed for performance comparison. The design goal was 18 dB small-signal gain and a saturated output power of at least 10 W in the frequency range of 8.5 GHz to 11 GHz. The gain specification requires a two-stage design. Load-pull waveform measurements and ADS nonlinear simulations on a 8x125 µm HEMT cell both lead to a saturated output power of about 5 W/mm at a DC drain voltage of 30 V for X-band frequencies. For the output and driver stage, 4 mm and 2 mm total gatewidth are used, respectively.

The same design approach was applied for the microstrip [10] and for the coplanar design [7]. The expected high bandwidth potential of the GaN HEMTs which stems from the high impedance levels, e.g. in comparison to GaAs devices of comparable output power levels, was confirmed in the design process. A nearly flat gain was simulated e.g. for the coplanar version of the amplifier in the frequency range from 5 GHz to 11 GHz.

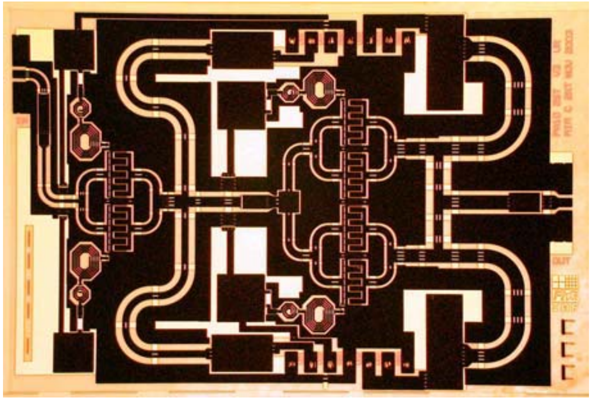

Fig. 4. Chip photograph of X-band CPW MMIC.

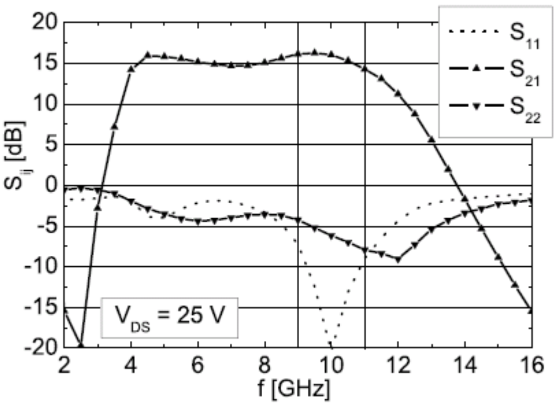

Fig. 5. Small signal S-parameters of X-band CPW MMIC at V_{DS} =25 V.

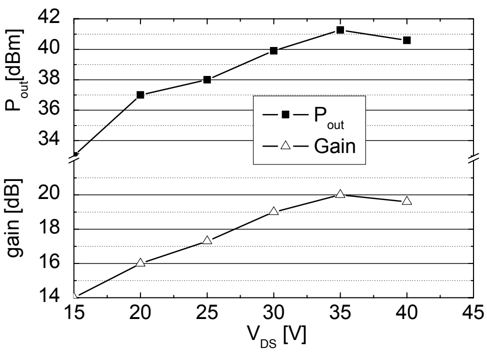

Fig. 6. X-band CPW MMIC pulsed-RF measurements at 10 GHz: Gain and output power vs. DC drain voltage.

B. Results

Fig. 4 depicts a chip photograph of the coplanar variant of the X-Band amplifier. The chip size is 4.5 mm x 3.0 mm. Besides CW small-signal S-parameter measurement, the large-signal behavior of the amplifiers was characterized in both CW and pulsed-RF frequency and power sweeps using a MTA-based waveform measurement system and an Agilent 85124 pulsed-RF network analyzer, respectively. The following performance data were measured on the coplanar X-band amplifier: 15 dB to 16 dB small-signal gain between 4.5 GHz and 11 GHz, input match better than 6 dB and output match better than 10 dB between 9 GHz and 11 GHz. The saturated pulsed-RF output power at 10 GHz amounts to 41.3 dBm (13.4 W) [7]. Fig. 5 depicts the small-signal S-parameters at V_{DS} =25 V.

Fig. 6 shows the dependency of the pulsed-RF output power (measured at 10 GHz with 10% duty cycle) on the DC drain voltage. The design was optimized for drain voltages from 30 V to 35 V. Output power and gain peak for V_{DS} = 35V, and drop again for higher DC drain bias. This is due to the constant value of the intrinsic load resistance, which has an optimum "Cripps" value at this bias. The microstrip version of this amplifier is presented in [10] and has exactly the same chip size and rather similar electrical performance.

V. Hybrid Circuit Design Examples

A. Design

For the hybrid microstrip amplifier realization for 2 GHz basestation applications using standard passive SMD components and packaged HEMTs, we follow a modular concept for single-stage and multi-stage designs. The driver stages operate in class-A bias, while the output stages are in class-AB push-pull configuration. A stepwise impedance transformation from 50 Ω down to the input and output impedance levels of the FETs is used. The bias feed is done via quarter-wavelength line stubs at this low impedance level at input and output of the FETs. For the final input matching, we use a "forced matching" for low frequencies which maintains a good gain flatness and best performance at the upper band edge. For interstage matching in multistage designs, the impedance transformers from 50 Ω to e.g. 15 Ω can be omitted. This circuit concept was used in several designs with up to 8 mm gatewidth for each power FET without any pre-matching within the FET package, and fully confirmed the theoretical expectations of extremely high bandwidth [9].

B. Results

Several single-stage and dual-stage demonstrator amplifiers were realized for basestation applications. For a WCDMA test signal, these amplifiers meet the ACLR specifications (-45 dBc at 5 MHz offset, -50 dBc at 10 MHz offset) nearly over the entire range from 1 GHz to 2.7 GHz. Fig. 7 displays a broadband ACLR measurement of a 4 mm/8 mm dual-stage amplifier including peak/average output power. The gain is 18.5 ± 2 dB within the frequency range from 1.2 GHz to 2.5 GHz. For a 2x8 mm single-stage push-pull demonstrator, a maximum peak output power of 46.1 dBm (40 W, i.e. 2.5 W/mm) is measured at 1.85 GHz with a WCDMA input signal [9].

For more than 8 mm gatewidth per power cell, we simplify the modular design concept, omitting the "forced matching" at the input side because of excessive RF drive levels under large-signal operation, and exchanging bandwidth into gain at the upper band edge. Again, the design is without internal package prematching. Fig. 8 depicts the S-parameters of a recently realized 2x16 mm push-pull amplifier, which is designed for the frequency range between 1.8 GHz and 2.2 GHz. Within the 400 MHz range, the gain flatness is ±1.5 dB, the matching (S_{11} and S_{22}) is better than -7 dB.

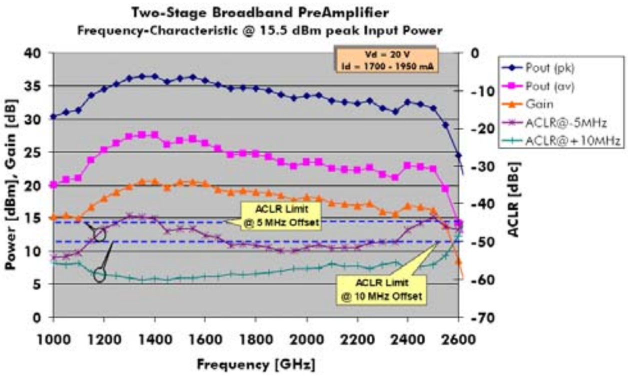

Fig. 7. ACLR measurement including peak and average power and gain for the 4 mm plus 8 mm dual-stage demonstrator.

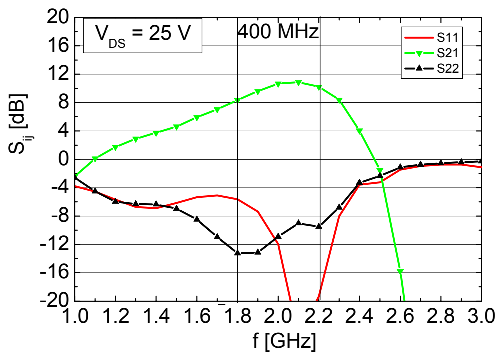

Fig. 8. S-parameters of 2x16 mm 2 GHz demonstrator.

VI. Conclusion

For X-band radar applications, microstrip and coplanar high-power (10 W) MMIC amplifiers were demonstrated in AlGaN/GaN HEMT 2"-technology on s.i. SiC substrate. For basestation applications in the 1 GHz to 2.7 GHz range, single-stage and dual-stage amplifiers with peak output power of 40 W have been realized in hybrid microstrip SMD technology with packaged HEMTs. The performance shows the high potential of GaN on SiC technologies for these applications with respect to bandwidth and power density. Future challenges are e.g. improved thermal management in small MMIC modules or packages for hybrid circuits, reliability, and realization of broadband basestation amplifiers at even higher power levels.

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