# CheckMate* Emulators For the Intel 80186 Family

- 25 MHz Target Operation Standard
- 5V and 3V Support from the Same Product
- Patented Emulator Technology Combined with Intel Processor Technology
- 10 Mbits Per Second Communications Speed
- Fully Supports Intel's ONCE™ Mode for Plug In and Run Operation
- Truly Transparent to the Target; Does Not Use Interrupts or Any Memory Space
- Paradigm DEBUG* Source Level Debug Interface Standard
- Logic Analyzer Style Event System for Target Control and Trace Capture Logic
- 16K Bus Cycles Trace Buffer
- 1024K Overlay Memory

The CheckMate II in-circuit emulator takes advantage of patented 1990's gate array and surface mount assembly technologies to deliver all the emulator features required today in a single low-profile, small foot print device. All CheckMate* emulators take full advantage of Intel's processor technology to insure true transparent and exact emulator functionality.

The emulator combines a robust, state machine driven bus event system and a wide and deep trace memory buffer to deliver next generation capability to the user. As you expect, CheckMate integrates into your existing development environment. We offer support for all Borland* and Microsoft* compilers as well as Intel compilers with the industry standard Paradigm/DEBUG source level debug interface.

The bus event system consists of four groups that each contain eight ADDRess/ADDR range, DATA and STATUS comparitor sets. Each event level or group has an independent 16-bit event pass counter and 8 independent Logic State Input channels. Within the group, each event is coupled independently to both the event counter and the LSI channels. This system makes it easy to identify even the most obscure execution faults.

The trace buffer captures 16K bus cycles of ADDRess, DATA, and STATUS along with the 16-bit timestamp and 8 Logic State Input channels. The trace display shows any combination of source, assembly and raw cycles interleaved for true execution history clarity, and can be fully qualified by any event in the Bus Event System. The timestamp uses 5 timebases – 100 nsec to 1 msec – that are independent of the target CLK; counter overflow is captured automatically to insure accurate long duration measurements. A special timestamp mode measures the MIN, MAX and MEAN interval time statistic.

The overlay RAM is 0-wait state at 25 MHz operation, and may be mapped across the entire target memory address space on 1K boundaries. Each segment can be access protected.

CheckMate emulators have two different models to complete your development tool environment. Finally, you can fine tune development tool capabilities to your team's individual requirements.

HOST SYSTEMS SUPPORTED:
486 PC or above (386 PC minimum), 4 MB RAM, Microsoft Windows* or OS/2 Warp or MS-DOS 6.0 or above. ISA, MCA or PCMCIA version II, type II expansion card slot.

PROCESSORS SUPPORTED:
80C186XL/EA/EB/EC @ 25 MHz,
80L186XL/EA/EB/EC @ 16 MHz

AVAILABILITY:
Stock to 3 weeks ARO.

CONTACT:
Beacon Development Tools
3307 Northland Drive, Suite 270
Austin, TX 78731
Phone: (800) 769-9143
FAX: (512) 467-8960
e-mail: info@beacontools.com
BBS: (512) 467-8947
WWW: http://beacontools.com

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