i960® CA Processor Bus Functional Model

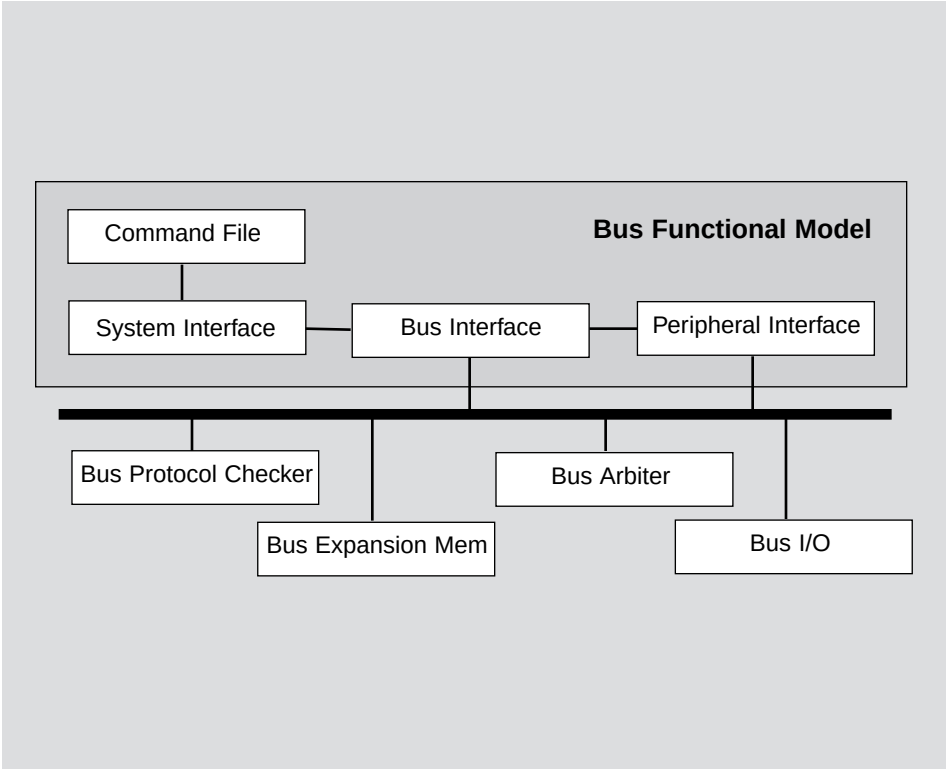
- Model is Done Using VHDL
- Can Simulate Various Transactions on the Bus
- Can Be Instantiated Into a Design as a Symbol
- Model Provides Violation Checks on Setup and Hold Times
- Available on a Variety of VHDL Simulators

The Bus Functional Model (BFM) i960® CA processor BusSim is developed for the simulation of Intel i960 CA processor-based systems. The model includes the various transactions on the bus such as read/write transactions. The BusSim provides a full system level simulation and debug capability.

The BFM is instantiated as a symbol whose behavior is described by the VHDL model. The model reads the transaction file for the commands, which specify the type of transactions the model has to do on the bus.

The model provides a violation check for the setup and hold times on the bus signals.

Each line of the transaction file has a transaction described with five fields describing the type of transaction, the address, data and the byte enables involved in the transaction. The transaction file is an easily editable ASCII file.



Model is available on most of the VHDL simulators such as Viewlogic, Vantage, Synopsis, ModelTech, etc. On Viewlogic the model is available immediately on order. On other simulators, it is available four weeks from receipt of order.

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