HECETA 2 ASIC

Low Cost
Hardware Monitor

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Contents

Revision History

Revision	Date	Who	Comments
0.1	4/10/97	Mike Boyd	Initial Release
0.2	4/15/97	Ed Davis	Modified pinout and updated front cover page and header/footer
0.3	4/25/97	Mike Boyd	Removed LM80 References
0.4	5/16/97	Mike Boyd	Corrected drawings
			Corrected package type to TSSOP-24
			Changed voltage inputs to direct
			Added internal 2.5v reference
0.5	5/19/97	Mike Boyd	Removed duplicate test load schematic
			Added interrupt descriptions
			Corrected interrupt structure diagram
0.6	5/20/97	Mike Boyd	Added company identification byte & stepping
0.7	5/22/97	Mike Boyd	Changed analog inputs from IN0.IN5 to real names
			Changed analog center to 3/4 scale
			Changed suggested external series R from 22 Ohm to 1K
			Added test mode register
0.8	5/22/97	Mike Boyd	Added analog output for fan speed control
			Added default value for analog output
			Changed analog output to 8 bit
0.9	5/22/97		Corrected pinouts of VID[0..4]
			Added fan output circuit
0.91	5/27/97	Mike Boyd	Changed power supply min from 2.8v to 2.85v
			Changed digital input voltages for 3.3v
			Set analog outputs to 0-1.22v
			Updated Connection Diagram to show NAND_TREE/AOUT
0.92	6/4/97	Mike Boyd	Changed +2.5(A) to +2.5
			Changed +2.5(B) to +Vccp
			Explain +Vccp scaling
0.93	6/6/97	Mike Boyd	Set range of Vccp input
0.94	6/6/97	Mike Boyd	Changed references of “-5” to “+3.3”
			Changed references of “+2.5v(A)” to “+2.5v”
			Changed references of “+2.5v(B)” to “Vccp”
0.95	6/18/97	Mike Boyd	Changed register mapping
0.96	6/19/97	Greg Lento	Corrected Register Mapping and Minor Errors
0.97	6/26/97	Greg Lento	Changed Value Ram to match HECETA 1
0.98	7/1/97	Greg Lento	Matched Bit Values to HECETA 1
0.99	7/10/97	Greg Lento	Removed OS# output function. Added Vccp2 selectable function. Changed Icc shutdown spec.
1.0	7/14/97	Greg Lento	Pulled out resistor ladder for –12V (internal to external). Minor corrections. Changed references to I^2C interface to SMBus interface.
1.01	7/24/97	Greg Lento	Changed 330Ω to 10kΩ resistors from A1,A0 pins on block diagram Changed Chart on Page 14 to reflect 10mV LSB weighting Changed References to Register 47h power on defaults to <7:4>=0101
1.02	7/31/97	Greg Lento	Changed Chart on Page 14 back to reflect range of 1.2 to 3.6 Volts
1.03	8/4/97	Greg Lento	Removed Reference to 2.5V VRef

References

1. ***"I^2C Bus Compatible ICs," Philips pgs. 28-58 - "I^2C Bus Specification," 1989***
2. ***Fan Specifications***
3. ***Power Supply Specifications***
4. ***Pentium® Processor (P54/P55) Specification***
5. ***Pentium Pro Processor Specification***
6. ***National LM-78 Specification***
7. ***HECETA Head ASIC Specification***
8. ***System Management Bus Specification***

General Description

The HECETA 2 ASIC provides low-cost instrumentation capabilities for a PC, to lower the total cost of ownership over its life cycle. The HECETA 2 can be used in a PC to monitor temperature, supply voltages and fan speeds. Using these monitored values compared to programmable Watchdog* limits, a fully-programmable interrupt system can be used to alert the user for discrepancies.

Features

- Temperature sensing.
- Two fan speed sensors (connects to fan via wire cable, stab-on connector).
- Monitor power supplies (+5, +12, -12/Vccp2, +3.3, +2.5A, +Vccp1).
- Intrusion detect for security (detects when chassis lid has been removed, even if power is off).
- Remote reset (from a remote peer or server through LANDesk* Configuration Manager 3.0 application and service layers).
- Provides the “reliable hardware” to run Windows NT*.
- SMBus interface used to access the ASIC.
- Watchdog comparisons of all monitored values.

The block diagram of HECETA Head hardware is illustrated in Figure 1 on the next page. The hardware implementation is a single-chip ASIC solution. Everything is on one chip, including the thermal sensor. There is an onboard NAND TREE for testability in a board-level environment.

Applications

- System Thermal and Hardware Monitoring
- Personal Computers
- Office Electronics
- Electronic Test Equipment and Instrumentation

Key Specifications

Voltage monitoring accuracy	±1% (max)	
Temperature accuracy	-40 °C to +125 °C	±3°C(max)
Supply voltage	2.85V to 5.75V	

Supply Current

Operating	250 µA typical
Shutdown	≤ 500 µA typical
Analog-to-Digital Converter Resolution	8 Bits

Ordering Information

Temperature Range $40°C \leq T_A \leq +125°C$ Order Number	**Package Number**	**Specified Power Supply Voltage**
HECETA 2CI?-3	TSSOP-24	3.3-5V

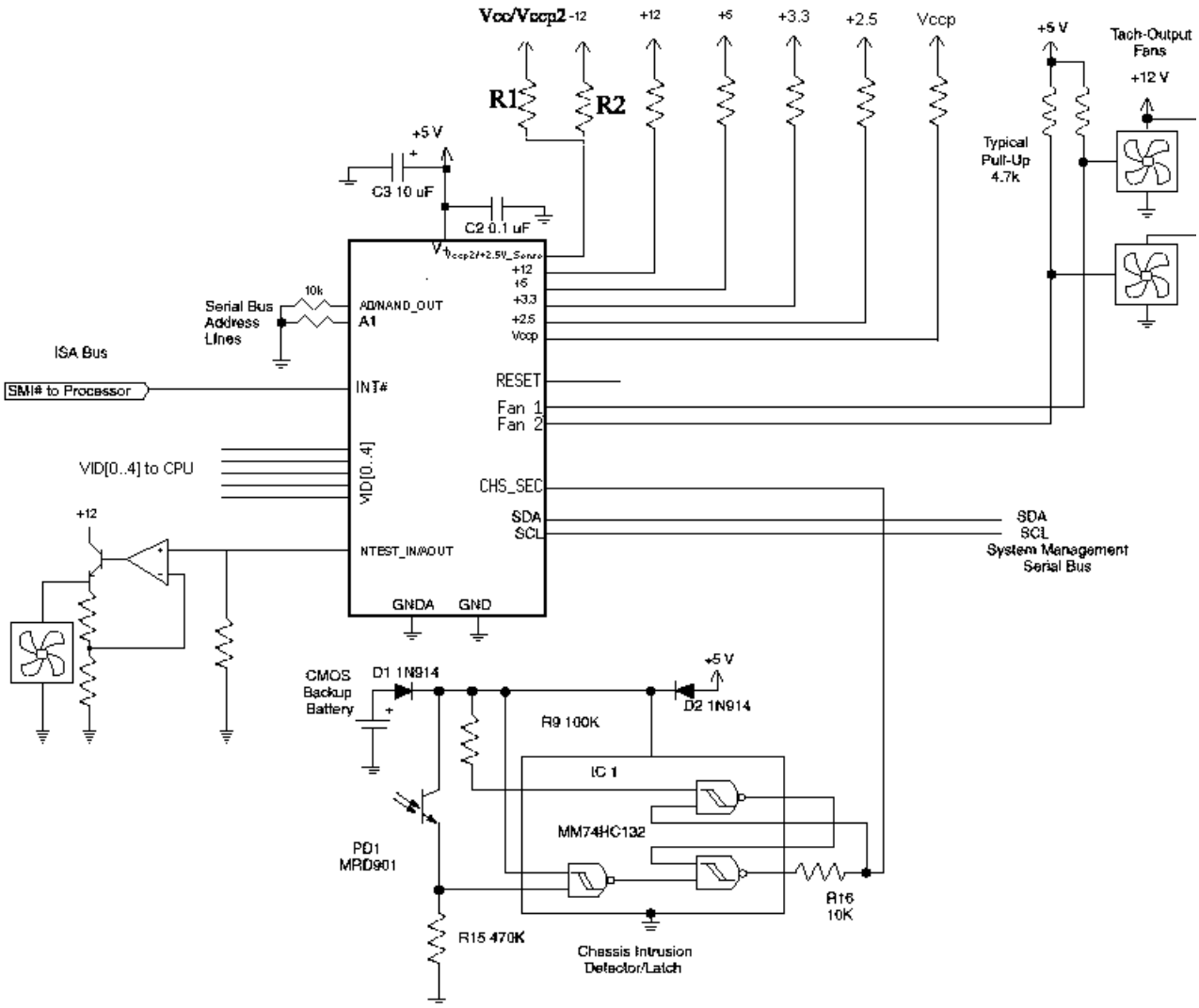


Figure 1: HECETA 2 Block Diagram

Note: *The Chassis Intrusion Detector Latch shown above is only an example. If the Chassis Intrusion circuit runs on battery power, two Toshiba TC7S14 Schmitt Inverters could be used to limit current draw. Also, R1 and R2 on the –12V resistance ladder should be ratioed such that approximately +2.5V appears at the input pin (in other words, R1=40k*Ω*, R2=232k*Ω*). If a second processor voltage needs to be monitored (Vccp2), leave R2 empty, and make R1 zero ohms, with Vccp2 appearing here.*

Connection Diagram

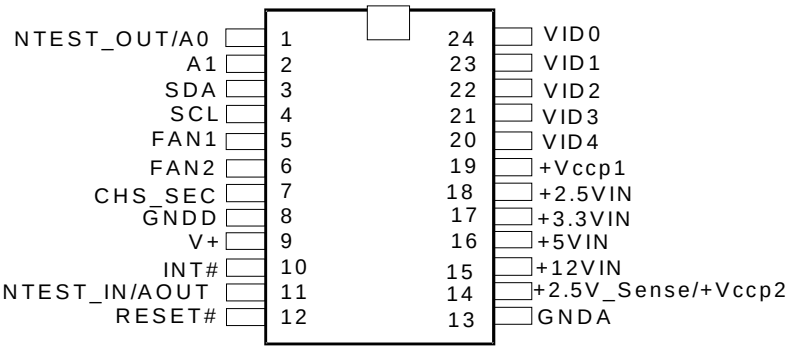


Figure 2: Connection Diagram

Pin Description

Pin Name	Pin Number	Type	Description
NTEST_OUT/A0	1	Digital I/O	The lowest order programmable bit of the SMBus Address. This pin functions as an output when doing a NAND Tree test.
A1	2	Digital Input	The highest order programmable bit of the SMBus Address.
SDA	3	Digital I/O	System Management Bus bi-directional data. Open-drain output.
SCL	4	Digital Input	SMBus clock.
FAN1	5	Digital Input	0 to V+ amplitude fan tachometer input.
FAN2	6	Digital Input	0 to V+ amplitude fan tachometer input.
CHS_SEC (Chassis Intrusion)	7	Digital I/O	An active high input from an external circuit, which latches a Chassis Intrusion event. This line can go high without any clamping action, regardless of the powered state of the HECETA 2. The HECETA 2 provides an internal open drain on this line, controlled by Bit 6 of Configuration Register, to provide a minimum 20 ms reset of this line.
GNDD	8	GROUND	Internally connected to all of the digital circuitry.
V+ (+2.8-5.75V)	9	POWER	+3.3V or +5V V+ power. Bypass with the parallel combination of 10 µF (electrolytic or tantalum) and 0.1 µF (ceramic) bypass capacitors.
INT#	10	Digital Output	The output is enabled when Bit 1 of the Configuration Register is set to 1. The default state is disabled.
NTEST_IN/AOUT	11	Test Input/AOUT	An active-high input that enables NAND Tree board-level connectivity testing. Refer to Section 13.0 on NAND Tree testing. Used as a analog output when NAND Tree is not selected.
RESET#	12	Digital I/O	Master Reset, 5 ma driver (open drain), active low output with at least a 20 ms minimum pulse width. Available when enabled via Bit 4 in the Configuration Register. This is a bi-directional I/O pin. It acts as power on RESET input.
GNDA	13	GROUND	Internally connected to all analog circuitry. The ground reference for all analog inputs.
+2.5V_Sense/+Vccp2	14	Analog Input	Analog input for monitoring -12V or +Vccp2, referenced to +2.5 Volts at the input. Selectable by choosing the appropriate resistor values on the external resistor ladder. Input to this pin

Pin Name	Pin Number	Type	Description
			should be scaled to +2.5V.
+12	15	Analog Input	Analog input for +12V.
+5	16	Analog Input	Analog input for +5V.
+3.3	17	Analog Input	Analog input for +3.3V.
+2.5	18	Analog Input	Analog input for +2.5V.
+Vccp1	19	Analog Input	Analog input for +Vccp.
VID4	20	Digital Input	Voltage supply readouts from the processor. This value is read in the VID0-VID4 Status Register.
VID3	21	Digital Input	Voltage supply readouts from the processor. This value is read in the VID0-VID4 Status Register.
VID2	22	Digital Input	Voltage supply readouts from the processor. This value is read in the VID0-VID4 Status Register.
VID1	23	Digital Input	Voltage supply readouts from the processor. This value is read in the VID0-VID4 Status Register.
VID0	24	Digital Input	Voltage supply readouts from the processor. This value is read in the VID0-VID4 Status Register.

# Indicates Active Low (“Not”)

Absolute Maximum Ratings

Positive Supply Voltage (V+)	6.5V
Voltage on Any Input or Output Pin	-0.3V to (V++0.3V) (Except analog inputs)
Ground Difference (GND-GNDA)	± 300 mV
Input Current at Any Pin (Note 3)	±5mA
Package Input Current (Note 3)	±20mA
Maximum Junction Temperature (TJmax)	150 °C

ESD Susceptibility

ESD Human Body Model	2 kV (except for Chassis Intrusion pin = 500V)

Soldering Information

TSSOP-24 Package (note 5):

Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature	-65°C to +150°C

Operating Temperature

Operating Temperature Range	$-40°C \le T_A \le +125°C$

Operating Voltage Ratings

Supply Voltage (V+)	+2.8V to +5.75V
Ground Difference (|GND-GNDA|)	±100 mV
VIN Voltage Range	-0.05V to V^+ + 0.05V

DC Electrical Characteristics

Symbol	Parameter	Conditions	Typical	Limits	Units (Limits)
Power Supply Characteristics					
ICC	Supply Current Interface Inactive		1.0	2	ma (max)
	Shutdown Mode		≤ 500		µA
Temperature-to-Digital Converter Characteristics					
	Accuracy $-40°C \le T_A \le +125°C$ $-25°C \le T_A \le +100°C$			 ± 3 ± 2	 °C (max) °C (max)
	Resolution			0.5	°C (min)
Voltage Range					
	3.3V -5% < V+ < 5V +5%				°C (min)
Symbol	**Parameter**	**Conditions**	**Typical**	**Limits**	**Units (Limits)**

Analog-to-Digital Converter Characteristics					
TUE	Total Unadjusted Error (Note 7)			±1	% (max)
DNL	Differential Non-Linearity		±1		LSB
PSS	Power Supply Sensitivity		±1		%/V
t_C	Total Monitoring Cycle Time (Note 8)		1.0	1.5	sec (max)
Multiplexer/ADC Input Characteristics					
	On Resistance		400	2000	Ω (max)
	Off Channel Leakage Current		±0.1		nA
	Input Current (On Channel Leakage Current)		±0.1		nA
Fan RPM-to-Digital Converter					
	Accuracy	+25°C < TA < +75°C -10 °C < TA < +100°C		±6 ±12	% (max) % (max)
	Full-scale Count			255	(max)
	FAN1 and FAN2 Nominal Input RPM	Divisor = 1, Fan Count = 153 (Note 9)	8800		RPM
		Divisor = 2, Fan Count = 153 (Note 9)	4400		RPM
		Divisor = 4, Fan Count = 153 (Note 9)	2200		RPM
		Divisor = 8, Fan Count = 153 (Note 9)	1100		RPM
	Internal Clock Frequency	+25°C < TA < +75°C	22.5		
	Set so that fan speeds fall within the specified RPM ranges.	-10°C < TA < +100°C	22.5		
Digital Outputs: A0/NTEST_OUT, INT#					
VOUT(1)	Logical ‘1’ Output Voltage	IOUT = ±5.0 ma at V+= 4.25V IOUT = ±3.0 ma at V+= 2.85V		2.4 2.4	V (min) V (min)
VOUT(0)	Logical ‘0’ Output Voltage	IOUT = ±5.0 ma at V+= 5.75V IOUT = ±3.0 ma at V+= 3.45V		0.4 0.4	V (max) V (max)

Symbol	Parameter	Conditions	Typical	Limits	Units (Limits)
Open Drain Digital Outputs: RST#, CI					
VOUT(0)	Logical '0' Output Voltage	IOUT = ±5.0 ma at V+= 5.75V IOUT = ±3.0 ma at V+= 3.45V		0.4	V (min)
IOH	High Level Output Current	VOUT = V+	0.1	100	µA (max)
	RST# and CI Pulse Width		45	20	ms (min)
Open Drain SMBus Output: SDA					
VOUT(0)	Logical '0' Output Voltage	IOUT = ±3.0 ma at V+= 5.75V IOUT = ±3.0 ma at V+= 3.45V		0.4 0.4	V (min) V (min)
IOH	High Level Output Current	VOUT = V+	0.1	100	µA (max)
SMBus Digital Inputs: SCL, SDA					
VIN(1)	Logical '1' Input Voltage			0.7 x V+	V (min)
VIN(0)	Logical '0' Input Voltage			0.3 x V+	V (max)
Digital Inputs: NTEST_IN, A0/NTEST_OUT, A1, CI, VID0-VID4 and Tach Pulse Logic Inputs (Fan1, Fan2)					
VIN(1)	Logical '1' Input Voltage (5V)			2.4	V (min)
VIN(0)	Logical '0' Input Voltage (5V)			0.8	V (max)
VIN(1)	Logical '1' Input Voltage (3.3V)			2.0	V (min)
VIN(0)	Logical '0' Input Voltage (3.3V)			0.4	V (max)
All Digital Inputs					
IIN(1)	Logical '1' Input Current	VIN= V+	-0.005	-1	µA (min)
IIN(0)	Logical '0' Input Current	VIN=0 VDC	0.005	1	µA (max)
CIN	Digital Input Capacitance		20		pF

AC Electrical Characteristics

Symbol	Parameter	Conditions	Typical	Limits	Units (Limits)
SMBus Timing Characteristics					
t1	SCL (Clock) Period			**2.5**	µs (min)
t2	Data In Setup Time to SCL High			**100**	ns (min)
t3	Data Out Stable After SCL Low			**0**	ns (min)
t4	SDA Low Setup Time to SCL Low (start)			**100**	ns (min)
t5	SDA High Hold Time After SCL High (stop)			**100**	ns (min)

Notes

- Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

- All voltages are measured with respect to ground, unless otherwise specified.

- When the input voltage (VIN) at any pin exceeds the power supplies (VIN< (GND or GNDA) or VIN>V+, except for analog voltage inputs), the current at that pin should be limited to 5mA. The 20mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5mA to four.

- The maximum power dissipation must be derated at elevated temperatures and is dictated by TJmax, QJA and the ambient temperature, TA. The maximum allowable power dissipation at any temperature is PD = (TJmax - TA) / QJA.

- Solder according to Interprocess Communications (IPC) standards.

- Typicals are at TJ=TA=25°C, and represent the most likely parametric norm.

- TUE (Total Unadjusted Error) includes Offset, Gain and Linearity errors of the ADC.

- Total Monitoring Cycle Time includes temperature conversion, all analog input voltage conversions, and all tachometer readings.

- The total fan count is based on two pulses-per-revolution of the fan tachometer output.

- Timing specifications are tested at the Transistor Transistor Logic (TTL) levels, VIL=0.4V for a falling edge and VIH=2.4V for a rising edge. TRI-STATE output voltage is forced to 1.4V.

Functional Description

1.0 General Description

The HECETA 2 provides six analog inputs, an analog output, five digital inputs, two fan speed inputs, a temperature sensor, and Watchdog registers on a single chip**,** which communicates on a System Management bus (SMBus). The HECETA 2 performs power supply, temperature, and fan monitoring for personal computers.

The analog voltages are divided internally by the HECETA 2 (excluding the 2.5V_Sense/+Vccp2 input). The inputs are then converted to 8-bit digital words with a 10 mV LSB (Least Significant Bit) weighting. The analog inputs are intended to be connected to the several power supplies present in a typical computer. Temperature can be converted to an 8-bit two's-complement digital word with a 0.5°C LSB.

The analog output is approximately a 0-1.25V output from an 8-bit D/A converter, which is used to control fan speeds.

Fan inputs can be programmed to accept either fan failure indicator or tachometer signals. Fan failure signals can be programmed to be either active high or active low. Fan inputs measure the period of tachometer pulses from the fans, providing a higher count for lower fan speeds. The fan inputs are digital inputs with an acceptable range of 0 to V+ volts and a transition level of approximately 1.4 Volts. Full-scale fan counts are 255 (8-bit counter), and this represents a stopped or very slow fan. Nominal speeds, based on a count of 153, are programmable from 1100 to 8800 RPM on FAN1 and FAN2. Signal conditioning circuitry is included to accommodate slow rise and fall times.

The HECETA 2 provides a number of internal registers, as detailed in Table 1. These include:

- **Configuration Register**: Provides control and configuration, as well as initialization.
- **Interrupt (INT#) Status Registers**: Two registers to provide status of each Watchdog limit or Interrupt event.
- **Interrupt (INT#) Mask Registers**: Allows masking of individual Interrupt sources, as well as separate masking for the hardware interrupt output.
- **Temperature Configuration Register**: The lower 2 bits of this register configure the type of temperature interrupt mode to be used. Bit 7 reflects the lowest bit of the temperature reading.
- **VID Register, VID 4 Register**: Bits 0-3 of the VID register reflect the status of the VID0-VID3 pins, bit 0 of the VID 4 register reflect the status of VID 4 pin. These are simply input pins — not processed in any way. In a multiprocessor system, these signals will be multiplexed externally from the various processor sources, with the source being controlled by software.
- **Value RAM**: The monitoring results and limits for temperature, voltages, fan counts, and Fan Divisor/RST# Register limits are all contained in the Value RAM.

When the HECETA 2 is started, it cycles through each measurement in sequence, and it continuously loops through the sequence approximately once every second. Each measured value is compared to values stored in Watchdog, or Limit registers. When the measured value violates the programmed limit the HECETA 2 will set a corresponding System Management Interrupt (SMI) in the Interrupt Status Registers. One hardware interrupt line, INT#, is available to generate an SMI. INT# is fully-programmable with masking of each Interrupt source, and masking of each output. In addition, the Fan Divisor register has control bits to enable or disable the hardware Interrupts.

A CI (Chassis Intrusion) digital input is provided. The Chassis Intrusion input is designed to accept an active high signal from an external circuit that latches when the case is removed from the computer; this dual purpose pin will be driven low by the HECETA to reset the external circuit.

2.0 SMBus Interface

When using the SMBus Interface a write will always consist of the HECETA 2 SMBus Interface Address byte, followed by the Internal Address Register byte, then the data byte. There are two cases for a read:

- If the Internal Address Register is known to be at the desired Address, simply read the HECETA 2 with the SMBus Interface Address byte, followed by the data byte read from the HECETA 2.

- If the Internal Address Register value is unknown, write to the HECETA 2 with the SMBus Interface Address byte, followed by the Internal Address Register byte. Then restart the Serial Communication with a Read consisting of the SMBus Interface Address byte, followed by the data byte read from the HECETA 2.

The default power on SMBus address for the HECETA 2 is 01011(A1)(A0) binary, where A0-A1 reflects the state of the pins defined by the same names. The address can be changed by writing any desired value to the SMBus Address register (excluding the 2 LSBs). All of these communications are depicted in the SMBus Interface Timing Diagrams, as shown in the SMBus Timing Section at the end of this document.

Table 1. The internal registers and their corresponding internal HECETA 2 addresses:

Register	HECETA 2 Internal Hex Address (This is the data to be written to the Address Register)	Power on Value	Notes
Configuration Register	40h	0000 1000	
Interrupt (INT#) Status Register 1	41h	0000 0000	
Interrupt (INT#) Status Register 2	42h	0000 0000	
Interrupt (INT#) Mask Register 1	43h	0000 0000	
Interrupt (INT#) Mask Register 2	44h	0000 0000	
Chassis Intrusion Clear Register	46h	0000 0000	Bit 7 of this register clears Chassis Intrusion. The other bits are reserved.
VID Register	47h	0101 XXXX	The lower 4 bits reflect the state of VID0-VID3 pins.
Serial Address Register	48h	0010 1101	
VID 4 Register	49h	1000 000X	Bit 0 = VID 4. The rest are reserved.
Temperature Configuration Register	4Bh	0000 0001	
Value RAM	15h-3Dh		
Analog output	19h	1111 1111	Full on.
Company ID	3Eh	Company-dependent	Read only.
Stepping	3Fh	Company-dependent	Read only.

3.0 Using The HECETA 2

3.1 Power On

Applying power to the HECETA 2 resets several of the registers. Power on conditions of the registers are shown in Table 1 on the previous page. Some registers have indeterminate power on values, such as the Watchdog and RAM registers, and these are not shown in the table. Upon power up, the ADC is inactive. Writing Watchdog limits into the Value RAM should usually be the first action performed after power up. The RESET pin is bi-directional. It forces RESET at power on, but can also be pulled low to force RESET internally.

3.2 Resets

Using the Configuration Register Initialization causes the same effect as a power-on reset. However, unlike the power-on reset, if the Value RAM and Watchdog limits were previously set, they will not be affected by the Configuration Register Initialization. The power on reset and configuration register initialization clear or initialize these registers:

- *Configuration Register*
- *Interrupt Status Register 1*
- *Interrupt Status Register 2*
- *INT# Mask Register 1*
- *INT# Mask Register 2*
- *Temperature Configuration Register*

Note: *Setting Bit 7 high of the Configuration Register causes a Configuration Register Initialization. This bit automatically clears after being set.*

3.3 Using the Configuration Register

Control of the HECETA 2 is provided through the configuration register. The Analog-to-Digital Converter is stopped upon power up, and the INT_Clear signal is asserted, clearing the INT# outputs. The Configuration Register is used to start and stop the HECETA 2; enable or disable interrupt outputs and modes, and provides the initialization function described above.

Bit Number	Purpose
0	Controls the monitoring loop of the HECETA 2. Setting Bit 0 low stops the monitoring loop and puts the HECETA 2 into a shutdown mode. SMBus communication is still possible with any register in the HECETA 2 during the shutdown mode. Setting Bit 0 high starts the monitoring loop.
1	Enables or disables the INT# Interrupt output. Setting Bit 1 high enables the INT# output. Setting bit 1 low disables the output.
3	Clears the INT# interrupt output when set high. The HECETA 2 monitoring function will stop until bit 3 is set low. Interrupt Status register contents will not be affected.
4	Initiates a minimum 20 ms RESET signal on the RESET# output if the pin is configured for the RESET# mode.
6	Resets the Chassis Intrusion (CI) output pin when set high.
7	Starts a Configuration Register Initialization when taken high.

3.4 Beginning A Conversion

The HECETA 2 Monitoring function is started by writing to the Configuration Register and setting the INT_Clear (Bit 3) low, and Start (Bit 0) high. At this point the INT#_Enable (Bit 1) should be set high to enable interrupts (INT#). The HECETA 2 then performs a “round robin” sampling of the inputs, sampling each approximately once-a-second, in the order (corresponding to locations in the Value RAM) shown below:

1	Temperature reading
2	Analog -12v/Vccp2
3	Analog +12v
4	Analog +5v
5	Analog +3.3v
6	Analog +2.5v
7	Analog +2.5v
8	Fan 1
9	Fan 2

3.5 Reading Conversion Values

The results of the sampling and conversions can be found in the Value RAM and are available at any time.

4.0 Analog Inputs

The HECETA 2 contains inputs for directly monitoring the power supplies typically found in a PC (+12 V, +5V, +3.3V, +2.5V, +Vccp). These inputs are scaled internally to an internal reference source, converted via an 8-bit successive approximation register ADC or a Delta-Sigma ADC, and scaled so that the correct value refers to 3/4 scale or 192 decimal. This removes the original external resistors and allows for a more accurate means of measurement since the voltages are referenced to a known value.

Since these inputs are above Vcc and below ground, they are not diode-protected to the power rails. The +Vccp input is used to measure the processor core voltage, which varies from 1.2v-3.6v. This table will help:

Starting voltage	1.2
Ending voltage	3.6
Delta	2.4
mV/Step	0.094 mV

Decimal		Voltage (V)		Decimal		Voltage (V)
0		1.200		246		3.519
1		1.209		247		3.528
2		1.218		248		3.537
3		1.227		249		3.546
4		1.236		250		3.555
5		1.245		251		3.564
6		1.254		252		3.573
7		1.263		253		3.582
8		1.272		254		3.591
9		1.281		255		3.600

4.1 Input safety

Since the power supply voltages will appear directly at the pins, small external series resistors such as 500 ohm should be put into the lines driving the chip. This prevents damaging the traces or power supplies should an accidental short such as a probe connect two power supplies together. The +2.5V_Sense/+Vccp2 input uses its external resistance ladder for this purpose.

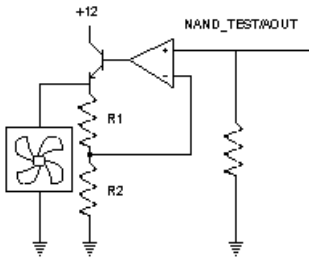
The worst accident would be connecting -12V to +12V—a total of 24V difference—with the series resistors. This would draw a maximum of approximately 24ma.

Keep this value as small as possible, since raising this resistor will affect the accuracy of the internal dividers.

5.0 Analog Output

The HECETA 2 has a single analog output from an unsigned 8-bit D/A that produces 0-1.25 volts. This is amplified and scaled with external circuitry, such as an op-amp and transistor, to provide fan-speed control. This register is set to 0xFF on reset, which produces full fan-speed control.

This voltage must be scaled and have an output current of at least 250ma, which is needed to drive the fans. Here is a simple circuit that can be used—R1 and R2 select gain.



Note: *The full voltage is specified as 1.25V. This is desired. Other voltages, depending on manufacturer, can be considered.*

A table of common values for 1.25V:

Input	1.22
Output	12
Gain	9.84
R1	**R2**
1,000	9,000
2,200	19,439
3,300	29,159
4,700	41,530
10,000	88,361

6.0 Layout and Grounding

Analog inputs will provide best accuracy when referred to the AGND pin. A separate, low-impedance ground plane for analog ground, which provides a ground point for the voltage dividers and analog components, will provide best performance. However, this is not mandatory. Analog components such as voltage dividers should be located physically as close as possible to the HECETA 2.

The power-supply bypass, the parallel combination of 10µF (electrolytic or tantalum) and 0.1 µF (ceramic) bypass capacitors connected between pin 9 and ground, should also be located as close as possible to the HECETA 2.

7.0 Fan Inputs

Inputs are provided for signals from fans equipped with tachometer outputs. These are logic-level inputs with an approximate threshold of 1.4 volts. Signal conditioning in the HECETA 2 accommodates the slow rise and fall times typical of fan tachometer outputs. The maximum input signal range is 0 to V+.

In the event these inputs are supplied from fan outputs that exceed 0 to V+, either resistive division or diode clamping must be included to keep inputs within an acceptable range, as shown in Section 5.0.

R2 is selected so that it does not develop excessive voltage due to input leakage. R1 is selected based on R2 to provide a minimum input of 2 volts and a maximum of V+. R1 should be as low as possible to provide the maximum possible input up to V+, for best noise immunity. Alternatively, use a shunt reference or zener diode to clamp the input level.

Counts are based on 2 pulses-per-revolution tachometer outputs.

RPM	**Time per revolution**	**Counts for 'Divide by 2' (default) in decimal**	**Comments**
4400	13.64 ms	153 counts	Typical RPM
3080	19.48 ms	219 counts	70% RPM
2640	22.73 ms	255 counts (maximum counts)	60% RPM

.

Mode Select	**Nominal RPM**	**Time per revolution**	**Counts for given speed (decimal)**	**70% RPM**	**Time-per-revolution for 70% RPM**
Divide by 1	8800	6.82 ms	153	6160	9.74 ms
Divide by 2	4400	13.64 ms	153	3080	19.48 ms
Divide by 4	2200	27.27 ms	153	1540	38.96 ms
Divide by 8	1100	54.54 ms	153	770	77.92 ms

$$\text{Count} = \frac{1.35 \times 10^6}{\text{RPM} \times \text{Divisor}}$$

If fans can be powered while the power to the HECETA 2 is off, the HECETA 2 inputs will provide diode clamping. Limit input current to the Input Current at Any Pin specification shown in the ABSOLUTE MAXIMUM RATINGS section. In most cases, open collector outputs with pull-up resistors inherently limit this current. If this maximum current could be exceeded, either a larger pull-up resistor should be used, or resistors connected in series with the fan inputs.

The Fan Inputs gate an internal 22.5 kHz oscillator for one period of the Fan signal into an 8-bit counter (maximum count = 255). The default divisor, located in the Fan Divisor/RST# Register, is set to 2 (choices are 1, 2, 4, and 8), providing a nominal count of 153 for a 4400 rpm fan with two pulses-per-revolution. Typical practice is to consider 70% of normal RPM a fan failure, at which point the count will be 219.

Determine the fan count according to:

$$\text{Count} = \frac{1.35 \times 10^6}{\text{RPM} \times \text{Divisor}}$$

Note: *Fan 1 and Fan 2-Divisors are programmable via the Fan Divisor/RST# Register. FAN1 and FAN2 inputs can also be programmed to be level-sensitive digital inputs.*

8.0 Temperature Measurement System

The HECETA 2 bandgap-type temperature sensor and ADC perform 9-bit two's-complement conversions of the temperature. A digital 8-bit comparator (Watchdog) is also incorporated to compare the readings to the user-programmable Overtemperature and Hot setpoints, and Hysteresis values.

8.1 Temperature Interrupts

There are two Value RAM Watchdog limits for the Temperature reading that affect the INT# outputs of the HECETA 2. They are Hot Temperature Limit and Hot Temperature Hysteresis Limit. There are three interrupt modes of operation: "One-time Interrupt" mode, "Default Interrupt" mode, and "Comparator" mode. INT# can be programmed for any of these interrupt modes of operation.

8.1.1 Default Interrupt mode

Exceeding the hot temperature limit causes a System Management Interrupt (SMI) that will remain active indefinitely, until reset by reading Interrupt Status Register 1 or cleared by the INT_Clear bit in the Configuration register. Once an Interrupt event has occurred by crossing the Hot Temperature limit, then reset, an Interrupt will occur again once the next temperature conversion has completed. The interrupts will continue to occur in this manner until the temperature goes below the hot temperature hysterisis value.

8.1.2 One-Time Interrupt mode

Exceeding the hot temperature limit causes an SMI that will remain active indefinitely until reset by reading Interrupt Status Register 1 or cleared by the INT_Clear bit in the Configuration register. Once an SMI event occurs by crossing the hot temperature limit, then subsequently reset, an SMI will not occur again until the temperature goes below the hot temperature hysteresis limit.

8.1.3 Comparator mode

Exceeding the hot temperature limit causes the SMI output to go Low (default). SMI will remain low until the temperature goes below the hot temperature limit. Once the temperature goes below the hot temperature limit, SMI will go high.

8.2 Temperature Data Format

Temperature data can be read from the Hot Temperature Set Point and Hot Temperature Hysteresis Set Point registers, and written to the Hot Temperature Set Point, and Hot Temperature Hysteresis registers. Temperature data is represented by an 8-bit, two's complement word with an LSB (Least Significant Bit) equal to 1.0°C:

Temperature	Digital Output	
	Binary	Hex
+125°C	0111 1101	7Dh
+25°C	0001 1001	19h
+1.0°C	0000 0001	01h
0°C	0000 0000	00h
-1.0°C	1111 1111	FFh
-25°C	1110 0111	E7h
-55°C	1100 1001	C9h

The Temperature reading can have a 9-bit format. Eight Most Significant Bits (MBS) of the temperature reading can be found at Value RAM address 28 h. The remainder of the Temperature reading can be found in the Temperature Configuration Register Bit 7.

9.0 Interrupt Inputs

An external interrupt can come from the following sources. While the label suggests a specific type or source of Interrupt, this label is not a restriction on the usage; it could come from any desired source.

9.1 Analog voltage

An interrupt will be generated if an analog voltage High or Low limit has been exceeded. This is generally when a power supply is out of its normal operating range; these limits are set by software.

9.2 Temperature

An interrupt will be generated if a High or a Low Hot Temperature limit has been exceeded.

9.3 Fan speed

An interrupt will be generated if a fan count limit has been exceeded.

9.4 Chassis intrusion

CI (Chassis Intrusion): This is an active high interrupt from any type of device that detects and captures chassis intrusion violations. This could be accomplished mechanically, optically, or electrically, and circuitry external to the HECETA 2 is expected to latch the event.

The design of the HECETA 2 allows this input to go high even with no power applied to the HECETA 2, and no clamping or other interference with the line will occur. This line can also be pulled low for at least 20 ms by the HECETA 2 to reset a typical Chassis Intrusion circuit. Accomplish this reset by setting Bit 5 of the Configuration Register high. The bit in the Register is self-clearing.

Important: The Chassis Intrusion input does **NOT** have a protection diode to Vcc. This can cause the pin to be pulled to ground when the power supply is off, and cause a reset of the chassis intrusion latch.

10.0 Interrupt Outputs

INT#: All System Management Interrupts (SMIs) are indicated in the two Interrupt Status Registers. The INT# has individual mask registers and individual masks for each Interrupt. As described in Section 3.3, this hardware Interrupt line can also be enabled or disabled in the Configuration Register.

11.0 Interrupt Clearing

Reading an Interrupt Status Register will output the contents of the Register, and reset the Register. A subsequent read done before the analog 'round-robin' monitoring loop is complete will indicate a cleared Register. Allow at least 1.5 seconds to allow all Registers to be updated between reads. When the Interrupt Status Register clears, the hardwire interrupt line will also clear until the Registers are updated by the monitoring loop.

The hardware Interrupt lines are cleared with the INT_Clear bit, which is Bit 3 of the Configuration Register, without affecting the contents of the Interrupt (INT#) Status Registers. When this bit is high, the HECETA 2 monitoring loop will stop. It will resume when the bit is low.

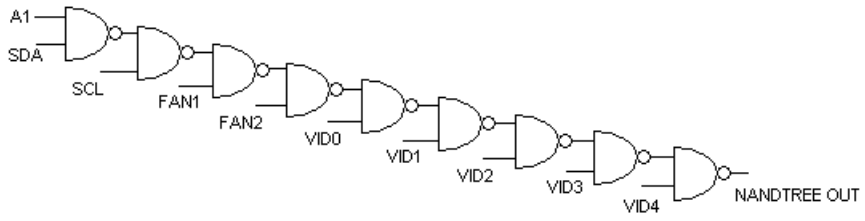
12.0 RST# Output

RST# is intended to provide a master reset to devices connected to this line. Setting Bit 4 in the Configuration Register high outputs at least a 20 ms low on this line, at the end of which Bit 4 in the Configuration Register automatically clears. Again, the label for this pin is only its suggested use. In applications where the RST# capability is not needed, it can be used for any type of digital control that requires a 20 ms active low open drain output.

13.0 NAND Tree Tests

A NAND tree is provided in the HECETA 2 for Automated Test Equipment (ATE) board level connectivity testing. If the user applies a logic one to the NTEST_IN input pin, the device will be in the NAND tree test mode. A0/NTEST_OUT will become the NAND tree output pin. To perform a NAND tree test, all pins included in the NAND tree should be driven high.

Beginning with A1 and working clockwise around the chip, each pin can be toggled and a resulting toggle can be observed on A0/NTEST_OUT.



Allow for a typical propagation delay of 500 Ns.

Note: *To properly implement the NAND tree test on the PCB, no pins listed in the tree should be connected directly to power or ground. If a pin is needed to configure as a permanent low, such as an address, it should be connected to such ground through a low-value resister such as 330 ohms to allow the ATE to drive it high.*

14.0 Registers and RAM

14.1 Address Register

BIT	Name	Read/Write	Description
7-0	Address Pointer	Write	Address of RAM and Registers. See the tables below for detail.

Address Pointer (Power on default 00h):

Registers and RAM	A7 - A0 in hex	Power On Value of Registers: <7:0> in binary
Configuration Register	40h	0000 1000
Interrupt INT# Status Register 1	41h	0000 0000
Interrupt INT# Status Register 2	42h	0000 0000
INT# Mask Register 1	43h	0000 0000
INT# Mask Register 2	44h	0000 0000
Chassis Intrusion Clear Register	46h	0000 0000
VID Register	47h	<7:4> = 0101, <4:0> = VID3 - VID0
Serial Address Register	48h	0010 1101
VID 4 Register	49h	<0>=VID 4
Temperature Configuration Register	4Bh	0000 0001
Value RAM	20 - 3Dh	
Company ID	3Eh	Contains company number
Stepping	3Fh	Contains stepping number

REGISTER 0x40 CONFIGURATION REGISTER

BIT	Name	R/W	Description
0	START	R/W	Logic 1 enables startup of monitor ASIC. Logic 0 places the ASIC in standby mode. Caution: The outputs of the Interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred (see “INT# Clear” bit). At startup, limit checking functions and scanning begins. Note: Set all HIGH and LOW LIMITS into the LANDesk Configuration Manager ASIC prior to turning on this bit. (Powerup default=0)
1	INT# Enable	R/W	Logic 1 enables the INT# output. 1=Enabled 0=Disabled (Powerup Default = 0.)
2	Reserved		
3	INT_Clear	R/W	During Interrupt Service Routine (ISR) this bit-asserted logic 1 clears INT# output without affecting the contents of the Interrupt Status Register. The device will stop monitoring. It will resume after clearing this bit. (Powerup default=1.)
4	RESET#	R/W	Creates a RESET (Active Low) signal for 20 ms. minimum (Powerup default = 0). This bit is cleared once the pulse goes active.
5	Reserved	R/W	Default = 0.
6	CI_Reset	R/W	Logic 1 resets the chassis intrusion pin. (Powerup default = 0.)
7	Initialization	R/W	Logic 1 restores powerup default values to the Configuration register, Interrupt status registers, Interrupt Mask registers, Fan Devisor/RST#/OS# register, and the OS# Configuration/Temperature Resolution register. This bit automatically clears itself since the power on default is zero.

Register 0x41 INTERRUPT STATUS REGISTER 1

Power on default <7:0> = 00 h

BIT	Name	Read/Write	Description
0	+2.5v_Error	Read Only	A one indicates a High or Low limit has been exceeded.
1	Vccp_Error	Read Only	A one indicates a High or Low limit has been exceeded.
2	+3.3v_Error	Read Only	A one indicates a High or Low limit has been exceeded.
3	+5v_Error	Read Only	A one indicates a High or Low limit has been exceeded.
4	Temp_Error	Read Only	A one indicates that a High or a Low Hot Temperature limit has been exceeded. Only 'Default Interrupt' and 'One-Time Interrupt' modes are supported. The mode is set by bit 6 of the Interrupt Mask Register 2.
5	Reserved	Read Only	Undefined.
6	FAN1_Error	Read Only	A one indicates that a fan count limit has been exceeded.
7	FAN2_Error	Read Only	A one indicates that a fan count limit has been exceeded.

Register 0x42 INTERRUPT STATUS REGISTER 2

Power on default <7:0> = 00 h

BIT	Name	Read/Write	Description
0	+12v_Error	Read Only	A one indicates a High or Low limit has been exceeded.
1	-12v/Vccp2_Error	Read Only	A one indicates a High or Low limit has been exceeded.
2	Reserved	Read Only	Undefined.
3	Reserved	Read Only	Undefined.
4	Chassis_Error	Read Only	A one indicates Chassis Intrusion has gone high.
5	Reserved	Read Only	Undefined.
6	Reserved	Read Only	Undefined.
7	Reserved	Read Only	Undefined.

Note: Any time the STATUS Register is read out, the conditions (in other words, Register) that are read are automatically RESET. In the case of the VOLTAGE priority indication, if two or more Voltages were out of LIMITS, then another indication would automatically be generated if it was not handled during the ISR.

In the Control Register, the errant voltage may be disabled, until the operator has time to clear the errant condition or set the limit higher or lower.

Register 0x43 INT# INTERRUPT MASK REGISTER 1

Power on default <7:0> = 00h

BIT	Name	Read/Write	Description
0	+2.5v	Read/Write	A one disables the corresponding interrupt status bit for INT# interrupt.
1	+Vccp	Read/Write	A one disables the corresponding interrupt status bit for INT# interrupt.
2	+3.3v	Read/Write	A one disables the corresponding interrupt status bit for INT# interrupt.
3	+5v	Read/Write	A one disables the corresponding interrupt status bit for INT# interrupt.
4	Temp	Read/Write	A one disables the corresponding interrupt status bit for INT# interrupt.
5	Reserved	Read/Write	Power on default = 0.
6	FAN1	Read/Write	A one disables the corresponding interrupt status bit for INT# interrupt.
7	FAN2	Read/Write	A one disables the corresponding interrupt status bit for INT# interrupt.

Register 0x44 INT# MASK REGISTER 2

Power on default <7:0> = 00h

Bit	Name	Read/Write	Description
0	+12v	Read/Write	A one disables the corresponding interrupt status bit for INT# interrupt.
1	-12v/Vccp2	Read/Write	A one disables the corresponding interrupt status bit for INT# interrupt.
2	Reserved	Read/Write	Power up default set to Low.
3	Reserved	Read/Write	Power up default set to Low.
4	Chs_sec(Chassis Intrusion)	Read/Write	A one disables the corresponding interrupt status bit for INT# interrupt.
5	Reserved	Read/Write	Undefined.
6	Reserved	Read/Write	Undefined.
7	Reset# Enable	Read/Write	A one enables the RESET# in the configuration register.

Register 0x45 RESERVED

BIT	Name	Read/Write	Description
0-7	RESERVED	Read/Write	Undefined (Power On = 00h).

Register 0x46 Chassis Intrusion Clear

BIT	Name	Read/Write	Description
0-6	RESERVED	Read/Write	Undefined (Power On = 00h).
7	Chassis Int Clear	Read/Write	A one outputs a minimum 20 ms active low pulse on the Chassis Intrusion pin. The register bit clears itself once the pulse is output.

Register 0x47h VID REGISTER

Bit	Name	Read/Write	Description
0-3	VID	Read	The VID[3:0] inputs from Pentium® Pro processor power supplies to indicate the operating voltage (for example, 1.5V to 2.9V)
4-5	FAN1 RPM control	Read/Write	FAN1 Speed Control. <3:2> = 00 - divide by 1. <3:2> = 01 - divide by 2. <3:2> = 10 - divide by 4. <3:2> = 11 - divide by 8. If level-sensitive input is selected: • <2> = 1 selects an active-low input (an interrupt will be generated if the FAN1 input is Low) • <2> = 0 selects an active-high input (an interrupt will be generated if the FAN1 input is High).
6-7	FAN2 RPM control	Read/Write	FAN2 Speed Control. <5:4> = 00 - divide by 1. <5:4> = 01 - divide by 2. <5:4> = 10 - divide by 4. <5:4> = 11 - divide by 8. If level-sensitive input is selected: • <2> = 1 selects an active-low input (an interrupt will be generated if the FAN2 input is Low) • <2> = 0 selects an active-high input (an interrupt will be generated if the FAN2 input is High).

Register 0x48h Serial Address Register

BIT	Name	Read/Write	Description
0-7	SMBus Address	Read/Write	SMBus Address (Power On = 01011(A1)(A0))

Register 0x49h VID 4 / Device ID Register

Bit	Name	Read/Write	Description
0	VID 4	Read	VID 4 Input
1-7	Reserved	Read/Write	Default Power On Values = 1000000

Register 0x4Bh Temperature Resolution Register

Power on <7:0> = 01 h

BIT	Name	Read/Write	Description
0	Hot Temperature Interrupt mode select Bit 0	Read/Write	If Bits 0 and Bits 1 of this register are both zero or one, this selects the default interrupt mode, which gives the user an interrupt if the temperature goes above the hot limit. The interrupt will be cleared once the status register is read, but it will again be generated when the next conversion has completed. It will continue to do so until the temperature goes below the ***hysteresis*** limit. A zero on Bit 1 and a one on Bit 0 selects the one-time interrupt mode that gives the user an indefinite interrupt when it goes above the hot limit. The interrupt will be cleared once the status register is read. Another interrupt will not be generated until the temperature first goes below the ***hysteresis*** limit. It will also be cleared if the status register is read. No more interrupts will be generated until the temperature goes above the hot limit again. The corresponding bit will be cleared in the status register every time it is read but may not set again when the next conversion is done.
1	Hot Temperature Interrupt mode select Bit 1	Read/Write	A one on this bit (Bit 1) and a zero on Bit 0 selects the comparator mode. This gives an SMI when the temperature exceeds the hot limit. This SMI remains active until the temperature goes below the ***hot limit (no hysteresis)***, when the SMI will become inactive.
2-6	Reserved	Read/Write	Default = 00000.
7	Temp [0]	Read only	For 8-bit plus sign temperature resolution, <7> = Temp [0] (LSB, 0.5°C).

Registers 0x15h - 0x3Dh Value Ram

Address A7- A0	Description
15h	Manufacturers Test Register
19h	Analog Output
20h	+2.5V
21h	Vccp1
22h	+3.3V
23h	+5V
24h	+12V
25h	+2.5V_Sense /Vccp2
26h	Reserved

Address A7- A0	Description
27h	Temperature reading
28h	FAN1 reading **Note:** *This location stores the number of counts of the internal clock per-revolution.*
29h	FAN2 reading **Note:** *This location stores the number of counts of the internal clock per-revolution.*
2Ah	Reserved
2Bh	+2.5V High Limit
2Ch	+2.5V Low Limit
2Dh	+Vccp1 High Limit
2Eh	+Vccp1 Low Limit
2Fh	+3.3V High Limit
30h	+3.3V Low Limit
31h	+5V High Limit
32h	+5V Low Limit
33h	+12V High Limit
34h	+12V Low Limit
35h	+2.5V_Sense/Vccp2 High Limit
36h	+2.5V_Sense/Vccp2 Low Limit
37h	Reserved
38h	Reserved
39h	Hot Temperature Limit (High)
3Ah	Hot Temperature Hysteresis Limit (Low)
3Bh	FAN1 Fan Count Limit **Note:** *It is the number of counts of the internal clock for the Low Limit of the fan speed.*
3Ch	FAN2 Fan Count Limit **Note:** *It is the number of counts of the internal clock for the Low Limit of the fan speed.*
3Dh	Reserved
3Eh	Company ID number
3Fh	Stepping ID number

Setting all ones to the high limits for voltages and fans (1111 1111 binary for temperature) means interrupts will never be generated except the case when voltages go below the low limits.

Note: *For the high limits of the voltages, the device is doing a greater-than comparison. For the low limits, however, it is doing a less than or equal comparison.*

Manufacturers Test Register - Address 15h

This register should only be used by the manufacturer for testing the ASIC. Reading or writing to this register during normal use may lead to erroneous events.

Analog output - Address 19h

This register will latch an 8-bit value into an R-2R D/A to provide a range of 0-1.25 volts. Accuracy can be +/-5% or more.

Company ID - Address 3Eh

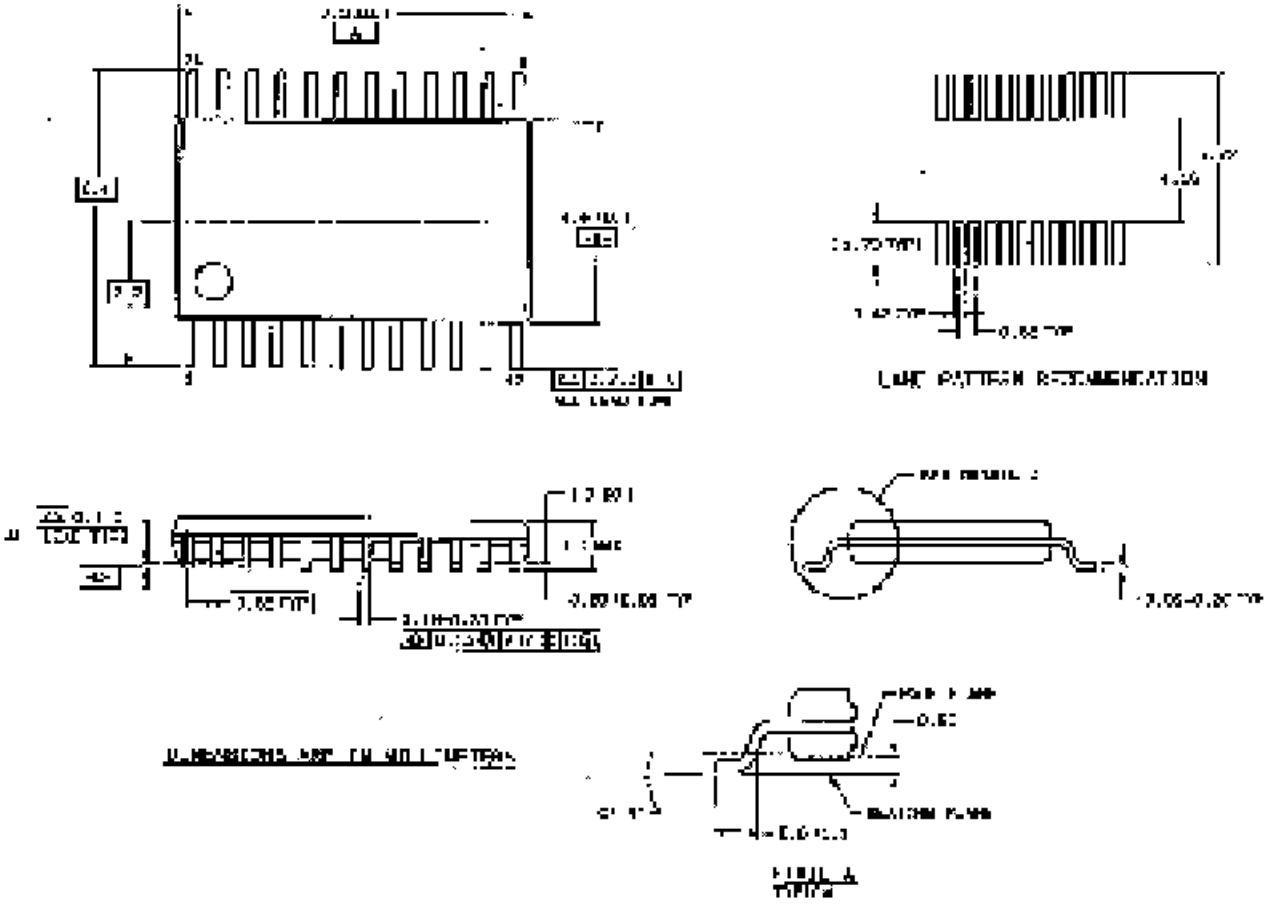
This location will contain the company identification number that will be used by software to determine analog voltage curves. This register is read-only.

Stepping - Address 3Fh

This location will contain the stepping number of the part. This register is read-only.

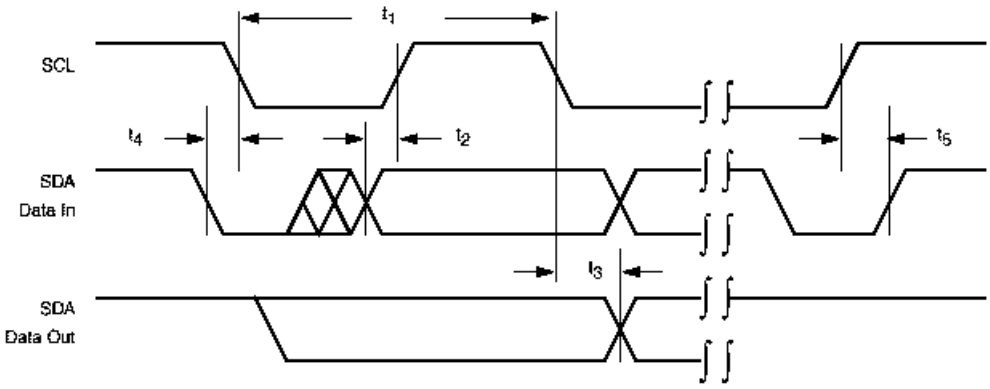
Physical Dimensions

Dimensions listed in inches followed by millimeters.

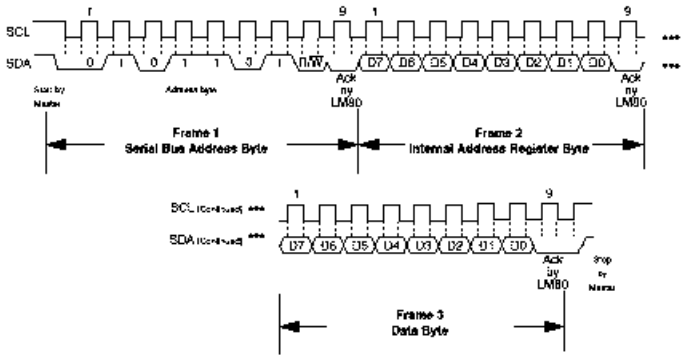


24-Lead TSSOP Package

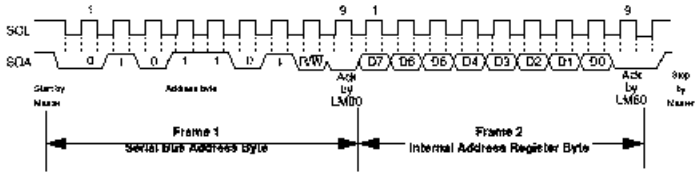
SMBus Timing Diagram



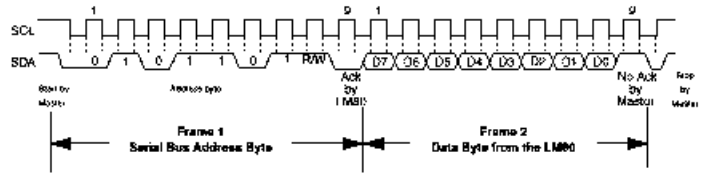
Functional Description



(a) Serial Bus Write to the Internal Address Register followed by the Data Byte



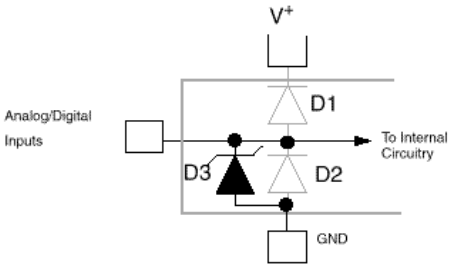
(b) Serial Bus Write to the Internal Address Register only



(c) Serial Bus Read from a Register with the Internal Address Register preset to desired location.

ESD Protection Input Structure (Use this example Method as a reference only!)

diodes are forward biased by more than 50 mV. As an example, if V^+ is 4.50 V_{DC}, input voltage must be ≤ 4.55 V_{DC}, to ensure accurate conversions.



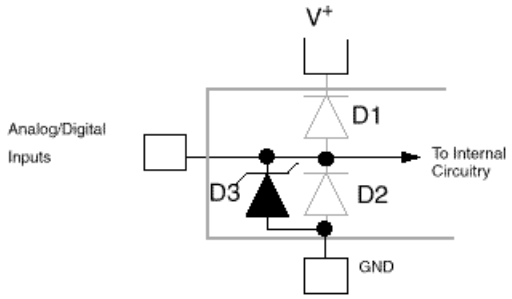
*An x indicates that the diode exists.

Pin Name	D1	D2	D3
CI		x	x
FAN1-FAN2			x
SCL			x
SDA		x	x
RST#/OS#		x	x
NTEST_IN			x

Pin Name	D1	D2	D3
+12,-12,+5,+3.3,+2.5,Vccp			
INT#	x	x	x
A1	x	x	x
A0/NTEST_OUT	x	x	x

Digital Output Load Circuitry (Use this example Method as a reference only!)

diodes are forward biased by more than 50 mV. As an example, if V^+ is 4.50 V_{DC}, input voltage must be ≤ 4.55 V_{DC}, to ensure accurate conversions.

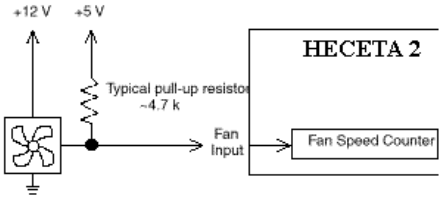


*An x indicates that the diode exists.

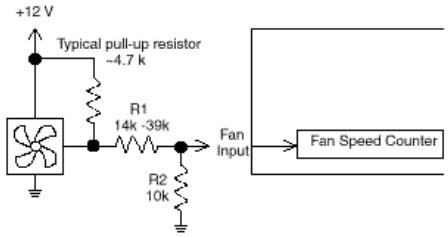
Pin Name	D1	D2	D3
CI		x	x
FAN1-FAN2			x
SCL			x
SDA		x	x
RST#/OS#		x	x
NTEST_IN			x

Pin Name	D1	D2	D3
+12,-12,+5,+3.3,+2.5,Vccp			
INT#	x	x	x
A1	x	x	x
A0/NTEST_OUT	x	x	x

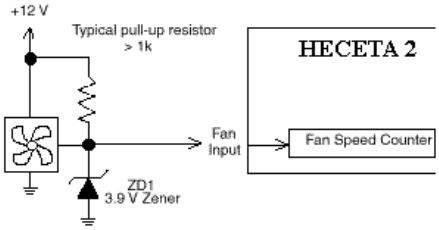
Alternatives for fan inputs



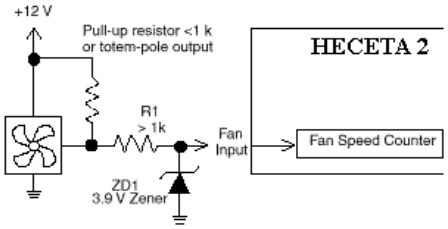
a) Fan With Tach Pull-Up to +5 V



b) Fan With Tach Pull-Up to +12 V, or Totem-Pole Output and Resistor Attenuator



c) Fan With Tach Pull-Up to +12 V and Diode Clamp



d) Fan With Strong Tach Pull-Up or Totem Pole Output and Diode Clamp

Interrupt Structure