Management Hardware Design, Interface and Layout Guidelines

(Heceta Head ASIC = LM-78)

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Version 1.4, May 1997

Revision History

Revision	Date	Who	Description
0.0			Initial document
0.1	4/17/97	Ed Davis	Reformatted document & added cleaner pictures

Estimated time to Complete

Procedure Number	Time (hours)
1	
2	

Table of contents

Introduction

This document provides specific layout considerations that should be followed when incorporating the Heceta Head (level2 ASIC) and its successors interface circuitry on the motherboard.

The guidelines cover the schematic, design, cabling, grounding, termination and board placement, and layout considerations that should be used for the Heceta Head ASIC.

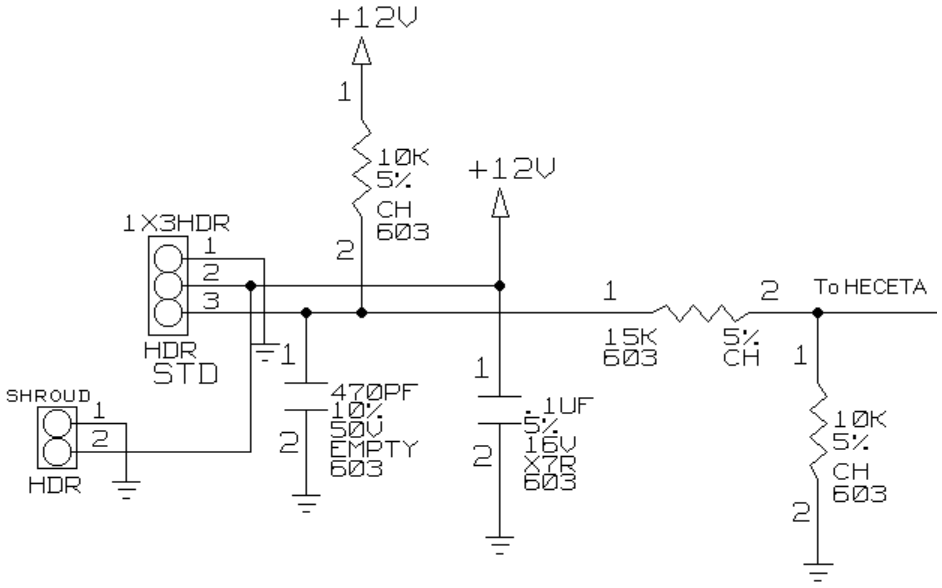
Overview

The typical design should look like the schematic below. Any exceptions and options are noted in the sections that follow.

Schematic design

Fans

There are three fan inputs. If there are less than three fans required in the design, always use the fans beginning at fan 1. (This is due to software detection considerations.) The fans may be 5V or 12V and should be connected exactly as illustrated below:

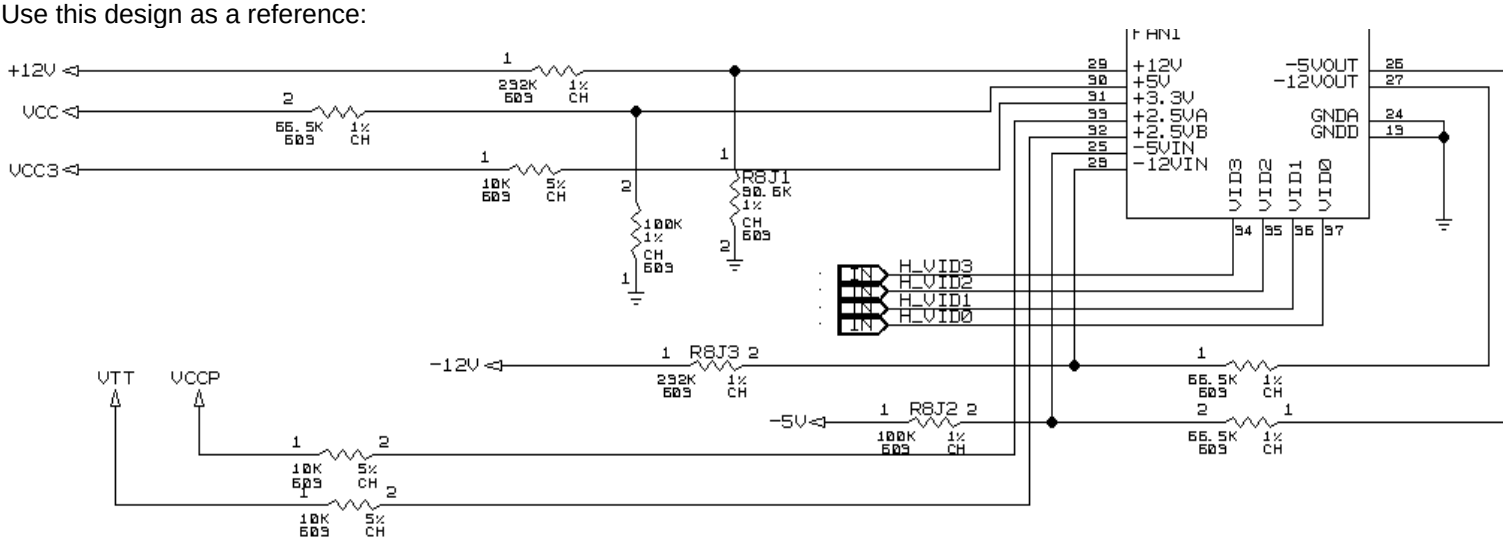


Note: Terminate unused fan inputs to ground using 10K resistors.

Power Supply Monitoring and VID Lines

The Heceta will monitor seven analog inputs. Most of these need voltage dividers to scale them down to the operating range of the Heceta; others need feedback to allow them to monitor negative voltages.

Use this design as a reference:



Power Bypass

I2C lines (SDA, SCL) On earlier version of the LM-78 the A0, A1, the Power Bypass pin contains a protection diode to 5V. When powered down this output drops to about .7V. A buffer gate (like a 7407 or equivalent) should be used to isolate it from POWERGOOD as well as a diode. (See the figure below.)

The I2C bus is optional in designs up to Pentium® Pro processor and 440FX, in newer chipsets, the I2C bus must be connected to the Pentium® II Processor, PIIX4, PIIX5, 440BX, etc. to enable advanced management software. Since they are both I/O pins, they should be pulled up with a 10K to Vcc if not used.

Note: This bus is required if external temperature sensors (for example, LM75 or DS1621) are used other than the sensor internal to the LM-78.

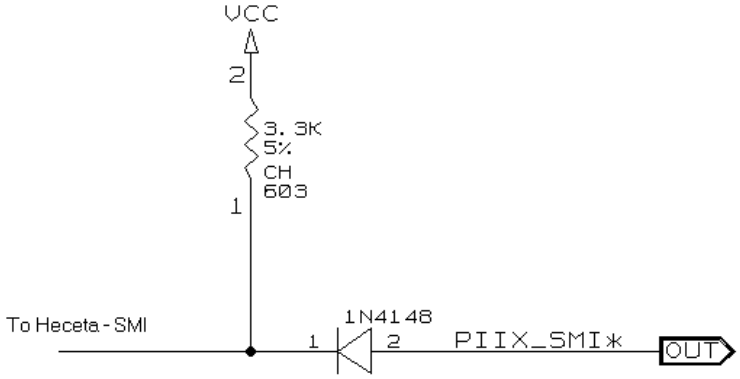
Note also, that in this case the BTI (Board Temperature Interrupt) input would be connected to these external sensors and pulled up with a 10K resistor.

CAUTION: For 307 and 308 Ultra I/O chips, there must be two dedicated GPI/O pins dedicated to SDA and wire OR'ed if dual processors are used or more than one external temperature sensor is used.

The BTI (Board Temperature Interrupt) input should be pulled up with a 10K resistor whether or not it is used.

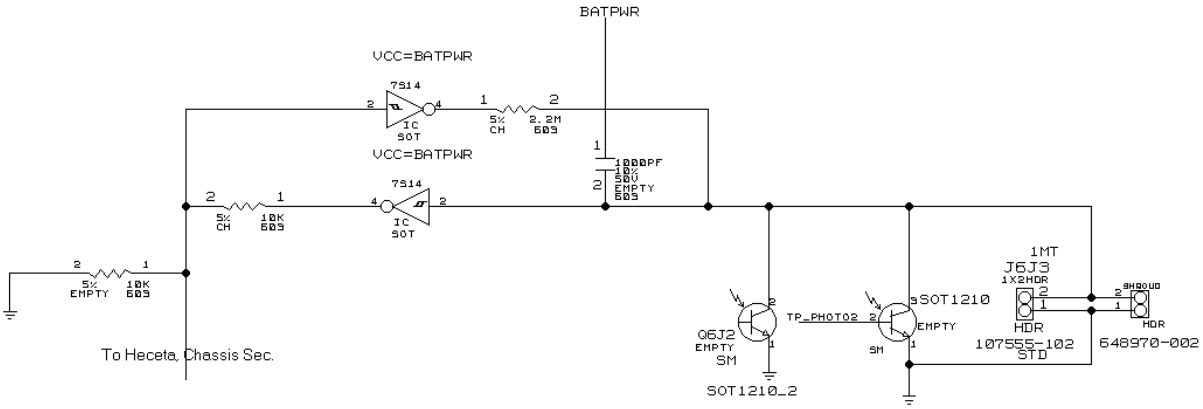
SMI

The SMI output of the Heceta should be coupled to the system through a diode:



Chassis Intrusion

The chassis intrusion circuit should be implemented exactly as shown in the figure below. Note that the TC7S14 parts are NOT Schottky. This is merely Toshiba's designation of a small (SOT-23 sized) 5 pin Low Power CMOS device containing a single gate. (They require about 1 uA to run from 5VSB or VBAT.)



(Chassis optional)

NTEST

NTEST is the output of the NAND tree test function which allows an in-circuit test of the part. None of the pins (except ground) should be directly tied to ground since the ATE needs to drive them.

Fan Cabling

Observe the following guidelines with respect to the fan cabling and connectors:

The fans are three-wire, with a keyed 3 pin connector with pinout, as follows:

Pin	Use
1	Ground
2	+12
3	Tachometer

Cable Length

Each fan cable should be less than or equal to 18 inches.

Placement

Make sure that there's a maximum of 6 inches between drive connectors on the cable. If one drive is placed on the cable, it should be placed at the end of the cable. If a second drive is placed on the same cable, it should be placed on the next closest connector to the end of the cable (6 inches away from the end of the cable).

Grounding

Provide a direct, low-impedance chassis path between the motherboard ground and hard-disk drives.

Motherboard Layout

Observe the following guidelines (with respect to the Heceta Head, LM-78) when laying out the motherboard:

LM-78 Placement

Place the LM-78 component with onboard temperature sensor as close as possible to the hottest elements on the board such as the CPU, even though the LM-78 senses the backplane temperature.

Resistor Location

The termination resistors should be in series and placed as close to the driver of the signals Figure 1. Procedure 3. Series Termination

The resistor values called out in the figure on page are the current recommended series termination resistors for the Heceta Head interface circuitry.

Recommended Termination Resistors

Signal	Resistor	Comments
RESET	22-47 Ω	The RESET Signal comes from the 82371B RSTDRV signal, through a Schmitt trigger.
		Diode to Vcc
SMI_IN#	?	Bypass
SMI_OUT#	?	?

One resistor per cable is recommended for all signals. For signals labeled as 22Ω - 47Ω, the correct value should be determined for each unique motherboard design, based on signal quality.

Signal Line Capacitance

IRQ Pull-Up