# Preboot eXecution Environment (PXE) BIOS Support

## White Paper

## Revision 1.1



**6/9/97**

# Revision History

| Revision | Date | By | Description |
|---|---|---|---|
| 1.0 | 04/18/97 | N Yoke | Initial Release. - NJY |
| 1.1 | 06/09/97 | T. Labatte | Changed Title of White Paper.<br>Changed BIOS Boot Spec from optional to a requirement.<br>Removed requirement to support DMI Vital Product Data Specification. |

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## 1.1 Introduction

The following information helps you provide the system BIOS interfaces and programming for LANDesk® Service Agent integration into the system BIOS. You can also use this document as a guide, along with the other referenced Desktop Management Interface documents, to aid DMI Instrumentation efforts.

## 1.2 Definition of Terms

The following is a definition of the terms used in this document.

| | |
|---|---|
| **DMI** | Desktop Management Interface—See "Desktop Management BIOS Specification" Version 2.0, October 16, 1995 for more details. |
| **LAN** | Local Area Network—A means of interconnection used to allow clients to provide network access. |
| **LAN CONTROLLER** | Local Area Network Controller—A device used to connect a client to the network to provide network access. |
| **PXE** | Preboot eXecution Environment—A DHCP remote boot protocol used to help provide system manageability. |
| **NVRAM** | Non-Volatile RAM—A RAM used to retain programmed information after power is removed from the CPU and main memory. |
| **OPROM** | Option ROM—A ROM that follows the standard interface designs for option ROMs, including ISA, PNP, and PCI. |
| **POWER-UP SIGNAL** | A signal on the motherboard design used to indicate whether system is ready to be powered-up remotely. |
| **RWA** | Remote Wake-up ASIC—This ASIC asserts a power-up and/or wake-up signal when it receives a power-up sequence over the network. |
| **SYSTEM EVENT LOG** | Entity that's used to store critical system status in an area of Non-Volatile RAM. |
| **WAKE-UP SIGNAL** | A signal on the motherboard design used to indicate whether the system is ready to be woken-up remotely. |

## 1.3 Required Interfaces

The following information provides details for integrating PXE support OPROM binaries into the system BIOS and explains the implementation details of the system BIOS PXE support. Support in system BIOS to:

- Provide full PNP BIOS Specification Version 1.0A compliance, specifically the programmatic and OPROM interfaces.
- Provide full PCI Local Bus Specification Revision 2.1 and PCI BIOS Specification Revision 2.1 compliance, specifically the programmatic and OPROM interfaces.
- Allow legacy remote boot via INT 18h hooking.
- Provide status on the Remote Wake ASIC (RWA) to determine how the system powered on.
- Provide full DM BIOS compliance according to the Version 2.0 (or above) specification referred to above.

- Provide required BIOS Boot Spec (BBS) 1.01 compliance. This means that the OPROM PXE binary code should be written to support BBS and the legacy mode of Remote Boot operation.
- Provide PXE OPROM during POST-Time (Pre-Boot) for integrated LAN controller inclusion in the motherboard design.

## 1.4 PXE OPROM BIOS Integration

This integration is optional, depending on the integrated LAN controller inclusion in the motherboard design. This integration is system-BIOS specific and depends on the manner in which the system BIOS handles integrated peripherals. The integrated OPROM should be handled just like the non-integrated add-in card OPROMs.

## 1.5 Remote Wake-up ASIC Interface

This support is defined by:

- Check for Power On LAN Enabled. This involves determining if the RWA is stuffed (read a General Purpose IO bit) and reading a CMOS RAM (also known as a battery backed up RAM) bit to see if this feature is enabled.

  This feature should always be enabled and not have a setup option. An exception is when the hardware does not filter wake-up signals from the RWA to the Resume/Power-up input (of the motherboard circuitry that handles this signal, usually a Super IO part or South Bridge) when power is already on.

  In other words, if the signal only supports Power-up but the event is not conditioned by Power already being on then this needs to be taken into account. Thus, under these conditions, if enabled, this functionality should be enabled in the Resume/Power-up Input Motherboard Circuitry (RIMC) initialization.
- Store RIMC status in the Extended BIOS Data Area (EBDA) or some other BIOS storage region. We recommend that the EBDA be used, since EBDA is automatically cleared on power-up or reset. Before video initialization, read the RIMC status and store in a byte in the EBDA. This is usually necessary since these types of RIMC status bits are cleared when read.
- Support “Determine System Wake-up” API. This function returns a value representing which event caused the system to power up and reads the value of the RIMC status stored in the EBDA.

  INT 15h

  Input: AX = 2307h

  BX = 5755h

  Output: CL = 06h Power Switch

  05h LAN RWA

  04h COM 1 Modem Ring

  03h Reserved for APM Timer Wake-up

  NC = No error