PIC16F83 → PIC16F84A Migration

DEVICE MIGRATIONS

This document is intended to describe the functional differences and the electrical specification differences that are present when migrating from one device to the next. Table 1-1 shows the considerations that must be taken into account when migrating from the PIC16F83 to the PIC16F84A. Table 2 shows electrical and timing differences.

Note:	Even though compatible devices are tested to the same electrical specifications, the device characteristics may be different from each other (due to process differences). These process differences should have no effect on systems that were designed well within the device specifications. For systems that operate close to the device specifications, process differences may cause the device to behave differently.

Note:	Even though the user has made no changes to the oscillator circuit, oscillator operation should be verified to ensure that it starts and performs as expected. Adjusting the loading capacitor values and /or the oscillator mode may be required.

TABLE 1: PIC16F83 → PIC16F84A FUNCTIONAL DIFFERENCES

No.	Module	Differences from PIC16F83	H/W	S/W
1	Memory	Program Memory (FLASH): The PIC16F83 has 512 words. The PIC16F84A has 1024 words.	—	Yes
		Data Memory (RAM): The PIC16F83 has 36 bytes. The PIC16F84A has 68 bytes.	—	Yes
2	Oscillator	The PIC16F83 oscillator can run up to 10MHz. The PIC16F84A oscillator can run up to 20MHz.	Yes	Yes

Legend: H/W - Issues may exist with regard to the application circuit.
S/W - Issues may exist with regard to the user program.

MEMORY

Program addressing and paging in the PIC16F83 is upwardly compatible with the PIC16F84A. No code changes are required.

All SFR's remain at the same addresses, performing the same functions for both devices. Data space addressing and banking in the PIC16F83 is upwardly compatible with the PIC16F84A. No code changes are required.

OSCILLATOR

The PIC16F84A can use crystals up to 20 MHz, resulting in double the execution speed. No changes to the code, other than for timing concerns, are required. No changes to the configuration word are required. The crystal loading capacitors may need to be adjusted for the higher speed crystal, but verifying oscillator operation at the same speed is already recommended for the transition from the PIC16F83 to the PIC16F84A.

TABLE 2: PIC16F83 → PIC16F84A SPECIFICATION DIFFERENCES

Param No.	Symbol	Characteristic		PIC16F83			PIC16F84A			Units
				Min	Typ†	Max	Min	Typ†	Max	
Core										
	FOSC	Eternal CLKIN Frequency (HS mode) Oscillator Frequency (HS mode)		DC 1	— —	10 10	DC 1	— —	**20** **20**	MHz MHz
D001 D001A	VDD VDD	Supply Voltage (XT, RC, LP modes) Supply Voltage (HS mode)		4.0 4.5	— —	6.0 6.0	4.0 4.5	— —	**5.5** **5.5**	V V
30	TmcL	$\overline{MCLR}$ pulse width (low)		1	—	—	**2**	—	—	µS
D004A	SVDD	VDD rise rate to ensure internal Power-on Reset signal (PWRT disabled)		N/A	N/A	N/A	**TBD**	—	—	V/mS
D010A	IDD	Supply current during FLASH programming (Fosc = 4.0 MHz, VDD = 5.5V)		—	7.3	10	—	**3.0**	10	mA
D013	IDD	Supply Current HS mode (VDD = 5.5V)	PIC16F83 (FOSC = 10 MHz)	—	5	10				mA
			PIC16F84A (FOSC = 20 MHz)				—	**10**	**20**	mA
D021	IPD	Power down current (VDD = 4.0V, WDT disabled)	Commercial	—	1.0	14	—	**TBD**	**1.0[2]**	µA
D021A			Industrial	—	1.0	14	—	**TBD**	**1.0[2]**	µA
D022	ΔIWDT	Module Differential Current Watchdog Timer	Commercial	N/A	N/A	N/A	—	**6.0**	**20**	µA
			Extended	N/A	N/A	N/A	—	—	**25**	µA
	VIH	Input High Voltage I/O Ports								
D040		with TTL buffer (4.5V<VDD<5.5V)[1]		2.4	—	VDD	**2.0**	—	VDD	V
D040A		(VDD = Entire Range)[1]		0.48VDD	—	VDD	**0.25VDD**	—	VDD	V
D041		with Schmitt Trigger		0.45VDD	—	VDD	**0.8VDD**	—	VDD	V
D042		$\overline{MCLR}$, RA4/T0CKI OSC1 (RC mode)		0.85VDD	—	VDD	**0.8VDD**	—	**VDD**	V
D043		OSC1 (XT, HS and LP modes)		0.7VDD	—	VDD	0.7VDD	—	VDD	V
D043A		OSC1 (RC mode)		N/A	N/A	N/A	**0.9VDD**	—	**VDD**	V
D050	VHYS	Hysteresis of Schmitt Trigger inputs		TBD	—	—	—	**0.1**	—	V
EEPROM Data Memory										
D121	VDRW	VDD for read/write		VMIN	—	6.0	VMIN	—	**5.5**	V
D122	TDEW	Erase/Write Cycle Time		—	10	20	—	**4**	**8**	mS
FLASH Program Memory										
D131	VPR	VDD for read		VMIN	—	6.0	VMIN	—	**5.5**	V
D133	TDEW	Erase/Write Cycle Time		—	10	20	—	**4**	**8**	mS

†Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The user may choose the better of the two specifications.

2: This specification has changed since the last data sheet or errata was published as of 5/99.

NOTES:

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