PIC16C72 → PIC16C72A Migration

DEVICE MIGRATIONS

This document is intended to describe the functional differences and the electrical specification differences that are present when migrating from one device to the next. Table 1-1 shows functional differences, while Table 1-2 shows electrical and timing differences.

Note:	Even though compatible devices are specified to be tested to the same electrical specification, the device characteristics may be different from each other (due to process differences). For systems that were designed to the device specifications, these process differences should not cause any issues in the application. For systems that did not tightly meet the electrical specifications, the process differences may cause the device to behave differently in the application.

Note:	While there are no functional or electrical changes to the device oscillator specifications, the user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or the oscillator mode may be required.

TABLE 1: PIC16C72 → PIC16C72A FUNCTIONAL DIFFERENCES

No.	Module	Differences from PIC16C72	H/W	S/W	Prog.
7	SSP	Supports all four SPI modes. (Now uses SSP vs BSSP module.) See SSP module in the PICmicro® Mid-Range Reference Manual, (DS33023A).	—	Yes	—

Legend: H/W - Issues may exist with regard to the application circuits.
S/W - Issues may exist with regard to the user program.
Prog - Issues may exist when writing the program to the controller.

TABLE 2: PIC16C72 → PIC16C72A SPECIFICATION DIFFERENCES

Param No.	Symbol	Characteristic		PIC16C72			PIC16C72A			Unit
				Min	Typ†	Max	Min	Typ†	Max	
Core										
D005	VBOR	Brown-out Reset Voltage		3.7	4.0	4.3	**3.65**	—	**4.35**	V
D022	ΔIWDT	Watchdog Module Differential Current		—	—	—	—	**6.0**	**20**	µA
D023/ **D022A**	ΔIBOR	Brown-Out Detect Module Differential Current		— —	350 —	425 —	— —	— **TBD**	— **200**	µA µA
D150†	VOD	Open-Drain High Voltage on RA4		—	—	14.0	—	—	**8.5**	V
A/D Converter										
130	TAD	A/D Clock Period A/D RC clock mode	PIC16LCXX	2.5	6.0	9.0	**3.0**	6.0	9.0	µS
131	TCNV	Conversion time**(2)** (not including S/H time)		—	9.5**(3)**	—	**11(4)**	—	**11(4)**	TAD
SSP in SPI mode										
71	TscH	SCK input high time (slave mode)	**Continuous**	T_{CY} + 20	—	—	**1.25T_{CY} + 30**	—	—	ns
71A			Single Byte				**40**	—	—	ns
72	TscL	SCK input low time (slave mode)	**Continuous**	T_{CY} + 20	—	—	**1.25T_{CY} + 30**	—	—	ns
72A			Single Byte				**40**	—	—	ns
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge		50	—	—	**100**	—	—	ns
73A(5)	TB2B	Last clock edge of Byte1 to the 1st clock edge of Byte2		—	—	—	**1.5T_{CY} + 40**	—	—	ns
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		50	—	—	**100**	—	—	ns
75	TdoR	SDO data output rise time	PIC16CXX	—	10	25	—	10	25	ns
			PIC16LCXX				—	**20**	**45**	ns
78	TscR	SCK output rise time (master mode)	PIC16CXX	—	10	25	—	10	25	ns
			PIC16LCXX				—	**20**	**45**	ns
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge	PIC16CXX	—	—	50	—	—	50	ns
			PIC16LCXX				—	—	**100**	ns
82	**TssL2doV**	SDO data output valid after $\overline{SS}$ falling edge	PIC16CXX	—	—	—	—	—	**50**	ns
			PIC16LCXX	N/A	N/A	N/A	—	—	**100**	ns
83	TscH2ssH, TscL2ssH	$\overline{SS}$ ↑ after SCK edge		—	—	50	**1.5T_{CY} + 40**	—	—	ns

†Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When BOR is enabled, the device will operate correctly above the V_{BOR} voltage trip point.
2: ADRES register may be read on the following TCY cycle.
3: This is the time that the actual conversion requires.
4: This is the time from when the GO/$\overline{DONE}$ bit is set to when the conversion result appears in ADRES.
5: Specification 73A is only required if specifications 71A and 72A are used.

NOTES:

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