PIC16C774

PIC16C774 Rev. A Silicon Errata Sheet

The PIC16C774 (Rev. A) parts you have received conform functionally to the Device Data Sheet (DS30275**A**), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC16C774 silicon.

1. Module: RESET

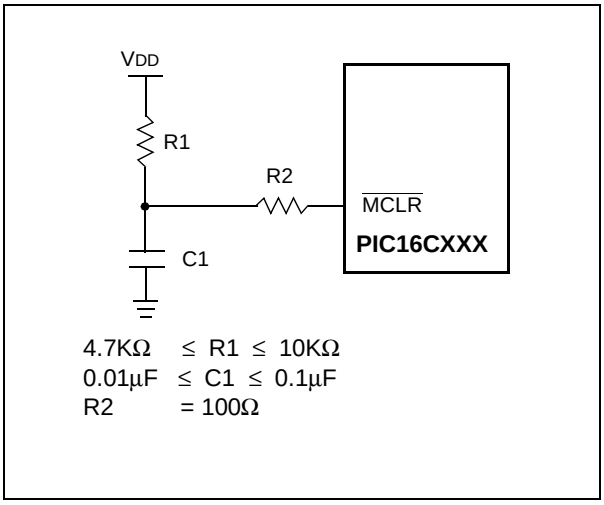
   The minimum specification for the $\overline{\text{MCLR}}$ must be met in order to RESET the PIC16CXXX. If a $\overline{\text{MCLR}}$ pulse occurs that is less that the minimum specification (parameter #30), improper device operation can occur.

   If the minimum specification cannot be met, then an external circuit must be used to insure that any pulse width less than the specification will be filtered before it reaches the $\overline{\text{MCLR}}$ pin.

   Work Around

   A possible circuit is shown in Figure 1. Proper design validation needs to be done to ensure desire operation over the applications operating conditions.

FIGURE 1: $\overline{\text{MCLR}}$ EXTERNAL CIRCUIT



Note: As with any windowed EPROM device, please cover the window at all times, except when erasing.

2. Module: OSCILLATOR

   The Oscillator Start-up Timer (TOST) delay may not occur when the device wakes-up from sleep.

   Figure 2 shows the start-up of the crystal after the event that causes the device to wake up from sleep mode (as specified in device data sheet). The start-up time (TOST) may not occur.

   The events that wake-up the device from sleep are:

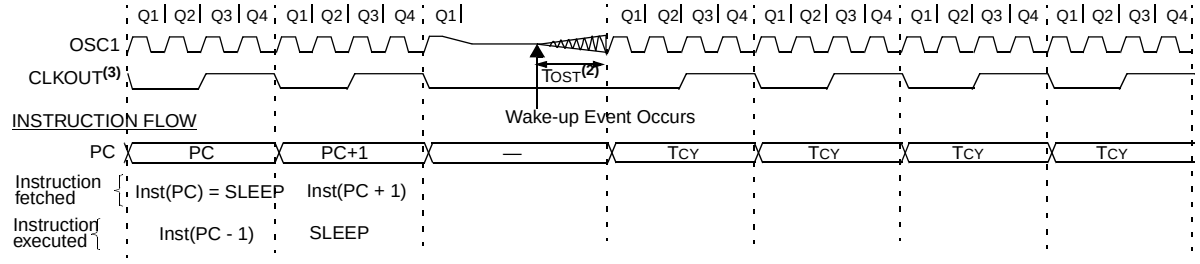
   - An interrupt
   - A WDT overflow (wake-up)
   - A Brown-out Reset
   - A $\overline{\text{MCLR}}$ reset

   In applications where time based measurements are started immediately after wake-up from sleep, the suggested work around should be implemented.

Work Around

After the SLEEP instruction, do a software delay of 256 TCY (same as 1024 TOSC). At the Reset and Interrupt vector addresses, test to see if the device woke from sleep (the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits), and if the device did wake from sleep, ensure that the total cycle delay is 256 TCY.

FIGURE 2: WAKE-UP FROM SLEEP



Note 1: For TOST delay to be enabled, the XT, HS or LP oscillator mode must be selected.
2: TOST = 1024TOSC. This delay may not occur and every valid clock edge will generate internal device clocks.
3: CLKOUT is not available in these osc modes, but shown here for timing reference.

3. Module: TMR1

   When operating in external clock mode (TMR1CS is set), reading either of the timer 1 registers (TMR1H or TMR1L) may cause the timer not to increment as expected. This occurs for both synchronous and asynchronous inputs.

   The scenarios which display this are:

   - When a read operation of the TMR1H register occurs, the TMR1L register may not increment.
   - When a read operation of the TMR1L register occurs, the TMR1H register may not increment. This improper operation is only an issue when the TMR1L register increments from FFh to 00h (FFh → 00H) during the read of the TMR1L register.

   Work Around

   Do not read either the TMR1H or the TMR1L registers when operating in external clock mode (TMR1CS is set). If the application needs to read the 16-bit counter, evaluate if this function can be moved to the TMR0 or one of the other timer resources on the device.

4. Module: MSSP- SPI™ Mode

   The SDI pin cannot be used as a general purpose output by clearing the TRIS bit when the MSSP module is in SPI mode.

   Work Around

   None for current silicon revision.

5. Module: V_{REF}

   a. The operating voltage range for VRL is $V_{DD} \geq$ 3.0V. (See parameter D400)

      Work Around

      None.

   b. The maximum output voltage for VRL is 2.25V. The minimum output voltage for VRL is 1.8V. The maximum output voltage for VRH is 4.5V. The minimum output voltage for VRH is 3.7V. (See parameter D400)

      Work Around

      None.

   c. The VRH and VRL outputs may have an output voltage fluctuation that is typically 50mV p-p.

      Work Around

      Connecting a 1µF capacitor to each voltage reference pin that is used will reduce the fluctuations, if present.

6. Module: 12-bit A/D Converter

   The maximum integral error specification for the A/D converter (parameter A03) is +/-3 LSb.

   The maximum offset error specification for the A/D converter (parameter A06) is +/-5 LSb.

   The maximum integral error specification (parameter A03) may be exceeded when either of the V_{REF} module outputs is used as a reference for the A/D converter.

   The operating voltage range for the A/D converter is $3.5V \leq V_{DD} \leq 5.5V$.

   Work Around

   None.

7. Module: LVD

The minimum levels (parameter D420) specified for the LVD module differ from the Device Data Sheet as follows:

Work Around

None.

TABLE 15-3 ELECTRICAL CHARACTERISTICS: LVD

DC CHARACTERISTICS	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC spec Section 15.1 and Section 15.2.

Param No.	Characteristic		Symbol	Min	Typ†	Max	Units	Conditions
D420	LVD Voltage	LVV = 0100		**2.25**	2.58	2.66	V	
		LVV = 0101		**2.44**	2.78	2.86	V	
		LVV = 0110		**2.55**	2.89	2.98	V	
		LVV = 0111		**2.76**	3.1	3.2	V	
		LVV = 1000		**3.04**	3.41	3.52	V	
		LVV = 1001		**3.25**	3.61	3.72	V	
		LVV = 1010		**3.35**	3.72	3.84	V	
		LVV = 1011		**3.53**	3.92	4.04	V	
		LVV = 1100		**3.72**	4.13	4.26	V	
		LVV = 1101		**3.89**	4.33	4.46	V	
		LVV = 1110		**4.17**	4.64	4.78	V	
D421	Supply Current		ΔILVD	—	10	20	µA	
D422*	LVD Voltage Drift Temperature coefficient		TCVOUT	—	15	50	ppm/°C	
D423*	LVD Voltage Drift with respect to VDD Regulation		ΔVLVD/ ΔVDD	—	—	50	µV/V	
D424*	Low-voltage Detect Hysteresis		VLHYS	TBD	—	100	mV	

* These parameters are characterized but not tested.

Note 1: Production tested at Tamb = 25°C. Specifications over temperature limits ensured by characterization.

8. Module: BOR

The maximum levels specified (parameter D005) for the BOR module differ from the Device Data Sheet as follows:

Work Around

None.

TABLE 15-4 ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC spec Section 15.1 and Section 15.2.					
Param No.	**Characteristic**		**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D005	BOR Voltage	BORV1:0 = 11	VBOR	1.8	2.58	**2.8**	V	
		BORV1:0 = 10		2.0	2.78	**2.9**		
		BORV1:0 = 01		3.6	4.33	**4.45**		
		BORV1:0 = 00		4.0	4.64	**4.85**		
D006*	BOR Voltage Drift Temperature coefficient		TCVOUT	—	15	50	ppm/°C	
D006A*	BOR Voltage Drift with respect to VDD Regulation		ΔVBOR/ ΔVDD	—	—	50	μV/V	
D007	Brown-out Hysteresis		VBHYS	TBD	—	100	mV	
D022A	Supply Current		ΔIBOR	—	10	TBD	μA	

* These parameters are characterized but not tested.

Note 1: Production tested at TAMB = 25°C. Specifications over temperature limits ensured by characterization.

9. Module: PORTE

The minimum VIH specification for PORTE (parameter D040) is 2.4 volts.

Work Around

None.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS30275**A**), the following clarifications and corrections should be noted.

The typical A/D converter supply current (parameter D026) should be the value indicated in Table 15-1 and Table 15-2 below.

15.1 DC Characteristics: PIC16C77X (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	4.0	—	5.5	V	XT, RC and LP osc configuration
D001A			4.5	—	5.5	V	HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	—	1.5	—	V	
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	—	VSS	—	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	—	—	V/ms	See section on Power-on Reset for details. PWRT enabled
D010	Supply Current (Note 2)	IDD	—	2.7	5	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 5.5V (Note 4)
D013			—	13.5	30	mA	HS osc configuration FOSC = 20 MHz, VDD = 5.5V
D020	Power-down Current (Note 3)	IPD	—	1.5	16	µA	VDD = 4.0V, -0°C to +70°C
D020A			—	1.5	19	µA	VDD = 4.0V, -40°C to +85°C
	Module Differential Current (Note 5)						
D021	Watchdog Timer	ΔIWDT	—	6.0	20	µA	VDD = 4.0V
D023B*	Bandgap voltage generator	ΔIBG[6]	—	40µA	TBD	µA	
D025*	Timer1 oscillator	ΔIT1OSC	—	5	9	µA	VDD = 4.0V
D026*	A/D Converter	ΔIAD	—	**70**	—	µA	VDD = 5.5V, A/D on, not converting

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD.
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: The Δ current is the additional current consumed when the peripheral is enabled. This current should be added to the base (IPD or IDD) current.

6: The bandgap voltage reference provides 1.22V to the VRL, VRH, LVD and BOR circuits. When calculating current consumption, use the following formula: ΔIVRL + ΔIVRH + ΔILVD + ΔIBOR + ΔIBG. Any of the ΔIVRL, ΔIVRH, ΔILVD or ΔIBOR can be 0.

15.2 DC Characteristics:PIC16LC77X-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	2.5	—	5.5	V	LP, XT, RC osc configuration (DC - 4 MHz)
D002*	RAM Data Retention Voltage (Note 1)	VDR	—	1.5	—	V	
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	—	VSS	—	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	—	—	V/ms	See section on Power-on Reset for details. PWRT enabled
D010	Supply Current (Note 2)	IDD	—	2.0	3.8	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 3.0V (Note 4)
D010A			—	22.5	48	µA	LP osc configuration FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D020	Power-down Current (Note 3)	IPD	—	0.9	5	µA	VDD = 3.0V, 0°C to +70°C
D020A			—	0.9	5	µA	VDD = 3.0V, -40°C to +85°C
	Module Differential Current (note5)						
D021	Watchdog Timer	ΔIWDT	—	6	20	µA	VDD = 3.0V
D025*	Timer1 oscillator	ΔIT1OSC	—	1.5	3	µA	VDD = 3.0V
D026*	A/D Converter	ΔIAD	—	**70**	—	µA	VDD = 5.5V, A/D on, not converting

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD.
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

5: The Δ current is the additional current consumed when the peripheral is enabled. This current should be added to the base (IPD or IDD) current.

The typical Vref line regulation should be the value specified in Table 15-2 below.

TABLE 15-2 ELECTRICAL CHARACTERISTICS: VREF

DC CHARACTERISTICS	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC spec Section 15.1 and Section 15.2.						
Param No.	**Characteristic**	**Symbol**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D400	Output Voltage	VRL	2.0	2.048	2.1	V	VDD ≥ 2.5V
		VRH	4.0	4.096	4.2	V	VDD ≥ 4.5V
D401A	VRL Quiescent Supply Current	ΔIVRL	—	70	TBD	µA	No load on VRL.
D401B	VRH Quiescent Supply Current	ΔIVRH	—	70	TBD	µA	No load on VRH.
D402	Ouput Voltage Drift	TCVOUT	—	15*	50*	ppm/°C	Note 1
D404	External Load Source	IVREFSO	—	—	5*	mA	
D405	External Load Sink	IVREFSI	—	—	-5*	mA	
D406	Load Regulation	ΔVOUT/ ΔIOUT	—	1	TBD*	mV/mA	Isource = 0 mA to 5 mA
			—	1	TBD*		Isink = 0 mA to 5 mA
D407	Line Regulation	ΔVOUT/ ΔVDD	—	**1**	—	mV/V	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Production tested at TAMB = 25°C. Specifications over temp limits ensured by characterization.

The maximum LVD supply current (parameter D421) should be the value indicated in Table 15-3 below.

TABLE 15-3 ELECTRICAL CHARACTERISTICS: LVD

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC spec Section 15.1 and Section 15.2.					
Param No.	**Characteristic**		**Symbol**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D420	LVD Voltage	LVV = 0100		2.5	2.58	2.66	V	
		LVV = 0101		2.7	2.78	2.86	V	
		LVV = 0110		2.8	2.89	2.98	V	
		LVV = 0111		3.0	3.1	3.2	V	
		LVV = 1000		3.3	3.41	3.52	V	
		LVV = 1001		3.5	3.61	3.72	V	
		LVV = 1010		3.6	3.72	3.84	V	
		LVV = 1011		3.8	3.92	4.04	V	
		LVV = 1100		4.0	4.13	4.26	V	
		LVV = 1101		4.2	4.33	4.46	V	
		LVV = 1110		4.5	4.64	4.78	V	
D421	Supply Current		ΔILVD	—	10	**TBD**	µA	
D422*	LVD Voltage Drift Temperature coefficient		TCVOUT	—	15	50	ppm/°C	
D423*	LVD Voltage Drift with respect to VDD Regulation		ΔVLVD/ ΔVDD	—	—	50	µV/V	
D424*	Low-voltage Detect Hysteresis		VLHYS	TBD	—	100	mV	

* These parameters are characterized but not tested.

Note 1: Production tested at Tamb = 25°C. Specifications over temperature limits ensured by characterization.

The maximum BOR supply current (parameter D022A) should be the value indicated in Table 15-4 below.

TABLE 15-4 ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC spec Section 15.1 and Section 15.2.					
Param No.	**Characteristic**		**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D005	BOR Voltage	BORV1:0 = 11	VBOR	2.5	2.58	2.66	V	
		BORV1:0 = 10		2.7	2.78	2.86		
		BORV1:0 = 01		4.2	4.33	4.46		
		BORV1:0 = 00		4.5	4.64	4.78		
D006*	BOR Voltage Drift Temperature coefficient		TCVOUT	—	15	50	ppm/°C	
D006A*	BOR Voltage Drift with respect to VDD Regulation		ΔVBOR/ ΔVDD	—	—	50	μV/V	
D007	Brown-out Hysteresis		VBHYS	TBD	—	100	mV	
D022A	Supply Current		ΔIBOR	—	10	**TBD**	μA	

* These parameters are characterized but not tested.

Note 1: Production tested at TAMB = 25°C. Specifications over temperature limits ensured by characterization.

NOTES:

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