

## PIC16C773 Rev. A Silicon Errata Sheet

The PIC16C773 (Rev. A) parts you have received conform functionally to the Device Data Sheet (DS30275A), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC16C773 silicon.

### 1. Module: RESET

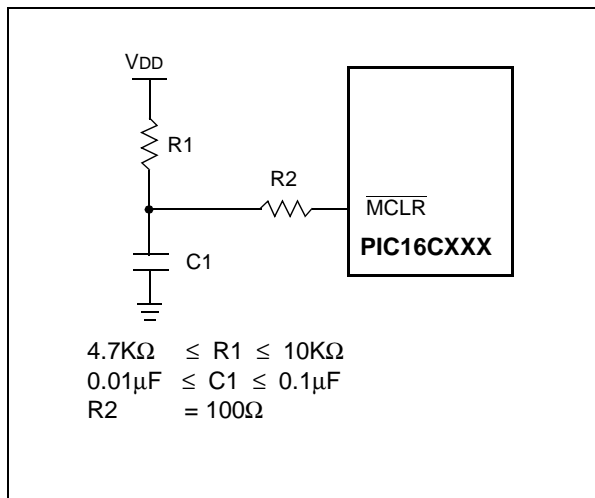
The minimum specification for the  $\overline{\text{MCLR}}$  must be met in order to RESET the PIC16CXXX. If a  $\overline{\text{MCLR}}$  pulse occurs that is less than the minimum specification (parameter #30), improper device operation can occur.

If the minimum specification cannot be met, then an external circuit must be used to insure that any pulse width less than the specification will be filtered before it reaches the  $\overline{\text{MCLR}}$  pin.

#### Work Around

A possible circuit is shown in Figure 1. Proper design validation needs to be done to ensure desired operation over the applications operating conditions.

**FIGURE 1:  $\overline{\text{MCLR}}$  EXTERNAL CIRCUIT**



**Note:** As with any windowed EPROM device, please cover the window at all times, except when erasing.

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## 2. Module: OSCILLATOR

The Oscillator Start-up Timer (TOST) delay may not occur when the device wakes-up from sleep.

Figure 2 shows the start-up of the crystal after the event that causes the device to wake up from sleep mode (as specified in device data sheet). The start-up time (TOST) may not occur.

The events that wake-up the device from sleep are:

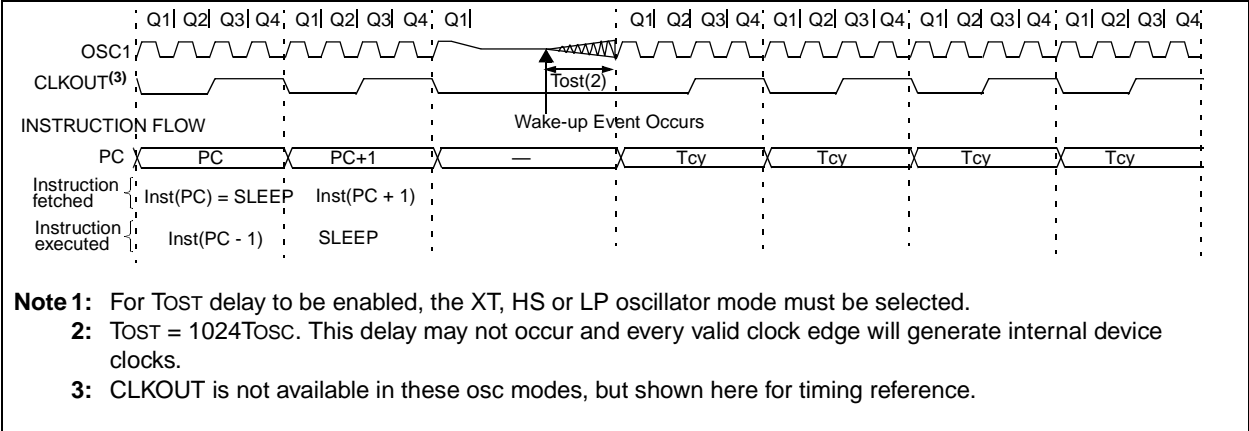
- An interrupt
- A WDT overflow (wake-up)
- A Brown-out Reset
- A  $\overline{\text{MCLR}}$  reset

In applications where time based measurements are started immediately after wake-up from sleep, the suggested work around should be implemented.

### Work Around

After the SLEEP instruction, do a software delay of 256 T<sub>cy</sub> (same as 1024 T<sub>osc</sub>). At the Reset and Interrupt vector addresses, test to see if the device woke from sleep (the  $\overline{\text{TO}}$  and  $\overline{\text{PD}}$  bits), and if the device did wake from sleep, ensure that the total cycle delay is 256 T<sub>cy</sub>.

**FIGURE 2: WAKE-UP FROM SLEEP**



### 3. Module: TMR1

When operating in external clock mode (TMR1CS is set), reading either of the timer 1 registers (TMR1H or TMR1L) may cause the timer not to increment as expected. This occurs for both synchronous and asynchronous inputs.

The scenarios which display this are:

- When a read operation of the TMR1H register occurs, the TMR1L register may not increment.
- When a read operation of the TMR1L register occurs, the TMR1H register may not increment. This improper operation is only an issue when the TMR1L register increments from FFh to 00h (FFh → 00h) during the read of the TMR1L register.

#### Work Around

Do not read either the TMR1H or the TMR1L registers when operating in external clock mode (TMR1CS is set). If the application needs to read the 16-bit counter, evaluate if this function can be moved to the TMR0 or one of the other timer resources on the device.

### 4. Module: MSSP- SPI™ Mode

The SDI pin cannot be used as a general purpose output by clearing the TRIS bit when the MSSP module is in SPI mode.

#### Work Around

None for current silicon revision.

### 5. Module: VREF

- a. The operating voltage range for VRL is  $V_{DD} \geq 3.0V$ . (See parameter D400)

#### Work Around

None.

- b. The maximum output voltage for VRL is 2.25V. The minimum output voltage for VRL is 1.8V. The maximum output voltage for VRH is 4.5V. The minimum output voltage for VRH is 3.7V. (See parameter D400)

#### Work Around

None.

- c. The VRH and VRL outputs may have an output voltage fluctuation that is typically 50mV p-p.

#### Work Around

Connecting a 1 $\mu$ F capacitor to each voltage reference pin that is used will reduce the fluctuations, if present.

### 6. Module: 12-bit A/D Converter

The maximum integral error specification for the A/D converter (parameter A03) is  $\pm 3$  LSb.

The maximum offset error specification for the A/D converter (parameter A06) is  $\pm 5$  LSb.

The maximum integral error specification (parameter A03) may be exceeded when either of the VREF module outputs is used as a reference for the A/D converter.

The operating voltage range for the A/D converter is  $3.5V \leq V_{DD} \leq 5.5V$ .

#### Work Around

None.

### 7. Module: PORTD, PORTE

The internal operation of the PIC16C773, Rev. A device is equivalent to a PIC16C774 device. That is, these devices include PORTD, PORTE and the Parallel Slave Port module.

#### Work Around

The application source code should set the TRISD and TRISE registers to 00h.

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8. Module: LVD

Work Around

The minimum levels (parameter D420) specified for the LVD module differ from the Device Data Sheet as follows:

None.

**TABLE 15-3 ELECTRICAL CHARACTERISTICS: LVD**

Standard Operating Conditions (unless otherwise stated)							
DC CHARACTERISTICS							
Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial							
Operating voltage $V_{DD}$ range as described in DC spec Section 15.1 and Section 15.2.							
Param No.	Characteristic	Symbol	Min	Typ†	Max	Units	Conditions
D420	LVD Voltage	LVV = 0100	<b>2.25</b>	2.58	2.66	V	
		LVV = 0101	<b>2.44</b>	2.78	2.86	V	
		LVV = 0110	<b>2.55</b>	2.89	2.98	V	
		LVV = 0111	<b>2.76</b>	3.1	3.2	V	
		LVV = 1000	<b>3.04</b>	3.41	3.52	V	
		LVV = 1001	<b>3.25</b>	3.61	3.72	V	
		LVV = 1010	<b>3.35</b>	3.72	3.84	V	
		LVV = 1011	<b>3.53</b>	3.92	4.04	V	
		LVV = 1100	<b>3.72</b>	4.13	4.26	V	
		LVV = 1101	<b>3.89</b>	4.33	4.46	V	
		LVV = 1110	<b>4.17</b>	4.64	4.78	V	
D421	Supply Current	$\Delta I_{LVD}$	—	10	20	$\mu\text{A}$	
D422*	LVD Voltage Drift Temperature coefficient	$TC_{VOUT}$	—	15	50	$\text{ppm}/^{\circ}\text{C}$	
D423*	LVD Voltage Drift with respect to $V_{DD}$ Regulation	$\Delta V_{LVD}/\Delta V_{DD}$	—	—	50	$\mu\text{V}/\text{V}$	
D424*	Low-voltage Detect Hysteresis	$V_{LHYS}$	TBD	—	100	mV	

\* These parameters are characterized but not tested.

**Note 1:** Production tested at  $T_{amb} = 25^{\circ}\text{C}$ . Specifications over temperature limits ensured by characterization.

9. Module: BOR

Work Around

The maximum levels specified (parameter D005) for the BOR module differ from the Device Data Sheet as follows:

None.

**TABLE 15-4 ELECTRICAL CHARACTERISTICS: BOR**

<b>Standard Operating Conditions (unless otherwise stated)</b> Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial Operating voltage VDD range as described in DC spec Section 15.1 and Section 15.2.							
Param No.	Characteristic	Symbol	Min	Typ	Max	Units	Conditions
D005	BOR Voltage	V <sub>BOR</sub>	1.8	2.58	<b>2.8</b>	V	
			2.0	2.78	<b>2.9</b>		
			3.6	4.33	<b>4.45</b>		
			4.0	4.64	<b>4.85</b>		
D006*	BOR Voltage Drift Temperature coefficient	TCVOUT	—	15	50	ppm/°C	
D006A*	BOR Voltage Drift with respect to VDD Regulation	$\Delta V_{BOR}/\Delta V_{DD}$	—	—	50	$\mu\text{V}/\text{V}$	
D007	Brown-out Hysteresis	V <sub>BHYS</sub>	TBD	—	100	mV	
D022A	Supply Current	$\Delta I_{BOR}$	—	10	TBD	$\mu\text{A}$	

\* These parameters are characterized but not tested.

**Note 1:** Production tested at T<sub>AMB</sub> = 25°C. Specifications over temperature limits ensured by characterization.

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## Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS30275A), the following clarifications and corrections should be noted.

The typical A/D converter supply current (parameter D026) should be the value indicated in Table 15-1 and Table 15-2 below.

### 15.1 DC Characteristics: PIC16C77X (Commercial, Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated)					
		Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial					
Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
D001 D001A	Supply Voltage	VDD	4.0 4.5	—	5.5 5.5	V V	XT, RC and LP osc configuration HS osc configuration
D002*	RAM Data Retention Voltage (Note 1)	VDR	—	1.5	—	V	
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	—	VSS	—	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	—	—	V/ms	See section on Power-on Reset for details. PWRT enabled
D010  D013	Supply Current (Note 2)	IDD	—	2.7 13.5	5 30	mA mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 5.5V (Note 4)  HS osc configuration FOSC = 20 MHz, VDD = 5.5V
D020 D020A	Power-down Current (Note 3)	IPD	— —	1.5 1.5	16 19	μA μA	VDD = 4.0V, -0°C to +70°C VDD = 4.0V, -40°C to +85°C
D021	Module Differential Current (Note 5)						
D021	Watchdog Timer	ΔIWDT	—	6.0	20	μA	VDD = 4.0V
D023B*	Bandgap voltage generator	ΔIBG <sup>6</sup>	—	40μA	TBD	μA	
D025*	Timer1 oscillator	ΔIT1OSC	—	5	9	μA	VDD = 4.0V
D026*	A/D Converter	ΔIAD	—	70	—	μA	VDD = 5.5V, A/D on, not converting

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which VDD can be lowered without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD.

MCLR = VDD; WDT enabled/disabled as specified.

**3:** The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

**4:** For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula  $I_r = V_{DD}/2R_{ext}$  (mA) with Rext in kOhm.

**5:** The Δ current is the additional current consumed when the peripheral is enabled. This current should be added to the base (IPD or IDD) current.

**6:** The bandgap voltage reference provides 1.22V to the VRL, VRH, LVD and BOR circuits. When calculating current consumption, use the following formula:  $\Delta I_{VRL} + \Delta I_{VRH} + \Delta I_{LVD} + \Delta I_{BOR} + \Delta I_{BG}$ . Any of the  $\Delta I_{VRL}$ ,  $\Delta I_{VRH}$ ,  $\Delta I_{LVD}$  or  $\Delta I_{BOR}$  can be 0.

## 15.2 DC Characteristics: PIC16LC77X-04 (Commercial, Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial					
Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
D001	Supply Voltage	VDD	2.5	—	5.5	V	LP, XT, RC osc configuration (DC - 4 MHz)
D002*	RAM Data Retention Voltage (Note 1)	VDR	—	1.5	—	V	
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	—	VSS	—	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	0.05	—	—	V/ms	See section on Power-on Reset for details. PWRT enabled
D010	Supply Current (Note 2)	IDD	—	2.0	3.8	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 3.0V (Note 4)
D010A			—	22.5	48	$\mu\text{A}$	LP osc configuration FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D020	Power-down Current (Note 3)	IPD	—	0.9	5	$\mu\text{A}$	VDD = 3.0V, $0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$
D020A			—	0.9	5	$\mu\text{A}$	VDD = 3.0V, $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
	Module Differential Current (note5)						
D021	Watchdog Timer	$\Delta I_{\text{WDT}}$	—	6	20	$\mu\text{A}$	VDD = 3.0V
D025*	Timer1 oscillator	$\Delta I_{\text{T1OSC}}$	—	1.5	3	$\mu\text{A}$	VDD = 3.0V
D026*	A/D Converter	$\Delta I_{\text{AD}}$	—	70	—	$\mu\text{A}$	VDD = 5.5V, A/D on, not converting

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V,  $25^{\circ}\text{C}$  unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which VDD can be lowered without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD.

MCLR = VDD; WDT enabled/disabled as specified.

**3:** The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

**4:** For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula  $I_r = V_{\text{DD}}/2R_{\text{ext}}$  (mA) with Rext in kOhm.

**5:** The  $\Delta$  current is the additional current consumed when the peripheral is enabled. This current should be added to the base (IPD or IDD) current.

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The typical Vref line regulation should be the value specified in Table 15-2 below.

**TABLE 15-2 ELECTRICAL CHARACTERISTICS: VREF**

Standard Operating Conditions (unless otherwise stated)							
DC CHARACTERISTICS							
Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial							
Operating voltage VDD range as described in DC spec Section 15.1 and Section 15.2.							
Param No.	Characteristic	Symbol	Min	Typ†	Max	Units	Conditions
D400	Output Voltage	VRL	2.0	2.048	2.1	V	VDD ≥ 2.5V
		VRH	4.0	4.096	4.2	V	VDD ≥ 4.5V
D401A	VRL Quiescent Supply Current	ΔIVRL	—	70	TBD	μA	No load on VRL.
D401B	VRH Quiescent Supply Current	ΔIVRH	—	70	TBD	μA	No load on VRH.
D402	Output Voltage Drift	TCVOUT	—	15*	50*	ppm/°C	Note 1
D404	External Load Source	IVREFSO	—	—	5*	mA	
D405	External Load Sink	IVREFSI	—	—	-5*	mA	
D406	Load Regulation	ΔVOUT/ ΔIOUT	—	1	TBD*	mV/mA	Isource = 0 mA to 5 mA
		ΔVOUT/ ΔIOUT	—	1	TBD*		Isink = 0 mA to 5 mA
D407	Line Regulation	ΔVOUT/ ΔVDD	—	1	—	mV/V	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Production tested at TAMB = 25°C. Specifications over temp limits ensured by characterization.



The maximum LVD supply current (parameter D421) should be the value indicated in Table 15-3 below.

**TABLE 15-3 ELECTRICAL CHARACTERISTICS: LVD**

Standard Operating Conditions (unless otherwise stated)							
DC CHARACTERISTICS							
Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial							
Operating voltage VDD range as described in DC spec Section 15.1 and Section 15.2.							
Param No.	Characteristic	Symbol	Min	Typ†	Max	Units	Conditions
D420	LVD Voltage	LVV = 0100	2.5	2.58	2.66	V	
		LVV = 0101	2.7	2.78	2.86	V	
		LVV = 0110	2.8	2.89	2.98	V	
		LVV = 0111	3.0	3.1	3.2	V	
		LVV = 1000	3.3	3.41	3.52	V	
		LVV = 1001	3.5	3.61	3.72	V	
		LVV = 1010	3.6	3.72	3.84	V	
		LVV = 1011	3.8	3.92	4.04	V	
		LVV = 1100	4.0	4.13	4.26	V	
		LVV = 1101	4.2	4.33	4.46	V	
		LVV = 1110	4.5	4.64	4.78	V	
D421	Supply Current	$\Delta I_{LVD}$	—	10	TBD	$\mu\text{A}$	
D422*	LVD Voltage Drift Temperature coefficient	TCVOUT	—	15	50	ppm/ $^{\circ}\text{C}$	
D423*	LVD Voltage Drift with respect to VDD Regulation	$\frac{\Delta V_{LVD}}{\Delta V_{DD}}$	—	—	50	$\mu\text{V}/\text{V}$	
D424*	Low-voltage Detect Hysteresis	VLHYS	TBD	—	100	mV	

\* These parameters are characterized but not tested.

**Note 1:** Production tested at  $T_{amb} = 25^{\circ}\text{C}$ . Specifications over temperature limits ensured by characterization.

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The maximum BOR supply current (parameter D022A) should be the value indicated in Table 15-4 below.

**TABLE 15-4 ELECTRICAL CHARACTERISTICS: BOR**

<b>Standard Operating Conditions (unless otherwise stated)</b> Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial Operating voltage VDD range as described in DC spec Section 15.1 and Section 15.2.							
Param No.	Characteristic	Symbol	Min	Typ	Max	Units	Conditions
D005	BOR Voltage	BORV1:0 = 11	2.5	2.58	2.66	V	
		BORV1:0 = 10	2.7	2.78	2.86		
		BORV1:0 = 01	4.2	4.33	4.46		
		BORV1:0 = 00	4.5	4.64	4.78		
D006*	BOR Voltage Drift Temperature coefficient	TCVOUT	—	15	50	ppm/°C	
D006A*	BOR Voltage Drift with respect to VDD Regulation	$\Delta V_{BOR}/\Delta V_{DD}$	—	—	50	$\mu\text{V}/\text{V}$	
D007	Brown-out Hysteresis	V <sub>BHYS</sub>	TBD	—	100	mV	
D022A	Supply Current	$\Delta I_{BOR}$	—	10	<b>TBD</b>	$\mu\text{A}$	

\* These parameters are characterized but not tested.

**Note 1:** Production tested at T<sub>AMB</sub> = 25°C. Specifications over temperature limits ensured by characterization.

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### AMERICAS

#### Corporate Office

Microchip Technology Inc.  
2355 West Chandler Blvd.  
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Technical Support: 480-786-7627  
Web Address: <http://www.microchip.com>

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Tel: 937-291-1654 Fax: 937-291-9175

#### Detroit

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Tri-Atria Office Building  
32255 Northwestern Highway, Suite 190  
Farmington Hills, MI 48334  
Tel: 248-538-2250 Fax: 248-538-2260

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18201 Von Karman, Suite 1090  
Irvine, CA 92612  
Tel: 949-263-1888 Fax: 949-263-1338

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150 Motor Parkway, Suite 202  
Hauppauge, NY 11788  
Tel: 631-273-5305 Fax: 631-273-5335

#### San Jose

Microchip Technology Inc.  
2107 North First Street, Suite 590  
San Jose, CA 95131  
Tel: 408-436-7950 Fax: 408-436-7955

### AMERICAS (continued)

#### Toronto

Microchip Technology Inc.  
5925 Airport Road, Suite 200  
Mississauga, Ontario L4V 1W1, Canada  
Tel: 905-405-6279 Fax: 905-405-6253

### ASIA/PACIFIC

#### Hong Kong

Microchip Asia Pacific  
Unit 2101, Tower 2  
Metroplaza  
223 Hing Fong Road  
Kwai Fong, N.T., Hong Kong  
Tel: 852-2-401-1200 Fax: 852-2-401-3431

#### Beijing

Microchip Technology, Beijing  
Unit 915, 6 Chaoyangmen Bei Dajie  
Dong Erhuan Road, Dongcheng District  
New China Hong Kong Manhattan Building  
Beijing 100027 PRC  
Tel: 86-10-85282100 Fax: 86-10-85282104

#### India

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India Liaison Office  
No. 6, Legacy, Convent Road  
Bangalore 560 025, India  
Tel: 91-80-229-0061 Fax: 91-80-229-0062

#### Japan

Microchip Technology Intl. Inc.  
Benex S-1 6F  
3-18-20, Shinyokohama  
Kohoku-Ku, Yokohama-shi  
Kanagawa 222-0033 Japan  
Tel: 81-45-471-6166 Fax: 81-45-471-6122

#### Korea

Microchip Technology Korea  
168-1, Youngbo Bldg. 3 Floor  
Samsung-Dong, Kangnam-Ku  
Seoul, Korea  
Tel: 82-2-554-7200 Fax: 82-2-558-5934

#### Shanghai

Microchip Technology  
RM 406 Shanghai Golden Bridge Bldg.  
2077 Yan'an Road West, Hong Qiao District  
Shanghai, PRC 200335  
Tel: 86-21-6275-5700 Fax: 86 21-6275-5060

### ASIA/PACIFIC (continued)

#### Singapore

Microchip Technology Singapore Pte Ltd.  
200 Middle Road  
#07-02 Prime Centre  
Singapore 188980  
Tel: 65-334-8870 Fax: 65-334-8850

#### Taiwan, R.O.C

Microchip Technology Taiwan  
10F-1C 207  
Tung Hua North Road  
Taipei, Taiwan, ROC  
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

### EUROPE

#### United Kingdom

Arizona Microchip Technology Ltd.  
505 Eskdale Road  
Wokingham  
Berkshire, England RG41 5TU  
Tel: 44 118 921 5858 Fax: 44-118 921-5835

#### Denmark

Microchip Technology Denmark ApS  
Regus Business Centre  
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Tel: 45 4420 9895 Fax: 45 4420 9910

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Batiment A - 1er Etage  
91300 Massy, France  
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

#### Germany

Arizona Microchip Technology GmbH  
Gustav-Heinemann-Ring 125  
D-81739 München, Germany  
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

#### Italy

Arizona Microchip Technology SRL  
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