

PIC16C72A Rev. A Silicon Errata Sheet

The PIC16C72A (Rev. A) parts you have received conform functionally to the Device Data Sheet (DS35008A), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC16C72A silicon.

1. Module: RESET

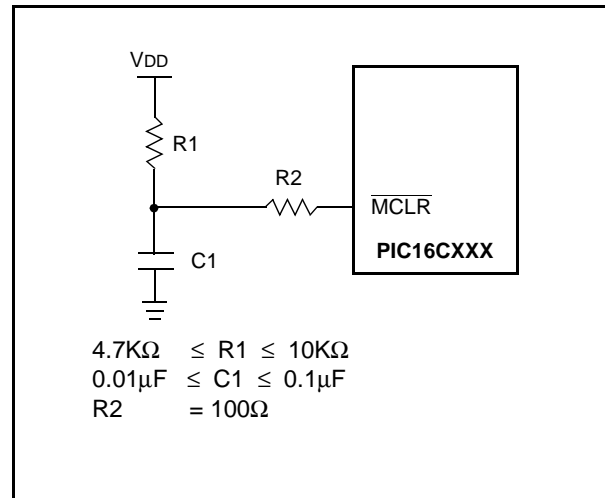
The minimum specification for the $\overline{\text{MCLR}}$ must be met in order to RESET the PIC16CXXX. If a $\overline{\text{MCLR}}$ pulse occurs that is less than the minimum specification (parameter #30), improper device operation can occur.

If the minimum specification cannot be met, then an external circuit must be used to insure that any pulse width less than the specification will be filtered before it reaches the $\overline{\text{MCLR}}$ pin.

Work Around

A possible circuit is shown in Figure 1. Proper design validation needs to be done to ensure desired operation over the applications operating conditions

FIGURE 1: $\overline{\text{MCLR}}$ EXTERNAL CIRCUIT



Note: As with any windowed EPROM device, please cover the window at all times, except when erasing.

PIC16C72A

2. Module: OSCILLATOR

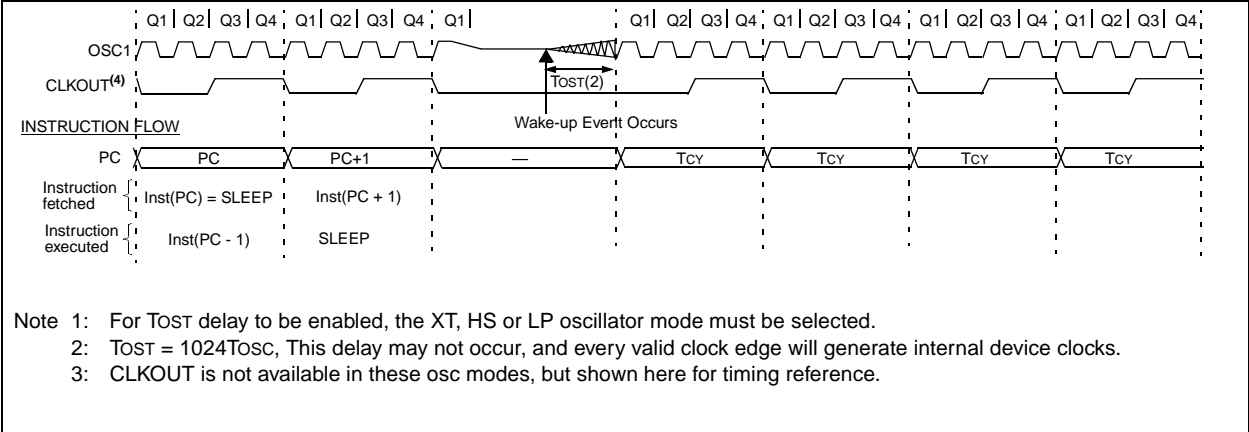
The Oscillator Start-up Timer (TOST) delay may not occur when the device wakes-up from sleep.

Figure 1 shows the start-up of the crystal after the event that causes the device to wake up from sleep mode (as specified in device data sheet). The start-up time (TOST) may not occur.

The events that wake-up the device from sleep are:

- An interrupt
- A WDT overflow (wake-up)
- A Brown-out Reset
- A $\overline{\text{MCLR}}$ reset

Figure 1: Wake-up from Sleep



In applications where time based measurements are started immediately after wake-up from sleep, the suggested work around should be implemented.

Work Around

After the SLEEP instruction, do a software delay of 256 Tcy (same as 1024 TOSC). At the Reset and Interrupt vector addresses, test to see if the device woke from sleep (the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits), and if the device did wake from sleep, ensure that the total cycle delay is 256 Tcy.

3. Module: TMR1

When operating in external clock mode (TMR1CS is set), reading either of the timer 1 registers (TMR1H or TMR1L) may cause the timer not to increment as expected. This occurs for both synchronous and asynchronous inputs.

The scenarios which display this are:

- When a read operation of the TMR1H register occurs, the TMR1L register may not increment.
- When a read operation of the TMR1L register occurs, the TMR1H register may not increment. This improper operation is only an issue when the TMR1L register increments from FFh to 00h (FFh → 00H) during the read of the TMR1L register.

Work Around

Do not read either the TMR1H or the TMR1L registers when operating in external clock mode (TMR1CS is set). If the application needs to read the 16-bit counter, evaluate if this function can be moved to the TMR0 or one of the other timer resources on the device.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS35008A), the following clarifications and corrections should be noted.

none



WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

Microchip Technology Inc.
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-786-7200 Fax: 480-786-7277
Technical Support: 480-786-7627
Web Address: <http://www.microchip.com>

Atlanta

Microchip Technology Inc.
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Boston

Microchip Technology Inc.
5 Mount Royal Avenue
Marlborough, MA 01752
Tel: 508-480-9990 Fax: 508-480-8575

Chicago

Microchip Technology Inc.
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas

Microchip Technology Inc.
4570 Westgrove Drive, Suite 160
Addison, TX 75248
Tel: 972-818-7423 Fax: 972-818-2924

Dayton

Microchip Technology Inc.
Two Prestige Place, Suite 150
Miamisburg, OH 45342
Tel: 937-291-1654 Fax: 937-291-9175

Detroit

Microchip Technology Inc.
Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Los Angeles

Microchip Technology Inc.
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

New York

Microchip Technology Inc.
150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose

Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

AMERICAS (continued)

Toronto

Microchip Technology Inc.
5925 Airport Road, Suite 200
Mississauga, Ontario L4V 1W1, Canada
Tel: 905-405-6279 Fax: 905-405-6253

ASIA/PACIFIC

Hong Kong

Microchip Asia Pacific
Unit 2101, Tower 2
Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2-401-1200 Fax: 852-2-401-3431

Beijing

Microchip Technology, Beijing
Unit 915, 6 Chaoyangmen Bei Dajie
Dong Erhuan Road, Dongcheng District
New China Hong Kong Manhattan Building
Beijing 100027 PRC
Tel: 86-10-85282100 Fax: 86-10-85282104

India

Microchip Technology Inc.
India Liaison Office
No. 6, Legacy, Convent Road
Bangalore 560 025, India
Tel: 91-80-229-0061 Fax: 91-80-229-0062

Japan

Microchip Technology Intl. Inc.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa 222-0033 Japan
Tel: 81-45-471-6166 Fax: 81-45-471-6122

Korea

Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Shanghai

Microchip Technology
RM 406 Shanghai Golden Bridge Bldg.
2077 Yan'an Road West, Hong Qiao District
Shanghai, PRC 200335
Tel: 86-21-6275-5700 Fax: 86 21-6275-5060

ASIA/PACIFIC (continued)

Singapore

Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan, R.O.C

Microchip Technology Taiwan
10F-1C 207
Tung Hua North Road
Taipei, Taiwan, ROC
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

United Kingdom

Arizona Microchip Technology Ltd.
505 Eskdale Road
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5858 Fax: 44-118 921-5835

Denmark

Microchip Technology Denmark ApS
Regus Business Centre
Lautrup hof 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France

Arizona Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany

Arizona Microchip Technology GmbH
Gustav-Heinemann-Ring 125
D-81739 München, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy

Arizona Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

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