

PIC16C62B Rev. A Silicon Errata Sheet

The PIC16C62B (Rev. A) parts you have received conform functionally to the Device Data Sheet (DS35008A), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC16C62B silicon.

1. Module: RESET

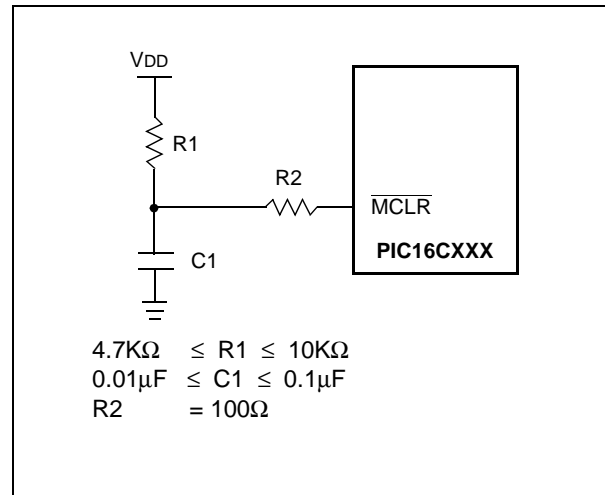
The minimum specification for the $\overline{\text{MCLR}}$ must be met in order to RESET the PIC16CXXX. If a $\overline{\text{MCLR}}$ pulse occurs that is less than the minimum specification (parameter #30), improper device operation can occur.

If the minimum specification cannot be met, then an external circuit must be used to insure that any pulse width less than the specification will be filtered before it reaches the $\overline{\text{MCLR}}$ pin.

Work Around

A possible circuit is shown in Figure 1. Proper design validation needs to be done to ensure desired operation over the applications operating conditions

FIGURE 1: $\overline{\text{MCLR}}$ EXTERNAL CIRCUIT



Note: As with any windowed EPROM device, please cover the window at all times, except when erasing.

PIC16C62B

2. Module: OSCILLATOR

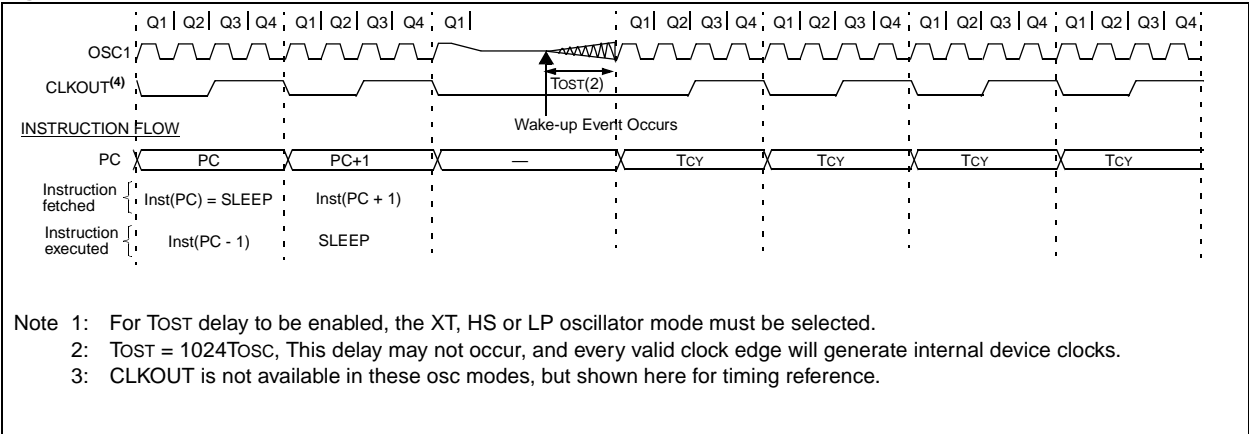
The Oscillator Start-up Timer (TOST) delay may not occur when the device wakes-up from sleep.

Figure 1 shows the start-up of the crystal after the event that causes the device to wake up from sleep mode (as specified in device data sheet). The start-up time (TOST) may not occur.

The events that wake-up the device from sleep are:

- An interrupt
- A WDT overflow (wake-up)
- A Brown-out Reset
- A $\overline{\text{MCLR}}$ reset

Figure 1: Wake-up from Sleep



In applications where time based measurements are started immediately after wake-up from sleep, the suggested work around should be implemented.

Work Around

After the SLEEP instruction, do a software delay of 256 Tcy (same as 1024 TOSC). At the Reset and Interrupt vector addresses, test to see if the device woke from sleep (the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits), and if the device did wake from sleep, ensure that the total cycle delay is 256 Tcy.

3. Module: TMR1

When operating in external clock mode (TMR1CS is set), reading either of the timer 1 registers (TMR1H or TMR1L) may cause the timer not to increment as expected. This occurs for both synchronous and asynchronous inputs.

The scenarios which display this are:

- When a read operation of the TMR1H register occurs, the TMR1L register may not increment.
- When a read operation of the TMR1L register occurs, the TMR1H register may not increment. This improper operation is only an issue when the TMR1L register increments from FFh to 00h (FFh → 00H) during the read of the TMR1L register.

Work Around

Do not read either the TMR1H or the TMR1L registers when operating in external clock mode (TMR1CS is set). If the application needs to read the 16-bit counter, evaluate if this function can be moved to the TMR0 or one of the other timer resources on the device.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS35008A), the following clarifications and corrections should be noted.

none.



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