PIC12C508/509

Errata Sheet for PIC12C508/509 (Rev. A Silicon)

The PIC12C5XX-parts conform functionally to the PIC12C5XX Data Sheet (DS40139E), except for the anomalies described below:

None

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS40139E), the following clarifications and corrections should be noted.

Section 11: Corrections for the DC Characteristics, Section 11.2 are shown.

Corrections for the GPIO pull-up resistor ranges are shown in Table 11-1.

For the section titled “Reset”, additional information is provided on OSC1/CLKIN and OSC2/CLKOUT pin states during a $\overline{MCLR}$.

11.2 DC CHARACTERISTICS: PIC12C508/509 (Commercial, Industrial, Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating voltage VDD range as described in DC spec Section 11.1 and Section 11.2.				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	Input High Voltage						
	I/O ports	VIH		-			
D040	with TTL buffer		2.0V	-	VDD	V	4.5 ≤ VDD ≤ 5.5V
D040A			0.25VDD + 0.8V	-	VDD	V	otherwise
D070	GPIO weak pull-up current (Note 7)	IPUR	50	250	400	µA	VDD = 5V, VPIN = VSS
	Input Leakage Current (2, 3)	IIL					For VDD ≤5.5V
D061	GP3/$\overline{MCLR}$ (Note 5)		8	130	250	µA	Vss ≤ VPIN ≤ VDD
D061A	GP3/$\overline{MCLR}$ (Note 6)		-	-	±5	µA	Vss ≤ VPIN ≤ VDD

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12C5XX be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: **Extended operating range is Advanced Information for this device.**

5: This spec. applies to GP3/$\overline{MCLR}$ configured as external $\overline{MCLR}$ and GP3/$\overline{MCLR}$ configured as input with internal pull-up enabled.

6: This spec. applies when GP3/$\overline{MCLR}$ is configured as an input with pull-up disabled. The leakage current of the $\overline{MCLR}$ circuit is higher than the standard I/O logic.

7: Does not include GP3. For GP3 see parameters D0061 and D0061A.

TABLE 11-1: PULL-UP RESISTOR RANGES - PIC12C508/C509

VDD (Volts)	Temperature (°C)	Min	Typ	Max	Units
GP0/GP1					
2.5	–40	38K	42K	63K	Ω
	25	42K	48K	63K	Ω
	85	42K	49K	63K	Ω
	125	50K	55K	63K	Ω
5.5	–40	15K	17K	20K	Ω
	25	18K	20K	23K	Ω
	85	19K	22K	25K	Ω
	125	22K	24K	28K	Ω
GP3(1)					
2.5	–40	65K	80K	850K	Ω
	25	80K	100K	1150K	Ω
	85	85K	110K	1300K	Ω
	125	100K	120K	1500K	Ω
5.5	–40	50K	60K	600K	Ω
	25	60K	65K	750K	Ω
	85	65K	80K	900K	Ω
	125	75K	90K	990K	Ω

***** These parameters are characterized but not tested.

Note 1: The weak pull-up resistor and associated current for the GP3/$\overline{\text{MCLR}}$ pin is non-linear when the respective pin voltage is less than VDD - 1.0V. See parameter D061 for GP3/$\overline{\text{MCLR}}$ pin current specifications.

Reset

When $\overline{\text{MCLR}}$ is asserted, the state of the OSC1/CLKIN and CLKOUT/OSC2 pins are as follows:

CLKIN/CLKOUT PIN STATES WHEN $\overline{\text{MCLR}}$ ASSERTED

Oscillator Mode	OSC1/CLKIN Pin	OSC2/CLKOUT Pin
EXTRC, CLKOUT on OSC2	OSC1 pin is tristated and driven by external circuit	OSC2 pin is driven low
EXTRC, OSC2 is I/O	OSC1 pin is tristated and driven by external circuit	OSC2 pin is tristate input
INTRC, CLKOUT on OSC2	OSC1 pin is tristate input	OSC2 pin is driven low
INTRC, OSC2 is I/O	OSC1 pin is tristate input	OSC2 pin is tristate input

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