

## Errata Sheet for PIC16C54B (Rev. A and Rev. B Silicon)

The PIC16C54B (**Rev. A Silicon ONLY**) parts conform functionally to the PIC16C5X Data Sheet (**DS30453B**), except for the anomalies described below:

All the problems listed here will be addressed in future revisions of the PIC16C54B silicon.

### 1. Module: RESET

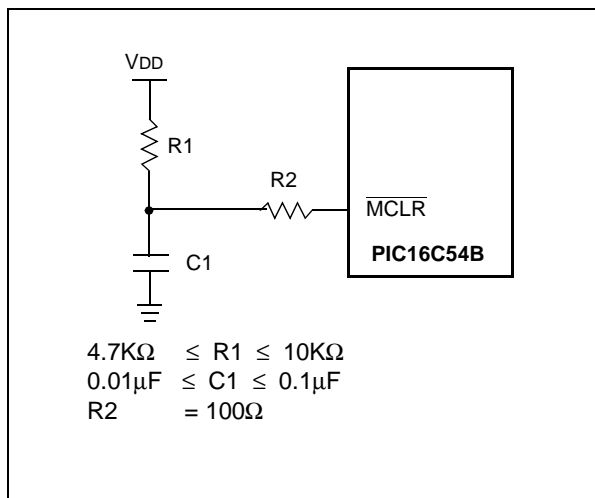
The minimum specification for the  $\overline{\text{MCLR}}$  must be met in order to RESET the PIC16C54B. If a  $\overline{\text{MCLR}}$  pulse occurs that is less than the minimum specification (parameter #30), improper device operation can occur.

If the Minimum specification cannot be met, then an external circuit must be used to insure that any pulse width less than the specification will be filtered before it reaches the  $\overline{\text{MCLR}}$  pin.

#### Work Around

A possible circuit is shown in Figure 1. Proper design validation needs to be done to ensure desired operation over the applications operating conditions.

**FIGURE 1:  $\overline{\text{MCLR}}$  EXTERNAL CIRCUIT**

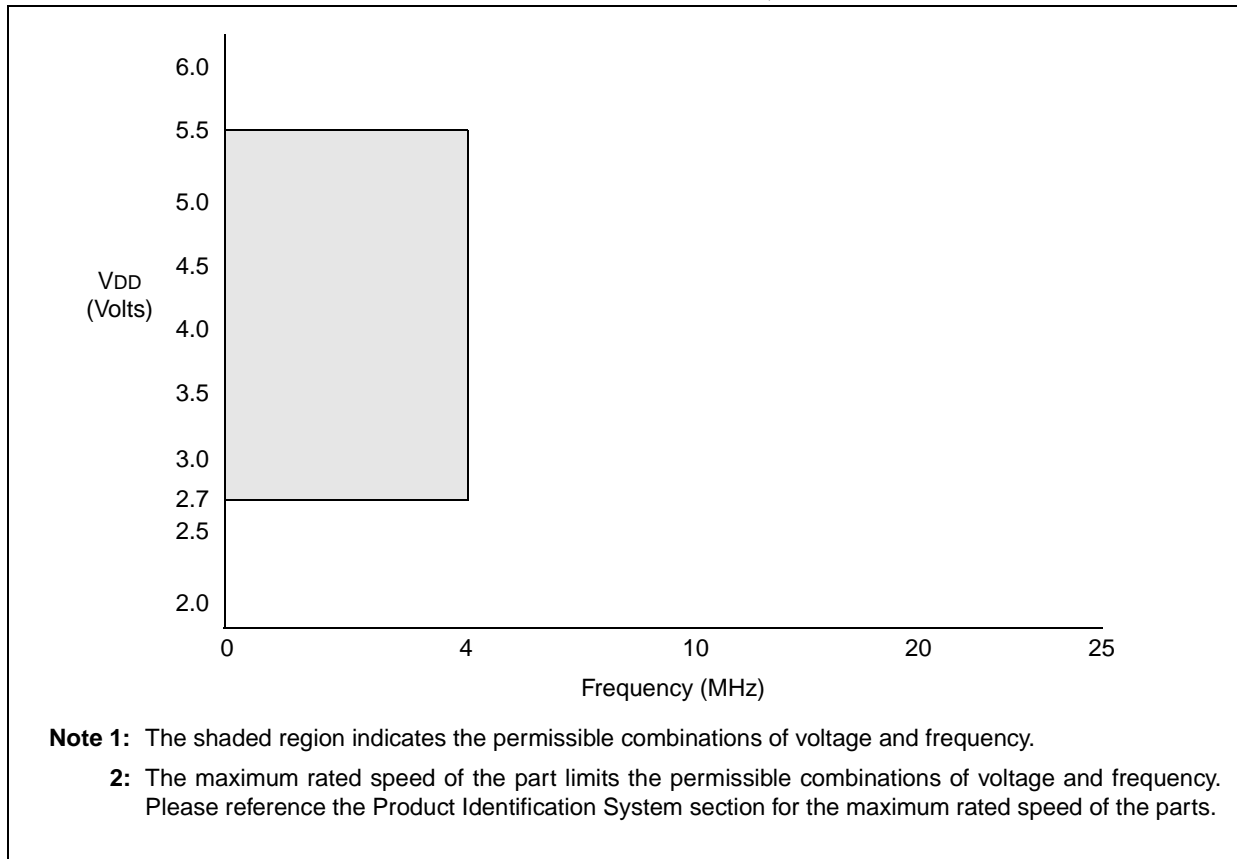


**Note:** As with any windowed EPROM device, please cover the window at all times, except when erasing.

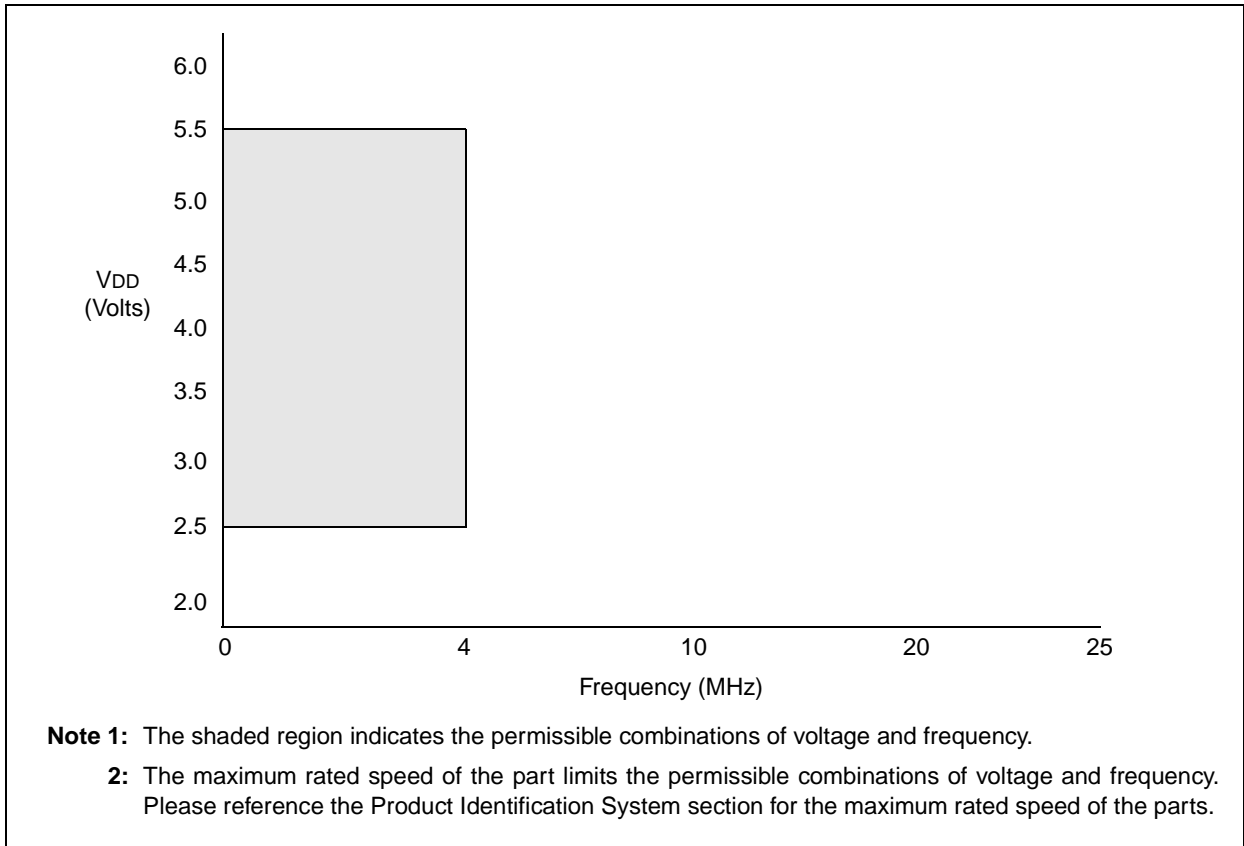
# PIC16C54B

The PIC16C54B (Rev. A and Rev. B Silicon) parts you have received conform functionally to the Device Data Sheet (DS30453B), except for the anomalies described below.

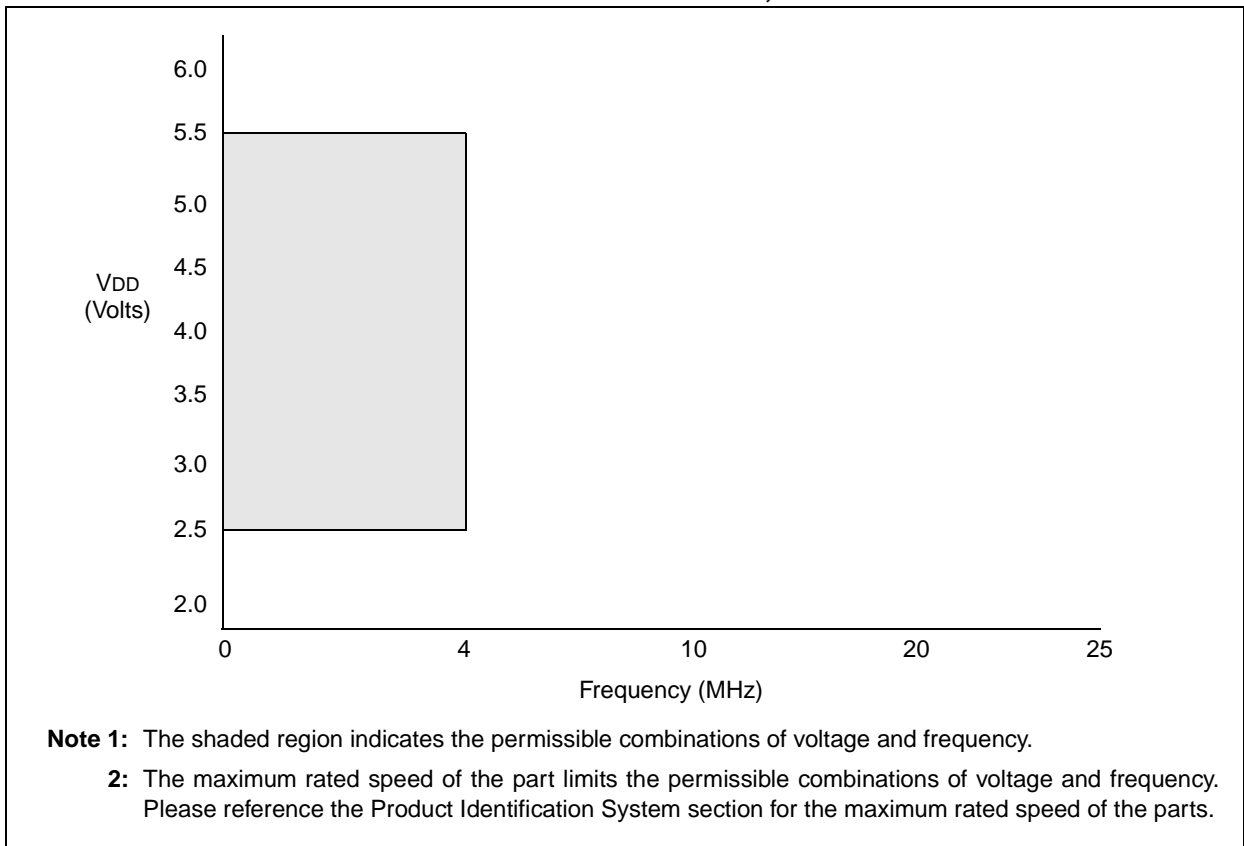
**FIGURE 1: PIC16LC54B VOLTAGE-FREQUENCY GRAPH,  $-40^{\circ}\text{C} \leq T_A \leq 0^{\circ}\text{C}$**



**FIGURE 2: PIC16LC54B VOLTAGE-FREQUENCY GRAPH,  $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$**



**FIGURE 3: PIC16LC54B VOLTAGE-FREQUENCY GRAPH,  $+70^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$**

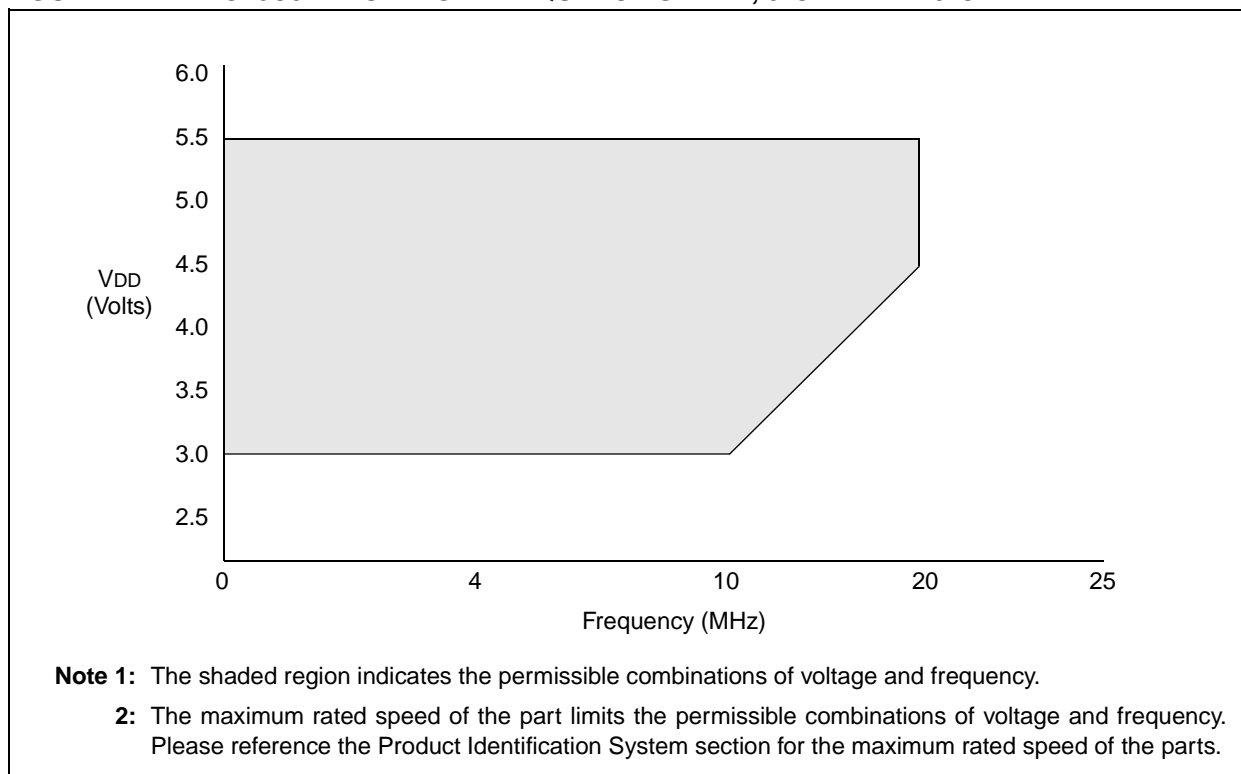


# PIC16C54B

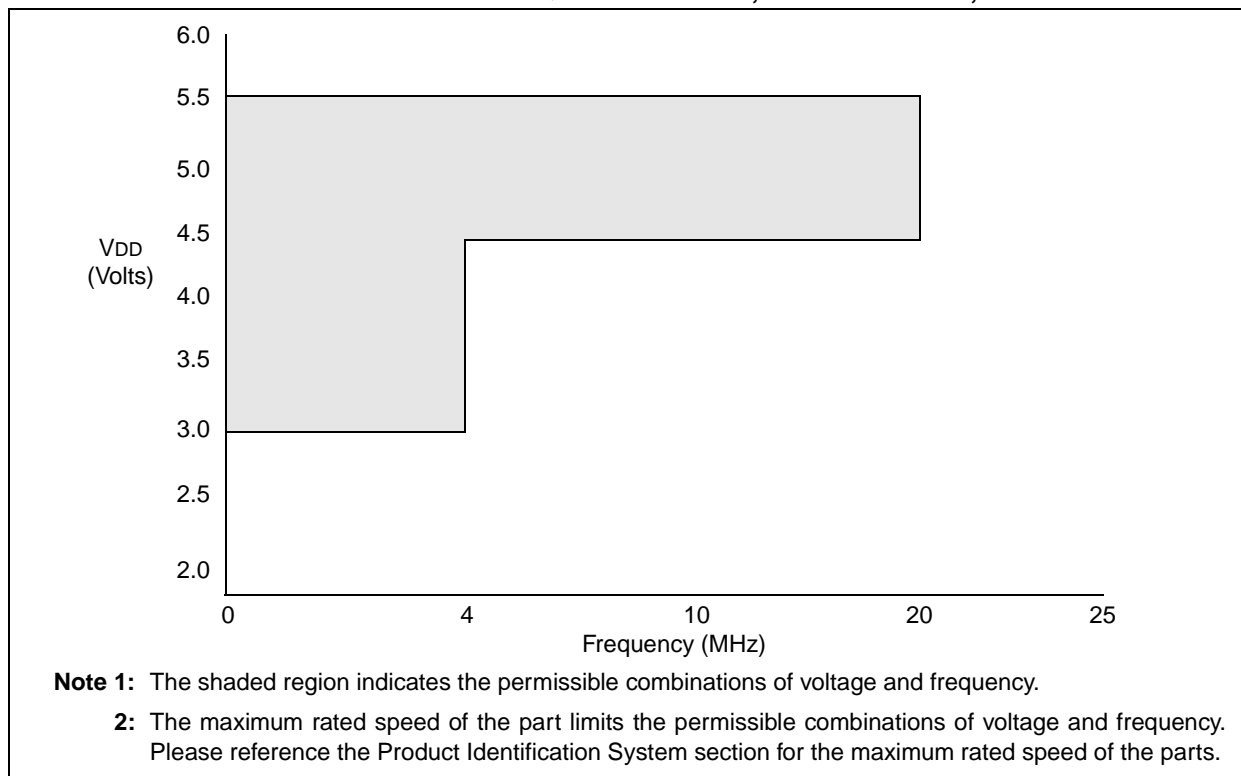
## Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS30453B), the following clarifications and corrections should be noted.

**FIGURE 1: PIC16C54B VOLTAGE-FREQUENCY GRAPH,  $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$**



**FIGURE 2: PIC16C54B VOLTAGE-FREQUENCY GRAPH,  $-40^{\circ}\text{C} \leq T_A < 0^{\circ}\text{C}$ ,  $+70^{\circ}\text{C} < T_A \leq +125^{\circ}\text{C}$**



**19.1 DC Characteristics: PIC16C54B/C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial)  
 PIC16CR54B/CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial)  
 PIC16C54B/C54C/C55A/C56A/C57C/C58B-04I, 20I (Industrial)  
 PIC16CR54B/CR54C/CR56A/CR57C/CR58B-04I, 20I (Industrial)**

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	Sym	Min	Typ <sup>(1)</sup>	Max	Units	Conditions
Supply Voltage	VDD	3.0	—	5.5	V	
RAM Data Retention Voltage <sup>(2)</sup>	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD rise rate to ensure Power-On Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current <sup>(3)(4)</sup>	IDD	—	1.8 — — — 17	2.4 3.6 16 32 40	mA mA mA μA μA	FOSC = 4 MHz, VDD = 5.5V, XT mode FOSC = 10 MHz, VDD = 3.0V, HS mode FOSC = 20 MHz, VDD = 5.5V, HS mode FOSC = 32 kHz, VDD = 3.0V, LP mode, Commercial FOSC = 32 kHz, VDD = 3.0V, LP mode, Industrial
Power Down Current <sup>(5)</sup>	IPD	—	0.25 — — 2.0	4.0 5.0 7.0 8.0	μA μA μA μA	VDD = 3.0V, WDT disabled, Commercial VDD = 3.0V, WDT disabled, Industrial VDD = 5.5V, WDT disabled, Commercial VDD = 5.5V, WDT disabled, Industrial
Watchdog Timer Current	ΔIWDT	—	3.75 — — 10	8.0 9.0 20 22	μA μA μA μA	VDD = 3.0V, Commercial VDD = 3.0V, Industrial VDD = 5.5V*, Commercial VDD = 5.5V*, Industrial
LP Oscillator Operating Frequency	Fosc	0	—	200	kHz	All temperatures
RC Oscillator Operating Frequency		0	—	4	MHz	All temperatures
XT Oscillator Operating Frequency		0	—	4	MHz	All temperatures
HS Oscillator Operating Frequency		0	—	20	MHz	All temperatures

\* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**2:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**3:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to

VSS, T0CKI = VDD, MCLR = VDD; WDT disabled.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

**4:** For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

**5:** The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

# PIC16C54B

## 19.2 DC Characteristics: PIC16C54B/C54C/C55A/C56A/C57C/C58B-04E, 20E (Extended) PIC16CR54B/CR54C/CR56A/CR57C/CR58B-04E, 20E (Extended)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended)				
Characteristic	Sym	Min	Typ <sup>(1)</sup>	Max	Units	Conditions
Supply Voltage	VDD	3.0	—	5.5	V	
RAM Data Retention Voltage <sup>(2)</sup>	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD rise rate to ensure Power-On Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current <sup>(3)(4)</sup>	IDD	—	1.8 9.0	3.3 20	mA mA	FOSC = 4 MHz, VDD = 5.5V, XT mode FOSC = 20 MHz, VDD = 5.5V, HS mode
Power Down Current <sup>(5)</sup>	IPD	—	0.3 10 12	17 50 60	$\mu\text{A}$ $\mu\text{A}$ $\mu\text{A}$	VDD = 3.0V, WDT disabled VDD = 4.5V, WDT disabled VDD = 5.5V, WDT disabled
Watchdog Timer Current	$\Delta\text{IWDT}$	—	4.5 8 14	14 18 30	$\mu\text{A}$ $\mu\text{A}$ $\mu\text{A}$	VDD = 3.0V VDD = 4.5V* VDD = 5.5V*
LP Oscillator Operating Frequency	Fosc	0	—	200	kHz	All temperatures
RC Oscillator Operating Frequency		0	—	4	MHz	All temperatures
XT Oscillator Operating Frequency		0	—	4	MHz	All temperatures
HS Oscillator Operating Frequency		0	—	20	MHz	All temperatures

\* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**2:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**3:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT disabled.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

**4:** For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula:  $I_R = V_{DD}/2R_{ext}$  (mA) with Rext in k $\Omega$ .

**5:** The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

## 19.3 DC Characteristics: PIC16LC5X-04, PIC16LCR5X-04 (Commercial) PIC16LC5X-04I, PIC16LCR5X-04I (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	Sym	Min	Typ <sup>(1)</sup>	Max	Units	Conditions
Supply Voltage	VDD	2.5	—	5.5	V	
RAM Data Retention Voltage <sup>(2)</sup>	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD rise rate to ensure Power-On Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current <sup>(3)(4)</sup>	IDD	—	0.4 — — —	0.6 2.4 27 35	mA mA μA μA	FOSC = 4.0 MHz, VDD = 2.5V, XT mode FOSC = 4.0 MHz, VDD = 5.5V, XT mode FOSC = 32 kHz, VDD = 2.5V, LP mode, Commercial FOSC = 32 kHz, VDD = 2.5V, LP mode, Industrial
Power Down Current <sup>(5)</sup>	IPD	—	0.25 —	2.0 3.0	μA μA	VDD = 2.5V, WDT disabled, Commercial VDD = 2.5V, WDT disabled, Industrial
Watchdog Timer Current	ΔIWDT	—	0.8 —	3.0 5.0	μA μA	VDD = 2.5V, Commercial VDD = 2.5V, Industrial
LP Oscillator Operating Frequency	Fosc	0	—	200	kHz	All temperatures
RC Oscillator Operating Frequency		0	—	4	MHz	All temperatures
XT Oscillator Operating Frequency		0	—	4	MHz	All temperatures
HS Oscillator Operating Frequency		0	—	20	MHz	All temperatures

\* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**2:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**3:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT disabled.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

**4:** For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

**5:** The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

# PIC16C54B

**19.4 DC Characteristics:** PIC16C54B/C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial, Extended)  
PIC16LC54B/LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial)  
PIC16CR54B/CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial, Extended)  
PIC16LCR54B/LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

DC Characteristics All Pins Except Power Supply Pins		Standard Operating Conditions (unless otherwise specified)				
		Operating Temperature 0°C ≤ T <sub>A</sub> ≤ +70°C (commercial) -40°C ≤ T <sub>A</sub> ≤ +85°C (industrial) -40°C ≤ T <sub>A</sub> ≤ +125°C (extended) Operating Voltage V <sub>DD</sub> range is described in Section 19.1, Section 19.2 and Section 19.3.				
Characteristic	Sym	Min	Typ <sup>(1)</sup>	Max	Units	Conditions
<b>Input Low Voltage</b>	V <sub>IL</sub>	V <sub>SS</sub>	—	0.8 V	V	4.5V < V <sub>DD</sub> ≤ 5.5V otherwise
I/O Ports						
I/O Ports						
$\overline{\text{MCLR}}$ (Schmitt Trigger)						
T0CKI (Schmitt Trigger)						
OSC1 (Schmitt Trigger)						
OSC1	V <sub>IH</sub>	2.0 0.25 V <sub>DD</sub> +0.8V	—	V <sub>DD</sub>	V	4.5V < V <sub>DD</sub> ≤ 5.5V <sup>(5)</sup> otherwise
I/O ports						
$\overline{\text{MCLR}}$ (Schmitt Trigger)						
T0CKI (Schmitt Trigger)						
OSC1 (Schmitt Trigger)						
OSC1						
<b>Hysteresis of Schmitt Trigger inputs</b>	V <sub>HYS</sub>	0.15V <sub>DD</sub> *	—	—	V	
<b>Input Leakage Current<sup>(3)</sup></b>	I <sub>IL</sub>	-1.0	0.5	+1.0	μA	<b>For V<sub>DD</sub> ≤ 5.5V</b> V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub> , Pin at hi-impedance V <sub>PIN</sub> = V <sub>SS</sub> +0.25V <sup>(2)</sup> V <sub>PIN</sub> = V <sub>DD</sub> <sup>(2)</sup> V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub> V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub> , XT, HS and LP options
I/O ports						
$\overline{\text{MCLR}}$						
T0CKI						
OSC1						
<b>Output Low Voltage</b>	V <sub>OL</sub>	—	—	0.6	V	I <sub>OL</sub> = 8.7 mA, V <sub>DD</sub> = 4.5V I <sub>OL</sub> = 1.6 mA, V <sub>DD</sub> = 4.5V, RC option only
I/O ports						
OSC2/CLKOUT				0.6	V	
<b>Output High Voltage</b>	V <sub>OH</sub>	V <sub>DD</sub> -0.7	—	—	V	I <sub>OH</sub> = -5.4 mA, V <sub>DD</sub> = 4.5V I <sub>OH</sub> = -1.0 mA, V <sub>DD</sub> = 4.5V, RC option only
I/O ports <sup>(3)</sup>						
OSC2/CLKOUT		V <sub>DD</sub> -0.7			V	

\* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**2:** The leakage current on the  $\overline{\text{MCLR}}$ /V<sub>PP</sub> pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

**3:** Negative current is defined as coming out of the pin.

**4:** For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.



NOTES:



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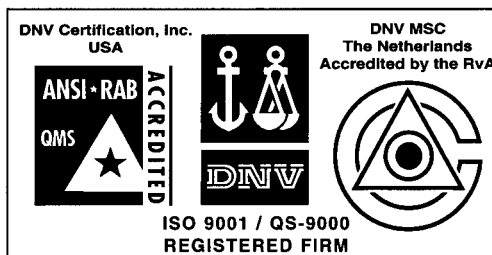
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