PIC16C54C

Errata Sheet for PIC16C54C (Rev. A and Rev. B Silicon)

The PIC16C54C **(Rev. A Silicon ONLY)** parts conform functionally to the PIC16C5X Data Sheet (**DS30453**B), except for the anomalies described below:

All the problems listed here will be addressed in future revisions of the PIC16C54C silicon.

1. Module: RESET

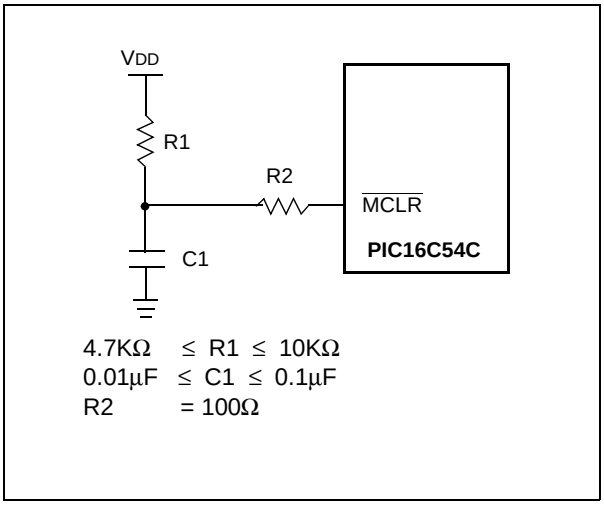
   The minimum specification for the $\overline{\text{MCLR}}$ must be met in order to RESET the PIC16C54C. If a $\overline{\text{MCLR}}$ pulse occurs that is less that the minimum specification (parameter #30), improper device operation can occur.

   If the Minimum specification cannot be met, then an external circuit must be used to insure that any pulse width less than the specification will be filtered before it reaches the $\overline{\text{MCLR}}$ pin.

   Work Around

   A possible circuit is shown in Figure 1. Proper design validation needs to be done to ensure desired operation over the applications operating conditions.

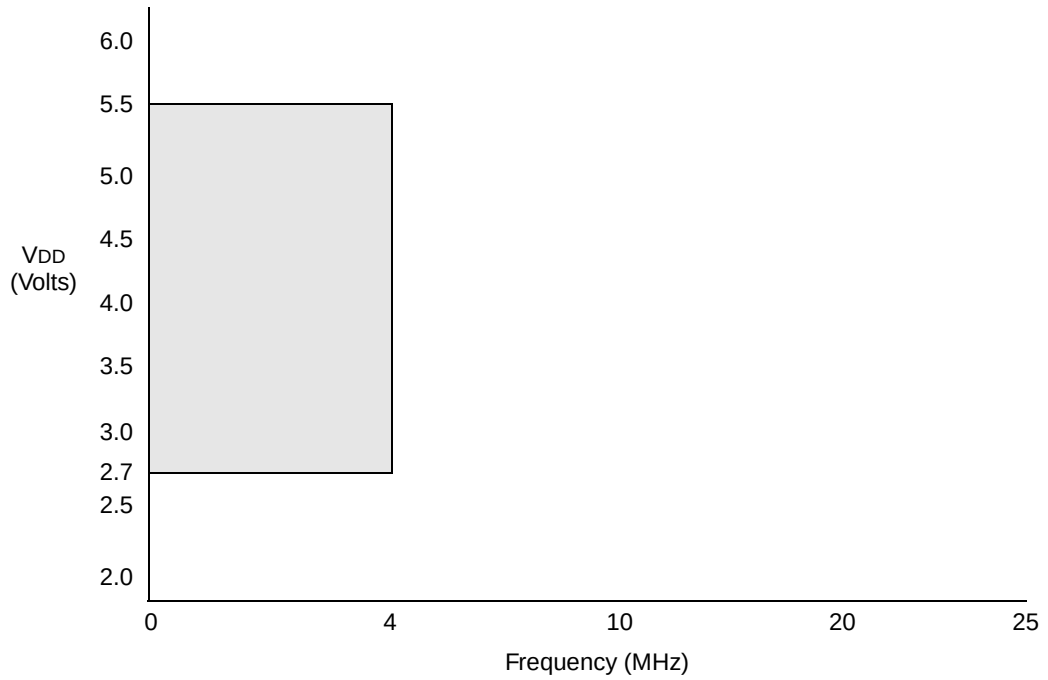
FIGURE 1: $\overline{\text{MCLR}}$ EXTERNAL CIRCUIT



Note: As with any windowed EPROM device, please cover the window at all times, except when erasing.

The PIC16C54C **(Rev. A and Rev. B Silicon)** parts you have received conform functionally to the Device Data Sheet (**DS30453**B), except for the anomalies described below.

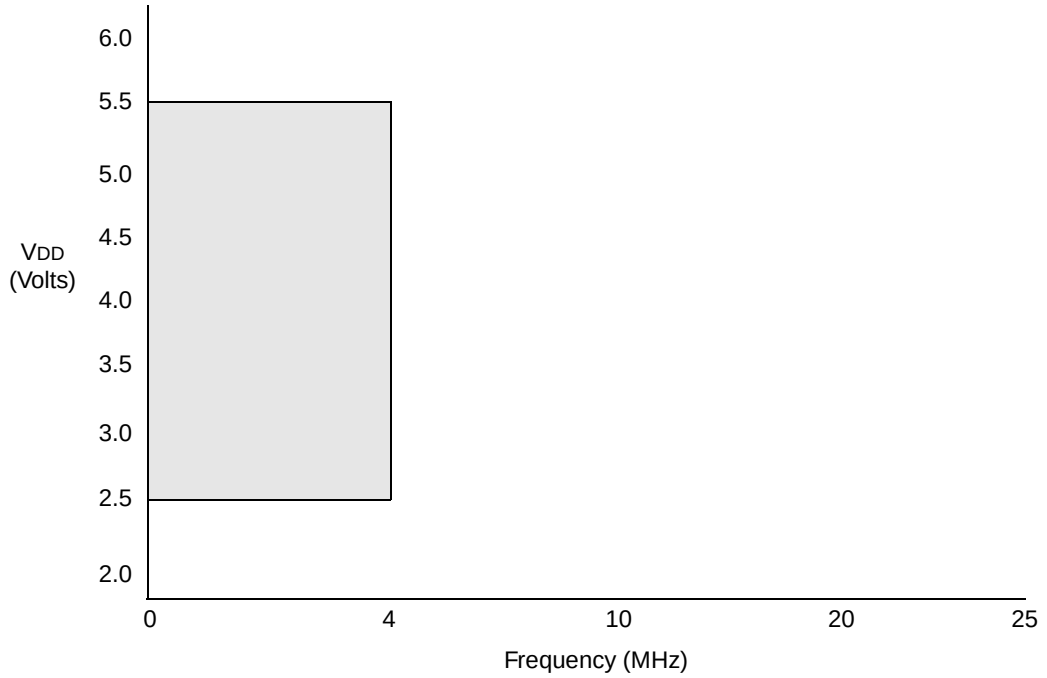
FIGURE 1: PIC16LC54C VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ 0°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

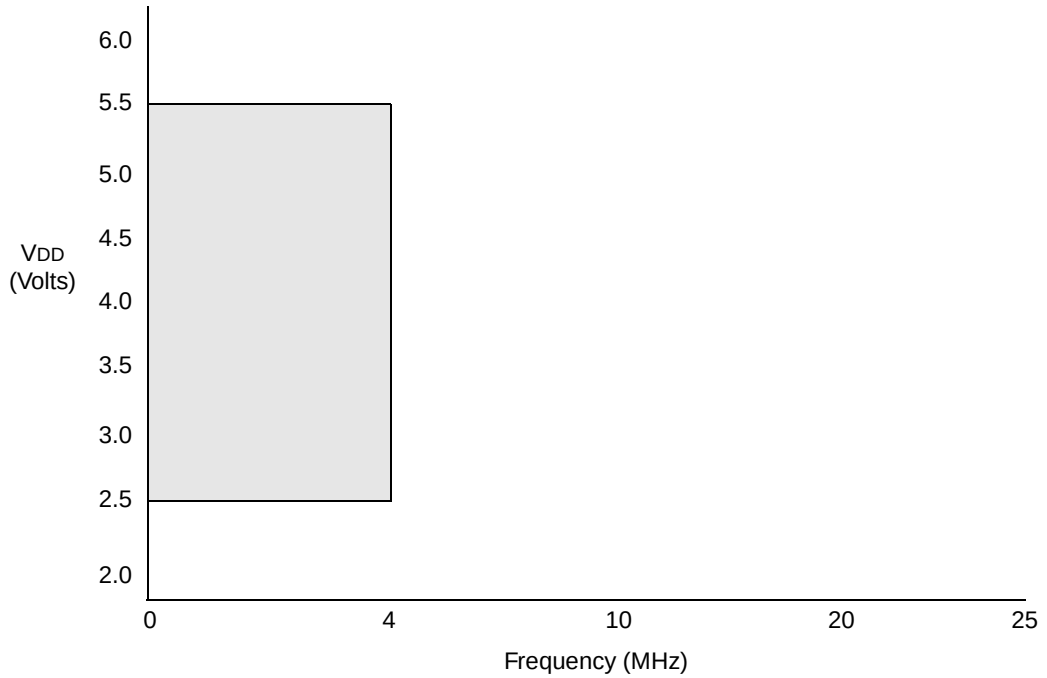
FIGURE 2: PIC16LC54C VOLTAGE-FREQUENCY GRAPH, 0°C ≤ TA ≤ +70°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

FIGURE 3: PIC16LC54C VOLTAGE-FREQUENCY GRAPH, +70°C ≤ TA ≤ +85°C



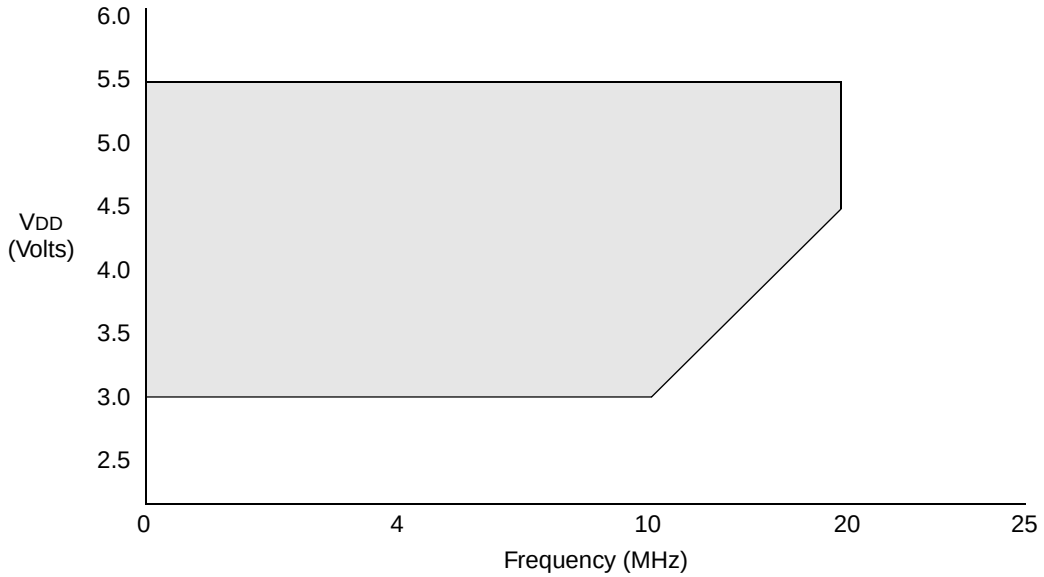
Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (**DS30453**B), the following clarifications and corrections should be noted.

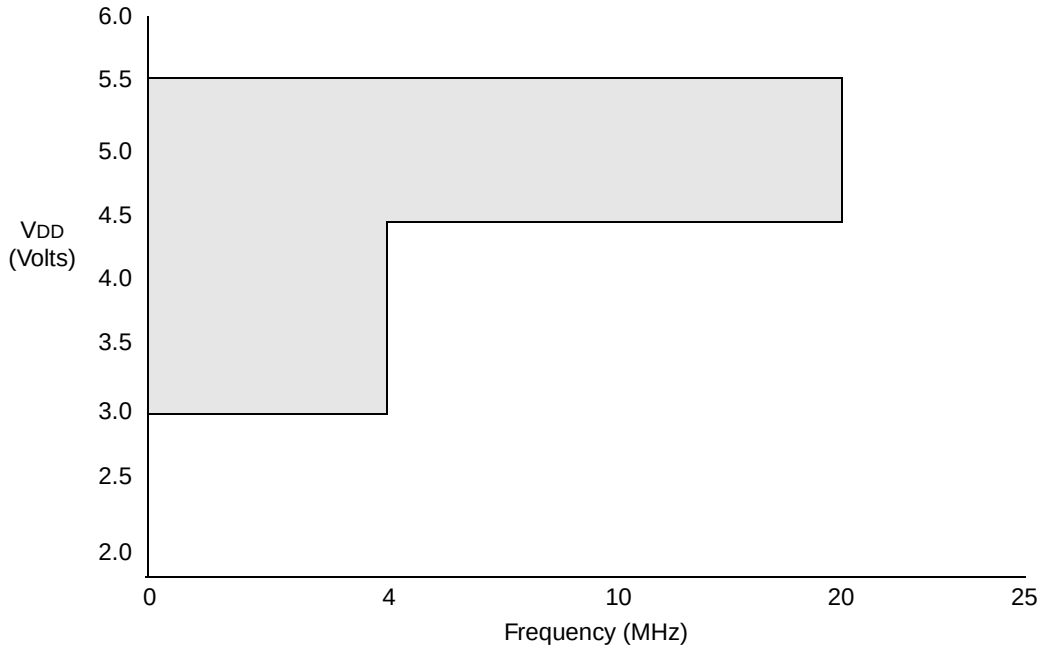
FIGURE 1: PIC16C54C VOLTAGE-FREQUENCY GRAPH, 0°C ≤ TA ≤ +70°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

FIGURE 2: PIC16C54C VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA < 0°C, +70°C < TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

19.1 DC Characteristics: PIC16C54B/C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial) PIC16CR54B/CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial) PIC16C54B/C54C/C55A/C56A/C57C/C58B-04I, 20I (Industrial) PIC16CR54B/CR54C/CR56A/CR57C/CR58B-04I, 20I (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	3.0	—	5.5	V	
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD rise rate to ensure Power-On Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)(4)	IDD	—	1.8	2.4	mA	FOSC = 4 MHz, VDD = 5.5V, XT mode
		—	2.6	3.6	mA	FOSC = 10 MHz, VDD = 3.0V, HS mode
		—	4.5	16	mA	FOSC = 20 MHz, VDD = 5.5V, HS mode
		—	14	32	µA	FOSC = 32 kHz, VDD = 3.0V, LP mode, Commercial
		—	17	40	µA	FOSC = 32 kHz, VDD = 3.0V, LP mode, Industrial
Power Down Current(5)	IPD	—	0.25	4.0	µA	VDD = 3.0V, WDT disabled, Commercial
		—	0.25	5.0	µA	VDD = 3.0V, WDT disabled, Industrial
		—	1.8	7.0	µA	VDD = 5.5V, WDT disabled, Commercial
		—	2.0	8.0	µA	VDD = 5.5V, WDT disabled, Industrial
Watchdog Timer Current	ΔIWDT	—	3.75	8.0	µA	VDD = 3.0V, Commercial
		—	3.75	9.0	µA	VDD = 3.0V, Industrial
		—	8	20	µA	VDD = 5.5V*, Commercial
		—	10	22	µA	VDD = 5.5V*, Industrial
LP Oscillator Operating Frequency	Fosc	0	—	200	kHz	All temperatures
RC Oscillator Operating Frequency		0	—	4	MHz	All temperatures
XT Oscillator Operating Frequency		0	—	4	MHz	All temperatures
HS Oscillator Operating Frequency		0	—	20	MHz	All temperatures

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT disabled.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

19.2 DC Characteristics: PIC16C54B/C54C/C55A/C56A/C57C/C58B-04E, 20E (Extended) PIC16CR54B/CR54C/CR56A/CR57C/CR58B-04E, 20E (Extended)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C (extended)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	3.0	—	5.5	V	
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD rise rate to ensure Power-On Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)(4)	IDD	— —	1.8 9	3.3 20	mA mA	FOSC = 4 MHz, VDD = 5.5V, XT mode FOSC = 20 MHz, VDD = 5.5V, HS mode
Power Down Current(5)	IPD	— — —	0.3 10 12	17 50 60	µA µA µA	VDD = 3.0V, WDT disabled VDD = 4.5V, WDT disabled VDD = 5.5V, WDT disabled
Watchdog Timer Current	ΔIWDT	— — 	4.5 8 14	14 18 30	µA µA µA	VDD = 3.0V VDD = 4.5V* VDD = 5.5V*
LP Oscillator Operating Frequency	Fosc	0	—	200	kHz	All temperatures
RC Oscillator Operating Frequency		0	—	4	MHz	All temperatures
XT Oscillator Operating Frequency		0	—	4	MHz	All temperatures
HS Oscillator Operating Frequency		0	—	20	MHz	All temperatures

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT disabled.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

19.3 DC Characteristics: PIC16LC5X-04, PIC16LCR5X-04 (Commercial) PIC16LC5X-04I, PIC16LCR5X-04I (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	2.5	—	5.5	V	
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD rise rate to ensure Power-On Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)(4)	IDD	—	0.4	0.6	mA	FOSC = 4.0 MHz, VDD = 2.5V, XT mode
		—	0.5	2.4	mA	FOSC = 4.0 MHz, VDD = 5.5V, XT mode
		—	11	27	µA	FOSC = 32 kHz, VDD = 2.5V, LP mode, Commercial
		—	14	35	µA	FOSC = 32 kHz, VDD = 2.5V, LP mode, Industrial
Power Down Current(5)	IPD	—	0.25	2	µA	VDD = 2.5V, WDT disabled, Commercial
		—	0.25	3	µA	VDD = 2.5V, WDT disabled, Industrial
Watchdog Timer Current	ΔIWDT	—	0.8	3	µA	VDD = 2.5V, Commercial
		—	1	5	µA	VDD = 2.5V, Industrial
LP Oscillator Operating Frequency	Fosc	0	—	200	kHz	All temperatures
RC Oscillator Operating Frequency		0	—	4	MHz	All temperatures
XT Oscillator Operating Frequency		0	—	4	MHz	All temperatures
HS Oscillator Operating Frequency		0	—	20	MHz	All temperatures

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT disabled.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

19.4 DC Characteristics: PIC16C54B/C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial, Extended) PIC16LC54B/LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54B/CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial, Extended) PIC16LCR54B/LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

DC Characteristics All Pins Except Power Supply Pins	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 19.1, Section 19.2 and Section 19.3.

Characteristic	Sym	Min	Typ(1)	Max	Units	Conditions
Input Low Voltage	VIL					
I/O Ports		VSS	—	0.8 V	V	4.5V <VDD ≤ 5.5V
I/O Ports		VSS	—	0.15 VDD	V	otherwise
$\overline{\text{MCLR}}$ (Schmitt Trigger)		VSS	—	0.15 VDD	V	
T0CKI (Schmitt Trigger)		VSS	—	0.15 VDD	V	
OSC1 (Schmitt Trigger)		VSS	—	0.15 VDD	V	RC option only(4)
OSC1				0.3 VDD	—	XT, HS and LP options
Input High Voltage	VIH					
		2.0	—	VDD	V	4.5V < VDD ≤ 5.5V(5)
I/O ports		0.25 VDD+0.8V	—	VDD	V	otherwise
$\overline{\text{MCLR}}$ (Schmitt Trigger)		0.85 VDD	—	VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD	—	VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD	—	VDD	V	RC option only(4)
OSC1		0.7 VDD	—	VDD	V	XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*	—	—	V	
Input Leakage Current(3)	IIL					**For VDD ≤ 5.5V**
I/O ports		-1.0	0.5	+1.0	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
$\overline{\text{MCLR}}$		-5.0	—	+5.0	µA	VPIN = VSS +0.25V(2)
			0.5	+3.0	µA	VPIN = VDD(2)
T0CKI		-3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD
OSC1		-3.0	0.5	—	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP options
Output Low Voltage	VOL					
I/O ports		—	—	0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT		—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, RC option only
Output High Voltage	VOH					
I/O ports(3)		VDD-0.7	—	—	V	IOH = -5.4 mA, VDD = 4.5V
OSC2/CLKOUT		VDD-0.7	—	—	V	IOH = -1.0 mA, VDD = 4.5V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the $\overline{\text{MCLR}}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

NOTES:

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