

Errata Sheet for PIC16C58B (Rev. A and Rev. B Silicon)

The PIC16C58B (Rev. A Silicon ONLY) parts conform functionally to the PIC16C5X Data Sheet (DS30453B), except for the anomalies described below:

All the problems listed here will be addressed in future revisions of the PIC16C58B silicon.

1. Module: RESET

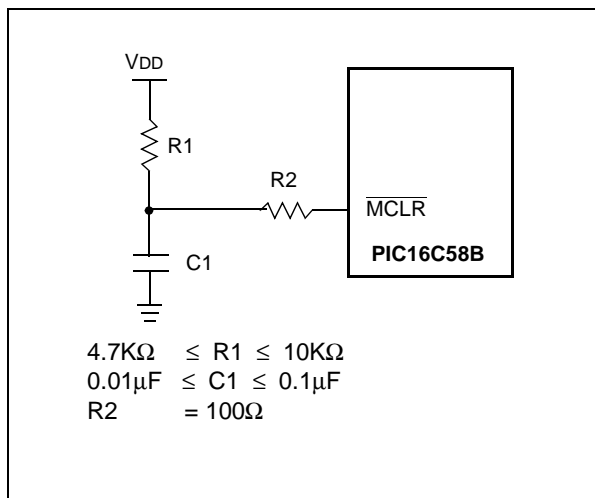
The minimum specification for the $\overline{\text{MCLR}}$ must be met in order to RESET the PIC16C58B. If a $\overline{\text{MCLR}}$ pulse occurs that is less than the minimum specification (parameter #30), improper device operation can occur.

If the Minimum specification cannot be met, then an external circuit must be used to insure that any pulse width less than the specification will be filtered before it reaches the $\overline{\text{MCLR}}$ pin.

Work Around

A possible circuit is shown in Figure 1. Proper design validation needs to be done to ensure desired operation over the applications operating conditions.

FIGURE 1: $\overline{\text{MCLR}}$ EXTERNAL CIRCUIT



Note: As with any windowed EPROM device, please cover the window at all times, except when erasing.

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The PIC16C58B (Rev. A and Rev. B Silicon) parts conform functionally to the PIC16C5X Data Sheet (DS30453B), except for the anomalies described below:

FIGURE 1: PIC16LC58B VOLTAGE-FREQUENCY GRAPH, $-40^{\circ}\text{C} \leq T_A \leq 0^{\circ}\text{C}$

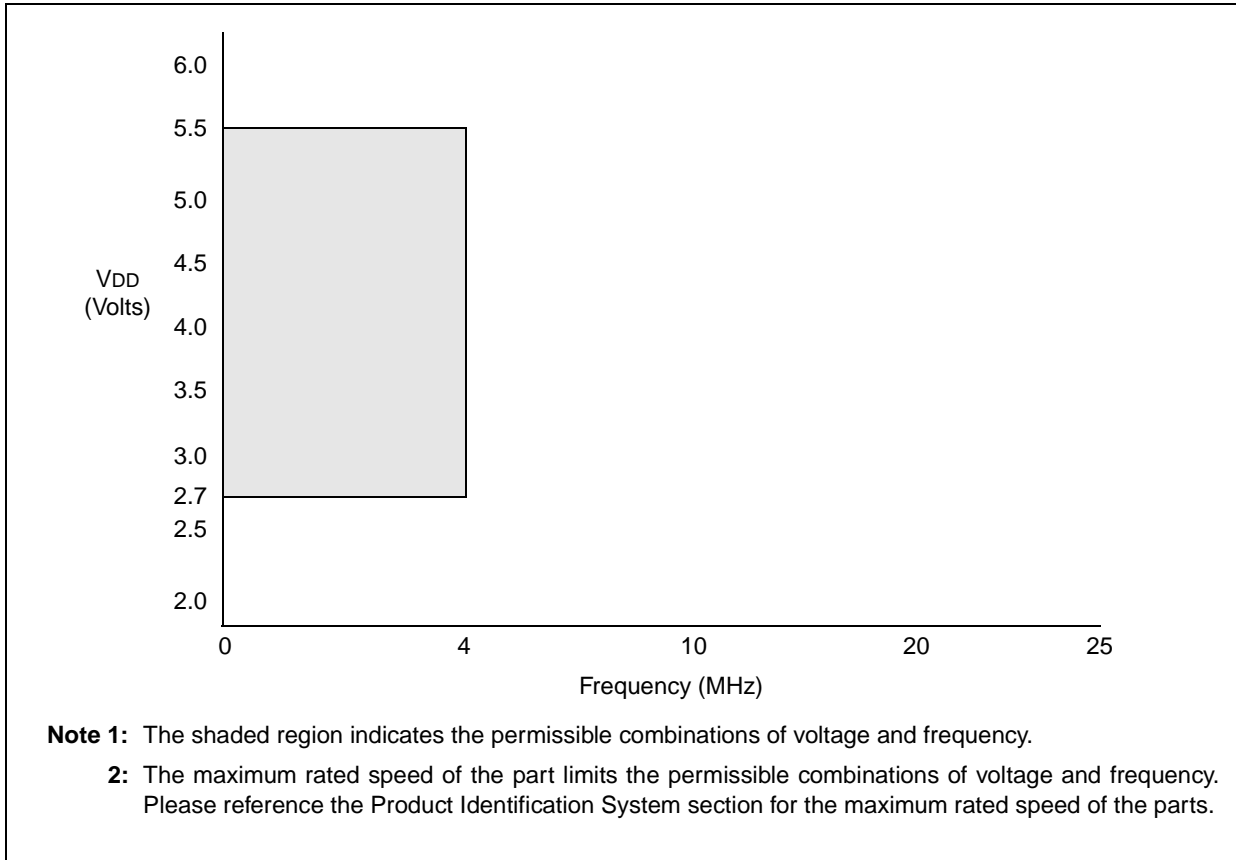


FIGURE 2: PIC16LC58B VOLTAGE-FREQUENCY GRAPH, $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$

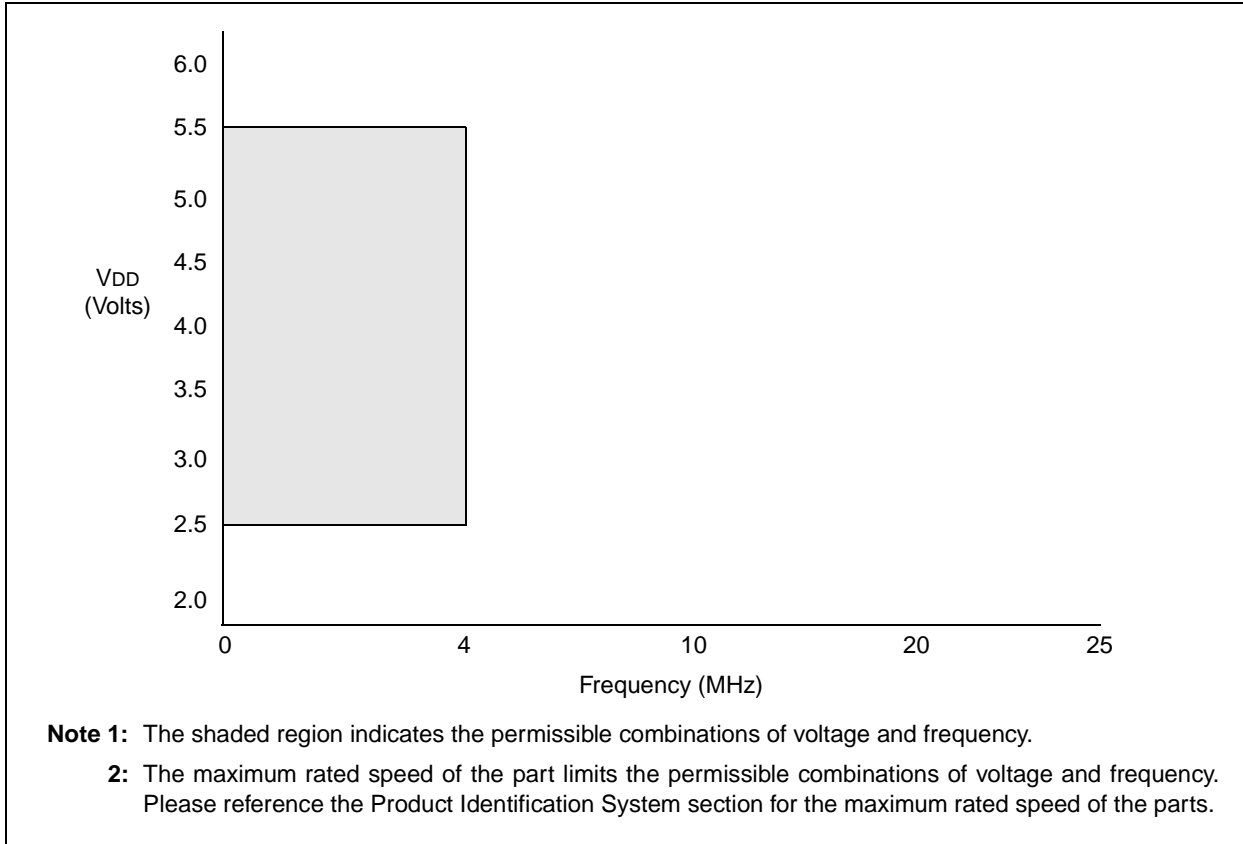
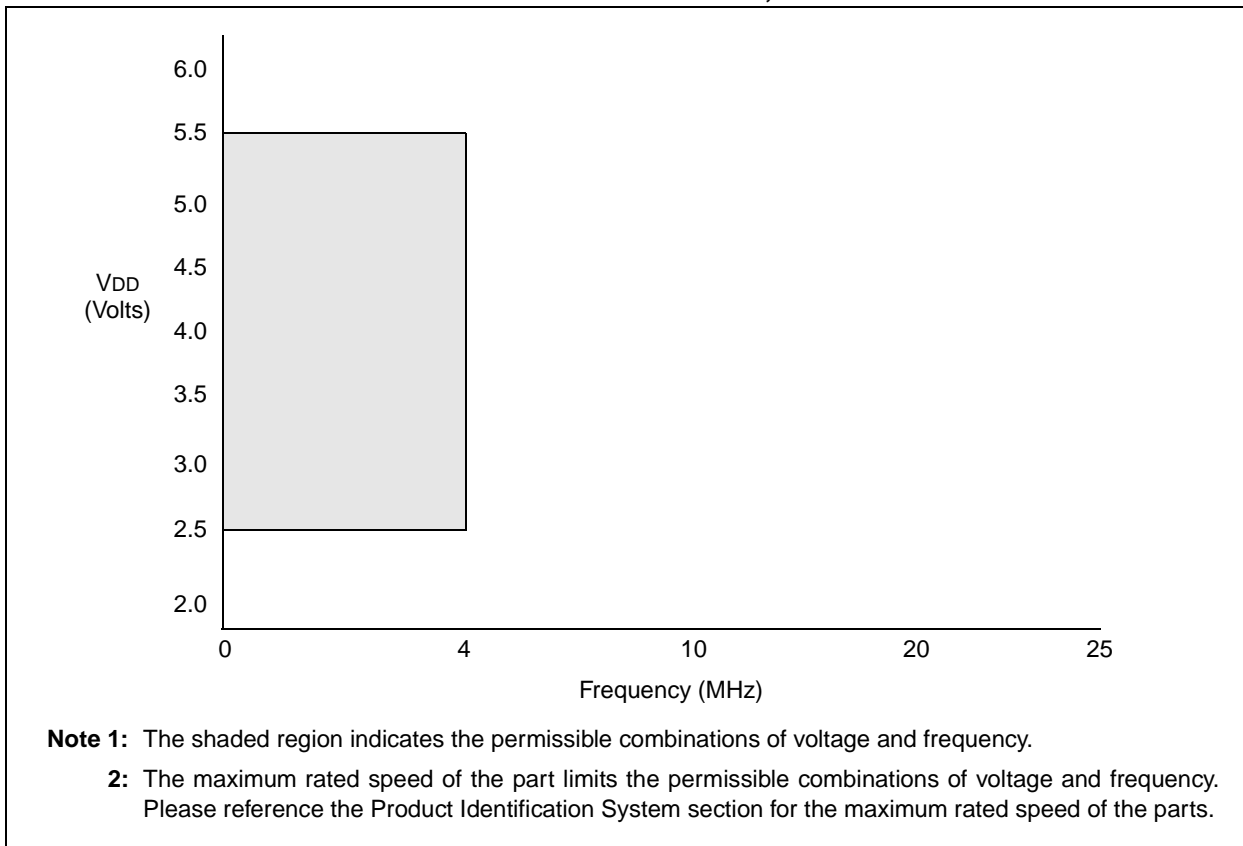


FIGURE 3: PIC16LC58B VOLTAGE-FREQUENCY GRAPH, $+70^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$



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Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS30453B), the following clarifications and corrections should be noted.

FIGURE 1: PIC16C58B VOLTAGE-FREQUENCY GRAPH, $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$

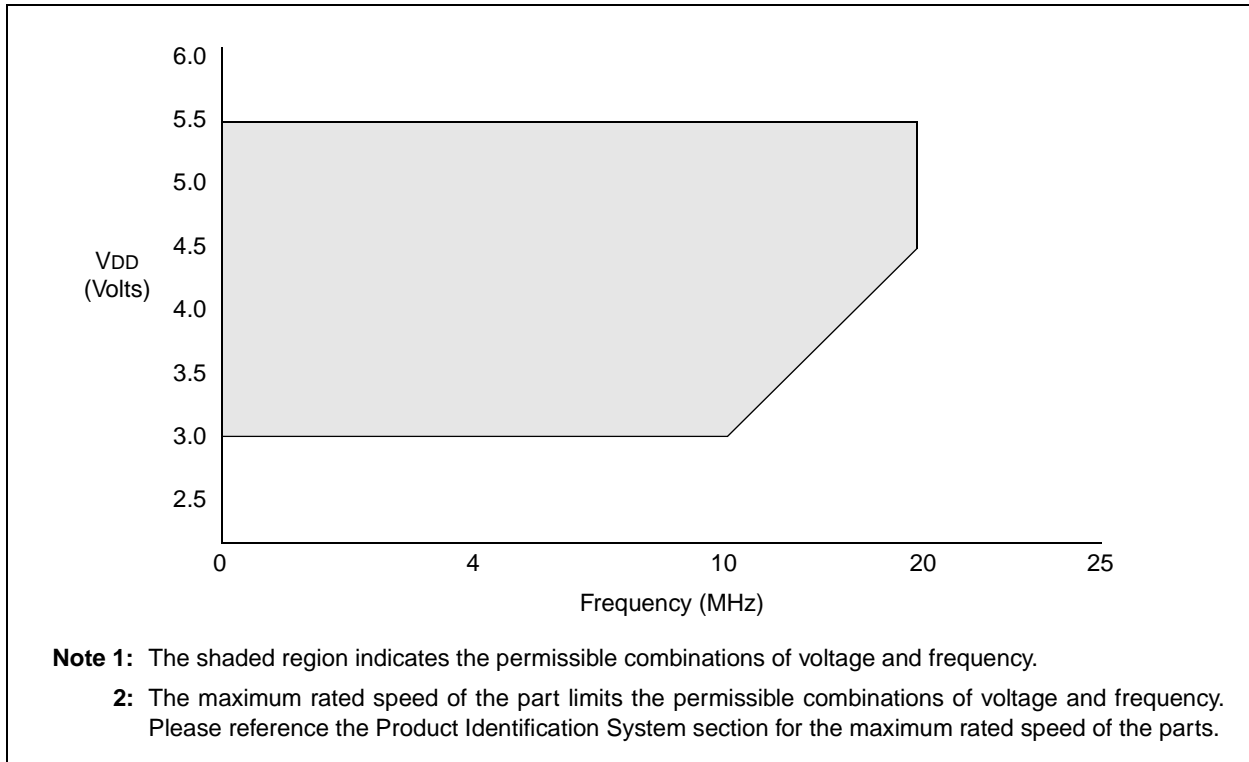
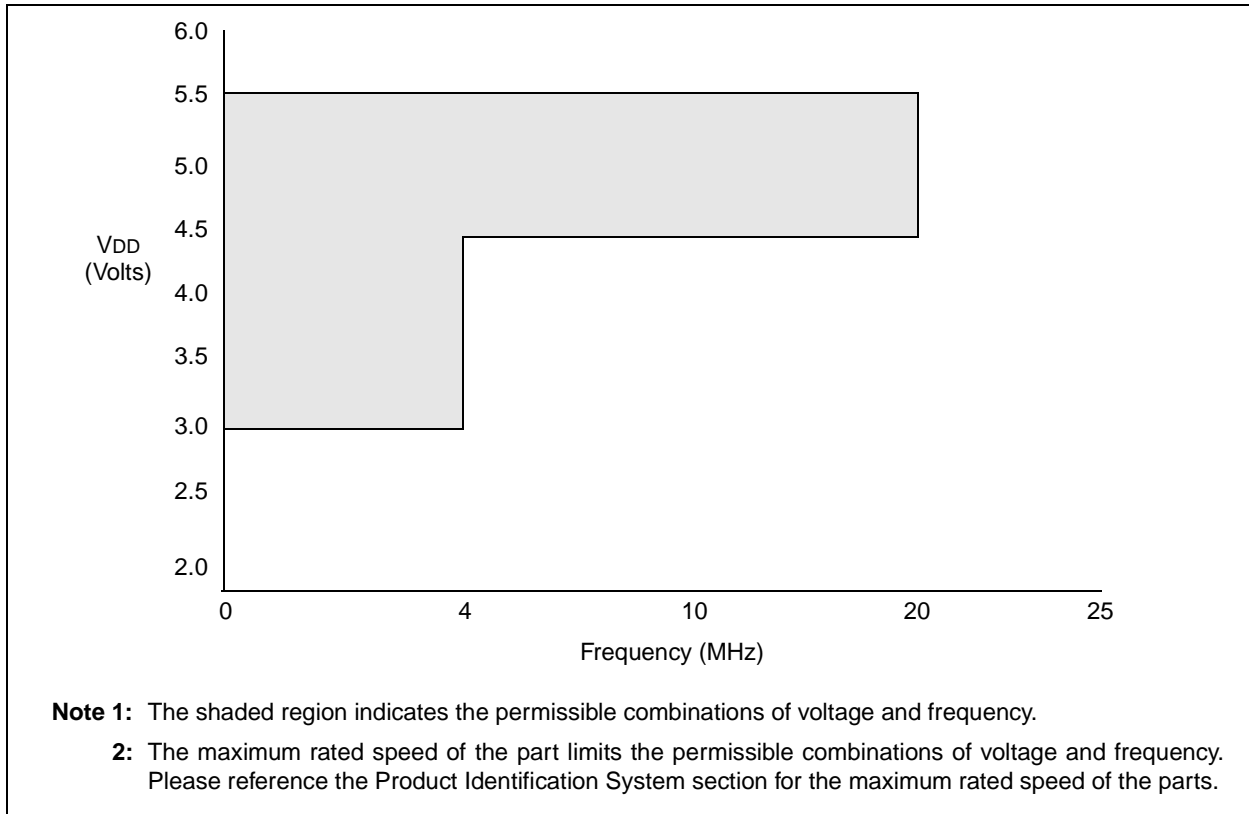


FIGURE 2: PIC16C58B VOLTAGE-FREQUENCY GRAPH, $-40^{\circ}\text{C} \leq T_A < 0^{\circ}\text{C}$, $+70^{\circ}\text{C} < T_A \leq +125^{\circ}\text{C}$



19.1 DC Characteristics: PIC16C54B/C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial)
PIC16CR54B/CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial)
PIC16C54B/C54C/C55A/C56A/C57C/C58B-04I, 20I (Industrial)
PIC16CR54B/CR54C/CR56A/CR57C/CR58B-04I, 20I (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions
Supply Voltage	VDD	3.0	—	5.5	V	
RAM Data Retention Voltage ⁽²⁾	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD rise rate to ensure Power-On Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current ⁽³⁾⁽⁴⁾	IDD	—	1.8	2.4	mA	FOSC = 4 MHz, VDD = 5.5V, XT mode
		—	2.6	3.6	mA	FOSC = 10 MHz, VDD = 3.0V, HS mode
		—	4.5	16	mA	FOSC = 20 MHz, VDD = 5.5V, HS mode
		—	14	32	μA	FOSC = 32 kHz, VDD = 3.0V, LP mode, Commercial
		—	17	40	μA	FOSC = 32 kHz, VDD = 3.0V, LP mode, Industrial
Power Down Current ⁽⁵⁾	IPD	—	0.25	4.0	μA	VDD = 3.0V, WDT disabled, Commercial
		—	0.25	5.0	μA	VDD = 3.0V, WDT disabled, Industrial
		—	1.8	7.0	μA	VDD = 5.5V, Commercial
		—	2.0	8.0	μA	VDD = 5.5V, Industrial
Watchdog Timer Current	ΔIWDT	—	3.75	8.0	μA	VDD = 3.0V, Commercial
		—	3.75	9.0	μA	VDD = 3.0V, Industrial
		—	8	20	μA	VDD = 5.5V*, Commercial
		—	10	22	μA	VDD = 5.5V*, Industrial
LP Oscillator Operating Frequency	Fosc	0	—	200	kHz	All temperatures
RC Oscillator Operating Frequency		0	—	4	MHz	All temperatures
XT Oscillator Operating Frequency		0	—	4	MHz	All temperatures
HS Oscillator Operating Frequency		0	—	20	MHz	All temperatures

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
- 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are:
 OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT disabled.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
- 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
- 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

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19.2 DC Characteristics: PIC16C54B/C54C/C55A/C56A/C57C/C58B-04E, 20E (Extended) PIC16CR54B/CR54C/CR56A/CR57C/CR58B-04E, 20E (Extended)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended)				
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions
Supply Voltage	VDD	3.0	—	5.5	V	
RAM Data Retention Voltage ⁽²⁾	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD rise rate to ensure Power-On Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current ⁽³⁾⁽⁴⁾	IDD	—	1.8 9.0	3.3 20	mA mA	FOSC = 4 MHz, VDD = 5.5V, XT mode FOSC = 20 MHz, VDD = 5.5V, HS mode
Power Down Current ⁽⁵⁾	IPD	—	0.3 10 12	17 50 60	μA μA μA	VDD = 3.0V, WDT disabled VDD = 4.5V, WDT disabled VDD = 5.5V, WDT disabled
Watchdog Timer Current	ΔI_{WDT}	—	4.5 8.0 14	14 18 30	μA μA μA	VDD = 3.0V VDD = 4.5V* VDD = 5.5V*
LP Oscillator Operating Frequency	Fosc	0	—	200	kHz	All temperatures
RC Oscillator Operating Frequency		0	—	4	MHz	All temperatures
XT Oscillator Operating Frequency		0	—	4	MHz	All temperatures
HS Oscillator Operating Frequency		0	—	20	MHz	All temperatures

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to

VSS, T0CKI = VDD, MCLR = VDD; WDT disabled.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula: $I_R = V_{DD}/2R_{ext}$ (mA) with Rext in k Ω .

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

19.3 DC Characteristics: PIC16LC5X-04, PIC16LCR5X-04 (Commercial) PIC16LC5X-04I, PIC16LCR5X-04I (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions
Supply Voltage	VDD	2.5	—	5.5	V	
RAM Data Retention Voltage ⁽²⁾	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD rise rate to ensure Power-On Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current ⁽³⁾⁽⁴⁾	IDD	—	0.4 0.5 11 14	0.6 2.4 27 35	mA mA μA μA	FOSC = 4.0 MHz, VDD = 2.5V, XT mode FOSC = 4.0 MHz, VDD = 5.5V, XT mode FOSC = 32 kHz, VDD = 2.5V, LP mode, Commercial FOSC = 32 kHz, VDD = 2.5V, LP mode, Industrial
Power Down Current ⁽⁵⁾	IPD	—	0.25 0.25	2.0 3.0	μA μA	VDD = 2.5V, WDT disabled, Commercial VDD = 2.5V, WDT disabled, Industrial
Watchdog Timer Current	ΔIWDT	—	0.8 1.0	3.0 5.0	μA μA	VDD = 2.5V, Commercial VDD = 2.5V, Industrial
LP Oscillator Operating Frequency	Fosc	0	—	200	kHz	All temperatures
RC Oscillator Operating Frequency		0	—	4	MHz	All temperatures
XT Oscillator Operating Frequency		0	—	4	MHz	All temperatures
HS Oscillator Operating Frequency		0	—	20	MHz	All temperatures

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT disabled.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

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19.4 DC Characteristics: PIC16C54B/C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial, Extended)
PIC16LC54B/LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial)
PIC16CR54B/CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial, Extended)
PIC16LCR54B/LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

Characteristic		Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions
DC Characteristics All Pins Except Power Supply Pins		Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial) -40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 19.1, Section 19.2 and Section 19.3.					
Input Low Voltage		VIL					
I/O Ports			VSS	—	0.8 V	V	4.5V < VDD ≤ 5.5V
I/O Ports			VSS	—	0.15 VDD	V	otherwise
MCLR (Schmitt Trigger)			VSS	—	0.15 VDD	V	
T0CKI (Schmitt Trigger)			VSS	—	0.15 VDD	V	
OSC1 (Schmitt Trigger)			VSS	—	0.15 VDD	V	RC option only ⁽⁴⁾
OSC1					0.3 VDD	—	XT, HS and LP options
Input High Voltage		VIH					
I/O ports			2.0	—	VDD	V	4.5V < VDD ≤ 5.5V ⁽⁵⁾
I/O ports			0.25 VDD+0.8V	—	VDD	V	otherwise
MCLR (Schmitt Trigger)			0.85 VDD	—	VDD	V	
T0CKI (Schmitt Trigger)			0.85 VDD	—	VDD	V	
OSC1 (Schmitt Trigger)			0.85 VDD	—	VDD	V	RC option only ⁽⁴⁾
OSC1			0.7 VDD	—	VDD	V	XT, HS and LP options
Hysteresis of Schmitt Trigger inputs		VHYS	0.15VDD*	—	—	V	
Input Leakage Current⁽³⁾		IIL					For VDD ≤ 5.5V
I/O ports			-1.0	0.5	+1.0	μA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR			-5.0	—	+5.0	μA	VPIN = VSS + 0.25V ⁽²⁾
MCLR				0.5	+3.0	μA	VPIN = VDD ⁽²⁾
T0CKI			-3.0	0.5	+3.0	μA	VSS ≤ VPIN ≤ VDD
OSC1			-3.0	0.5	—	μA	VSS ≤ VPIN ≤ VDD, XT, HS and LP options
Output Low Voltage		VOL					
I/O ports			—	—	0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT			—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, RC option only
Output High Voltage		VOH					
I/O ports ⁽³⁾			VDD-0.7	—	—	V	IOH = -5.4 mA, VDD = 4.5V
OSC2/CLKOUT			VDD-0.7	—	—	V	IOH = -1.0 mA, VDD = 4.5V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

NOTES:



WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

Microchip Technology Inc.
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-786-7200 Fax: 480-786-7277
Technical Support: 480-786-7627
Web Address: <http://www.microchip.com>

Atlanta

Microchip Technology Inc.
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Boston

Microchip Technology Inc.
5 Mount Royal Avenue
Marlborough, MA 01752
Tel: 508-480-9990 Fax: 508-480-8575

Chicago

Microchip Technology Inc.
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas

Microchip Technology Inc.
4570 Westgrove Drive, Suite 160
Addison, TX 75248
Tel: 972-818-7423 Fax: 972-818-2924

Dayton

Microchip Technology Inc.
Two Prestige Place, Suite 150
Miamisburg, OH 45342
Tel: 937-291-1654 Fax: 937-291-9175

Detroit

Microchip Technology Inc.
Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Los Angeles

Microchip Technology Inc.
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

New York

Microchip Technology Inc.
150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose

Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

AMERICAS (continued)

Toronto

Microchip Technology Inc.
5925 Airport Road, Suite 200
Mississauga, Ontario L4V 1W1, Canada
Tel: 905-405-6279 Fax: 905-405-6253

ASIA/PACIFIC

Hong Kong

Microchip Asia Pacific
Unit 2101, Tower 2
Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2-401-1200 Fax: 852-2-401-3431

Beijing

Microchip Technology, Beijing
Unit 915, 6 Chaoyangmen Bei Dajie
Dong Erhuan Road, Dongcheng District
New China Hong Kong Manhattan Building
Beijing 100027 PRC
Tel: 86-10-85282100 Fax: 86-10-85282104

India

Microchip Technology Inc.
India Liaison Office
No. 6, Legacy, Convent Road
Bangalore 560 025, India
Tel: 91-80-229-0061 Fax: 91-80-229-0062

Japan

Microchip Technology Intl. Inc.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa 222-0033 Japan
Tel: 81-45-471-6166 Fax: 81-45-471-6122

Korea

Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Shanghai

Microchip Technology
Unit B701, Far East International Plaza,
No. 317, Xianxia Road
Shanghai, 200051 P.R.C.
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

ASIA/PACIFIC (continued)

Singapore

Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan, R.O.C

Microchip Technology Taiwan
10F-1C 207
Tung Hua North Road
Taipei, Taiwan, ROC
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

United Kingdom

Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5858 Fax: 44-118 921-5835

Denmark

Microchip Technology Denmark ApS
Regus Business Centre
Lautrup hof 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France

Arizona Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

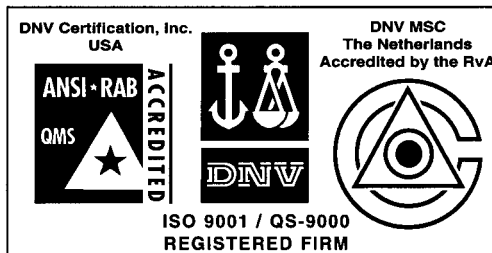
Germany

Arizona Microchip Technology GmbH
Gustav-Heinemann-Ring 125
D-81739 München, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy

Arizona Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

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