PIC18CXX2

PIC18CXX2 Rev. B Silicon Errata Sheet

The PIC18CXX2 (Rev. B) parts you have received conform functionally to the Device Data Sheet (DS39026**B**), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC18CXX2 silicon.

1. Module: CPU

Using the LFSR instruction to load a value into the specified FSR register, may also corrupt a RAM location.

Work around

Do not use the LFSR instruction. The use of MOVLW and MOVWF instructions can be implemented to load the FSR registers. The WREG register may need to be saved before these operations and restored afterwards.

EXAMPLE 1: DEFINED OPERATION

```
    LFSR        FSR1, Pointer
```

EXAMPLE 2: WORK AROUND

```
;
; Optionally save the WREG register
;
    MOVLW       HIGH (Pointer)
    MOVWF       FSR1H
    MOVLW       LOW (Pointer)
    MOVWF       FSR1L
;
; Optionally restore the WREG register
;
```

2. Module: CCP

When the CCP module is configured to Compare mode toggle output pin (CCPxCON = b'00xx0010'), unexpected pin operation may be observed.

When the timer used for the CCP module time-base is configured to have a prescale ratio greater than 1:1, the output on the CCP pin will toggle the prescaled number of times for each compare match. That is, for a n:1 timer prescale ratio, the CCP output pin will toggle n times at each compare match. The toggle occurs each instruction cycle (T_{CY}).

Work around

The prescale ratio for the timer used as the CCP module time-base must be 1:1. If a longer compare time is needed, the timer must be running in Timer mode or Synchronized Counter mode (external clock source).

Date Codes that pertain to this issue:

ALL

Note: When the manufacture date of a newer version of silicon is in production, the last date where this issue may occur, will be specified.

3. Module: Oscillator

In-Circuit Serial Programming™ (ICSP) may become unpredictable, when a free-running clock source is present on OSC1.

When entering ICSP mode, the PIC18C452 switches from OSC1 to RB6 for its external clock source. (Refer to the PIC18CXX2 Programming Specification (DS39028D) for additional information.) If OSC1 is high at the time, a high-to-low transition occurs upon the transition to RB6.The ICSP logic interprets this as a clock, and advances the internal clock logic to Q2. This causes an unrecoverable mismatch between ICSP logic and the clock.

Work around

Before entering ICSP mode, OSC1 must be driven to and held in a low state. This must occur before changing states on $\overline{MCLR}/V_{PP}$, RB6 and RB7.

Note: As with any windowed EPROM device, please cover the window at all times, except when erasing.

4. Module: CCP (Compare Mode)

The Compare mode may not operate as expected when configuring the compare match to drive the I/O pin low (CCPxM<3:0> = 1001).

When the CCP module is changed to compare output low (CCPxM<3:0> = 1001) from any other non-compare CCP mode, the I/O pin will immediately be driven low, regardless of the state of the I/O data latch. The pin will remain low when the compare match occurs (see Table 1).

However, when the CCP module is changed to compare output high (CCPxM<3:0> = 1000) from any other CCP mode, the I/O pin will immediately be driven low, regardless of the state of the I/O data latch. The pin will be driven high when the compare match occurs.

TABLE 1: COMPARE OUTPUT LOW SWITCHING

CCP Mode CCPxM<3:0> =	I/O Pin State	Change CCP to CCPxM<3:0> =	
		1001	1000
0xxx	H	L	L
	L	L	L
1000	H	H	—
	L	L	—
1001	H	—	L
	L	—	L
101x	H	L	L
	L	L	L
11xx	H	L	L
	L	L	L

Work around

To have the I/O pin high until the compare match low occurs, force a compare match high to get the I/O pin into the high state, then reconfigure the compare match to force the I/O low when the compare condition occurs.

5. Module: Timer1 and Timer3

When the prescaler select bits (bits 5:4 of the T1CON or T3CON registers) are modified, the timer may inadvertently increment. This can occur even if the timer is in the OFF state. Changing the prescaler may cause clock glitches, which may cause the counter to increment improperly.

Work around

Always re-initialize the timer registers (either TMR1H and TMR1L, or TMR3H and TMR3L) after changing the prescaler bits of registers T1CON or T3CON.

As an alternative, store the timer value before changing the prescaler bits of the timer control registers, and restore the timer value after changing the bits.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39026**B**), the following clarifications and corrections should be noted.

1. Module: Brown-out Reset (BOR)

The voltage selection ranges for the BOR module (parameter D005) have changed. The new values are shown in Table 1.

TABLE 1: MINIMUM AND MAXIMUM BROWN-OUT RESET VOLTAGE SPECIFICATIONS

Param No	Symbol	Characteristic		New Specification			Data Sheet Specification			Units
				Min	Typ	Max	Min	Typ	Max	
D005	VBOR	Brown-out Reset Voltage	BORV<1:0>=11	2.35	—	2.80	2.50	—	2.66	V
			BORV<1:0>=10	2.55	—	3.02	2.70	—	2.86	V
			BORV<1:0>=01	3.95	—	4.71	4.20	—	4.46	V
			BORV<1:0>=00	4.23	—	5.05	4.50	—	4.78	V

2. Module: Low Voltage Detect (LVD)

The voltage selection ranges for the LVD module (parameter D420) have changed. The new values are shown in Table 2.

TABLE 2: MINIMUM AND MAXIMUM LOW VOLTAGE DETECT SPECIFICATIONS

Param No	Symbol	Characteristic		New Specification			Data Sheet Specification			Units
				Min	Typ	Max	Min	Typ	Max	
D420	VLVD	Low Voltage Detect	LVV<3:0>=0100	2.35	—	2.80	2.5	—	2.66	V
			LVV<3:0>=0101	2.55	—	3.02	2.7	—	2.86	V
			LVV<3:0>=0110	2.64	—	3.14	2.8	—	2.98	V
			LVV<3:0>=0111	2.83	—	3.37	3.0	—	3.20	V
			LVV<3:0>=1000	3.11	—	3.71	3.3	—	3.52	V
			LVV<3:0>=1001	3.29	—	3.93	3.5	—	3.72	V
			LVV<3:0>=1010	3.39	—	4.04	3.6	—	3.84	V
			LVV<3:0>=1011	3.58	—	4.26	3.8	—	4.04	V
			LVV<3:0>=1100	3.77	—	4.49	4.0	—	4.26	V
			LVV<3:0>=1101	3.95	—	4.71	4.2	—	4.46	V
			LVV<3:0>=1110	4.23	—	5.05	4.5	—	4.78	V

REVISION HISTORY

Rev D Document
Added Corrections to BOR and LVD modules (page 3, items 1 and 2).

Rev C Document
Added ICSP issue (page 1, issue 3).

Added CCP (Compare mode) issue (page 2, issue 4).

Added Timer issue (page 2, issue 5).

Rev B Document
Added CCP silicon issue (page 1, issue 2).

Rev A Document
1st revision of this document.

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01/30/01