MCP2510

MCP2510 Rev. A Silicon Errata Sheet

The MCP2510 (Rev. A) parts you have received conform functionally to the Device Data Sheet (DS21291C), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the MCP2510 silicon.

1. Module: Configuration Mode State Machine

   The device may not enter Normal mode after a valid request to enter Normal mode (by writing the REQOP2:REQOP0 bits to '100').

   <u>Work Around</u>

   After requesting Normal mode, always read the OPMODE2:OPMODE0 bits (CANSTAT register) to confirm that the device entered into Normal mode. If these bits do not reflect Normal mode, reset the device to Configuration mode by writing the REQOP2:REQOP0 bits to '100' (CANCTRL register). Then request Normal mode (by writing the REQOP2:REQOP0 bits to '000'). Read the OPMODE2:OPMODE0 bits (CANSTAT register) to confirm that the device is in Normal mode.

2. Module: Configuration Mode State Machine

   Sleep mode is entered when the REQOP2:REQOP0 bits (CANCTRL register) are modified from 'x00' → 'xx1').

   <u>Work Around</u>

   There are two cases where the REQOP2:REQOP0 bits can be modified.

   Case 1:

   REQOP2:REQOP0 is modified from '000' → '001'. In this case, Sleep mode is desired and the operation is intended.

   Case 2:

   REQOP2:REQOP0 is modified from '000' → '011'. In this case, Listen Only mode is desired but the device enters Sleep mode.

   The work around is to first place the device into Loopback mode (REQOP2:REQOP0 is modified from '000' → '010') and then select Listen Only mode (REQOP2:REQOP0 is modified from '010' → '011').

3. Module: Configuration Mode State Machine

   Configuring the REQOP2:REQOP0 bits (CANCTRL register) to enter Listen Only mode ('011') may cause the device to enter Sleep Mode.

   <u>Work Around</u>

   First configure the REQOP2:REQOP0 bits (CAN-CTRL register) to enter Loopback Mode ('010'). Then configure the REQOP2:REQOP0 bits to enter Listen Only mode ('011').

4. Module: Error Flags

   The TXWAR bit (EFLG register) will be set when the TEC register increments from 96 to 97 (decimal) and from 224 to 225 (decimal). The first condition is specified in the data sheet, but the second is not a specified operation.

Note 1:	The EWARN bit (EFLG register) is automatically set when the TXWAR bit becomes set.
Note 2:	If the ERRIE bit (CANINTE register) is set, an interrupt will be generated. The microcontrollers Interrupt service routine (ISR) will need to be written to address this.

   <u>Work Around</u>

   None

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5. Module: Bus Timing Logic

Transmission of a pending message may not start immediately after the 11 recessive bit times following the previous message frame's ACK slot bit. A delay of between zero and two additional bit times may occur before transmission of the message.

This may only occur when a message is queued for transmission (by setting the TXREQ bit (TXBnCTRL register) for the buffer) while receiving a message. If the message is received (i.e. transferred to a receive buffer) by passing the mask and filter values, a delay of between zero and two additional bit times occurs before the pending message is transmitted. If the received message is rejected (based on the mask and filter values), no addition bit time delay occurs.

This additional message transmission delay is a function of the total number of OSC1 clocks per bit time. By setting the total number of OSC1 clocks per bit time to 26 or greater, this delay will always be zero and the issue does not exist. If the number of OSC1 clocks per bit time is between 18 and 24, the delay will be one bit time, and if the number of OSC1 clocks per bit time is less than 18, the delay will be two bit times.

Work Around

Provide 26 or more OSC1 clocks per bit time. To provide 26 or more OSC1 clocks per bit time, the user should do one or more of the following:

- Use a higher speed oscillator for a given nominal bit time (this allows the value in BRP5:BRP0 to be increased, thereby increasing the time of T_Q)
- Increase the BRP5:BRP0 value
- Increase the number of T_Q per nominal bit time

The number of OSC1 clocks per bit time is determined by two things:

- The baud rate prescaler setting
- The total number of T_Q in a bit time

The baud rate prescaler (BRP5:BRP0) bits control the number of OSC1 clocks per T_Q. The minimum number of OSC1 clocks per T_Q is 2 (for BRP5:BRP0 = 000000). This number can be increased by increasing the baud rate prescaler setting in the CNF1 register. A BRP5:BRP0 value of 000001 doubles the number of OSC1 clocks per T_Q to 4, a BRP5:BRP0 value of 000010 doubles this again to 8, etc.

The total number of T_Q in a bit time is a simple multiplier to the number of OSC1 clocks per T_Q which yields the number of OSC1 clocks that occur during a bit time. This is shown in Equation 1.

EQUATION 1:   CALCULATION OF OSC1 CLOCKS

$$\#OSC1\ clocks = 2 \bullet (BRP5{:}BRP0 + 1) \bullet \frac{\#\ T_Q}{bit\ time}$$

Table 1 shows common CAN bus speeds and how to set up the other parameters to meet 26 OSC1 clocks per bit time, so no additional delays occur.

TABLE 1:   CAN BUS SPEEDS AND OSC1 CLOCKS PER BIT TIME

CAN Bus Speed (Bits/Second)	Minimum OSC1 Frequency (MHz)	Baud Rate Prescaler (BRP5:BRP0)	# of T_Q's per Bit Time	Clocks per Bit Time	Comment
125K	4	000000	16	32	No additional delay occurs
125K	4	000001	8	32	No additional delay occurs
250K	4	000000	8	16	Additional delay occurs
250K	8	000000	16	32	No additional delay occurs
250K	8	000001	8	32	No additional delay occurs
500K	8	000000	8	16	Additional delay occurs
500K	16	000000	16	32	No additional delay occurs
500K	16	000001	8	32	No additional delay occurs

6. Module: Receive Logic

Data from a Received message may be corrupted when three messages (Message #1, #2, and #3) are received (back-to-back-to-back). This corruption occurs when all messages are destined for the same receive buffer, message #2 and #3 both match the same filter.

Since Message #1 is not serviced until message #3 begins to be received into the Message Acceptance Buffer (MAB). Message #2 which is currently in the MAB, starts to be overwritten by the reception of Message #3. Once the RXnIF bit is cleared, the contents of the MAB is loaded into the Receive Buffer. The value loaded into the Receive Buffer will contain part of message #2 and part of Message #3.

Work Around

The RXnOVR bit (EFLG register) must be checked before accepting each message. If this bit is set, the message that is currently in the receive buffer must be discarded (since the data could be corrupted). If data is not to be lost, the system should implement a handshaking protocol for data transfers.

7. Module: Receive Logic

Invalid data will be transmitted every time there are two messages (Message #1 and #2) received and one message (Message #3) transmitted (back-to-back-to-back). This invalid data will be transmitted when Message #1 and Message #2 are destined for the same receive buffer, and if the 1st received message has not been serviced (i.e. RXnIF cleared) before the start of transmission of Message #3.

Since Message #1 does not get serviced until message #3 is being transmitted. The receive flag is cleared and message #2 begins moving into the receive buffer. At this point, the transmitting message malfunctions and random and repeating data is transmitted.

Work Around

Checking for a transmitting message before clearing the RXnIF bit (CANINTF register) and waiting to clear the receive interrupt until after the appropriate TXREQ bit is cleared signifying the message is done transmitting. This can be done via an SPI™ Read Status command.

8. Module: Receive Buffer 0

The Receive Buffer 0 FILHIT0 bit (RXB0CTRL register) does not function. This bit is stuck clear, and can not be used to determine which filter match occurred to receive the Message into Receive Buffer 0.

Work Around

None

9. Module: Receive Buffer 0

When the device is in Listen Only mode, the Receive Buffer 0 RX0OVR bit (EFLG register) is set whenever an error occurs on the CAN bus.

Work Around

None

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10. Module: SPI Interface

The Output Valid from Clock Low timing specification (Tv) for the SPI interface may exceed the maximum specification shown in the data sheet. The new tested specification is shown in Table 3.

This can occur when the SPI "Read" command (0x03) is used for sequentially reading multiple bytes from certain registers. These registers are shown in Table 2. Only sequential reads of these registers will cause the Tv specification to be exceeded. Byte reads will not affect the Tv specification.

> **Note:** Sequential reads of all other SRAM registers, including the Transmit and Receive Buffers, are unaffected.

TABLE 2:   REGISTERS AFFECTED

Register	
Name	**Address**
RXFnSIDH RXFnSIDL RXFnEID8 RXFnEID0	0x00 - 0x0B 0x10 - 0x1B
RXMnSIDH RXMnSIDL RXMnEID8 RXMnEID0	0x20 - 0x27
CNF2	0x29
CNF1	0x2A
CANSTAT	0xnE [1]
CANCNTL	0xnF [1]
TEC	0x1C
REC	0x1D
CANINTE	0x2B
CANINTF	0x2C
EFLG	0x2D

Note 1: $0 \leq n \leq 7$

<u>Work Around</u>

There are two potential work arounds that can be implemented:

1   Ensure that the SPI clock frequency is less than 4.25 MHz.

2   If the SPI clock is greater than 4.25 MHz, check the Data Setup Time (T$_{SU}$) requirements of the microcontroller's SPI port to determine if T$_V$ is an issue.

If T$_V$ is an issue, use byte reads (single byte) when reading multiple bytes of the registers listed in Table 2. Typical applications configure the MCP2510 by programming most of these registers during initialization and subsequent sequential reads are not required. However, if it becomes necessary to read these registers, they may be read individually (as opposed to sequentially) without violating the Data Sheet T$_V$ specification.

TABLE 3:   TESTED TIMING SPECIFICATIONS

| Parm No. | Sym. | Characteristic | Specification | | | | Units | Condition |
| | | | Tested | | Data Sheet | | | |
			Min	Max	Min	Max		
—	T$_V$	Output Valid from Clock Low						When sequentially reading multiple bytes from registers shown in Table 2.
			—	115	—	90	nS	V$_{DD}$ = 4.5V to 5.5V (I$_{TEMP}$)
			—	115	—	115	nS	V$_{DD}$ = 4.5V to 5.5V (E$_{TEMP}$)
			—	180	—	180	nS	V$_{DD}$ = 3.0V to 4.5V

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11. Module: Receive Buffer 1

The Receive Buffer 1 RXRTR bit (RXB1CTRL register) does not function properly. After the RXRTR bit has been set by an RTR event, it can not be cleared. This includes the reception of subsequent non-RTR messages into Receive Buffer 1.

If a CAN bus system does not use RTR messages, then this is not an issue.

Work Around

If a CAN bus system uses Remote Transmission Request messages for Receive Buffer 1, it is recommended that the RTR status be read directly from the appropriate Receive Buffer 1 register (not from the RXB1CTRL register).

For a Standard RTR Frame, the RTR status is indicated by the SRR bit (RXB1SIDL register). For an Extended RTR Frame, the RTR status is indicated by the RTR bit (RXB1DLC register).

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS21291C), the following clarifications and corrections should be noted.

None

REVISION HISTORY

Rev. A Document

1st revision of this document.

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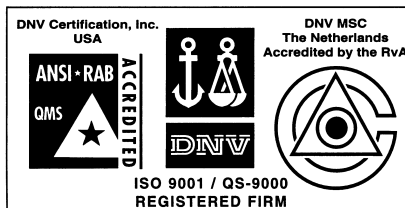
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