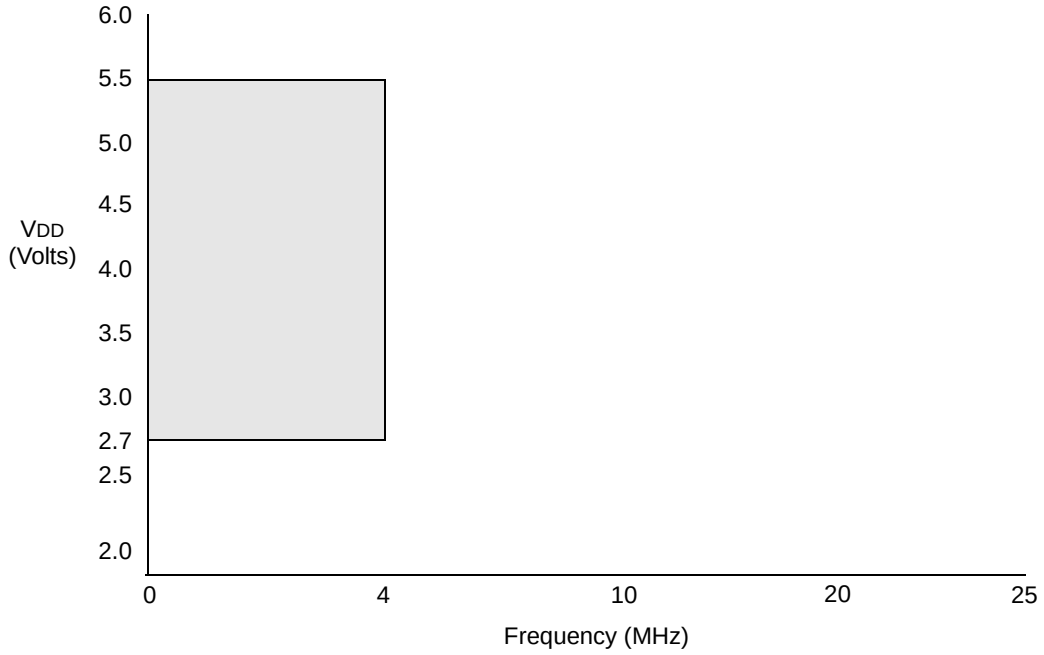
PIC12C508A/C509A/CR509A

PIC12C508A/C509A/CR509A Rev. B Silicon Errata Sheet

The PIC12C508A/C509A/CR509A (Rev. B) parts you have received conform functionally to the Device Data Sheet (**DS40139**), except for the anomalies described below.

1. Valid regions of operation:

FIGURE 1: PIC12LC508A/LC509A/LCR509A VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ 0°C

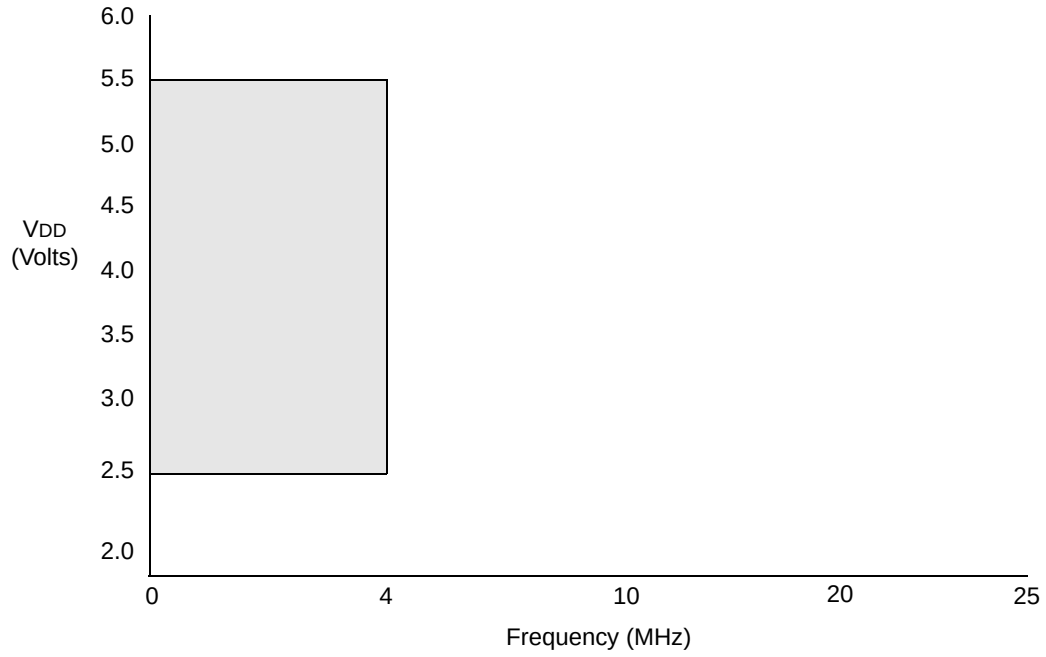


Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

Note: As with any windowed EPROM device, please cover the window at all times, except when erasing.

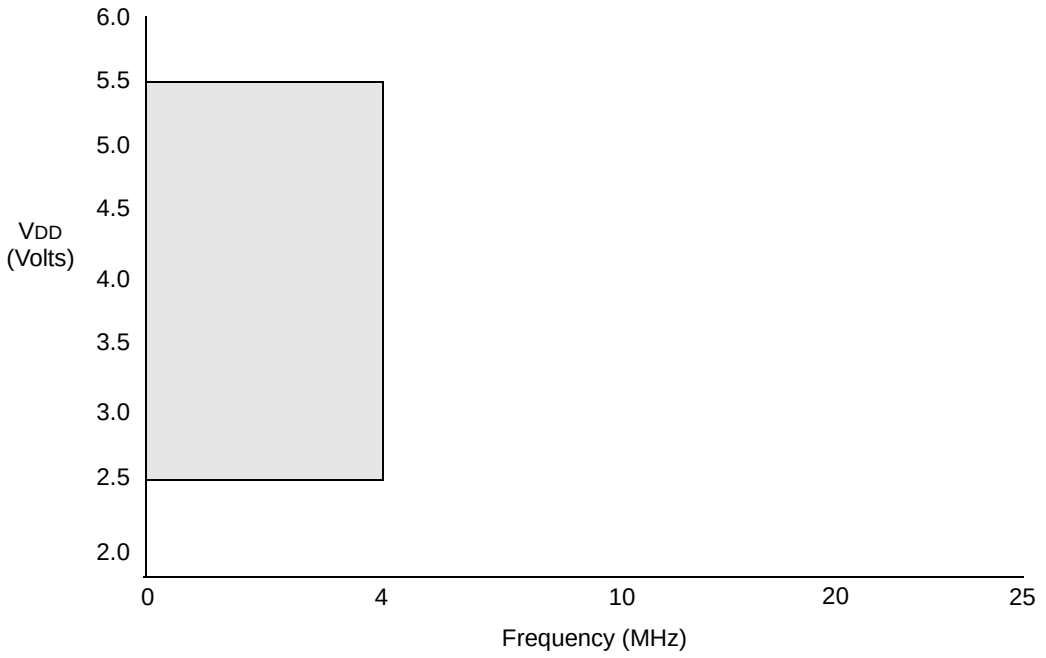
FIGURE 2: PIC12LC508A/LC509A/LCR509A VOLTAGE-FREQUENCY GRAPH, 0°C ≤ TA ≤ +70°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

FIGURE 3: PIC12LC508A/LC509A/LCR509A VOLTAGE-FREQUENCY GRAPH, +70°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

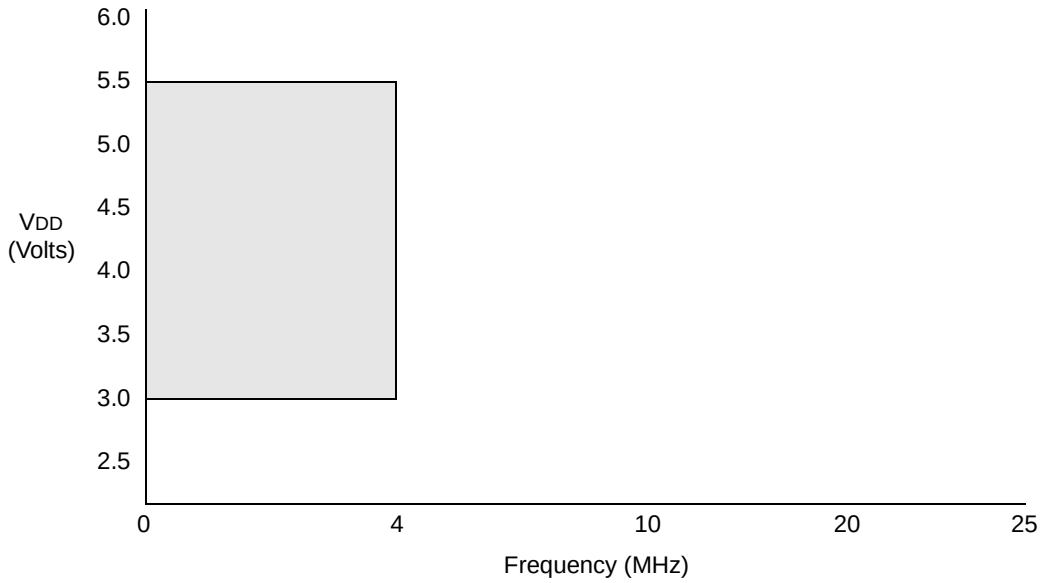
2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (**DS40139E**), the following clarifications and corrections should be noted.

1. Valid regions of operation:

FIGURE 4: PIC12C508A/C509A/CR509A VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

2. Section 13: Corrections for the DC Characteristics, Sections 13.1, 13.2, 13.3, and 13.4 are shown. Corrections for the GPIO pull-up resistor ranges are shown in Table 13-1. For the section titled “Reset”, additional information is provided on OSC1/CLKIN and OSC2/CLKOUT pin states during a $\overline{\text{MCLR}}$.

13.1 DC CHARACTERISTICS: PIC12C508A/509A (Commercial, Industrial, Extended) PIC12CE518/519 (Commercial, Industrial, Extended) PIC12CR509A (Commercial, Industrial, Extended)

DC Characteristics Power Supply Pins			Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended)				
Parm No.	**Characteristic**	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
D001	**Supply Voltage**	VDD	3.0		5.5	V	See Figures 1-4.
D010	**Supply Current(3)**	IDD	—	0.8	1.4	mA	XT and EXTRC options (Note 4) FOSC = 4 MHz, VDD = 5.5V
D010C			—	0.8	1.4	mA	INTRC Option FOSC = 4 MHz, VDD = 5.5V
D010A			—	19	27	µA	Commercial Temperature, LP Option FOSC = 32 kHz, VDD = 3.0V, WDT disabled
			—	19	35	µA	Industrial Temperature, LP Option FOSC = 32 kHz, VDD = 3.0V, WDT disabled
			—	30	55	µA	Extended Temperature, LP Option FOSC = 32 kHz, VDD = 3.0V, WDT disabled
1A	LP Oscillator Operating Frequency XT Oscillator Operating Frequency	FOSC	0 0	– –	200 4	kHz MHz	All temperatures All temperatures

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS,
T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kOhm.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

13.2 DC CHARACTERISTICS: PIC12LC508A/509A (Commercial, Industrial) PIC12LCE518/519 (Commercial, Industrial) PIC12LCR509A (Commercial, Industrial)

DC Characteristics Power Supply Pins			Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)				
Parm No.	**Characteristic**	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
D001	**Supply Voltage**	VDD	2.5		5.5	V	See Figures 1-4.
1A	LP Oscillator Operating Frequency XT Oscillator Operating Frequency	FOSC	0 0	– –	200 4	kHz MHz	All temperatures All temperatures
		ΔIWDT	–	2.0 2.0	4 5	µA µA	VDD = 2.5V, Commercial VDD = 2.5V, Industrial

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss,
T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kOhm.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

13.3 DC CHARACTERISTICS: PIC12C508A/509A (Commercial, Industrial, Extended) PIC12CE518/519 (Commercial, Industrial, Extended) PIC12CR509A (Commercial, Industrial, Extended)

DC CHARACTERISTICS							**Standard Operating Conditions (unless otherwise specified)** Operating temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating voltage VDD range as described in DC spec Section 13.1 and Section 13.2.
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	Input High Voltage						
	I/O ports	VIH		-			
D040	with TTL buffer		2.0V	-	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			0.25VDD + 0.8V	-	VDD	V	otherwise
D070	GPIO weak pull-up current (Note 4)	IPUR	30	250	400	µA	VDD = 5V, VPIN = VSS
	Input Leakage Current (Notes 2, 3)	IIL					
D061	GP3/$\overline{\text{MCLR}}$ (Note 5)		8	130	250	µA	Vss ≤ VPIN ≤ VDD
D061A	GP3/$\overline{\text{MCLR}}$ (Note 6)		-	-	±5	µA	Vss ≤ VPIN ≤ VDD

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12C5XX be driven with external clock in RC mode.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: Does not include GP3. For GP3 see parameters D0061 and D0061A.

5: This spec. applies to GP3/$\overline{\text{MCLR}}$ configured as external $\overline{\text{MCLR}}$ and GP3/$\overline{\text{MCLR}}$ configured as input with internal pull-up enabled.

6: This spec. applies when GP3/$\overline{\text{MCLR}}$ is configured as an input with pull-up disabled. The leakage current of the $\overline{\text{MCLR}}$ circuit is higher than the standard I/O logic.

13.4 DC CHARACTERISTICS: PIC12LC508A/509A (Commercial, Industrial) PIC12LCE518/519 (Commercial, Industrial) PIC12LCR509A (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) Operating voltage VDD range as described in DC spec Section 13.1 and Section 13.2.				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	Input High Voltage						
	I/O ports	VIH		-			
D040	with TTL buffer		2.0V	-	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			0.25VDD + 0.8V	-	VDD	V	otherwise
D070	GPIO weak pull-up current (Note 4)	IPUR	30	250	400	µA	VDD = 5V, VPIN = VSS
	Input Leakage Current (Notes 2, 3)	IIL					
D061	GP3/$\overline{\text{MCLR}}$ (Note 5)		8	130	250	µA	Vss ≤ VPIN ≤ VDD
D061A	GP3/$\overline{\text{MCLR}}$ (Note 6)		-	-	±5	µA	Vss ≤ VPIN ≤ VDD

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12C5XX be driven with external clock in RC mode.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: Does not include GP3. For GP3 see parameters D0061 and D0061A.

5: This spec. applies to GP3/$\overline{\text{MCLR}}$ configured as external $\overline{\text{MCLR}}$ and GP3/$\overline{\text{MCLR}}$ configured as input with internal pull-up enabled.

6: This spec. applies when GP3/$\overline{\text{MCLR}}$ is configured as an input with pull-up disabled. The leakage current of the $\overline{\text{MCLR}}$ circuit is higher than the standard I/O logic.

TABLE 13-1: PULL-UP RESISTOR RANGES* - PIC12C508A, PIC12C509A, PIC12CR509A, PIC12CE518, PIC12CE519, PIC12LC508A, PIC12LC509A, PIC12LCR509A, PIC12LCE518 and PIC12LCE519

VDD (Volts)	Temperature (°C)	Min	Typ	Max	Units
GP0/GP1					
2.5	–40	38K	42K	63K	Ω
	25	42K	48K	63K	Ω
	85	42K	49K	63K	Ω
	125	50K	55K	63K	Ω
5.5	–40	15K	17K	20K	Ω
	25	18K	20K	23K	Ω
	85	19K	22K	25K	Ω
	125	22K	24K	28K	Ω
GP3(1)					
2.5	–40	65K	80K	850K	Ω
	25	80K	100K	1150K	Ω
	85	85K	110K	1300K	Ω
	125	100K	120K	1500K	Ω
5.5	–40	50K	60K	600K	Ω
	25	60K	65K	750K	Ω
	85	65K	80K	900K	Ω
	125	75K	90K	990K	Ω

***** These parameters are characterized but not tested.

Note 1: The weak pull-up resistor and associated current for the GP3/$\overline{\text{MCLR}}$ pin is non-linear when the respective pin voltage is less than VDD - 1.0V. See parameter D061 for GP3/$\overline{\text{MCLR}}$ pin current specifications.

Reset

When $\overline{\text{MCLR}}$ is asserted, the state of the OSC1/CLKIN and CLKOUT/OSC2 pins are as follows:

CLKIN/CLKOUT PIN STATES WHEN $\overline{\text{MCLR}}$ ASSERTED

Oscillator Mode	OSC1/CLKIN Pin	OSC2/CLKOUT Pin
EXTRC, CLKOUT on OSC2	OSC1 pin is tristated and driven by external circuit	OSC2 pin is driven low
EXTRC, OSC2 is I/O	OSC1 pin is tristated and driven by external circuit	OSC2 pin is tristate input
INTRC, CLKOUT on OSC2	OSC1 pin is tristate input	OSC2 pin is driven low
INTRC, OSC2 is I/O	OSC1 pin is tristate input	OSC2 pin is tristate input

NOTES:

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