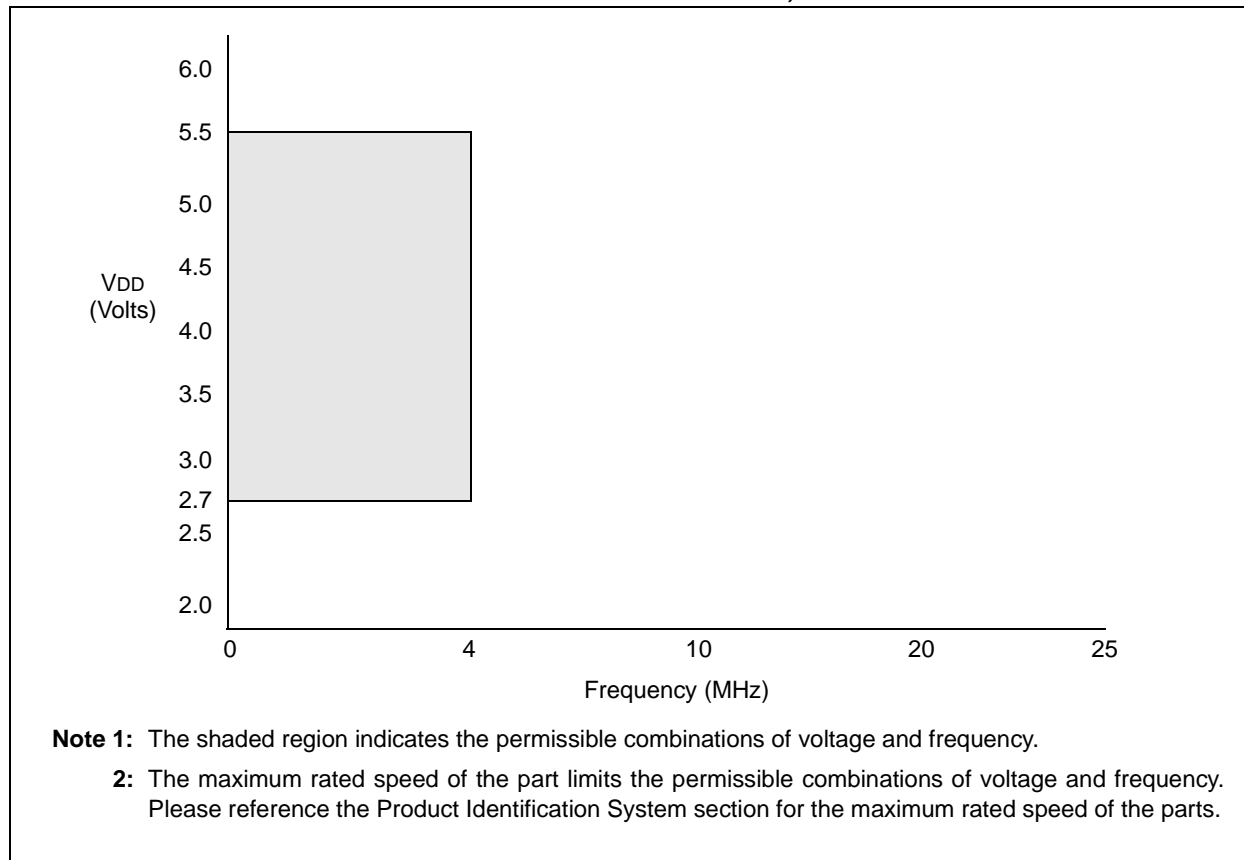


## PIC12CE67X Rev. B Silicon Errata Sheet

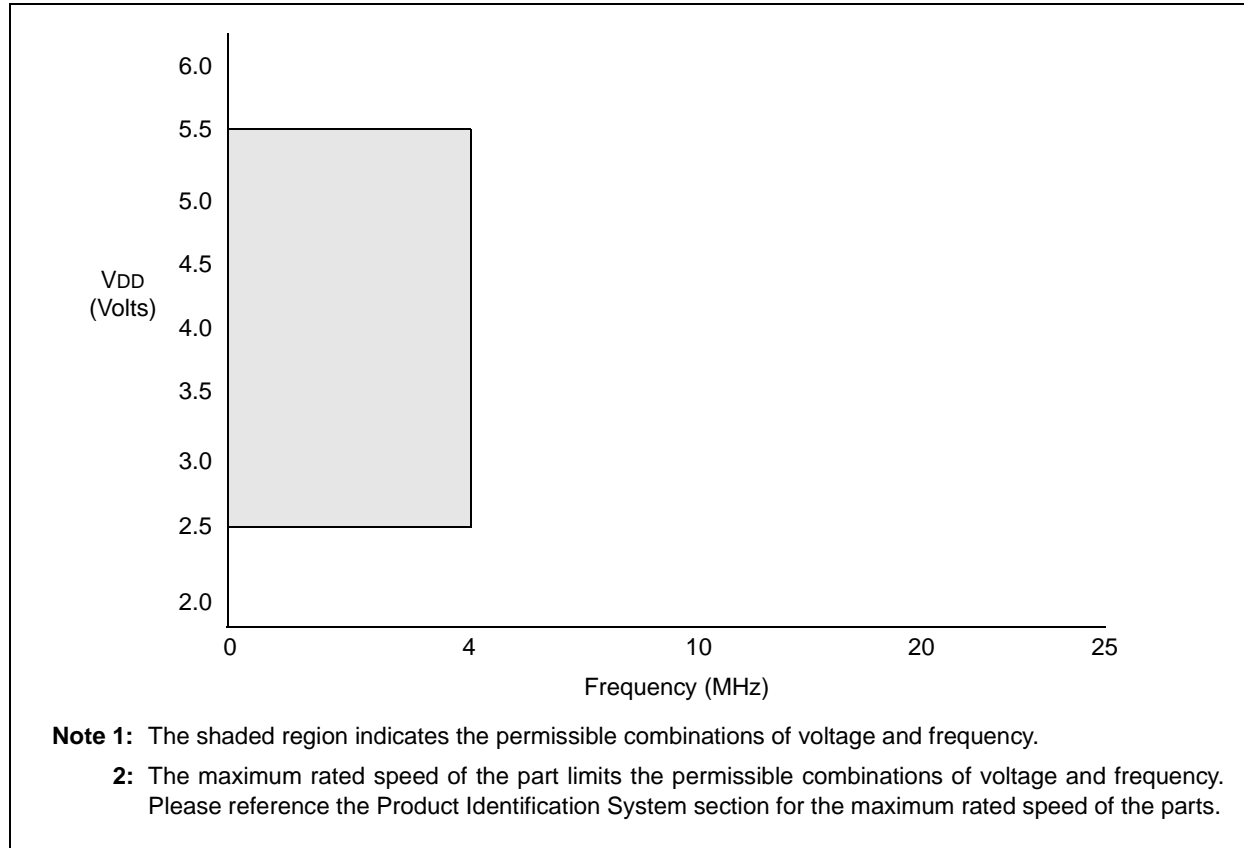
The PIC12CE67X (Rev. B) parts you have received conform functionally to the Device Data Sheet (**DS30561** and **DS40181A**), except for the anomalies described below.

**FIGURE 1: PIC12LCE67X VOLTAGE-FREQUENCY GRAPH,  $-40^{\circ}\text{C} \leq T_A \leq 0^{\circ}\text{C}$**

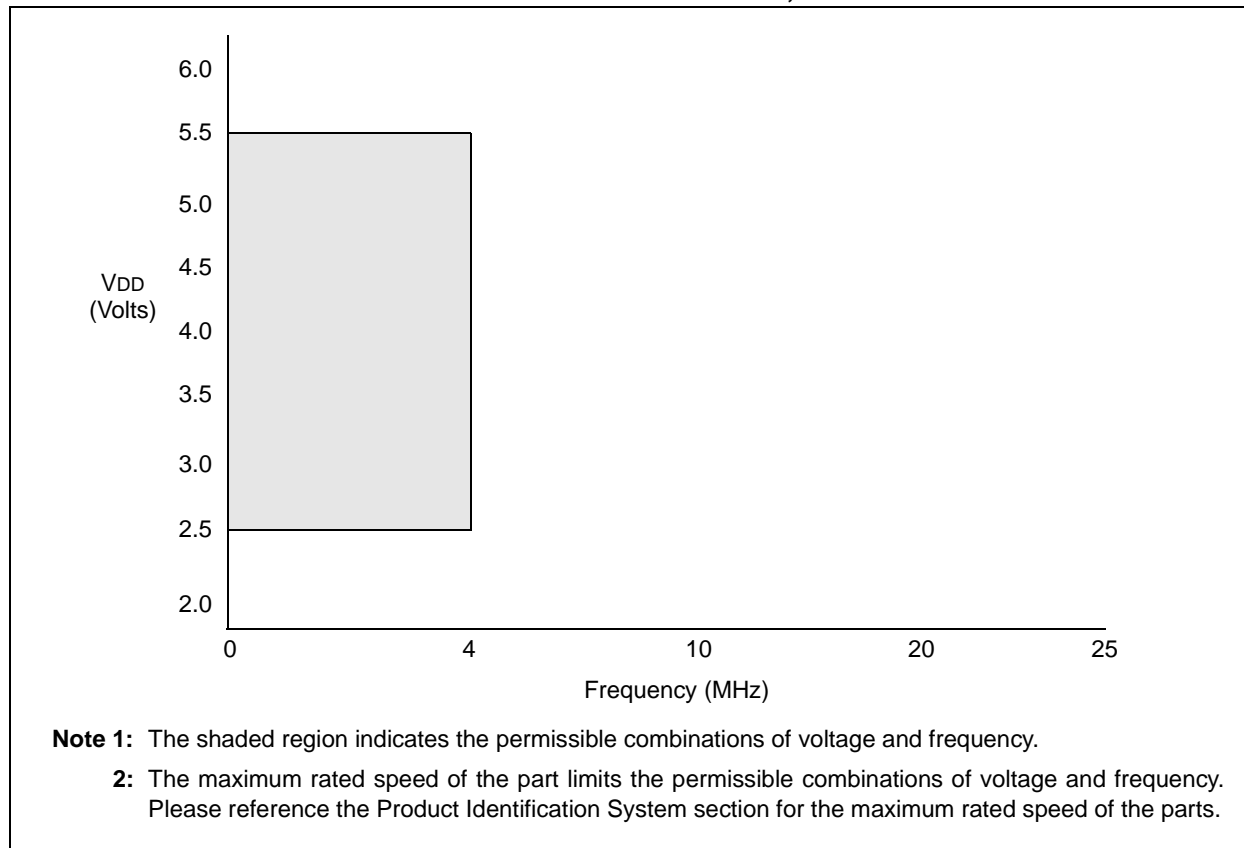


# PIC12CE67X

**FIGURE 2: PIC12LCE67X VOLTAGE-FREQUENCY GRAPH,  $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$**



**FIGURE 3: PIC12LCE67X VOLTAGE-FREQUENCY GRAPH,  $+70^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$**



## Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (**DS30561B**), the following clarifications and corrections should be noted.

In Section 4.0, corrections for the Special Function Register Summary, Table 4-1, are shown. Correction for the “OSCCAL” Register, Section 4.2.2.7, is shown. Clarification to the “GPIO”, Section 5.1 is provided. Corrections for the Internal 4 MHz RC Oscillator, Section 9.2.5, are shown. Corrections for Section 9.0, Initialization Conditions for all registers, Table 9-7, are shown. Corrections for the DC Characteristics, Sections 12.3 and 12.4 are shown.

Corrections for the GPIO pull-up resistor ranges are shown in Table 12-6.

**TABLE 4-1: PIC12C67X SPECIAL FUNCTION REGISTER SUMMARY**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other Resets <sup>(3)</sup>
<b>Bank 1</b>											
8Fh	OSCCAL	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	—	1000 00--	uuuu uu--

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'.  
Shaded locations are unimplemented, read as '0'.

- Note 1:** These registers can be addressed from either bank.  
**2:** The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.  
**3:** Other (non power-up) resets include external reset through MCLR and Watchdog Timer Reset.  
**4:** The IRP and RP1 bits are reserved on the CE67X; always maintain these bits clear.  
**5:** The SCL (GP7) and SDA (GP6) bits are unimplemented on the PIC12C671/672 and read as '0'.

### 4.2.2.7 OSCCAL REGISTER

The Oscillator Calibration (OSCCAL) Register is used to calibrate the internal 4 MHz oscillator. It contains six bits for calibration. Increasing the calue value increases the frequency.

**REGISTER 4-7: OSCCAL REGISTER (ADDRESS 8Fh)**

R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	—
bit7						bit0	
<p>bit 7-2: <b>CAL&lt;5:0&gt;</b>: Calibration</p> <p>bit 1-0: <b>Unimplemented</b>: Read as '0'</p>							

R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as '0'  
- n = Value at POR reset

# PIC12CE67X

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## 5.1 GPIO

GPIO is an 8-bit I/O register. Only the low order 6 bits are used (GP<5:0>). Bits 6 and 7 (SDA and SCL, respectively) are used by the EEPROM peripheral on the PIC12CE673/674. Refer to Section 6.0 and Appendix B for use of SDA and SCL. Please note that GP3 is an input only pin. The configuration word can set several I/O's to alternate functions. When acting as alternate functions, the pins will read as '0' during port read.

Pins GP0, GP1 and GP3 can be configured with weak pull-ups and also with interrupt-on-change. The interrupt on change and weak pull-up functions are not pin selectable. If pin 4, (GP3), is configured as MCLR, a weak pull-up is always on. Interrupt-on-change for this pin is not set and GP3 will read as '0'. Interrupt-on-change is enabled by setting bit GPIE, INTCON<3>.

The interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

- a) Any read or write of GPIO will end the mismatch condition.
- b) Clear flag bit GPIF.

A mismatch condition will continue to set flag bit GPIF. Reading GPIO will end the mismatch condition and allow flag bit GPIF to be cleared.

Note that external oscillator use overrides the GPIO functions on GP4 and GP5.

## 9.2.5 INTERNAL 4 MHz RC OSCILLATOR

OSCCAL, when written to with the calibration value, will “trim” the internal oscillator to remove process variation from the oscillator frequency. Only bits<7:2> of OSCCAL are implemented, and bits<1:0> should be written as 0 for compatibility with future devices. The oscillator calibration location is not code protected.

**TABLE 9-7: INITIALIZATION CONDITIONS FOR ALL REGISTERS**

Register	Power-on Reset	MCLR Resets WDT Reset	Wake-up via WDT or Interrupt
OSCCAL	1000 00--	uuuu uu--	uuuu uu--

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition.

**Note 1:** One or more bits in INTCON and PIR1 will be affected (to cause wake-up).

**2:** When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

**3:** See Table 9-5 for reset value for specific condition.

**4:** If wake-up was due to A/D completing then bit 6 = 1, all other interrupts generating a wake-up will cause bit 6 = u.

**5:** If wake-up was due to A/D completing then bit 3 = 0, all other interrupts generating a wake-up will cause bit 3 = u.

Revision Ax Engineering Samples of the PIC12CE673/4 are not included as part of this operational clarification for the OSCCAL register.

# PIC12CE67X

## 12.3 DC CHARACTERISTICS: PIC12C671/672 (Commercial, Industrial, Extended) PIC12CE673/674 (Commercial, Industrial, Extended)

Standard Operating Conditions (unless otherwise specified)							
Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended)							
Operating voltage $V_{DD}$ range as described in DC spec Section 12.1 and Section 12.2.							
Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
	<b>Input Leakage Current</b> (Notes 2, 3)						
D061	$\overline{\text{GP3/MCLR}}$ (Note 5)	IIL	8	130	250	$\mu\text{A}$	$V_{SS} \leq V_{PIN} \leq V_{DD}$
D061A	$\overline{\text{GP3/MCLR}}$ (Note 6)				$\pm 5$	$\mu\text{A}$	$V_{SS} \leq V_{PIN} \leq V_{DD}$
D070	GPIO weak pull-up current (Note 4)	IPUR	50	250	400	$\mu\text{A}$	$V_{DD} = 5\text{V}, V_{PIN} = V_{SS}$

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the CE67X be driven with external clock in RC mode.
- 2:** The leakage current on the  $\overline{\text{MCLR}}$  pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3:** Negative current is defined as coming out of the pin.
- 4:** Does not include GP3. For GP3 see parameters D061 and D061A.
- 5:** This spec. applies to  $\overline{\text{GP3/MCLR}}$  configured as external  $\overline{\text{MCLR}}$  and  $\overline{\text{GP3/MCLR}}$  configured as input with internal pull-up enabled.
- 6:** This spec. applies when  $\overline{\text{GP3/MCLR}}$  is configured as an input with pull-up disabled. The leakage current of the  $\overline{\text{MCLR}}$  circuit is higher than the standard I/O logic.

**12.4 DC CHARACTERISTICS: PIC12LC671/672 (Commercial, Industrial)  
PIC12LCE673/674 (Commercial, Industrial)**

Standard Operating Conditions (unless otherwise specified)							
Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial)							
Operating voltage $V_{DD}$ range as described in DC spec Section 12.1 and Section 12.2.							
Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
	<b>Input Leakage Current</b> (Notes 2, 3)						
D061	GP3/MCLR (Note 5)	IIL	8	130	250	$\mu\text{A}$	$V_{SS} \leq V_{PIN} \leq V_{DD}$
D061A	GP3MCLR (Note 6)						
D070	GPIO weak pull-up current (Note 4)	IPUR	50	250	400	$\mu\text{A}$	$V_{DD} = 5\text{V}, V_{PIN} = V_{SS}$

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the CE67X be driven with external clock in RC mode.
- 2:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3:** Negative current is defined as coming out of the pin.
- 4:** Does not include GP3. For GP3 see parameters D061 and D061A.
- 5:** This spec. applies to GP3/MCLR configured as external MCLR and GP3/MCLR configured as input with internal pull-up enabled.
- 6:** This spec. applies when GP3/MCLR is configured as an input with pull-up disabled. The leakage current of the MCLR circuit is higher than the standard I/O logic.

**TABLE 12-6: GPIO PULL-UP RESISTOR RANGES**

VDD (Volts)	Temperature (°C)	Min	Typ	Max	Units
GP0/GP1					
2.5	-40	38K	42K	63K	$\Omega$
	25	42K	48K	63K	$\Omega$
	85	42K	49K	63K	$\Omega$
	125	50K	55K	63K	$\Omega$
5.5	-40	15K	17K	20K	$\Omega$
	25	18K	20K	23K	$\Omega$
	85	19K	22K	25K	$\Omega$
	125	22K	24K	28K	$\Omega$
GP3 <sup>(1)</sup>					
2.5	-40	65K	80K	850K	$\Omega$
	25	80K	100K	1150K	$\Omega$
	85	85K	110K	1300K	$\Omega$
	125	100K	120K	1500K	$\Omega$
5.5	-40	50K	60K	600K	$\Omega$
	25	60K	65K	750K	$\Omega$
	85	65K	80K	900K	$\Omega$
	125	75K	90K	990K	$\Omega$

\* These parameters are characterized but not tested.

**Note 1:** The weak pull-up resistor and associated current for the GP3/MCLR pin is non-linear when the respective pin voltage is less than  $V_{DD} - 1.0\text{V}$ . See parameter D061 for GP3/MCLR pin current specifications.



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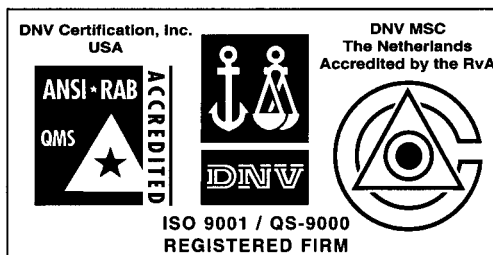
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