

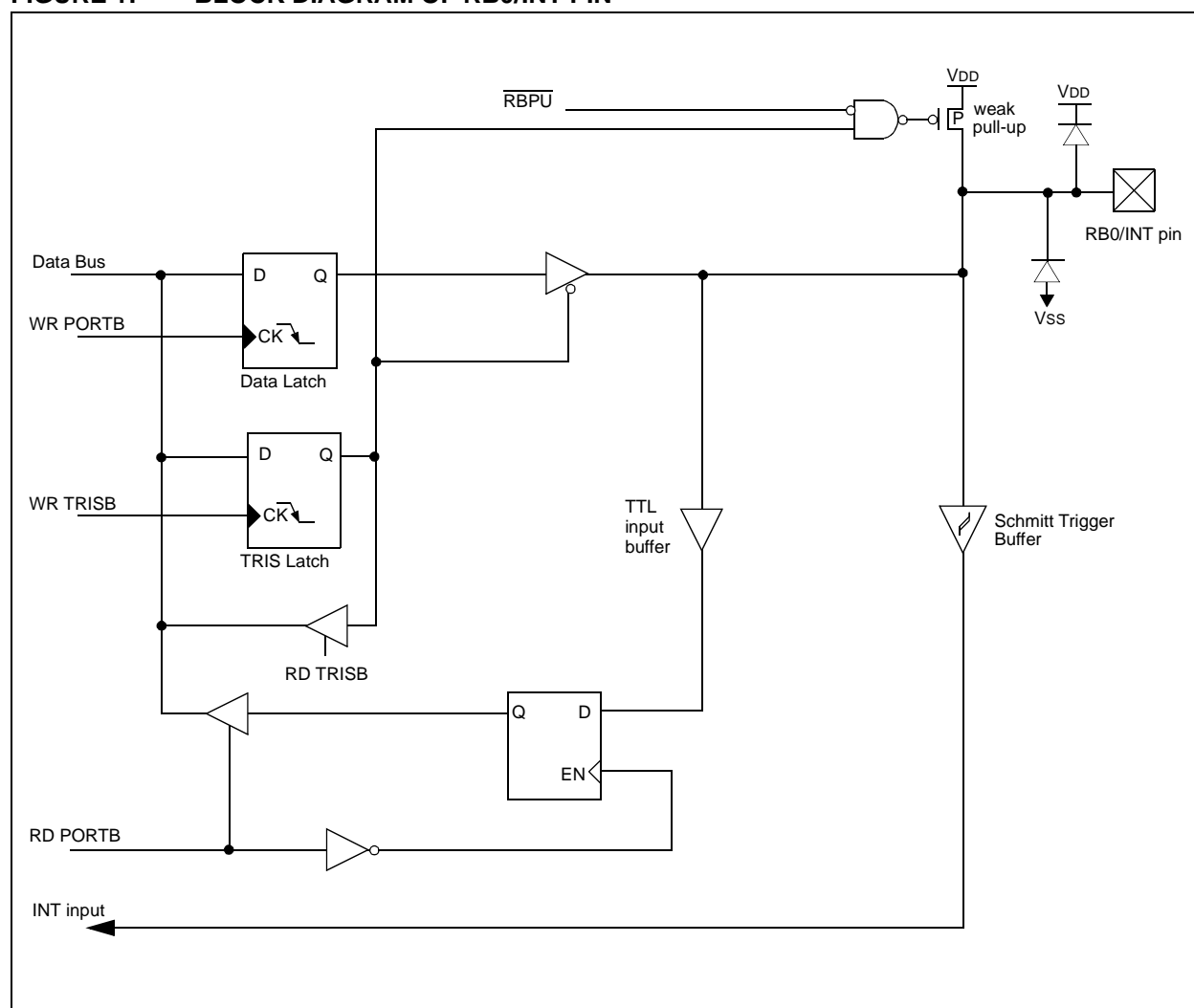
PIC16F627 Rev. A Silicon Errata Sheet

The PIC16F627 (Rev. A) parts you have received conform functionally to the Device Data Sheet (DS40300B), except for the anomalies described below.

1. Module: I/O Ports

A read of the PORTB Data Direction Register (TRISB) returns the Data Direction state on the port pins themselves and not the contents of the TRISB register latch.

FIGURE 1: BLOCK DIAGRAM OF RB0/INT PIN



PIC16F627

FIGURE 2: BLOCK DIAGRAM OF RB1/TX/DT PIN

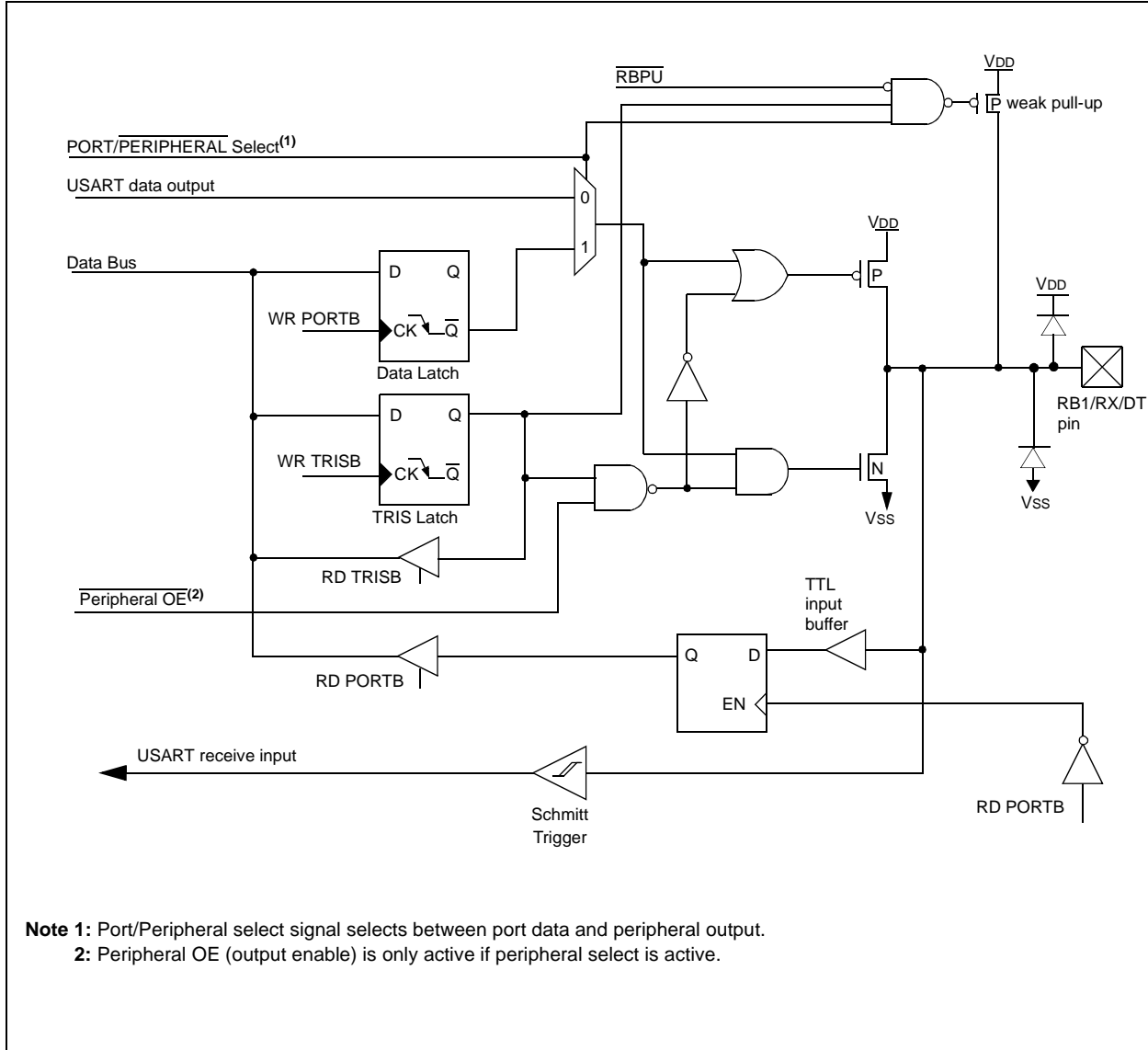
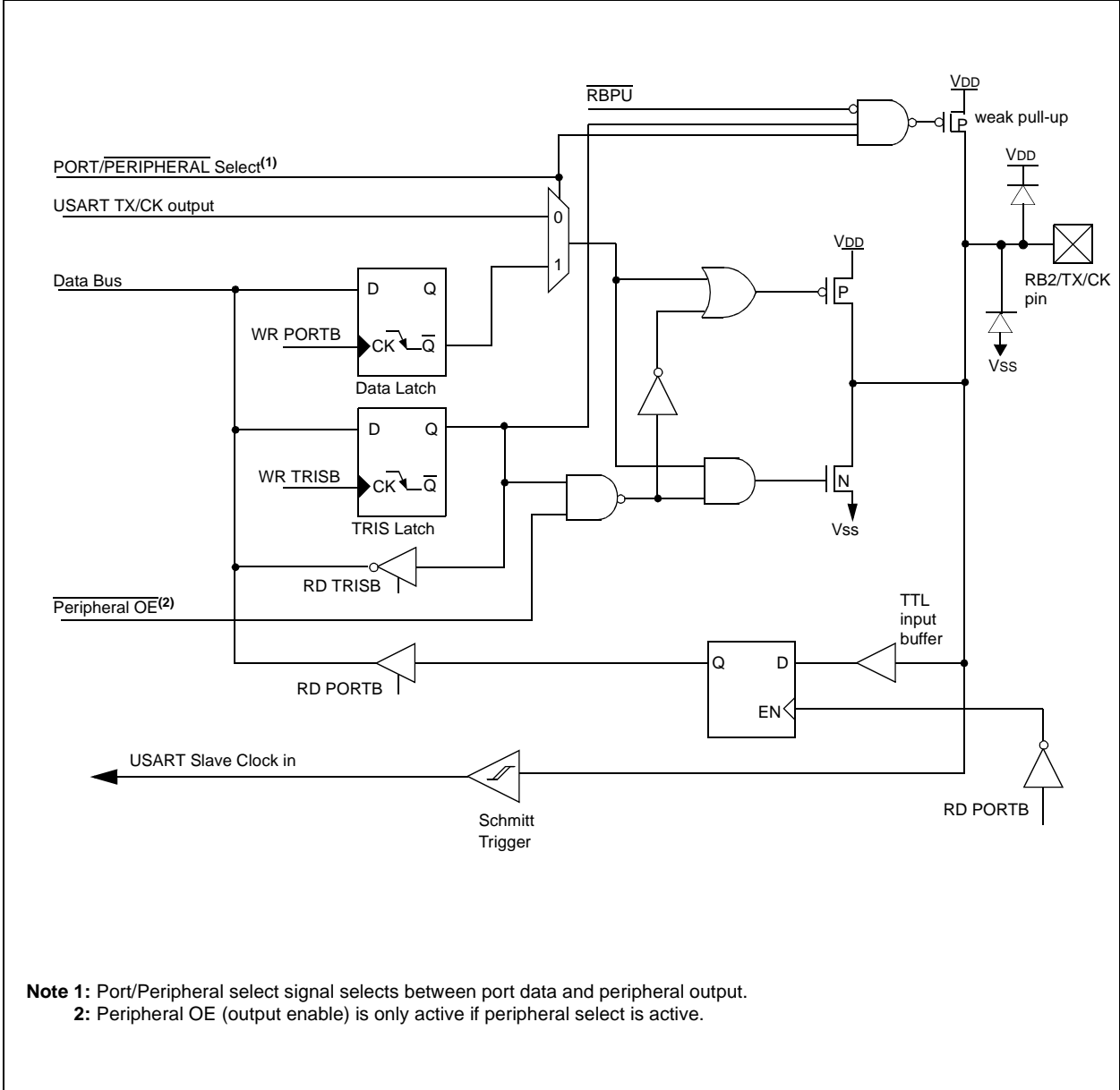
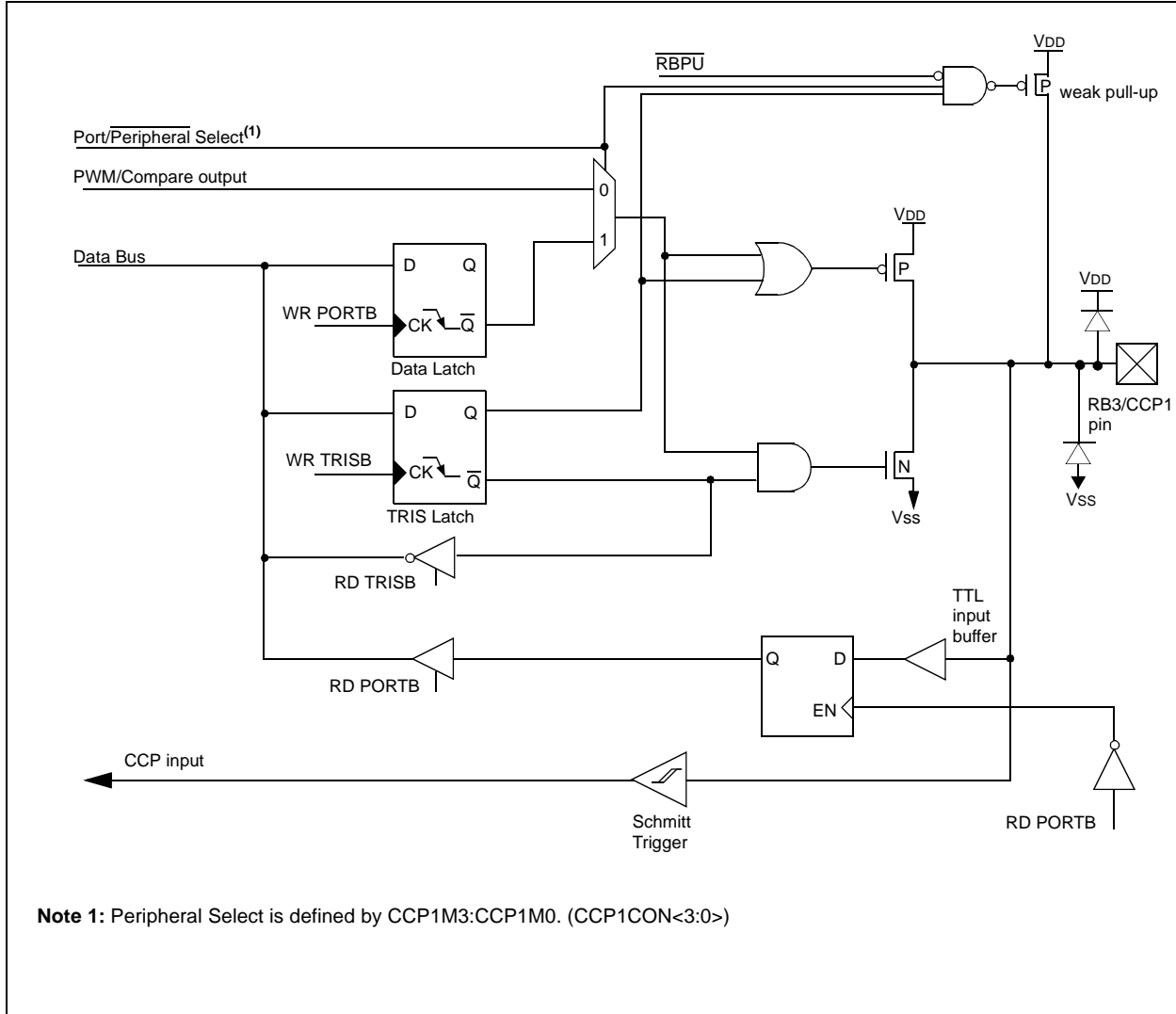


FIGURE 3: BLOCK DIAGRAM OF RB2/TX/CK PIN



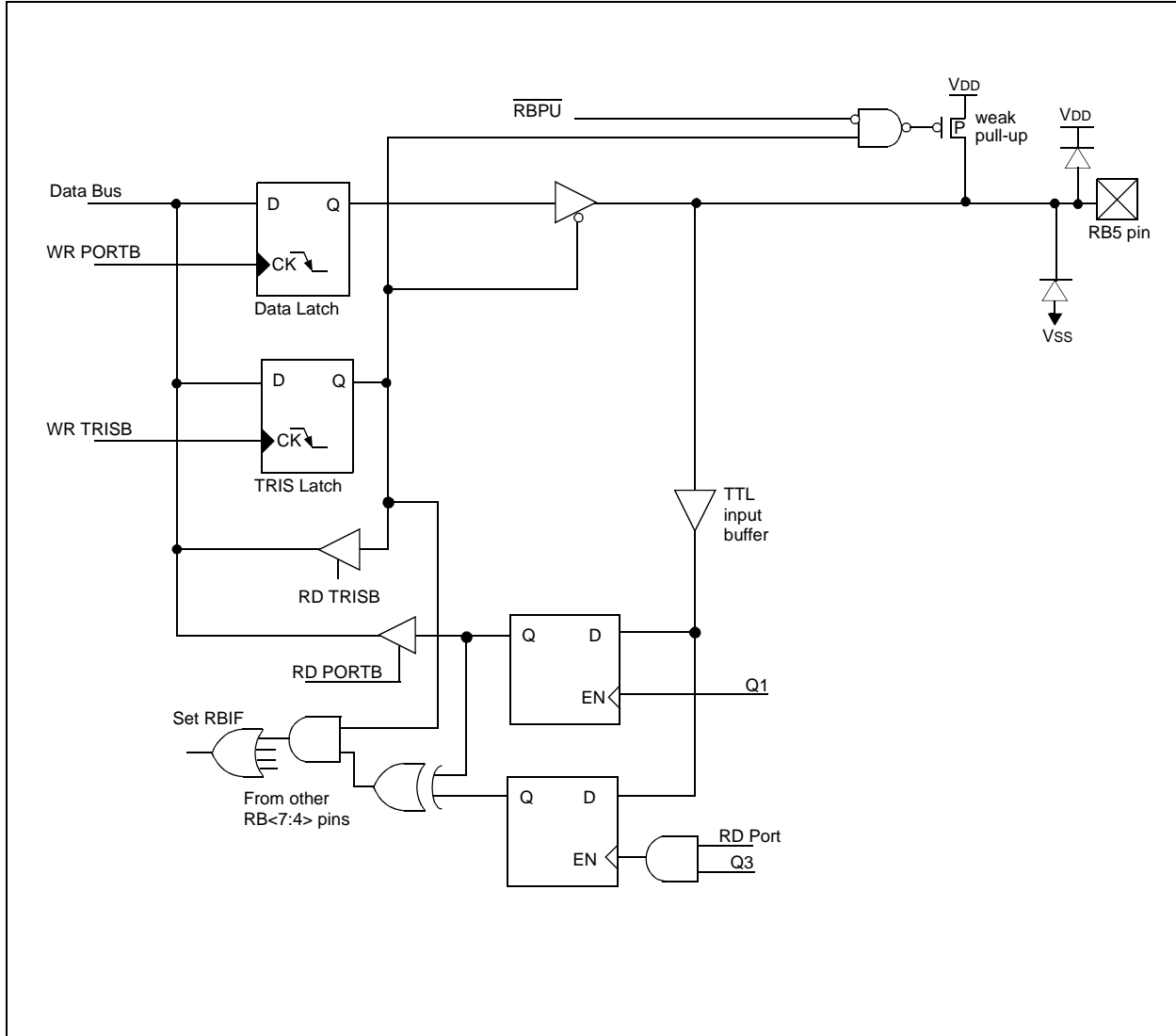
PIC16F627

FIGURE 4: BLOCK DIAGRAM OF THE RB3/CCP1 PIN



PIC16F627

FIGURE 6: BLOCK DIAGRAM OF RB5 PIN



PIC16F627

FIGURE 8: BLOCK DIAGRAM OF THE RB7/T1OSI PIN

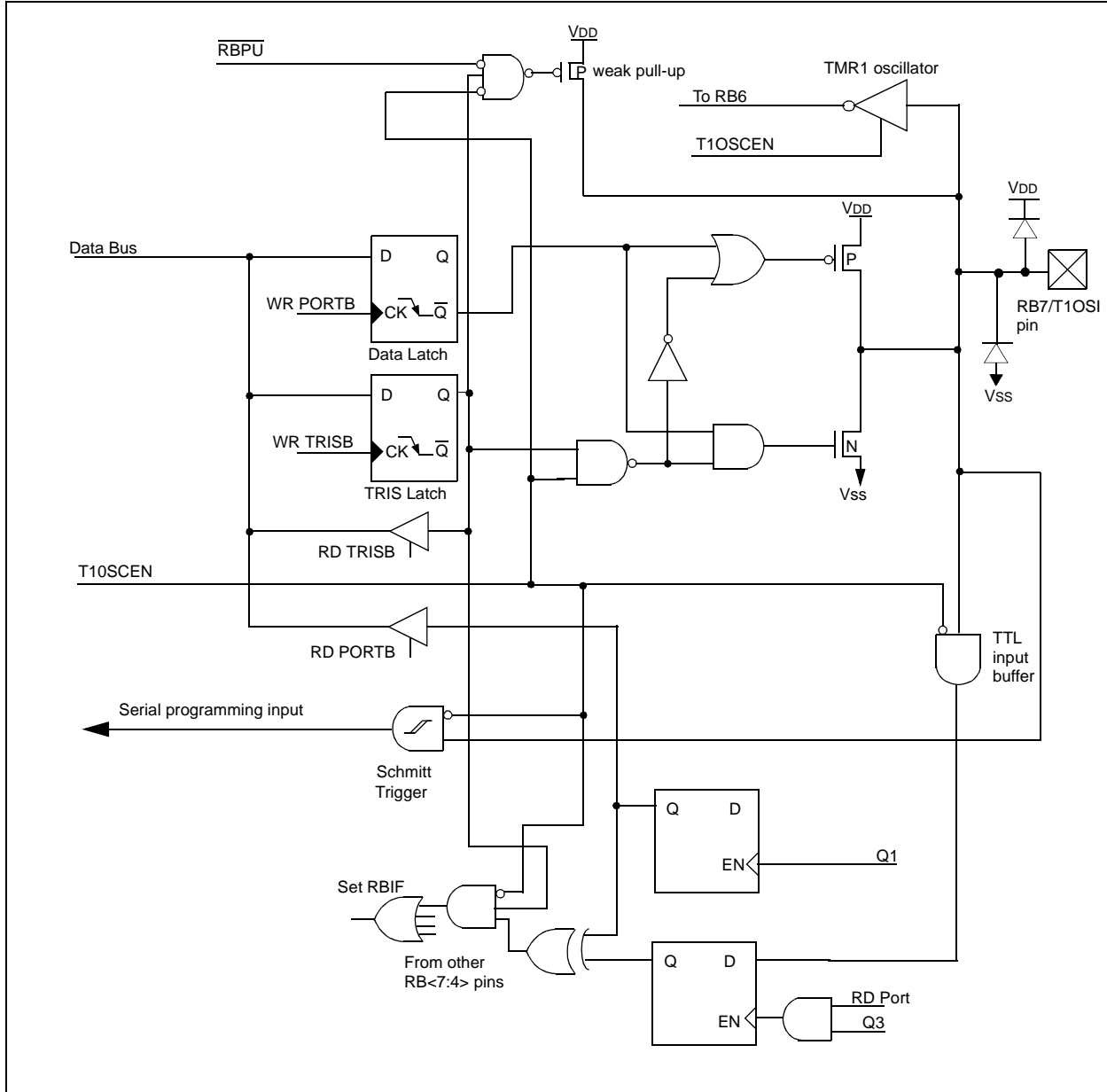
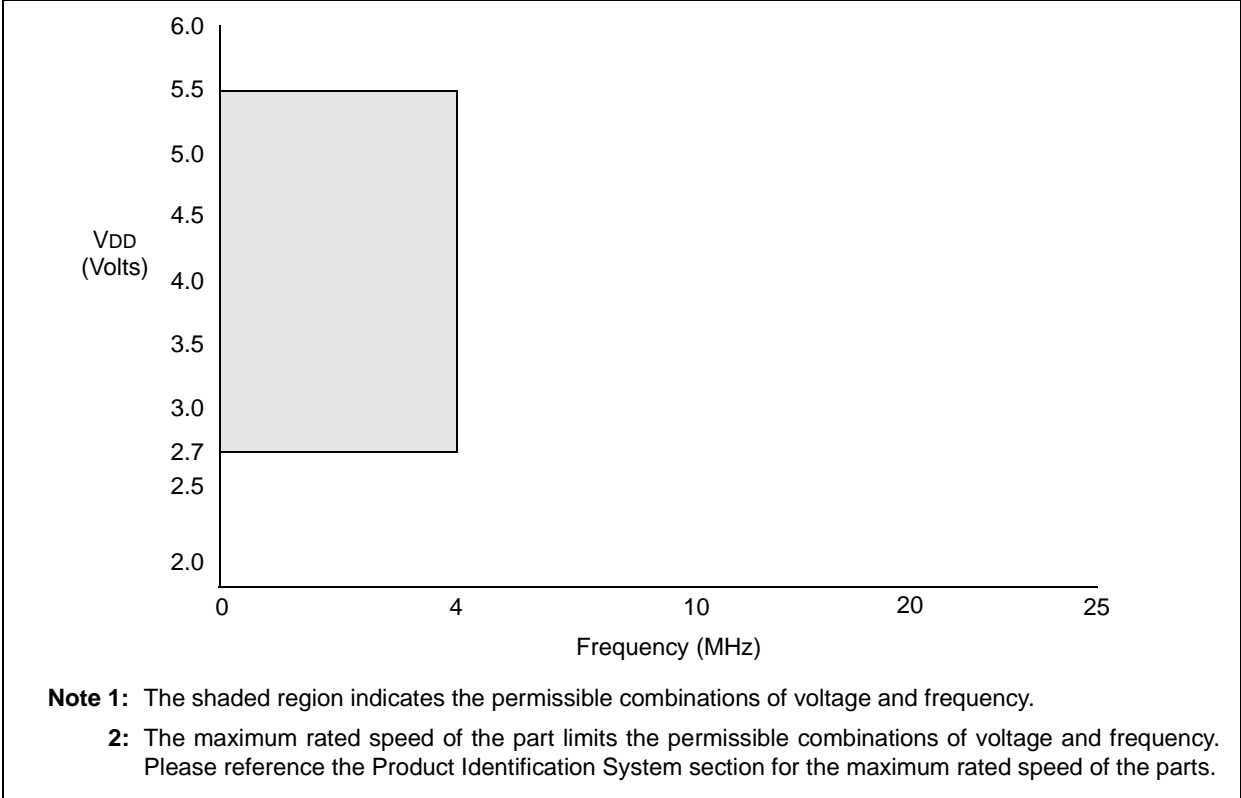


FIGURE 9: PIC16LF627 VOLTAGE-FREQUENCY GRAPH, $-40^{\circ}\text{C} \leq T_A \leq 0^{\circ}\text{C}$



PIC16F627

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS40300B), the following clarifications and corrections should be noted.

1. The bit T1SYNC in the Register T1CON (address 10h) should be asserted logic low (ie., $\overline{T1SYNC}$. Table 4-1, page 15, and Table 10-2, page 65, of DS40300B should be listed as follows:
2. The bit ADEN in Register RCSTA (address 18h), Table 4-1, is misspelled. The correct spelling should be ADDEN. This also appears in Figures and text on pages 72, 79, 80, 81, 82, 83, 84, 85, 86 and 89.

TABLE 4-1: SPECIAL REGISTERS SUMMARY BANK0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other Resets ⁽¹⁾
Bank 0											
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	--00 0000	--uu uuuu
18h	RCSTA	SPEN	RX9	SREN	CREN	ADEN	FERR	OERR	RX9D	0000 -00x	0000 -00x

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (non power-up) resets include \overline{MCLR} Reset, Brown-out Detect and Watchdog Timer Reset during normal operation.

TABLE 10-2 REGISTERS ASSOCIATED WITH CAPTURE, COMPARE, AND TIMER1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on all other resets
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	--00 0000	--uu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by Capture and Timer1.

3. Valid regions of operation:

FIGURE 17-1: PIC16F62X VOLTAGE-FREQUENCY GRAPH, $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$

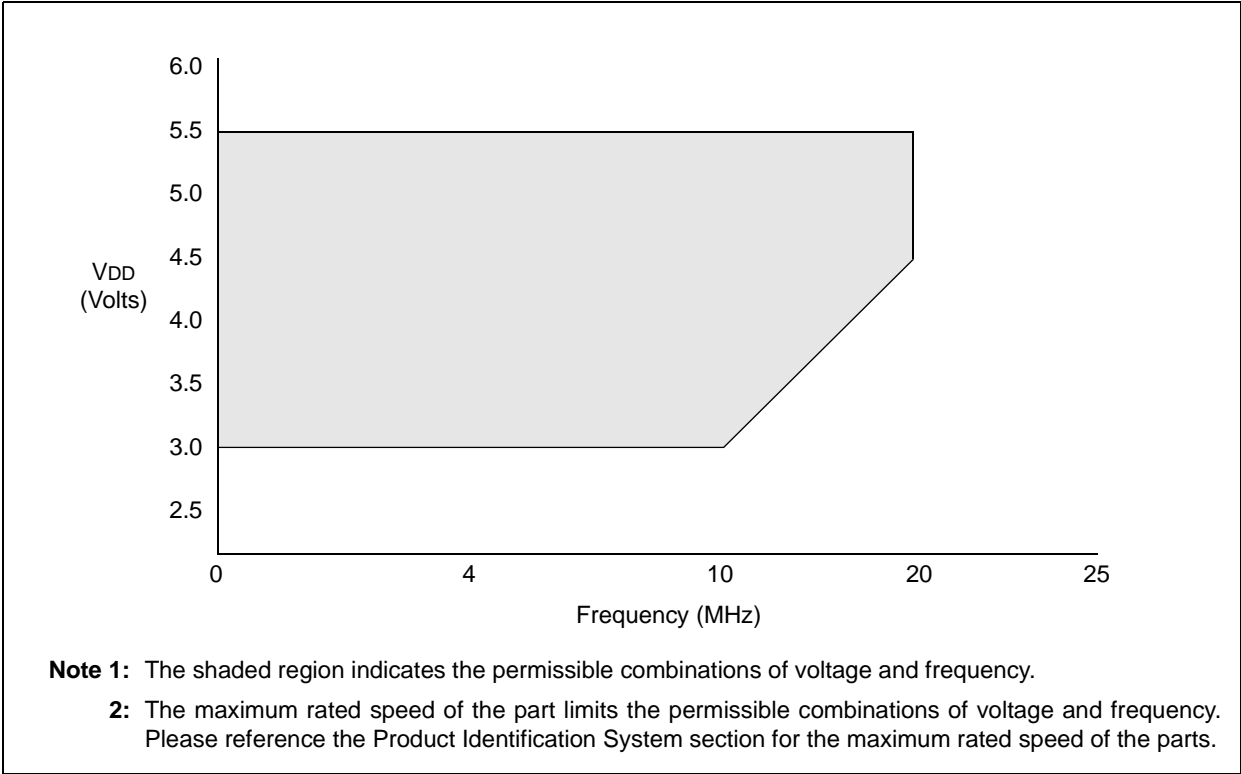
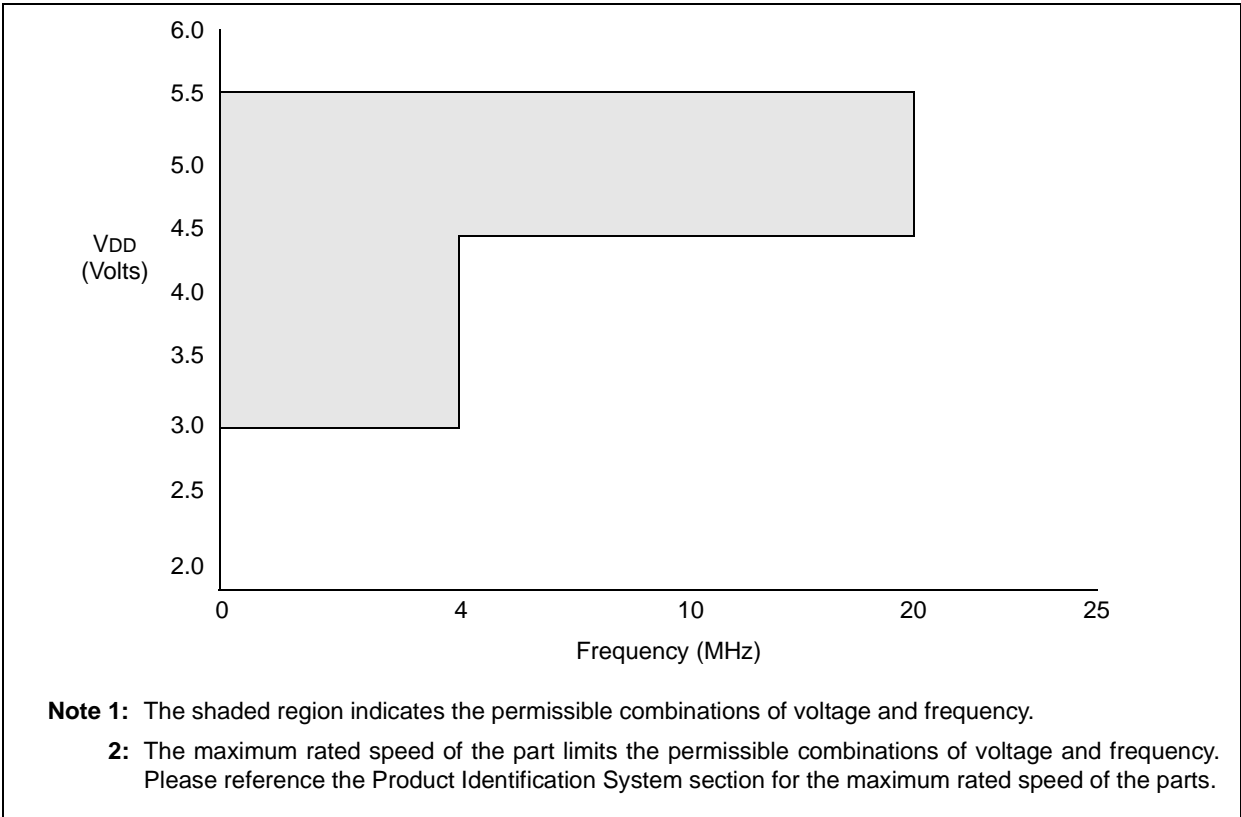


FIGURE 17-2: PIC16F62X VOLTAGE-FREQUENCY GRAPH, $-40^{\circ}\text{C} \leq T_A < 0^{\circ}\text{C}$, $+70^{\circ}\text{C} < T_A \leq +125^{\circ}\text{C}$



PIC16F627

FIGURE 17-3: PIC16LF62X VOLTAGE-FREQUENCY GRAPH, $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$

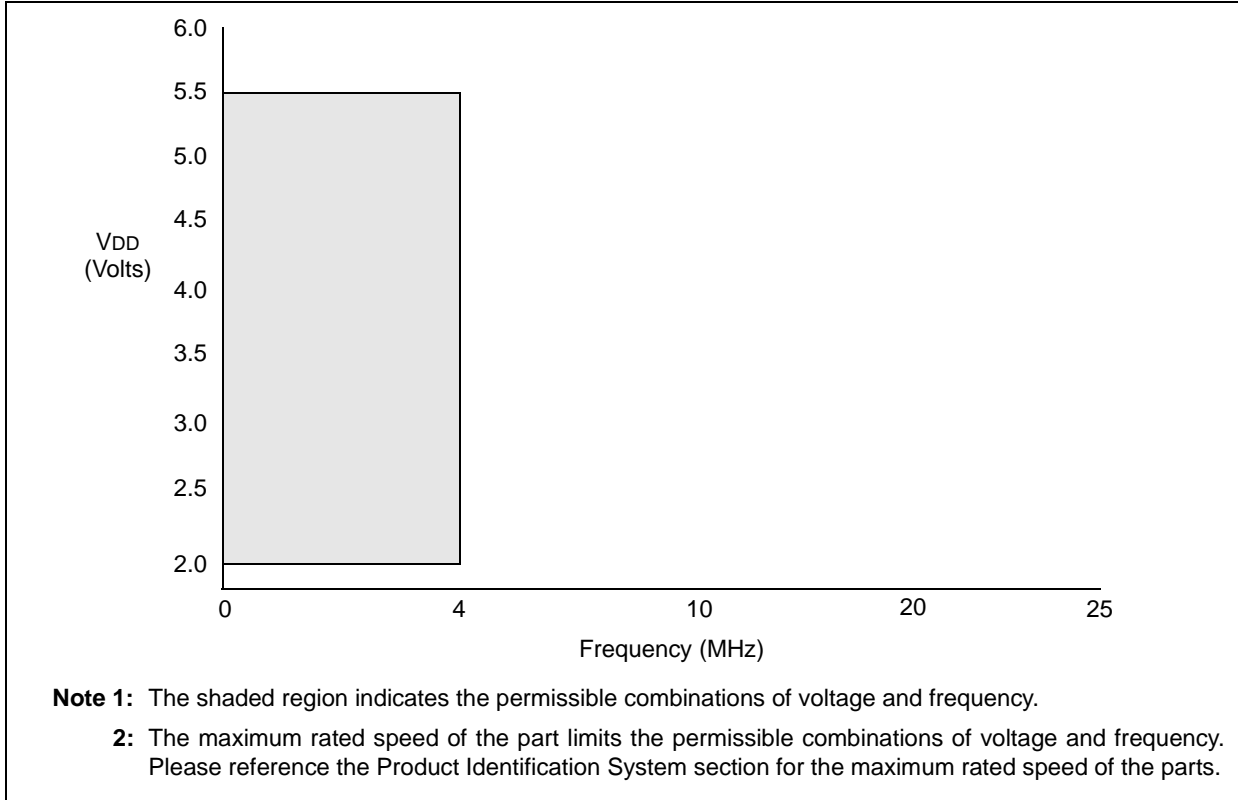
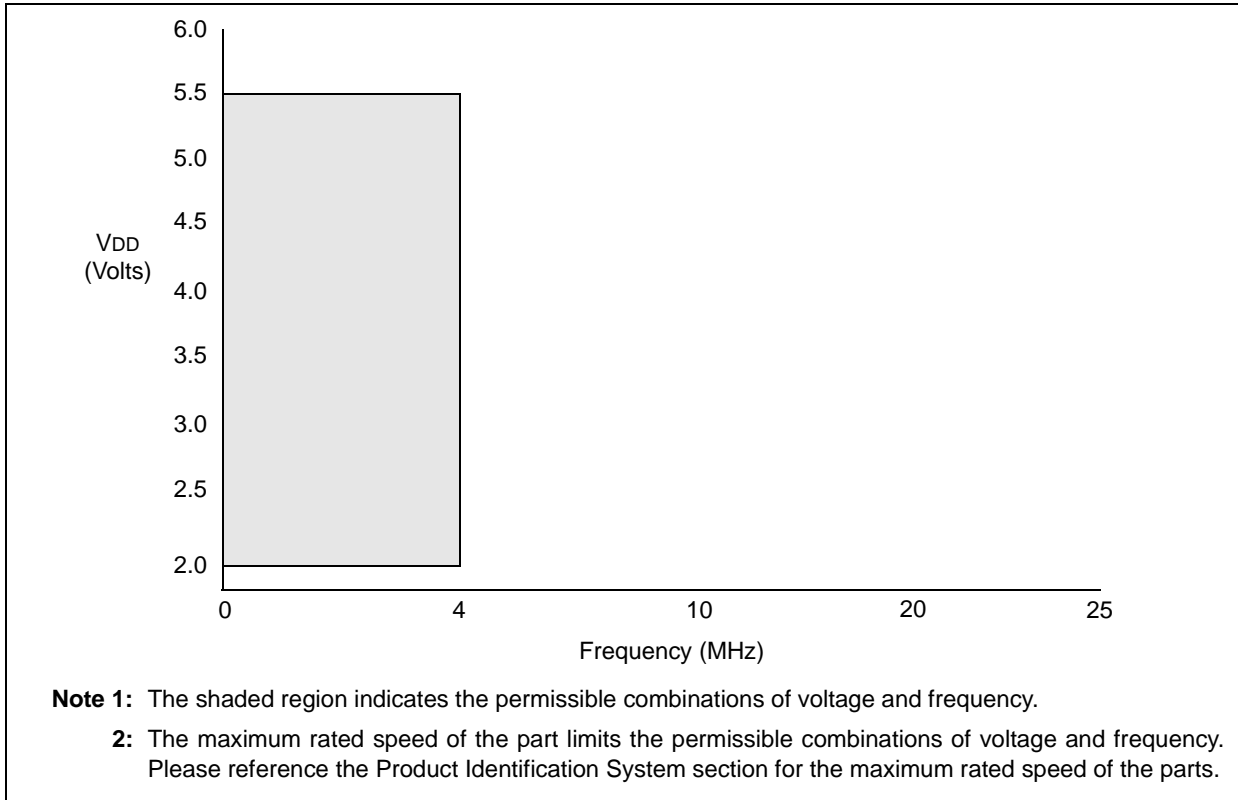


FIGURE 17-4: PIC16LF62X VOLTAGE-FREQUENCY GRAPH, $+70^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$



**TABLE 17-1: DC CHARACTERISTICS: PIC16F62X-04 (COMMERCIAL, INDUSTRIAL, EXTENDED)
PIC16F62X-20 (COMMERCIAL, INDUSTRIAL, EXTENDED)**

Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended							
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage	3.0	-	5.5	V	
D002	VDR	RAM Data Retention Voltage (Note 1)	-	1.5*	-	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure Power-on Reset	-	VSS	-	V	See section on power-on reset for details
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	-	-	V/ms	See section on power-on reset for details
D005	VBOD	Brown-out Detect Voltage	3.7	4.0	4.35	V	BODEN configuration bit is cleared
D010	IDD	Supply Current (Note 2, 5)	-	-	0.7	mA	FOSC = 4.0MHz, VDD = 3.0
-			4.0	7.0	mA	FOSC = 4.0MHz, VDD = 5.5*	
-			-	6.0	mA	FOSC = 20.0MHz, VDD = 5.5*	
-			-	2.0	mA	FOSC = 20.0MHz, VDD = 4.5 FOSC = 10.0MHz, VDD = 3.0 (Note 6) FOSC = 32kHz, VDD = 3.0	
D020	IPD	Power Down Current (Note 3)	-	-	2.2	μA	VDD = 3.0
-			-	5.0	μA	VDD = 4.5	
-			-	9.0	μA	VDD = 5.5*	
-			-	15.0	μA	VDD = 5.5 Extended*	
D022	ΔI _{WDT}	WDT Current (Note 4)	-	6.0	20	μA	VDD = 4.0V (125°C)
D022A	ΔI _{BOD}	Brown-out Detect Current (Note 4)	-	75	125	μA	BOD enabled, VDD = 5.0V
D023	ΔI _{COMP}	Comparator Current for each Comparator (Note 4)	-	30	50	μA	VDD = 4.0V
D023A	ΔI _{VREF}	VREF Current (Note 4)	-	-	135	μA	VDD = 4.0V
1A	FOSC	LP Oscillator Operating Frequency	0	-	200	kHz	All temperatures
		INTRC Oscillator Operating Frequency	-	-	4	MHz	All temperatures
		XT Oscillator Operating Frequency	0	-	4	MHz	All temperatures
		HS Oscillator Operating Frequency	0	-	20	MHz	All temperatures

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

5: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula, $I_r = VDD/2R_{ext}$ (mA) with Rext in kΩ.

6: Commercial temperature range only.

PIC16F627

TABLE 17-2: DC CHARACTERISTICS: PIC16LF62X-04 (COMMERCIAL, INDUSTRIAL, EXTENDED)

Standard Operating Conditions (unless otherwise stated)							
Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended							
Operating voltage V_{DD} range as described in DC spec Table 17-1 and Table 12-2							
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage	2.0	-	5.5	V	
D002	VDR	RAM Data Retention Voltage (Note 1)	-	1.5*	-	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure Power-on Reset	-	VSS	-	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	-	-	V/ms	See section on Power-on Reset for details
D005	VBOD	Brown-out Detect Voltage	3.7	4.0	4.35	V	BODEN configuration bit is cleared
D010	IDD	Supply Current (Note 2, 5)	-	-	0.6	mA	FOSC = 4.0MHz, VDD = 2.0, WDT disabled (Note 5)
D013							FOSC = 4.0MHz, VDD = 5.5, WDT disabled (Note 5)* FOSC = 32kHz, VDD = 2.0, WDT disabled
D020	IPD	Power Down Current (Note 2, 3)	-	-	2.0	μA	VDD = 2.0
					2.2	μA	VDD = 2.5*
					9.0	μA	VDD = 3.0*
					15.0	μA	VDD = 5.5 VDD = 5.5 Extended
D023	ΔI_{WDT}	WDT Current (Note 4)	-	6.0	15	μA	VDD = 3.0V
	ΔI_{BOD}	Brown-out Detect Current (Note 4)	-	75	125	μA	BOD enabled, VDD = 5.0V
	ΔI_{COMP}	Comparator Current for each Comparator (Note 4)	-	30	50	μA	VDD = 3.0V
	ΔI_{VREF}	VREF Current (Note 4)	-	-	135	μA	VDD = 3.0V
1A	FOSC	LP Oscillator Operating Frequency	0	-	200	kHz	All temperatures
		INTRC Oscillator Operating Frequency	-	-	4	MHz	All temperatures
		XT Oscillator Operating Frequency	0	-	4	MHz	All temperatures
		HS Oscillator Operating Frequency	0	-	20	MHz	All temperatures

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD to VSS.

4: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

5: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{ext}$ (mA) with Rext in k Ω .

**TABLE 17-3: DC CHARACTERISTICS: PIC16F62X (COMMERCIAL, INDUSTRIAL, EXTENDED)
PIC16LF62X (COMMERCIAL, INDUSTRIAL, EXTENDED)**

Standard Operating Conditions (unless otherwise stated)							
Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended							
Operating voltage V_{DD} range as described in DC spec Table 17-1 and Table 12-2							
Param. No.	Sym	Characteristic	Min	Typ†	Max	Unit	Conditions
D030	V _{IL}	Input Low Voltage I/O ports with TTL buffer	V _{SS}	–	0.8V 0.15V _{DD}	V	V _{DD} = 4.5V to 5.5V otherwise
D031		with Schmitt Trigger input	V _{SS}	–	0.2V _{DD}	V	Note1
D032		MCLR, RA4/T0CKI, OSC1 (in ER mode)	V _{SS}	–	0.2V _{DD}	V	
D033		OSC1 (in XT and HS)	V _{SS}	–	0.3V _{DD}	V	
		OSC1 (in LP)	V _{SS}	–	0.6V _{DD} -1.0	V	
D040	V _{IH}	Input High Voltage I/O ports with TTL buffer	2.0V .25V _{DD} + 0.8V	–	V _{DD} V _{DD}	V	V _{DD} = 4.5V to 5.5V otherwise
D041		with Schmitt Trigger input	0.8V _{DD}	–	V _{DD}	V	
D042		MCLR RA4/T0CKI	0.8V _{DD}	–	V _{DD}	V	
D043		OSC1 (XT, HS and LP)	0.7V _{DD}	–	V _{DD}	V	
D043A		OSC1 (in ER mode)	0.9V _{DD}	–			Note1
D070	IPURB	PORTB weak pull-up current	50	200	400	μA	V _{DD} = 5.0V, V _{PIN} = V _{SS}
		Input Leakage Current (Notes 2, 3)					
D060	I _{IL}	I/O ports (Except PORTA)	–	–	±1.0	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , pin at hi-impedance
D061		PORTA	–	–	±0.5	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , pin at hi-impedance
D063		RA4/T0CKI	–	–	±1.0	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD}
		OSC1, MCLR	–	–	±5.0	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , XT, HS and LP osc configuration
D080	V _{OL}	Output Low Voltage I/O ports	–	–	0.6	V	I _{OL} =8.5 mA, V _{DD} =4.5V, -40° to +85°C
D083		OSC2/CLKOUT (ER only)	–	–	0.6	V	I _{OL} =7.0 mA, V _{DD} =4.5V, +125°C
			–	–	0.6	V	I _{OL} =1.6 mA, V _{DD} =4.5V, -40° to +85°C
			–	–	0.6	V	I _{OL} =1.2 mA, V _{DD} =4.5V, +125°C
D090	V _{OH}	Output High Voltage (Note 3) I/O ports (Except RA4)	V _{DD} -0.7	–	–	V	I _{OH} =-3.0 mA, V _{DD} =4.5V, -40° to +85°C
D092		OSC2/CLKOUT (ER only)	V _{DD} -0.7	–	–	V	I _{OH} =-2.5 mA, V _{DD} =4.5V, +125°C
			V _{DD} -0.7	–	–	V	I _{OH} =-1.3 mA, V _{DD} =4.5V, -40° to +85°C
			V _{DD} -0.7	–	–	V	I _{OH} =-1.0 mA, V _{DD} =4.5V, +125°C
D150	V _{OD}	Open-Drain High Voltage		–	8.5	V	RA4 pin PIC16F62X, PIC16LF62X
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2 pin		–	15	pF	In XT, HS and LP modes when external clock used to drive OSC1.
D101	C _{IO}	All I/O pins/OSC2 (in ER mode)		–	50	pF	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In ER oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16F62X be driven with external clock in ER mode.

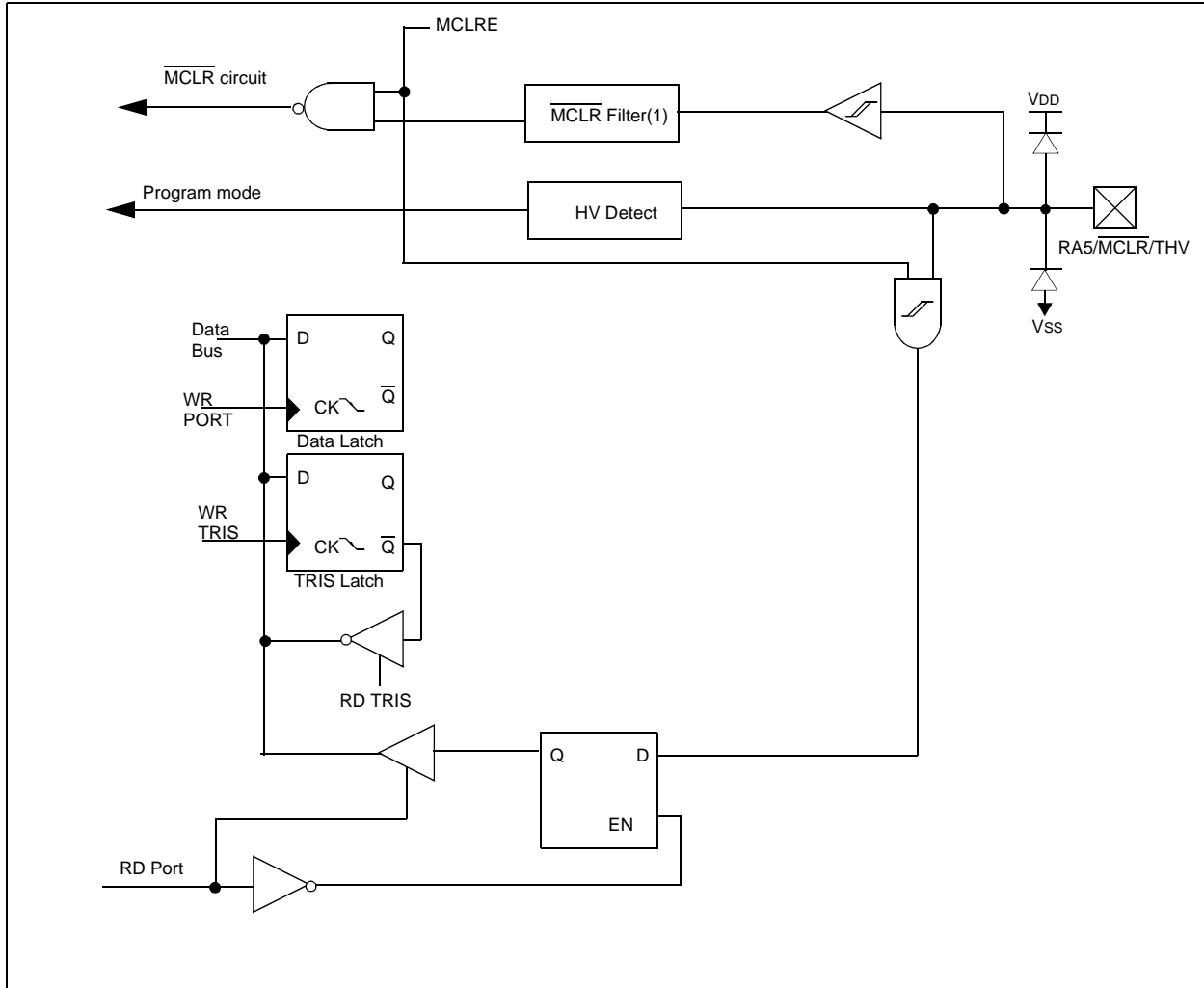
2: The leakage current on the MCLR pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

PIC16F627

4. The following block diagram shown in Section 5, Figure 5-5 is incorrect. The following figure should be used instead.

FIGURE 5-5: BLOCK DIAGRAM OF THE RA5/MCLR/THV PIN



5. The example given in Section 9, Example 9-1, concerning Initializing the Comparator Module is incorrect. The following code example should be used instead.

EXAMPLE 9-1: INITIALIZING COMPARATOR MODULE

```
BCF      INTCON,GIE      ; Turn OFF Global Interrupts
BCF      INTCON,PEIE     ; Turn OFF Peripheral Interrupts
CLRF     PORTA          ; Init Port A
MOVLW   0X03            ; Init comparator mode
MOVWF   CMCON           ; CM<2:0> = 011
BSF     STATUS,RP0      ; Select BANK 1
MOVLW   0x07            ; Initialize Port A Direction
MOVWF   TRISA           ; Set RA<2:0> as Inputs
                          ; RA<4:3> as outputs
                          ; TRIS<5> always reads '0'

BCF     STATUS,RP0      ; Select BANK 0
CALL    DELAY10         ; Wait 10us for comparator output to become valid
                          ; See Table 17-1 Parameter 301

MOVF    CMCON,F         ; Read CMCON to end change condition
BCF     PIR1,CMIF       ; Clear pending interrupts
BSF     STATUS,RP0      ; Select BANK 1
BSF     PIE1,CMIE       ; Enable Comparator Interrupts
BCF     STATUS,RP0      ; Select BANK 0
BSF     INTCON,PEIE     ; Enable Peripheral Interrupts
BSF     INTCON,GIE      ; Global Interrupt Enable

; Insert Your code....

; Helper function is the Delay for 10us routine show below.

DELAY10      ; burns 8 cycles + the call for 10 cycles or 10us at 4Mhz
goto $+1     ; goto the next instruction and burn 2 cycles
call retlbl  ; goto the next instruction and burn 2 more cycles
retlbl      return      ; go back and burn 2 cycles (actually done 2x for 4 cycles consumed)
```

PIC16F627

6. The examples given in Section 13, concerning the Data EEPROM are incorrect. The EEPROM registers are all located in Bank 1. The examples show the registers in Bank 0 and Bank 1. The following code examples should be used instead to use this feature.

EXAMPLE 13-1: DATA EEPROM READ

```
BSF     STATUS, RP0 ; Bank 1
MOVLW  CONFIG_ADDR ;
MOVWF  EEADR       ; Address to read
BSF     EECON1, RD ; EE Read
MOVF   EEDATA, W  ; W = EEDATA
BCF     STATUS, RP0 ; Bank 0
```

EXAMPLE 13-2: DATA EEPROM WRITE

```
                ; set up the data and
                ; the address
BSF     STATUS, RP0 ; Bank 1
MOVLW  CONFIG_ADDR ;
MOVWF  EEADR       ; Address to write
MOVLW  CONFIG_DATA ;
MOVWF  EEDATA      ; Data to write

                ; perform the write
                ; operation
BSF     EECON, WREN ; Enable Write
BCF     INTCON, GIE ; Disable INTs
MOVLW  055h        ;
MOVWF  EECON2      ; Write 55
MOVLW  0AAh        ;
MOVWF  EECON2      ; Write AA
BSF     EECON1, WR ; Set WR bit
BCF     STATUS, RP0 ; Bank 0
```

EXAMPLE 13-3: DATA EEPROM VERIFY

```
; after the write in complete (i.e. in the
write interrupt)
BSF     STATUS, RP0 ; Bank 1
MOVF   EEDATA, W   ; load the last
                    ; written value into W
BSF     EECON, RD  ; start a read
;
; Is the value written (in W Reg) and
; read (in EEDATA) the same?
;
SUBWF  EEDATA, W   ; the EEDATA has fresh
                    ; data
BTFSS  STATUS, Z   ; Is the Zero flag set?
GOTO   WRITE_ERR  ; NO, Write Error
                    ; YES, Good Write
                    ; continue program
```

NOTES:



WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: <http://www.microchip.com>

Rocky Mountain

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-692-7966 Fax: 480-792-7456

Atlanta

500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Boston

2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-782-3848 Fax: 978-692-3821

Chicago

333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas

4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Dayton

Two Prestige Place, Suite 130
Miamisburg, OH 45342
Tel: 937-291-1654 Fax: 937-291-9175

Detroit

Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Los Angeles

18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

New York

150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose

Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto

6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

China - Beijing

Microchip Technology Beijing Office
Unit 915
New China Hong Kong Manhattan Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Shanghai

Microchip Technology Shanghai Office
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

Hong Kong

Microchip Asia Pacific
RM 2101, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India

Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaughnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan

Microchip Technology Intl. Inc.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471-6166 Fax: 81-45-471-6122

Korea

Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea
Tel: 82-2-554-7200 Fax: 82-2-558-5934

ASIA/PACIFIC (continued)

Singapore

Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan

Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark

Microchip Technology Denmark ApS
Regus Business Centre
Lautrup høj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France

Arizona Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany

Arizona Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

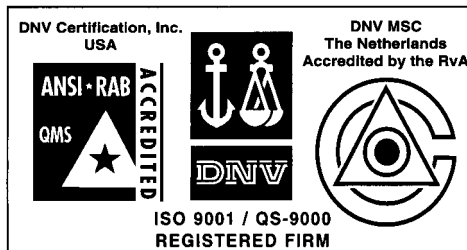
Italy

Arizona Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom

Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

10/01/00



Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELoc® code hopping devices, Serial EEPROMs and microperipheral products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.

All rights reserved. © 2000 Microchip Technology Incorporated. Printed in the USA. 11/00 Printed on recycled paper.

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, except as maybe explicitly expressed herein, under any intellectual property rights. The Microchip logo and name are registered trademarks of Microchip Technology Inc. in the U.S.A. and other countries. All rights reserved. All other trademarks mentioned herein are the property of their respective companies.