PIC16F628

PIC16F628 Rev. A Silicon Errata Sheet

The PIC16F628 (Rev. A) parts you have received conform functionally to the Device Data Sheet (DS40300**B**), except for the anomalies described below.

1. Module: I/O Ports

   A read of the PORTB Data Direction Register (TRISB) returns the Data Direction state on the port pins themselves and not the contents of the TRISB register latch.

FIGURE 1: BLOCK DIAGRAM OF RB0/INT PIN

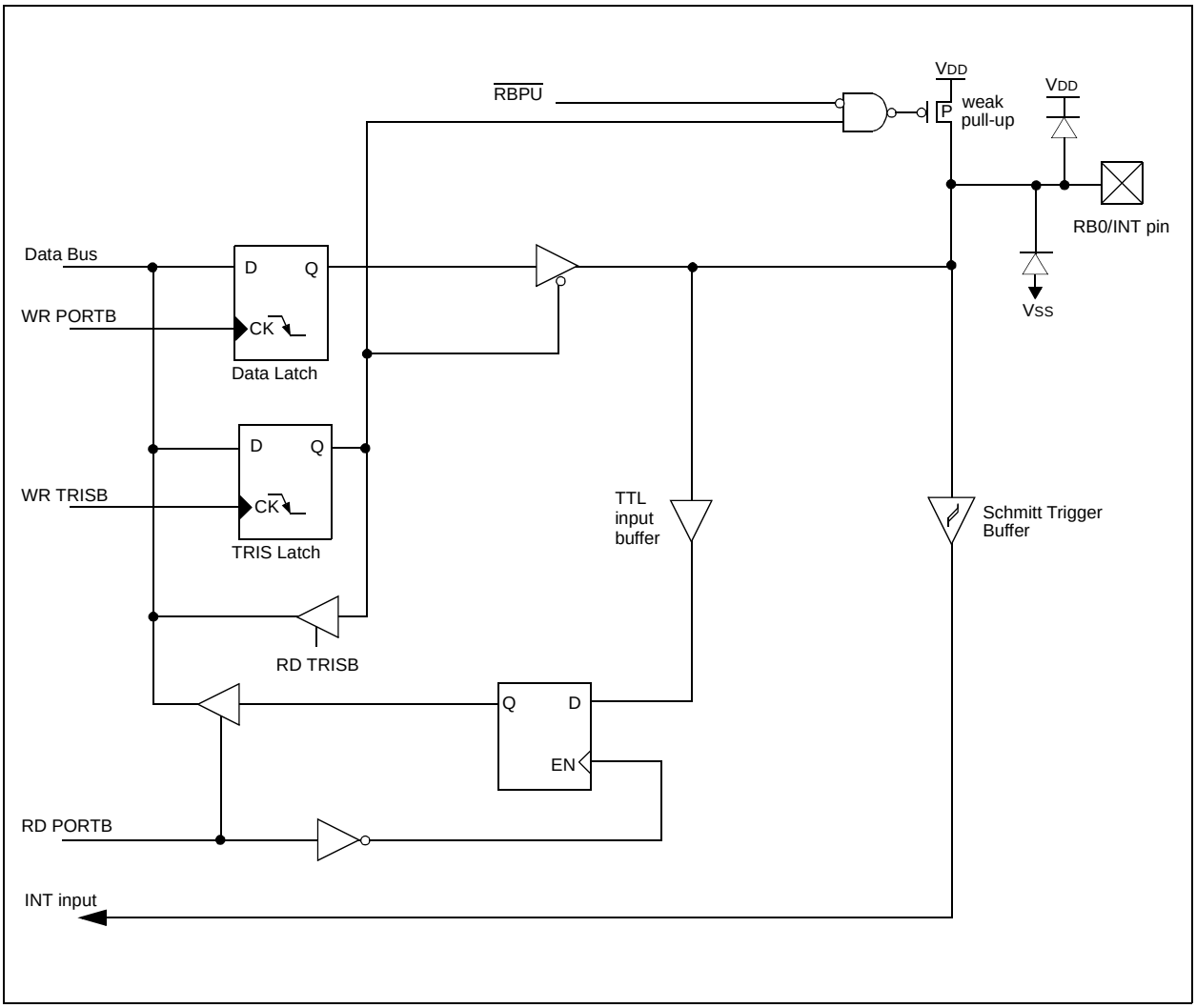
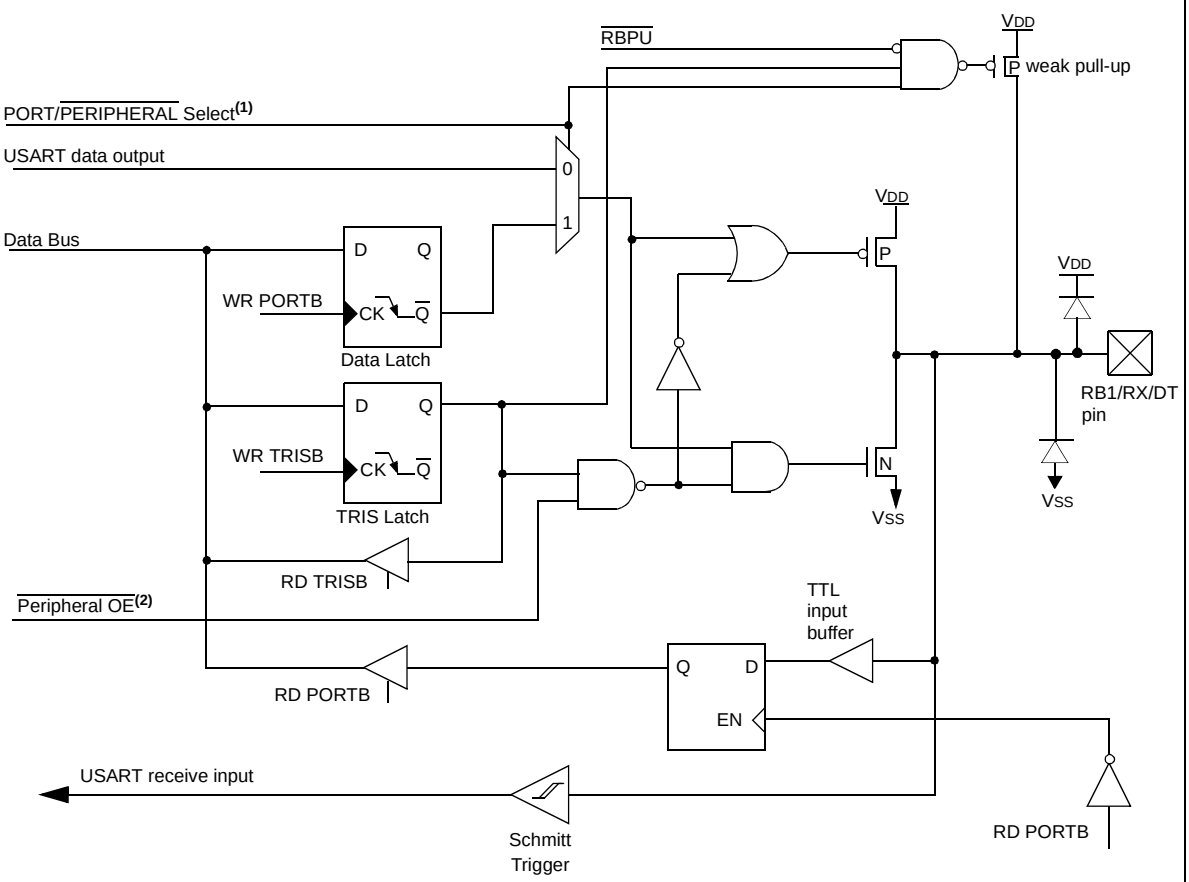
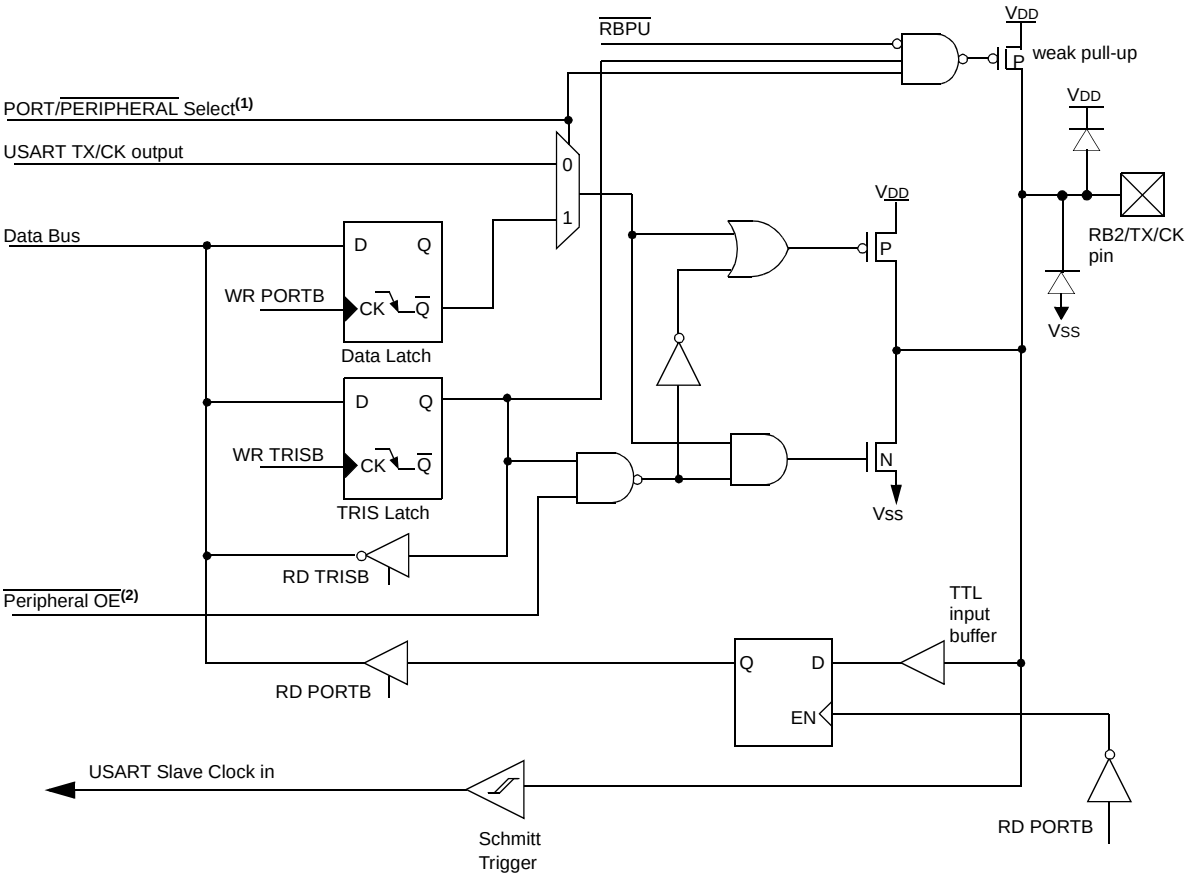


FIGURE 2: BLOCK DIAGRAM OF RB1/TX/DT PIN



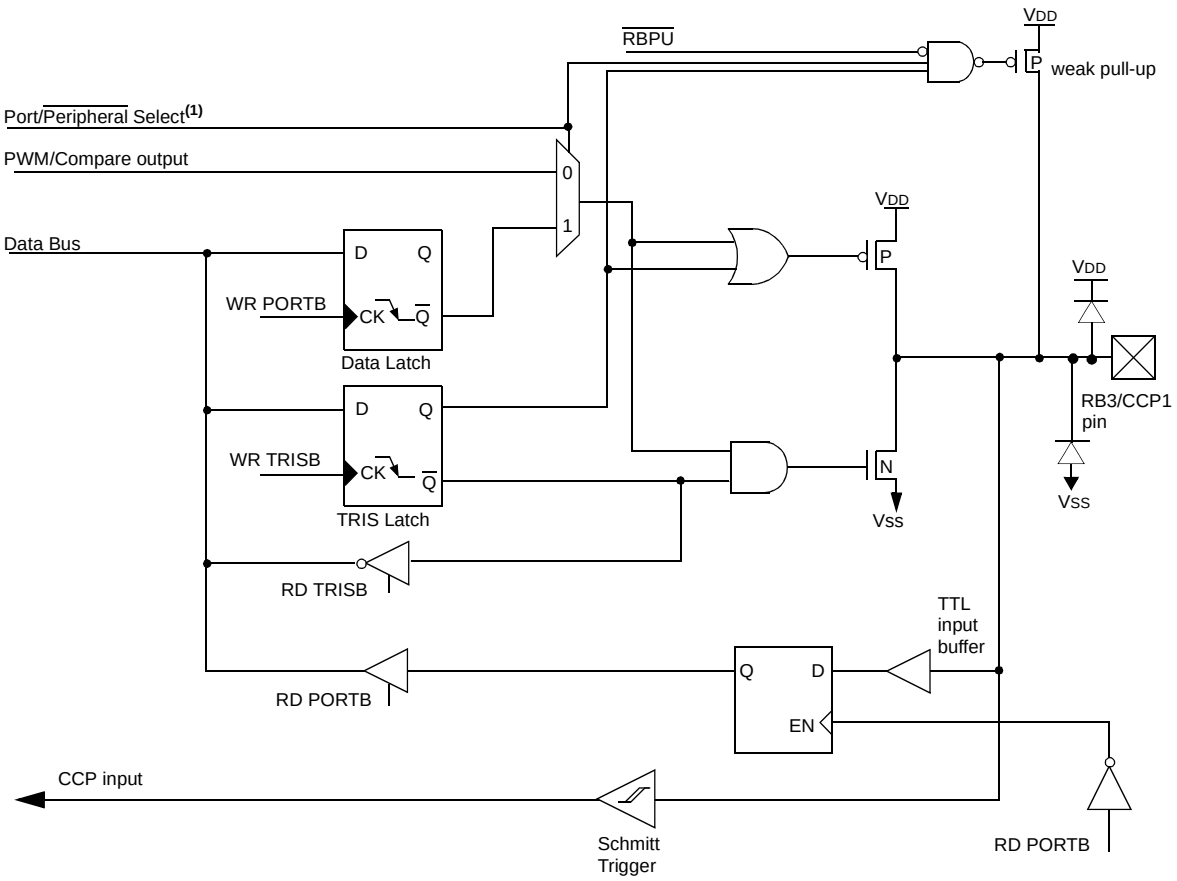
Note 1: Port/Peripheral select signal selects between port data and peripheral output.
2: Peripheral OE (output enable) is only active if peripheral select is active.

FIGURE 3: BLOCK DIAGRAM OF RB2/TX/CK PIN



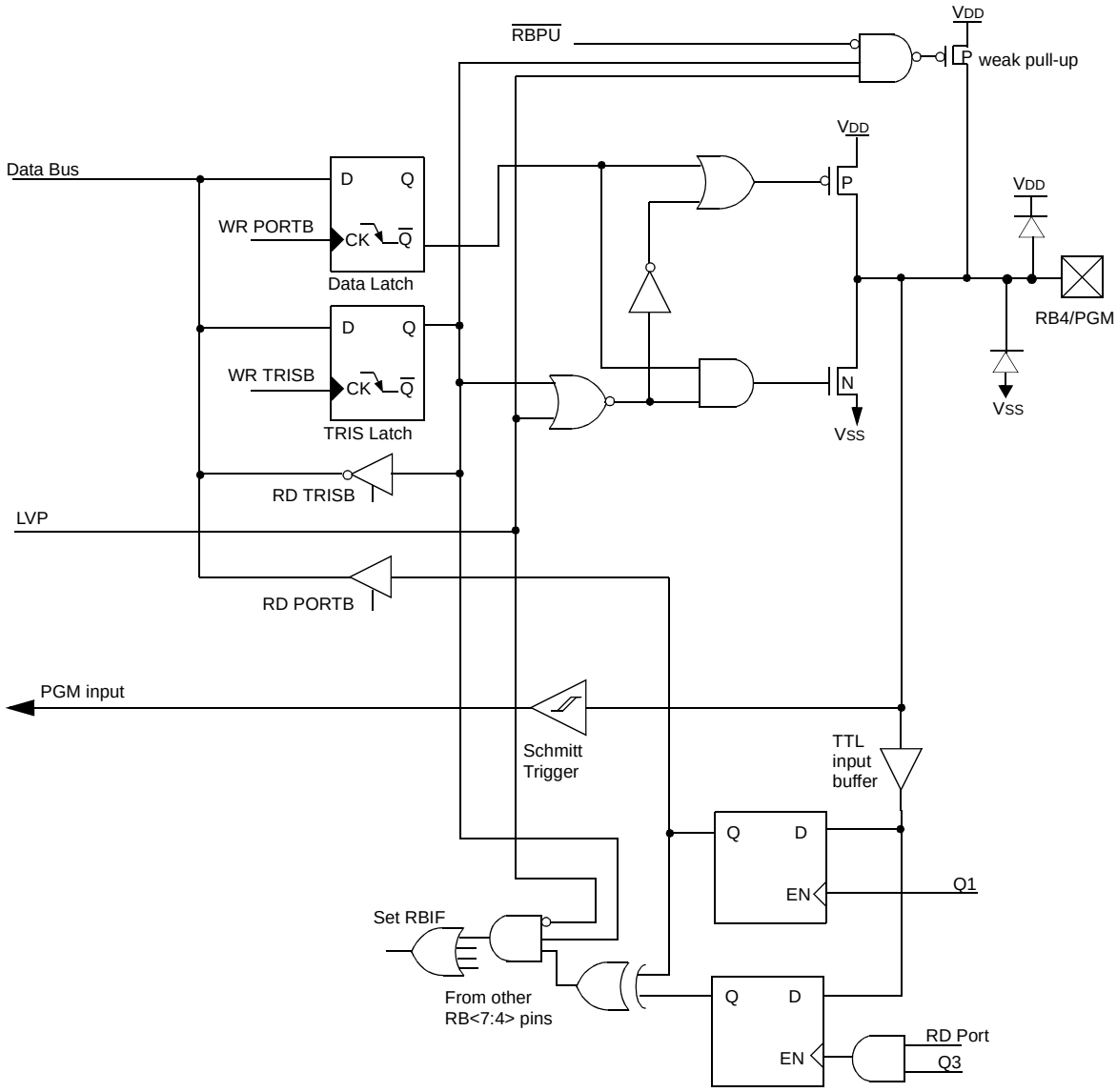
Note 1: Port/Peripheral select signal selects between port data and peripheral output.
2: Peripheral OE (output enable) is only active if peripheral select is active.

FIGURE 4: BLOCK DIAGRAM OF THE RB3/CCP1 PIN



Note 1: Peripheral Select is defined by CCP1M3:CCP1M0. (CCP1CON<3:0>)

FIGURE 5: BLOCK DIAGRAM OF RB4/PGM PIN



Note: The low voltage programming disables the interrupt on change and the weak pull-ups on RB4.

FIGURE 6: BLOCK DIAGRAM OF RB5 PIN

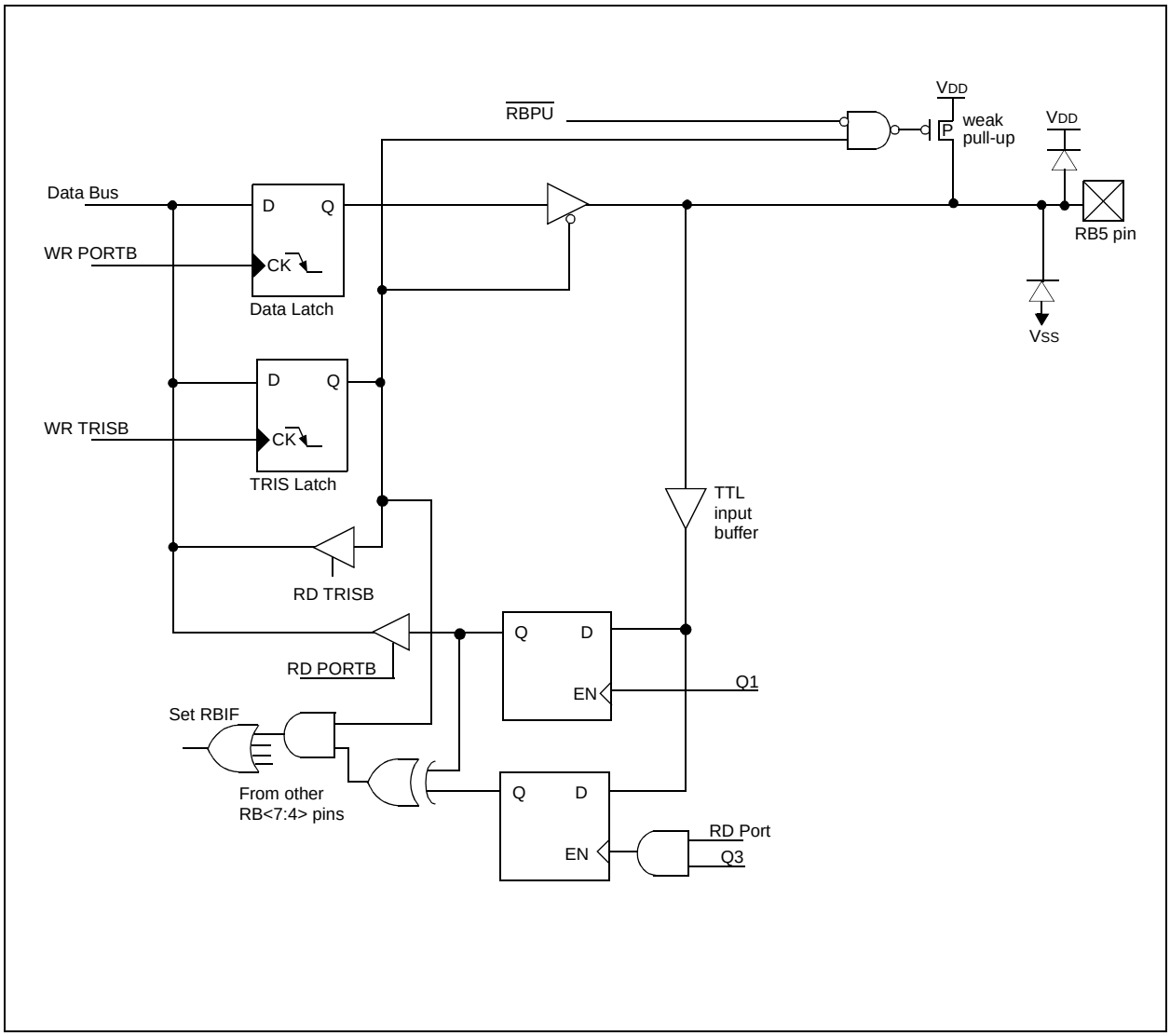


FIGURE 7: BLOCK DIAGRAM OF RB6/T1OSO/T1CKI PIN

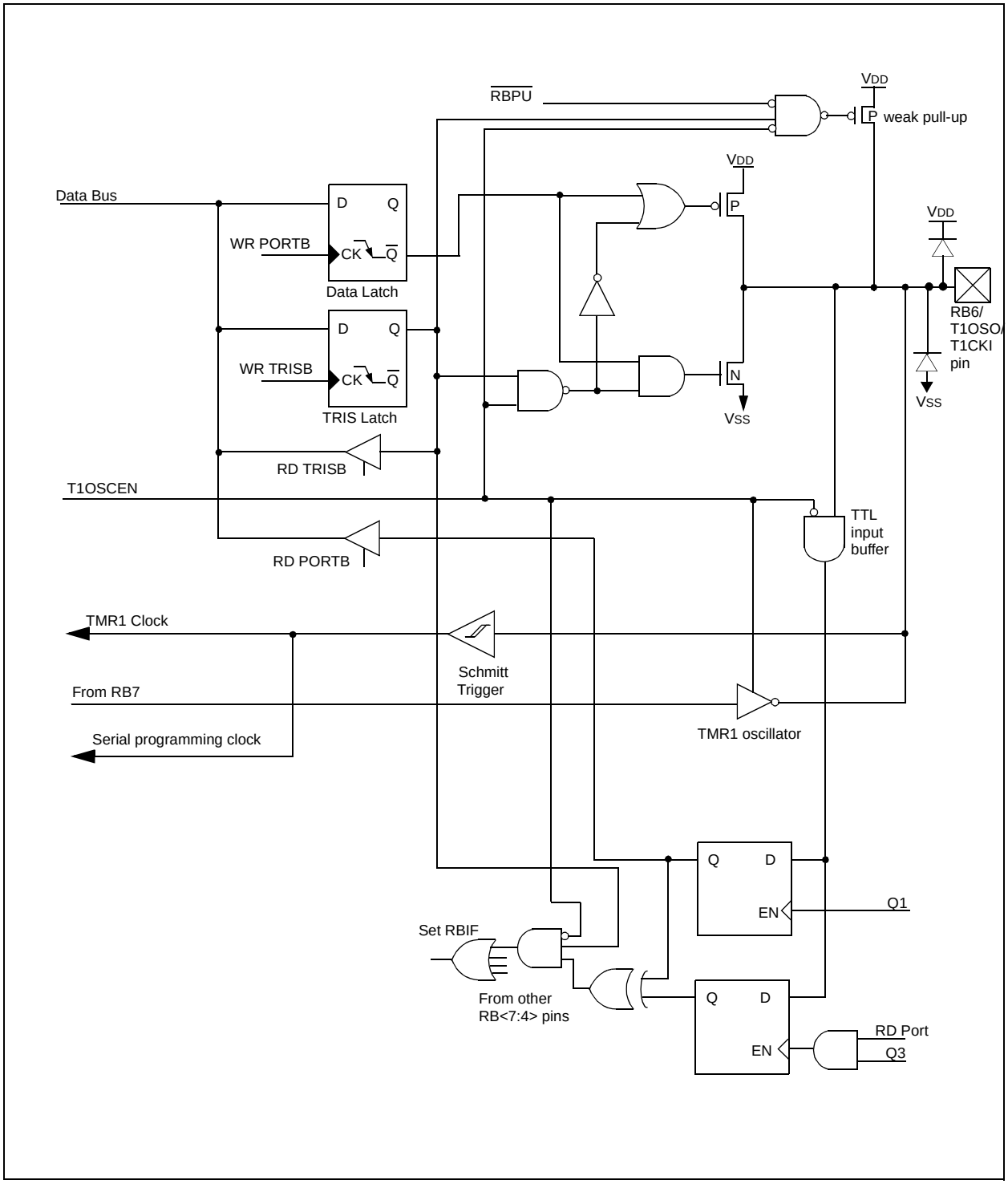


FIGURE 8: BLOCK DIAGRAM OF THE RB7/T1OSI PIN

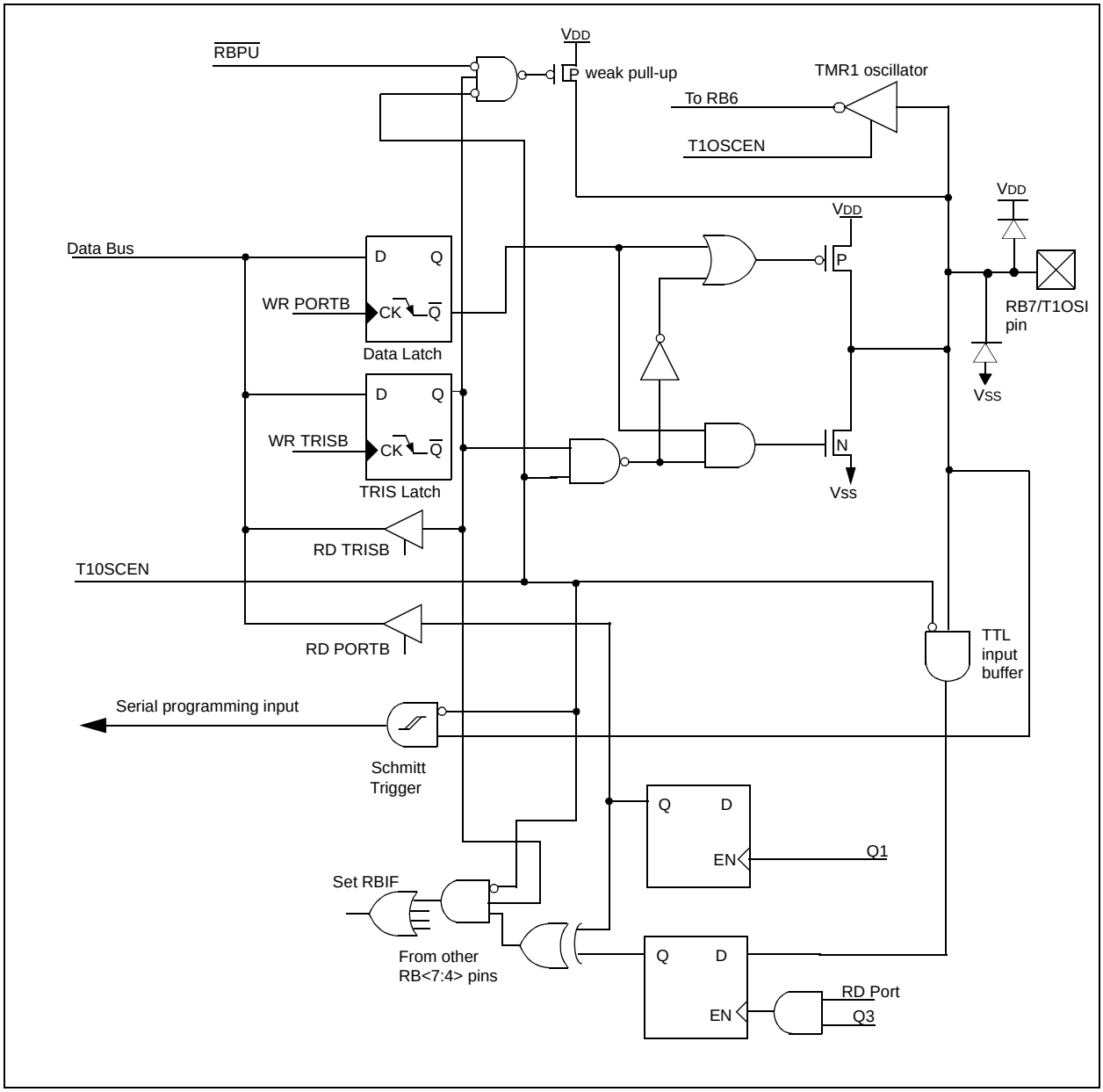
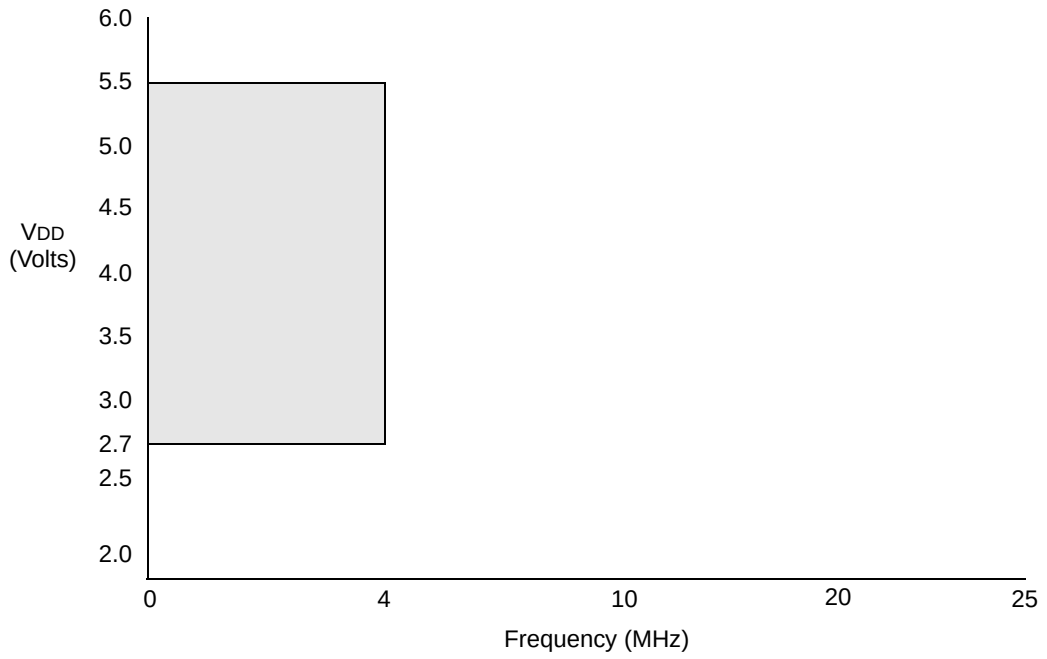


FIGURE 9: PIC16LF628 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ 0°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS40300**B**), the following clarifications and corrections should be noted.

1. The bit T1SYNC in the Register T1CON (address 10h) should be asserted logic low (ie., $\overline{\text{T1SYNC}}$. Table 4-1, page 15, and Table 10-2, page 65, of DS40300B should be listed as follows:
2. The bit ADEN in Register RCSTA (address 18h), Table 4-1, is misspelled. The correct spelling should be ADDEN. This also appears in Figures and text on pages 72, 79, 80, 81, 82, 83, 84, 85, 86 and 89.

TABLE 4-1: SPECIAL REGISTERS SUMMARY BANK0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other Resets(1)
Bank 0											
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	--00 0000	--uu uuuu
18h	RCSTA	SPEN	RX9	SREN	CREN	ADEN	FERR	OERR	RX9D	0000 -00x	0000 -00x

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (non power-up) resets include $\overline{\text{MCLR}}$ Reset, Brown-out Detect and Watchdog Timer Reset during normal operation.

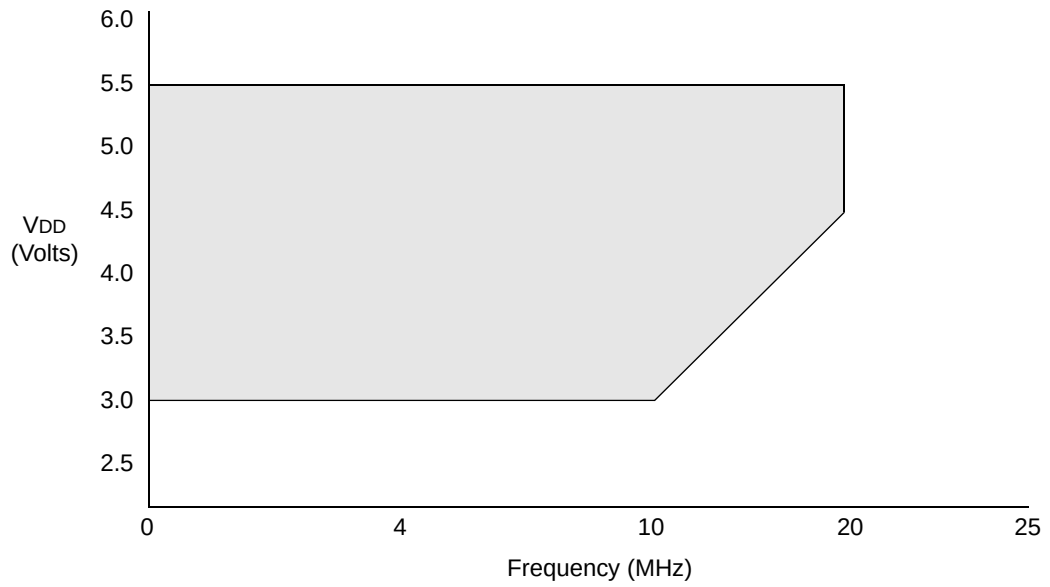
TABLE 10-2 REGISTERS ASSOCIATED WITH CAPTURE, COMPARE, AND TIMER1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on all other resets
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	--00 0000	--uu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by Capture and Timer1.

3. Valid regions of operation:

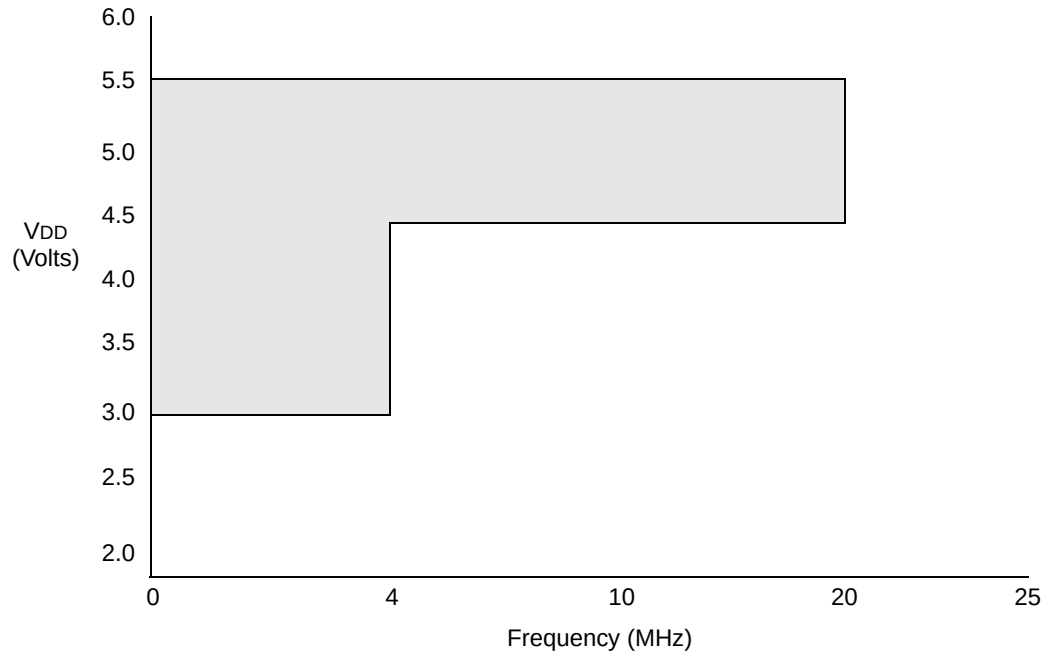
FIGURE 17-1: PIC16F62X VOLTAGE-FREQUENCY GRAPH, 0°C ≤ TA ≤ +70°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

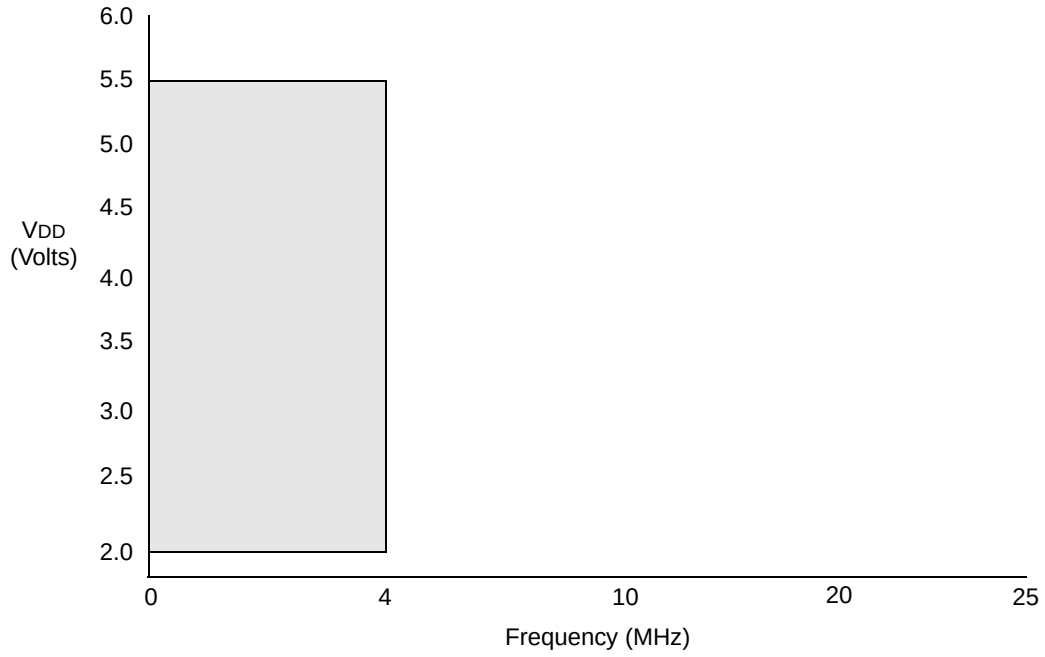
FIGURE 17-2: PIC16F62X VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA < 0°C, +70°C < TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

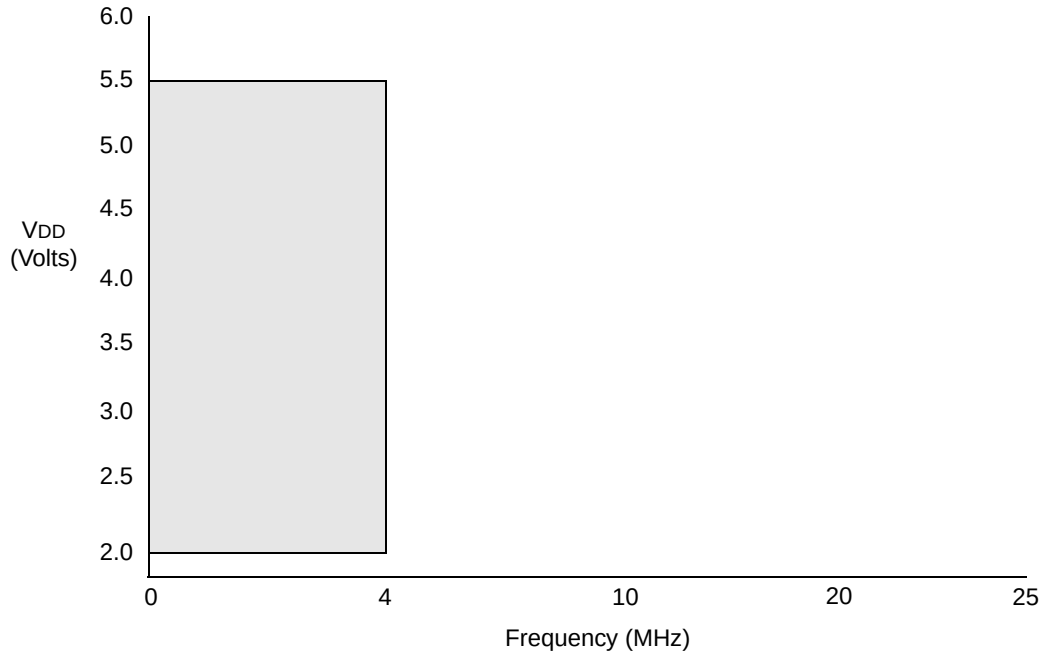
FIGURE 17-3: PIC16LF62X VOLTAGE-FREQUENCY GRAPH, 0°C ≤ TA ≤ +70°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

FIGURE 17-4: PIC16LF62X VOLTAGE-FREQUENCY GRAPH, +70°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

**TABLE 17-1: DC CHARACTERISTICS: PIC16F62X-04 (COMMERCIAL, INDUSTRIAL, EXTENDED)
PIC16F62X-20 (COMMERCIAL, INDUSTRIAL, EXTENDED)**

		Standard Operating Conditions (unless otherwise stated) Operating temperature –40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and –40°C ≤ TA ≤ +125°C for extended					
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	Supply Voltage	3.0	-	5.5	V	
D002	VDR	RAM Data Retention Voltage (Note 1)	–	1.5*	–	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure Power-on Reset	–	Vss	–	V	See section on power-on reset for details
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	–	–	V/ms	See section on power-on reset for details
D005	VBOD	Brown-out Detect Voltage	3.7	4.0	4.35	V	BODEN configuration bit is cleared
D010	IDD	Supply Current (Note 2, 5)	–	–	0.7	mA	FOSC = 4.0MHz, VDD = 3.0
							FOSC = 4.0MHz, VDD = 5.5*
D013			–	4.0	7.0	mA	FOSC = 20.0MHz, VDD = 5.5*
			–	–	6.0	mA	FOSC = 20.0MHz, VDD = 4.5
			–	–	2.0	mA	FOSC = 10.0MHz, VDD = 3.0 (Note 6)
							FOSC = 32kHz, VDD = 3.0
D020	IPD	Power Down Current (Note 3)	–	–	2.2	µA	VDD = 3.0
			–	–	5.0	µA	VDD = 4.5
			–	–	9.0	µA	VDD = 5.5*
			–	–	15.0	µA	VDD = 5.5 Extended*
D022	ΔIWDT	WDT Current (Note 4)	–	6.0	20	µA	VDD = 4.0V
					25	µA	(125°C)
D022A	ΔIBOD	Brown-out Detect Current (Note 4)	–	75	125	µA	BOD enabled, VDD = 5.0V
D023	ΔICOMP	Comparator Current for each Comparator (Note 4)	–	30	50	µA	VDD = 4.0V
D023A	ΔIVREF	VREF Current (Note 4)	–		135	µA	VDD = 4.0V
1A	FOSC	LP Oscillator Operating Frequency	0	–	200	kHz	All temperatures
		INTRC Oscillator Operating Frequency	–	–	4	MHz	All temperatures
		XT Oscillator Operating Frequency	0	–	4	MHz	All temperatures
		HS Oscillator Operating Frequency	0	–	20	MHz	All temperatures

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,
MCLR = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

5: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula, Ir = VDD/2Rext (mA) with Rext in kΩ.

6: Commercial temperature range only.

TABLE 17-2: DC CHARACTERISTICS: PIC16LF62X-04 (COMMERCIAL, INDUSTRIAL, EXTENDED)

		Standard Operating Conditions (unless otherwise stated) Operating temperature –40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and –40°C ≤ TA ≤ +125°C for extended Operating voltage VDD range as described in DC spec Table 17-1 and Table 12-2					
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	Supply Voltage	2.0	-	5.5	V	
D002	VDR	RAM Data Retention Voltage (Note 1)	–	1.5*	–	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure Power-on Reset	–	VSS	–	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	–	–	V/ms	See section on Power-on Reset for details
D005	VBOD	Brown-out Detect Voltage	3.7	4.0	4.35	V	BODEN configuration bit is cleared
D010	IDD	Supply Current (Note 2, 5)	–	–	0.6	mA	FOSC = 4.0MHz, VDD = 2.0, WDT disabled (Note 5)
D013							FOSC = 4.0MHz, VDD = 5.5, WDT disabled (Note 5)* FOSC = 32kHz, VDD = 2.0, WDT disabled
D020	IPD	Power Down Current (Note 2, 3)					VDD = 2.0
			–	–	2.0	µA	VDD = 2.5*
			–	–	2.2	µA	VDD = 3.0*
			–	–	9.0	µA	VDD = 5.5
					15.0	µA	VDD = 5.5 Extended
	ΔIWDT	WDT Current (Note 4)	–	6.0	15	µA	VDD = 3.0V
D023	ΔIBOD	Brown-out Detect Current (Note 4)	–	75	125	µA	BOD enabled, VDD = 5.0V
	ΔICOMP	Comparator Current for each Comparator (Note 4)	–	30	50	µA	VDD = 3.0V
	ΔIVREF	VREF Current (Note 4)	–		135	µA	VDD = 3.0V
1A	FOSC	LP Oscillator Operating Frequency	0	–	200	kHz	All temperatures
		INTRC Oscillator Operating Frequency	–	–	4	MHz	All temperatures
		XT Oscillator Operating Frequency	0	–	4	MHz	All temperatures
		HS Oscillator Operating Frequency	0	–	20	MHz	All temperatures

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD to VSS.

4: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

5: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kΩ.

TABLE 17-3: DC CHARACTERISTICS: PIC16F62X (COMMERCIAL, INDUSTRIAL, EXTENDED) PIC16LF62X (COMMERCIAL, INDUSTRIAL, EXTENDED)

		Standard Operating Conditions (unless otherwise stated) Operating temperature –40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial and –40°C ≤ TA ≤ +125°C for extended Operating voltage VDD range as described in DC spec Table 17-1 and Table 12-2					
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Unit**	**Conditions**
	VIL	**Input Low Voltage**					
		I/O ports					
D030		with TTL buffer	VSS	–	0.8V 0.15VDD	V	VDD = 4.5V to 5.5V otherwise
D031		with Schmitt Trigger input	VSS		0.2VDD	V	
D032		$\overline{MCLR}$, RA4/T0CKI,OSC1 (in ER mode)	Vss	–	0.2VDD	V	Note1
D033		OSC1 (in XT and HS)	Vss	–	0.3VDD	V	
		OSC1 (in LP)	Vss	–	0.6VDD-1.0	V	
	VIH	**Input High Voltage**					
		I/O ports		–			
D040		with TTL buffer	2.0V .25VDD + 0.8V	–	VDD VDD	V	VDD = 4.5V to 5.5V otherwise
D041		with Schmitt Trigger input	0.8VDD	–	VDD		
D042		$\overline{MCLR}$ RA4/T0CKI	0.8VDD	–	VDD	V	
D043		OSC1 (XT, HS and LP)	0.7VDD	–	VDD	V	
D043A		OSC1 (in ER mode)	0.9VDD				Note1
D070	IPURB	PORTB weak pull-up current	50	200	400	µA	VDD = 5.0V, VPIN = VSS
	IIL	**Input Leakage Current** (Notes 2, 3)					
		I/O ports (Except PORTA)			±1.0	µA	VSS ≤ VPIN ≤ VDD, pin at hi-impedance
D060		PORTA	–	–	±0.5	µA	Vss ≤ VPIN ≤ VDD, pin at hi-impedance
D061		RA4/T0CKI	–	–	±1.0	µA	Vss ≤ VPIN ≤ VDD
D063		OSC1, $\overline{MCLR}$	–	–	±5.0	µA	Vss ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
	VOL	**Output Low Voltage**					
D080		I/O ports	–	–	0.6	V	IOL=8.5 mA, VDD=4.5V, -40° to +85°C
			–	–	0.6	V	IOL=7.0 mA, VDD=4.5V, +125°C
D083		OSC2/CLKOUT (ER only)	–	–	0.6	V	IOL=1.6 mA, VDD=4.5V, -40° to +85°C
			–	–	0.6	V	IOL=1.2 mA, VDD=4.5V, +125°C
	VOH	**Output High Voltage** (Note 3)					
D090		I/O ports (Except RA4)	VDD-0.7	–	–	V	IOH=-3.0 mA, VDD=4.5V, -40° to +85°C
			VDD-0.7	–	–	V	IOH=-2.5 mA, VDD=4.5V, +125°C
D092		OSC2/CLKOUT (ER only)	VDD-0.7	–	–	V	IOH=-1.3 mA, VDD=4.5V, -40° to +85°C
			VDD-0.7	–	–	V	IOH=-1.0 mA, VDD=4.5V, +125°C
*D150	VOD	**Open-Drain High Voltage**		–	8.5*	V	RA4 pin PIC16F62X, PIC16LF62X
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2 pin		–	15	pF	In XT, HS and LP modes when external clock used to drive OSC1.
D101	CIO	All I/O pins/OSC2 (in ER mode)		–	50	pF	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

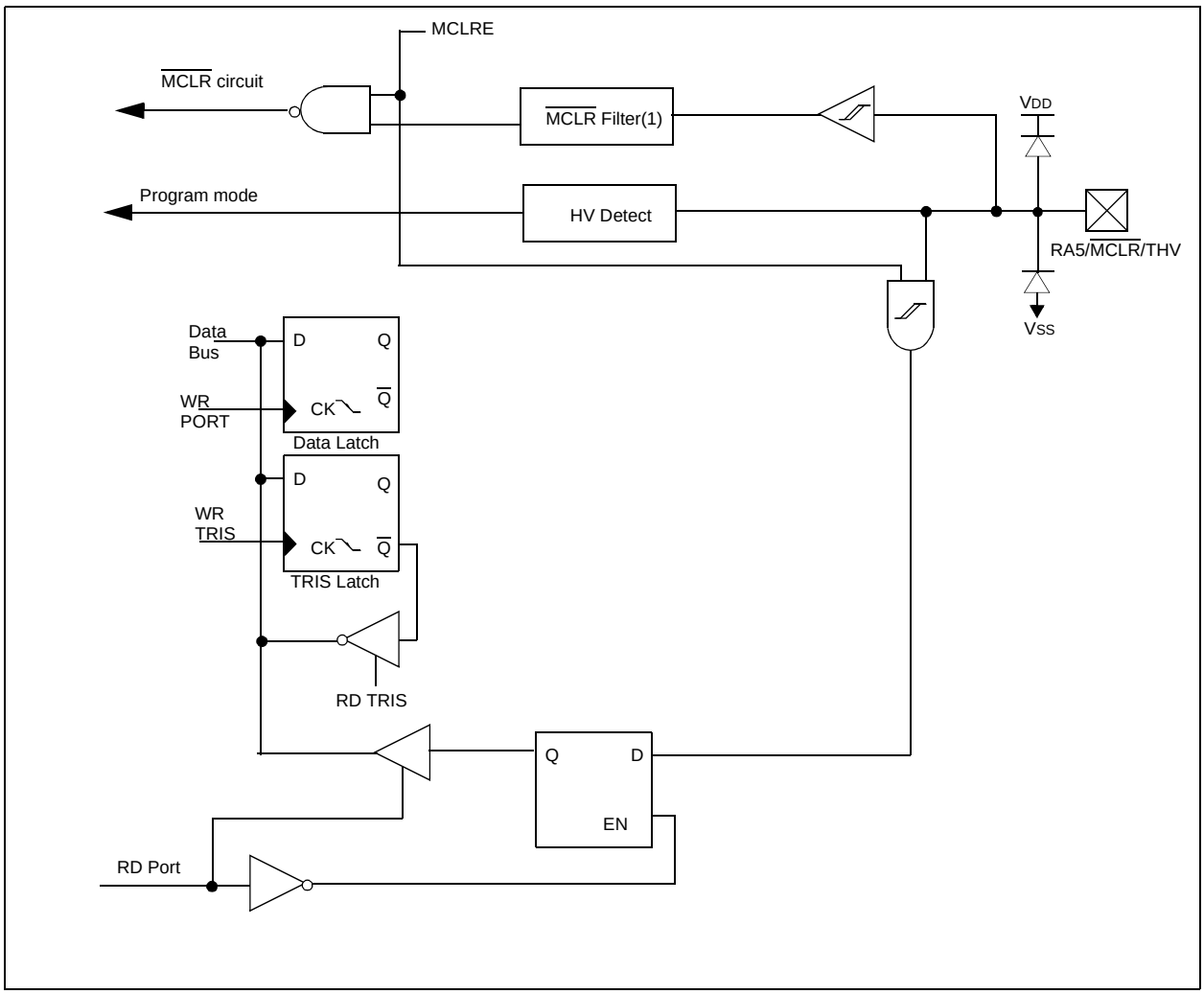
Note 1: In ER oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16F62X be driven with external clock in ER mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4. The following block diagram shown in Section 5, Figure 5-5 is incorrect. The following figure should be used instead.

FIGURE 5-5: BLOCK DIAGRAM OF THE RA5/$\overline{\text{MCLR}}$/THV PIN



5. The example given in Section 9, Example 9-1, concerning Initializing the Comparator Module is incorrect. The following code example should be used instead.

EXAMPLE 9-1: INITIALIZING COMPARATOR MODULE

```
        BCF         INTCON,GIE       ; Turn OFF Global Interrupts
        BCF         INTCON,PEIE      ; Turn OFF Peripheral Interrupts
        CLRF        PORTA            ; Init Port A
        MOVLW       0X03             ; Init comparator mode
        MOVWF       CMCON            ; CM<2:0> = 011
        BSF         STATUS,RP0       ; Select BANK 1
        MOVLW       0x07             ; Initialize Port A Direction
        MOVWF       TRISA            ; Set RA<2:0> as Inputs
                                     ; RA<4:3> as outputs
                                     ; TRIS<5> always reads '0'
        BCF         STATUS,RP0       ; Select BANK 0
        CALL        DELAY10          ; Wait 10us for comparator output to become valid
                                     ; See Table 17-1 Parameter 301
        MOVF        CMCON,F          ; Read CMCON to end change condition
        BCF         PIR1,CMIF        ; Clear pending interrupts
        BSF         STATUS,RP0       ; Select BANK 1
        BSF         PIE1,CMIE        ; Enable Comparator Interrupts
        BCF         STATUS,RP0       ; Select BANK 0
        BSF         INTCON,PEIE      ; Enable Peripheral Interrupts
        BSF         INTCON,GIE       ; Global Interrupt Enable

        ; Insert Your code....

        ; Helper function is the Delay for 10us routine show below.

DELAY10             ; burns 8 cycles + the call for 10 cycles or 10us at 4Mhz
        goto $+1    ; goto the next instruction and burn 2 cycles
        call retlbl ; goto the next instruction and burn 2 more cycles
retlbl  return      ; go back and burn 2 cycles (actualy done 2x for 4 cycles consumed)
```

6. The examples given in Section 13, concerning the Data EEPROM are incorrect. The EEPROM registers are all located in Bank 1. The examples show the registers in Bank 0 and Bank 1. The following code examples should be used instead to use this feature.

EXAMPLE 13-1: DATA EEPROM READ

```
BSF     STATUS, RP0  ; Bank 1
MOVLW   CONFIG_ADDR  ;
MOVWF   EEADR        ; Address to read
BSF     EECON1, RD   ; EE Read
MOVF    EEDATA, W    ; W = EEDATA
BCF     STATUS, RP0  ; Bank 0
```

EXAMPLE 13-2: DATA EEPROM WRITE

```
                     ; set up the data and
                       the address
BSF     STATUS, RP0  ; Bank 1
MOVLW   CONFIG_ADDR  ;
MOVWF   EEADR        ; Address to write
MOVLW   CONFIG_DATA  ;
MOVWF   EEDATA       ; Data to write

                     ; perform the write
                       operation
BSF     EECON, WREN  ; Enable Write
BCF     INTCON, GIE  ; Disable INTs
MOVLW   055h         ;
MOVWF   EECON2       ; Write 55
MOVLW   0AAh         ;
MOVWF   EECON2       ; Write AA
BSF     EECON1, WR   ; Set WR bit
BCF     STATUS, RP0  ; Bank 0
```

EXAMPLE 13-3: DATA EEPROM VERIFY

```
; after the write in complete (i.e. in the
  write interrupt)
    BSF   STATUS, RP0 ; Bank 1
    MOVF  EEDATA, W   ; load the last
                        written value into W
    BSF   EECON, RD   ; start a read
;
; Is the value written (in W Reg) and
; read (in EEDATA) the same?
;
    SUBWF EEDATA, W   ; the EEDATA has fresh
                        data
    BTFSS STATUS, Z   ; Is the Zero flag set?
    GOTO  WRITE_ERR   ; NO, Write Error
                      ; YES, Good Write
                      ; continue program
```

NOTES:

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