PIC16CR63 Rev. A Silicon Errata Sheet

The PIC16CR63 parts you have received conform functionally to the Device Data Sheet (**DS30234D**), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC16CR63 silicon.

1. **Module: CCP (Compare Mode)**

   The Compare mode may not operate as expected when configuring the compare match to drive the I/O pin low (CCPxM<3:0> = 1001).

   When the CCP module is changed to compare output low (CCPxM<3:0> = 1001) from any other non-compare CCP mode, the I/O pin will immediately be driven low regardless of the state of the I/O data latch. The pin will remain low when the compare match occurs (see Table 1).

   However, when the CCP module is changed to compare output high (CCPxM<3:0> = 1000) from any other CCP mode, the I/O pin will immediately be driven low regardless of the state of the I/O data latch. The pin will be driven high when the compare match occurs.

TABLE 1: COMPARE OUTPUT LOW SWITCHING

CCP Mode CCPxM<3:0> =	I/O pin State	Change CCP to CCPxM<3:0> =	
		1001	1000
0xxx	H	L	L
	L	L	L
1000	H	H	—
	L	L	—
1001	H	—	L
	L	—	L
101x	H	L	L
	L	L	L
11xx	H	L	L
	L	L	L

Work Around

To have the I/O pin high until the compare match low occurs, force a compare match high to get the I/O pin into the high state, then reconfigure the compare match to force the I/O low, when the compare condition occurs.

2. **Module: SSP Module (I^2C™ mode)**

   If the bus is active when the I^2C mode is enabled, and the next 8-bits of data on the bus match the address of the device, then the SSP module will generate an acknowledge pulse.

   Work Around

   Before enabling the I^2C mode, ensure that the bus is not active.

3. **Module: Timer0**

   The TMR0 register may increment when the WDT postscaler is switched to the Timer0 prescaler. If TMR0 = FFh, this will cause TMR0 to overflow (setting T0IF).

   Work Around

   Follow the following sequence:

a) Read the 8-bit TMR0 register into the W register
b) Clear the TMR0 register
c) Assign WDT postscaler to Timer0
d) Write W register to TMR0

Note: As with any windowed EPROM device, please cover the window at all times, except when erasing.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (**DS30234D**), the following clarifications and corrections should be noted.

1. Module: I/O Ports

The specification for the High Voltage Open Drain I/O (The RA4 pin on most devices) cannot be met without possible long term reliability issues on that I/O pin. If a high voltage drive is required, use an external transistor that can support the required voltage.

TABLE 2: DC SPECIFICATION CHANGES FROM DATA SHEET

Param No.	Sym.	Characteristic	New Specification			Data Sheet Specification			Units
			Min	Typ	Max	Min	Typ	Max	
D150	V_{OD}	Open-drain High Voltage	—	—	10	—	—	14	V

2. Module: SSP (SPI Mode Timing Specifications)

a) The SPI interface timings have been modified to the values shown in Table 3.

TABLE 3: DC SPECIFICATION CHANGES FROM DATA SHEET

Parm No.	Sym.	Characteristic		New Specification			Data Sheet Specification			Units
				Min	Typ	Max	Min	Typ	Max	
71	T_{SCH}	SCK input high time (slave mode)	Continuous	1.25 T_{CY} + 30 ns	—	—	T_{CY} + 20 ns	—	—	ns
71A			Single Byte (1)	40	—	—	N.A.			ns
72	T_{SCL}	SCK input low time (slave mode)	Continuous	1.25 T_{CY} + 30 ns	—	—	T_{CY} + 20 ns	—	—	ns
72A			Single Byte (1)	40	—	—	N.A.			ns
73A	T_{B2B}	Last clock edge of the Byte1 to 1st clock edge of the Byte2 (1)		1.5 T_{CY} + 40 ns	—	—	N.A.			ns

* This parameter is characterized but not tested

Note 1: Specification 73A is only required if specifications 71A and 72A are used.

3. Module: Timer1

a) The operation of Timer1 needs some clarification when the timer registers are written when the TMR1ON bit is set.

The internal clock signal that is the input to the TMR1 prescaler affects the incrementing of Timer1 (TMR1H:TMR1L registers and the Timer1 prescaler). When the Timer1 registers are NOT written, the Timer1 will increment on the rising edge of the TMR1 increment clock.

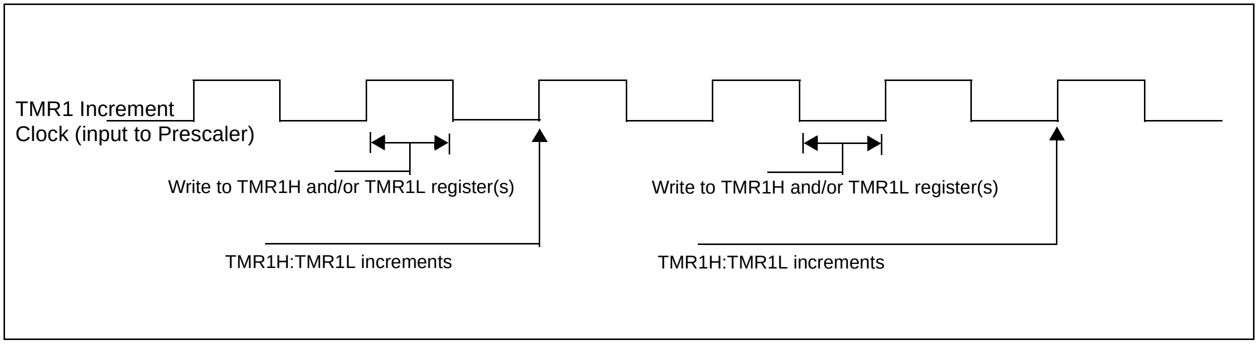
When the TMR1H and/or TMR1L registers are written while this clock is high, TMR1 will increment on the next rising edge of this clock.

When the TMR1H and/or TMR1L registers are written while this clock is low, TMR1 will not increment on the next rising edge of this clock, but must first have a falling clock and the the rising clock for TMR1 to increment.

Figure 1 shows the two cases of writes to the TMR1H and/or TMR1L registers. Due to the V_{IH} and V_{IL} thresholds on the oscillator/clock pins, external Timer1 oscillator components, and external clock frequency, the Timer1 increment clock may not be of a 50% duty cycle.

The TMR1 increment clock is out of phase of the T1OSO/T1CKI pin by a small propagation delay.

FIGURE 1: WRITES TO TIMER1 (EXTERNAL CLOCK / OSCILLATOR MODE)



1. The Brown-out Reset Voltage specification is different than that specified in the Data Sheet.

22.1 DC Characteristics: PIC16CR63-04 (Commercial, Industrial) PIC16CR63-10 (Commercial, Industrial) PIC16CR63-20 (Commercial, Industrial)

DC CHARACTERISTICS	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +85°C for industrial and 0°C ≤ T_A ≤ +70°C for commercial						
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D005	Brown-out Reset Voltage	B_{VDD}	3.65	4.0	4.35	V	BODEN configuration bit is enabled

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which V_{DD} can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all I_{DD} measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to V_{DD},
$\overline{\text{MCLR}}$ = V_{DD}; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V_{DD} and V_{SS}.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = V_{DD}/2Rext (mA) with Rext in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base I_{DD} or I_{PD} measurement.

REVISION HISTORY

Rev A Document

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