



PIC16F77

PIC16F77 Rev. B1 Silicon Errata Sheet

The PIC16F77 Rev. B1 parts you have received conform functionally to the Device Data Sheet (DS30325A), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC16F77 silicon.

1. Module: Timer1

When Timer1 is running in Asynchronous mode and then disabled, data in the Timer1 register (TMR1) may become corrupted. Corruption occurs when the timer enable is turned off at the same instant that a ripple carry occurs in the timer module.

This issue only occurs in asynchronous operation. In synchronous operation, the relevant signals are latched with the CPU clock and the problem condition does not arise.

Work around

When Timer1 is configured to operate as an asynchronous counter, care must be taken that there is no incoming pulse while the module is being turned off. If an incoming pulse arrives while Timer1 is being turned off, the value of register TMR1 may become corrupted.

If an application requires that Timer1 be turned off, and if it is possible that Timer1 may receive an incoming pulse while being turned off, synchronize the external clock first by clearing the T1SYNC bit of register T1CON (T1CON<2>). Please note, however, that this may cause Timer1 to miss up to one count.

Note: As with any windowed EPROM device, please cover the window at all times, except when erasing.

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Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS30325A), the following clarifications and corrections should be noted.

None.

REVISION HISTORY

Rev A Document (2/01)
Original errata document.
Issue 1 (Timer1), page 1.

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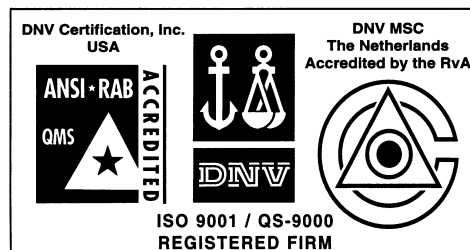
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