

PIC16C924 Rev. A Silicon Errata Sheet

The PIC16C924 (Rev. A) parts you have received conform functionally to the Device Data Sheet (DS30444D), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC16C924 silicon.

1. Module: 8-bit A/D Module

If the Analog Port is configured so that all analog pins are digital inputs (PCFG2:PCFG0 = 11xb), then doing a conversion on any pin of the analog port will give a result of ADRES = 0xFF.

Work Around

Configure the PCFG2:PCFG0 bits to a value that has any pin of the analog port configured as an analog input (such as PCFG2:PCFG0 = 100b). Conversion on any pin of the analog port (analog or digital) will now convert as expected.

2. Module: CCP (Compare Mode)

The Compare mode may not operate as expected when configuring the compare match to drive the I/O pin low (CCPxM<3:0> = 1001).

When the CCP module is changed to compare output low (CCPxM<3:0> = 1001) from any other non-compare CCP mode, the I/O pin will immediately be driven low regardless of the state of the I/O data latch. The pin will remain low when the compare match occurs (see Table 1).

However, when the CCP module is changed to compare output high (CCPxM<3:0> = 1000) from any other CCP mode, the I/O pin will immediately be driven low regardless of the state of the I/O data latch. The pin will be driven high when the compare match occurs.

TABLE 1: Compare Output Low Switching

| CCP Mode CCPxM<3:0> = | I/O pin State | Change CCP to CCPxM<3:0> = | |
|--------------------------|------------------|-------------------------------|------|
| | | 1001 | 1000 |
| 0xxx | H | L | L |
| | L | L | L |
| 1000 | H | H | — |
| | L | L | — |
| 1001 | H | — | L |
| | L | — | L |
| 101x | H | L | L |
| | L | L | L |
| 11xx | H | L | L |
| | L | L | L |

Work Around

To have the I/O pin high until the compare match low occurs, force a compare match high to get the I/O pin into the high state, then reconfigure the compare match to force the I/O low, when the compare condition occurs.

Note: As with any windowed EPROM device, please cover the window at all times, except when erasing.

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3. Module: CCP (Compare Mode)

The special event trigger of the Compare mode may not occur if both of the following conditions exist:

- An instruction one cycle (T_{CY}) prior to a Timer1/Compare register match has literal data equal to the address of a CCP register being used.⁽¹⁾
- An instruction in the same cycle as a Timer1/Compare register match has an MSb of '0'.

The interrupt for the compare event will still be generated, but no special event trigger will occur.

Note 1: 15h(CCPR1L), 16h(CCPR1H) or 17h(CCP1CON) for CCP1.

Work Around

Use the interrupt service routine instead of using the special event trigger to reset Timer1 (and start an A/D conversion, if applicable).

4. Module: SSP Module (I²C mode)

If the bus is active when the I²C mode is enabled, and the next 8-bits of data on the bus match the address of the device, then the SSP module will generate an acknowledge pulse.

Work Around

Before enabling the I²C mode, ensure that the bus is not active.

5. Module: SSP (SPI Mode)

The Synchronous Serial Port module in SPI Master mode only allows the transmission of 1 byte of data at a time. The module must be disabled and then re-enabled between each byte transmission.

Work Around

Once the SSP module has been configured in SPI Master mode and one byte of data has been transmitted, wait for the interrupt flag bit SSPIF (PIR1<3>) or BF(SSPSTAT<0>) to be set. This indicates that the byte of data has been transmitted. Then, disable the SSP by clearing the SSPEN bit of the SSPCON register. Re-enable the SSP by setting the SSPEN bit. The SPI module will now transmit the next data byte written to SSPBUF.

Example Code:

```
movwf SSPBUF      ;data byte is
                  ;in W register
bsf STATUS, RP0  ;change to bank1
wait btfs PIR1, SSPIF ;wait for xmit
                  ;buffer to empty
goto wait
bcf STATUS, RP0  ;change to bank0
bcf SSPCON, SSPEN ;disable SSP
bsf SSPCON, SSPEN ;enable SSP
```

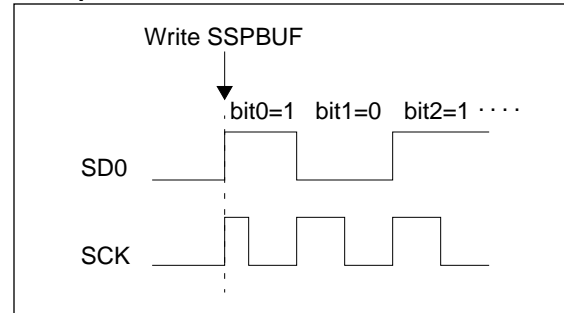
When the SSP is disabled, the PORTC data latch value is placed on the pins. The value in bit 3 of PORTC (SCK) should have the same value as the

idle state of SCK. For example, if the clock idles high, then bit 3 of PORTC must be set high. If bit 3 of PORTC is not configured the same as the idle state of the clock, you may experience an additional clock when the SPI is disabled then re-enabled.

6. Module: SSP (SPI Mode)

When the SPI is using Timer2/2 as the clock source, a shorter-than-expected SCK pulse may occur on the first bit of the transmitted/received data.

Example:



Work Around

To avoid producing the short pulse, turn off Timer2 and clear the TMR2 register, load the SSPBUF with the data to transmit, and then turn Timer2 back on.

Example Code:

```
BSF STATUS, RP0      ;Bank 1
LOOP BTFS SSPSTAT, BF ;Data received?
                  ;(Xmit complete?)
GOTO LOOP            ;No
BCF STATUS, RP0      ;Bank 0
MOVF SSPBUF, W       ;W = SSPBUF
MOVWF RXDATA        ;Save in user RAM
MOVF TXDATA, W       ;W = TXDATA
BCF T2CON, TMR2ON   ;Timer2 off
CLR TMR2             ;Clear Timer2
MOVWF SSPBUF        ;Xmit New data
BSF T2CON, TMR2ON   ;Timer2 on
```

7. Module: Timer0

The TMR0 register may increment when the WDT postscaler is switched to the Timer0 prescaler. If TMR0 = FFh, this will cause TMR0 to overflow (setting T0IF).

Work Around

Follow the following sequence:

- a) Read the 8-bit TMR0 register into the W register
- b) Clear the TMR0 register
- c) Assign WDT postscaler to Timer0
- d) Write W register to TMR0

8. Module: Timer1

The Timer1 value may unexpectedly increment if either the TMR1H or the TMR1L register is written. If Timer1 is ON, then turned OFF, performing any write instruction with TMR1H as the destination may cause TMR1L to increment.

Example 1:

```
BSF T1CON, TMR1ON
:
BCF T1CON, TMR1ON
MOVF TMR1H, 1
```

TMR1 value before MOVF instruction:

TMR1H:TMR1L = 3F:00

TMR1 value after MOVF instruction:

TMR1H:TMR1L = 3F:01

Example 2:

```
BSF T1CON, TMR1ON
:
BCF T1CON, TMR1ON
MOVF TMR1H, 1
```

TMR1 value before MOVF instruction:

TMR1H:TMR1L = FF:FF

TMR1 value after MOVF instruction:

TMR1H:TMR1L = FF:00

If Timer1 is ON, then turned OFF when TMR1H:TMR1L = xx:FF, performing any write instruction with TMR1L as the destination may cause TMR1H to increment.

Example 1:

```
BSF T1CON, TMR1ON
:
BCF T1CON, TMR1ON
CLRF TMR1L
```

TMR1 value before CLRF instruction:

TMR1H:TMR1L = FF:FF

TMR1 value after CLRF instruction:

TMR1H:TMR1L = 00:00

(TMR1IF is **not** set.)

Work Around

To preserve Timer1 register values:

Read Timer1 register values into “shadow” registers. Perform any write instruction(s) on the shadow registers. Write the shadow register values back into the Timer1 registers.

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Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS30444D), the following clarifications and corrections should be noted.

1. Module: I/O Ports

The specification for the High Voltage Open Drain I/O (The RA4 pin on most devices) cannot be met without possible long term reliability issues on that I/O pin. If a high voltage drive is required, use an external transistor that can support the required voltage.

TABLE 2: DC SPECIFICATION CHANGES FROM DATA SHEET

| Param No. | Sym. | Characteristic | New Specification | | | Data Sheet Specification | | | Units |
|-----------|------|-------------------------|-------------------|-----|-----------|--------------------------|-----|-----|-------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| D150 | VOD | Open-drain High Voltage | — | — | 10 | — | — | 14 | V |

2. Module: 8-Bit A/D

- a) The minimum A/D reference voltage has been improved to the values shown in Table 3.

TABLE 3: DC SPECIFICATION CHANGES FROM DATA SHEET

| Parm No. | Sym. | Characteristic | New Specification | | | Data Sheet Specification | | | Units |
|----------|------|-------------------|-------------------|-----|-------------|--------------------------|-----|-------------|-------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| A20 | VREF | Reference Voltage | 2.5 * | — | VDD + 0.3 V | 3.0 | — | VDD + 0.3 V | V |

* This parameter is characterized but not tested

3. Module: SSP (SPI Mode Timing Specifications)

- a) The SPI interface timings have been modified to the values shown in Table 3.

TABLE 4: DC SPECIFICATION CHANGES FROM DATA SHEET

| Parm No. | Sym. | Characteristic | New Specification | | | Data Sheet Specification | | | Units | |
|----------|------------------|--|-----------------------------|------------------------------|-----|--------------------------|-------------------------|-----|-------|----|
| | | | Min | Typ | Max | Min | Typ | Max | | |
| 71 | Tsch | SCK input high time (slave mode) | Continuous | 1.25 T _{CY} + 30 ns | — | — | T _{CY} + 20 ns | — | — | ns |
| 71A | | | Single Byte ⁽¹⁾ | 40 | — | — | N.A. | | | ns |
| 72 | TscL | SCK input low time (slave mode) | Continuous | 1.25 T _{CY} + 30 ns | — | — | T _{CY} + 20 ns | — | — | ns |
| 72A | | | Single Byte ⁽¹⁾ | 40 | — | — | N.A. | | | ns |
| 73A | T _{B2B} | Last clock edge of the Byte1 to 1st clock edge of the Byte2 ⁽¹⁾ | 1.5 T _{CY} + 40 ns | — | — | N.A. | | | ns | |

* This parameter is characterized but not tested

Note 1: Specification 73A is only required if specifications 71A and 72A are used.

4. Module: Timer1

- a) The operation of Timer1 needs some clarification when the timer registers are written when the TMR1ON bit is set.

The internal clock signal that is the input to the TMR1 prescaler affects the incrementing of Timer1 (TMR1H:TMR1L registers and the Timer1 prescaler). When the Timer1 registers are NOT written, the Timer1 will increment on the rising edge of the TMR1 increment clock.

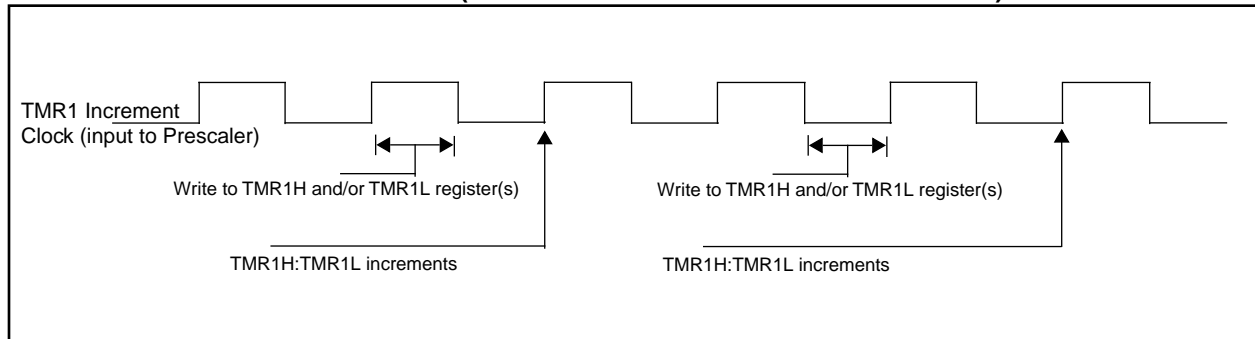
When the TMR1H and/or TMR1L registers are written while this clock is high, TMR1 will increment on the next rising edge of this clock.

When the TMR1H and/or TMR1L registers are written while this clock is low, TMR1 will not increment on the next rising edge of this clock, but must first have a falling clock and the rising clock for TMR1 to increment.

Figure 1 shows the two cases of writes to the TMR1H and/or TMR1L registers. Due to the V_{IH} and V_{IL} thresholds on the oscillator/clock pins, external Timer1 oscillator components, and external clock frequency, the Timer1 increment clock may not be of a 50% duty cycle.

The TMR1 increment clock is out of phase of the T1OSO/T1CKI pin by a small propagation delay.

FIGURE 1: WRITES TO TIMER1 (EXTERNAL CLOCK / OSCILLATOR MODE)





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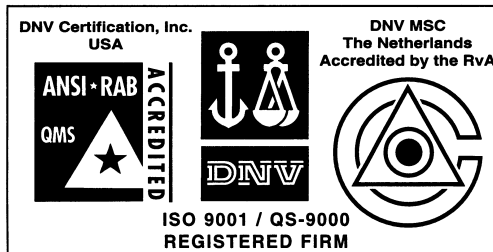
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