PIC16CR83

PIC16CR83 Rev. A Silicon Errata Sheet

The PIC16CR83 (Rev. A) parts you have received conform functionally to the Device Data Sheet (DS30081**F**), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC16CR83 silicon.

1. Module: CPU (STATUS bit)

The operation of the power-down ($\overline{PD}$) bit in the STATUS register may not function correctly for temperatures below - 20 ˚C.

Work Around

None

2. Module: Data EEPROM

Do not perform a modify (set or clear a bit) of the EECON1 register one instruction cycle after an EEPROM read. This will corrupt the EEDATA register.

Example:

```
BSF   EECON1, RD
BCF   EECON1, WREN
```

Work Around

Use either of the following two code segment in place of the above example.

```
BSF   EECON1, RD
NOP
BCF   EECON1, WREN
```

or

```
BCF   EECON1, WREN
BSF   EECON1, RD
```

3. Module: Timer0

The TMR0 register may increment when the WDT postscaler is switched to the Timer0 prescaler. If TMR0 = FFh, this will cause TMR0 to overflow (setting T0IF).

Work Around

Follow the following sequence:

a) Read the 8-bit TMR0 register into the W register
b) Clear the TMR0 register
c) Assign WDT postscaler to Timer0
d) Write W register to TMR0

Note: As with any windowed EPROM device, please cover the window at all times, except when erasing.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS30081**F**), the following clarifications and corrections should be noted.

1. Module: Data EEPROM

In the PIC16F8X Data Sheet (DS30430**B**), the following clarifications and corrections should be noted.

a) Erase/Write Cycle Time for Data EEPROM should be changed from 10 ms maximum to 20 ms maximum, as shown in Table 1.

TABLE 1: DC SPECIFICATION LIMITS THAT VARY FROM DATA SHEET

Parameter No.	Sym.	Characteristic	Actual Data		Data Sheet		Units
			Typ	Max	Typ	Max	
D122	TDEW	Erase Write Cycle Time	10	20 *	—	10	ms

* This parameter is characterized but not tested

2. Module: Device Idd

a) The maximum device IDD in the LP oscillaor mode (at 32KHz, 2.0 V, and WDT disabled) should be changed from 32 µA maximum to 45 µA maximum, as shown in Table 1.

TABLE 2: DC SPECIFICATION LIMITS THAT VARY FROM DATA SHEET

Parameter No.	Sym.	Characteristic	Actual Data		Data Sheet		Units
			Typ	Max	Typ	Max	
D014	IDD	Supply Current	15	45	15	32	µA

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