



JEDEC
SOLID STATE PRODUCT
OUTLINES

THIS REGISTERED OUTLINE HAS BEEN PREPARED BY THE JEDEC JC-11
COMMITTEE AND REFLECTS A PRODUCT WITH ANTICIPATED USAGE IN
THE ELECTRONICS INDUSTRY : CHANGES ARE LIKELY TO OCCUR

TITLE
SMALL OUTLINE
TRANSISTOR (SOT)
PLASTIC PACKAGE

JESD-30 DESIGNATOR
R-PDSO-G

ISSUE
A

DATE
OCT
1995

ITEM
MO-178

SHEET
1 OF 2

SYMBOL	VARIATIONS (ALL DIMENSIONS SHOWN IN MILLIMETERS)											
	AA			NOTE	AB			NOTE	AC			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	0.95	-	1.45									
A1	0.05	-	0.15									
A2	0.90	1.15	1.30									
b	0.35	-	0.50	8								
b1	0.35	0.40	0.45	8								
c	0.08	-	0.20	8								
c1	0.08	0.10	0.15	8								
D	2.80	2.90	3.00	3,5								
E	2.60	2.80	3.00									
E1	1.50	1.60	1.70	4,5								
L	0.35	0.45	0.55									
L1	0.20 BSC											
e	0.95 BSC											
e1	1.90 BSC											
N	5			7								
α	0°	5°	10°									
NOTE	1, 2											
REF.	10-355											
ISSUE	A											

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M - 1982.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER SIDE.
4. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.
5. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PACKAGE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND THE BOTTOM OF THE MOLDED BODY. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM PLANE -H-.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08MM AND 0.15MM FROM THE LEAD TIP.

JEDEC SOLID STATE PRODUCT OUTLINES	TITLE SMALL OUTLINE TRANSISTOR (SOT) PKG R-PDSO-G	ISSUE A	DATE OCT 1995	ITEM MO-178	SHEET 2 OF 2
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