1998 Annual Reliability Report (compiled 7/99)

INTRODUCTION

"Quality Comes First"

By adhering to this guiding value, Microchip Technology Inc. has achieved competitive leadership in quality and reliability for its products. Demonstrated performance levels of less than 100 Failures in Time (FITS) for most products have been realized through the design-in of reliability and continued use of reliability monitors.

This report details Microchip's quality and reliability systems as well as presenting data on the results of these systems. It includes the following:

- Reliability Control System
- Failure Calculation Methodology
- Reliability Test Descriptions
- 1999 Product Reliability

RELIABILITY CONTROL SYSTEM

A comprehensive qualification system is employed to ensure that released products are designed, processed, packaged, and tested to meet both design functionality and reliability objectives. Once qualified, a reliability monitor system ensures that wafer fabrication and assembly process performance is stable over time. A set of baseline specifications is maintained that states which changes require requalification. These process changes can only be made after successful demonstration of reliability performance. This system results in reliable field performance, while enabling the smooth phase-in of improved designs and product capability. The system is diagrammed in Table 1.

TABLE 1: RELIABILITY CONTROL SYSTEM DIAGRAM

DESIGN AND DEVELOPMENT	QUALIFICATION	RELIABILITY CONTROL
Specify: • Design objectives/ specifications • Testability goals • Reliability requirements • Process/packaging requirements • Design guidelines **Design:** • Functional models • Logic design and verification • Circuit design and verification • Layout design and verification • Prototype verification • Performance characterization **Develop (as required):** • Wafer fabrication processes • Package/packaging technology	**Confirm Design Objectives Using Qualification Tests:** • Dynamic life, 125°C ambient • Temp-cycle, -65°/150°C • Thermal shock, -55°/125°C • ESD, volts HBM ± 4000 • ESD, volts MM ±400 • Latch-up (CMOS devices) • HAST 130°C/85% RH • Autoclave (pressure cooker) • Retention bake,150°C ambient	**Assure Outgoing Quality Level:** • Design release document • Baseline wafer fabrication process • Baseline assembly process • Qualification release • Enter device to specification system • Wafer-level reliability controls • Assembly reliability controls • Early failure rate sampling • Reliability monitoring • Statistical process control feedback • Audit specifications • Analyze returned failures • Requalify devices as needed for major changes such as ESD resistance enhancement, cost reduction/die shrink, process improvement and new package types

FAILURE RATE CALCULATION

FIT (Failure in Time): Expresses the estimated field failure rate in number of failures per billion device hours. 100 FITS equals 0.01% fail per 1,000 device hours.

Extended field life is simulated by using high ambient temperature. In the semiconductor industry, high temperatures dramatically accelerate the mechanisms leading to component failure. Using performance results at different temperatures, an activation energy is determined using the Arrhenius Equation. For each type of failure mechanism, the activation energy expresses the degree to which temperature increases the failure rate.

The activation energy values determined by Microchip agree closely with those published in the literature. For complex CMOS devices in production at Microchip, an activation energy of 0.6 eV has been shown to be representative of typical failures on operating life. By definition, failure is reached when a device no longer meets the data sheet specifications as a direct result of the reliability test environment to which it was exposed. Common failure modes for CMOS integrated circuits are identified for each test environment.

To establish a field failure rate, an acceleration factor is applied to the device operating hours observed at high temperature stress and extrapolated to a failure rate at 55°C ambient temperature in still air.

The actual failure rate experienced could be considerably less than that calculated if lower device temperatures occur in the application board, such as would be the case if a fan, a heat sink or air flow by convection is used.

Environment	Attribute Tested
Dynamic Life	Process parameter drift/shift
	Metal electromigration
	Internal leakage path
	Data retention
	Bond/ball bond integrity
Temperature Cycle	Bond/ball integrity
	Die or surface integrity
	Bond pad integrity
Biased-Humidity	Internal device leakage
	Corrosion resistance
PCT	Inter-pin leakage
	Data retention
	Corrosion resistance
High Temp. Bake	Data retention

RELIABILITY TEST DESCRIPTIONS

High Temperature (125°C) Dynamic Life Test

High temperature dynamic life testing accelerates random failure modes which could occur in user applications. Voltage bias and address signals are used to exercise the device in a manner similar to user systems. The voltage maintained during the tests is at or near the maximum data sheet voltage supply. Derating from high temperature, an ambient use condition failure rate can be calculated. The extrapolation of data for FIT rate purposes of this test does not include electrical acceleration.

Temperature Cycle

The devices are exposed to severe extremes of temperature in an alternating fashion (-65°C for 10 minutes, 150°C for 10 minutes per cycle). Package strength, bond quality and consistency of assembly process are stressed using this environment.

PCT (Pressure Cooker or Autoclave)

Using a pressure of one atmosphere above atmospheric pressure, plastic packaged devices are exposed to moisture at 121°C. The pressure forces moisture permeation of the package and accelerates related failure mechanisms, if present, on the device.

Thermal Shock

Exposes devices to extreme temperatures from -55°C to +125°C by alternate immersion in liquid media. This is a sudden temperature change, as opposed to the gradual change in the Temperature Cycling test. Otherwise, it induces the same stresses as Temperature Cycling.

Data Retention Bake

A 150°C temperature stress is used to accelerate charge loss in the memory cell and measure the data retention on the EPROM and EEPROM portions of the circuitry.

Data storage in applicable devices is done by developing a charge on the floating gate structure in the memory cell. Charge loss in this cell structure results in a conversion of data states. In order to evaluate the level of this type of failure, devices are subjected to a 150°C bake. This bake accelerates charge loss in the memory cell and 1000 hours at 150°C is equivalent to greater than 25 years in the field at 55°C.

Highly Accelerated Stress Test (HAST)

Moisture, extreme heat and bias are used to accelerate corrosion and contamination in plastic packages. The conditions are 130°C and 85% relative humidity. Typical bias voltage is +5 V and ground on alternating pins.

Erase/Write Endurance of EEPROMs

Measurement of Cycling

Microchip defines a device lifetime in the strictest sense, that is, stated lifetime has to exhibit the truest correlation to customer results. An endurance failure is determined when any one bit in the array is not capable of being correctly written and maintained in that state indefinitely.

The device lifetime is defined when a specified percentage of devices (Microchip currently uses a cumulative 2.5 percent) have a customer detectable error under worst case operating conditions.

Ongoing monitors are acquired from wafer lots of material manufactured for shipment. Samples are subjected to page cycling of an alternating checkerboard and inverse checkerboard pattern at 85°C in rapid succession to a specified number of cycles. These units then are baked at 150°C for 48 hours in both checkerboard and inverse checkerboard states and electrically tested to ensure that data sheet requirements are met. This data is accumulated on a regular basis and reviewed to measure both results of continuous improvement programs and conformance to the device standards.

Endurance Variables

a) **Temperature:** Within the FLOTOX technology, temperature has an inverse effect on the endurance of a EEPROM device. The activation energy of these cycling failures is approximately 0.15 eV. The long term trap up portion of the curve is worsened by temperature to a greater extent than the early fails due to the difficult failure mechanisms that are activated.

b) **Delay Between Cycles:** This has been reported in the industry as having an enhanced effect on the lifetime of EEPROM devices. For some technologies, this does have a positive effect; however, this is not strictly the case for FLOTOX manufacturers. While the second failure rate increase period (associated with end of life) may be impacted by this due to a decreased rate of electron trapping, the first failure rate is actually not impacted by this variable.

c) **Write Timing:** The decrease in write time to the device correlates directly with the write/erase cycling failure rate of the device. This shorter pulse reduces the cell time at voltage which then provides an enhanced life prior to the occurrence of a time dependent oxide breakdown. It also passes fewer electrons through the oxide providing less potential trapping possibilities while maintaining adequate margins for the written state.

Note: The rise time of the signal, which the customer does not have control over, is also a dominant effect.

d) **VCC Voltage:** The higher voltages generate higher fields within the device. This causes more stress which is offset by the operational increase of internal timers and actually shortens the write time of the device.

Lower voltages have the opposite effect on the individual parameters except in cycles obviously where the write timer is externally controlled. This overall effect is minor compared to the others in magnitude on the failure rate curve and is variable over the customer operating range with a maximum at VCC = 5.5 V.

e) **Pattern Effect:** The pattern that is programmed in the device does play a first order role in the overall lifetime. The act of programming a nonvolatile memory inflicts damage on the device that cannot be repaired. This damage is the result of exposure to high electric fields which over a period of time either breakdown or trap up the effected oxide causing failures. The act of writing a cell from a one to a zero provides the maximum amount of stress by exercising the charge pump and passing electrons through the tunnel dielectric.

Note: To write a zero even from a zero state causes an automatic byte erase prior to the write converting the bit to a one and returning it to its original state!

Conversely writing a one from a one then passes no charge through the cell and, therefore, does no damage to the cell but does stress the charge pump.

From an array standpoint, this would allow a checkerboard/ inverse checkerboard patterned device to endure twice the number of write cycles of an all zero patterned device. In general, this appears to be approximately correct but does neglect the charge pump and other peripheral wear-out mechanisms.

Cycling Mode: Three modes exist in Microchip devices that are primarily used for endurance evaluations. The byte write mode (one single byte written at a time) is the standard mode used by the customer in the field as well as the method of monitoring that has been chosen internally. This is to best estimate field lifetime expectations and actual failure rates. A second technique exists called block mode which exercises all the cells of the array simultaneously. The failure rates of byte cycled devices are approximately two times the failure rates of block cycled devices according to experimental test data. This effect has been traced back to the rise time of the programming signal at the memory cell. The faster this voltage rise occurs, the more damage occurs and the shorter the lifetime. The block mode has a much slower rise time given the entire array being utilized provides a much larger resistive/capacitive load which slows the signal rise ultimately resulting in the greater lifetime. Please note that the page mode which can be utilized by the customers falls between the block and byte modes with respect to failure rate.

f) **Array Size:** This effect is a direct result of how fast most devices will fail due to a single bit not working simply due to the number of bits involved. This is not exactly double the failure rate with a doubling of the memory size since some circuits fail within the charge pump or decoding circuitry sections and are, therefore, not directly related to array size.

Field Results

After significant experimentation, Microchip has developed a model of the endurance failure rates as a function of all the variables listed above. This model is available to the customer in the form of a diskette called Total Endurance™. The Total Endurance Software Model allows the customer to bypass confusing information and conditions other than their application and directly predict the failure rate in their application conditions within a few percent. This also allows the customer to adjust operating parameters and immediately evaluate the impact on the results of the final system.

RELIABILITY DATA SUMMARY

The following section provides a reliability summary of Microchip's product. Included is reliability data and packaging information obtained during 1998.

SUMMARY OF RELIABILITY – 1998 ANNUAL REPORT DEVICE DATA

I. DYNAMIC LIFE/ RETENTION BAKE

Dynamic Life

Stress Temperature:	125°C	Activation Energy:	0.6	eV	77K
Derated Temperature:	55°C	Acceleration Rate:	42		
		Activation Energy:	0.7	eV	90K, 120K
		Acceleration Rate:	78		

Retention Bake

Stress Temperature:	150°C	Activation Energy:	1.2	eV	77K, 90K and 120K
Derated Temperature:	55°C	Acceleration Rate:	13718		

Microcontrollers						**Fit rates, 60% Confidence Level**		
Device	**Operation**	**168 Hrs.**	**1008 Hrs.**	**Fails**	**Device Hrs.**	**Infant Mortality**	**Long Term Life**	**Total Life**
ALL PICS	Dynamic Life	5/22735	2/10483	7	12,625,200	25	5	10
	Retention Bake	4/29313	0/6945	4	10,758,384	<1	<1	<1
ALL 90k PICS	Dynamic Life	4/16161	1/7425	5	8,952,048	25	4	9
	Retention Bake	4/23615	0/5488	4	8,577,240	<1	<1	<1
ALL 77k PICS	Dynamic Life	1/6574	1/3058	2	3,673,152	44	19	20
	Retention Bake	0/5698	0/1457	0	2,181,144	<1	<1	<1
PIC16C924	Dynamic Life	0/1478	0/660	0	802,704	48	21	15
	Retention Bake	0/1857	0/425	0	668,976	<1	<1	<1
PIC16C622	Dynamic Life	0/689	0/380	0	434,952	102	37	27
	Retention Bake	0/2364	0/549	0	858,312	<1	<1	<1
PIC16C84A	Dynamic Life	0/1900	0/760	0	957,600	69	34	23
	Retention Bake	0/0	0/0	0	0	N/A	N/A	N/A
PIC16C74A	Dynamic Life	0/1759	0/810	0	975,912	40	17	12
	Retention Bake	0/2648	0/716	0	1,046,304	<1	<1	<1
PIC16C72	Dynamic Life	0/1626	0/572	0	753,648	43	25	16
	Retention Bake	0/2532	0/512	0	855,456	<1	<1	<1
PIC16C66/67/68	Dynamic Life	4/2599	1/1218	5	1,459,752	154	25	56
	Retention Bake	4/3737	0/858	4	1,348,536	1	<1	<1
PIC16C63/65A	Dynamic Life	0/2341	0/972	0	1,209,768	30	14	10
	Retention Bake	0/3139	0/614	0	1,043,112	<1	<1	<1
PIC16C62A/64A	Dynamic Life	0/1620	0/648	0	816,480	43	22	14
	Retention Bake	0/1946	0/405	0	667,128	<1	<1	<1
PIC16C58A	Dynamic Life	0/1365	0/760	0	867,720	51	18	14
	Retention Bake	0/2842	0/545	0	935,256	<1	<1	<1
PIC16C57	Dynamic Life	0/403	0/208	0	242,424	325	126	91
	Retention Bake	0/512	0/112	0	180,096	1	1	<1
PIC16C54	Dynamic Life	1/4271	1/2090	2	2,473,128	68	28	30
	Retention Bake	0/5186	0/1345	0	2,001,048	<1	<1	<1
PIC17C44	Dynamic Life	0/1947	0/808	0	1,005,816	36	17	12
	Retention Bake	0/1666	0/632	0	810,768	<1	<1	<1
PIC12C508	Dynamic Life	0/737	0/597	0	625,296	95	24	19
	Retention Bake	0/884	0/232	0	343,392	<1	<1	<1

Microcontrollers (Continued)		**Fit rates, 60% Confidence Level**
Failure Modes:	Dynamic Life	3 units of PIC16C67 failed for high sleep current due to oxide breakdown
		1 unit of PIC16C54 failed due to single bit charge loss
		1 unit of PIC16C54 failed a bit column
		1 unit of PIC16C67 failed core functional tests
		1 unit of PIC16C67 failed due to single SRAM bit retention
	Retention Bake	3 units of PIC16C67 failed for high sleep current due to oxide breakdown
		1 unit of PIC16C77 failed for high sleep current due to oxide breakdown

Serial EEPROMs — **Fit rates, 60% Confidence Level**

Device	Operation	168 Hrs.	1008 Hrs.	Fails	Device Hrs.	Infant Mortality	Long Term Life	Total Life
ALL SERIAL	Dynamic Life	6/46624	16/20031	20	24,658,872	16	25	21
EEPROMS	Retention Bake	14/59135	8/13075	22	20,917,680	<1	<1	<1
77k SERIAL	Dynamic Life	4/44272	15/19071	19	23,457,336	17	25	21
EEPROMS	Retention Bake	10/58169	1/12863	11	20,577,312	<1	<1	<1
121k SERIAL	Dynamic Life	0/2352	1/960	1	1,201,536	30	32	22
EEPROMS	Retention Bake	4/966	7/212	11	340,368	2	3	3
93LC46	Dynamic Life	0/3514	0/1473	0	1,827,672	37	18	12
	Retention Bake	6/9124	0/2100	6	3,296,832	<1	<1	<1
93LC56/66	Dynamic Life	0/7927	0/3460	0	4,238,136	17	8	5
	Retention Bake	2/13094	1/2852	3	4,595,472	<1	<1	<1
93LC86	Dynamic Life	0/2306	0/980	0	1,210,608	57	27	18
	Retention Bake	0/2028	0/448	0	717,024	<1	<1	<1
24LC01B	Dynamic Life	0/1970	0/900	0	1,086,960	66	29	20
	Retention Bake	0/2536	0/540	0	879,648	<1	<1	<1
24LC02B	Dynamic Life	0/5462	12/2320	12	2,866,416	24	167	114
	Retention Bake	0/7623	0/1647	0	2,664,144	<1	<1	<1
24LC04B	Dynamic Life	0/5482	0/2398	0	2,935,296	24	11	7
	Retention Bake	0/5070	0/1108	0	1,782,480	<1	<1	<1
24LC08B	Dynamic Life	0/1183	0/520	0	635,544	111	50	35
	Retention Bake	1/1536	0/332	1	536,928	1	<1	<1
24LC16B	Dynamic Life	0/5880	1/2580	1	3,155,040	22	22	15
	Retention Bake	1/7129	0/1648	1	2,581,992	<1	<1	<1
24LC32A	Dynamic Life	3/1945	0/800	3	998,760	307	33	100
	Retention Bake	0/3985	0/904	0	1,428,840	<1	<1	<1
24LC64	Dynamic Life	0/388	0/160	0	199,584	337	164	110
	Retention Bake	0/0	0/0	0	0	N/A	N/A	N/A
24LCS21	Dynamic Life	1/6646	0/2840	1	3,502,128	43	9	14
	Retention Bake	0/4042	0/884	0	1,421,616	<1	<1	<1
24LCS52	Dynamic Life	0/1957	2/800	2	1,000,776	67	111	74
	Retention Bake	0/2002	0/400	0	672,336	<1	<1	<1
24LC128	Dynamic Life	0/773	1/320	1	398,664	91	97	65
	Retention Bake	4/966	7/212	11	340,368	2	3	3

Serial EEPROMs (Continued)						**Fit rates, 60% Confidence Level**		
Device	**Operation**	**168 Hrs.**	**1008 Hrs.**	**Fails**	**Device Hrs.**	**Infant Mortality**	**Long Term Life**	**Total Life**
25LC08/16/162	Dynamic Life	0/1191	0/480	0	603,288	110	55	36
	Retention Bake	0/0	0/0	0	0	N/A	N/A	N/A
Failure Modes:	Dynamic Life	1 unit of 24LC16B failed for high standby current due to oxide breakdown 1 unit of 24LCS21A failed to program 1 unit of 24LCS52 failed for high Idds due to oxide breakdown 1 unit of 24LCS52 failed to program due to a blown charge pump 1 unit of 24LC128 failed to erase a byte column 3 units of 24LC32A failed due to single bit charge loss 12 units of 24LC02B failed to function in page mode						
	Retention Bake	1 unit of 24LC16B failed a single byte due to oxide breakdown 6 units of 93LC46 failed due to single bit charge loss 3 units of 93LC66B failed due to single bit charge loss 1 unit of 24LC08B failed to program due to a charge pump failure 7 units of 24LC128 failed due to single bit charge loss 2 units of 24LC128 failed due to voided vias 1 unit of 24LC128 failed due to oxide breakdown 1 unit of 24LC128 failed due to high static Idd due to oxide breakdown						

Parallel EEPROMs						**Fit rates, 60% Confidence Level**		
Device	**Operation**	**168 Hrs.**	**1008 Hrs.**	**Fails**	**Device Hrs.**	**Infant Mortality**	**Long Term Life**	**Total Life**
ALL PARALLEL	Dynamic Life	0/1226	0/992	0	1,039,248	107	26	21
EEPROMS	Retention Bake	0/2462	2/500	2	833,616	<1	1	<1
28C64	Dynamic Life	0/1226	0/992	0	1,039,248	107	26	21
	Retention Bake	0/2462	2/500	2	833,616	<1	1	<1
Failure Modes:	Dynamic Life	N/A						
	Retention Bake	2 units of 28C64A failed due to single bit charge loss						

EPROMs						**Fit rates, 60% Confidence Level**		
Device	**Operation**	**168 Hrs.**	**1008 Hrs.**	**Fails**	**Device Hrs.**	**Infant Mortality**	**Long Term Life**	**Total Life**
ALL EPROMS	Dynamic Life	4/1648	0/673	4	842,184	377	31	121
	Retention Bake	0/1939	0/400	0	661,752	<1	<1	<1
ALL 90k EPROMS	Dynamic Life	4/392	0/193	4	227,976	1024	73	296
	Retention Bake	0/473	0/100	0	163,464	1	1	<1
ALL 77k EPROMS	Dynamic Life	0/1256	0/480	0	614,208	104	55	36
	Retention Bake	0/1466	0/300	0	498,288	<1	<1	<1
27C256	Dynamic Life	0/1256	0/480	0	614,208	104	55	36
	Retention Bake	0/1466	0/300	0	498,288	<1	<1	<1
27C512A	Dynamic Life	4/392	0/193	4	227,976	1024	73	296
	Retention Bake	0/473	0/100	0	163,464	1	1	<1
Failure Modes:	Dynamic Life	4 units of 27C512A failed due to single bit charge loss						
	Retention Bake	N/A						

Secure Data Products						**Fit rates, 60% Confidence Level**		
Device	**Operation**	**168 Hrs.**	**1008 Hrs.**	**Fails**	**Device Hrs.**	**Infant Mortality**	**Long Term Life**	**Total Life**
ALL SECURE DATA PRODUCTS	Dynamic Life	0/1152	0/1152	0	1,161,216	114	23	19
	Retention Bake	0/0	0/0	0	0	N/A	N/A	N/A
HCS301	Dynamic Life	0/768	0/768	0	774,144	170	34	28
	Retention Bake	0/0	0/0	0	0	N/A	N/A	N/A
HCS360	Dynamic Life	0/384	0/384	0	387,072	341	68	57
	Retention Bake	0/0	0/0	0	0	N/A	N/A	N/A
Failure Modes:	Dynamic Life	N/A						
	Retention Bake	N/A						

II. PRESSURE COOKER, HAST, TEMPERATURE CYCLE, AND THERMAL SHOCK PACKAGE DATA SUMMARY

Pressure Cooker

Stress Temperature:	121.5°C	Activation Energy:	0.6 eV
Derated Temperature:	55°C	Acceleration Rate:	36

HAST

Stress Temperature:	130°C	Activation Energy:	0.6 eV
Derated Temperature:	55°C	Acceleration Rate:	52

Operation	Package	24 Hrs.	168 Hrs.	Fails	Device Hrs.	% fails per 1000 hrs.
Pressure Cooker	ALL PACKAGES	0/34136	51/34079	51	5,726,640	0.902
Pressure Cooker	MQFP	0/2650	0/2646	0	444,624	0.156
Pressure Cooker	PDIP	0/12754	29/12752	29	2,142,384	1.385
Pressure Cooker	PLCC	0/3200	1/3195	1	536,880	0.313
Pressure Cooker	SOIC	0/15282	21/15236	21	2,560,752	0.846
Pressure Cooker	SOT	0/150	0/150	0	25,200	2.751
Pressure Cooker	TSOP	0/100	0/100	0	16,800	4.126
Failure Modes:	1 unit of 8L SOIC (24LC65) failed due to single byte data disturb 1 unit of 8L TSSOP (24LCS52) failed to program due to a decode failure 8 units of 28L PDIP (PIC16C57) failed due to metal corrosion 13 units of 28L PDIP (PIC16C55) failed due to moisture penetration 1 unit of 8L PDIP (93LC86) failed for high static Idd due to oxide breakdown 1 unit of 8L PDIP (93LC86) failed for high static Idd due to moisture penetration of passivation cracks 1 unit of 8L PDIP (24LC01B) failed due to leakage 5 units of 18L PDIP (PIC16C622A) failed due to via voids 1 unit of 32L PLCC (28C64A) failed due to a fractured wire bond 1 unit of 8L TSSOP (24LCS52) failed due to moisture penetration 1 unit of 8L SOIC (24LCS52) failed due to wire sweep 13 units of 8L SOIC (24LC04B) failed to function due to moisture penetration of passivation cracks 2 units of 28L SSOP (PIC16C57) failed due to moisture penetration 2 units of 8L TSSOP (24LCS52) failed functionality					

Operation	Package	24 Hrs.	168 Hrs.	Fails	Device Hrs.	% fails per 1000 hrs.
HAST	ALL PACKAGES	2/21797	8/21711	10	3,651,576	0.292
HAST	MQFP	0/1618	0/1596	0	268,656	0.258
HAST	PDIP	0/8199	0/8196	0	1,377,072	0.05
HAST	PLCC	0/1889	0/1889	0	317,352	0.218
HAST	SOIC	2/9677	8/9617	10	1,618,536	0.659
HAST	SOT	0/90	0/90	0	15,120	4.584
HAST	TSOP	0/324	0/323	0	54,312	1.276
Failure Modes:	8 units of 8L SOIC (93LC46B) failed due to delamination 2 units of 8L SOIC (93LC46B) failed due to bond pad corrosion					

Operation	Package	50 Cyc.	100 Cyc.	Fails
Temp. Cycles	ALL PACKAGES	0/10	1/6822	1
Temp. Cycles	MQFP	0/0	0/500	0
Temp. Cycles	PDIP	0/0	0/2746	0
Temp. Cycles	PLCC	0/0	0/540	0
Temp. Cycles	SOIC	0/0	1/2996	1
Temp. Cycles	SOT	0/10	0/30	0
Temp. Cycles	TSOP	0/0	0/10	0
Failure Modes:	1 unit of 18L SOIC (PIC16C54A) failed functionality at Vddhi			

Operation	Package	100 Cyc.	500 Cyc.	Fails
Thermal Shock	ALL PACKAGES	0/7087	0/10	0
Thermal Shock	MQFP	0/500	0/0	0
Thermal Shock	PDIP	0/2846	0/0	0
Thermal Shock	PLCC	0/580	0/0	0
Thermal Shock	SOIC	0/3121	0/0	0
Thermal Shock	SOT	0/30	0/10	0
Thermal Shock	TSOP	0/10	0/0	0
Failure Modes:	N/A			

NOTES:

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

Microchip Technology Inc.
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 602-786-7200 Fax: 602-786-7277
Technical Support: 602-786-7627
Web Address: http://www.microchip.com

After September 1, 1999:
Tel: 480-786-7200 Fax: 480-786-7277
Technical Support: 480-786-7627

Atlanta

Microchip Technology Inc.
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Boston

Microchip Technology Inc.
5 Mount Royal Avenue
Marlborough, MA 01752
Tel: 508-480-9990 Fax: 508-480-8575

Chicago

Microchip Technology Inc.
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas

Microchip Technology Inc.
4570 Westgrove Drive, Suite 160
Addison, TX 75248
Tel: 972-818-7423 Fax: 972-818-2924

Dayton

Microchip Technology Inc.
Two Prestige Place, Suite 150
Miamisburg, OH 45342
Tel: 937-291-1654 Fax: 937-291-9175

Detroit

Microchip Technology Inc.
Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Los Angeles

Microchip Technology Inc.
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

New York

Microchip Technology Inc.
150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 516-273-5305 Fax: 516-273-5335

San Jose

Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

AMERICAS (continued)

Toronto

Microchip Technology Inc.
5925 Airport Road, Suite 200
Mississauga, Ontario L4V 1W1, Canada
Tel: 905-405-6279 Fax: 905-405-6253

ASIA/PACIFIC

Hong Kong

Microchip Asia Pacific
Unit 2101, Tower 2
Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2-401-1200 Fax: 852-2-401-3431

Beijing

Microchip Technology, Beijing
Unit 915, 6 Chaoyangmen Bei Dajie
Dong Erhuan Road, Dongcheng District
New China Hong Kong Manhattan Building
Beijing 100027 PRC
Tel: 86-10-85282100 Fax: 86-10-85282104

India

Microchip Technology Inc.
India Liaison Office
No. 6, Legacy, Convent Road
Bangalore 560 025, India
Tel: 91-80-229-0061 Fax: 91-80-229-0062

Japan

Microchip Technology Intl. Inc.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa 222-0033 Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea

Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Shanghai

Microchip Technology
RM 406 Shanghai Golden Bridge Bldg.
2077 Yan'an Road West, Hong Qiao District
Shanghai, PRC 200335
Tel: 86-21-6275-5700 Fax: 86 21-6275-5060

ASIA/PACIFIC (continued)

Singapore

Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan, R.O.C

Microchip Technology Taiwan
10F-1C 207
Tung Hua North Road
Taipei, Taiwan, ROC
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

United Kingdom

Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5858 Fax: 44-118 921-5835

Denmark

Microchip Technology Denmark ApS
Regus Business Centre
Lautrup hoj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France

Arizona Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - ler Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany

Arizona Microchip Technology GmbH
Gustav-Heinemann-Ring 125
D-81739 München, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy

Arizona Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-39-65791-1 Fax: 39-39-6899883

08/11/99

ISO 9001 REGISTERED FIRM

Microchip received ISO 9001 Quality System certification for its worldwide headquarters, design, and wafer fabrication facilities in January 1997. Our field-programmable PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, related specialty memory products and development systems conform to the stringent quality standards of the International Standard Organization (ISO).