1999 Annual Reliability Report (compiled 7/00)

INTRODUCTION

"Quality Comes First"

By adhering to this guiding value, Microchip Technology Inc. has achieved competitive leadership in quality and reliability for its products. Demonstrated performance levels of less than 100 Failures in Time (FITS) for most products have been realized through the design-in of reliability and continued use of reliability monitors.

This report details Microchip's quality and reliability systems as well as presenting data on the results of these systems. It includes the following:

- Reliability Control System
- Failure Calculation Methodology
- Reliability Test Descriptions
- 1999 Product Reliability

RELIABILITY CONTROL SYSTEM

A comprehensive qualification system is employed to ensure that released products are designed, processed, packaged, and tested to meet both design functionality and reliability objectives. Once qualified, a reliability monitor system ensures that wafer fabrication and assembly process performance is stable over time. A set of baseline specifications is maintained that states which changes require requalification. These process changes can only be made after successful demonstration of reliability performance. This system results in reliable field performance, while enabling the smooth phase-in of improved designs and product capability. The system is diagrammed in Table 1.

TABLE 1: RELIABILITY CONTROL SYSTEM DIAGRAM

DESIGN AND DEVELOPMENT	QUALIFICATION	RELIABILITY CONTROL
Specify: • Design objectives/ specifications • Testability goals • Reliability requirements • Process/packaging requirements • Design guidelines **Design:** • Functional models • Logic design and verification • Circuit design and verification • Layout design and verification • Prototype verification • Performance characterization **Develop (as required):** • Wafer fabrication processes • Package/packaging technology	**Confirm Design Objectives Using Qualification Tests:** • Dynamic life, 125°C ambient • Temp-cycle, -65°/150°C • Thermal shock, -55°/125°C • ESD, volts HBM ± 4000 • ESD, volts MM ±400 • Latch-up (CMOS devices) • HAST 130°C/85% RH • Autoclave (pressure cooker) • Retention bake,150°C ambient	**Assure Outgoing Quality Level:** • Design release document • Baseline wafer fabrication process • Baseline assembly process • Qualification release • Enter device to specification system • Wafer-level reliability controls • Assembly reliability controls • Early failure rate sampling • Reliability monitoring • Statistical process control feedback • Audit specifications • Analyze returned failures • Requalify devices as needed for major changes such as ESD resistance enhancement, cost reduction/die shrink, process improvement and new package types

FAILURE RATE CALCULATION

FIT (Failure in Time): Expresses the estimated field failure rate in number of failures per billion device hours. 100 FITS equals 0.01% fail per 1,000 device hours.

Extended field life is simulated by using high ambient temperature. In the semiconductor industry, high temperatures dramatically accelerate the mechanisms leading to component failure. Using performance results at different temperatures, an activation energy is determined using the Arrhenius Equation. For each type of failure mechanism, the activation energy expresses the degree to which temperature increases the failure rate.

The activation energy values determined by Microchip agree closely with those published in the literature. For complex CMOS devices in production at Microchip, an activation energy of 0.6 eV has been shown to be representative of typical failures on operating life. By definition, failure is reached when a device no longer meets the data sheet specifications as a direct result of the reliability test environment to which it was exposed. Common failure modes for CMOS integrated circuits are identified for each test environment.

To establish a field failure rate, an acceleration factor is applied to the device operating hours observed at high temperature stress and extrapolated to a failure rate at 55°C ambient temperature in still air.

The actual failure rate experienced could be considerably less than that calculated if lower device temperatures occur in the application board, such as would be the case if a fan, a heat sink or air flow by convection is used.

Environment	Attribute Tested
Dynamic Life	Process parameter drift/shift
	Metal electromigration
	Internal leakage path
	Data retention
	Bond/ball bond integrity
Temperature Cycle	Bond/ball integrity
	Die or surface integrity
	Bond pad integrity
Biased-Humidity	Internal device leakage
	Corrosion resistance
PCT	Inter-pin leakage
	Data retention
	Corrosion resistance
High Temp. Bake	Data retention

RELIABILITY TEST DESCRIPTIONS

High Temperature (125°C) Dynamic Life Test

High temperature dynamic life testing accelerates random failure modes which could occur in user applications. Voltage bias and address signals are used to exercise the device in a manner similar to user systems. The voltage maintained during the tests is at or near the maximum data sheet voltage supply. Derating from high temperature, an ambient use condition failure rate can be calculated. The extrapolation of data for FIT rate purposes of this test does not include electrical acceleration.

Temperature Cycle

The devices are exposed to severe extremes of temperature in an alternating fashion (-65°C for 10 minutes, 150°C for 10 minutes per cycle). Package strength, bond quality and consistency of assembly process are stressed using this environment.

PCT (Pressure Cooker or Autoclave)

Using a pressure of one atmosphere above atmospheric pressure, plastic packaged devices are exposed to moisture at 121°C. The pressure forces moisture permeation of the package and accelerates related failure mechanisms, if present, on the device.

Thermal Shock

Exposes devices to extreme temperatures from -55°C to +125°C by alternate immersion in liquid media. This is a sudden temperature change, as opposed to the gradual change in the Temperature Cycling test. Otherwise, it induces the same stresses as Temperature Cycling.

Data Retention Bake

A 150°C temperature stress is used to accelerate charge loss in the memory cell and measure the data retention on the EPROM and EEPROM portions of the circuitry.

Data storage in applicable devices is done by developing a charge on the floating gate structure in the memory cell. Charge loss in this cell structure results in a conversion of data states. In order to evaluate the level of this type of failure, devices are subjected to a 150°C bake. This bake accelerates charge loss in the memory cell and 1000 hours at 150°C is equivalent to greater than 25 years in the field at 55°C.

Highly Accelerated Stress Test (HAST)

Moisture, extreme heat and bias are used to accelerate corrosion and contamination in plastic packages. The conditions are 130°C and 85% relative humidity. Typical bias voltage is +5 V and ground on alternating pins.

Erase/Write Endurance of EEPROMs

Measurement of Cycling

Microchip defines a device lifetime in the strictest sense, that is, stated lifetime has to exhibit the truest correlation to customer results. An endurance failure is determined when any one bit in the array is not capable of being correctly written and maintained in that state indefinitely.

The device lifetime is defined when a specified percentage of devices (Microchip currently uses a cumulative 2.5 percent) have a customer detectable error under worst case operating conditions.

Ongoing monitors are acquired from wafer lots of material manufactured for shipment. Samples are subjected to page cycling of an alternating checkerboard and inverse checkerboard pattern at 85°C in rapid succession to a specified number of cycles. These units then are baked at 150°C for 48 hours in both checkerboard and inverse checkerboard states and electrically tested to ensure that data sheet requirements are met. This data is accumulated on a regular basis and reviewed to measure both results of continuous improvement programs and conformance to the device standards.

Endurance Variables

a) **Temperature:** Within the FLOTOX technology, temperature has an inverse effect on the endurance of a EEPROM device. The activation energy of these cycling failures is approximately 0.15 eV. The long term trap up portion of the curve is worsened by temperature to a greater extent than the early fails due to the difficult failure mechanisms that are activated.

b) **Delay Between Cycles:** This has been reported in the industry as having an enhanced effect on the lifetime of EEPROM devices. For some technologies, this does have a positive effect; however, this is not strictly the case for FLOTOX manufacturers. While the second failure rate increase period (associated with end of life) may be impacted by this due to a decreased rate of electron trapping, the first failure rate is actually not impacted by this variable.

c) **Write Timing:** The decrease in write time to the device correlates directly with the write/erase cycling failure rate of the device. This shorter pulse reduces the cell time at voltage which then provides an enhanced life prior to the occurrence of a time dependent oxide breakdown. It also passes fewer electrons through the oxide providing less potential trapping possibilities while maintaining adequate margins for the written state.

Note:	The rise time of the signal, which the customer does not have control over, is also a dominant effect.

d) **VCC Voltage:** The higher voltages generate higher fields within the device. This causes more stress which is offset by the operational increase of internal timers and actually shortens the write time of the device.

Lower voltages have the opposite effect on the individual parameters except in cycles obviously where the write timer is externally controlled. This overall effect is minor compared to the others in magnitude on the failure rate curve and is variable over the customer operating range with a maximum at V_{CC} = 5.5 V.

e) **Pattern Effect:** The pattern that is programmed in the device does play a first order role in the overall lifetime. The act of programming a non-volatile memory inflicts damage on the device that cannot be repaired. This damage is the result of exposure to high electric fields which over a period of time either breakdown or trap up the effected oxide causing failures. The act of writing a cell from a one to a zero provides the maximum amount of stress by exercising the charge pump and passing electrons through the tunnel dielectric.

Note:	To write a zero even from a zero state causes an automatic byte erase prior to the write converting the bit to a one and returning it to its original state! Conversely writing a one from a one then passes no charge through the cell and, therefore, does no damage to the cell but does stress the charge pump. From an array standpoint, this would allow a checkerboard/ inverse checkerboard patterned device to endure twice the number of write cycles of an all zero patterned device. In general, this appears to be approximately correct but does neglect the charge pump and other peripheral wear-out mechanisms.

f) **Cycling Mode:** Three modes exist in Microchip devices that are primarily used for endurance evaluations. The byte write mode (one single byte written at a time) is the standard mode used by the customer in the field as well as the method of monitoring that has been chosen internally. This is to best estimate field lifetime expectations and actual failure rates. A second technique exists called block mode which exercises all the cells of the array simultaneously. The failure rates of byte cycled devices are approximately two times the failure rates of block cycled devices according to experimental test data. This effect has been traced back to the rise time of the programming signal at the memory cell. The faster this voltage rise occurs, the more damage occurs and the shorter the lifetime. The block mode has a much slower rise time given the entire array being utilized provides a much larger resistive/ capacitive load which slows the signal rise ultimately resulting in the greater lifetime. Please note that the page mode which can be utilized by the customers falls between the block and byte modes with respect to failure rate.

g) **Array Size:** This effect is a direct result of how fast most devices will fail due to a single bit not working simply due to the number of bits involved. This is not exactly double the failure rate with a doubling of the memory size since some circuits fail within the charge pump or decoding circuitry sections and are, therefore, not directly related to array size.

Field Results

After significant experimentation, Microchip has developed a model of the endurance failure rates as a function of all the variables listed above. This model is available to the customer in the form of a diskette called Total Endurance™. The Total Endurance Software Model allows the customer to bypass confusing information and conditions other than their application and directly predict the failure rate in their application conditions within a few percent. This also allows the customer to adjust operating parameters and immediately evaluate the impact on the results of the final system.

RELIABILITY DATA SUMMARY

The following section provides a reliability summary of Microchip's product. Included is reliability data and packaging information obtained during 1999.

SUMMARY OF RELIABILITY – 1999 ANNUAL REPORT DEVICE DATA

I. DYNAMIC LIFE/ RETENTION BAKE

Dynamic Life

Stress Temperature:	125°C	Activation Energy:	0.6 eV	77K
Derated Temperature:	55°C	Acceleration Rate:	42	
		Activation Energy:	0.7 eV	90K, 120K
		Acceleration Rate:	78	

Retention Bake

Stress Temperature:	150°C	Activation Energy:	1.2 eV	77K, 90K
Derated Temperature:	55°C	Acceleration Rate:	13718	& 120K

Microcontrollers						**Fit rates, 60% Confidence Level**		
Device	**Operation**	**168 Hrs.**	**1008 Hrs.**	**Fails**	**Device Hrs.**	**Infant Mortality**	**Long Term Life**	**Total Life**
ALL PICS	Dynamic Life	4/18105	1/14467	5	15,193,920	23	2	5
	Retention Bake	4/13840	6/8517	10	9,479,400	<1	<1	<1
ALL 120K PICS	Dynamic Life	1/8520	1/6945	2	7,265,160	18	4	6
	Retention Bake	3/6542	4/4336	7	4,741,296	<1	<1	<1
ALL 90K PICS	Dynamic Life	3/9015	0/7332	3	7,673,400	36	2	7
	Retention Bake	1/7298	2/4181	3	4,738,104	<1	<1	<1
ALL 77K PICS	Dynamic Life	0/570	0/190	0	255,360	230	138	86
	Retention Bake	0/0	0/0	0	0	N/A	N/A	N/A
PIC16C622A	Dynamic Life	0/500	0/499	0	503,160	141	28	23
	Retention Bake	0/566	0/563	0	568,008	1	<1	<1
PIC16C84A	Dynamic Life	0/570	0/190	0	255,360	230	138	86
	Retention Bake	0/0	0/0	0	0	N/A	N/A	N/A
PIC16C73B	Dynamic Life	0/3155	1/2733	1	2,825,760	22	11	9
	Retention Bake	0/1932	4/1508	4	1,591,296	<1	<1	<1
PIC16C72A	Dynamic Life	0/1253	0/1253	0	1,263,024	56	11	9
	Retention Bake	3/1187	0/699	3	786,576	2	<1	<1
PIC16C72	Dynamic Life	0/679	0/393	0	444,192	103	36	27
	Retention Bake	0/730	0/100	0	206,640	1	1	<1
PIC16C71	Dynamic Life	0/1399	0/1399	0	1,410,192	50	10	8
	Retention Bake	0/1441	1/1434	1	1,446,648	<1	<1	<1
PIC16C66/67/68	Dynamic Life	2/1719	0/1150	2	1,254,792	139	12	32
	Retention Bake	1/1031	0/298	1	423,528	1	<1	<1
PIC16C62A/64A	Dynamic Life	0/945	0/702	0	748,440	74	20	16
	Retention Bake	0/737	0/311	0	385,056	1	<1	<1
PIC16C58B	Dynamic Life	0/1620	0/1050	0	1,154,160	43	13	10
	Retention Bake	0/2040	0/759	0	980,280	<1	<1	<1
PIC16C58A	Dynamic Life	0/827	0/636	0	673,176	85	22	18
	Retention Bake	0/759	0/225	0	316,512	1	<1	<1
PIC17C44	Dynamic Life	1/1854	0/1739	1	1,772,232	84	8	15
	Retention Bake	0/1459	1/1104	1	1,172,472	<1	<1	<1
PIC12C508	Dynamic Life	0/1592	0/1313	0	1,370,376	44	11	9
	Retention Bake	0/1141	0/709	0	787,248	<1	<1	<1

Microcontrollers (Continued)						Fit rates, 60% Confidence Level		
PIC12C509A	Dynamic Life	1/1992	0/1410	1	1,519,056	78	10	17
	Retention Bake	0/1141	0/709	0	787,248	<1	<1	<1
Failure Modes:	Dynamic Life	1 unit of PIC17C44 failed for high IDD's that could not be localized						
		2 units of PIC16C67 failed SRAM						
		1 unit of PIC16C73B failed due to high IPD						
		1 unit of PIC12C509A failed due to high dynamic IDD						
	Retention Bake	1 unit of PIC16C67 failed due to high IPD						
		1 unit of PIC16C73B failed due to fuse charge loss (oxide)						
		3 units of PIC16C72A failed due to ONO oxide breakdown						
		1 unit of PIC16C71 failed due to oxide breakdown in the A/D capacitor array						
		3 units of PIC16C73B failed to read the test EPROM						
		1 unit of PIC17C44 failed to read the test EPROM						

Serial EEPROMs						Fit rates, 60% Confidence Level		
Device	**Operation**	**168 Hrs.**	**1008 Hrs.**	**Fails**	**Device Hrs.**	**Infant Mortality**	**Long Term Life**	**Total Life**
ALL SERIAL	Dynamic Life	6/40808	12/26978	18	29,517,264	26	14	16
EEPROMS	Retention Bake	45/38770	74/17651	119	21,340,200	1	<1	<1
77K SERIAL	Dynamic Life	2/28579	3/16262	5	18,461,352	16	7	8
EEPROMS	Retention Bake	6/34026	5/13737	11	17,255,448	<1	<1	<1
121K SERIAL	Dynamic Life	4/12229	9/10716	13	11,055,912	33	15	17
EEPROMS	Retention Bake	39/4744	69/3914	108	4,084,752	4	2	2
93LC46	Dynamic Life	0/2270	0/953	0	1,181,880	58	27	19
	Retention Bake	2/6515	2/2244	4	2,979,480	<1	<1	<1
93LC56/66	Dynamic Life	0/6100	0/4242	0	4,588,080	21	6	5
	Retention Bake	2/5014	0/2669	2	3,084,312	<1	<1	<1
93LC86	Dynamic Life	0/1157	3/500	3	614,376	113	238	163
	Retention Bake	0/497	0/112	0	177,576	1	1	<1
24LC01B	Dynamic Life	0/300	0/300	0	302,400	436	87	73
	Retention Bake	0/0	0/0	0	0	N/A	N/A	N/A
24LC02B	Dynamic Life	0/3952	0/1780	0	2,159,136	33	15	10
	Retention Bake	0/3983	0/1690	0	2,088,744	<1	<1	<1
24LC04B	Dynamic Life	0/3554	0/1600	0	1,941,072	37	16	11
	Retention Bake	0/6635	0/1920	0	2,727,480	<1	<1	<1
24LC16B	Dynamic Life	2/8014	0/4998	2	5,544,672	55	5	13
	Retention Bake	0/6003	3/3247	3	3,735,984	<1	<1	<1
24LC32A	Dynamic Life	0/600	0/600	0	604,800	218	44	36
	Retention Bake	2/865	0/863	2	870,240	2	<1	<1
24LCS21	Dynamic Life	0/1546	0/660	0	814,128	85	40	27
	Retention Bake	0/2542	0/568	0	904,176	<1	<1	<1
24LCS52	Dynamic Life	0/701	0/469	0	511,728	187	56	43
	Retention Bake	0/1466	0/312	0	508,368	<1	<1	<1
24LC64	Dynamic Life	3/4509	3/4061	6	4,168,752	71	16	23
	Retention Bake	6/1431	1/1423	7	1,435,728	2	<1	<1

Serial EEPROMs (Continued)						Fit rates, 60% Confidence Level		
Device	**Operation**	**168 Hrs.**	**1008 Hrs.**	**Fails**	**Device Hrs.**	**Infant Mortality**	**Long Term Life**	**Total Life**
24LC128	Dynamic Life	0/3676	3/2999	3	3,136,728	19	21	17
	Retention Bake	14/1860	38/1452	52	1,532,160	4	2	3
24LC256	Dynamic Life	1/4044	3/3656	4	3,750,432	38	18	18
	Retention Bake	19/1453	30/1039	49	1,116,864	6	3	3
25LC08/16/162	Dynamic Life	0/385	0/160	0	199,080	340	164	110
	Retention Bake	0/506	0/112	0	179,088	1	1	<1
Failure Modes:	Dynamic Life	1 unit of 24LC16B failed for high static I_{DD} due to oxide breakdown						
		1 unit of 24LC16B was a row fail						
		3 units of 93LC86 failed due to oxide failure in the charge pump						
		1 unit of 24LC64 failed due to oxide failure in the charge pump						
		5 units of 24LC64 failed due to single/multiple bit charge loss						
		3 units of 24LC128 failed due to single bit charge loss						
		1 unit of 24LC256 failed due to oxide failure in the charge pump						
		3 units of 24LC256 failed due to single/multiple bit charge loss						
	Retention Bake	2 units of 93LC56B failed due to single bit charge loss						
		3 units of 24LC16B failed due to single bit charge loss						
		7 units of 24LC64 failed due to single bit charge loss						
		52 units of 24LC128 failed due to single/multiple bit charge loss						
		49 units 24LC256 failed due to single/multiple bit charge loss						
		4 units of 93LC46B failed due to single bit charge loss						
		2 units of 24LC32A failed due to single/multiple bit charge loss						

Secure Data Products						Fit rates, 60% Confidence Level		
Device	**Operation**	**168 Hrs.**	**1008 Hrs.**	**Fails**	**Device Hrs.**	**Infant Mortality**	**Long Term Life**	**Total Life**
ALL SECURE DATA PRODUCTS	Dynamic Life	1/732	0/731	1	737,016	394	36	66
	Retention Bake	0/0	0/0	0	0	N/A	N/A	N/A
HCS301	Dynamic Life	0/348	0/348	0	350,784	376	75	63
	Retention Bake	0/0	0/0	0	0	N/A	N/A	N/A
HCS360	Dynamic Life	1/384	0/383	1	386,232	752	68	126
	Retention Bake	0/0	0/0	0	0	N/A	N/A	N/A
Failure Modes:	Dynamic Life	1 HCS360 failed data retention in the counter/semaphore						
	Retention Bake	N/A						

II. PRESSURE COOKER, HAST, TEMPERATURE CYCLE, AND THERMAL SHOCK PACKAGE DATA SUMMARY

Pressure Cooker

Stress Temperature: 121.5°C

HAST

Stress Temperature: 130°C

Operation	Package	24 Hrs.	168 Hrs.	Fails	Device Hrs.
Pressure Cooker	ALL PACKAGES	0/6650	212/6552	212	1,103,088
Pressure Cooker	MQFP	0/300	0/299	0	50,256
Pressure Cooker	PDIP	0/3850	118/3766	118	634,704
Pressure Cooker	PLCC	0/300	0/288	0	48,672
Pressure Cooker	SOIC/SSOP	0/1950	94/1949	94	327,456
Pressure Cooker	SOT	0/250	0/250	0	42,000
Failure Modes:	2 units of 8L PDIP (24LC04B) failed due to moisture penetration through passivation cracks 1 unit of 40L PDIP (PIC16C74B) failed due to corrosion of the lead post of 1 pin 5 units of 8L PDIP (24LC08B) failed due to moisture penetration through passivation cracks 3 units of 8L PDIP (24LC16B) failed due to array failures 14 units of 8L PDIP (24LC02) failed due to metal corrosion 37 units of 8L PDIP (24LC04B) failed due to leakage and functionality 9 units of 8L PDIP (24LC04B) failed due to moisture penetration of passivation cracks 16 units of 8L PDIP (93LC46B) failed due to metal corrosion 3 units of 28L PDIP (PIC16C54) failed to verify properly 2 units of 18L PDIP (PIC16C54) failed due to I/O leakage 26 units of 8L PDIP (24LC02B) failed due to moisture penetration through passivation cracks 2 units of 8L SOIC (93LC56B) failed due to moisture penetration of passivation cracks 15 units of 8L TSSOP (93LC56B) failed due to metal corrosion 77 units of 28L SSOP (PIC16C57) failed due to passivation cracking allowing metal corrosion				

Operation	Package	48 Hrs.	168 Hrs.	Fails	Device Hrs.
HAST	ALL PACKAGES	0/3360	4/3327	4	560,520
HAST	MQFP	0/150	0/142	0	20,048
HAST	PDIP	0/1700	4/1686	4	283,920
HAST	PLCC	0/240	0/240	0	40,320
HAST	SOIC	0/1160	0/1149	0	193,560
HAST	SOT	0/110	0/110	0	18,480
Failure Modes:	4 units of 18L PDIP (PIC16C54) failed due to bond pad corrosion				

Operation	Package	50 Cyc.	500 Cyc.	Fails
Temp. Cycles	ALL PACKAGES	0/1784	0/701	0
Temp. Cycles	MQFP	0/230	0/15	0
Temp. Cycles	PDIP	0/450	0/390	0
Temp. Cycles	PLCC	0/230	0/15	0
Temp. Cycles	SOIC	0/874	0/240	0
Temp. Cycles	SOT	0/0	0/41	0
Failure Modes:	N/A			

Operation	Package	100 Cyc.	500 Cyc.	Fails
Thermal Shock	ALL PACKAGES	0/2501	0/0	0
Thermal Shock	MQFP	0/245	0/0	0
Thermal Shock	PDIP	0/840	0/0	0
Thermal Shock	PLCC	0/245	0/0	0
Thermal Shock	SOIC	0/1129	0/0	0
Thermal Shock	SOT	0/42	0/0	0
Failure Modes:	N/A			

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