PIC16C433

In-Circuit Serial Programming™ for PIC16C433 OTP MCUs

This document includes the programming specifications for the following device:

• PIC16C433

1.0 PROGRAMMING THE PIC16C433

The PIC16C433 can be programmed using a serial method. In Serial mode, the PIC16C433 can be programmed while in the users system. This allows for increased design flexibility.

1.1 Hardware Requirements

The PIC16C433 requires two programmable power supplies, one for V_{DD} (2.0V to 6.0V recommended) and one for V_{PP} (12V to 14V). Both supplies should have a minimum resolution of 0.25V.

1.2 Programming Mode

The Programming mode for the PIC16C433 allows programming of user program memory, special locations used for ID, and the configuration word for the PIC16C433.
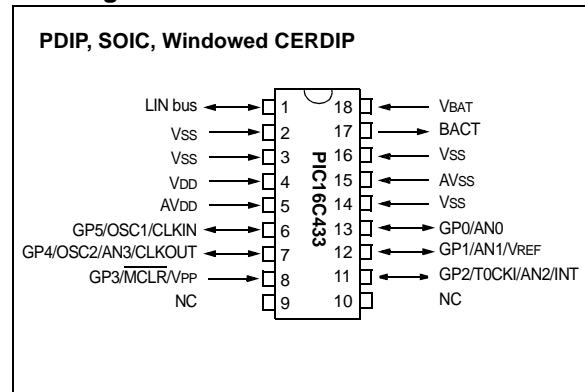
Pin Diagram

PDIP, SOIC, Windowed CERDIP

	PIC16C433	
LIN bus — 1		18 — V_{BAT}
V_{SS} — 2		17 — BACT
V_{SS} — 3		16 — V_{SS}
V_{DD} — 4		15 — AV_{SS}
AV_{DD} — 5		14 — V_{SS}
GP5/OSC1/CLKIN — 6		13 — GP0/AN0
GP4/OSC2/AN3/CLKOUT — 7		12 — GP1/AN1/V_{REF}
GP3/$\overline{MCLR}$/V_{PP} — 8		11 — GP2/T0CKI/AN2/INT
NC — 9		10 — NC

TABLE 1-1: PIN DESCRIPTIONS (DURING PROGRAMMING): PIC16C433

Pin Name	During Programming		
	Pin Name	Pin Type	Pin Description
GP1	CLOCK	I	Clock Input
GP0	DATA	I/O	Data Input/Output
$\overline{MCLR}$/V_{PP}	V_{PP}	P	Programming Power
V_{DD}	V_{DD}	P	Power Supply
V_{SS}	V_{SS}	P	Ground

PIC16C433

2.0 PROGRAM MODE ENTRY

2.1 User Program Memory Map

The user memory space extends from 0x0000 to 0x1FFF (8K). Table 2-1 shows actual implementation of program memory in the PIC16C433 family.

TABLE 2-1: IMPLEMENTATION OF PROGRAM MEMORY IN THE PIC16C433

Device	Program Memory Size
PIC16C433	0x000 - 0x7FF (2K)

When the PC reaches the last location of the implemented program memory, it will wrap around and address a location within the physically implemented memory (see Figure 2-1).

In Programming mode, the program memory space extends from 0x0000 to 0x3FFF, with the first half (0x0000-0x1FFF) being user program memory and the second half (0x2000-0x3FFF) being configuration memory. The PC will increment from 0x0000 to 0x1FFF and wrap to 0x000 or 0x2000 to 0x3FFF and wrap around to 0x2000 (not to 0x0000). Once in configuration memory, the highest bit of the PC stays a '1', thus always pointing to the configuration memory. The only way to point to user program memory is to reset the part and reenter Program/Verify mode, as described in Section 2.2.
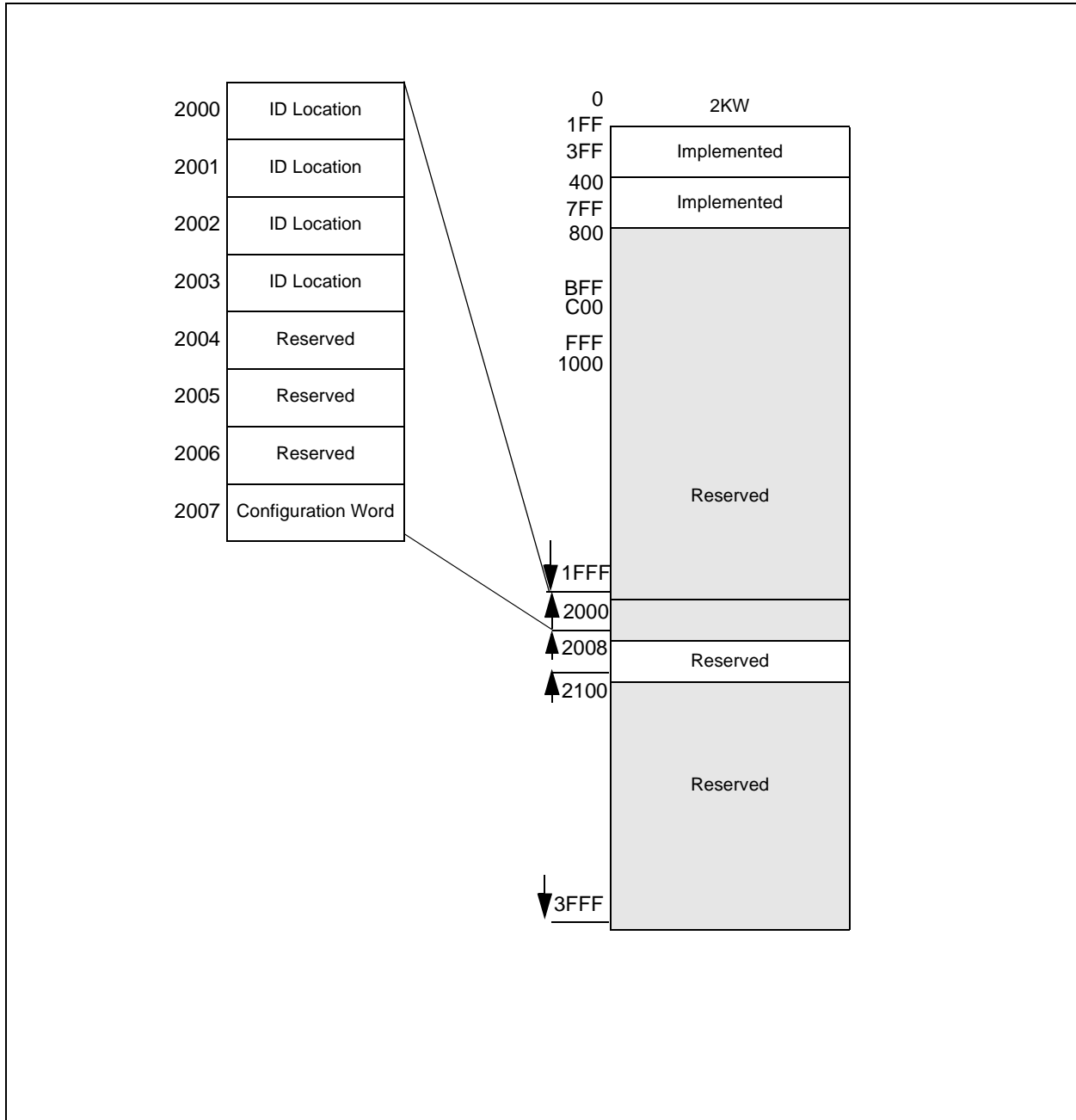
The last location of the program memory space holds the factory programmed oscillator calibration value. This location should not be programmed except when blank (a non-blank value should not cause the device to fail a blank check). If blank, the programmer should program it to a RETLW XX statement where "XX" is the calibration value.

In the configuration memory space, 0x2000-0x20FF are utilized. When in configuration memory, as in the user memory, the 0x2000-0x2XFF segment is repeatedly accessed as the PC exceeds 0x2XFF (see Figure 2-1).

A user may store identification information (ID) in four ID locations. The ID locations are mapped in [0x2000:0x2003].

Note 1: All other locations in PICmicro® MCU configuration memory are reserved and should not be programmed.

FIGURE 2-1: PROGRAM MEMORY MAPPING

2000	ID Location
2001	ID Location
2002	ID Location
2003	ID Location
2004	Reserved
2005	Reserved
2006	Reserved
2007	Configuration Word

0   2KW
1FF
3FF   Implemented
400
7FF   Implemented
800

BFF
C00

FFF
1000

Reserved

1FFF
2000
2008
Reserved
2100

Reserved

3FFF

PIC16C433

2.2 Program/Verify Mode

The Program/Verify mode is entered by holding pins GP1 and GP0 low while raising $\overline{MCLR}$ pin from V_{IL} to V_{IHH} (high voltage). V_{DD} is then raised from VIL to VIH.Once in this mode, the user program memory and the configuration memory can be accessed and programmed in serial fashion. The mode of operation is serial, and the memory that is accessed is the user program memory. GP1 is a Schmitt Trigger input in this mode.

The sequence that enters the device into the Programming/Verify mode places all other logic into the RESET state (the $\overline{MCLR}$ pin was initially at V_{IL}). This means that all I/O are in the RESET state (hi-impedance inputs).

Note 1: The $\overline{MCLR}$ pin must be raised from V_{IL} to V_{IHH} before V_{DD} is applied. This is to ensure that the device does not have the PC incremented while in valid operation range.

    2: Do not power GP2, GP4, or GP5 before V_{DD} is applied.

2.2.1 PROGRAM/VERIFY OPERATION

The GP1 pin is used as a clock input pin, and the GP0 pin is used for entering command bits and data input/output during serial operation. To input a command, the clock pin (GP1) is cycled six times. Each command bit is latched on the falling edge of the clock with the least significant bit (LSb) of the command being input first. The data on pin GP0 is required to have a minimum setup and hold time (see AC/DC specs) with respect to

the falling edge of the clock. Commands that have data associated with them (read and load) are specified to have a minimum delay of 1μs between the command and the data. After this delay, the clock pin is cycled 16 times with the first cycle being a START bit and the last cycle being a STOP bit. Data is also input and output LSb first. Therefore, during a read operation the LSb will be transmitted onto pin GP0 on the rising edge of the second cycle, and during a load operation the LSb will be latched on the falling edge of the second cycle. A minimum 1μs delay is also specified between consecutive commands.

All commands are transmitted LSb first. Data words are also transmitted LSb first. The data is transmitted on the rising edge and latched on the falling edge of the clock. To allow for decoding of commands and reversal of data pin configuration, a time separation of at least 1μs is required between a command and a data word (or another command).

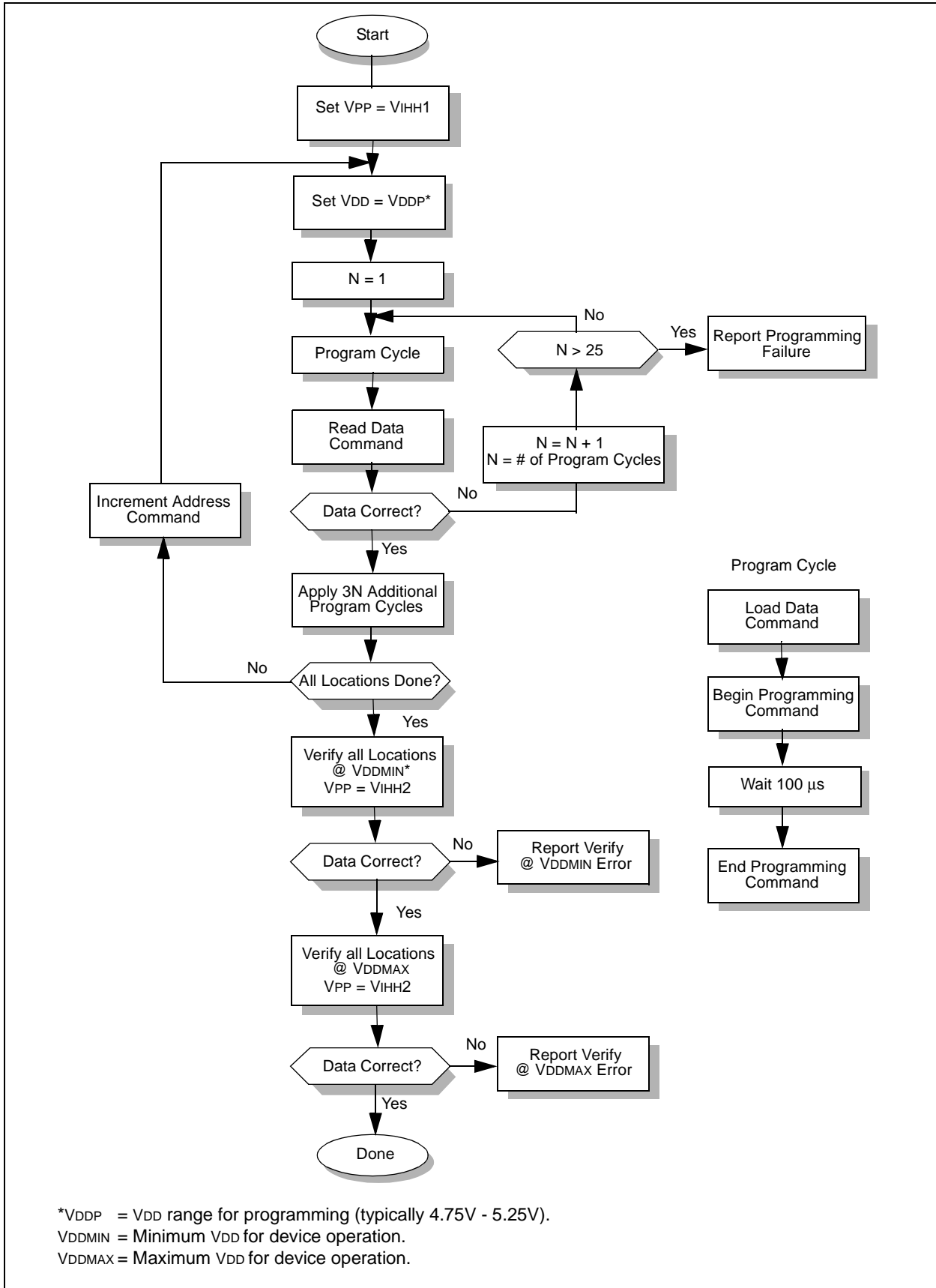The commands that are available are listed inTable 2-2.

2.2.1.1 Load Configuration

After receiving this command, the program counter (PC) will be set to 0x2000. By then applying 16 cycles to the clock pin, the chip will load 14-bits, a "data word" as described above, to be programmed into the configuration memory. A description of the memory mapping schemes for normal operation and Configuration mode operation is shown in Figure 2-1. After the configuration memory is entered, the only way to get back to the user program memory is to exit the Program/Verify Test mode by taking $\overline{MCLR}$ low (V_{IL}).
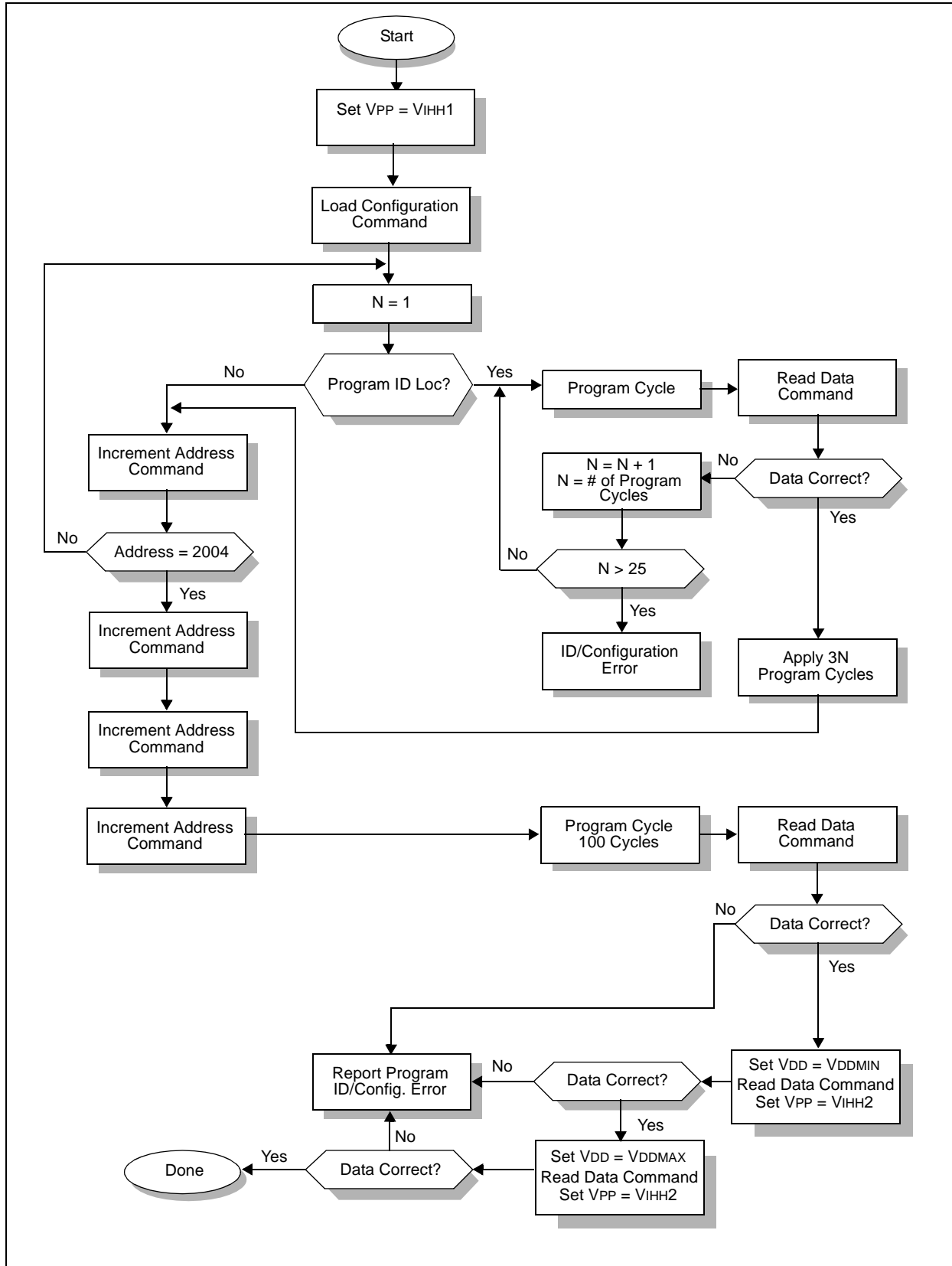
TABLE 2-2: COMMAND MAPPING

Command	Mapping (MSb ... LSb)						Data
Load Configuration	0	0	0	0	0	0	0, data(14), 0
Load Data	0	0	0	0	1	0	0, data(14), 0
Read Data	0	0	0	1	0	0	0, data(14), 0
Increment Address	0	0	0	1	1	0	
Begin programming	0	0	1	0	0	0	
End Programming	0	0	1	1	1	0	

FIGURE 2-2: PROGRAM FLOW CHART - PIC16C433 PROGRAM MEMORY

*V_{DDP} = V_{DD} range for programming (typically 4.75V - 5.25V).
V_{DDMIN} = Minimum V_{DD} for device operation.
V_{DDMAX} = Maximum V_{DD} for device operation.

PIC16C433

Start

Set $V_{PP} = V_{IHH1}$

Load Configuration
Command

N = 1

Program ID Loc? — No → Increment Address Command

Program ID Loc? — Yes → Program Cycle → Read Data Command

Increment Address Command → Address = 2004 — No (loop back)

Address = 2004 — Yes → Increment Address Command

Read Data Command → Data Correct? — No → N = N + 1 / N = # of Program Cycles

N = N + 1 / N = # of Program Cycles → N > 25 — No (loop back)

N > 25 — Yes → ID/Configuration Error

Data Correct? — Yes → Apply 3N Program Cycles

Increment Address Command

Increment Address Command → Program Cycle 100 Cycles → Read Data Command

Data Correct? — No → Report Program ID/Config. Error

Data Correct? — Yes → Set $V_{DD} = V_{DDMIN}$ / Read Data Command / Set $V_{PP} = V_{IHH2}$

Set $V_{DD} = V_{DDMIN}$ / Read Data Command / Set $V_{PP} = V_{IHH2}$ → Data Correct?

Data Correct? — No → Report Program ID/Config. Error

Data Correct? — Yes → Set $V_{DD} = V_{DDMAX}$ / Read Data Command / Set $V_{PP} = V_{IHH2}$

Report Program ID/Config. Error → Data Correct? — No

Set $V_{DD} = V_{DDMAX}$ / Read Data Command / Set $V_{PP} = V_{IHH2}$ → Data Correct?

Data Correct? — Yes → Done

2.2.1.2 Load Data

After receiving this command, the chip will load in a 14-bit "data word" when 16 cycles are applied, as described previously. A timing diagram for the load data command is shown in Figure 5-1.

2.2.1.3 Read Data

After receiving this command, the chip will transmit data bits out of the memory currently accessed, starting with the second rising edge of the clock input. The GP0 pin will go into output mode on the second rising clock edge, and it will revert back to input mode (hi-impedance) after the 16th rising edge. A timing diagram of this command is shown in Figure 5-2.

2.2.1.4 Increment Address

The PC is incremented when this command is received. A timing diagram of this command is shown in Figure 5-3.

2.2.1.5 Begin Programming

A load command (load configuration or load data) must be given before every begin programming command. Programming of the appropriate memory (test program memory or user program memory) will begin after this command is received and decoded. Programming should be performed with a series of 100µs programming pulses. A programming pulse is defined as the time between the begin programming command and the end programming command.

2.2.1.6 End Programming

After receiving this command, the chip stops programming the memory (configuration program memory or user program memory) that it was programming at the time.

2.3 Programming Algorithm Requires Variable V_{DD}

The PIC16C433 uses an intelligent algorithm. The algorithm calls for program verification at V_{DDMIN} as well as V_{DDMAX}. Verification at V_{DDMIN} guarantees good "erase margin". Verification at V_{DDMAX} guarantees good "program margin".

The actual programming must be done with V_{DD} in the V_{DDP} range (4.75 - 5.25V).

V_{DDP} = V_{CC} range required during programming.

V_{DDMIN} = minimum operating V_{DD} spec for the part.

V_{DDMAX} = maximum operating V_{DD} spec for the part.

Programmers must verify the PIC16C433 at its specified V_{DDMAX} and V_{DDMIN} levels. Since Microchip may introduce future versions of the PIC16C433 with a broader V_{DD} range, it is best that these levels are user selectable (defaults are ok).

Note:	Any programmer not meeting these requirements may only be classified as "prototype" or "development" programmer, but not a "production" quality programmer.

PIC16C433

3.0   CONFIGURATION WORD

The PIC16C433 family members have several configu-
ration bits. These bits can be programmed (reads '0'),
or left unprogrammed (reads '1'), to select various
device configurations. Figure 3-1 provides an overview
of configuration bits.

FIGURE 3-1:   CONFIGURATION WORD

Bit Number:

13	12	11	10	9	8	7	6	5	4	3	2	1	0
CP1	CP0	CP1	CP0	CP1	CP0	MCLRE	CP1	CP0	$\overline{\text{PWRTE}}$	WDTE	FOSC2	FOSC1	FOSC0

Register: CONFIG
Address   2007h

bit 13-8, 6-5: **CP1:CP0:** Code Protection bits**(1, 2)**
          11 = Code protection off
          10 = 0400h-07FFh code protected
          01 = 0200h-07FFh code protected
          00 = 0000h-07FFh code protected

bit 7:   **MCLRE:** GP3/$\overline{\text{MCLR}}$ Pin Function Select
          1 = GP3/$\overline{\text{MCLR}}$ pin function is $\overline{\text{MCLR}}$
          0 = GP3/$\overline{\text{MCLR}}$ pin function is digital I/O, $\overline{\text{MCLR}}$ internally tied to V$_{DD}$

bit 4:   **PWRTE:** Power-up Timer Enable bit
          1 = PWRT disabled
          0 = PWRT enabled

bit 3:   **WDTE:** Watchdog Timer Enable bit
          1 = WDT enabled
          0 = WDT disabled

bit 2-0:   **FOSC2:FOSC0:** Oscillator Selection bits
          111 = EXTRC oscillator / CLKOUT function on GP4/OSC2/CLKOUT pin
          110 = EXTRC oscillator / GP4 function on GP4/OSC2/CLKOUT pin
          101 = INTRC oscillator / CLKOUT function on GP4/OSC2/CLKOUT pin
          100 = INTRC oscillator / GP4 function on GP4/OSC2/CLKOUT pin
          011 = Invalid selection
          010 = HS oscillator
          001 = XT oscillator
          000 = LP oscillator

Note 1: All of the CP1:CP0 pairs have to be given the same value to enable the code protection scheme listed.

2: 07FFh is always uncode protected on the PIC16C433. This location contains the RETLW xx calibration instruction for the INTRC.

© 2000 Microchip Technology Inc.

4.0   CODE PROTECTION

The program code written into the EPROM can be protected by writing to the CP0 and CP1 bits of the configuration word.

For PIC16C433 devices, once code protection is enabled, all protected segments read '0's (or "garbage values") and are prevented from further programming. All unprotected segments, including ID and configuration word locations, and calibration word location, read normally and can be programmed.

4.1   Embedding Configuration Word and ID Information in the HEX File

To allow portability of code, the programmer is required to read the configuration word and ID locations from the HEX file when loading the HEX file. If configuration word information was not present in the HEX file, then a simple warning message may be issued. Similarly, while saving a HEX file, configuration word and ID information must be included. An option to not include this information may be provided.

Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

TABLE 4-1:   CONFIGURATION WORD

PIC16C433

To code protect:

- Protect all memory   `00 0000 X00X XXXX`
- Protect 0200h-07FFh `01 0101 X01X XXXX`
- Protect 0400h-07FFh `10 1010 X10X XXXX`
- No code protection   `11 1111 X11X XXXX`

Program Memory Segment	R/W in Protected Mode	R/W in Unprotected Mode
Configuration Word (0x2007)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Unprotected memory segment	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
Protected memory segment	Read All 0's, Write Disabled	Read Unscrambled, Write Enabled
ID Locations (0x2000:0x2003)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled
INTRC Calibration Word (0X7FF)	Read Unscrambled, Write Enabled	Read Unscrambled, Write Enabled

PIC16C433

4.2 Checksum

4.2.1 CHECKSUM CALCULATIONS

Checksum is calculated by reading the contents of the PIC16C433 memory locations and adding the opcodes, up to the maximum user addressable location, excluding the oscillator calibration location in the last address. Any carry bits exceeding 16-bits are neglected. Finally, the configuration word (appropriately masked) is added to the checksum. Checksum computation for the PIC16C433 device is shown in Table 4-2.

The checksum is calculated by summing the following:

• The contents of all program memory locations
• The configuration word, appropriately masked
• Masked ID locations (when applicable)

The least significant 16 bits of this sum is the checksum.

The following table describes how to calculate the checksum for each device. Note that the checksum calculation differs depending on the code protect setting. Since the program memory locations read out differently depending on the code protect setting, the table describes how to manipulate the actual program memory values to simulate the values that would be read from a protected device. When calculating a checksum by reading a device, the entire program memory can simply be read and summed. The configuration word and ID locations can always be read.

Note that some older devices have an additional value added in the checksum. This is to maintain compatibility with older device programmer checksums.

TABLE 4-2: CHECKSUM COMPUTATION

Device	Code Protect	Checksum*	Blank Value	Ox25E6 at 0 and max address
PIC16C433	OFF	SUM[0x000:0x7FE] + CFGW & 0x3FFF	F800	C3CE
	1/2	SUM[0x000:0x3FF] + CFGW & 0x3FFF + SUM_ID	1EDF	D094
	3/4	SUM[0x000:0x1FF] + CFGW & 0x3FFF + SUM_ID	0BBF	BD74
	ALL	CFGW & 0x3FFF + SUM_ID	F89F	C46D

Legend: CFGW = Configuration Word
SUM[a:b] = [Sum of locations a through b inclusive]
SUM_ID = ID locations masked by 0xF then made into a 16-bit value with ID0 as the most significant nibble. For example,
ID0 = 0x12, ID1 = 0x37, ID2 = 0x4, ID3 = 0x26, then SUM_ID = 0x2746.
SUM_ID defaults to the non-code protected checksum.
*Checksum = [Sum of all the individual expressions] **MODULO** [0xFFFF]
+ = Addition
& = Bitwise AND

5.0 PROGRAM/VERIFY MODE ELECTRICAL CHARACTERISTICS

TABLE 5-1: AC/DC CHARACTERISTICS
TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE

Standard Operating Conditions Operating Temperature: $+10°C \leq T_A \leq +40°C$, unless otherwise stated, (25°C is recommended) Operating Voltage: $4.5V \leq V_{DD} \leq 5.5V$, unless otherwise stated.							
Parameter No.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
		General					
PD1	V_{DDP}	Supply voltage during programming	4.75	5.0	5.25	V	
PD2	I_{DDP}	Supply current (from V_{DD}) during programming			20	mA	
PD3	V_{DDV}	Supply voltage during verify	V_{DDMIN}		V_{DDMAX}	V	**(Note 1)**
PD4	V_{IHH1}	Voltage on $\overline{MCLR}$/V_{PP} during programming	12.75		13.25	V	**(Note 2)**
PD5	V_{IHH2}	Voltage on $\overline{MCLR}$/V_{PP} during verify	$V_{DD} + 4.0$		13.5		
PD6	I_{PP}	Programming supply current (from V_{PP})			50	mA	
PD9	V_{IH1}	(GP0, GP1) input high level	0.8 V_{DD}			V	Schmitt Trigger input
PD8	V_{IL1}	(GP0, GP1) input low level	0.2 V_{DD}			V	Schmitt Trigger input

		Serial Program Verify					
P1	T_R	$\overline{MCLR}$/V_{PP} rise time (V_{SS} to V_{IHH}) for Test mode entry			8.0	μs	
P2	T_f	$\overline{MCLR}$ fall time			8.0	μs	
P3	T_{set1}	Data in setup time before clock ↓	100			ns	
P4	T_{hld1}	Data in hold time after clock ↓	100			ns	
P5	T_{dly1}	Data input not driven to next clock input (delay required between command/data or command/command)	1.0			μs	
P6	T_{dly2}	Delay between clock ↓ to clock ↑ of next command or data	1.0			μs	
P7	T_{dly3}	Clock ↑ to data out valid (during read data)	200			ns	
P8	T_{hld0}	Hold time after V_{DD}↑	2			μs	
P9	T_{PPDP}	Hold time after V_{PP}↑	5			μs	

Note 1: Program must be verified at the minimum and maximum V_{DD} limits for the part.
2: V_{IHH} must be greater than $V_{DD} + 4.5V$ to stay in Programming/Verify mode.

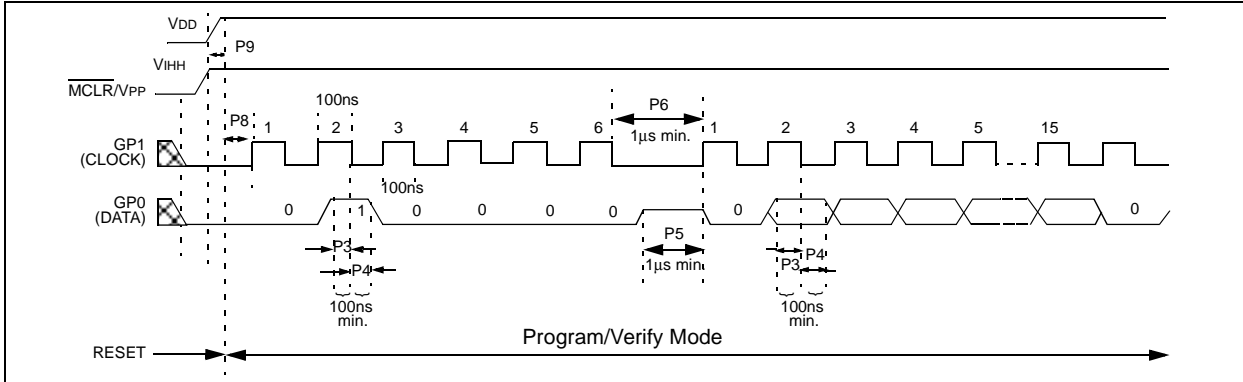# PIC16C433

FIGURE 5-1: LOAD DATA COMMAND (PROGRAM/VERIFY)
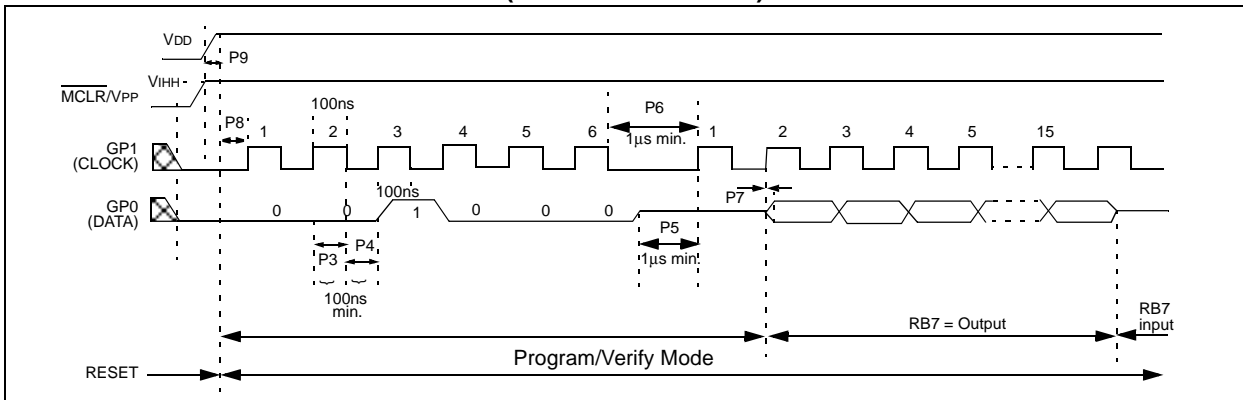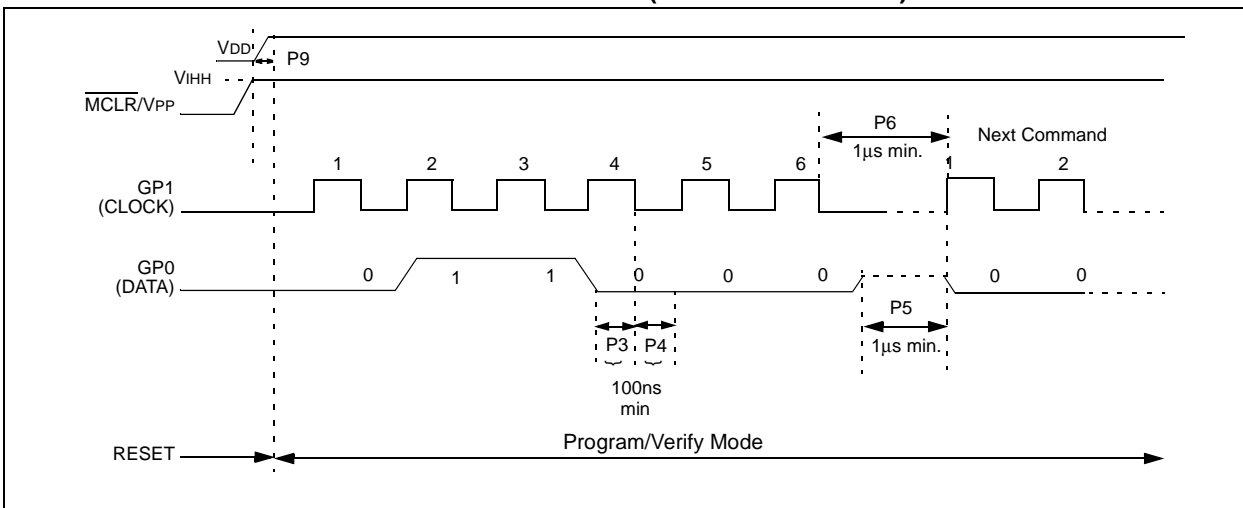

FIGURE 5-2: READ DATA COMMAND (PROGRAM/VERIFY)

FIGURE 5-3: INCREMENT ADDRESS COMMAND (PROGRAM/VERIFY)

© 2000 Microchip Technology Inc.

NOTES:

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: http://www.microchip.com

Rocky Mountain
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-7456

Atlanta
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Boston
2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Chicago
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas
4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Dayton
Two Prestige Place, Suite 130
Miamisburg, OH 45342
Tel: 937-291-1654 Fax: 937-291-9175

Detroit
Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Los Angeles
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

New York
150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

China - Beijing
Microchip Technology Beijing Office
Unit 915
New China Hong Kong Manhattan Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Shanghai
Microchip Technology Shanghai Office
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

Hong Kong
Microchip Asia Pacific
RM 2101, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India
Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan
Microchip Technology Intl. Inc.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea
Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea
Tel: 82-2-554-7200 Fax: 82-2-558-5934

ASIA/PACIFIC (continued)

Singapore
Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan
Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark
Microchip Technology Denmark ApS
Regus Business Centre
Lautrup hoj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France
Arizona Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - ler Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany
Arizona Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy
Arizona Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom
Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

10/01/00
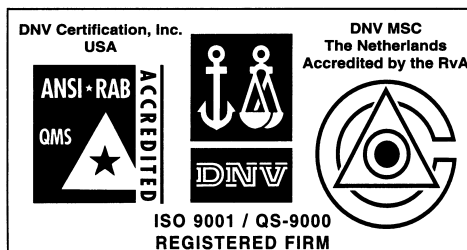
Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs and microperipheral products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.

DNV Certification, Inc. USA

DNV MSC The Netherlands Accredited by the RvA

ANSI • RAB
QMS
ACCREDITED
DNV

ISO 9001 / QS-9000 REGISTERED FIRM