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TECHNICAL MANUAL

MK77679 MDX-SASI2 STD BUS SHUGART ASSOCIATES SYSTEM INTERFACE (SASI™)

FEATURES

- ☐ STD-Z80™ Bus Compatible
- ☐ 5 Volt Operation
- ☐ Supports Shugart Associates System Interface (SASI)*
- ☐ Polled or Interrupt Driven
- ☐ Mode 2 Interrupt Capability
- ☐ 2.5 to 4 MHz Operation
- ☐ Eight Address I/O Port Block
- ☐ I/O EXP Supported
- ☐ Auto Acknowledge Logic
- ☐ On-Board DMA Controller
- ☐ External DMA Request Supported
- ☐ DMA Daisy-Chain Supported
- ☐ External Wait Request Supported

DESCRIPTION

The MDX-SASI2 interfaces the STD-Z80 Bus to Shugart Associates System Interface (SASI). SASI is a universal system interface that lets OEMs upgrade, mix, and interchange peripherals without affecting software. SASI is an intelligent systems interface, which results in easy peripheral integration.

MDX-SASI2 addressing may be strapped for any eight-byte boundary in the STD-Z80 I/O space. In addition, the IOEXP* signal is supported for maximum configuration flexibility. The card contains an on-board DMA controller for increased throughput. An external request input allows other cards in the system to use this controller as well. The STD-Z80 WAITRQ* signal can be used to speed-match the DMA to slower memories, and DMA daisy-chaining is provided for via an additional connector.

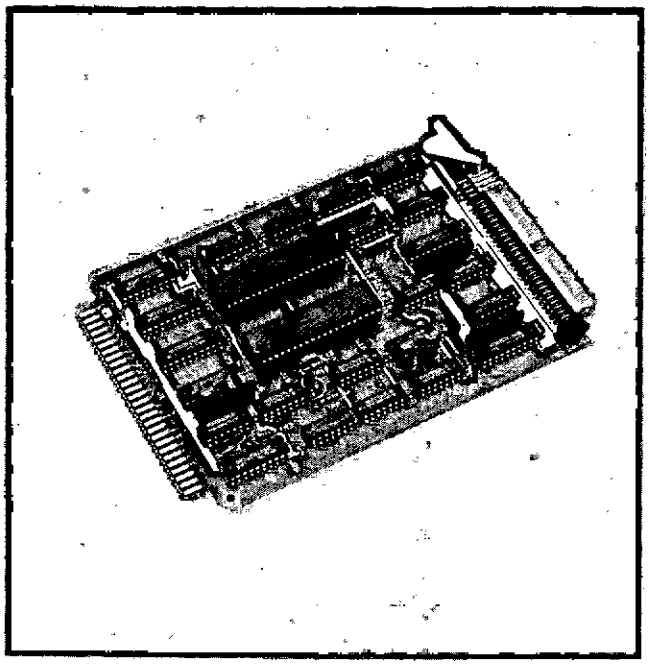


Figure 1. MDX-SASI2

The board also contains Auto Acknowledge logic. This strapping option provides automatic handshaking for SASI information transfers, and is essential to the board's DMA operation. If finer control is required for debugging purposes, Auto Acknowledge can be disabled.

MDX-SASI2 is a medium cost, high performance interface. At 4 MHz, MDX-SASI2 has a maximum transfer rate of 570 KBytes/second. In comparison, a double-sided, double-density floppy disk has a transfer rate of 62.5 KBytes/second.

SASI is a trademark of Shugart Associates.
Z-80 is a trademark of Zilog Corporation.
* indicates low active signal.

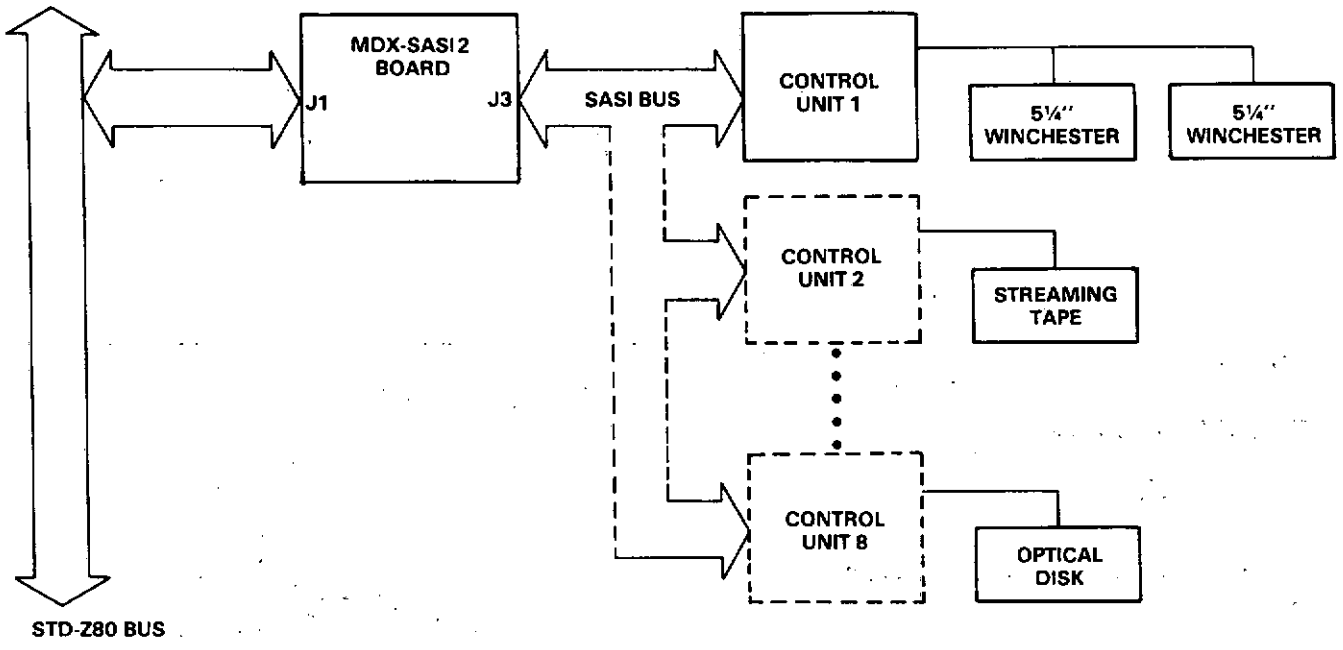


Figure 2. System Inter Connection Diagram

SPECIFICATIONS
(Note: * = low active signal)

Electrical Specifications

System Bus: STD-Z80 Compatible

Inputs: One 74 LS Load Max

Outputs: I_{OH} = 15 mA min at 2.5 VDC
I_{OL} = 24 mA min at 0.5 VDC

Interrupts: Mode 2. Vectored Interrupts generated. Interrupt vector programmable upon initialization. Daisy-chained interrupt priority.

System Interrupt Units (SIUs) = 2

System Clock: 2.5 to 4 MHz

I/O Addressing: 8 ports on board selectable to any of 32 eight port slots by jumper options; board may be placed in main I/O space or expansion I/O space (IOEXP*)

Power Requirements: +5VDC ± 5% @ 1.1A max

Operating Temperature: 32°F to 140°F
0°C to 60°C

Mechanical Specifications

Card dimensions
4.5" (11.43 cm) high by 6.50" (16.51 cm) long
0.48" (1.22 cm) maximum profile thickness

0.062" (0.16 cm) printed circuit board thickness

Connectors

J1 - STD-Bus:
56 pin dual readout edge connector; 0.125" centers
Mating connectors:
PCB - Viking 3VH28/1CE5
W/W - Viking 3VH28/1CND5
SDR LUG - Viking 3VH28/1CN5

J2 - External Ready/DMA Daisy-Chain:
2 x 4, 0.025" square pins; 0.1" centers, right angle

J3 - SASI Interface:
Shrouded 2 x 25, 0.025" square pins; 0.1" centers, right angle
Mating connectors:
Winchester 51-1150
Berg 65485-022

STRAPPIING OPTIONS

Figure 3 shows the location of the strapping options J4, J5, J6, and J7. The following description gives the purpose of each strap and how the strap is set at the factory.

J4: EXT REQ* Level - This jumper determines whether the EXT REQ* input to MDX-SASI2 is active low or active high. For an active high EXT REQ*, strap pins 1 and 2; for an active low EXT REQ*, strap pins 2 and 3 (factory setting).

J5: Auto Acknowledge Enable - The factory straps J5 to enable the Auto Acknowledge logic. This circuit will carry out the SASI bus handshake on information transfers without requiring the CPU to bit toggle control lines (SASI ACK). J5 must be strapped if DMA operation is desired. If the user needs to explicitly bit toggle the SASI ACK line (e.g., to debug a controller board) the J5 strap should be removed.

J6: Port Select - The board may be placed on any eight byte boundary by changing J6. The factory setting is port A0'H, for compatibility with Mostek's M/OS-80 Operating Systems and CP/M 3.0™ Operating System (see reference section). The pins on J6 are defined in Figure 4. Note that a strap installed implies a logic zero.

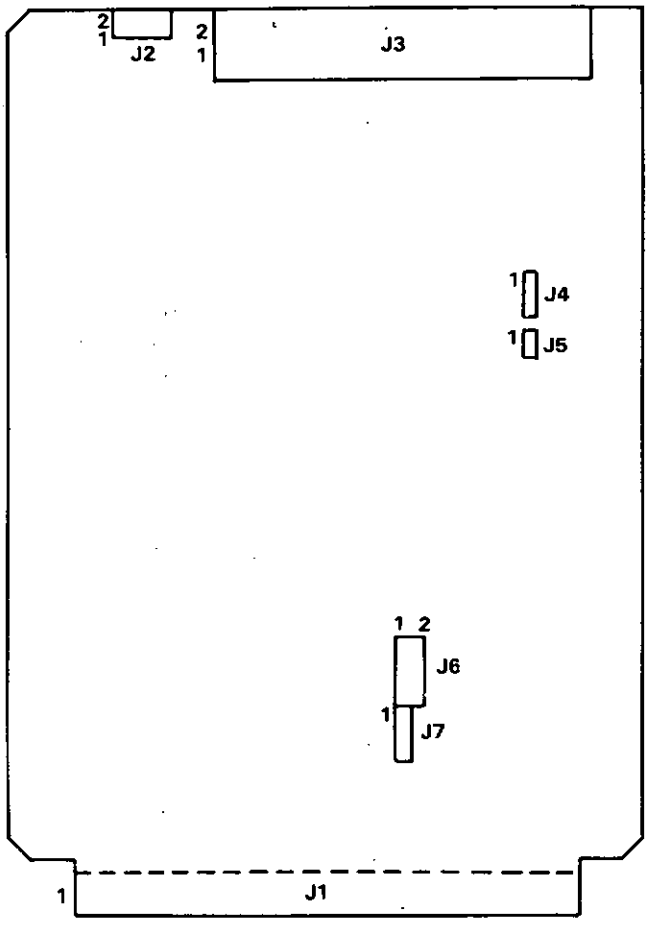


Figure 3. MDX-SASI2 Board Outline and Header Locations

CP/M 3.0 is a trademark of Digital Research

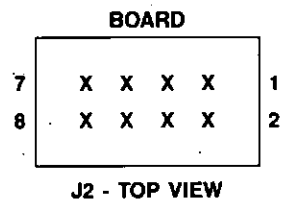
Address	Corresponding Pins on J6	Factory Setting	(AOH)
A3	1 and 2	strapped	(0)
A4	3 and 4	strapped	(0)
A5	5 and 6	not strapped	(1)
A6	7 and 8	strapped	(0)
A7	9 and 10	not strapped	(1)

Figure 4. Address Strapping Options

J7: I/O Expand - This jumper allows the IOEXP* line to be included or ignored in the address decoding of MDX-SASI2. Strapping pins 2 and 3 causes IOEXP* to be ignored (factory setting). If a given board is to be selected on IOEXP* = 0, strap pins 1 and 2, then pins 3 and 4. To cause board selection when IOEXP* = 1, strap pins 1 and 2 only.

Multiple DMA Option

MDX-SASI2 is designed to support the operation of multiple DMA devices in a system. Two signals, BAI (Bus Acknowledge In) and BAO (Bus Acknowledge Out), provide for the connection of a priority DMA daisy-chain. Figure 5 shows their locations on connector J2. As an example, suppose a system requires the use of four MDX-SASI2 boards. As shown in Figure 6, the highest priority board would be the DMA device 1, while the lowest priority board would be DMA device 4. Thus, MDX-SASI2 boards are prioritized for multiple DMA operation by their electrical position in a system as determined by their J2 interconnections. Typically, twisted



Pin No.	Function
1, 3, 5, 7	Ground
2	BAI (Bus ACK In)
4	BAO (Bus ACK Out)
6	No connection
8	External DMA Request Input (/EXT REQ)

Figure 5. J2 Connector Pin Definitions

pairs (signal + ground) are used to connect the bus priority chain.

Pin 8 of J2 provides an external request input (EXT REQ*), whereby other STD-Z80 I/O cards without on-board DMA capability can 'borrow' it from MDX-SASI2. This is done by feeding a card's DMA request signal through EXT REQ* to the READY pin of the MK3883 Z80-DMA chip on MDX-SASI2. EXT REQ* can be active low or active high (strap J4).

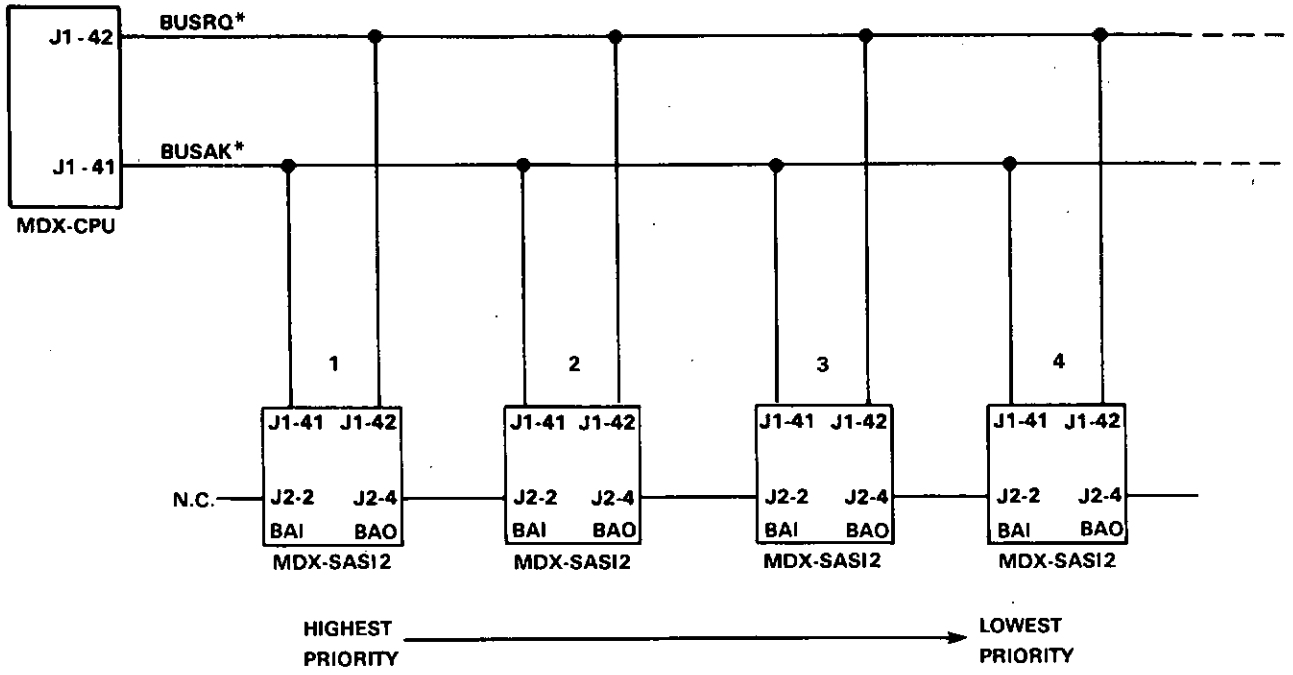


Figure 6. Connection of DMA Daisy-Chain.

CONNECTION TO THE SASI BUS

The following shows the pin definitions of J3, the 50 pin connector to the SASI bus. Note that the SASI bus is divided into a data section and a control section. Except for the data bus parity line (pin 18) and the ATN (attention) line (pin 34), MDX-SASI2 fully supports the SASI bus. Parity is a SASI bus option while ATN is not widely used by SASI peripheral controllers.

NOTE: All odd pins are ground.

Pin. No.	Signal	
2	DBO (data bit 0, LSB)	SASI Data Bus
4	DB1 (data bit 1)	
6	DB2 (data bit 2)	
8	DB3 (data bit 3)	
10	DB4 (data bit 4)	
12	DB5 (data bit 5)	
14	DB6 (data bit 6)	
16	DB7 (data bit 7, MSB	
18	Not used (data bus parity)	
20	Not used	
22	Not used	
24	Not used	
26	Not used	
28	Not used	
30	Not used	
32	Not used	
34	Not used (ATN, attention)	SASI Control Bus
36	BSY (busy)	
38	ACK (acknowledge)	
40	RST (reset)	
42	MSG (message)	
44	SEL (select)	
46	C/D (control/data)	
48	REQ (request)	
50	I/O (input/output)	

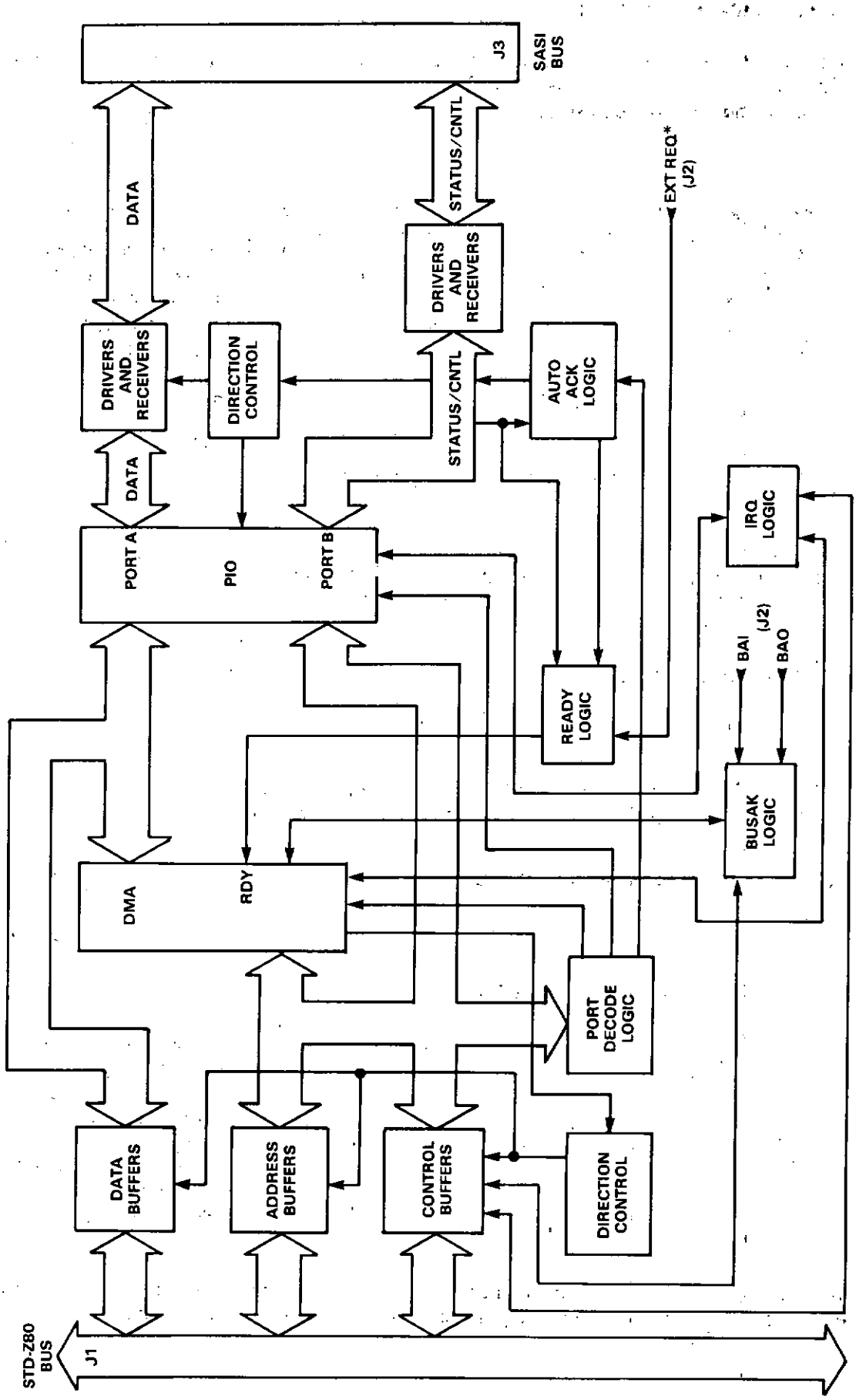


Figure 7. MDX-SASI2 Block Diagram

Programmer's Model of MDX-SASI2

MDX-SASI2 is compatible with any STD-Z80 bus system. The board consumes eight contiguous I/O port locations, beginning on any 8-byte boundary as strapped by the user. This is illustrated in the table below.

A7	A6	A5	A4	A3	A2	A1	A0	Function
X	X	X	X	X	0	0	0	PIO Port A Data (Bidirectional)
X	X	X	X	X	0	0	1	PIO Port B Data (Bit Control Mode)
X	X	X	X	X	0	1	0	PIO Port A Control
X	X	X	X	X	0	1	1	PIO Port B Control
X	X	X	X	X	1	0	0	DMA Controller
X	X	X	X	X	1	0	1	Reserved
X	X	X	X	X	1	1	0	Reserved
X	X	X	X	X	1	1	1	Reserved

Where X = Port Strapping options of the MDX-SASI2 Board.

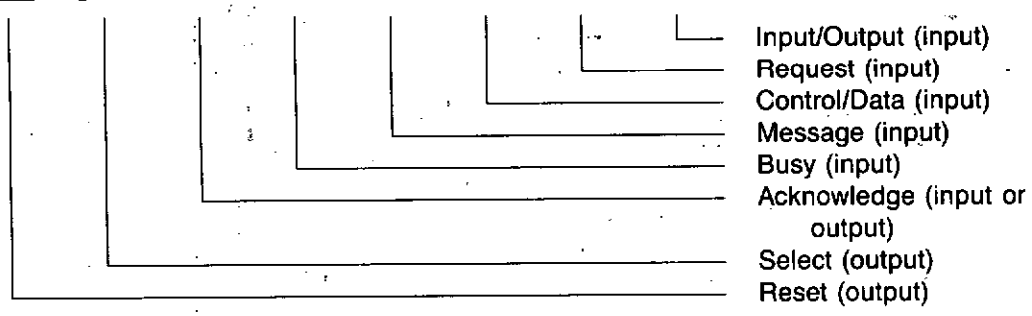
PIO Port A Data is used as a bidirectional data port. It is connected in hardware to the data portion of the SASI bus. PIO Port B Data is used in bit control mode to implement the control portion of the SASI bus. The bit definitions of these two ports are shown below.

SASI Data Port Definitions (PIO Port A):

a7	a6	a5	a4	a3	a2	a1	a0
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

SASI Control Port Definitions (PIO Port B):

b7	b6	b5	b4	b3	b2	b1	b0
RES	SEL	ACK	BSY	MSG	C/D	REQ	I/O



Note that if Automatic Acknowledge is enabled for use, b5 on the PIO should be programmed as an input. If Automatic Acknowledge is disabled, b5 should be programmed as an output.

STD-Z80 Bus Signals Used by MDX-SASI2

The following is a list of STD-Z80 Bus signals used by the MDX-SASI2 board. Pin numbers without a description are not used by MDX-SASI2. The signals are accessed via J1, a 56 pin edge connector.

Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	+5	5 VDC system power	2	+5	5 VDC system power
3	GND	System Ground	4	GND	System Ground
5			6		
7	D3	Data bit 3	8	D7	Data bit 7
9	D2	Data bit 2	10	D6	Data bit 6
11	D1	Data bit 1	12	D5	Data bit 5
13	D0	Data bit 0	14	D4	Data bit 4
15	A7	Address bit 7	16		
17	A6	Address bit 6	18		
19	A5	Address bit 5	20		
21	A4	Address bit 4	22		
23	A3	Address bit 3	24		
25	A2	Address bit 2	26		
27	A1	Address bit 1	28		
29	A0	Address bit 0	30		
31	WR*	Write	32	RD*	Read
33	IORQ*	Input/Output Request	34		
35	IOEXP*	Input/Output Expand	36		
37			38		
39	M1*	Machine Cycle	40		
41	BUSAK*	Bus Acknowledge	42	BUSRQ*	Bus Request
43	INTAK*	Interrupt Acknowledge	44	INTRQ*	Interrupt Request
45	WAITRQ*	Wait Request	46		
47	SYSRST*	System Reset	48		
49	CLOCK*	System Clock	50		
51	PCO	Priority Chain Out	52	PCI	Priority Chain In
53			54		
55			56		

REFERENCES

System Design Using the Mostek STD-Z80 Bus
--Publication Number 4420237

Mostek 1984/1985 Microelectronic Data Book
--Publication Number 4420479

M/OS-80 Flexible Disk Operating System - Operation Manual
--Publication Number 4420064

CP/M Plus Data Sheet Publication No. 4420642

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-SASI2	SASI2 module (including Technical Manual)	MK77679
	SASI2 Technical Manual only	4420346

PART NUMBER	QTY.	DESCRIPTION	REFERENCE DESIGNATOR
		SCH 450-01132-00	MDX-SASI-2
		FAB 450-01130-10	MDX-SASI-2
		ASSY 450-01130-10	MDX-SASI-2
4150172	22	CAPACITOR 0.1UF, 50V	C1-22
4150140	1	CAPACITOR 15UF, 35V	C23
4150090	1	CAPACITOR, 100PF, 300V	C24
4280155	1	EJECTOR CARD SHORT SL	E1
4210432	1	HEADER, 8PIN, 2X4	J2
4210229	1	CONN HDR, 50POS, ST	J3
4210478	1	HEADER, 3PIN, 1X3	J4
4210087	1	HEADER, 2PIN, 2X1	J5
4210144	1	HEADER, 10PIN, 2X5	J6
4210402	1	HEADER, 4PIN, 1X4	J7
4480011	1	TRANS, 2N3906, PNP, SW	Q1
4470056	1	RESISTOR, 2000HM, ¼W	R1
4470051	1	RESISTOR, 1200HM, ¼W	R2
4470073	1	RESISTOR, 1K, ¼W	R3
4313413	3	IC, TTL, 74LS74	U1, 8, 11
4313078	3	IC, TTL, 7438, QUAD2, INP	U2, 4, 5
4313461	2	IC, TTL, 74LS240, OCT INV	U3,6
4313291	2	IC, TTL, 74LS14, HEX INV	U7, 18
4313411	2	IC, TTL, 74LS32, QUAD2, N	U9, 12
4313501	1	IC, TTL, 74LS27, TRIP3, N	U10
4312026	1	IC, MOS, MK3883N-4, Z80	U13
4313533	1	IC, MOS, MK3881N-4, Z80	U14
4313266	1	IC, TTL, 74S74, DUALD, FF	U15
4313289	1	IC, TTL, 74LS08, QUAD2	U16
4313500	1	IC, TTL, 74LS11, TRIP3	U17
4313412	1	IC, TTL, 74LS38, QUAD2	U19
4313508	2	IC, TTL, 74LS245, OCT	U20, 22
4313507	2	IC, TTL, 74LS244, OCT	U21, 25
4312138	1	IC, TTL, 74LS682, 8BIT	U23
4313562	1	IC, TTL, 74LS243, QUAD	U24
4470415	2	RESISTOR, SIP, 220/230	UR1, 2
4470200	1	RESISTOR, SIP, 10K, 5%	UR3
4470178	1	RESISTOR, SIP, 1K, 5%	UR4
4620019	2	SOCKET, IC, 40PIN, DIP	X13, 14
4210244	5	CONN, JUMPER, MINI	ZZ:

Figure 8. MDX-SASI2 Parts List

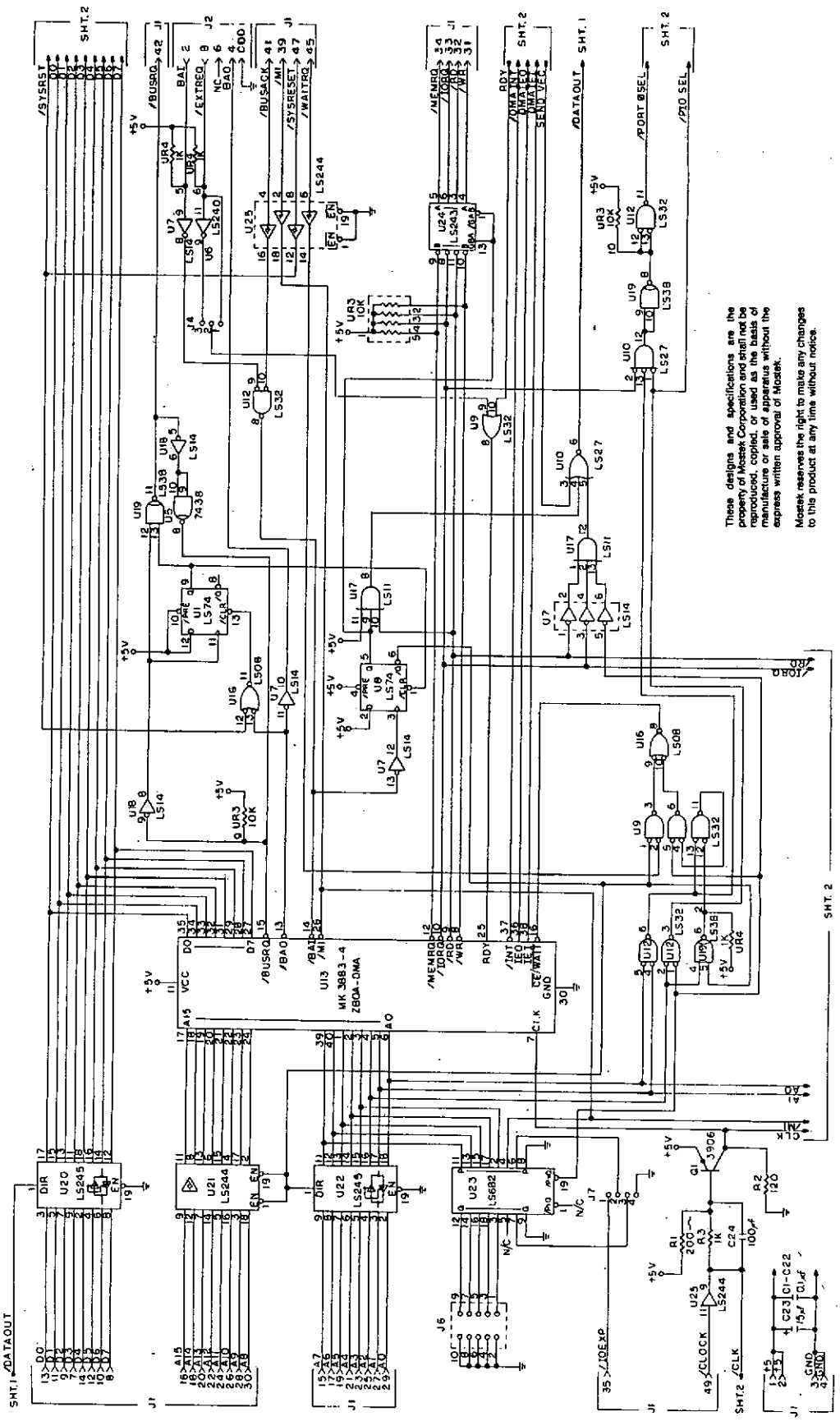


Figure 9. MDX-SASI2 Schematic Diagram (Sheet 1 of 2)

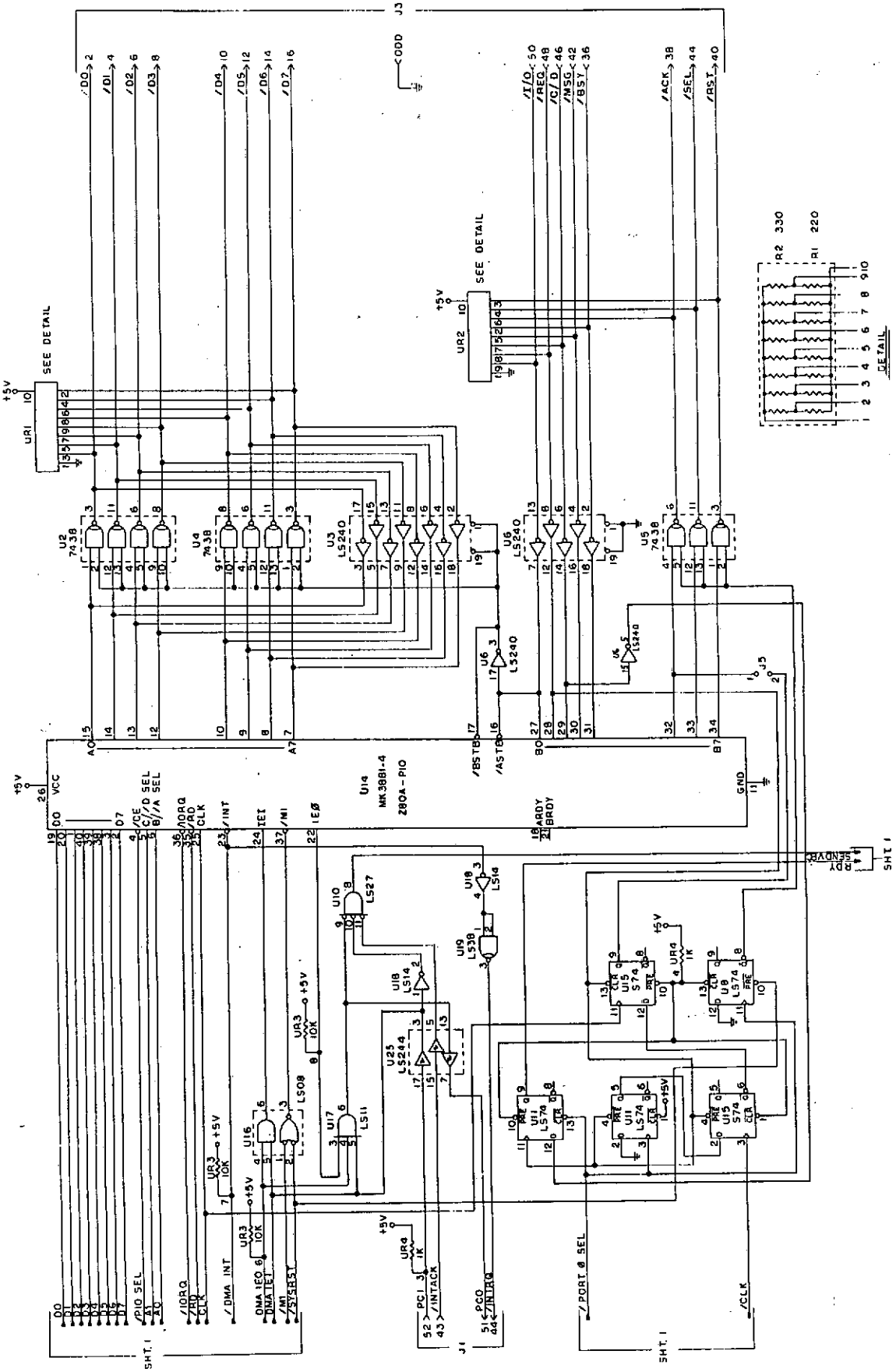


Figure 9. MDX-SASI2 Schematic Diagram (Sheet 2 of 2)

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