DH11

STATIC LOGIC TEST

CZDHAC0

AH-8445C-MC

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MADE IN USA

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SEQ 0001

IDENTIFICATION

PRODUCT CODE: AC-8444C-MC

PRODUCT NAME: CZDHACO DH11 STATIC LOGIC TEST

DATE: MAY 1978

MAINTAINER: DIAGNOSTIC GROUP

AUTHOR: MICHAEL DAVIS

1. ABSTRACT

THE DH11 STATIC LOGIC TEST IS DESIGNED TO PROVIDE A MEANS
FOR TESTING THE CORRECT FUNCTION OF ALL READ/WRITE BITS
IN THE FOLLOWING DH11 REGISTERS:

DH11 SYSTEM CONTROL REGISTER

DH11 LINE PARAMETER REGISTER

DH11 BREAK CONTROL REGISTER

DH11 SILO STATUS REGISTER

IN ADDITION, TESTS ARE PROVIDED TO CHECK THE FUNCTION
OF THOSE BITS THAT ARE READ ONLY IN MAINTENANCE MODE.
ALSO PROVIDED ARE TESTS OF REGISTER ADDRESSABILITY,
AND OF THE FUNCTION OF MASTER CLEAR.

THE DIAGNOSTIC HAS BEEN WRITTEN SO THAT THE TESTING
OF EACH FUNCTION IS CONTAINED IN AN INDIVIDUAL
TEST LOOP.

2. REQUIREMENTS

2.1 EQUIPMENT

PDP-11 FAMILY STANDARD COMPUTER WITH 8KW OF MEMORY
ASR-33 TELETYPE OR EQUIVALENT
DH11 ASYNCHRONOUS MULTIPLEXER
DM11 MAINTENANCE CARD INSTALLED

2.2 STORAGE

THE PROGRAM LOADS INTO 8KW OF MEMORY

3. LOADING PROCEDURE

THE STANDART PROCEDURE FOR LOADING ABSOLUTE BINARY TAPES
IS TO BE USED

4. STARTING PROCEDURE

4.1 CONTROL SWITCH SETTINGS

4.1.1 AFTER PROGRAM LOAD (INITIAL PROGRAM START)

ALL CONSOLE SWITCHES DOWN

4.1.2 TO MODIFY DEVICE VECTOR AND CONTROL REGISTER ADDRESSES
AFTER PROGRAM RESTART

SW00-1

4.1.3 TO START PROGRAM AT SELECTED TEST AFTER PROGRAM RESTART

SW01=1

4.2 STARTING ADDRESS

THE STARTING ADDRESS FOR ALL TESTS IS 000200

THE RESTART ADDRESS FOR ALL TESTS I 0002000

THE STARTING ADDRESS TO ENTER A SELECTED TEST IS 000200

4.3 PROGRAM AND/OR OPERATOR ACTION

4.3.1 INITIAL PROGRAM START

4.3.1.1 LOAD PROGRAM INTO MEMORY
4.3.1.2 LOAD ADDRESS 000200
4.3.1.3 CLEAR CONSOLE SWITCHES
4.3.1.4 PRESS START
4.3.1.5 THE PROGRAM WILL TYPE 'DH11 STATIC LOGIC TEST''
AND WILL THEN TYPE 'VECTOR ADDRESS-'' AND WAIT FOR AN
INPUT FROM THE TELETYPE KEYBOARD.

4.3 (CONT'D)

4.3.1.6 TYPE IN THE ADDRESS OF THE RECEIVER INTERRUPT VECTOR
FOR THE DH11 TO BE TESTED FOLLOWED BY <CARRIAGE RETURN>

NOTE: WORDS IN ANGLE BRACKETS, I.E. <CARRIAGE RETURN> MEAN THAT
THE TELETYPE KEY WITH THE NAMED FUNCTION SHOULD BE STRUCK

IF AN INCORRECT ADDRESS IS ENTERED, THE PROGRAM
WILL TYPE '?' AND WILL REPEAT THE SECOND MESSAGE OF 4.3.1.5
4.3.1.7 THE PROGRAM WILL TYPE 'CONTROL REGISTER ADDRESS-'
AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.1.8 TYPE IN THE ADDRESS OF THE SYSTEM CONTROL REGISTER OF THE
DH11 TO BE TESTED FOLLOWED BY <CARRIAGE RETURN>

IF AN INCORRECT ADDRESS IS TYPED, THE PROGRAM WILL TYPE
'?' AND WILL THEN REPEAT THE MESSAGE OF 4.3.1.7
4.3.1.9 THE PROGRAM WILL TYPE 'R' TO INDICATE THAT IT IS
ABOUT TO START TESTING, AND THEN TESTING WILL BEGIN

4.3.2 PROGRAM RESTART WITH ALL SWITCHES DOWN

4.3.2.1 PERFORM 4.3.1.2 TO 4.3.1.5
4.3.2.2 THE PROGRAM WILL TYPE 'DH11 STATIC LOGIC TEST'
AND WILL THEN CONTINUE AS DESCRIBED IN 4.3.1.9

4.3.3 PROGRAM RESTART WITH SW00=1

4.3.3.1 LOAD ADDRESS 000200
4.3.3.2 SET SW01-1
4.3.3.3 PRESS START
4.3.3.4 THE PROGRAM WILL PERFORM AS DESCRIBED IN 4.3.1.5 TO 4.3.1.9

4.3.4 PROGRAM RESTART WITH SW01 1

4.3.4.1 LOAD ADDRESS 000200
4.3.4.2 SET SW01=1
4.3.4.3 PRESS START
4.3.4.4 THE PROGRAM WILL TYPE 'DH11 STATIC LOGIC TEST'
AND WILL THEN TYPE 'TEST PC-' AND WILL WAIT FOR AN INPUT
FROM THE TELETYPE KEYBOARD
4.3.4.5 TYPE IN THE ADDRESS OF THE TEST AT WHICH THE PROGRAM IS TO
BE STARTED FOLLOWED BY <CARRIAGE RETURN>
4.3.4.6 THE PROGRAM WILL TYPE R TO INDICATE THAT IT HAS STARTED
AND WILL START TESTING AT THE SELECTED TEST.

NOTE: CARE MUST BE TAKEN WHEN THS FEATURE IS USED, SINCE
THERE IS NO PROTECTION AGAINST SELECTING AN ADDRESS THAT
IS IN THE MIDDLE OF A TEST

NOTE: IF IT IS DESIRED TO LOOP ON THE TEST THAT IS SELECTED
SET SW14 1 BEFORE ENTERING THE TEST ADDRESS

5. OPERATING PROCEDURE

5.1 OPERATIONAL SWITCH SETTINGS

SW15=1, HALT ON ERROR
SW14=1, LOOP ON CURRENT TEST
SW13=1, SUPPRESS ERROR TYPEOUT
SW11=1, INHIBIT ITERATIONS
SW10=1, ESCAPE TO NEXT TEST ON ERROR
SW09=1, FREEZE VARIABLE PARAMETER IN CURRENT TEST
SW01=1, START PROGRAM AT SELECTED TEST
SW00=1, CHANGE PARAMETERS AT PROGRAM RESTART

5.2 SUBROUTINE ABSTRACTS

5.2.1 TRAPCATCHER (LOCATIONS 000000-000776)

THIS ROUTINE IS USED TO INTERCEPT UNEXPECTED INTERRUPTS
AND TRAPS. THE AREA FROM 000000-000776 IS LOADED
WITH THE FOLLOWING SEQUENCE

```
2
0
4
0
...
772
0
776
0
```

IF AN UNEXPECTED INTERRUPT OR TRAP OCCURS, THE PROGRAM
WILL HALT WITH THE PC 2 GREATER THAN THE ADDRESS TO
WHICH THE PROGRAM TRAPPED. THE PROCESSOR STACK MAY
BE EXAMINED TO DETERMINE WHERE THE PROGRAM WAS WHEN THE
TRAP OR INTERRUPT OCCURED.

5.2.2 START (PROGRAM INITIALIZATION)

THIS ROUTINE INITIALIZES ALL PROGRAM FLAGS AND COUNTERS,
TYPES THE PROGRAM TITLE MESSAGE, AND INPUTS THE VECTOR
AND CONTROL REGISTER ADDRESSES OF THE DH11 TO BE TESTED.

5.2.3 BEGIN (PROGRAM START AND RESTART)

THIS ROUTINE IS ENTERED IMMEDIATLY AFTER "START"
AND EACH TIME A PROGRAM PASS HAS BEEN COMPLETED.
THE ROUTINE SETS UP THE PROCESSOR STACK AND STATUS WORD
AND THEN TRANSFERS CONTROL TO THE TEST AT WHICH
TESTING WILL BEGIN. IF SW01=0 WHEN THIS ROUTINE IS ENTERD
TESTING WILL START AT T1 (TEST 1). IF SW01=1 WHEN
THIS ROUTINE IS ENTERED, TESTING WILL START AT THE PC
ENTERED FROM THE TELETYPE KEYBOARD.

5.2.4 EOP (END OF PASS)

THIS ROUTINE IS ENTERED ONCE PER PASS AFTER ALL TESTS HAVE BEEN COMPLETED. THIS ROUTINE TYPES THE MAINDEC IDENTIFICATION CODE OF THE PROGRAM, CLEARS ERROR FLAGS AND UPDATES THE PASS COUNT. IF THE PROGRAM WAS LOADED UNDER ACT11 OR DDP, THE ROUTINE CHECKS FOR RETURN TO THE ACT11 OR DDP MONITOR. IF THE PROGRAM IS NOT UNDER MONITOR CONTROL, THE ROUTINE TRANSFERS TO BEGIN.

5.2.5 SCOPER (SCOPE LOOP AND ITERATION HANDLER)

THIS ROUTINE IS ENTERED EACH TIME A TEST IS COMPLETED. THE ROUTINE CHECKS FOR THE FOLLOWING UPON ENTRY
A) IF SW10=1, THE ROUTINE WILL TRANSFER TO THE NEXT TEST IN SEQUENCE, AFTER CLEARING ERROR FLAGS.
B) IF SW11=1, THE ROUTINE WILL TRANSFER TO THE NEXT TEST SEQUENCE, AFTER CLEARING ERROR FLAGS.
C) IF SW14=1, THE ROUTINE WILL LOOP ON THE CURRENT TEST REGARDLESS OF THE ITERATION COUNT.

IF NONE OF THE ABOVE IS TRUE, THE ROUTINE WILL ADD 1 TO THE COUNT OF TEST ITERATIONS, AND COMPARE THIS VALUE TO THE NUMBER OF ITERATIONS THAT SHOULD BE PERFORMED. IF THESE NUMBERS ARE EQUAL, THE ROUTINE WILL TRANSFER TO THE NEXT TEST IN SEQUENCE. THE THE NUMBERS ARE NOT EQUAL, THE TEST CURRENTLY IN PROGRESS WILL BE REPEATED.

5.2.6 SCOP1R (FREEZE ON CURRENT DATA)

THE CALL TO THIS ROUTINE FOLLOWS IMMEDIATLY AFTER THE THE CALL TO THE ERROR HANDLER IN THOSE TESTS THAT HAVE VARIABLE PARAMETERS. THIS ROUTINE IS ALWAYS ENTERED IN THOSE TESTS, WHETHER OR NOT AN ERROR OCCURS.
IF SW09=1, THE ROUTINE WILL TRANSFER CONTROL BACK TO THE TEST AT A POINT WHICH WILL ALLOW REPEATING THE FUNCTION UNDER TEST CONTINUOUSLY WITH THE SAME DATA. IF THIS OPTION IS SELECTED, THE ROUTINE "SCOPER" IS NEVER ENTERED AND ITERATION COUNTS WILL NOT BE UPDATED.

5.2.7 ERRORS (ERROR HANDLER)

THIS ROUTINE IS ENTERED UPON ERROR DETECTION ONLY.
WITH ALL CONSOLE SWITCHES DOWN, THE ROUTINE PROCEDES AS FOLLOWS:
A) THE PC OF THE INSTRUCTION THAT CALLED THE ERROR HANDLER
IS ACCESSED THRU THE STACK, AND THEN THE EMT INSTRUCTION
ITSELF IS FETCHED. THE 8 LSB OF THE EMT
INSTRUCTION ARE THE ERROR CODE. THIS CODE IS
USED TO ACCESS A TABLE OF ERROR MESSAGES AND ERROR
DATA STORAGE LOCATIONS.
B) IF THE TEST THAT FAILED DID NOT FAIL PREVIOUSLY
DURING THIS PASS, A COMPLETE ERROR REPORT IS MADE
IF THE TEST THAT FAILED FAILED MOR THAT ONCE DURING
THE CURRENT PASS, ONLY THE DATA RELATING TO THE FAILUER
IS TYPED. IF SW13=1 NO ERROR TYPEOUT IS MADE.
C) THE ROUTINE NOW CHECKS FOR HALT ON ERROR. IF SW15=1
THE PROGRAM WILL HALT WITH THE PC OF THE CALL TO
THE ERROR ROUTINE IN RC. IF SW15=0, THE PROGRAM WILL
NOT HALT, BUT WILL CHECK FOR ESCAPE TO NEXT TEST.
D) IF SW10=0, THE ROUTINE WILL RETURN
TO THE TEST IN PROGRESS. IF SW10=1, THE ROUTINE WILL
ABORT THE CURRENT TEST, AND TRANSFER TO THE NEXT
TEST IN SEQUENCE, THRU THE ROUTINE ''SCOPEP''.

5.2.8 TRPSRV (TRAP DECODE AND DISPATCH)

THIS ROUTINE DECODES THE 8 LSB OF THE TRAP INSTRUCTION
THAT CAUSED TH PROGRAM INTERRUPT, AND TRANSFERS CONTROL
TO THE ROUTINE THRU THE TABLE ''TRPTAB'' USING THE 8 LSB
OF THE TRAP INSTRUCTION AS AN OFFSET TO THE POINTER TO
THE ROUTINE TO BE ENTERED.

5.3 PROGRAM AND OR OPERATOR ACTION

5.3.1 PROGRAM START WITH ALL SWITCHES DOWN

5.3.1.1 REFER TO SECTIONS 4.3.1 AND 4.3.2 FOR INITIAL PROGRAM BEHAVIOR.

5.3.1.2 AFTER 'R'' HAS BEEN TYPED BY THE PROGRAM, TEST EXECUTION WILL BEGIN. EACH TEST WILL BE REPEATED A SELECTED NUMBER OF ITERATIONS (SEE LISTING FOR EXACT NUMBER FOR EACH TEST) AND THEN THE PROGRAM WILL PROCEED TO THE NEXT TEST.

5.3.1.3 WHEN ALL ITERATIONS HAVE BEEN COMPLETED, THE PROGRAM WILL TYPE ''CZDHA-C'' AND THEN RESTART TESTING AT TEST 1 (LOCATION T1 IN THE PROGRAM).

5.3.1.4 IF AN ERROR OCCURS, THE PROGRAM WILL TYPE AN APPROPRIATE ERROR MESSAGE, AND THEN CONTINUE THE TEST IN PROGRESS.

5.3.2 PROGRAM START WITH SW00=1

THE PROGRAM WILL PERFORM AS DESCRIBED IN 4.3.1 AND 5.3.1

5.3.3 PROGRAM START WITH SW01=1

5.3.3.1 REFER TO SECTION 4.3.4 FOR INITIAL PROGRAM BEHAVIOR

5.3.3.2 TEST EXECUTION WILL START AT THE ADDRESS SPECIFIED AND WILL CONTINUE AS DESCRIBED IN 5.3.1.2

5.3.3.3 AFTER ''CZDHA-C'' HAS BEEN TYPED, THE PROGRAM WILL RESUME TESTING AT TEST 1

5.3.4 PROGRAM OPERATION WITH SW15=1

SAME AS 5.3.1, EXCEPT THAT IN THE CASE OF AN ERROR, THE PROGRAM WILL HALT AFTER THE ERROR TYPEOUT, AND THE PC+2 OF THE CALL TO THE ERROR ROUTINE WILL BE DISPLAYED IN R0.

5.3.5 PROGRAM OPERATION WITH SW13=1

SAME AS 5.3.1 EXCEPT THAT NO ERROR TYPEOUTS WILL OCCUR

5.3.6 PROGRAM OPERATION WITH SW11=1

SAME AS 5.3.1 EXCEPT THAT EACH TEST WILL BE REPEATED ONCE ONLY

5.3.7 PROGRAM OPERATION WITH SW10=1

SAME AS 5.3.1, EXCEPT THAT IN THE CASE OF AN ERROR THE CURRENT TEST WILL BE ABORTED, AND THE PROGRAM WILL PROCEED TO THE NEXT TEST IN SEQUENCE.

5. (CONT'D)

5.3.8 PROGRAM OPERATION WITH SW14=1, OR SW09=1

THESE FUNCTIONS ARE NORMALLY USED FOR TROUBLE SHOOTING.
SEE SECTION 6.3 FOR THEIR USE.

6. ERRORS

6.1 ERROR HALTS

THE ERROR MESSAGE FORMAT FOR ALL ERROR TYPEOUTS
IS AS FOLLOWS

PC+2 MESSAGE
HEADER (IF APPLICABLE)
DATA (IF APPLICABLE)

WHERE
PC+2 IS THE ADDRESS OF THE CALL TO THE ERROR HANDLER + 2
MESSAGE IS AN ASCII MESSAGE DESCRIBING (BRIEFLY) THE FAILURE
HEADER IS A DESCRIPTION OF THE DATA TO FOLLOW
DATA IS OCTAL INFORMATION RELATING TO THE CAUSE OF THE FAILURE
IF THE SAME ERROR OCCURS IN A GIVEN TEST ON THE SAME
PASS, AND IF DATA IS ASSOCIATED WITH THAT ERROR, ONLY
DATA IS TYPE ON SUCCEEDING ERROR TYPEOUTS

IF NO DATA IS ASSOCIATED WITH THE ERROR
THE COMPLETE ERROR MESSAGE IS TYPED.

6.1.1 ERROR DESCRIPTIONS

SEE LISTING FOR DETAILS OF ERRORS

6.2 ERROR RECOVERY

6.2.1 SW15=0

IF THE PROGRAM IS RUN WITH SW15-0, NO OPERATOR ACTION IS
REQUIRED TO CONTINUE TESTING

6.2.2 SW15-1

IF THE PROGRAM IS RUN WITH SW15=1, TO CONTINUE TESTING
AFTER THE PROGRAM HAS HALTED, PRESS THE PROCESSOR
CONSOLE CONTINUE SWITCH

6.3 SCOPE LOOPING

6.3.1 TO SCOPE ON A SPECIFIC TEST, SET SW14=1 AND SW13 1
THIS WILL CAUSE THE PROGRAM TO CONTINUOUSLY LOOP ON THE
SAME TEST, AND WILL CAUSE ALL ERROR TYPEOUTS TO BE INHIBITED

6.3.2 TO SCOPE ON A SPECIFIC VALUE OF A PARAMETER WITHIN
A TEST, SET SW09=1 TO FREEZE THE DATA
(SEE LISTING FOR THOSE TESTS THAT INCORPORATE THIS FEATURE)

6. (CONT'D)

6.3.3 PROGRAM START TO SCOPE LOOP ON SELECTED TEST

PERFORM SECTION 4.3.4 WITH SW14=1

7. RESTRICTIONS

7.1 STARTING

THE DH11 TEST CARD MUST BE INSTALLED

7.2 RUNNING

NONE

8. MISCELLANEOUS

8.1 EXECUTION TIME

THE TIME FOR ONE PASS OF THE PROGRAM (END OF TYPEOUT OF CZDHA-C TO END OF TYPEOUT OF CZDHA-C) IS GIVEN FOR VARIOUS PROCESSORS IN THE TABLE BELOW

PROCESSOR	TIME
PDP-11/05,10	
PDP-11/20	
PDP-11/40	
PDP-11/45	

9. PROGRAM DESCRIPTION

THIS PROGRAM IS A LOW LEVEL TEST OF DH11 CONTROL
REGISTERS.

THE PROGRAM BEGINS BY CHECKING THE ADDRESSABILITY OF
EACH DH11 REGISTER WITHOUT CONCERN FOR ANY DATA CONTENT.
THE PURPOSE OF THESE TESTS IS TO VERFIY THAT THE ADDRESS
SELECTORS FOR THE VARIOUS REGISTERS ARE FUNCTIONING.

THE NEXT SET OF TESTS VERIFIES THAT EACH DH11 REGISTER
CAN BE MASTER CLEARED, AFTER ALL READ/WRITE BITS HAVE
BEEN SET TO 1. THIS TEST DOES NOT VERIFY THAT ALL
BITS HAVE BEEN SET, ONLY THAT THEY HAVE BEEN CLEARED.

THE NEXT GROUP OF TESTS EXERCISES EACH READ/WRITE BIT
IN THE DH11 SYSTEM CONTROL REGISTER, IN BOTH NORMAL AND
MAINTENANCE MODES OF OPERATION. IN NORMAL MODE, EACH
READ/WRITE BIT IS SET AND CLEARED, AND READ ONLY BITS
ARE CHECKED FOR READ ONLY FUNCTION.

IN MAINTENANCE MODE, THE BITS THAT ARE
READ ONLY IN NORMAL MODE ARE CHECKED FOR READ/WRITE OPERATION.

THE NEXT GROUP OF TESTS CHECKS EACH READ/WRITE BIT
OF THE DH11 LINE PARAMATER REGISTER, BREAK CONTROL REGISTER
AND SILO STATUS REGISTER FOR READ/WRITE CAPABILITY. EACH
BIT OF EACH REGISTER IS CHECKED IN AN INDIVIDUAL TEST LOOP.

THE NEXT GROUP OF TESTS CHECKS CLEARING OF A SINGLE
BIT IN EACH OF THE LINE PARAMETER, BREAK CONTROL AND
SILO STATUS REGISTERS WITH ALL OTHER READ/WRITE BITS
SET TO 1.

THE FINAL TWO TESTS VERIFY THAT A MOVE BYTE TO ONE BYTE
OF THE SYSTEM CONTROL REGISTER DOES NOT AFFECT THE OTHER BYTE
OF THE SYSTEM CONTROL REGISTER.

AFTER ALL TESTS HAVE BEEN COMPLETED, THE PROGRAM TYPES
''CZDHA-C'' AND RESTARTS THE SEQUENCE OF TESTING JUST DESCRIBED.

10. LISTING

```
                        ;DH11 STATIC LOGIC TEST
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                                ;STARTING PROCEDURE
                                ;LOAD PROGRAM
                                ;LOAD ADDRESS 000200
                                ;PRESS START
                                ;PROGRAM WILL TYPE DH11 STATIC LOGIC TEST
                                ;PROGRAM WILL TYPE "VECTOR ADDRESS-"
                                ;TYPE IN THE ADDRESS OF THE RECEIVER INTERRUPT VECTOR
                                ;FOR THE DH11 TO BE TESTED, FOLLOWED BY <CARRIAGE RETURN>
                                ;PROGRAM WILL TYPE "CONTROL REGISTER ADDRESS-"
                                ;TYPE IN THE ADDRESS OF THE SYSTEM CONTROL REGISTER
                                ;FOR THE DH11 TO BE TESTED, FOLLOWED BY <CARRIAGE RETURN>
                                ;PROGRAM WILL TYPE "R" TO INDICATE THAT TESTING HAS STARTED
                                ;AT THE END OF A PASS, PROGRAM WILL TYPE " CZDHA-C "
                                ;AND THEN RESUM TESTING


                        ;SWITCH REGISTER OPTIONS

100000                  SW15=100000             ;=1,HALT ON ERROR
040000                  SW14=40000              ;=1,LOOP ON CURRENT TEST
020000                  SW13=20000              ;=1,INHIBIT ERROR TYPEOUT
010000                  SW12=10000
004000                  SW11=4000               ;=1,INHIBIT ITERATIONS
002000                  SW10=2000               ;=1,ESCAPE TO NEXT TEST ON ERROR
001000                  SW09=1000               ;-1,LOOP WITH CURRENT DATA
000400                  SW08=400
000100                  SW06=100
000040                  SW05=40
000020                  SW04=20
000010                  SW03=10
000004                  SW02=4
000002                  SW01=2                          ;RESTART PROGRAM AT SELECTED TEST
000001                  SW00=1                          ;RESELECT VECTOR AND CONTROL REGISTER
                                                        ;ADDRESS AFTER PROGRAM RESTART
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                                ;REGISTER DEFINITIONS

000000                          R0=%0           ;GENERAL REGISTER
000001                          R1=%1           ;GENERAL REGISTER
000002                          R2=%2           ;GENERAL REGISTER
000003                          R3=%3           ;GENERAL REGISTER
000004                          R4=%4           ;GENERAL REGISTER
000005                          R5=%5           ;GENERAL REGISTER
000006                          SP=%6           ;PROCESSOR STACK POINTER
000007                          PC=%7           ;PROGRAM COUNTER

                                ;LOCATION EQUIVALENCIES

177570                          SWR=177570      ;CONSOLE SWITCH REGISTER
177570                          LIGHTS=177570   ;PDP-11/45 DISPLAY REGISTER
177776                          PS=177776       ;PROCESSOR STATUS WORD
021360                          STACK=ENDCOD+200;START OF PROCESSOR STACK

                                ;INSTRUCTION DEFINITIONS

005746                          PUSH1SP=5746    ;DECREMENT PROCESSOR STACK 1 WORD
005726                          POP1SP=5726     ;INCREMENT PROCESSOR STACK 1 WORD
010046                          PUSHR0=10046    ;SAVE R0 ON STACK
012600                          POPR0=12600     ;RESTORE R0 FROM STACK
024646                          PUSH2SP=24646   ;DECREMENT STACK TWICE
022626                          POP2SP=22626    ;INCREMENT STACK TWICE
                                .EQUIV  EMT,HLT ;BASIC DEFINITION OF ERROR CALL


100000                          BIT15=100000
040000                          BIT14=40000
020000                          BIT13=20000
010000                          BIT12=10000
004000                          BIT11=4000
002000                          BIT10=2000
001000                          BIT09=1000
000400                          BIT08=400
000200                          BIT07=200
000100                          BIT06=100
000040                          BIT05=40
000020                          BIT04=20
000010                          BIT03=10
000004                          BIT02=4
000002                          BIT01=2
000001                          BIT00=1
```

```
                                        ;TRAP CATCHER FOR ILLEGAL INTERRUPTS
                        000000  . 0
000000  000002          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000002  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000004  000006          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000006  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000010  000012          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000012  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000014  000016          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000016  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000020  000022          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000022  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000024  000026          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000026  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000030  000032          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000032  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000034  000036          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000036  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000040  000042          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000042  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000044  000046          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000046  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000050  000052          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000052  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000054  000056          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000056  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000060  000062          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000062  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000064  000066          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000066  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000070  000072          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000072  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000074  000076          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000076  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000100  000102          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000102  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000104  000106          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000106  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000110  000112          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000112  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000114  000116          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000116  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000120  000122          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000122  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000124  000126          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000126  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000130  000132          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000132  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000134  000136          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000136  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000140  000142          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000142  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000144  000146          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000146  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000150  000152          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000152  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
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  142  000154  000156                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  143  000156  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  144  000160  000162                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  145  000162  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  146  000164  000166                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  147  000166  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  148  000170  000172                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  149  000172  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  150  000174  000176                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  151  000176  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  152  000200  000202                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  153  000202  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  154  000204  000206                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  155  000206  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  156  000210  000212                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  157  000212  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  158  000214  000216                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  159  000216  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  160  000220  000222                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  161  000222  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  162  000224  000226                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  163  000226  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  164  000230  000232                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  165  000232  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  166  000234  000236                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  167  000236  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  168  000240  000242                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  169  000242  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  170  000244  000246                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  171  000246  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  172  000250  000252                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  173  000252  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  174  000254  000256                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  175  000256  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  176  000260  000262                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  177  000262  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  178  000264  000266                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  179  000266  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  180  000270  000272                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  181  000272  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  182  000274  000276                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  183  000276  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  184  000300  000302                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  185  000302  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  186  000304  000306                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  187  000306  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  188  000310  000312                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  189  000312  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  190  000314  000316                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  191  000316  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  192  000320  000322                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  193  000322  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  194  000324  000326                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  195  000326  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
  196  000330  000332                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
  197  000332  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
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198  000334  000336                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
199  000336  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
200  000340  000342                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
201  000342  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
202  000344  000346                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
203  000346  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
204  000350  000352                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
205  000352  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
206  000354  000356                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
207  000356  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
208  000360  000362                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
209  000362  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
210  000364  000366                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
211  000366  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
212  000370  000372                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
213  000372  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
214  000374  000376                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
215  000376  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
216  000400  000402                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
217  000402  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
218  000404  000406                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
219  000406  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
220  000410  000412                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
221  000412  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
222  000414  000416                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
223  000416  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
224  000420  000422                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
225  000422  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
226  000424  000426                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
227  000426  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
228  000430  000432                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
229  000432  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
230  000434  000436                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
231  000436  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
232  000440  000442                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
233  000442  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
234  000444  000446                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
235  000446  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
236  000450  000452                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
237  000452  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
238  000454  000456                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
239  000456  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
240  000460  000462                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
241  000462  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
242  000464  000466                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
243  000466  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
244  000470  000472                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
245  000472  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
246  000474  000476                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
247  000476  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
248  000500  000502                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
249  000502  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
250  000504  000506                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
251  000506  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
252  000510  000512                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
253  000512  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
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254  000514  000516                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
255  000516  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
256  000520  000522                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
257  000522  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
258  000524  000526                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
259  000526  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
260  000530  000532                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
261  000532  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
262  000534  000536                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
263  000536  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
264  000540  000542                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
265  000542  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
266  000544  000546                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
267  000546  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
268  000550  000552                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
269  000552  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
270  000554  000556                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
271  000556  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
272  000560  000562                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
273  000562  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
274  000564  000566                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
275  000566  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
276  000570  000572                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
277  000572  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
278  000574  000576                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
279  000576  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
280  000600  000602                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
281  000602  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
282  000604  000606                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
283  000606  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
284  000610  000612                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
285  000612  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
286  000614  000616                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
287  000616  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
288  000620  000622                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
289  000622  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
290  000624  000626                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
291  000626  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
292  000630  000632                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
293  000632  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
294  000634  000636                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
295  000636  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
296  000640  000642                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
297  000642  000000                    HALT          EXAMINE STACK TO FIND CAUSE
298  000644  000646                    .+2          ,UNEXPECTED TRAP TO THIS LOCATION
299  000646  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
300  000650  000652                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
301  000652  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
302  000654  000656                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
303  000656  000000                     ALT         ;EXAMINE STACK TO FIND CAUSE
304  000660  000662                      2          ;UNEXPECTED TRAP TO THIS LOCATION
305  000662  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
306  000664  000666                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
307  000666  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
308  000670  000672                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
309  000672  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
```

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 310  000674  000676                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 311  000676  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
 312  000700  000702                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 313  000702  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
 314  000704  000706                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 315  000706  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
 316  000710  000712                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 317  000712  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
 318  000714  000716                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 319  000716  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
 320  000720  000722                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 321  000722  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
 322  000724  000726                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 323  000726  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
 324  000730  000732                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 325  000732  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
 326  000734  000736                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 327  000736  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
 328  000740  000742                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 329  000742  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
 330  000744  000746                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 331  000746  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
 332  000750  000752                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 333  000752  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
 334  000754  000756                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 335  000756  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
 336  000760  000762                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 337  000762  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
 338  000764  000766                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 339  000766  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
 340  000770  000772                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 341  000772  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
 342  000774  000776                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
 343  000776  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
```

```
                                        ;STANDARD INTERRUPT VECTORS


                    000024              .=24
000024  017752                         PFAIL                   ;POWER FAIL HANDLER
000026  000340                         340                     ;SERVICE AT LEVEL 7
000030  016616                         ERRORS                  ;ERROR HANDLER
000032  000340                         340                     ;SERVICE AT LEVEL 7
000034  017020                         TRPSRV                  ;GENERAL HANDLER DISPATCH SERVICE
000036  000340                         340                     ;SERVICE AT LEVEL 7
                    000200              .-200
000200  000167  000574                 JMP     START           ;GO TO START OF PROGRAM


                                        ;DEFINITIONS FOR TRAP SUBROUTINE CALLS
                                        ;POINTERS TO SUBROUTINES CAN BE FOUND STARTING
                                        ;AT LOCATION "TRPTAB"

                    104400              SCOPE=TRAP+Y            ;SCOPE LOOP AND ITERATION HANDLER
                    104401              TYPE=TRAP+Y             ;TELETYPE OUTPUT ROUTINE
                    104402              OCTASC=TRAP+Y           ;OCTAL TO ASCII CONVERSION
                    104403              INSTR=TRAP+Y            ;INPUT ASCII STRING
                    104404              INSTER=TRAP+Y           ;STRING INPUT ERROR
                    104405              PARAM=TRAP+Y            ;CONVERT STRING TO OCTAL, CHECK LIMITS
                    104406              SAV05P=TRAP+Y           ;SAVE R0-R5, PC
                    104407              RES05=TRAP+Y            ;RESTORE R0-R5
                    104410              SCOPE1=TRAP+Y           ;CHECK FOR FREEZE ON CURRENT DATA
                    000046              .-46
000046  016464                         LOGICAL
                    000052              .-52
000052  040000                         40000
```

```
                        001000                  .=1000

                                                ;PROGRAM INITIALIZATION
                                                ;LOCK OUT INTERRUPTS
                                                ;SET UP PROCESSOR STACK
                                                ;SET UP POWER FAIL VECTOR
                                                ;CLEAR PROGRAM FLAGS AND COUNTS
                                                ;TYPE TITLE MESSAGE

001000  012767  000340  176770  START:  MOV     #340,PS                 ;LOCK OUT INTERRUPTS
001006  012706  021360                  MOV     #STACK,SP               ;SET UP PROCESSOR STACK
001012  012737  017752  000024          MOV     #PF IL,@#24             ;SET UP POWER FAIL TRAP
001020  005067  016722                  CLR     STFLG                   ;CLEAR TEST START FLAG
001024  005067  016656                  CLR     PASCNT                  ;CLEAR PASS COUNT
001030  005067  016654                  CLR     ERRCNT                  ;CLEAR ERROR COUNT
001034  005067  016644                  CLR     ERRFLG                  ;CLEAR ERROR FLAG
001040  005067  016640                  CLR     ERRFLG                  ;CLEAR LAST ERROR PC
001044  104401  020116                  TYPE    ,MTITLE                 ;TYPE TITLE MESSAGE
001050  005767  016670                  TST     INIFLG                  ;CHECK INITIALIZATION FLAG
001054  001001                          BNE     VEC1                    ;IF NOT 0, CHECK SWITCHES
                                                                        ;FOR REINITIALIZATION
001056  000404                          BR      VEC2
001060  032767  000001  176502  VEC1:   BIT     #SW00,SWR               ;IF SW00=1, GET NEW VECTOR
001066  001445                          BEQ     BEGIN                   ;AND CSR
001070  012701  000300          VEC2:   MOV     #300,R1
001074  012702  000302                  MOV     #302,R2
001100  012703  000004                  MOV     #4,R3
001104  010211                  1$:     MOV     R2,(R1)                 ;RESTORE TRAPCATCHER
001106  005012                          CLR     (R2)                    ;IN FLOATING VECTOR AREA
001110  060301                          ADD     R3,R1
001112  060302                          ADD     R3,R2
001114  020127  001000                  CMP     R1,#1000
001120  001371                          BNE     1$
001122  104403                          INSTR                           ;INPUT ADDRESS OF DEVICE VECTOR
001124  020153                          MVECTOR                         ;MESSAGE 'VECTOR ADDRESS-''
001126  104405                          PARAM                           ;CONVERT STRING TO OCTAL
001130  000300                          300                             ;LOW LIMIT
001132  000770                          770                             ;HIGH  LIMIT
001134  017674                          DHRVEC                          ;LOCATIONS TO BE FILLED
001136     003                  .BYTE   3                               ;NUMBER OF LOCATIONS
001137     004                  .BYTE   4                               ;LSB MASK
001140  104403                          INSTR                           ;INPUT ADDRESS OF DEVICE CSR
001142  020175                          MREGAD                          ;MESSAGE 'CONTROL REGISTER ADDRESS-''
001144  104405                          PARAM                           ;CONVERT STRING TO OCTAL
001146  000000                          0                               ;LOW LIMIT
001150  177776                          177776                          ;HIGH LIMIT
001152  017652                          DHSLR                           ;LOCATIONS TO BE FILLED
001154     007                  .BYTE   7                               ;NUMBER OF LOCATIONS
001155     010                  .BYTE   10                              ;LSB MASK
001156  016767  016506  016506          MOV     DHSSR,DHSLR             ;SET UP ADDRESS OF SILO
001164  005267  016502                  INC     DHSLR                   ;STATUS REGISTER HIGH BYTE
001170  005767  016550                  TST     INIFLG                  ;IF INITIALIZATION FLAG
001174  001002                          BNE     BEGIN                   ;IS CLEARED
001176  005167  016542                  COM     INIFLG                  ;SET IT

                                        ;PROGRAM START
```

```
 432                                                    ;CHECK FOR PROGRAM START AT SELECTED ADDRESS
 433
 434  001202  012767  000340  176566  BEGIN:  MOV     #340,PS                 ;LOCK OUT INTERRUPTS
 435  001210  012706  021360                  MOV     #STACK,SP               ;SET UP PROCESSOR STACK
 436  001214  032767  000002  176346          BIT     #SW01,SWR               ;IF SW01=1
 437  001222  001410                          BEQ     1$                      ;GET PC FOR PROGRAM START
 438  001224  104403                          INSTR                           ;GET PC
 439  001226  020343                          MTSTPC                          ;MESSAGE 'TEST PC'
 440  001230  104405                          PARAM                           ;CONVERT STRING TO OCTAL
 441  001232  000000                          0
 442  001234  017500                          17500
 443  001236  017712                          RETRN
 444  001240     001                  .BYTE   1
 445  001241     001                  .BYTE   1
 446  001242  000410                          BR      2$
 447  001244  012767  001274  016440  1$:     MOV     #T1,RETRN               ;NORMAL START, TEST 1
 448  001252  005767  016470                  TST     STFLG                   ;IF LOOPING, BYPASS TYPEOUT
 449  001256  001004                          BNE     3$
 450  001260  005167  016462                  COM     STFLG
 451  001264  104401  020337          2$:     TYPE    ,MR                     ;TYPE 'R' TO INDICATE START
 452  001270  000177  016416          3$:     JMP     @RETRN                  ;START TESTING
```

```
                                        ;DH11 SYSTEM CONTROL REGISTER ADDRESSING TEST
                                        ;VERIFY THAT DH11 SYSTEM CONTROL REGISTER RESPONDS TO ADDRESSING
                                        ;IF DH11 SYSTEM CONTROL REGISTER DOES NOT RESPOND, A BUSS ERROR TRAP
                                        ;WILL OCCUR, AND AN ERROR MESSAGE WILL BE TYPED.

001274  012767  000340  176474  T1:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
001302  012767  000100  016410        MOV     #100,ICOUNT             ;SET UP FOR 100 ITERATIONS
001310  012767  001346  016376        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
001316  012737  001340  000004        MOV     #1$,@#4                 ;SET UP TIME OUT TRAP
001324  012737  000340  000006        MOV     #340,@#6
001332  005777  016314                TST     @DHSCR                  ;ADDRESS DH11 SYSTEM CONTROL
                                                                        ;REGISTER
001336  000406                        BR      3$                      ;NO TRAP, REGISTER RESPONDS
                                                                        ;TO ADDRESSING
001340  016705  016306          1$:   MOV     DHSCR,R5                ;REGISTER DID NOT RESPOND
001344  104000                        HLT     0                       ;TIME OUT TRAP, DH11 SYSTEM CONTROL
                                                                        ;REGISTER DID NOT RESPOND
001346  012716  001354          2$:   MOV     #3$,(SP)                ;SET UP TO RETURN FROM TRAP
001352  000002                        RTI                             ;RETURN FROM TRAP
001354  012737  000006  000004  3$:   MOV     #6,@#4
001362  005037  000006                CLR     @#6                     ;RESTORE TRAP CATCHER
001366  104400                        SCOPE                           ;CHECK FOR ITERATIONS, LOOP

                                        ;DH11 NEXT RECEIVED CHARACTER REGISTER ADDRESSING TEST
                                        ;VERIFY THAT DH11 NEXT RECEIVED CHARACTER REGISTER RESPONDS TO ADDRESSING
                                        ;IF DH11 NEXT RECEIVED CHARACTER REGISTER DOES NOT RESPOND, A BUSS ERROR TRAP
                                        ;WILL OCCUR, AND AN ERROR MESSAGE WILL BE TYPED.

001370  012767  000340  176400  T2:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
001376  012767  000100  016314        MOV     #100,ICOUNT             ;SET UP FOR 100 ITERATIONS
001404  012767  001442  016302        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
001412  012737  001434  000004        MOV     #1$,@#4                 ;SET UP TIME OUT TRAP
001420  012737  000340  000006        MOV     #340,@#6
001426  005777  016222                TST     @DHNRC                  ;ADDRESS DH11 NEXT RECEIVED CHARACTER
                                                                        ;REGISTER
001432  000406                        BR      3$                      ;NO TRAP, REGISTER RESPONDS
                                                                        ;TO ADDRESSING
001434  016705  016214          1$:   MOV     DHNRC,R5                ;REGISTER DID NOT RESPOND
001440  104000                        HLT     0                       ;TIME OUT TRAP, DH11 NEXT RECEIVED CHARACTER
                                                                        ;REGISTER DID NOT RESPOND
001442  012716  001450          2$:   MOV     #3$,(SP)                ;SET UP TO RETURN FROM TRAP
001446  000002                        RTI                             ;RETURN FROM TRAP
001450  012737  000006  000004  3$:   MOV     #6,@#4
001456  005037  000006                CLR     @#6                     ;RESTORE TRAP CATCHER
001462  104400                        SCOPE                           ;CHECK FOR ITERATIONS, LOOP

                                        ;DH  11 LINE PARAMETER REGISTER ADDRESSING TEST
                                        ;VERIFY THAT DH  11 LINE PARAMETER REGISTER RESPONDS TO ADDRESSING
                                        ;IF DH  11 LINE PARAMETER REGISTER DOES NOT RESPOND, A BUSS ERROR TRAP
                                        ;WILL OCCUR, AND AN ERROR MESSAGE WILL BE TYPED.

001464  012767  000340  176304  T3:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
001472  012767  000100  016220        MOV     #100,ICOUNT             ;SET UP FOR 100 ITERATIONS
001500  012767  001536  016206        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
001506  012737  001530  000004        MOV     #1$,@#4                 ;SET UP TIME OUT TRAP
```

```
                                MOV     #340,@#6
001522  005777  016130          TST     @DHLPR                  ;ADDRESS DH  11 LINE PARAMETER
                                                                ;REGISTER
001526  000406                  BR      3$                      ;NO TRAP, REGISTER RESPONDS
                                                                ;TO ADDRESSING
001530  016705  016122  1$:     MOV     DHLPR,R5                ;REGISTER DID NOT RESPOND
001534  104000                  HLT     0                       ;TIME OUT TRAP, DH  11 LINE PARAMETER
                                                                ;REGISTER DID NOT RESPOND
001536  012716  001544  2$.     MOV     #3$,(SP)                ;SET UP TO RETURN FROM TRAP
001542  000002                  RTI                             ;RETURN FROM TRAP
001544  012737  000006  000004  3$:     MOV     #6,@#4
001552  005037  000006          CLR     @#6                     ;RESTORE TRAP CATCHER
001556  104400                  SCOPE                           ;CHECK FOR ITERATIONS, LOOP

                                ;DH11 BUS ADDRESS REGISTER ADDRESSING TEST
                                ;VERIFY THAT DH11 BUS ADDRESS REGISTER RESPONDS TO ADDRESSING
                                ;IF DH11 BUS ADDRESS REGISTER DOES NOT RESPOND, A BUSS ERROR TRAP
                                ;WILL OCCUR, AND AN ERROR MESSAGE WILL BE TYPED.

001560  012767  000340  176210  T4:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
001566  012767  000100  016124          MOV     #100,ICOUNT             ;SET UP FOR 100 ITERATIONS
001574  012767  001632  016112          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
001602  012737  001624  000004          MOV     #1$,@#4                 ;SET UP TIME OUT TRAP
001610  012737  000340  000006          MOV     #340,@#6
001616  005777  016036                  TST     @DHBA                   ;ADDRESS DH11 BUS ADDRESS
                                                                        ;REGISTER
001622  000406                          BR      3$                      ;NO TRAP, REGISTER RESPONDS
                                                                        ;TO ADDRESSING
001624  016705  016030          1$:     MOV     DHBA,R5         ;REGISTER DID NOT RESPOND
001630  104000                          HLT     0                       ;TIME OUT TRAP, DH11 BUS ADDRESS
                                                                        ;REGISTER DID NOT RESPOND
001632  012716  001640          2$:     MOV     #3$,(SP)                ;SET UP TO RETURN FROM TRAP
001636  000002                          RTI                             ;RETURN FROM TRAP
001640  012737  000006  000004  3$:     MOV     #6,@#4
001646  005037  000006                  CLR     @#6                     ;RESTORE TRAP CATCHER
001652  104400                          SCOPE                           ;CHECK FOR ITERATIONS, LOOP

                                ;DH11 BYTE COUNT REGISTER ADDRESSING TEST
                                ;VERIFY THAT DH11 BYTE COUNT REGISTER RESPONDS TO ADDRESSING
                                ;IF DH11 BYTE COUNT REGISTER DOES NOT RESPOND, A BUSS ERROR TRAP
                                ;WILL OCCUR, AND AN ERROP MESSAGE WILL BE TYPED.

001654  012767  000340  176114  T5:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
001662  012767  000100  016030          MOV     #100,ICOUNT             ;SET UP FOR 100 ITERATIONS
001670  012767  001726  016016          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
001676  012737  001720  000004          MOV     #1$,@#4                 ;SET UP TIME OUT TRAP
001704  012737  000340  000006          MOV     #340,@#6
001712  005777  015744                  TST     @DHBC                   ;ADDRESS DH11 BYTE COUNT
                                                                        ;REGISTER
001716  000406                          BR      3$                      ;NO TRAP, REGISTER RESPONDS
                                                                        ;TO ADDRESSING
001720  016705  015736          1$:     MOV     DHBC,R5         ;REGISTER DID NOT RESPOND
001724  104000                          HLT     0                       ;TIME OUT TRAP, DH11 BYTE COUNT
                                                                        ;REGISTER DID NOT RESPOND
001726  012716  001734          2$:     MOV     #3$,(SP)                ;SET UP TO RETURN FROM TRAP
001732  000002                          RTI                             ;RETURN FROM TRAP
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                                        ;DH11 BREAK CONTROL REGISTER ADDRESSING TEST
                                        ;VERIFY THAT DH11 BREAK CONTROL REGISTER RESPONDS TO ADDRESSING
                                        ;IF DH11 BREAK CONTROL REGISTER DOES NOT RESPOND, A BUSS ERROR TRAP
                                        ;WILL OCCUR, AND AN ERROR MESSAGE WILL BE TYPED.

001750  012767  000340  176020  T6:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
001756  012767  000100  015734        MOV     #100,ICOUNT             ;SET UP FOR 100 ITERATIONS
001764  012767  002022  015722        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
001772  012737  002014  000004        MOV     #1$,@#4                 ;SET UP TIME OUT TRAP
002000  012737  000340  000006        MOV     #340,@#6
002006  005777  015654                TST     @DHBCR                  ;ADDRESS DH11 BREAK CONTROL
                                                                      ;REGISTER
002012  000406                        BR      3$                      ;NO TRAP, REGISTER RESPONDS
                                                                      ;TO ADDRESSING
002014  016705  015646        1$:     MOV     DHBCR,R5                ;REGISTER DID NOT RESPOND
002020  104000                        HLT     0                       ;TIME OUT TRAP, DH11 BREAK CONTROL
                                                                      ;REGISTER DID NOT RESPOND
002022  012716  002030        2$:     MOV     #3$,(SP)                ;SET UP TO RETURN FROM TRAP
002026  000002                        RTI                             ;RETURN FROM TRAP
002030  012737  000006  000004  3$:   MOV     #6,@#4
002036  005037  000006                CLR     @#6                     ;RESTORE TRAP CATCHER
002042  104400                        SCOPE                           ;CHECK FOR ITERATIONS, LOOP

                                        ;BUS ACTIVE REGISTER ADDRESSING TEST
                                        ;VERIFY THAT BUS ACTIVE REGISTER RESPONDS TO ADDRESSING
                                        ;IF BUS ACTIVE REGISTER DOES NOT RESPOND, A BUSS ERROR TRAP
                                        ;WILL OCCUR, AND AN ERROR MESSAGE WILL BE TYPED.

002044  012767  000340  175724  T7:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
002052  012767  000100  015640        MOV     #100,ICOUNT             ;SET UP FOR 100 ITERATIONS
002060  012767  002116  015626        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
002066  012737  002110  000004        MOV     #1$,@#4                 ;SET UP TIME OUT TRAP
002074  012737  000340  000006        MOV     #340,@#6
002102  005777  015556                TST     @DHBAR                  ;ADDRESS BUS ACTIVE
                                                                      ;REGISTER
002106  000406                        BR      3$                      ;NO TRAP, REGISTER RESPONDS
                                                                      ;TO ADDRESSING
002110  016705  015550        1$:     MOV     DHBAR,R5                ;REGISTER DID NOT RESPOND
002114  104000                        HLT     0                       ;TIME OUT TRAP, BUS ACTIVE
                                                                      ;REGISTER DID NOT RESPOND
002116  012716  002124        2$:     MOV     #3$,(SP)                ;SET UP TO RETURN FROM TRAP
002122  000002                        RTI                             ;RETURN FROM TRAP
002124  012737  000006  000004  3$:   MOV     #6,@#4
002132  005037  000006                CLR     @#6                     ;RESTORE TRAP CATCHER
002136  104400                        SCOPE                           ;CHECK FOR ITERATIONS, LOOP

                                        ;SILO STATUS REGISTER ADDRESSING TEST
                                        ;VERIFY THAT SILO STATUS REGISTER RESPONDS TO ADDRESSING
                                        ;IF SILO STATUS REGISTER DOES NOT RESPOND, A BUSS ERROR TRAP
                                        ;WILL OCCUR, AND AN ERROR MESSAGE WILL BE TYPED.

002140  012767  000340  175630  T10:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
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                                                    ;SET UP FOR 100 ITERATIONS
                                                    ;SET UP TO ESCAPE TO NEXT TEST
                                                    ;SET UP TIME OUT TRAP
                                                    ;ADDRESS SILO STATUS
                                                            ;REGISTER
                                                    ;NO TRAP, REGISTER RESPONDS
                                                    ;TO ADDRESSING
                                                    ;REGISTER DID NOT RESPOND
                                                    ;TIME OUT TRAP, SILO STATUS
                                                    ;REGISTER DID NOT RESPOND
                                                    ;SET UP TO RETURN FROM TRAP
                                                    ;RETURN FROM TRAP
                                                    ;RESTORE TRAP CATCHER
                                                    ;CHECK FOR ITERATIONS, LOOP

                                                    ;MASTER CLEAR TEST
                                                    ;SET SYSTEM CONTROL REGISTER TO 'CDATA'
                                                    ;ISSUE MASTER CLEAR
                                                    ;VERIFY THAT SYSTEM CONTPOL WAS CLEARED

                                                    ;DISABLE ALL INTERRUPTS
                                                    ;SET UP FOR 4000 ITERATIONS
                                                    ;SET UP TO ESCAPE TO NEXT TEST
                                                    ;SET SYSTEM CONTROL REGISTER
                                                    ;TO 173777
                                                    ;ISSUE MASTER CLEAR
                                                    ;(R4)=ACTUAL DATA IN
                                                    ;SYSTEM CONTROL REGISTER
                                                            ;VERIFY THAT SYSTEM CONTROL REGISTER
                                                    ;WAS CLEARED

                                                    ;(R5)=EXPECTED DATA IN
                                                    ;SYSTEM CONTROL REGISTER, 0
                                                            ;GET REGISTER ADDRESS
                                                    ;MASTER CLEAR FAILED
                                                    ;CHECK FOR ITERATIONS, LOOP

                                                    ;MASTER CLEAR TEST
                                                    ;SET LINE PARAMETER REGISTER TO 'CDATA'
                                                    ;ISSUE MASTER CLEAR
                                                    ;VERIFY THAT LINE PARAMETER WAS CLEARED

                                                    ;DISABLE ALL INTERRUPTS
                                                    ;SET UP FOR 4000 ITERATIONS
                                                    ;SET UP TO ESCAPE TO NEXT TEST
                                                    ;SET LINE PARAMETER REGISTER
                                                    ;TO 177777
                                                    ;ISSUE MASTER CLEAR
                                                    ;(R4)=ACTUAL DATA IN
                                                    ;LINE PARAMETER REGISTER
                                                            ;VERIFY THAT LINE PARAMETER REGISTER
                                                    ;WAS CLEARED
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                                        CLR     R5                      ;(R5)=EXPECTED DATA IN
                                                                        ;LINE PARAMETER REGISTER, 0
002364  016703  015266                  MOV     DHLPR,R3                        ;GET REGISTER ADDRESS
002370  104005                          HLT     5                       ;MASTER CLEAR FAILED
002372  104400                  1$:     SCOPE                           ;CHECK FOR ITERATIONS, LOOP

                                        ;MASTER CLEAR TEST
                                        ;SET BREAK CONTROL REGISTER TO 'CDATA'
                                        ;ISSUE MASTER CLEAR
                                        ;VERIFY THAT BREAK CONTROL WAS CLEARED

002374  012767  000340  175374  T13:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
002402  012767  004000  015310          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
002410  012767  002452  015276          MOV     #1$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
002416  012777  177777  015242          MOV     #177777,@DHBCR          ;SET BREAK CONTROL REGISTER
                                                                        ;TO 177777
002424  052777  004000  015220          BIS     #BIT11,@DHSCR           ;ISSUE MASTER CLEAR
002432  017704  015230                  MOV     @DHBCR,R4               ;(R4)=ACTUAL DATA IN
                                                                        ;BREAK CONTROL REGISTER
002436  005704                          TST     R4                              ;VERIFY THAT BREAK CONTROL REGISTER
                                                                        ;WAS CLEARED
002440  001404                          BEQ     1$
002442  005005                          CLR     R5                      ;(R5)=EXPECTED DATA IN
                                                                        ;BREAK CONTROL REGISTER, 0
002444  016703  015216                  MOV     DHBCR,R3                        ;GET REGISTER ADDRESS
002450  104005                          HLT     5                       ;MASTER CLEAR FAILED
002452  104400                  1$:     SCOPE                           ;CHECK FOR ITERATIONS, LOOP

                                        ;MASTER CLEAR TEST
                                        ;SET SILO STATUS REGISTER TO 'CDATA'
                                        ;ISSUE MASTER CLEAR
                                        ;VERIFY THAT SILO STATUS WAS CLEARED

002454  012767  000340  175314  T14:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
002462  012767  004000  015230          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
002470  012767  002536  015216          MOV     #1$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
002476  012777  100077  015164          MOV     #100077,@DHSSR          ;SET SILO STATUS REGISTER
                                                                        ;TO 100077
002504  052777  004000  015140          BIS     #BIT11,@DHSCR           ;ISSUE MASTER CLEAR
002512  017704  015152                  MOV     @DHSSR,R4               ;(R4)=ACTUAL DATA IN
                                                                        ;SILO STATUS REGISTER
002516  042704  077700                  BIC     #77700,R4                       ;CLEAR UNWANTED BITS
002522  005704                          TST     R4                              ;VERIFY THAT SILO STATUS REGISTER
                                                                        ;WAS CLEARED
002524  001404                          BEQ     1$
002526  005005                          CLR     R5                      ;(R5)=EXPECTED DATA IN
                                                                        ;SILO STATUS REGISTER, 0
002530  016703  015134                  MOV     DHSSR,R3                        ;GET REGISTER ADDRESS
002534  104005                          HLT     5                       ;MASTER CLEAR FAILED
002536  104400                  1$:     SCOPE                           ;CHECK FOR ITERATIONS, LOOP

                                        ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
                                        ;SET LINE SELECT BIT 0 IN SYSTEM CONTROL REGISTER
                                        ;VERIFY THAT LINE SELECT BIT 0 WAS SET
                                        ;CLEAR LINE SELECT BIT 0
                                        ;VERIFY THAT LINE SELECT BIT 0 WAS CLEARED
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002540  012767  000340  175230  T15:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
002546  012767  004000  015144          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
002554  012767  002624  015132          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
002562  016703  015064                  MOV     DHSCR,R3                ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
002566  012713  000001                  MOV     #BIT00,(R3)             ;SET LINE SELECT BIT 0
002572  022713  000001                  CMP     #BIT00,(R3)             ;VERIFY THAT LINE SELECT BIT 0 WAS SET
002576  001404                          BEQ     1$
002600  012705  000001                  MOV     #BIT00,R5               ;(R5)= EXPECTED VALUE
                                                                        ;IN SYSTEM CONTROL REGISTER
                                                                        ;LINE SELECT BIT 0
002604  011304                          MOV     (R3),R4                 ;(R4)=ACTUAL DATA IN
                                                                        ;SYSTEM CONTROL REGISTER
002606  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
                                                                        ;WRITE/READ ERROR
002610  042713  000001          1$:     BIC     #BIT00,(R3)             ;CLEAR LINE SELECT BIT 0
002614  001403                          BEQ     2$
002616  005005                          CLR     R5                      ;(R5)=EXPECTED DATA IN
                                                                        ;SYSTEM CONTROL REGISTER, 0
002620  011304                          MOV     (R3),R4                 ;(R4)=ACTUAL DATA IN
                                                                        ;SYSTEM CONTROL REGISTER
002622  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
                                                                        ;WRITE/READ ERROR
002624  104400                  2$:     SCOPE                           ;CHECK FOR ITERATIONS, LOOP

                                        ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
                                        ;SET LINE SELECT BIT 1 IN SYSTEM CONTROL REGISTER
                                        ;VERIFY THAT LINE SELECT BIT 1 WAS SET
                                        ;CLEAR LINE SELECT BIT 1
                                        ;VERITY THAT LINE SELECT BIT 1 WAS CLEARED

002626  012767  000340  175142  T16:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
002634  012767  004000  015056          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
002642  012767  002712  015044          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
002650  016703  014776                  MOV     DHSCR,R3                ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
002654  012713  000002                  MOV     #BIT01,(R3)             ;SET LINE SELECT BIT 1
002660  022713  000002                  CMP     #BIT01,(R3)             ;VERIFY THAT LINE SELECT BIT 1 WAS SET
002664  001404                          BEQ     1$
002666  012705  000002                  MOV     #BIT01,R5               ;(R5)= EXPECTED VALUE
                                                                        ;IN SYSTEM CONTROL REGISTER
                                                                        ;LINE SELECT BIT 1
002672  011304                          MOV     (R3),R4                 ;(R4)=ACTUAL DATA IN
                                                                        ;SYSTEM CONTROL REGISTER
002674  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
                                                                        ;WRITE/READ ERROR
002676  042713  000002          1$:     BIC     #BIT01,(R3)             ;CLEAR LINE SELECT BIT 1
002702  001403                          BEQ     2$
002704  005005                          CLR     R5                      ;(R5)=EXPECTED DATA IN
                                                                        ;SYSTEM CONTROL REGISTER, 0
002706  011304                          MOV     (R3),R4                 ;(R4)=ACTUAL DATA IN
                                                                        ;SYSTEM CONTROL REGISTER
002710  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
                                                                        ;WRITE/READ ERROR
002712  104400                  2$:     SCOPE                           ;CHECK FOR ITERATIONS, LOOP

                                        ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
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                                        ;SET LINE SELECT BIT 2 IN SYSTEM CONTROL REGISTER
                                        ;VERIFY THAT LINE SELECT BIT 2 WAS SET
                                        ;CLEAR LINE SELECT BIT 2
                                        ;VERITY THAT LINE SELECT BIT 2 WAS CLEARED

002714  012767  000340  175054  T17:  MOV   #340,PS          ;DISABLE ALL INTERRUPTS
002722  012767  004000  014770        MOV   #4000,ICOUNT     ;SET UP FOR 4000 ITERATIONS
002730  012767  003000  014756        MOV   #2$,ESCAPE       ;SET UP TO ESCAPE TO NEXT TEST
002736  016703  014710                MOV   DHSCR,R3         ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
002742  012713  000004                MOV   #BIT02,(R3)      ;SET LINE SELECT BIT 2
002746  022713  000004                CMP   #BIT02,(R3)      ;VERIFY THAT LINE SELECT BIT 2 WAS SET
002752  001404                        BEQ   1$
002754  012705  000004                MOV   #BIT02,R5        ;(R5)= EXPECTED VALUE
                                                            ;IN SYSTEM CONTROL REGISTER
                                                            ;LINE SELECT BIT 2
002760  011304                        MOV   (R3),R4          ;(R4)=ACTUAL DATA IN
                                                            ;SYSTEM CONTROL REGISTER
002762  104001                        HLT   1                ;SYSTEM CONTROL REGISTER
                                                            ;WRITE/READ ERROR
002764  042713  000004          1$:   BIC   #BIT02,(R3)      ;CLEAR LINE SELECT BIT 2
002770  001403                        BEQ   2$
002772  005005                        CLR   R5               ;(R5)=EXPECTED DATA IN
                                                            ;SYSTEM CONTROL REGISTER, 0
002774  011304                        MOV   (R3),R4          ;(R4)=ACTUAL DATA IN
                                                            ;SYSTEM CONTROL REGISTER
002776  104001                        HLT   1                ;SYSTEM CONTROL REGISTER
                                                            ;WRITE/READ ERROR
003000  104400                  2$:   SCOPE                  ;CHECK FOR ITERATIONS, LOOP

                                        ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
                                        ;SET LINE SELECT BIT 3 IN SYSTEM CONTROL REGISTER
                                        ;VERIFY THAT LINE SELECT BIT 3 WAS SET
                                        ;CLEAR LINE SELECT BIT 3
                                        ;VERITY THAT LINE SELECT BIT 3 WAS CLEARED

003002  012767  000340  174766  T20:  MOV   #340,PS          ;DISABLE ALL INTERRUPTS
003010  012767  004000  014702        MOV   #4000,ICOUNT     ;SET UP FOR 4000 ITERATIONS
003016  012767  003066  014670        MOV   #2$,ESCAPE       ;SET UP TO ESCAPE TO NEXT TEST
003024  016703  014622                MOV   DHSCR,R3         ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
003030  012713  000010                MOV   #BIT03,(R3)      ;SET LINE SELECT BIT 3
003034  022713  000010                CMP   #BIT03,(R3)      ;VERIFY THAT LINE SELECT BIT 3 WAS SET
003040  001404                        BEQ   1$
003042  012705  000010                MOV   #BIT03,R5        ;(R5)= EXPECTED VALUE
                                                            ;IN SYSTEM CONTROL REGISTER
                                                            ;LINE SELECT BIT 3
003046  011304                        MOV   (R3),R4          ;(R4)=ACTUAL DATA IN
                                                            ;SYSTEM CONTROL REGISTER
003050  104001                        HLT   1                ;SYSTEM CONTROL REGISTER
                                                            ;WRITE/READ ERROR
003052  042713  000010          1$:   BIC   #BIT03,(R3)      ;CLEAR LINE SELECT BIT 3
003056  001403                        BEQ   2$
003060  005005                        CLR   R5               ;(R5)=EXPECTED DATA IN
                                                            ;SYSTEM CONTROL REGISTER, 0
003062  011304                        MOV   (R3),R4          ;(R4)=ACTUAL DATA IN
                                                            ;SYSTEM CONTROL REGISTER
003064  104001                        HLT   1                ;SYSTEM CONTROL REGISTER
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                                                        ;WRITE/READ ERROR
003066  104400                2$:     SCOPE           ;CHECK FOR ITERATIONS, LOOP

                        ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
                        ;SET MEMORY EXTENSION BIT 0 IN SYSTEM CONTROL REGISTER
                        ;VERIFY THAT MEMORY EXTENSION BIT 0 WAS SET
                        ;CLEAR MEMORY EXTENSION BIT 0
                        ;VERITY THAT MEMORY EXTENSION BIT 0 WAS CLEARED

003070  012767  000340  174700  T21:   MOV     #340,PS         ;DISABLE ALL INTERRUPTS
003076  012767  004000  014614        MOV     #4000,ICOUNT    ;SET UP FOR 4000 ITERATIONS
003104  012767  003154  014602        MOV     #2$,ESCAPE      ;SET UP TO ESCAPE TO NEXT TEST
003112  016703  014534                MOV     DHSCR,R3        ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
003116  012713  000020                MOV     #BIT04,(R3)     ;SET MEMORY EXTENSION BIT 0
003122  022713  000020                CMP     #BIT04,(R3)     ;VERIFY THAT MEMORY EXTENSION BIT 0 WAS SET
003126  001404                        BEQ     1$
003130  012705  000020                MOV     #BIT04,R5       ;(R5)= EXPECTED VALUE
                                                        ;IN SYSTEM CONTROL REGISTER
                                                        ;MEMORY EXTENSION BIT 0
003134  011304                        MOV     (R3),R4         ;(R4)=ACTUAL DATA IN
                                                        ;SYSTEM CONTROL REGISTER
003136  104001                        HLT     1               ;SYSTEM CONTROL REGISTER
                                                        ;WRITE/READ ERROR
003140  042713  000020        1$:     BIC     #BIT04,(R3)     ;CLEAR MEMORY EXTENSION BIT 0
003144  001403                        BEQ     2$
003146  005005                        CLR     R5              ;(R5)=EXPECTED DATA IN
                                                        ;SYSTEM CONTROL REGISTER, 0
003150  011304                        MOV     (R3),R4         ;(R4)=ACTUAL DATA IN
                                                        ;SYSTEM CONTROL REGISTER
003152  104001                        HLT     1               ;SYSTEM CONTROL REGISTER
                                                        ;WRITE/READ ERROR
003154  104400                2$:     SCOPE           ;CHECK FOR ITERATIONS, LOOP

                        ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
                        ;SET MEMORY EXTENSION BIT 1 IN SYSTEM CONTROL REGISTER
                        ;VERIFY THAT MEMORY EXTENSION BIT 1 WAS SET
                        ;CLEAR MEMORY EXTENSION BIT 1
                        ;VERITY THAT MEMORY EXTENSION BIT 1 WAS CLEARED

003156  012767  000340  174612  T22:   MOV     #340,PS         ;DISABLE ALL INTERRUPTS
003164  012767  004000  014526        MOV     #4000,ICOUNT    ;SET UP FOR 4000 ITERATIONS
003172  012767  003242  014514        MOV     #2$,ESCAPE      ;SET UP TO ESCAPE TO NEXT TEST
003200  016703  014446                MOV     DHSCR,R3        ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
003204  012713  000040                MOV     #BIT05,(R3)     ;SET MEMORY EXTENSION BIT 1
003210  022713  000040                CMP     #BIT05,(R3)     ;VERIFY THAT MEMORY EXTENSION BIT 1 WAS SET
003214  001404                        BEQ     1$
003216  012705  000040                MOV     #BIT05,R5       ;(R5)= EXPECTED VALUE
                                                        ;IN SYSTEM CONTROL REGISTER
                                                        ;MEMORY EXTENSION BIT 1
003222  011304                        MOV     (R3),R4         ;(R4)=ACTUAL DATA IN
                                                        ;SYSTEM CONTROL REGISTER
003224  104001                        HLT     1               ;SYSTEM CONTROL REGISTER
                                                        ;WRITE/READ ERROR
003226  042713  000040        1$:     BIC     #BIT05,(R3)     ;CLEAR MEMORY EXTENSION BIT 1
003232  001403                        BEQ     2$
003234  005005                        CLR     R5              ;(R5)=EXPECTED DATA IN
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                                                        ;SYSTEM CONTROL REGISTER, 0
003236  011304                          MOV     (R3),R4 ;(R4)=ACTUAL DATA IN
                                                        ;SYSTEM CONTROL REGISTER
003240  104001                          HLT     1       ;SYSTEM CONTROL REGISTER
                                                        ;WRITE/READ ERROR
003242  104400                  2$:     SCOPE           ;CHECK FOR ITERATIONS, LOOP

                                ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
                                ;SET RECEIVER INTERRUPT ENABLE IN SYSTEM CONTROL REGISTER
                                ;VERIFY THAT RECEIVER INTERRUPT ENABLE WAS SET
                                ;CLEAR RECEIVER INTERRUPT ENABLE
                                ;VERITY THAT RECEIVER INTERRUPT ENABLE WAS CLEARED

003244  012767  000340  174524  T23:    MOV     #340,PS         ;DISABLE ALL INTERRUPTS
003252  012767  004000  014440          MOV     #4000,ICOUNT    ;SET UP FOR 4000 ITERATIONS
003260  012767  003330  014426          MOV     #2$,ESCAPE      ;SET UP TO ESCAPE TO NEXT TEST
003266  016703  014360                  MOV     DHSCR,R3        ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
003272  012713  000100                  MOV     #BIT06,(R3)     ;SET RECEIVER INTERRUPT ENABLE
003276  022713  000100                  CMP     #BIT06,(R3)     ;VERIFY THAT RECEIVER INTERRUPT ENABLE WAS SET
003302  001404                          BEQ     1$
003304  012705  000100                  MOV     #BIT06,R5       ;(R5)= EXPECTED VALUE
                                                                ;IN SYSTEM CONTROL REGISTER
                                                                ;RECEIVER INTERRUPT ENABLE
003310  011304                          MOV     (R3),R4         ;(R4)=ACTUAL DATA IN
                                                                ;SYSTEM CONTROL REGISTER
003312  104001                          HLT     1               ;SYSTEM CONTROL REGISTER
                                                                ;WRITE/READ ERROR
003314  042713  000100          1$:     BIC     #BIT06,(R3)     ;CLEAR RECEIVER INTERRUPT ENABLE
003320  001403                          BEQ     2$
003322  005005                          CLR     R5              ;(R5)=EXPECTED DATA IN
                                                                ;SYSTEM CONTROL REGISTER, 0
003324  011304                          MOV     (R3),R4         ;(R4)=ACTUAL DATA IN
                                                                ;SYSTEM CONTROL REGISTER
003326  104001                          HLT     1               ;SYSTEM CONTROL REGISTER
                                                                ;WRITE/READ ERROR
003330  104400                  2$:     SCOPE                   ;CHECK FOR ITERATIONS, LOOP

                                ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
                                ;SET MAINTENANCE MODE IN SYSTEM CONTROL REGISTER
                                ;VERIFY THAT MAINTENANCE MODE WAS SET
                                ;CLEAR MAINTENANCE MODE
                                ;VERITY THAT MAINTENANCE MODE WAS CLEARED

003332  012767  000340  174436  T24:    MOV     #340,PS         ;DISABLE ALL INTERRUPTS
003340  012767  004000  014352          MOV     #4000,ICOUNT    ;SET UP FOR 4000 ITERATIONS
003346  012767  003416  014340          MOV     #2$,ESCAPE      ;SET UP TO ESCAPE TO NEXT TEST
003354  016703  014272                  MOV     DHSCR,R3        ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
003360  012713  001000                  MOV     #BIT09,(R3)     ;SET MAINTENANCE MODE
003364  022713  001000                  CMP     #BIT09,(R3)     ;VERIFY THAT MAINTENANCE MODE WAS SET
003370  001404                          BEQ     1$
003372  012705  001000                  MOV     #BIT09,R5       ;(R5)= EXPECTED VALUE
                                                                ;IN SYSTEM CONTROL REGISTER
                                                                ;MAINTENANCE MODE
003376  011304                          MOV     (R3),R4         ;(R4)=ACTUAL DATA IN
                                                                ;SYSTEM CONTROL REGISTER
003400  104001                          HLT     1               ;SYSTEM CONTROL REGISTER
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                                                        ;WRITE/READ ERROR
003402  042713  001000        1$:     BIC     #BIT09,(R3)     ;CLEAR MAINTENANCE MODE
003406  001403                        BEQ     2$
003410  005005                        CLR     R5              ;(R5)=EXPECTED DATA IN
                                                        ;SYSTEM CONTROL REGISTER, 0
003412  011304                        MOV     (R3),R4         ;(R4)=ACTUAL DATA IN
                                                        ;SYSTEM CONTROL REGISTER
003414  104001                        HLT     1               ;SYSTEM CONTROL REGISTER
                                                        ;WRITE/READ ERROR
003416  104400              2$:     SCOPE                   ;CHECK FOR ITERATIONS, LOOP

                        ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
                        ;SET SILO OVERFLOW INTERRUPT ENABLE IN SYSTEM CONTROL REGISTER
                        ;VERIFY THAT SILO OVERFLOW INTERRUPT ENABLE WAS SET
                        ;CLEAR SILO OVERFLOW INTERRUPT ENABLE
                        ;VERITY THAT SILO OVERFLOW INTERRUPT ENABLE WAS CLEARED

003420  012767  000340  174350  T25:    MOV     #340,PS         ;DISABLE ALL INTERRUPTS
003426  012767  004000  014264          MOV     #4000,ICOUNT    ;SET UP FOR 4000 ITERATIONS
003434  012767  003504  014252          MOV     #2$,ESCAPE      ;SET UP TO ESCAPE TO NEXT TEST
003442  016703  014204                  MOV     DHSCR,R3        ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
003446  012713  010000                  MOV     #BIT12,(R3)     ;SET SILO OVERFLOW INTERRUPT ENABLE
003452  022713  010000                  CMP     #BIT12,(R3)     ;VERIFY THAT SILO OVERFLOW INTERRUPT ENABLE WAS
003456  001404                        BEQ     1$
003460  012705  010000                  MOV     #BIT12,R5       ;(R5)= EXPECTED VALUE
                                                        ;IN SYSTEM CONTROL REGISTER
                                                        ;SILO OVERFLOW INTERRUPT ENABLE
003464  011304                        MOV     (R3),R4         ;(R4)=ACTUAL DATA IN
                                                        ;SYSTEM CONTROL REGISTER
003466  104001                        HLT     1               ;SYSTEM CONTROL REGISTER
                                                        ;WRITE/READ ERROR
003470  042713  010000        1$:     BIC     #BIT12,(R3)     ;CLEAR SILO OVERFLOW INTERRUPT ENABLE
003474  001403                        BEQ     2$
003476  005005                        CLR     R5              ;(R5)=EXPECTED DATA IN
                                                        ;SYSTEM CONTROL REGISTER, 0
003500  011304                        MOV     (R3),R4         ;(R4)=ACTUAL DATA IN
                                                        ;SYSTEM CONTROL REGISTER
003502  104001                        HLT     1               ;SYSTEM CONTROL REGISTER
                                                        ;WRITE/READ ERROR
003504  104400              2$:     SCOPE                   ;CHECK FOR ITERATIONS, LOOP

                        ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
                        ;SET TRANSMITTER INTERRUPT ENABLE IN SYSTEM CONTROL REGISTER
                        ;VERIFY THAT TRANSMITTER INTERRUPT ENABLE WAS SET
                        ;CLEAR TRANSMITTER INTERRUPT ENABLE
                        ;VERITY THAT TRANSMITTER INTERRUPT ENABLE WAS CLEARED

003506  012767  000340  174262  T26:    MOV     #340,PS         ;DISABLE ALL INTERRUPTS
003514  012767  004000  014176          MOV     #4000,ICOUNT    ;SET UP FOR 4000 ITERATIONS
003522  012767  003572  014164          MOV     #2$,ESCAPE      ;SET UP TO ESCAPE TO NEXT TEST
003530  016703  014116                  MOV     DHSCR,R3        ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
003534  012713  020000                  MOV     #BIT13,(R3)     ;SET TRANSMITTER INTERRUPT ENABLE
003540  022713  020000                  CMP     #BIT13,(R3)     ;VERIFY THAT TRANSMITTER INTERRUPT ENABLE WAS SE
003544  001404                        BEQ     1$
003546  012705  020000                  MOV     #BIT13,R5       ;(R5)= EXPECTED VALUE
                                                        ;IN SYSTEM CONTROL REGISTER
```

```
1013
1014  003552  011304                        MOV     (R3),R4         ;TRANSMITTER INTERRUPT ENABLE
1015                                                                  ;(R4)=ACTUAL DATA IN
1016  003554  104001                        HLT     1               ;SYSTEM CONTROL REGISTER
1017                                                                  ;SYSTEM CONTROL REGISTER
1018  003556  042713  020000        1$:     BIC     #BIT13,(R3)     ;WRITE/READ ERROR
1019  003562  001403                        BEQ     2$              ;CLEAR TRANSMITTER INTERRUPT ENABLE
1020  003564  005005                        CLR     R5
1021                                                                  ;(R5)=EXPECTED DATA IN
1022  003566  011304                        MOV     (R3),R4         ;SYSTEM CONTROL REGISTER, 0
1023                                                                  ;(R4)=ACTUAL DATA IN
1024  003570  104001                        HLT     1               ;SYSTEM CONTROL REGISTER
1025                                                                  ;SYSTEM CONTROL REGISTER
1026  003572  104400        2$:     SCOPE                           ;WRITE/READ ERROR
1027                                                                  ;CHECK FOR ITERATIONS, LOOP
1028                        ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
1029                        ;SET TRANSMITTER DONE IN SYSTEM CONTROL REGISTER
1030                        ;VERIFY THAT TRANSMITTER DONE WAS SET
1031                        ;CLEAR TRANSMITTER DONE
1032                        ;VERITY THAT TRANSMITTER DONE WAS CLEARED
1033
1034  003574  012767  000340  174174  T27:   MOV     #340,PS         ;DISABLE ALL INTERRUPTS
1035  003602  012767  004000  014110        MOV     #4000,ICOUNT    ;SET UP FOR 4000 ITERATIONS
1036  003610  012767  003660  014076        MOV     #2$,ESCAPE      ;SET UP TO ESCAPE TO NEXT TEST
1037  003616  016703  014030                MOV     DHSCR,R3        ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
1038  003622  012713  100000                MOV     #BIT15,(R3)     ;SET TRANSMITTER DONE
1039  003626  022713  100000                CMP     #BIT15,(R3)     ;VERIFY THAT TRANSMITTER DONE WAS SET
1040  003632  001404                        BEQ     1$
1041  003634  012705  100000                MOV     #BIT15,R5       ;(R5)= EXPECTED VALUE
1042                                                                  ;IN SYSTEM CONTROL REGISTER
1043                                                                  ;TRANSMITTER DONE
1044  003640  011304                        MOV     (R3),R4         ;(R4)=ACTUAL DATA IN
1045                                                                  ;SYSTEM CONTROL REGISTER
1046  003642  104001                        HLT     1               ;SYSTEM CONTROL REGISTER
1047                                                                  ;WRITE/READ ERROR
1048  003644  042713  100000        1$:     BIC     #BIT15,(R3)     ;CLEAR TRANSMITTER DONE
1049  003650  001403                        BEQ     2$
1050  003652  005005                        CLR     R5
1051                                                                  ;(R5)=EXPECTED DATA IN
1052  003654  011304                        MOV     (R3),R4         ;SYSTEM CONTROL REGISTER, 0
1053                                                                  ;(R4)=ACTUAL DATA IN
1054  003656  104001                        HLT     1               ;SYSTEM CONTROL REGISTER
1055                                                                  ;SYSTEM CONTROL REGISTER
1056  003660  104400        2$:     SCOPE                           ;WRITE/READ ERROR
1057                                                                  ;CHECK FOR ITERATIONS, LOOP
1058                        ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
1059                        ;VERIFY THAT CHARACTER AVAILABLE IS READ ONLY IN NORMAL MODE
1060
1061  003662  012767  000340  174106  T30:   MOV     #340,PS         ;DISABLE ALL INTERRUPTS
1062  003670  012767  004000  014022        MOV     #4000,ICOUNT    ;SET UP FOR 4000 ITERATIONS
1063  003676  012767  003734  014010        MOV     #1$,ESCAPE      ;SET UP TO ESCAPE TO NEXT TEST
1064  003704  012777  000200  013740        MOV     #BIT07,@DHSCR   ;ATTEMPT TO WRITE
1065                                                                  ;CHARACTER AVAILABLE IN
1066                                                                  ;SYSTEM CONTROL REGISTER
1067  003712  005777  013734                TST     @DHSCR          ;WAS CHARACTER AVAILABLE SET
1068  003716  001406                        BEQ     1$
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1069  003720  005005                          CLR     R5                      ;(R5)=EXPECTED DATA
1070                                                                          ;IN SYSTEM CONTROL REGISTER, 0
1071  003722  017704  013724                  MOV     @DHSCR,R4               ;(R4)=ACTUAL DATA IN SYSTEM
1072                                                                          ;CONTROL REGISTER
1073  003726  016703  013720                  MOV     DHSCR,R3                ;ADDRESS OF SYSTEM CONTROL REGISTER
1074  003732  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
1075                                                                          ;WRITE/READ ERROR
1076  003734  104400              1$:         SCOPE
1077
1078                                          ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
1079                                          ;VERIFY THAT CLEAR      NON EXISTANT MEMORY IS READ ONLY IN NORMAL MODE
1080
1081  003736  012767  000340  174032  T31:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1082  003744  012767  004000  013746          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1083  003752  012767  004010  013734          MOV     #1$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1084  003760  012777  000400  013664          MOV     #BIT08,@DHSCR           ;ATTEMPT TO WRITE
1085                                                                          ;CLEAR  NON EXISTANT MEMORY IN
1086                                                                          ;SYSTEM CONTROL REGISTER
1087  003766  005777  013660                  TST     @DHSCR                  ;WAS CLEAR      NON EXISTANT MEMORY SET
1088  003772  001406                          BEQ     1$
1089  003774  005005                          CLR     R5                      ;(R5)=EXPECTED DATA
1090                                                                          ;IN SYSTEM CONTROL REGISTER, 0
1091  003776  017704  013650                  MOV     @DHSCR,R4               ;(R4)=ACTUAL DATA IN SYSTEM
1092                                                                          ;CONTROL REGISTER
1093  004002  016703  013644                  MOV     DHSCR,R3                ;ADDRESS OF SYSTEM CONTROL REGISTER
1094  004006  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
1095                                                                          ;WRITE/READ ERROR
1096  004010  104400              1$:         SCOPE
1097
1098                                          ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
1099                                          ;VERIFY THAT NON EXISTANT MEMORY IS READ ONLY IN NORMAL MODE
1100
1101  004012  012767  000340  173756  T32:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1102  004020  012767  004000  013672          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1103  004026  012767  004064  013660          MOV     #1$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1104  004034  012777  002000  013610          MOV     #BIT10,@DHSCR           ;ATTEMPT TO WRITE
1105                                                                          ;NON EXISTANT MEMORY IN
1106                                                                          ;SYSTEM CONTROL REGISTER
1107  004042  005777  013604                  TST     @DHSCR                  ;WAS NON EXISTANT MEMORY SET
1108  004046  001406                          BEQ     1$
1109  004050  005005                          CLR     R5                      ;(R5)=EXPECTED DATA
1110                                                                          ;IN SYSTEM CONTROL REGISTER, 0
1111  004052  017704  013574                  MOV     @DHSCR,R4               ;(R4)=ACTUAL DATA IN SYSTEM
1112                                                                          ;CONTROL REGISTER
1113  004056  016703  013570                  MOV     DHSCR,R3                ;ADDRESS OF SYSTEM CONTROL REGISTER
1114  004062  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
1115                                                                          ;WRITE/READ ERROR
1116  004064  104400              1$:         SCOPE
1117
1118                                          ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
1119                                          ;VERIFY THAT MASTER CLEAR IS READ ONLY IN NORMAL MODE
1120
1121  004066  012767  000340  173702  T33:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1122  004074  012767  004000  013616          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1123  004102  012767  004140  013604          MOV     #1$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1124  004110  012777  004000  013534          MOV     #BIT11,@DHSCR           ;ATTEMPT TO WRITE
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1125
1126
1127  004116  005777  013530            TST     @DHSCR                  ;MASTER CLEAR IN
1128  004122  001406                    BEQ     1$                      ;SYSTEM CONTROL REGISTER
1129  004124  005005                    CLR     R5                      ;WAS MASTER CLEAR SET
1130                                                                      ;(R5)=EXPECTED DATA
1131  004126  017704  013520            MOV     @DHSCR,R4               ;IN SYSTEM CONTROL REGI. ER, 0
1132                                                                      ;(R4)=ACTUAL DATA IN SYSTEM
1133  004132  016703  013514            MOV     DHSCR,R3                ;CONTROL REGISTER
1134  004136  104001                    HLT     1                       ;ADDRESS OF SYSTEM CONTROL REGISTER
1135                                                                      ;SYSTEM CONTROL REGISTER
1136  004140  104400            1$:     SCOPE                           ;WRITE/READ ERROR
1137
1138                                    ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
1139                                    ;VERIFY THAT SILO OVERFLOW IS READ ONLY IN NORMAL MODE
1140
1141  004142  012767  000340  173626    34:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1142  004150  012767  004000  013542            MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1143  004156  012767  004214  013530            MOV     #1$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1144  004164  012777  040000  013460            MOV     #BIT14,@DHSCR           ;ATTEMPT TO WRITE
1145                                                                            ;SILO OVERFLOW IN
1146                                                                            ;SYSTEM CONTROL REGISTER
1147  004172  005777  013454                    TST     @DHSCR                  ;WAS SILO OVERFLOW SET
1148  004176  001406                            BEQ     1$
1149  004200  005005                            CLR     R5                      ;(R5)=EXPECTED DATA
1150                                                                            ;IN SYSTEM CONTROL REGISTER, 0
1151  004202  017704  013444                    MOV     @DHSCR,R4               ;(R4)=ACTUAL DATA IN SYSTEM
1152                                                                            ;CONTROL REGISTER
1153  004206  016703  013440                    MOV     DHSCR,R3                ;ADDRESS OF SYSTEM CONTROL REGISTER
1154  004212  104001                            HLT     1                       ;SYSTEM CONTROL REGISTER
1155                                                                            ;WRITE/READ ERROR
1156  004214  104400            1$:     SCOPE
1157                                    ;SYSTEM CONTROL REGISTER WRITE/READ TEST (MAINTENANCE MODE)
1158                                    ;SET MAINTENANCE MODE
1159                                    ;SET CHARACTER AVAILABLE IN SYSTEM CONTROL REGISTER
1160                                    ;VERIFY THAT CHARACTER AVAILABLE WAS SET
1161                                    ;CLEAR MAINTENANCE MODE
1162                                    ;VERIFY THAT CHARACTER AVAILABLE CANNOT BE CLEARED
1163                                    ;SET MAINTENANCE MODE
1164                                    ;CLEAR CHARACTER AVAILABLE
1165                                    ;VERIFY THAT CHARACTER AVAILABLE WAS CLEARED
1166
1167  004216  012767  000340  173552  T35:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1168  004224  012767  004000  013466            MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1169  004232  012767  004344  013454            MOV     #3$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1170  004240  016703  013406                    MOV     DHSCR,R3                ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
1171  004244  012713  001000                    MOV     #BIT09,(R3)             ;SET MAINTENANCE MODE
1172  004250  052713  000200                    BIS     #BIT07,(R3)             ;SET CHARACTER AVAILABLE
1173  004254  022713  001200                    CMP     #BIT09+BIT07,(R3)       ;VERIFY THAT CHARACTER AVAILABLE
1174                                                                            ;AND MAINTENANCE MODE ARE SET
1175  004260  001404                            BEQ     1$
1176  004262  012705  001200                    MOV     #BIT09+BIT07,R5 ;(R5)-EXPECTED DATA
1177                                                                            ;IN SYSTEM CONTROL REGISTER
1178                                                                            ;MAINTENANCE MODE AND CHARACTER AVAILABLE
1179  004266  011304                            MOV     (R3),R4                 ;(R4)=ACTUAL DATA IN
1180                                                                            ;SYSTEM CONTROL REGISTER
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1181  004270  104001                        HLT     1                       ;SYSTEM CONTROL REGISTER
1182                                                                          ;WRITE/READ ERROR
1183  004272  042713  001000          1$:   BIC     #BIT09,(R3)             ;CLEAR MAINTENANCE MODE
1184  004276  042713  000200                BIC     #BIT07,(R3)             ;ATTEMPT TO CLEAR CHARACTER AVAILABLE
1185  004302  022713  000200                CMP     #BIT07,(R3)             ;CHARACTER AVAILABLE SHOULD BE SET
1186  004306  001403                        BEQ     2$
1187  004310  012705  000200                MOV     #BIT07,R5               ;(R5)=EXPECTED DATA IN
1188                                                                          ;SYSTEM CONTROL REGISTER
1189                                                                          ;CHARACTER AVAILABLE
1190  004314  104001                        HLT     1                       ;SYSTEM CONTROL REGISTER
1191                                                                          ;WRITE/READ ERROR
1192  004316  052713  001000          2$:   BIS     #BIT09,(R3)             ;SET MAINTENANCE MODE
1193  004322  042713  000200                BIC     #BIT07,(R3)             ;CLEAR CHARACTER AVAILABLE
1194  004326  022713  001000                CMP     #BIT09,(R3)             ;EXPECT ONLY MAINTENANCE
1195                                                                          ;MODE TO BE SET
1196  004332  001404                        BEQ     3$
1197  004334  012705  001000                MOV     #BIT09,R5               ;(R5)=EXPECTED DATA IN
1198                                                                          ;SYSTEM CONTROL REGISTER,
1199                                                                          ;MAINTENANCE MODE BIT
1200  004340  011304                        MOV     (R3),R4                 ;(R4)=ACTUAL DATA IN
1201                                                                          ;SYSTEM CONTROL REGISTER
1202  004342  104001                        HLT     1                       ;SYSTEM CONTROL REGISTER
1203                                                                          ;WRITE/READ ERROR
1204  004344  104400                3$:     SCOPE                           ;CHECK FOR ITERATIONS, LOOP
1205                                        ;SYSTEM CONTROL REGISTER WRITE/READ TEST (MAINTENANCE MODE)
1206                                        ;SET MAINTENANCE MODE
1207                                        ;SET NON EXISTANT MEMORY IN SYSTEM CONTROL REGISTER
1208                                        ;VERIFY THAT NON EXISTANT MEMORY WAS SET
1209                                        ;CLEAR MAINTENANCE MODE
1210                                        ;VERIFY THAT NON EXISTANT MEMORY CANNOT BE CLEARED
1211                                        ;SET MAINTENANCE MODE
1212                                        ;CLEAR NON EXISTANT MEMORY
1213                                        ;VERIFY THAT NON EXISTANT MEMORY WAS CLEARED
1214
1215  004346  012767  000340  173422  T36:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1216  004354  012767  004000  013336        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1217  004362  012767  004474  013324        MOV     #3$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1218  004370  016703  013256                MOV     DHSCR,R3                ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
1219  004374  012713  001000                MOV     #BIT09,(R3)             ;SET MAINTENANCE MODE
1220  004400  052713  002000                BIS     #BIT10,(R3)             ;SET NON EXISTANT MEMORY
1221  004404  022713  003000                CMP     #BIT09+BIT10,(R3)       ;VERIFY THAT NON EXISTANT MEMORY
1222                                                                          ;AND MAINTENANCE MODE ARE SET
1223  004410  001404                        BEQ     1$
1224  004412  012705  003000                MOV     #BIT09+BIT10,R5 ;(R5)=EXPECTED DATA
1225                                                                          ;IN SYSTEM CONTROL REGISTER
1226                                                                          ;MAINTENANCE MODE AND NON EXISTANT MEMORY
1227  004416  011304                        MOV     (R3),R4                 ;(R4)=ACTUAL DATA IN
1228                                                                          ;SYSTEM CONTROL REGISTER
1229  004420  104001                        HLT     1                       ;SYSTEM CONTROL REGISTER
1230                                                                          ;WRITE/READ ERROR
1231  004422  042713  001000          1$:   BIC     #BIT09,(R3)             ;CLEAR MAINTENANCE MODE
1232  004426  042713  002000                BIC     #BIT10,(R3)             ;ATTEMPT TO CLEAR NON EXISTANT MEMORY
1233  004432  022713  002000                CMP     #BIT10,(R3)             ;NON EXISTANT MEMORY SHOULD BE SET
1234  004436  001403                        BEQ     2$
1235  004440  012705  002000                MOV     #BIT10,R5               ;(R5)=EXPECTED DATA IN
1236                                                                          ;SYSTEM CONTROL REGISTER
```

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                                                        ;NON EXISTANT MEMORY
004444  104001                  HLT     1               ;SYSTEM CONTROL REGISTER
                                                        ;WRITE/READ ERROR
004446  052713  001000    2$:   BIS     #BIT09,(R3)     ;SET MAINTENANCE MODE
004452  042713  002000          BIC     #BIT10,(R3)     ;CLEAR NON EXISTANT MEMORY
004456  022713  001000          CMP     #BIT09,(R3)     ;EXPECT ONLY MAINTENANCE
                                                        ;MODE TO BE SET
004462  001404                  BEQ     3$
004464  012705  001000          MOV     #BIT09,R5       ;(R5)=EXPECTED DATA IN
                                                        ;SYSTEM CONTROL REGISTER,
                                                        ;MAINTENANCE MODE BIT
004470  011304                  MOV     (R3),R4         ;(R4)=ACTUAL DATA IN
                                                        ;SYSTEM CONTROL REGISTER
004472  104001                  HLT     1               ;SYSTEM CONTROL REGISTER
                                                        ;WRITE/READ ERROR
004474  104400            3$:   SCOPE                   ;CHECK FOR ITERATIONS, LOOP
                        ;SYSTEM CONTROL REGISTER WRITE/READ TEST (MAINTENANCE MODE)
                        ;SET MAINTENANCE MODE
                        ;SET SILO OVERFLOW IN SYSTEM CONTROL REGISTER
                        ;VERIFY THAT SILO OVERFLOW WAS SET
                        ;CLEAR MAINTENANCE MODE
                        ;VERIFY THAT SILO OVERFLOW CANNOT BE CLEARED
                        ;SET MAINTENANCE MODE
                        ;CLEAR SILO OVERFLOW
                        ;VERIFY THAT SILO OVERFLOW WAS CLEARED
004476  012767  000340  173272  T37:   MOV     #340,PS         ;DISABLE ALL INTERRUPTS
004504  012767  004000  013206        MOV     #4000,ICOUNT    ;SET UP FOR 4000 ITERATIONS
004512  012767  004624  013174        MOV     #3$,ESCAPE      ;SET UP TO ESCAPE TO NEXT TEST
004520  016703  013126                MOV     DHSCR,R3        ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
004524  012713  001000                MOV     #BIT09,(R3)     ;SET MAINTENANCE MODE
004530  052713  040000                BIS     #BIT14,(R3)     ;SET SILO OVERFLOW
004534  022713  041000                CMP     #BIT09+BIT14,(R3)   ;VERIFY THAT SILO OVERFLOW
                                                        ;AND MAINTENANCE MODE ARE SET
004540  001404                      BEQ     1$
004542  012705  041000              MOV     #BIT09+BIT14,R5 ;(R5)=EXPECTED DATA
                                                        ;IN SYSTEM CONTROL REGISTER
                                                        ;MAINTENANCE MODE AND SILO OVERFLOW
004546  011304                      MOV     (R3),R4         ;(R4)=ACTUAL DATA IN
                                                        ;SYSTEM CONTROL REGISTER
004550  104001                      HLT     1               ;SYSTEM CONTROL REGISTER
                                                        ;WRITE/READ ERROR
004552  042713  001000    1$:       BIC     #BIT09,(R3)     ;CLEAR MAINTENANCE MODE
004556  042713  040000              BIC     #BIT14,(R3)     ;ATTEMPT TO CLEAR SILO OVERFLOW
004562  022713  040000              CMP     #BIT14,(R3)     ;SILO OVERFLOW SHOULD BE SET
004566  001403                      BEQ     2$
004570  012705  040000              MOV     #BIT14,R5       ;(R5)=EXPECTED DATA IN
                                                        ;SYSTEM CONTROL REGISTER
                                                        ;SILO OVERFLOW
004574  104001                      HLT     1               ;SYSTEM CONTROL REGISTER
                                                        ;WRITE/READ ERROR
004576  052713  001000    2$:       BIS     #BIT09,(R3)     ;SET MAINTENANCE MODE
004602  042713  040000              BIC     #BIT14,(R3)     ;CLEAR SILO OVERFLOW
004606  022713  001000              CMP     #BIT09,(R3)     ;EXPECT ONLY MAINTENANCE
                                                        ;MODE TO BE SET
004612  001404                      BEQ     3$
```

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1293  004614  012705  001000                MOV     #BIT09,R5               ;(R5)=EXPECTED DATA IN
1294                                                                          ;SYSTEM CONTROL REGISTER,
1295                                                                          ;MAINTENANCE MODE BIT
1296  004620  011304                        MOV     (R3),R4                 ;(R4)=ACTUAL DATA IN
1297                                                                          ;SYSTEM CONTROL REGISTER
1298  004622  104001                        HLT     1                       ;SYSTEM CONTROL REGISTER
1299                                                                          ;WRITE/READ ERROR
1300  004624  104400              3$:       SCOPE                           ;CHECK FOR ITERATIONS, LOOP
1301
1302                                        ;LINE PARAMETER REGISTER DATA TEST
1303                                        ;SET BIT 0 IN LINE PARAMETER TO 1
1304                                        ;VERIFY THAT BIT 0 WAS SET
1305                                        ;CLEAR BIT 0
1306                                        ;VERIFY THAT BIT 0 WAS CLEARED
1307
1308  004626  012767  000340  173142  T40:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1309  004634  012767  004000  013056        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1310  004642  012767  004714  013044        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1311  004650  012777  004000  012774        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1312  004656  016703  012774                MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
1313  004662  012705  000001                MOV     #1,R5                   ;BIT 0 WILL BE SET IN LINE PARAMETER
1314  004666  010513                        MOV     R5,(R3)                 ;SET BIT 0
1315  004670  011304                        MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
1316  004672  020504                        CMP     R5,R4                   ;WAS BIT 0 SET
1317  004674  001401                        BEQ     1$
1318  004676  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
1319  004700  040513              1$:       BIC     R5,(R3)                 ;CLEAR BIT 0
1320  004702  011304                        MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
1321  004704  005704                        TST     R4                      ;WAS BIT 0 CLEARED
1322  004706  001402                        BEQ     2$
1323  004710  005005                        CLR     R5
1324  004712  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
1325  004714  104400              2$:       SCOPE
1326
1327                                        ;LINE PARAMETER REGISTER DATA TEST
1328                                        ;SET BIT 1 IN LINE PARAMETER TO 1
1329                                        ;VERIFY THAT BIT 1 WAS SET
1330                                        ;CLEAR BIT 1
1331                                        ;VERIFY THAT BIT 1 WAS CLEARED
1332
1333  004716  012767  000340  173052  T41:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1334  004724  012767  004000  012766        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1335  004732  012767  005004  012754        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1336  004740  012777  004000  012704        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1337  004746  016703  012704                MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
1338  004752  012705  000002                MOV     #2,R5                   ;BIT 1 WILL BE SET IN LINE PARAMETER
1339  004756  010513                        MOV     R5,(R3)                 ;SET BIT 1
1340  004760  011304                        MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
1341  004762  020504                        CMP     R5,R4                   ;WAS BIT 1 SET
1342  004764  001401                        BEQ     1$
1343  004766  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
1344  004770  040513              1$:       BIC     R5,(R3)                 ;CLEAR BIT 1
1345  004772  011304                        MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
1346  004774  005704                        TST     R4                      ;WAS BIT 1 CLEARED
1347  004776  001402                        BEQ     2$
1348  005000  005005                        CLR     R5
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1349  005002  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1350  005004  104400                  2$:     SCOPE
1351
1352                                          ;LINE PARAMETER REGISTER DATA TEST
1353                                          ;SET BIT 2 IN LINE PARAMETER TO 1
1354                                          ;VERIFY THAT BIT 2 WAS SET
1355                                          ;CLEAR BIT 2
1356                                          ;VERIFY THAT BIT 2 WAS CLEARED
1357
1358  005006  012767  000340  172762  T42:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1359  005014  012767  004000  012676          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1360  005022  012767  005074  012664          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1361  005030  012777  004000  012614          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1362  005036  016703  012614                  MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
1363  005042  012705  000004                  MOV     #4,R5                   ;BIT 2 WILL BE SET IN LINE PARAMETER
1364  005046  010513                          MOV     R5,(R3)                 ;SET BIT 2
1365  005050  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
1366  005052  020504                          CMP     R5,R4                   ;WAS BIT 2 SET
1367  005054  001401                          BEQ     1$
1368  005056  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1369  005060  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 2
1370  005062  011304                          MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
1371  005064  005704                          TST     R4                      ;WAS BIT 2 CLEARED
1372  005066  001402                          BEQ     2$
1373  005070  005005                          CLR     R5
1374  005072  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1375  005074  104400                  2$:     SCOPE
1376
1377                                          ;LINE PARAMETER REGISTER DATA TEST
1378                                          ;SET BIT 4 IN LINE PARAMETER TO 1
1379                                          ;VERIFY THAT BIT 4 WAS SET
1380                                          ;CLEAR BIT 4
1381                                          ;VERIFY THAT BIT 4 WAS CLEARED
1382
1383  005076  012767  000340  172672  T43:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1384  005104  012767  004000  012606          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1385  005112  012767  005164  012574          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1386  005120  012777  004000  012524          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1387  005126  016703  012524                  MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
1388  005132  012705  000020                  MOV     #20,R5                  ;BIT 4 WILL BE SET IN LINE PARAMETER
1389  005136  010513                          MOV     R5,(R3)                 ;SET BIT 4
1390  005140  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
1391  005142  020504                          CMP     R5,R4                   ;WAS BIT 4 SET
1392  005144  001401                          BEQ     1$
1393  005146  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1394  005150  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 4
1395  005152  011304                          MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
1396  005154  005704                          TST     R4                      ;WAS BIT 4 CLEARED
1397  005156  001402                          BEQ     2$
1398  005160  005005                          CLR     R5
1399  005162  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1400  005164  104400                  2$:     SCOPE
1401
1402                                          ;LINE PARAMETER REGISTER DATA TEST
1403                                          ;SET BIT 5 IN LINE PARAMETER TO 1
1404                                          ;VERIFY THAT BIT 5 WAS SE
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1405                                                    ;CLEAR BIT 5
1406                                                    ;VERIFY THAT BIT 5 WAS CLEARED
1407
1408  005166  012767  000340  172602  T44:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1409  005174  012767  004000  012516          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1410  005202  012767  005254  012504          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1411  005210  012777  004000  012434          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1412  005216  016703  012434                  MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
1413  005222  012705  000040                  MOV     #40,R5                  ;BIT 5 WILL BE SET IN LINE PARAMETER
1414  005226  010513                          MOV     R5,(R3)                 ;SET BIT 5
1415  005230  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
1416  005232  020504                          CMP     R5,R4                   ;WAS BIT 5 SET
1417  005234  001401                          BEQ     1$
1418  005236  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1419  005240  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 5
1420  005242  011304                          MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
1421  005244  005704                          TST     R4                      ;WAS BIT 5 CLEARED
1422  005246  001402                          BEQ     2$
1423  005250  005005                          CLR     R5
1424  005252  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1425  005254  104400                  2$:     SCOPE
1426
1427                                                    ;LINE PARAMETER REGISTER DATA TEST
1428                                                    ;SET BIT 6 IN LINE PARAMETER TO 1
1429                                                    ;VERIFY THAT BIT 6 WAS SET
1430                                                    ;CLEAR BIT 6
1431                                                    ;VERIFY THAT BIT 6 WAS CLEARED
1432
1433  005256  012767  000340  172512  T45:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1434  005264  012767  004000  012426          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1435  005272  012767  005344  012414          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1436  005300  012777  004000  012344          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1437  005306  016703  012344                  MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
1438  005312  012705  000100                  MOV     #100,R5                 ;BIT 6 WILL BE SET IN LINE PARAMETER
1439  005316  010513                          MOV     R5,(R3)                 ;SET BIT 6
1440  005320  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
1441  005322  020504                          CMP     R5,R4                   ;WAS BIT 6 SET
1442  005324  001401                          BEQ     1$
1443  005326  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1444  005330  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 6
1445  005332  011304                          MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
1446  005334  005704                          TST     R4                      ;WAS BIT 6 CLEARED
1447  005336  001402                          BEQ     2$
1448  005340  005005                          CLR     R5
1449  005342  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1450  005344  104400                  2$:     SCOPE
1451
1452                                                    ;LINE PARAMETER REGISTER DATA TEST
1453                                                    ;SET BIT 7 IN LINE PARAMETER TO 1
1454                                                    ;VERIFY THAT BIT 7 WAS SET
1455                                                    ;CLEAR BIT 7
1456                                                    ;VERIFY THAT BIT 7 WAS CLEARED
1457
1458  005346  012767  000340  172422  T46:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1459  005354  012767  004000  012336          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1460  005362  012767  005434  012324          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
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1461  005370  012777  004000  012254          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1462  005376  016703  012254                  MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
1463  005402  012705  000200                  MOV     #200,R5                 ;BIT 7 WILL BE SET IN LINE PARAMETER
1464  005406  010513                          MOV     R5,(R3)                 ;SET BIT 7
1465  005410  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
1466  005412  020504                          CMP     R5,R4                   ;WAS BIT 7 SET
1467  005414  001401                          BEQ     1$
1468  005416  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1469  005420  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 7
1470  005422  011304                          MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
1471  005424  005704                          TST     R4                      ;WAS BIT 7 CLEARED
1472  005426  001402                          BEQ     2$
1473  005430  005005                          CLR     R5
1474  005432  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1475  005434  104400                  2$:     SCOPE
1476
1477                                          ;LINE PARAMETER REGISTER DATA TEST
1478                                          ;SET BIT 10 IN LINE PARAMETER TO 1
1479                                          ;VERIFY THAT BIT 10 WAS SET
1480                                          ;CLEAR BIT 10
1481                                          ;VERIFY THAT BIT 10 WAS CLEARED
1482
1483  005436  012767  000340  172332  T47:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1484  005444  012767  004000  012246          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1485  005452  012767  005524  012234          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1486  005460  012777  004000  012164          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1487  005466  016703  012164                  MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
1488  005472  012705  000400                  MOV     #400,R5                 ;BIT 10 WILL BE SET IN LINE PARAMETER
1489  005476  010513                          MOV     R5,(R3)                 ;SET BIT 10
1490  005500  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
1491  005502  020504                          CMP     R5,R4                   ;WAS BIT 10 SET
1492  005504  001401                          BEQ     1$
1493  005506  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1494  005510  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 10
1495  005512  011304                          MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
1496  005514  005704                          TST     R4                      ;WAS BIT 10 CLEARED
1497  005516  001402                          BEQ     2$
1498  005520  005005                          CLR     R5
1499  005522  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1500  005524  104400                  2$:     SCOPE
1501
1502                                          ;LINE PARAMETER REGISTER DATA TEST
1503                                          ;SET BIT 11 IN LINE PARAMETER TO 1
1504                                          ;VERIFY THAT BIT 11 WAS SET
1505                                          ;CLEAR BIT 11
1506                                          ;VERIFY THAT BIT 11 WAS CLEARED
1507
1508  005526  012767  000340  172242  T50:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1509  005534  012767  004000  012156          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1510  005542  012767  005614  012144          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1511  005550  012777  004000  012074          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1512  005556  016703  012074                  MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
1513  005562  012705  001000                  MOV     #1000,R5                ;BIT 11 WILL BE SET IN LINE PARAMETER
1514  005566  010513                          MOV     R5,(R3)                 ;SET BIT 11
1515  005570  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
1516  005572  020504                          CMP     R5,R4                   ;WAS BIT 11 SET
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1517  005574  001401                          BEQ     1$
1518  005576  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1519  005600  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 11
1520  005602  011304                          MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
1521  005604  005704                          TST     R4                      ;WAS BIT 11 CLEARED
1522  005606  001402                          BEQ     2$
1523  005610  005005                          CLR     R5
1524  005612  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1525  005614  104400                  2$:     SCOPE
1526
1527                                          ;LINE PARAMETER REGISTER DATA TEST
1528                                          ;SET BIT 12 IN LINE PARAMETER TO 1
1529                                          ;VERIFY THAT BIT 12 WAS SET
1530                                          ;CLEAR BIT 12
1531                                          ;VERIFY THAT BIT 12 WAS CLEARED
1532
1533  005616  012767  000340  172152  T51:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1534  005624  012767  004000  012066          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1535  005632  012767  005704  012054          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1536  005640  012777  004000  012004          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1537  005646  016703  012004                  MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
1538  005652  012705  002000                  MOV     #2000,R5                        ;BIT 12 WILL BE SET IN LINE PARAMETER
1539  005656  010513                          MOV     R5,(R3)                 ;SET BIT 12
1540  005660  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
1541  005662  020504                          CMP     R5,R4                   ;WAS BIT 12 SET
1542  005664  001401                          BEQ     1$
1543  005666  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1544  005670  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 12
1545  005672  011304                          MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
1546  005674  005704                          TST     R4                      ;WAS BIT 12 CLEARED
1547  005676  001402                          BEQ     2$
1548  005700  005005                          CLR     R5
1549  005702  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1550  005704  104400                  2$:     SCOPE
1551
1552                                          ;LINE PARAMETER REGISTER DATA TEST
1553                                          ;SET BIT 13 IN LINE PARAMETER TO 1
1554                                          ;VERIFY THAT BIT 13 WAS SET
1555                                          ;CLEAR BIT 13
1556                                          ;VERIFY THAT BIT 13 WAS CLEARED
1557
1558  005706  012767  000340  172062  T52:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1559  005714  012767  004000  011776          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1560  005722  012767  005774  011764          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1561  005730  012777  004000  011714          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1562  005736  016703  011714                  MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
1563  005742  012705  004000                  MOV     #4000,R5                        ;BIT 13 WILL BE SET IN LINE PARAMETER
1564  005746  010513                          MOV     R5,(R3)                 ;SET BIT 13
1565  005750  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
1566  005752  020504                          CMP     R5,R4                   ;WAS BIT 13 SET
1567  005754  001401                          BEQ     1$
1568  005756  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1569  005760  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 13
1570  005762  011304                          MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
1571  005764  005704                          TST     R4                      ;WAS BIT 13 CLEARED
1572  005766  001402                          BEQ     2$
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1573  005770  005005                          CLR     R5
1574  005772  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1575  005774  104400                  2$:     SCOPE
1576
1577                                          ;LINE PARAMETER REGISTER DATA TEST
1578                                          ;SET BIT 14 IN LINE PARAMETER TO 1
1579                                          ;VERIFY THAT BIT 14 WAS SET
1580                                          ;CLEAR BIT 14
1581                                          ;VERIFY THAT BIT 14 WAS CLEARED
1582
1583  005776  012767  000340  171772  T53:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1584  006004  012767  004000  011706          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1585  006012  012767  006064  011674          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1586  006020  012777  004000  011624          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1587  006026  016703  011624                  MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
1588  006032  012705  010000                  MOV     #10000,R5                       ;BIT 14 WILL BE SET IN LINE PARAMETER
1589  006036  010513                          MOV     R5,(R3)                 ;SET BIT 14
1590  006040  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
1591  006042  020504                          CMP     R5,R4                   ;WAS BIT 14 SET
1592  006044  001401                          BEQ     1$
1593  006046  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1594  006050  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 14
1595  006052  011304                          MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
1596  006054  005704                          TST     R4                      ;WAS BIT 14 CLEARED
1597  006056  001402                          BEQ     2$
1598  006060  005005                          CLR     R5
1599  006062  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1600  006064  104400                  2$:     SCOPE
1601
1602                                          ;LINE PARAMETER REGISTER DATA TEST
1603                                          ;SET BIT 15 IN LINE PARAMETER TO 1
1604                                          ;VERIFY THAT BIT 15 WAS SET
1605                                          ;CLEAR BIT 15
1606                                          ;VERIFY THAT BIT 15 WAS CLEARED
1607
1608  006066  012767  000340  171702  T54:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1609  006074  012767  004000  011616          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1610  006102  012767  006154  011604          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1611  006110  012777  004000  011534          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1612  006116  016703  011534                  MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
1613  006122  012705  020000                  MOV     #20000,R5                       ;BIT 15 WILL BE SET IN LINE PARAMETER
1614  006126  010513                          MOV     R5,(R3)                 ;SET BIT 15
1615  006130  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
1616  006132  020504                          CMP     R5,R4                   ;WAS BIT 15 SET
1617  006134  001401                          BEQ     1$
1618  006136  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1619  006140  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 15
1620  006142  011304                          MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
1621  006144  005704                          TST     R4                      ;WAS BIT 15 CLEARED
1622  006146  001402                          BEQ     2$
1623  006150  005005                          CLR     R5
1624  006152  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1625  006154  104400                  2$:     SCOPE
1626
1627                                          ;LINE PARAMETER REGISTER DATA TEST
1628                                          ;SET BIT 16 IN LINE PARAMETER TO 1
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                                                ;VERIFY THAT BIT 16 WAS SET
                                                ;CLEAR BIT 16
                                                ;VERIFY THAT BIT 16 WAS CLEARED

006156  012767  000340  171612  T55:  MOV   #340,PS              ;DISABLE ALL INTERRUPTS
006164  012767  004000  011526        MOV   #4000,ICOUNT         ;SET UP FOR 4000 ITERATIONS
006172  012767  006244  011514        MOV   #2$,ESCAPE           ;SET UP TO ESCAPE TO NEXT TEST
006200  012777  004000  011444        MOV   #BIT11,@DHSCR        ;MASTER CLEAR INTERFACE
006206  016703  011444                MOV   DHLPR,R3             ;SET UP POINTER TO LINE PARAMETER
006212  012705  040000                MOV   #40000,R5                  ;BIT 16 WILL BE SET IN LINE PARAMETER
006216  010513                        MOV   R5,(R3)              ;SET BIT 16
006220  011304                        MOV   (R3),R4              ;GET CONTENTS OF LINE PARAMETER
006222  020504                        CMP   R5,R4                ;WAS BIT 16 SET
006224  001401                        BEQ   1$
006226  104002                        HLT   2                    ;LINE PARAMETER REGISTER ERROR
006230  040513                1$:     BIC   R5,(R3)              ;CLEAR BIT 16
006232  011304                        MOV   (R3),R4              ;READ CONTENTS OF LINE PARAMETER
006234  005704                        TST   R4                   ;WAS BIT 16 CLEARED
006236  001402                        BEQ   2$
006240  005005                        CLR   R5
006242  104002                        HLT   2                    ;LINE PARAMETER REGISTER ERROR
006244  104400                2$:     SCOPE

                                                ;LINE PARAMETER REGISTER DATA TEST
                                                ;SET BIT 17 IN LINE PARAMETER TO 1
                                                ;VERIFY THAT BIT 17 WAS SET
                                                ;CLEAR BIT 17
                                                ;VERIFY THAT BIT 17 WAS CLEARED

006246  012767  000340  171522  T56:  MOV   #340,PS              ;DISABLE ALL INTERRUPTS
006254  012767  004000  011436        MOV   #4000,ICOUNT         ;SET UP FOR 4000 ITERATIONS
006262  012767  006334  011424        MOV   #2$,ESCAPE           ;SET UP TO ESCAPE TO NEXT TEST
006270  012777  004000  011354        MOV   #BIT11,@DHSCR        ;MASTER CLEAR INTERFACE
006276  016703  011354                MOV   DHLPR,R3             ;SET UP POINTER TO LINE PARAMETER
006302  012705  100000                MOV   #100000,R5                 ;BIT 17 WILL BE SET IN LINE PARAMETER
006306  010513                        MOV   R5,(R3)              ;SET BIT 17
006310  011304                        MOV   (R3),R4              ;GET CONTENTS OF LINE PARAMETER
006312  020504                        CMP   R5,R4                ;WAS BIT 17 SET
006314  001401                        BEQ   1$
006316  104002                        HLT   2                    ;LINE PARAMETER REGISTER ERROR
006320  040513                1$:     BIC   R5,(R3)              ;CLEAR BIT 17
006322  011304                        MOV   (R3),R4              ;READ CONTENTS OF LINE PARAMETER
006324  005704                        TST   R4                   ;WAS BIT 17 CLEARED
006326  001402                        BEQ   2$
006330  005005                        CLR   R5
006332  104002                        HLT   2                    ;LINE PARAMETER REGISTER ERROR
006334  104400                2$:     SCOPE

                                                ;BREAK CONTROL REGISTER DATA TEST
                                                ;SET BIT 0 IN BREAK CONTROL TO 1
                                                ;VERIFY THAT BIT 0 WAS SET
                                                ;CLEAR BIT 0
                                                ;VERIFY THAT BIT 0 WAS CLEARED

006336  012767  000340  171432  T57:  MOV   #340,PS              ;DISABLE ALL INTERRUPTS
006344  012767  004000  011346        MOV   #4000,ICOUNT         ;SET UP FOR 4000 ITERATIONS
```

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1685  006352  012767  006424  011334          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1686  006360  012777  004000  011264          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1687  006366  016703  011274                  MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
1688  006372  012705  000001                  MOV     #1,R5                   ;BIT 0 WILL BE SET IN BREAK CONTROL
1689  006376  010513                          MOV     R5,(R3)                 ;SET BIT 0
1690  006400  011304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
1691  006402  020504                          CMP     R5,R4                   ;WAS BIT 0 SET
1692  006404  001401                          BEQ     1$
1693  006406  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
1694  006410  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 0
1695  006412  011304                          MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
1696  006414  005704                          TST     R4                      ;WAS BIT 0 CLEARED
1697  006416  001402                          BEQ     2$
1698  006420  005005                          CLR     R5
1699  006422  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
1700  006424  104400                  2$:     SCOPE
1701
1702                                          ;BREAK CONTROL REGISTER DATA TEST
1703                                          ;SET BIT 1 IN BREAK CONTROL TO 1
1704                                          ;VERIFY THAT BIT 1 WAS SET
1705                                          ;CLEAR BIT 1
1706                                          ;VERIFY THAT BIT 1 WAS CLEARED
1707
1708  006426  012767  000340  171342  T60:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1709  006434  012767  004000  011256          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1710  006442  012767  006514  011244          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1711  006450  012777  004000  011174          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1712  006456  016703  011204                  MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
1713  006462  012705  000002                  MOV     #2,R5                   ;BIT 1 WILL BE SET IN BREAK CONTROL
1714  006466  010513                          MOV     R5,(R3)                 ;SET BIT 1
1715  006470  011304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
1716  006472  020504                          CMP     R5,R4                   ;WAS BIT 1 SET
1717  006474  001401                          BEQ     1$
1718  006476  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
1719  006500  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 1
1720  006502  011304                          MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
1721  006504  005704                          TST     R4                      ;WAS BIT 1 CLEARED
1722  006506  001402                          BEQ     2$
1723  006510  005005                          CLR     R5
1724  006512  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
1725  006514  104400                  2$:     SCOPE
1726
1727                                          ;BREAK CONTROL REGISTER DATA TEST
1728                                          ;SET BIT 2 IN BREAK CONTROL TO 1
1729                                          ;VERIFY THAT BIT 2 WAS SET
1730                                          ;CLEAR BIT 2
1731                                          ;VERIFY THAT BIT 2 WAS CLEARED
1732
1733  006516  012767  000340  171252  T61:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1734  006524  012767  004000  011166          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1735  006532  012767  006604  011154          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1736  006540  012777  004000  011104          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1737  006546  016703  011114                  MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
1738  006552  012705  000004                  MOV     #4,R5                   ;BIT 2 WILL BE SET IN BREAK CONTROL
1739  006556  010513                          MOV     R5,(R3)                 ;SET BIT 2
1740  006560  011304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
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1741  006562  020504                        CMP     R5,R4                   ;WAS BIT 2 SET
1742  006564  001401                        BEQ     1$
1743  006566  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
1744  006570  040513                1$:     BIC     R5,(R3)                 ;CLEAR BIT 2
1745  006572  011304                        MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
1746  006574  005704                        TST     R4                      ;WAS BIT 2 CLEARED
1747  006576  001402                        BEQ     2$
1748  006600  005005                        CLR     R5
1749  006602  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
1750  006604  104400                2$:     SCOPE
1751
1752                                        ;BREAK CONTROL REGISTER DATA TEST
1753                                        ;SET BIT 3 IN BREAK CONTROL TO 1
1754                                        ;VERIFY THAT BIT 3 WAS SET
1755                                        ;CLEAR BIT 3
1756                                        ;VERIFY THAT BIT 3 WAS CLEARED
1757
1758  006606  012767  000340  171162 T62:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1759  006614  012767  004000  011076        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1760  006622  012767  006674  011064        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1761  006630  012777  004000  011014        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1762  006636  016703  011024                MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
1763  006642  012705  000010                MOV     #10,R5                  ;BIT 3 WILL BE SET IN BREAK CONTROL
1764  006646  010513                        MOV     R5,(R3)                 ;SET BIT 3
1765  006650  011304                        MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
1766  006652  020504                        CMP     R5,R4                   ;WAS BIT 3 SET
1767  006654  001401                        BEQ     1$
1768  006656  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
1769  006660  040513                1$:     BIC     R5,(R3)                 ;CLEAR BIT 3
1770  006662  011304                        MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
1771  006664  005704                        TST     R4                      ;WAS BIT 3 CLEARED
1772  006666  001402                        BEQ     2$
1773  006670  005005                        CLR     R5
1774  006672  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
1775  006674  104400                2$:     SCOPE
1776
1777                                        ;BREAK CONTROL REGISTER DATA TEST
1778                                        ;SET BIT 4 IN BREAK CONTROL TO 1
1779                                        ;VERIFY THAT BIT 4 WAS SET
1780                                        ;CLEAR BIT 4
1781                                        ;VERIFY THAT BIT 4 WAS CLEARED
1782
1783  006676  012767  000340  171072 T63:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1784  006704  012767  004000  011006        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1785  006712  012767  006764  010774        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1786  006720  012777  004000  010724        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1787  006726  016703  010734                MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
1788  006732  012705  000020                MOV     #20,R5                  ;BIT 4 WILL BE SET IN BREAK CONTROL
1789  006736  010513                        MOV     R5,(R3)                 ;SET BIT 4
1790  006740  011304                        MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
1791  006742  020504                        CMP     R5,R4                   ;WAS BIT 4 SET
1792  006744  001401                        BEQ     1$
1793  006746  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
1794  006750  040513                1$:     BIC     R5,(R3)                 ;CLEAR BIT 4
1795  006752  011304                        MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
1796  006754  005704                        TST     R4                      ;WAS BIT 4 CLEARED
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1797  006756  001402                        BEQ     2$
1798  006760  005005                        CLR     R5
1799  006762  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
1800  006764  104400                2$:     SCOPE
1801
1802                                        ;BREAK CONTROL REGISTER DATA TEST
1803                                        ;SET BIT 5 IN BREAK CONTROL TO 1
1804                                        ;VERIFY THAT BIT 5 WAS SET
1805                                        ;CLEAR BIT 5
1806                                        ;VERIFY THAT BIT 5 WAS CLEARED
1807
1808  006766  012767  000340  171002  T64:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1809  006774  012767  004000  010716        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1810  007002  012767  007054  010704        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1811  007010  012777  004000  010634        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1812  007016  016703  010644                MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
1813  007022  012705  000040                MOV     #40,R5                  ;BIT 5 WILL BE SET IN BREAK CONTROL
1814  007026  010513                        MOV     R5,(R3)                 ;SET BIT 5
1815  007030  011304                        MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
1816  007032  020504                        CMP     R5,R4                   ;WAS BIT 5 SET
1817  007034  001401                        BEQ     1$
1818  007036  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
1819  007040  040513                1$:     BIC     R5,(R3)                 ;CLEAR BIT 5
1820  007042  011304                        MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
1821  007044  005704                        TST     R4                      ;WAS BIT 5 CLEARED
1822  007046  001402                        BEQ     2$
1823  007050  005005                        CLR     R5
1824  007052  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
1825  007054  104400                2$:     SCOPE
1826
1827                                        ;BREAK CONTROL REGISTER DATA TEST
1828                                        ;SET BIT 6 IN BREAK CONTROL TO 1
1829                                        ;VERIFY THAT BIT 6 WAS SET
1830                                        ;CLEAR BIT 6
1831                                        ;VERIFY THAT BIT 6 WAS CLEARED
1832
1833  007056  012767  000340  170712  T65:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1834  007064  012767  004000  010626        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1835  007072  012767  007144  010614        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1836  007100  012777  004000  010544        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1837  007106  016703  010554                MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
1838  007112  012705  000100                MOV     #100,R5                 ;BIT 6 WILL BE SET IN BREAK CONTROL
1839  007116  010513                        MOV     R5,(R3)                 ;SET BIT 6
1840  007120  011304                        MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
1841  007122  020504                        CMP     R5,R4                   ;WAS BIT 6 SET
1842  007124  001401                        BEQ     1$
1843  007126  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
1844  007130  040513                1$:     BIC     R5,(R3)                 ;CLEAR BIT 6
1845  007132  011304                        MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
1846  007134  005704                        TST     R4                      ;WAS BIT 6 CLEARED
1847  007136  001402                        BEQ     2$
1848  007140  005005                        CLR     R5
1849  007142  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
1850  007144  104400                2$:     SCOPE
1851
1852                                        ;BREAK CONTROL REGISTER DATA TEST
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1853                                            ;SET BIT 7 IN BREAK CONTROL TO 1
1854                                            ;VERIFY THAT BIT 7 WAS SET
1855                                            ;CLEAR BIT 7
1856                                            ;VERIFY THAT BIT 7 WAS CLEARED
1857
1858  007146  012767  000340  170622  T66:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1859  007154  012767  004000  010536          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1860  007162  012767  007234  010524          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1861  007170  012777  004000  010454          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1862  007176  016703  010464                  MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
1863  007202  012705  000200                  MOV     #200,R5                 ;BIT 7 WILL BE SET IN BREAK CONTROL
1864  007206  010513                          MOV     R5,(R3)                 ;SET BIT 7
1865  007210  011304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
1866  007212  020504                          CMP     R5,R4                   ;WAS BIT 7 SET
1867  007214  001401                          BEQ     1$
1868  007216  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
1869  007220  040513                   $:     BIC     R5,(R3)                 ;CLEAR BIT 7
1870  007222  011304                          MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
1871  007224  005704                          TST     R4                      ;WAS BIT 7 CLEARED
1872  007226  001402                          BEQ     2$
1873  007230  005005                          CLR     R5
1874  007232  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
1875  007234  104400                   2$:    SCOPE
1876
1877                                            ;BREAK CONTROL REGISTER DATA TEST
1878                                            ;SET BIT 10 IN BREAK CONTROL TO 1
1879                                            ;VERIFY THAT BIT 10 WAS SET
1880                                            ;CLEAR BIT 10
1881                                            ;VERIFY THAT BIT 10 WAS CLEARED
1882
1883  007236  012767  000340  170532  T67:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1884  007244  012767  004000  010446          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1885  007252  012767  007324  010434          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1886  007260  012777  004000  010364          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1887  007266  016703  010374                  MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
1888  007272  012705  000400                  MOV     #400,R5                 ;BIT 10 WILL BE SET IN BREAK CONTROL
1889  007276  010513                          MOV     R5,(R3)                 ;SET BIT 10
1890  007300  011304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
1891  007302  020504                          CMP     R5,R4                   ;WAS BIT 10 SET
1892  007304  001401                          BEQ     1$
1893  007306  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
1894  007310  040513                   1$:    BIC     R5,(R3)                 ;CLEAR BIT 10
1895  007312  011304                          MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
1896  007314  005704                          TST     R4                      ;WAS BIT 10 CLEARED
1897  007316  001402                          BEQ     2$
1898  007320  005005                          CLR     R5
1899  007322  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
1900  007324  104400                   2$:    SCOPE
1901
1902                                            ;BREAK CONTROL REGISTER DATA TEST
1903                                            ;SET BIT 11 IN BREAK CONTROL TO 1
1904                                            ;VERIFY THAT BIT 11 WAS SET
1905                                            ;CLEAR BIT 11
1906                                            ;VERIFY THAT BIT 11 WAS CLEARED
1907
1908  007326  012767  000340  170442  T70:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
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1909  007334  012767  004000  010356          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1910  007342  012767  007414  010344          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1911  007350  012777  004000  010274          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1912  007356  016703  010304                  MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
1913  007362  012705  001000                  MOV     #1000,R5                        ;BIT 11 WILL BE SET IN BREAK CONTROL
1914  007366  010513                          MOV     R5,(R3)                 ;SET BIT 11
1915  007370  011304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
1916  007372  020504                          CMP     R5,R4                   ;WAS BIT 11 SET
1917  007374  001401                          BEQ     1$
1918  007376  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
1919  007400  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 11
1920  007402  011304                          MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
1921  007404  005704                          TST     R4                      ;WAS BIT 11 CLEARED
1922  007406  001402                          BEQ     2$
1923  007410  005005                          CLR     R5
1924  007412  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
1925  007414  104400                  2$:     SCOPE
1926
1927                                          ;BREAK CONTROL REGISTER DATA TEST
1928                                          ;SET BIT 12 IN BREAK CONTROL TO 1
1929                                          ;VERIFY THAT BIT 12 WAS SET
1930                                          ;CLEAR BIT 12
1931                                          ;VERIFY THAT BIT 12 WAS CLEARED
1932
1933  007416  012767  000340  170352  T71:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1934  007424  012767  004000  010266          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1935  007432  012767  007504  010254          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1936  007440  012777  004000  010204          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1937  007446  016703  010214                  MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
1938  007452  012705  002000                  MOV     #2000,R5                        ;BIT 12 WILL BE SET IN BREAK CONTROL
1939  007456  010513                          MOV     R5,(R3)                 ;SET BIT 12
1940  007460  011304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
1941  007462  020504                          CMP     R5,R4                   ;WAS BIT 12 SET
1942  007464  001401                          BEQ     1$
1943  007466  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
1944  007470  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 12
1945  007472  011304                          MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
1946  007474  005704                          TST     R4                      ;WAS BIT 12 CLEARED
1947  007476  001402                          BEQ     2$
1948  007500  005005                          CLR     R5
1949  007502  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
1950  007504  104400                  2$:     SCOPE
1951
1952                                          ;BREAK CONTROL REGISTER DATA TEST
1953                                          ;SET BIT 13 IN BREAK CONTROL TO 1
1954                                          ;VERIFY THAT BIT 13 WAS SET
1955                                          ;CLEAR BIT 13
1956                                          ;VERIFY THAT BIT 13 WAS CLEARED
1957
1958  007506  012767  000340  170262  T72:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1959  007514  012767  004000  010176          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1960  007522  012767  007574  010164          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1961  007530  012777  004000  010114          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1962  007536  016703  010124                  MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
1963  007542  012705  004000                  MOV     #4000,R5                        ;BIT 13 WILL BE SET IN BREAK CONTROL
1964  007546  010513                          MOV     R5,(R3)                 ;SET BIT 13
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1965  007550  011304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
1966  007552  020504                          CMP     R5,R4                   ;WAS BIT 13 SET
1967  007554  001401                          BEQ     1$
1968  007556  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
1969  007560  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 13
1970  007562  011304                          MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
1971  007564  005704                          TST     R4                      ;WAS BIT 13 CLEARED
1972  007566  001402                          BEQ     2$
1973  007570  005005                          CLR     R5
1974  007572  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
1975  007574  104400                  2$:     SCOPE
1976
1977                                          ;BREAK CONTROL REGISTER DATA TEST
1978                                          ;SET BIT 14 IN BREAK CONTROL TO 1
1979                                          ;VERIFY THAT BIT 14 WAS SET
1980                                          ;CLEAR BIT 14
1981                                          ;VERIFY THAT BIT 14 WAS CLEARED
1982
1983  007576  012767  000340  170172  T73:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1984  007604  012767  004000  010106          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1985  007612  012767  007664  010074          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1986  007620  012777  004000  010024          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1987  007626  016703  010034                  MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
1988  007632  012705  010000                  MOV     #10000,R5                       ;BIT 14 WILL BE SET IN BREAK CONTROL
1989  007636  010513                          MOV     R5,(R3)                 ;SET BIT 14
1990  007640  011304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
1991  007642  020504                          CMP     R5,R4                   ;WAS BIT 14 SET
1992  007644  001401                          BEQ     1$
1993  007646  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
1994  007650  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 14
1995  007652  011304                          MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
1996  007654  005704                          TST     R4                      ;WAS BIT 14 CLEARED
1997  007656  001402                          BEQ     2$
1998  007660  005005                          CLR     R5
1999  007662  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
2000  007664  104400                  2$:     SCOPE
2001
20
2003
2004
2005                                          ;CLEAR BIT 15
2006                                          ;VERIFY THAT BIT 15 WAS CLEARED
2007
2008  007666  012767  000340  170102  T74:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2009  007674  012767  004000  010016          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2010  007702  012767  007754  010004          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2011  007710  012777  004000  007734          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2012  007716  016703  007744                  MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
2013  007722  012705  020000                  MOV     #20000,R5                       ;BIT 15 WILL BE SET IN BREAK CONTROL
2014  007726  010513                          MOV     R5,(R3)                 ;SET BIT 15
2015  007730  011304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
2016  007732  020504                          CMP     R5,R4                   ;WAS BIT 15 SET
2017  007734  001401                          BEQ     1$
2018  007736  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
2019  007740  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 15
2020  007742  011304                          MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
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2021  007744  005704                        TST     R4                      ;WAS BIT 15 CLEARED
2022  007746  001402                        BEQ     2$
2023  007750  005005                        CLR     R5
2024  007752  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
2025  007754  104400                  2$:   SCOPE
2026
2027                                        ;BREAK CONTROL REGISTER DATA TEST
2028                                        ;SET BIT 16 IN BREAK CONTROL TO 1
2029                                        ;VERIFY THAT BIT 16 WAS SET
2030                                        ;CLEAR BIT 16
2031                                        ;VERIFY THAT BIT 16 WAS CLEARED
2032
2033  007756  012767  000340  170012  T75:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2034  007764  012767  004000  007726        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2035  007772  012767  010044  007714        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2036  010000  012777  004000  007644        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2037  010006  016703  007654               MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
2038  010012  012705  040000               MOV     #40000,R5                       ;BIT 16 WILL BE SET IN BREAK CONTROL
2039  010016  010513                       MOV     R5,(R3)                 ;SET BIT 16
2040  010020  011304                       MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
2041  010022  020504                       CMP     R5,R4                   ;WAS BIT 16 SET
2042  010024  001401                       BEQ     1$
2043  010026  104003                       HLT     3                       ;BREAK CONTROL REGISTER ERROR
2044  010030  040513                  1$:  BIC     R5,(R3)                 ;CLEAR BIT 16
2045  010032  011304                       MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
2046  010034  005704                       TST     R4                      ;WAS BIT 16 CLEARED
2047  010036  001402                       BEQ     2$
2048  010040  005005                       CLR     R5
2049  010042  104003                       HLT     3                       ;BREAK CONTROL REGISTER ERROR
2050  010044  104400                  2$:  SCOPE
2051
2052                                        ;BREAK CONTROL REGISTER DATA TEST
2053                                        ;SET BIT 17 IN BREAK CONTROL TO 1
2054                                        ;VERIFY THAT BIT 17 WAS SET
2055                                        ;CLEAR BIT 17
2056                                        ;VERIFY THAT BIT 17 WAS CLEARED
2057
2058  010046  012767  000340  167722  T76:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2059  010054  012767  004000  007636        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2060  010062  012767  010134  007624        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2061  010070  012777  004000  007554        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2062  010076  016703  007564               MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
2063  010102  012705  100000               MOV     #100000,R5                      ;BIT 17 WILL BE SET IN BREAK CONTROL
2064  010106  010513                       MOV     R5,(R3)                 ;SET BIT 17
2065  010110  011304                       MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
2066  010112  020504                       CMP     R5,R4                   ;WAS BIT 17 SET
2067  010114  001401                       BEQ     1$
2068  010116  104003                       HLT     3                       ;BREAK CONTROL REGISTER ERROR
2069  010120  040513                  1$:  BIC     R5,(R3)                 ;CLEAR BIT 17
2070  010122  011304                       MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
2071  010124  005704                       TST     R4                      ;WAS BIT 17 CLEARED
2072  010126  001402                       BEQ     2$
2073  010130  005005                       CLR     R5
2074  010132  104003                       HLT     3                       ;BREAK CONTROL REGISTER ERROR
2075  010134  104400                  2$:  SCOPE
2076
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2077                                            ;SILO STATUS REGISTER DATA TEST
2078                                            ;SET BIT 0 IN SILO STATUS TO 1
2079                                            ;VERIFY THAT BIT 0 WAS SET
2080                                            ;CLEAR BIT 0
2081                                            ;VERIFY THAT BIT 0 WAS CLEARED
2082
2083  010136  012767  000340  167632  T77:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2084  010144  012767  004000  007546          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2085  010152  012767  010234  007534          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2086  010160  012777  004000  007464          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2087  010166  016703  007476                  MOV     DHSSR,R3                ;SET UP POINTER TO SILO STATUS
2088  010172  012705  000001                  MOV     #1,R5                   ;BIT 0 WILL BE SET IN SILO STATUS
2089  010176  010513                          MOV     R5,(R3)                 ;SET BIT 0
2090  010200  011304                          MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
2091  010202  042704  000700                  BIC     #700,R4         ;CLEAR UNWANTED BITS
2092  010206  020504                          CMP     R5,R4                   ;WAS BIT 0 SET
2093  010210  001401                          BEQ     1$
2094  010212  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
2095  010214  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 0
2096  010216  011304                          MOV     (R3),R4                 ;READ CONTENTS OF SILO STATUS
2097  010220  042704  000700                  BIC     #700,R4         ;CLEAR UNWANTED BITS
2098  010224  005704                          TST     R4                      ;WAS BIT 0 CLEARED
2099  010226  001402                          BEQ     2$
2100  010230  005005                          CLR     R5
2101  010232  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
2102  010234  104400                  2$:     SCOPE
2103
2104                                            ;SILO STATUS REGISTER DATA TEST
2105                                            ;SET BIT 1 IN SILO STATUS TO 1
2106                                            ;VERIFY THAT BIT 1 WAS SET
2107                                            ;CLEAR BIT 1
2108                                            ;VERIFY THAT BIT 1 WAS CLEARED
2109
2110  010236  012767  000340  167532  T100:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2111  010244  012767  004000  007446          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2112  010252  012767  010334  007434          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2113  010260  012777  004000  007364          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2114  010266  016703  007376                  MOV     DHSSR,R3                ;SET UP POINTER TO SILO STATUS
2115  010272  012705  000002                  MOV     #2,R5                   ;BIT 1 WILL BE SET IN SILO STATUS
2116  010276  010513                          MOV     R5,(R3)                 ;SET BIT 1
2117  010300  011304                          MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
2118  010302  042704  000700                  BIC     #700,R4         ;CLEAR UNWANTED BITS
2119  010306  020504                          CMP     R5,R4                   ;WAS BIT 1 SET
2120  010310  001401                          BEQ     1$
2121  010312  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
2122  010314  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 1
2123  010316  011304                          MOV     (R3),R4                 ;READ CONTENTS OF SILO STATUS
2124  010320  042704  000700                  BIC     #700,R4         ;CLEAR UNWANTED BITS
2125  010324  005704                          TST     R4                      ;WAS BIT 1 CLEARED
2126  010326  001402                          BEQ     2$
2127  010330  005005                          CLR     R5
2128  010332  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
2129  010334  104400                  2$:     SCOPE
2130
2131                                            ;SILO STATUS REGISTER DATA TEST
2132                                            ;SET BIT 2 IN SILO STATUS TO 1
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2133                                            ;VERIFY THAT BIT 2 WAS SET
2134                                            ;CLEAR BIT 2
2135                                            ;VERIFY THAT BIT 2 WAS CLEARED
2136
2137  010336  012767  000340  167432  T101:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2138  010344  012767  004000  007346          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2139  010352  012767  010434  007334          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2140  010360  012777  004000  007264          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2141  010366  016703  007276                  MOV     DHSSR,R3                ;SET UP POINTER TO SILO STATUS
2142  010372  012705  000004                  MOV     #4,R5                   ;BIT 2 WILL BE SET IN SILO STATUS
2143  010376  010513                          MOV     R5,(R3)                 ;SET BIT 2
2144  010400  011304                          MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
2145  010402  042704  000700                  BIC     #700,R4         ;CLEAR UNWANTED BITS
2146  010406  020504                          CMP     R5,R4                   ;WAS BIT 2 SET
2147  010410  001401                          BEQ     1$
2148  010412  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
2149  010414  040513                  $:      BIC     R5,(R3)                 ;CLEAR BIT 2
2150  010416  011304                          MOV     (R3),R4                 ;READ CONTENTS OF SILO STATUS
2151  010420  042704  000700                  BIC     #700,R4         ;CLEAR UNWANTED BITS
2152  010424  005704                          TST     R4                      ;WAS BIT 2 CLEARED
2153  010426  001402                          BEQ     2$
2154  010430  005005                          CLR     R5
2155  010432  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
2156  010434  104400                  2$:     SCOPE
2157
2158                                            ;SILO STATUS REGISTER DATA TEST
2159                                            ;SET BIT 3 IN SILO STATUS TO 1
2160                                            ;VERIFY THAT BIT 3 WAS SET
2161                                            ;CLEAR BIT 3
2162                                            ;VERIFY THAT BIT 3 WAS CLEARED
2163
2164  010436  012767  000340  167332  T102:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2165  010444  012767  004000  007246          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2166  010452  012767  010534  007234          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2167  010460  012777  004000  007164          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2168  010466  016703  007176                  MOV     DHSSR,R3                ;SET UP POINTER TO SILO STATUS
2169  010472  012705  000010                  MOV     #10,R5                  ;BIT 3 WILL BE SET IN SILO STATUS
2170  010476  010513                          MOV     R5,(R3)                 ;SET BIT 3
2171  010500  011304                          MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
2172  010502  042704  000700                  BIC     #700,R4         ;CLEAR UNWANTED BITS
2173  010506  020504                          CMP     R5,R4                   ;WAS BIT 3 SET
2174  010510  001401                          BEQ     1$
2175  010512  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
2176  010514  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 3
2177  010516  011304                          MOV     (R3),R4                 ;READ CONTENTS OF SILO STATUS
2178  010520  042704  000700                  BIC     #700,R4         ;CLEAR UNWANTED BITS
2179  010524  005704                          TST     R4                      ;WAS BIT 3 CLEARED
2180  010526  001402                          BEQ     2$
2181  010530  005005                          CLR     R5
2182  010532  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
2183  010534  104400                  2$:     SCOPE
2184
2185                                            ;SILO STATUS REGISTER DATA TEST
2186                                            ;SET BIT 4 IN SILO STATUS TO 1
2187                                            ;VERIFY THAT BIT 4 WAS SET
2188                                            ;CLEAR BIT 4
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                                                ;VERIFY THAT BIT 4 WAS CLEARED

010536  012767  000340  167232  T103:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
010544  012767  004000  007146          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
010552  012767  010634  007134          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
010560  012777  004000  007064          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
010566  016703  007076                  MOV     DHSSR,R3                ;SET UP POINTER TO SILO STATUS
010572  012705  000020                  MOV     #20,R5                  ;BIT 4 WILL BE SET IN SILO STATUS
010576  010513                          MOV     R5,(R3)                 ;SET BIT 4
010600  011304                          MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
010602  042704  000700                  BIC     #700,R4         ;CLEAR UNWANTED BITS
010606  020504                          CMP     R5,R4                   ;WAS BIT 4 SET
010610  001401                          BEQ     1$
010612  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
010614  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 4
010616  011304                          MOV     (R3),R4                 ;READ CONTENTS OF SILO STATUS
010620  042704  000700                  BIC     #700,R4         ;CLEAR UNWANTED BITS
010624  005704                          TST     R4                      ;WAS BIT 4 CLEARED
010626  001402                          BEQ     2$
010630  005005                          CLR     R5
010632  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
010634  104400                  2$:     SCOPE

                                        ;SILO STATUS REGISTER DATA TEST
                                        ;SET BIT 5 IN SILO STATUS TO 1
                                        ;VERIFY THAT BIT 5 WAS SET
                                        ;CLEAR BIT 5
                                        ;VERIFY THAT BIT 5 WAS CLEARED

010636  012767  000340  167132  T104:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
010644  012767  004000  007046          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
010652  012767  010734  007034          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
010660  012777  004000  006764          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
010666  016703  006776                  MOV     DHSSR,R3                ;SET UP POINTER TO SILO STATUS
010672  012705  000040                  MOV     #40,R5                  ;BIT 5 WILL BE SET IN SILO STATUS
010676  010513                          MOV     R5,(R3)                 ;SET BIT 5
010700  011304                          MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
010702  042704  000700                  BIC     #700,R4         ;CLEAR UNWANTED BITS
010706  020504                          CMP     R5,R4                   ;WAS BIT 5 SET
010710  001401                          BEQ     1$
010712  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
010714  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 5
010716  011304                          MOV     (R3),R4                 ;READ CONTENTS OF SILO STATUS
010720  042704  000700                  BIC     #700,R4         ;CLEAR UNWANTED BITS
010724  005704                          TST     R4                      ;WAS BIT 5 CLEARED
010726  001402                          BEQ     2$
010730  005005                          CLR     R5
010732  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
010734  104400                  2$:     SCOPE

                                        ;SILO STATUS REGISTER DATA TEST
                                        ;SET BIT 17 IN SILO STATUS TO 1
                                        ;VERIFY THAT BIT 17 WAS SET
                                        ;CLEAR BIT 17
                                        ;VERIFY THAT BIT 17 WAS CLEARED
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2245  010736  012767  000340  167032  T105:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2246  010744  012767  004000  006746          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2247  010752  012767  011034  006734          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2248  010760  012777  004000  006664          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2249  010766  016703  006676                  MOV     DHSSR,R3                ;SET UP POINTER TO SILO STATUS
2250  010772  012705  100000                  MOV     #100000,R5                      ;BIT 17 WILL BE SET IN SILO STATUS
2251  010776  010513                          MOV     R5,(R3)                 ;SET BIT 17
2252  011000  011304                          MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
2253  011002  042704  000700                  BIC     #700,R4         ;CLEAR UNWANTED BITS
2254  011006  020504                          CMP     R5,R4                   ;WAS BIT 17 SET
2255  011010  001401                          BEQ     1$
2256  011012  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
2257  011014  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 17
2258  011016  011304                          MOV     (R3),R4                 ;READ CONTENTS OF SILO STATUS
2259  011020  042704  000700                  BIC     #700,R4         ;CLEAR UNWANTED BITS
2260  011024  005704                          TST     R4                      ;WAS BIT 17 CLEARED
2261  011026  001402                          BEQ     2$
2262  011030  005005                          CLR     R5
2263  011032  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
2264  011034  104400                  2$:     SCOPE
2265
2266                                          ;LINE PARAMETER REGISTER DATA TEST
2267                                          ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
2268                                          ;CLEAR BIT 0
2269                                          ;VERIFY THAT BIT 0 WAS CLEARED
2270                                          ;RESTORE BIT 0
2271                                          ;VERIFY THAT BIT 0 WAS SET
2272
2273  011036  012767  000340  166732  T106:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2274  011044  012767  004000  006646          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2275  011052  012767  011140  006634          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2276  011060  012777  004000  006564          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2277  011066  016703  006564                  MOV     DHLPR,R3                        ;SET UP POINTER TO LINE PARAMETER
2278  011072  012705  177766                  MOV     #177766,R5              ;(R5)=EXPECTED DATA
2279                                                                          ;IN LINE PARAMETER REGISTER, 177766
2280  011076  012713  177767                  MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
2281                                                                          ;IN LINE PARAMETER REGISTER
2282  011102  042713  000001                  BIC     #1,(R3)         ;CLEAR BIT 0
2283  011106  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
2284  011110  020504                          CMP     R5,R4                   ;WAS BIT 0 CLEARED
2285  011112  001401                          BEQ     1$
2286  011114  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
2287  011116  052713  000001          1$:     BIS     #1,(R3)         ;SET BIT 0
2288  011122  011304                          MOV     (R3),R4
2289  011124  022704  177767                  CMP     #177767,R4              ;WAS BIT 0 SET
2290  011130  001403                          BEQ     2$
2291  011132  012705  177767                  MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
2292                                                                          ;LINE PARAMETER REGISTER, 177767
2293  011136  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
2294  011140  104400                  2$:     SCOPE
2295
2296                                          ;LINE PARAMETER REGISTER DATA TEST
2297                                          ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
2298                                          ;CLEAR BIT 1
2299                                          ;VERIFY THAT BIT 1 WAS CLEARED
2300                                          ;RESTORE BIT 1
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                                                ;VERIFY THAT BIT 1 WAS SET

011142  012767  000340  166626  T107:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
011150  012767  004000  006542          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
011156  012767  011244  006530          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
011164  012777  004000  006460          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
011172  016703  006460                  MOV     DHLPR,R3                        ;SET UP POINTER TO LINE PARAMETER
011176  012705  177765                  MOV     #177765,R5              ;(R5)=EXPECTED DATA
                                                                        ;IN LINE PARAMETER REGISTER, 177765
011202  012713  177767                  MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
                                                                        ;IN LINE PARAMETER REGISTER
011206  042713  000002                  BIC     #2,(R3)         ;CLEAR BIT 1
011212  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
011214  020504                          CMP     R5,R4                   ;WAS BIT 1 CLEARED
011216  001401                          BEQ     1$
011220  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
011222  052713  000002          $:      BIS     #2,(R3)         ;SET BIT 1
011226  011304                          MOV     (R3),R4
011230  022704  177767                  CMP     #177767,R4              ;WAS BIT 1 SET
011234  001403                          BEQ     2$
011236  012705  177767                  MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
                                                                        ;LINE PARAMETER REGISTER, 177767
011242  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
011244  104400                  2$:     SCOPE

                                                ;LINE PARAMETER REGISTER DATA TEST
                                                ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
                                                ;CLEAR BIT 2
                                                ;VERIFY THAT BIT 2 WAS CLEARED
                                                ;RESTORE BIT 2
                                                ;VERIFY THAT BIT 2 WAS SET

011246  012767  000340  166522  T110:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
011254  012767  004000  006436          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
011262  012767  011350  006424          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
011270  012777  004000  006354          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
011276  016703  006354                  MOV     DHLPR,R3                        ;SET UP POINTER TO LINE PARAMETER
011302  012705  177763                  MOV     #177763,R5              ;(R5)=EXPECTED DATA
                                                                        ;IN LINE PARAMETER REGISTER, 177763
011306  012713  177767                  MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
                                                                        ;IN LINE PARAMETER REGISTER
011312  042713  000004                  BIC     #4,(R3)         ;CLEAR BIT 2
011316  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
011320  020504                          CMP     R5,R4                   ;WAS BIT 2 CLEARED
011322  001401                          BEQ     1$
011324  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
011326  052713  000004          1$:     BIS     #4,(R3)         ;SET BIT 2
011332  011304                          MOV     (R3),R4
011334  022704  177767                  CMP     #177767,R4              ;WAS BIT 2 SET
011340  001403                          BEQ     2$
011342  012705  177767                  MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
                                                                        ;LINE PARAMETER REGISTER, 177767
011346  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
011350  104400                  2$:     SCOPE

                                                ;LINE PARAMETER REGISTER DATA TEST
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                                        ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
                                        ;CLEAR BIT 4
                                        ;VERIFY THAT BIT 4 WAS CLEARED
                                        ;RESTORE BIT 4
                                        ;VERIFY THAT BIT 4 WAS SET

011352  012767  000340  166416  T111:  MOV     #340,PS             ;DISABLE ALL INTERRUPTS
011360  012767  004000  006332         MOV     #4000,ICOUNT        ;SET UP FOR 4000 ITERATIONS
011366  012767  011454  006320         MOV     #2$,ESCAPE          ;SET UP TO ESCAPE TO NEXT TEST
011374  012777  004000  006250         MOV     #BIT11,@DHSCR       ;MASTER CLEAR INTERFACE
011402  016703  006250                 MOV     DHLPR,R3                    ;SET UP POINTER TO LINE PARAMETER
011406  012705  177747                 MOV     #177747,R5          ;(R5)=EXPECTED DATA
                                                                    ;IN LINE PARAMETER REGISTER, 177747
011412  012713  17776                  MOV     #177767,(R3)        ;SET ALL READ/WRITE BITS
                                                                    ;IN LINE PARAMETER REGISTER
011416  042713  000020                 BIC     #20,(R3)            ;CLEAR BIT 4
011422  011304                         MOV     (R3),R4             ;GET CONTENTS OF LINE PARAMETER
011424  020504                         CMP     R5,R4               ;WAS BIT 4 CLEARED
011426  001401                         BEQ     1$
011430  104002                         HLT     2                   ;LINE PARAMETER REGISTER ERROR
011432  052713  000020         1$:     BIS     #20,(R3)            ;SET BIT 4
011436  011304                         MOV     (R3),R4
011440  022704  177767                 CMP     #177767,R4          ;WAS BIT 4 SET
011444  001403                         BEQ     2$
011446  012705  177767                 MOV     #177767,R5          ;(R5)=EXPECTED DATA IN
                                                                    ;LINE PARAMETER REGISTER, 177767
011452  104002                         HLT     2                   ;LINE PARAMETER REGISTER ERROR
011454  104400         2$:     SCOPE

                                        ;LINE PARAMETER REGISTER DATA TEST
                                        ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
                                        ;CLEAR BIT 5
                                        ;VERIFY THAT BIT 5 WAS CLEARED
                                        ;RESTORE BIT 5
                                        ;VERIFY THAT BIT 5 WAS SET

011456  012767  000340  166312  T112:  MOV     #340,PS             ;DISABLE ALL INTERRUPTS
011464  012767  004000  006226         MOV     #4000,ICOUNT        ;SET UP FOR 4000 ITERATIONS
011472  012767  011560  006214         MOV     #2$,ESCAPE          ;SET UP TO ESCAPE TO NEXT TEST
011500  012777  004000  006144         MOV     #BIT11,@DHSCR       ;MASTER CLEAR INTERFACE
011506  016703  006144                 MOV     DHLPR,R3                    ;SET UP POINTER TO LINE PARAMETER
011512  012705  177727                 MOV     #177727,R5          ;(R5)=EXPECTED DATA
                                                                    ;IN LINE PARAMETER REGISTER, 177727
011516  012713  177767                 MOV     #177767,(R3)        ;SET ALL READ/WRITE BITS
                                                                    ;IN LINE PARAMETER REGISTER
011522  042713  000040                 BIC     #40,(R3)            ;CLEAR BIT 5
011526  011304                         MOV     (R3),R4             ;GET CONTENTS OF LINE PARAMETER
011530  020504                         CMP     R5,R4               ;WAS BIT 5 CLEARED
011532  001401                         BEQ     1$
011534  104002                         HLT     2                   ;LINE PARAMETER REGISTER ERROR
011536  052713  000040         1$:     BIS     #40,(R3)            ;SET BIT 5
011542  011304                         MOV     (R3),R4
011544  022704  177767                 CMP     #177767,R4          ;WAS BIT 5 SET
011550  001403                         BEQ     2$
011552  012705  177767                 MOV     #177767,R5          ;(R5)=EXPECTED DATA IN
                                                                    ;LINE PARAMETER REGISTER, 177767
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2413  011556  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
2414  011560  104400                2$:     SCOPE
2415
2416                                        ;LINE PARAMETER REGISTER DATA TEST
2417                                        ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
2418                                        ;CLEAR BIT 6
2419                                        ;VERIFY THAT BIT 6 WAS CLEARED
2420                                        ;RESTORE BIT 6
2421                                        ;VERIFY THAT BIT 6 WAS SET
2422
2423  011562  012767  000340  166206  T113: MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2424  011570  012767  004000  006122        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2425  011576  012767  011664  006110        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2426  011604  012777  004000  006040        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2427  011612  016703  006040                MOV     DHLPR,R3                        ;SET UP POINTER TO LINE PARAMETER
2428  011616  012705  177667                MOV     #177667,R5              ;(R5)=EXPECTED DATA
2429                                                                          ;IN LINE PARAMETER REGISTER, 177667
2430  011622  012713  177767                MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
2431                                                                          ;IN LINE PARAMETER REGISTER
2432  011626  042713  000100                BIC     #100,(R3)               ;CLEAR BIT 6
2433  011632  011304                        MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
2434  011634  020504                        CMP     R5,R4                   ;WAS BIT 6 CLEARED
2435  011636  001401                        BEQ     1$
2436  011640  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
2437  011642  052713  000100          1$:   BIS     #100,(R3)               ;SET BIT 6
2438  011646  011304                        MOV     (R3),R4
2439  011650  022704  177767                CMP     #177767,R4              ;WAS BIT 6 SET
2440  011654  001403                        BEQ     2$
2441  011656  012705  177767                MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
2442                                                                          ;LINE PARAMETER REGISTER, 177767
2443  011662  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
2444  011664  104400                2$:     SCOPE
2445
2446                                        ;LINE PARAMETER REGISTER DATA TEST
2447                                        ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
2448                                        ;CLEAR BIT 7
2449                                        ;VERIFY THAT BIT 7 WAS CLEARED
2450                                        ;RESTORE BIT 7
2451                                        ;VERIFY THAT BIT 7 WAS SET
2452
2453  011666  012767  000340  166102  T114: MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2454  011674  012767  004000  006016        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2455  011702  012767  011770  006004        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2456  011710  012777  004000  005734        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2457  011716  016703  005734                MOV     DHLPR,R3                        ;SET UP POINTER TO LINE PARAMETER
2458  011722  012705  177567                MOV     #177567,R5              ;(R5)=EXPECTED DATA
2459                                                                          ;IN LINE PARAMETER REGISTER, 177567
2460  011726  012713  177767                MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
2461                                                                          ;IN LINE PARAMETER REGISTER
2462  011732  042713  000200                BIC     #200,(R3)               ;CLEAR BIT 7
2463  011736  011304                        MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
2464  011740  020504                        CMP     R5,R4                   ;WAS BIT 7 CLEARED
2465  011742  001401                        BEQ     1$
2466  011744  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
2467  011746  052713  000200          1$:   BIS     #200,(R3)               ;SET BIT 7
2468  011752  011304                        MOV     (R3),R4
```

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2469  011754  022704  177767              CMP     #177767,R4              ;WAS BIT 7 SET
2470  011760  001403                      BEQ     2$
2471  011762  012705  177767              MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
2472                                                                        ;LINE PARAMETER REGISTER, 177767
2473  011766  104002                      HLT     2                       ;LINE PARAMETER REGISTER ERROR
2474  011770  104400              2$:     SCOPE
2475
2476                                      ;LINE PARAMETER REGISTER DATA TEST
2477                                      ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
2478                                      ;CLEAR BIT 10
2479                                      ;VERIFY THAT BIT 10 WAS CLEARED
2480                                      ;RESTORE BIT 10
2481                                      ;VERIFY THAT BIT 10 WAS SET
2482
2483  011772  012767  000340  165776  T115: MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2484  012000  012767  004000  005712      MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2485  012006  012767  012074  005700      MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2486  012014  012777  004000  005630      MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2487  012022  016703  005630              MOV     DHLPR,R3                        ;SET UP POINTER TO LINE PARAMETER
2488  012026  012705  177367              MOV     #177367,R5              ;(R5)=EXPECTED DATA
2489                                                                        ;IN LINE PARAMETER REGISTER, 177367
2490  012032  012713  177767              MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
2491                                                                        ;IN LINE PARAMETER REGISTER
2492  012036  042713  000400              BIC     #400,(R3)               ;CLEAR BIT 10
2493  012042  011304                      MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
2494  012044  020504                      CMP     R5,R4                   ;WAS BIT 10 CLEARED
2495  012046  001401                      BEQ     1$
2496  012050  104002                      HLT     2                       ;LINE PARAMETER REGISTER ERROR
2497  012052  052713  000400      1$:     BIS     #400,(R3)               ;SET BIT 10
2498  012056  011304                      MOV     (R3),R4
2499  012060  022704  177767              CMP     #177767,R4              ;WAS BIT 10 SET
2500  012064  001403                      BEQ     2$
2501  012066  012705  177767              MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
2502                                                                        ;LINE PARAMETER REGISTER, 177767
2503  012072  104002                      HLT     2                       ;LINE PARAMETER REGISTER ERROR
2504  012074  104400              2$:     SCOPE
2505
2506                                      ;LINE PARAMETER REGISTER DATA TEST
2507                                      ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
2508                                      ;CLEAR BIT 11
2509                                      ;VERIFY THAT BIT 11 WAS CLEARED
2510                                      ;RESTORE BIT 11
2511                                      ;VERIFY THAT BIT 11 WAS SET
2512
2513  012076  012767  000340  165672  T116: MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2514  012104  012767  004000  005606      MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2515  012112  012767  012200  005574      MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2516  012120  012777  004000  005524      MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2517  012126  016703  005524              MOV     DHLPR,R3                        ;SET UP POINTER TO LINE PARAMETER
2518  012132  012705  176767              MOV     #176767,R5              ;(R5)=EXPECTED DATA
2519                                                                        ;IN LINE PARAMETER REGISTER, 176767
2520  012136  012713  177767              MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
2521                                                                        ;IN LINE PARAMETER REGISTER
2522  012142  042713  001000              BIC     #1000,(R3)              ;CLEAR BIT 11
2523  012146  011304                      MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
2524  012150  020504                      CMP     R5,R4                   ;WAS BIT 11 CLEARED
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 2525  012152  001401                          BEQ     1$
 2526  012154  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
 2527  012156  052713  001000          1$:     BIS     #1000,(R3)              ;SET BIT 11
 2528  012162  011304                          MOV     (R3),R4
 2529  012164  022704  177767                  CMP     #177767,R4              ;WAS BIT 11 SET
 2530  012170  001403                          BEQ     2$
 2531  012172  012705  177767                  MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
 2532                                                                          ;LINE PARAMETER REGISTER, 177767
 2533  012176  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
 2534  012200  104400          2$:             SCOPE
 2535
 2536                                          ;LINE PARAMETER REGISTER DATA TEST
 2537                                          ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
 2538                                          ;CLEAR BIT 12
 2539                                          ;VERIFY THAT BIT 12 WAS CLEARED
 2540                                          ;RESTORE BIT 12
 2541                                          ;VERIFY THAT BIT 12 WAS SET
 2542
 2543  012202  012767  000340  165566  T117:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
 2544  012210  012767  004000  005502          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
 2545  012216  012767  012304  005470          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
 2546  012224  012777  004000  005420          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
 2547  012232  016703  005420                  MOV     DHLPR,R3                        ;SET UP POINTER TO LINE PARAMETER
 2548  012236  012705  175767                  MOV     #175767,R5              ;(R5)=EXPECTED DATA
 2549                                                                          ;IN LINE PARAMETER REGISTER, 175767
 2550  012242  012713  177767                  MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
 2551                                                                          ;IN LINE PARAMETER REGISTER
 2552  012246  042713  002000                  BIC     #2000,(R3)              ;CLEAR BIT 12
 2553  012252  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
 2554  012254  02^504                          CMP     R5,R4                   ;WAS BIT 12 CLEARED
 2555  012256  001401                          BEQ     1$
 2556  012260  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
 2557  012262  052713  002000          1$:     BIS     #2000,(R3)              ;SET BIT 12
 2558  012266  011304                          MOV     (R3),R4
 2559  012270  022704  177767                  CMP     #177767,R4              ;WAS BIT 12 SET
 2560  012274  001403                          BEQ     2$
 2561  012276  012705  177767                  MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
 2562                                                                          ;LINE PARAMETER REGISTER, 177767
 2563  012302  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
 2564  012304  04400           2$:             SCOPE
 2565
 2566                                          ;LINE PARAMETER REGISTER DATA TEST
 2567                                          ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
 2568                                          ;CLEAR BIT 13
 2569                                          ;VERIFY THAT BIT 13 WAS CLEARED
 2570                                          ;RESTORE BIT 13
 2571                                          ;VERIFY THAT BIT 13 WAS SE
 2572
 2573  012306  012767  000340  165462  T120:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
 2574  012314  012767  004000  005376          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
 2575  012322  012767  012410  005364          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NFXT TEST
 2576  012330  012777  004000  005314          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
 2577  012336  016703  005314                  MOV     DHLPR,R3                        ;SET UP POINTER TO LINE PARAMETER
 2578  012342  012705  173767                  MOV     #173767,R5              ;(R5)=EXPECTED DATA
 2579                                                                          ;IN LINE PARAMETER REGISTER, 173767
 2580  012346  012713  177767                  MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
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2581
2582  012352  042713  004000              BIC     #4000,(R3)              ;IN LINE PARAMETER REGISTER
2583  012356  011304                      MOV     (R3),R4                 ;CLEAR BIT 13
2584  012360  020504                      CMP     R5,R4                   ;GET CONTENTS OF LINE PARAMETER
2585  012362  001401                      BEQ     1$                      ;WAS BIT 13 CLEARED
2586  012364  104002                      HLT     2                       ;LINE PARAMETER REGISTER ERROR
2587  012366  052713  004000      1$:     BIS     #4000,(R3)              ;SET BIT 13
2588  012372  011304                      MOV     (R3),R4
2589  012374  022704  177767              CMP     #177767,R4              ;WAS BIT 13 SET
2590  012400  001403                      BEQ     2$
2591  012402  012705  177767              MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
2592                                                                      ;LINE PARAMETER REGISTER, 177767
2593  012406  104002                      HLT     2                       ;LINE PARAMETER REGISTER ERROR
2594  012410  104400      2$:             SCOPE
2595
2596                                      ;LINE PARAMETER REGISTER DATA TEST
2597                                      ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
2598                                      ;CLEAR BIT 14
2599                                      ;VERIFY THAT BIT 14 WAS CLEARED
2600                                      ;RESTORE BIT 14
2601                                      ;VERIFY THAT BIT 14 WAS SET
2602
2603  012412  012767  000340  165356  T121:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2604  012420  012767  004000  005272       MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2605  012426  012767  012514  005260       MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2606  012434  012777  004000  005210       MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2607  012442  016703  005210              MOV     DHLPR,R3                        ;SET UP POINTER TO LINE PARAMETER
2608  012446  012705  167767              MOV     #167767,R5              ;(R5)=EXPECTED DATA
2609                                                                      ;IN LINE PARAMETER REGISTER, 167767
2610  012452  012713  177767              MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
2611                                                                      ;IN LINE PARAMETER REGISTER
2612  012456  042713  010000              BIC     #10000,(R3)             ;CLEAR BIT 14
2613  012462  011304                      MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
2614  012464  020504                      CMP     R5,R4                   ;WAS BIT 14 CLEARED
2615  012466  001401                      BEQ     1$
2616  012470  104002                      HLT     2                       ;LINE PARAMETER REGISTER ERROR
2617  012472  052713  010000      1$:     BIS     #10000,(R3)             ;SET BIT 14
2618  012476  011304                      MOV     (R3),R4
2619  012500  022704  177767              CMP     #177767,R4              ;WAS BIT 14 SET
2620  012504  001403                      BEQ     2$
2621  012506  012705  177767              MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
2622                                                                      ;LINE PARAMETER REGISTER, 177767
2623  012512  104002                      HLT     2                       ;LINE PARAMETER REGISTER ERROR
2624  012514  104400      2$:             SCOPE
2625
2626                                      ;LINE PARAMETER REGISTER DATA TEST
2627                                      ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
2628                                      ;CLEAR BIT 15
2629                                      ;VERIFY THAT BIT 15 WAS CLEARED
2630                                      ;RESTORE BIT 15
2631                                      ;VERIFY THAT BIT 15 WAS SET
2632
2633  012516  012767  000340  165252  T122:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2634  012524  012767  004000  005166       MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2635  012532  012767  012620  005154       MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2636  012540  012777  004000  005104       MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
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2637  012546  016703  005104                  MOV     DHLPR,R3                        ;SET UP POINTER TO LINE PARAMETER
2638  012552  012705  157767                  MOV     #157767,R5              ;(R5)=EXPECTED DATA
2639                                                                            ;IN LINE PARAMETER REGISTER, 157767
2640  012556  012713  177767                  MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
2641                                                                            ;IN LINE PARAMETER REGISTER
2642  012562  042713  020000                  BIC     #20000,(R3)             ;CLEAR BIT 15
2643  012566  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
2644  012570  020504                          CMP     R5,R4                   ;WAS BIT 15 CLEARED
2645  012572  001401                          BEQ     1$
2646  012574  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
2647  012576  052713  020000          1$:     BIS     #20000,(R3)             ;SET BIT 15
2648  012602  011304                          MOV     (R3),R4
2649  012604  022704  177767                  CMP     #177767,R4              ;WAS BIT 15 SET
2650  012610  001403                          BEQ     2$
2651  012612  012705  177767                  MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
2652                                                                            ;LINE PARAMETER REGISTER, 177767
2653  012616  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
2654  012620  104400                  2$:     SCOPE
2655
2656                                          ;LINE PARAMETER REGISTER DATA TEST
2657                                          ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
2658                                          ;CLEAR BIT 16
2659                                          ;VERIFY THAT BIT 16 WAS CLEARED
2660                                          ;RESTORE BIT 16
2661                                          ;VERIFY THAT BIT 16 WAS SET
2662
2663  012622  012767  000340  165146  T123:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2664  012630  012767  004000  005062          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2665  012636  012767  012724  005050          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2666  012644  012777  004000  005000          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2667  012652  016703  005000                  MOV     DHLPR,R3                        ;SET UP POINTER TO LINE PARAMETER
2668  012656  012705  137767                  MOV     #137767,R5              ;(R5)=EXPECTED DATA
2669                                                                            ;IN LINE PARAMETER REGISTER, 137767
2670  012662  012713  177767                  MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
2671                                                                            ;IN LINE PARAMETER REGISTER
2672  012666  042713  040000                  BIC     #40000,(R3)             ;CLEAR BIT 16
2673  012672  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
2674  012674  020504                          CMP     R5,R4                   ;WAS BIT 16 CLEARED
2675  012676  001401                          BEQ     1$
2676  012700  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
2677  012702  052713  040000          1$:     BIS     #40000,(R3)             ;SET BIT 16
2678  012706  011304                          MOV     (R3),R4
2679  012710  022704  177767                  CMP     #177767,R4              ;WAS BIT 16 SET
2680  012714  001403                          BEQ     2$
2681  012716  012705  177767                  MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
2682                                                                            ;LINE PARAMETER REGISTER, 177767
2683  012722  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
2684  012724  104400                  2$:     SCOPE
2685
2686                                          ;LINE PARAMETER REGISTER DATA TEST
2687                                          ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
2688                                          ;CLEAR BIT 17
2689                                          ;VERIFY THAT BIT 17 WAS CLEARED
2690                                          ;RESTORE BIT 17
2691                                          ;VERIFY THAT BIT 17 WAS SET
2692
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2693  012726  012767  000340  165042  T124:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2694  012734  012767  004000  004756          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2695  012742  012767  013030  004744          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2696  012750  012777  004000  004674          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2697  012756  016703  004674                  MOV     DHLPR,R3                        ;SET UP POINTER TO LINE PARAMETER
2698  012762  012705  077767                  MOV     #77767,R5               ;(R5)=EXPECTED DATA
2699                                                                           ;IN LINE PARAMETER REGISTER, 77767
2700  012766  012713  177767                  MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
2701                                                                           ;IN LINE PARAMETER REGISTER
2702  012772  042713  100000                  BIC     #100000,(R3)            ;CLEAR BIT 17
2703  012776  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
2704  013000  020504                          CMP     R5,R4                   ;WAS BIT 17 CLEARED
2705  013002  001401                          BEQ     1$
2706  013004  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
2707  013006  052713  100000          1$:     BIS     #100000,(R3)            ;SET BIT 17
2708  013012  011304                          MOV     (R3),R4
2709  013014  022704  177767                  CMP     #177767,R4              ;WAS BIT 17 SET
2710  013020  001403                          BEQ     2$
2711  013022  012705  177767                  MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
2712                                                                           ;LINE PARAMETER REGISTER, 177767
2713  013026  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
2714  013030  104400                  2$:     SCOPE
2715
2716                                          ;BREAK CONTROL REGISTER DATA TEST
2717                                          ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
2718                                          ;CLEAR BIT 0
2719                                          ;VERIFY THAT BIT 0 WAS CLEARED
2720                                          ;RESTORE BIT 0
2721                                          ;VERIFY THAT BIT 0 WAS SET
2722
2723  013032  012767  000340  164736  T125:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2724  013040  012767  004000  004652          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2725  013046  012767  013134  004640          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2726  013054  012777  004000  004570          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2727  013062  016703  004600                  MOV     DHBCR,R3                        ;SET UP POINTER TO BREAK CONTROL
2728  013066  012705  177776                  MOV     #177776,R5              ;(R5)=EXPECTED DATA
2729                                                                           ;IN BREAK CONTROL REGISTER, 177776
2730  013072  012713  177777                  MOV     #177777,(R3)            ;SET ALL READ/WRITE BITS
2731                                                                           ;IN BREAK CONTROL REGISTER
2732  013076  042713  000001                  BIC     #1,(R3)         ;CLEAR BIT 0
2733  013102  011304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
2734  013104  020504                          CMP     R5,R4                   ;WAS BIT 0 CLEARED
2735  013106  001401                          BEQ     1$
2736  013110  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
2737  013112  052713  000001          1$:     BIS     #1,(R3)         ;SET BIT 0
2738  013116  011304                          MOV     (R3),R4
2739  013120  022704  177777                  CMP     #177777,R4              ;WAS BIT 0 SET
2740  013124  001403                          BEQ     2$
2741  013126  012705  177777                  MOV     #177777,R5              ;(R5)=EXPECTED DATA IN
2742                                                                           ;BREAK CONTROL REGISTER, 177777
2743  013132  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
2744  013134  104400                  2$:     SCOPE
2745
2746                                          ;BREAK CONTROL REGISTER DATA TEST
2747                                          ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
2748                                          ;CLEAR BIT 1
```

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2749                                            ;VERIFY THAT BIT 1 WAS CLEARED
2750                                            ;RESTORE BIT 1
2751                                            ;VERIFY THAT BIT 1 WAS SET
2752
2753  013136  012767  000340  164632  T126:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2754  013144  012767  004000  004546            MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2755  013152  012767  013240  004534            MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2756  013160  012777  004000  004464            MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2757  013166  016703  004474                    MOV     DHBCR,R3                        ;SET UP POINTER TO BREAK CONTROL
2758  013172  012705  177775                    MOV     #177775,R5              ;(R5)=EXPECTED DATA
2759                                                                            ;IN BREAK CONTROL REGISTER, 177775
2760  013176  012713  177777                    MOV     #177777,(R3)            ;SET ALL READ/WRITE BITS
2761                                                                            ;IN BREAK CONTROL REGISTER
2762  013202  042713  000002                    BIC     #2,(R3)         ;CLEAR BIT 1
2763  013206  011304                            MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
2764  013210  020504                            CMP     R5,R4                   ;WAS BIT 1 CLEARED
2765  013212  001401                            BEQ     1$
2766  013214  104003                            HLT     3                       ;BREAK CONTROL REGISTER ERROR
2767  013216  052713  000002            1$:     BIS     #2,(R3)         ;SET BIT 1
2768  013222  011304                            MOV     (R3),R4
2769  013224  022704  177777                    CMP     #177777,R4              ;WAS BIT 1 SET
2770  013230  001403                            BEQ     2$
2771  013232  012705  177777                    MOV     #177777,R5              ;(R5)=EXPECTED DATA IN
2772                                                                            ;BREAK CONTROL REGISTER, 177777
2773  013236  104003                            HLT     3                       ;BREAK CONTROL REGISTER ERROR
2774  013240  104400            2$:             SCOPE
2775
2776                                            ;BREAK CONTROL REGISTER DATA TEST
2777                                            ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
2778                                            ;CLEAR BIT 2
2779                                            ;VERIFY THAT BIT 2 WAS CLEARED
2780                                            ;RESTORE BIT 2
2781                                            ;VERIFY THAT BIT 2 WAS SET
2782
2783  013242  012767  000340  164526  T127:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2784  013250  012767  004000  004442            MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2785  013256  012767  013344  004430            MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2786  013264  012777  004000  004360            MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2787  013272  016703  004370                    MOV     DHBCR,R3                        ;SET UP POINTER TO BREAK CONTROL
2788  013276  012705  177773                    MOV     #177773,R5              ;(R5)=EXPECTED DATA
2789                                                                            ;IN BREAK CONTROL REGISTER, 177773
2790  013302  012713  177777                    MOV     #177777,(R3)            ;SET ALL READ/WRITE BITS
2791                                                                            ;IN BREAK CONTROL REGISTER
2792  013306  042713  000004                    BIC     #4,(R3)         ;CLEAR BIT 2
2793  013312  011304                            MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
2794  013314  020504                            CMP     R5,R4                   ;WAS BIT 2 CLEARED
2795  013316  001401                            BEQ     1$
2796  013320  104003                            HLT     3                       ;BREAK CONTROL REGISTER ERROR
2797  013322  052713  000004            1$:     BIS     #4,(R3)         ;SET BIT 2
2798  013326  011304                            MOV     (R3),R4
2799  013330  022704  177777                    CMP     #177777,R4              ;WAS BIT 2 SET
2800  013334  001403                            BEQ     2$
2801  013336  012705  177777                    MOV     #177777,R5              ;(R5)=EXPECTED DATA IN
2802                                                                            ;BREAK CONTROL REGISTER, 177777
2803  013342  104003                            HLT     3                       ;BREAK CONTROL REGISTER ERROR
2804  013344  104400            2$:             SCOPE
```

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2805
2806                                        ;BREAK CONTROL REGISTER DATA TEST
2807                                        ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
2808                                        ;CLEAR BIT 3
2809                                        ;VERIFY THAT BIT 3 WAS CLEARED
2810                                        ;RESTORE BIT 3
2811                                        ;VERIFY THAT BIT 3 WAS SET
2812
2813  013346  012767  000340  164422  T130: MOV   #340,PS               ;DISABLE ALL INTERRUPTS
2814  013354  012767  004000  004336        MOV   #4000,ICOUNT          ;SET UP FOR 4000 ITERATIONS
2815  013362  012767  013450  004324        MOV   #2$,ESCAPE            ;SET UP TO ESCAPE TO NEXT TEST
2816  013370  012777  004000  004254        MOV   #BIT11,@DHSCR         ;MASTER CLEAR INTERFACE
2817  013376  016703  004264               MOV   DHBCR,R3                      ;SET UP POINTER TO BREAK CONTROL
2818  013402  012705  177767               MOV   #177767,R5            ;(R5)=EXPECTED DATA
2819                                                                    ;IN BREAK CONTROL REGISTER, 177767
2820  013406  012713  177777               MOV   #177777,(R3)          ;SET ALL READ/WRITE BITS
2821                                                                    ;IN BREAK CONTROL REGISTER
2822  013412  042713  000010               BIC   #10,(R3)              ;CLEAR BIT 3
2823  013416  011304                       MOV   (R3),R4               ;GET CONTENTS OF BREAK CONTROL
2824  013420  020504                       CMP   R5,R4                 ;WAS BIT 3 CLEARED
2825  013422  001401                       BEQ   1$
2826  013424  104003                       HLT   3                     ;BREAK CONTROL REGISTER ERROR
2827  013426  052713  000010         1$:   BIS   #10,(R3)              ;SET BIT 3
2828  013432  011304                       MOV   (R3),R4
2829  013434  022704  177777               CMP   #177777,R4            ;WAS BIT 3 SET
2830  013440  001403                       BEQ   2$
2831  013442  012705  177777               MOV   #177777,R5            ;(R5)=EXPECTED DATA IN
2832                                                                    ;BREAK CONTROL REGISTER, 177777
2833  013446  104003                       HLT   3                     ;BREAK CONTROL REGISTER ERROR
2834  013450  104400                 2$:   SCOPE
2835
2836                                        ;BREAK CONTROL REGISTER DATA TEST
2837                                        ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
2838                                        ;CLEAR BIT 4
2839                                        ;VERIFY THAT BIT 4 WAS CLEARED
2840                                        ;RESTORE BIT 4
2841                                        ;VERIFY THAT BIT 4 WAS SET
2842
2843  013452  012767  000340  164316  T131: MOV   #340,PS               ;DISABLE ALL INTERRUPTS
2844  013460  012767  004000  004232        MOV   #4000,ICOUNT          ;SET UP FOR 4000 ITERATIONS
2845  013466  012767  013554  004220        MOV   #2$,ESCAPE            ;SET UP TO ESCAPE TO NEXT TEST
2846  013474  012777  004000  004150        MOV   #BIT11,@DHSCR         ;MASTER CLEAR INTERFACE
2847  013502  016703  004160               MOV   DHBCR,R3                      ;SET UP POINTER TO BREAK CONTROL
2848  013506  012705  177757               MOV   #177757,R5            ;(R5)=EXPECTED DATA
2849                                                                    ;IN BREAK CONTROL REGISTER, 177757
2850  013512  012713  177777               MOV   #177777,(R3)          ;SET ALL READ/WRITE BITS
2851                                                                    ;IN BREAK CONTROL REGISTER
2852  013516  042713  000020               BIC   #20,(R3)              ;CLEAR BIT 4
2853  013522  011304                       MOV   (R3),R4               ;GET CONTENTS OF BREAK CONTROL
2854  013524  020504                       CMP   R5,R4                 ;WAS BIT 4 CLEARED
2855  013526  001401                       BEQ   1$
2856  013530  104003                       HLT   3                     ;BREAK CONTROL REGISTER ERROR
2857  013532  052713  000020         1$:   BIS   #20,(R3)              ;SET BIT 4
2858  013536  011304                       MOV   (R3),R4
2859  013540  022704  177777               CMP   #177777,R4            ;WAS BIT 4 SET
2860  013544  001403                       BEQ   2$
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2861  013546  012705  177777                  MOV     #177777,R5              ;(R5)=EXPECTED DATA IN
2862                                                                          ;BREAK CONTROL REGISTER, 177777
2863  013552  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
2864  013554  104400              2$:         SCOPE
2865
2866                                          ;BREAK CONTROL REGISTER DATA TEST
2867                                          ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
2868                                          ;CLEAR BIT 5
2869                                          ;VERIFY THAT BIT 5 WAS CLEARED
2870                                          ;RESTORE BIT 5
2871                                          ;VERIFY THAT BIT 5 WAS SET
2872
2873  013556  012767  000340  164212  T132:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2874  013564  012767  004000  004126          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2875  013572  012767  013660  004114          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2876  013600  012777  004000  004044          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2877  013606  016703  004054                  MOV     DHBCR,R3                        ;SET UP POINTER TO BREAK CONTROL
2878  013612  012705  177737                  MOV     #177737,R5              ;(R5)=EXPECTED DATA
2879                                                                          ;IN BREAK CONTROL REGISTER, 177737
2880  013616  012713  177777                  MOV     #177777,(R3)            ;SET ALL READ/WRITE BITS
2881                                                                          ;IN BREAK CONTROL REGISTER
2882  013622  042713  000040                  BIC     #40,(R3)                ;CLEAR BIT 5
2883  013626  011304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
2884  013630  020504                          CMP     R5,R4                   ;WAS BIT 5 CLEARED
2885  013632  001401                          BEQ     1$
2886  013634  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
2887  013636  052713  000040          1$:     BIS     #40,(R3)                ;SET BIT 5
2888  013642  011304                          MOV     (R3),R4
2889  013644  022704  177777                  CMP     #177777,R4              ;WAS BIT 5 SET
2890  013650  001403                          BEQ     2$
2891  013652  012705  177777                  MOV     #177777,R5              ;(R5)=EXPECTED DATA IN
2892                                                                          ;BREAK CONTROL REGISTER, 177777
2893  013656  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
2894  013660  104400              2$:         SCOPE
2895
2896                                          ;BREAK CONTROL REGISTER DATA TEST
2897                                          ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
2898                                          ;CLEAR BIT 6
2899                                          ;VERIFY THAT BIT 6 WAS CLEARED
2900                                          ;RESTORE BIT 6
2901                                          ;VERIFY THAT BIT 6 WAS SET
2902
2903  013662  012767  000340  164106  T133:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2904  013670  012767  004000  004022          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2905  013676  012767  013764  004010          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2906  013704  012777  004000  003740          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2907  013712  016703  003750                  MOV     DHBCR,R3                        ;SET UP POINTER TO BREAK CONTROL
2908  013716  012705  177677                  MOV     #177677,R5              ;(R5)=EXPECTED DATA
2909                                                                          ;IN BREAK CONTROL REGISTER, 177677
2910  013722  012713  177777                  MOV     #177777,(R3)            ;SET ALL READ/WRITE BITS
2911                                                                          ;IN BREAK CONTROL REGISTER
2912  013726  042713  000100                  BIC     #100,(R3)               ;CLEAR BIT 6
2913  013732  011304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
2914  013734  020504                          CMP     R5,R4                   ;WAS BIT 6 CLEARED
2915  013736  001401                          BEQ     1$
2916  013740  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
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2917  013742  052713  000100          1$:     BIS     #100,(R3)               ;SET BIT 6
2918  013746  011304                          MOV     (R3),R4
2919  013750  022704  177777                  CMP     #177777,R4              ;WAS BIT 6 SET
2920  013754  001403                          BEQ     2$
2921  013756  012705  177777                  MOV     #177777,R5              ;(R5)=EXPECTED DATA IN
2922                                                                          ;BREAK CONTROL REGISTER, 177777
2923  013762  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
2924  013764  104400                  2$:     SCOPE
2925
2926                                          ;BREAK CONTROL REGISTER DATA TEST
2927                                          ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
2928                                          ;CLEAR BIT 7
2929                                          ;VERIFY THAT BIT 7 WAS CLEARED
2930                                          ;RESTORE BIT 7
2931                                          ;VERIFY THAT BIT 7 WAS SET
2932
2933  013766  012767  000340  164002  T134:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2934  013774  012767  004000  003716          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2935  014002  012767  014070  003704          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2936  014010  012777  004000  003634          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2937  014016  016703  003644                  MOV     DHBCR,R3                        ;SET UP POINTER TO BREAK CONTROL
2938  014022  012705  177577                  MOV     #177577,R5              ;(R5)=EXPECTED DATA
2939                                                                          ;IN BREAK CONTROL REGISTER, 177577
2940  014026  012713  177777                  MOV     #177777,(R3)            ;SET ALL READ/WRITE BITS
2941                                                                          ;IN BREAK CONTROL REGISTER
2942  014032  042713  000200                  BIC     #200,(R3)               ;CLEAR BIT 7
2943  014036  011304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
2944  014040  020504                          CMP     R5,R4                   ;WAS BIT 7 CLEARED
2945  014042  001401                          BEQ     1$
2946  014044  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
2947  014046  052713  000200          1$:     BIS     #200,(R3)               ;SET BIT 7
2948  014052  011304                          MOV     (R3),R4
2949  014054  022704  177777                  CMP     #177777,R4              ;WAS BIT 7 SET
2950  014060  001403                          BEQ     2$
2951  014062  012705  177777                  MOV     #177777,R5              ;(R5)=EXPECTED DATA IN
2952                                                                          ;BREAK CONTROL REGISTER, 177777
2953  014066  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
2954  014070  104400                  2$:     SCOPE
2955
2956                                          ;BREAK CONTROL REGISTER DATA TEST
2957                                          ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
2958                                          ;CLEAR BIT 10
2959                                          ;VERIFY THAT BIT 10 WAS CLEARED
2960                                          ;RESTORE BIT 10
2961                                          ;VERIFY THAT BIT 10 WAS SET
2962
2963  014072  012767  000340  163676  T135:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2964  014100  012767  004000  003612          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2965  014106  012767  014174  003600          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2966  014114  012777  004000  003530          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2967  014122  016703  003540                  MOV     DHBCR,R3                        ;SET UP POINTER TO BREAK CONTROL
2968  014126  012705  177377                  MOV     #177377,R5              ;(R5)=EXPECTED DATA
2969                                                                          ;IN BREAK CONTROL REGISTER, 177377
2970  014132  012713  177777                  MOV     #177777,(R3)            ;SET ALL READ/WRITE BITS
2971                                                                          ;IN BREAK CONTROL REGISTER
2972  014136  042713  000400                  BIC     #400,(R3)               ;CLEAR BIT 10
```

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2973  014142  0' 304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
2974  014144  020504                          CMP     R5,R4                   ;WAS BIT 10 CLEARED
2975  014146  001401                          BEQ     1$
2976  014150  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
2977  014152  052713  000400          1$:     BIS     #400,(R3)               ;SET BIT 10
2978  014156  011304                          MOV     (R3),R4
2979  014160  022704  177777                  CMP     #177777,R4              ;WAS BIT 10 SET
2980  014164  001403                          BEQ     2$
2981  014166  012705  177777                  MOV     #177777,R5              ;(R5)=EXPECTED DATA IN
2982                                                                          ;BREAK CONTROL REGISTER, 177777
2983  014172  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
2984  014174  104400                  2$:     SCOPE
2985
2986                                          ;BREAK CONTROL REGISTER DATA TEST
2987                                          ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
2988                                          ;CLEAR BIT 11
2989                                          ;VERIFY THAT BIT 11 WAS CLEARED
2990                                          ;RESTORE BIT 11
2991                                          ;VERIFY THAT BIT 11 WAS SET
2992
2993  014176  012767  000340  163572  T136:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2994  014204  012767  004000  003506          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2995  014212  012767  014300  003474          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2996  014220  012777  004000  003424          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2997  014226  016703  003434                  MOV     DHBCR,R3                        ;SET UP POINTER TO BREAK CONTROL
2998  014232  012705  176777                  MOV     #176777,R5              ;(R5)=EXPECTED DATA
2999                                                                          ;IN BREAK CONTROL REGISTER, 176777
3000  014236  012713  177777                  MOV     #177777,(R3)            ;SET ALL READ/WRITE BITS
3001                                                                          ;IN BREAK CONTROL REGISTER
3002  014242  042713  001000                  BIC     #1000,(R3)              ;CLEAR BIT 11
3003  014246  011304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
3004  014250  020504                          CMP     R5,R4                   ;WAS BIT 11 CLEARED
3005  014252  001401                          BEQ     1$
3006  014254  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
3007  014256  052713  001000          1$:     BIS     #1000,(R3)              ;SET BIT 11
3008  014262  011304                          MOV     (R3),R4
3009  014264  022704  177777                  CMP     #177777,R4              ;WAS BIT 11 SET
3010  014270  001403                          BEQ     2$
3011  014272  012705  177777                  MOV     #177777,R5              ;(R5)=EXPECTED DATA IN
3012                                                                          ;BREAK CONTROL REGISTER, 177777
3013  014276  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
3014  014300  104400                  2$:     SCOPE
3015
3016                                          ;BREAK CONTROL REGISTER DATA TEST
3017                                          ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
3018                                          ;CLEAR BIT 12
3019                                          ;VERIFY THAT BIT 12 WAS CLEARED
3020                                          ;RESTORE BIT 12
3021                                          ;VERIFY THAT BIT 12 WAS SET
3022
3023  014302  012767  000340  163466  T137:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3024  014310  012767  004000  003402          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
3025  014316  012767  014404  003370          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3026  014324  012777  004000  003320          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3027  014332  016703  003330                  MOV     DHBCR,R3                        ;SET UP POINTER TO BREAK CONTROL
3028  014336  012705  175777                  MOV     #175777,R5              ;(R5)=EXPECTED DATA
```

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3029
3030  014342  012713  177777                MOV     #177777,(R3)            ;IN BREAK CONTROL REGISTER, 175777
3031                                                                          ;SET ALL READ/WRITE BITS
3032  014346  042713  002000                BIC     #2000,(R3)              ;IN BREAK CONTROL REGISTER
3033  014352  011304                        MOV     (R3),R4                 ;CLEAR BIT 12
3034  014354  020504                        CMP     R5,R4                   ;GET CONTENTS OF BREAK CONTROL
3035  014356  001401                        BEQ     1$                      ;WAS BIT 12 CLEARED
3036  014360  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
3037  014362  052713  002000          1$:   BIS     #2000,(R3)              ;SET BIT 12
3038  014366  011304                        MOV     (R3),R4
3039  014370  022704  177777                CMP     #177777,R4              ;WAS BIT 12 SET
3040  014374  001403                        BEQ     2$
3041  014376  012705  177777                MOV     #177777,R5              ;(R5)=EXPECTED DATA IN
3042                                                                          ;BREAK CONTROL REGISTER, 177777
3043  014402  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
3044  014404  104400          2$:   SCOPE
3045
3046                                ;BREAK CONTROL REGISTER DATA TEST
3047                                ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
3048                                ;CLEAR BIT 13
3049                                ;VERIFY THAT BIT 13 WAS CLEARED
3050                                ;RESTORE BIT 13
3051                                ;VERIFY THAT BIT 13 WAS SET
3052
3053  014406  012767  000340  163362  T140:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3054  014414  012767  004000  003276        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
3055  014422  012767  014510  003264        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3056  014430  012777  004000  003214        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3057  014436  016703  003224                MOV     DHBCR,R3                        ;SET UP POINTER TO BREAK CONTROL
3058  014442  012705  173777                MOV     #173777,R5              ;(R5)=EXPECTED DATA
3059                                                                          ;IN BREAK CONTROL REGISTER, 173777
3060  014446  012713  177777                MOV     #177777,(R3)            ;SET ALL READ/WRITE BITS
3061                                                                          ;IN BREAK CONTROL REGISTER
3062  014452  042713  004000                BIC     #4000,(R3)              ;CLEAR BIT 13
3063  014456  011304                        MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
3064  014460  020504                        CMP     R5,R4                   ;WAS BIT 13 CLEARED
3065  014462  001401                        BEQ     1$
3066  014464  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
3067  014466  052713  004000          1$:   BIS     #4000,(R3)              ;SET BIT 13
3068  014472  011304                        MOV     (R3),R4
3069  014474  022704  177777                CMP     #177777,R4              ;WAS BIT 13 SET
3070  014500  001403                        BEQ     2$
3071  014502  012705  177777                MOV     #177777,R5              ;(R5)=EXPECTED DATA IN
3072                                                                          ;BREAK CONTROL REGISTER, 177777
3073  014506  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
3074  014510  104400          2$:   SCOPE
3075
3076                                ;BREAK CONTROL REGISTER DATA TEST
3077                                ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
3078                                ;CLEAR BIT 14
3079                                ;VERIFY THAT BIT 14 WAS CLEARED
3080                                ;RESTORE BIT 14
3081                                ;VERIFY THAT BIT 14 WAS SET
3082
3083  014512  012767  000340  163256  T141:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3084  014520  012767  004000  003172        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
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3085  014526  012767  014614  003160          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3086  014534  012777  004000  003110          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3087  014542  016703  003120                  MOV     DHBCR,R3                        ;SET UP POINTER TO BREAK CONTROL
3088  014546  012705  167777                  MOV     #167777,R5              ;(R5)=EXPECTED DATA
3089                                                                           ;IN BREAK CONTROL REGISTER, 167777
3090  014552  012713  177777                  MOV     #177777,(R3)            ;SET ALL READ/WRITE BITS
3091                                                                           ;IN BREAK CONTROL REGISTER
3092  014556  042713  010000                  BIC     #10000,(R3)             ;CLEAR BIT 14
3093  014562  011304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
3094  014564  020504                          CMP     R5,R4                   ;WAS BIT 14 CLEARED
3095  014566  001401                          BEQ     1$
3096  014570  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
3097  014572  052713  010000          1$:     BIS     #10000,(R3)             ;SET BIT 14
3098  014576  011304                          MOV     (R3),R4
3099  014600  022704  177777                  CMP     #177777,R4              ;WAS BIT 14 SET
3100  014604  001403                          BEQ     2$
3101  014606  012705  177777                  MOV     #177777,R5              ;(R5)=EXPECTED DATA IN
3102                                                                           ;BREAK CONTROL REGISTER, 177777
3103  014612  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
3104  014614  104400          2$:     SCOPE
3105
3106                                  ;BREAK CONTROL REGISTER DATA TEST
3107                                  ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
3108                                  ;CLEAR BIT 15
3109                                  ;VERIFY THAT BIT 15 WAS CLEARED
3110                                  ;RESTORE BIT 15
3111                                  ;VERIFY THAT BIT 15 WAS SET
3112
3113  014616  012767  000340  163152  T142:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3114  014624  012767  004000  003066          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
3115  014632  012767  014720  003054          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3116  014640  012777  004000  003004          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3117  014646  016703  003014                  MOV     DHBCR,R3                        ;SET UP POINTER TO BREAK CONTROL
3118  014652  012705  157777                  MOV     #157777,R5              ;(R5)=EXPECTED DATA
3119                                                                           ;IN BREAK CONTROL REGISTER, 157777
3120  014656  012713  177777                  MOV     #177777,(R3)            ;SET ALL READ/WRITE BITS
3121                                                                           ;IN BREAK CONTROL REGISTER
3122  014662  042713  020000                  BIC     #20000,(R3)             ;CLEAR BIT 15
3123  014666  011304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
3124  014670  020504                          CMP     R5,R4                   ;WAS BIT 15 CLEARED
3125  014672  001401                          BEQ     1$
3126  014674  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
3127  014676  052713  020000          1$:     BIS     #20000,(R3)             ;SET BIT 15
3128  014702  011304                          MOV     (R3),R4
3129  014704  022704  177777                  CMP     #177777,R4              ;WAS BIT 15 SET
3130  014710  001403                          BEQ     2$
3131  014712  012705  177777                  MOV     #177777,R5              ;(R5)=EXPECTED DATA IN
3132                                                                           ;BREAK CONTROL REGISTER, 177777
3133  014716  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
3134  014720  104400          2$:     SCOPE
3135
3136                                  ;BREAK CONTROL REGISTER DATA TEST
3137                                  ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
3138                                  ;CLEAR BIT 16
3139                                  ;VERIFY THAT BIT 16 WAS CLEARED
3140                                  ;RESTORE BIT 16
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                                        ;VERIFY THAT BIT 16 WAS SET

014722  012767  000340  163046  T143:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
014730  012767  004000  002762         MOV     #4000,ICUUNT            ;SET UP FOR 4000 ITERATIONS
014736  012767  015024  002750         MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
014744  012777  004000  002700         MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
014752  016703  002710                 MOV     DHBCR,R3                        ;SET UP POINTER TO BREAK CONTROL
014756  012705  137777                 MOV     #137777,R5              ;(R5)=EXPECTED DATA
                                                                        ;IN BREAK CONTROL REGISTER, 137777
014762  012713  177777                 MOV     #177777,(R3)            ;SET ALL READ/WRITE BITS
                                                                        ;IN BREAK CONTROL REGISTER
014766  042713  040000                 BIC     #40000,(R3)             ;CLEAR BIT 16
014772  011304                         MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
014774  020504                         CMP     R5,R4                   ;WAS BIT 16 CLEARED
014776  001401                         BEQ     1$
015000  104003                         HLT     3                       ;BREAK CONTROL REGISTER ERROR
015002  052713  040000          $:     BIS     #40000,(R3)             ;SET BIT 16
015006  011304                         MOV     (R3),R4
015010  022704  177777                 CMP     #177777,R4              ;WAS BIT 16 SET
015014  001403                         BEQ     2$
015016  012705  177777                 MOV     #177777,R5              ;(R5)=EXPECTED DATA IN
                                                                        ;BREAK CONTROL REGISTER, 177777
015022  104003                         HLT     3                       ;BREAK CONTROL REGISTER ERROR
015024  104400                 2$:    SCOPE

                                        ;BREAK CONTROL REGISTER DATA TEST
                                        ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
                                        ;CLEAR BIT 17
                                        ;VERIFY THAT BIT 17 WAS CLEARED
                                        ;RESTORE BIT 17
                                        ;VERIFY THAT BIT 17 WAS SET

015026  012767  000340  162742  T144:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
015034  012767  004000  002656         MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
015042  012767  015130  002644         MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
015050  012777  004000  002574         MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
015056  016703  002604                 MOV     DHBCR,R3                        ;SET UP POINTER TO BREAK CONTROL
015062  012705  077777                 MOV     #77777,R5               ;(R5)=EXPECTED DATA
                                                                        ;IN BREAK CONTROL REGISTER, 77777
015066  012713  177777                 MOV     #177777,(R3)            ;SET ALL READ/WRITE BITS
                                                                        ;IN BREAK CONTROL REGISTER
015072  042713  100000                 BIC     #100000,(R3)            ;CLEAR BIT 17
015076  011304                         MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
015100  020504                         CMP     R5,R4                   ;WAS BIT 17 CLEARED
015102  001401                         BEQ     1$
015104  104003                         HLT     3                       ;BREAK CONTROL REGISTER ERROR
015106  052713  100000          1$:    BIS     #100000,(R3)            ;SET BIT 17
015112  011304                         MOV     (R3),R4
015114  022704  177777                 CMP     #177777,R4              ;WAS BIT 17 SET
015120  001403                         BEQ     2$
015122  012705  177777                 MOV     #177777,R5              ;(R5)=EXPECTED DATA IN
                                                                        ;BREAK CONTROL REGISTER, 177777
015126  104003                         HLT     3                       ;BREAK CONTROL REGISTER ERROR
015130  104400                 2$:    SCOPE

                                        ;SILO STATUS REGISTER DATA TEST
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3197                                            ;SET ALL READ/WRITE BITS IN SILO STATUS REGISTER TO 1S
3198                                            ;CLEAR BIT 0
3199                                            ;VERIFY THAT BIT 0 WAS CLEARED
3200                                            ;RESTORE BIT 0
3201                                            ;VERIFY THAT BIT 0 WAS SET
3202
3203  015132  012767  000340  162636  T145:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3204  015140  012767  004000  002552          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
3205  015146  012767  015244  002540          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3206  015154  012777  004000  002470          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3207  015162  016703  002502                  MOV     DHSSR,R3                        ;SET UP POINTER TO SILO STATUS
3208  015166  012705  100076                  MOV     #CLRBIT,R5              ;(R5)=EXPECTED DATA
3209                                                                          ;IN SILO STATUS REGISTER, CLRBIT
3210  015172  012713  100077                  MOV     #100077,(R3)            ;SET ALL READ/WRITE BITS
3211                                                                          ;IN SILO STATUS REGISTER
3212  015176  042713  000001                  BIC     #1,(R3)         ;CLEAR BIT 0
3213  015202  011304                          MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
3214  015204  042704  077700                  BIC     #77700,R4               ;CLEAR UNWANTED BITS
3215  015210  020504                          CMP     R5,R4                   ;WAS BIT 0 CLEARED
3216  015212  001401                          BEQ     1$
3217  015214  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
3218  015216  052713  000001          1$:     BIS     #1,(R3)         ;SET BIT 0
3219  015222  011304                          MOV     (R3),R4
3220  015224  042704  077700                  BIC     #77700,R4               ;CLEAR UNWANTED BITS
3221  015230  022704  100077                  CMP     #100077,R4              ;WAS BIT 0 SET
3222  015234  001403                          BEQ     2$
3223  015236  012705  100077                  MOV     #100077,R5              ;(R5)=EXPECTED DATA IN
3224                                                                          ;SILO STATUS REGISTER, 100077
3225  015242  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
3226  015244  104400          2$:     SCOPE
3227
3228                                            ;SILO STATUS REGISTER DATA TEST
3229                                            ;SET ALL READ/WRITE BITS IN SILO STATUS REGISTER TO 1S
3230                                            ;CLEAR BIT 1
3231                                            ;VERIFY THAT BIT 1 WAS CLEARED
3232                                            ;RESTORE BIT 1
3233                                            ;VERIFY THAT BIT 1 WAS SET
3234
3235  015246  012767  000340  162522  T146:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3236  015254  012767  004000  002436          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
3237  015262  012767  015360  002424          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3238  015270  012777  004000  002354          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3239  015276  016703  002366                  MOV     DHSSR,R3                        ;SET UP POINTER TO SILO STATUS
3240  015302  012705  100075                  MOV     #CLRBIT,R5              ;(R5)=EXPECTED DATA
3241                                                                          ;IN SILO STATUS REGISTER, CLRBIT
3242  015306  012713  100077                  MOV     #100077,(R3)            ;SET ALL READ/WRITE BITS
3243                                                                          ;IN SILO STATUS REGISTER
3244  015312  042713  000002                  BIC     #2,(R3)         ;CLEAR BIT 1
3245  015316  011304                          MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
3246  015320  042704  077700                  BIC     #77700,R4               ;CLEAR UNWANTED BITS
3247  015324  020504                          CMP     R5,R4                   ;WAS BIT 1 CLEARED
3248  015326  001401                          BEQ     1$
3249  015330  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
3250  015332  052713  000002          1$:     BIS     #2,(R3)         ;SET BIT 1
3251  015336  011304                          MOV     (R3),R4
3252  015340  042704  077700                  BIC     #77700,R4               ;CLEAR UNWANTED BITS
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3253  015344  022704  100077                    CMP     #100077,R4              ;WAS BIT 1 SET
3254  015350  001403                            BEQ     2$
3255  015352  012705  100077                    MOV     #100077,R5              ;(R5)=EXPECTED DATA IN
3256                                                                            ;SILO STATUS REGISTER, 100077
3257  015356  104004                            HLT     4                       ;SILO STATUS REGISTER ERROR
3258  015360  104400                    2$:     SCOPE
3259
3260                                            ;SILO STATUS REGISTER DATA TEST
3261                                            ;SET ALL READ/WRITE BITS IN SILO STATUS REGISTER TO 1S
3262                                            ;CLEAR BIT 2
3263                                            ;VERIFY THAT BIT 2 WAS CLEARED
3264                                            ;RESTORE BIT 2
3265                                            ;VERIFY THAT BIT 2 WAS SET
3266
3267  015362  012767  000340  162406    T147:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3268  015370  012767  004000  002322            MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
3269  015376  012767  015474  002310            MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3270  015404  012777  004000  002240            MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3271  015412  016703  002252                    MOV     DHSSR,R3                        ;SET UP POINTER TO SILO STATUS
3272  015416  012705  100073                    MOV     #CLRBIT,R5              ;(R5)=EXPECTED DATA
3273                                                                            ;IN SILO STATUS REGISTER, CLRBIT
3274  015422  012713  100077                    MOV     #100077,(R3)            ;SET ALL READ/WRITE BITS
3275                                                                            ;IN SILO STATUS REGISTER
3276  015426  042713  000004                    BIC     #4,(R3)         ;CLEAR BIT 2
3277  015432  011304                            MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
3278  015434  042704  077700                    BIC     #77700,R4               ;CLEAR UNWANTED BITS
3279  015440  020504                            CMP     R5,R4                   ;WAS BIT 2 CLEARED
3280  015442  001401                            BEQ     1$
3281  015444  104004                            HLT     4                       ;SILO STATUS REGISTER ERROR
3282  015446  052713  000004            1$:     BIS     #4,(R3)         ;SET BIT 2
3283  015452  011304                            MOV     (R3),R4
3284  015454  042704  077700                    BIC     #77700,R4               ;CLEAR UNWANTED BITS
3285  015460  022704  100077                    CMP     #100077,R4              ;WAS BIT 2 SET
3286  015464  001403                            BEQ     2$
3287  015466  012705  100077                    MOV     #100077,R5              ;(R5)=EXPECTED DATA IN
3288                                                                            ;SILO STATUS REGISTER, 100077
3289  015472  104004                            HLT     4                       ;SILO STATUS REGISTER ERROR
3290  015474  104400                    2$:     SCOPE
3291
3292                                            ;SILO STATUS REGISTER DATA TEST
3293                                            ;SET ALL READ/WRITE BITS IN SILO STATUS REGISTER TO 1S
3294                                            ;CLEAR BIT 3
3295                                            ;VERIFY THAT BIT 3 WAS CLEARED
3296                                            ;RESTORE BIT 3
3297                                            ;VERIFY THAT BIT 3 WAS SET
3298
3299  015476  012767  000340  162272    T150:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3300  015504  012767  004000  002206            MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
3301  015512  012767  015610  002174            MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3302  015520  012777  004000  002124            MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3303  015526  016703  002136                    MOV     DHSSR,R3                        ;SET UP POINTER TO SILO STATUS
3304  015532  012705  100067                    MOV     #CLRBIT,R5              ;(R5)=EXPECTED DATA
3305                                                                            ;IN SILO STATUS REGISTER, CLRBIT
3306  015536  012713  100077                    MOV     #100077,(R3)            ;SET ALL READ/WRITE BITS
3307                                                                            ;IN SILO STATUS REGISTER
3308  015542  042713  000010                    BIC     #10,(R3)                ;CLEAR BIT 3
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3309  015546  011304                          MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
3310  015550  042704  077700                  BIC     #77700,R4               ;CLEAR UNWANTED BITS
3311  015554  020504                          CMP     R5,R4                   ;WAS BIT 3 CLEARED
3312  015556  001401                          BEQ     1$
3313  015560  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
3314  015562  052713  000010          1$:     BIS     #10,(R3)                ;SET BIT 3
3315  015566  011304                          MOV     (R3),R4
3316  015570  042704  077700                  BIC     #77700,R4               ;CLEAR UNWANTED BITS
3317  015574  022704  100077                  CMP     #100077,R4              ;WAS BIT 3 SET
3318  015600  001403                          BEQ     2$
3319  015602  012705  100077                  MOV     #100077,R5              ;(R5)=EXPECTED DATA IN
3320                                                                          ;SILO STATUS REGISTER, 100077
3321  015606  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
3322  015610  104400                  2$:     SCOPE
3323
3324                                          ;SILO STATUS REGISTER DATA TEST
3325                                          ;SET ALL READ/WRITE BITS IN SILO STATUS REGISTER TO 1S
3326                                          ;CLEAR BIT 4
3327                                          ;VERIFY THAT BIT 4 WAS CLEARED
3328                                          ;RESTORE BIT 4
3329                                          ;VERIFY THAT BIT 4 WAS SET
3330
3331  015612  012767  000340  162156  T151:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3332  015620  012767  004000  002072          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
3333  015626  012767  015724  002060          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3334  015634  012777  004000  002010          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3335  015642  016703  002022                  MOV     DHSSR,R3                        ;SET UP POINTER TO SILO STATUS
3336  015646  012705  100057                  MOV     #CLRBIT,R5              ;(R5)=EXPECTED DATA
3337                                                                          ;IN SILO STATUS REGISTER, CLRBIT
3338  015652  012713  100077                  MOV     #100077,(R3)            ;SET ALL READ/WRITE BITS
3339                                                                          ;IN SILO STATUS REGISTER
3340  015656  042713  000020                  BIC     #20,(R3)                ;CLEAR BIT 4
3341  015662  011304                          MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
3342  015664  042704  077700                  BIC     #77700,R4               ;CLEAR UNWANTED BITS
3343  015670  020504                          CMP     R5,R4                   ;WAS BIT 4 CLEARED
3344  015672  001401                          BEQ     1$
3345  015674  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
3346  015676  052713  000020          1$:     BIS     #20,(R3)                ;SET BIT 4
3347  015702  011304                          MOV     (R3),R4
3348  015704  042704  077700                  BIC     #77700,R4               ;CLEAR UNWANTED BITS
3349  015710  022704  100077                  CMP     #100077,R4              ;WAS BIT 4 SET
3350  015714  001403                          BEQ     2$
3351  015716  012705  100077                  MOV     #100077,R5              ;(R5)=EXPECTED DATA IN
3352                                                                          ;SILO STATUS REGISTER, 100077
3353  015722  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
3354  015724  104400                  2$:     SCOPE
3355
3356                                          ;SILO STATUS REGISTER DATA TEST
3357                                          ;SET ALL READ/WRITE BITS IN SILO STATUS REGISTER TO 1S
3358                                          ;CLEAR BIT 5
3359                                          ;VERIFY THAT BIT 5 WAS CLEARED
3360                                          ;RESTORE BIT 5
3361                                          ;VERIFY THAT BIT 5 WAS SET
3362
3363  015726  012767  000340  162042  T152:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3364  015734  012767  004000  001756          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
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3365  015742  012767  016040  001744          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3366  015750  012777  004000  001674          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3367  015756  016703  001706                  MOV     DHSSR,R3                        ;SET UP POINTER TO SILO STATUS
3368  015762  012705  100037                  MOV     #CLRBIT,R5              ;(R5)=EXPECTED DATA
3369                                                                          ;IN SILO STATUS REGISTER, CLRBIT
3370  015766  012713  100077                  MOV     #100077,(R3)            ;SET ALL READ/WRITE BITS
3371                                                                          ;IN SILO STATUS REGISTER
3372  015772  042713  000040                  BIC     #40,(R3)                ;CLEAR BIT 5
3373  015776  011304                          MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
3374  016000  042704  077700                  BIC     #77700,R4               ;CLEAR UNWANTED BITS
3375  016004  020504                          CMP     R5,R4                   ;WAS BIT 5 CLEARED
3376  016006  001401                          BEQ     1$
3377  016010  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
3378  016012  052713  000040          1$:     BIS     #40,(R3)                ;SET BIT 5
3379  016016  011304                          MOV     (R3),R4
3380  016020  042704  077700                  BIC     #77700,R4               ;CLEAR UNWANTED BITS
3381  016024  022704  100077                  CMP     #100077,R4              ;WAS BIT 5 SET
3382  016030  001403                          BEQ     2$
3383  016032  012705  100077                  MOV     #100077,R5              ;(R5)=EXPECTED DATA IN
3384                                                                          ;SILO STATUS REGISTER, 100077
3385  016036  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
3386  016040  104400          2$:     SCOPE
3387
3388                                  ;SILO STATUS REGISTER DATA TEST
3389                                  ;SET ALL READ/WRITE BITS IN SILO STATUS REGISTER TO 1S
3390                                  ;CLEAR BIT 17
3391                                  ;VERIFY THAT BIT 17 WAS CLEARED
3392                                  ;RESTORE BIT 17
3393                                  ;VERIFY THAT BIT 17 WAS SET
3394
3395  016042  012767  000340  161726  T153:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3396  016050  012767  004000  001642          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
3397  016056  012767  016154  001630          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3398  016064  012777  004000  001560          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3399  016072  016703  001572                  MOV     DHSSR,R3                        ;SET UP POINTER TO SILO STATUS
3400  016076  012705  000077                  MOV     #CLRBIT,R5              ;(R5)=EXPECTED DATA
3401                                                                          ;IN SILO STATUS REGISTER, CLRBIT
3402  016102  012713  100077                  MOV     #100077,(R3)            ;SET ALL READ/WR.TE BITS
3403                                                                          ;IN SILO STATUS REGISTER
3404  016106  042713  100000                  BIC     #100000,(R3)            ;CLEAR BIT 17
3405  016112  011304                          MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
3406  016114  042704  077700                  BIC     #77700,R4               ;CLEAR UNWANTED BITS
3407  016120  020504                          CMP     R5,R4                   ;WAS BIT 17 CLEARED
3408  016122  001401                          BEQ     1$
3409  016124  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
3410  016126  052713  100000          1$:     BIS     #100000,(R3)            ;SET BIT 17
3411  016132  011304                          MOV     (R3),R4
3412  016134  042704  077700                  BIC     #77700,R4               ;CLEAR UNWANTED BITS
3413  016140  022704  100077                  CMP     #100077,R4              ;WAS BIT 17 SET
3414  016144  001403                          BEQ     2$
3415  016146  012705  100077                  MOV     #100077,R5              ;(R5)=EXPECTED DATA IN
3416                                                                          ;SILO STATUS REGISTER, 100077
3417  016152  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
3418  016154  104400          2$:     SCOPE
```

```
3419
3420                                        ;SYSTEM CONTROL REGISTER MOVE-BYTE TEST (PART 1)
3421                                        ;ISSUE A MASTER CLEAR
3422                                        ;MOVE A BYTE TO SET INTERRUPT ENABLE BITS
3423                                        ;       IN UPPER BYTE OF SYSTEM CONTROL
3424                                        ;VERIFY BITS SET CORRECTLY
3425                                        ;MOVE A BYTE TO SET INTERRUPT ENABLE BIT
3426                                        ;       IN LOWER BYTE OF SYSTEM CONTROL
3427                                        ;VERIFY UPPER BYTE WAS NOT AFFECTED
3428
3429  016156  012706  021360          T154:  MOV     #STACK, SP      ;SET UP STACK
3430  016162  012767  000340  161606         MOV     #340,   PS      ;LOCK OUT INTERRUPTS
3431  016170  012767  016300  001516         MOV     #99$,   ESCAPE  ;SET UP TO ESCAPE TO NEXT TEST
3432  016176  012767  004000  001514         MOV     #4000,  ICOUNT  ;SET UP FOR 4000 ITERATIONS
3433  016204  052777  004000  001440         BIS     #BIT11, @DHSCR  ;ISSUE MASTER CLEAR
3434  016212  016703  001434                 MOV     DHSCR,  R3      ;(R3)=SYSTEM CONTROL REGISTER ADDRESS
3435  016216  005203                         INC     R3              ;       UPPER BYTE
3436  016220  112713  000060                 MOVB    #60,    (R3)    ;SET INTERRUPT ENABLE BITS
3437                                                                  ;IN UPPER BYTE OF SYSTEM CONTROL
3438  016224  022777  030000  001420         CMP     #BIT13+BIT12,@DHSCR     ;VERIFY BITS SET CORRECTLY
3439  016232  001406                         BEQ     2$              ;BRANCH IF OK
3440  016234  012705  030000                 MOV     #BIT13+BIT12,R5 ;(R5)=REGISTER EXPECTED DATA
3441  016240  017704  001406                 MOV     @DHSCR, R4      ;(R4)=REGISTER ACTUAL DATA
3442  016244  104001                         HLT     1               ;BITS DID NOT SET CORRECTLY
3443  016246  000414                         BR      99$             ;BRANCH TO SCOPE
3444  016250  112777  000100  001374  2$:    MOVB    #BIT06, @DHSCR  ;SET INTERRUPT ENABLE BIT
3445                                                                  ;IN LOWER BYTE OF SYSTEM CONTROL
3446  016256  022777  030100  001366         CMP     #BIT13+BIT12+BIT06,@DHSCR       ;VERIFY BITS SET CORRECTLY
3447  016264  001405                         BEQ     99$             ;BRANCH IF OK
3448  016266  012705  030100                 MOV     #BIT13+BIT12+BIT06,R5   ;(R5)=REGISTER EXPECTED DATA
3449  016272  017704  001354                 MOV     @DHSCR, R4      ;(R4)=REGISTER ACTUAL DATA
3450  016276  104001                         HLT     1               ;UPPER BYTE WAS AFFECTED?
3451  016300  104400                 99$:    SCOPE                   ;CHECK FOR ITERATIONS,LOOP
3452
3453                                        ;SYSTEM CONTROL REGISTER MOVE-BYTE TEST (PART 2)
3454                                        ;ISSUE MASTER CLEAR
3455                                        ;MOVE A BYTE TO SET LINE SELECT BITS
3456                                        ;       IN LOWER BYTE OF SYSTEM CONTROL
3457                                        ;VERIFY BITS SET CORRECTLY
3458                                        ;MOVE A BYTE TO SET THE MAINTENANCE BIT
3459                                        ;       IN UPPER BYTE OF SYSTEM CONTROL
3460                                        ;VERIFY LOWER BYTE WAS NOT AFFECTED
3461
3462  016302  012706  021360          T155:  MOV     #STACK, SP      ;SET UP STACK
3463  016306  012767  000340  161462         MOV     #340,   PS      ;LOCK OUT INTERRUPTS
3464  016314  012767  016424  001372         MOV     #99$,   ESCAPE  ;SET UP TO ESCAPE TO NEXT TEST
3465  016322  012767  004000  001370         MOV     #4000,  ICOUNT  ;SET UP FOR 4000 ITERATIONS
3466  016330  052777  004000  001314         BIS     #BIT11, @DHSCR  ;ISSUE MASTER CLEAR
3467  016336  016703  001310                 MOV     DHSCR,  R3      ;(R3)=SYSTEM CONTROL REGISTER ADDRESS
3468  016342  005203                         INC     R3              ;       UPPER BYTE
3469  016344  112777  000017  001300         MOVB    #17,    @DHSCR  ;SET LINE SELECT BITS
3470                                                                  ;IN LOWER BYTE OF SYSTEM CONTROL
3471  016352  022777  000017  001272         CMP     #17,    @DHSCR  ;VERIFY BITS SET CORRECTLY
3472  016360  001406                         BEQ     2$              ;BRANCH IF OK
3473  016362  012705  000017                 MOV     #17,    R5      ;(R5)=REGISTER EXPECTED DATA
3474  016366  017704  001260                 MOV     @DHSCR, R4      ;(R40=REGISTER ACTUAL DATA
```

```
3475  016372  104001                          HLT     1               ;BITS DID NOT SET CORRECTLY
3476  016374  000413                          BR      99$             ;BRANCH TO SCOPE
3477  016376  112713  000002          2$:     MOVB    #2,     (R3)    ;SET MAINTENANCE BIT
3478                                                                  ;       IN UPPER BYTE OF SYSTEM CONTROL
3479  016402  022777  001017  001242          CMP     #1017,  @DHSCR  ;VERIFY BITS SET CORRECTLY
3480  016410  001405                          BEQ     99$             ;BRANCH IF OK
3481  016412  012705  001017                  MOV     #1017,  R5      ;(R5)=REGISTER EXPECTED DATA
3482  016416  017704  001230                  MOV     @DHSCR, R4      ;(R4)=REGISTER ACTUAL DATA
3483  016422  104001                          HLT     1               ;LOWER BYTE WAS AFFECTED?
3484  016424  104400                  99$:    SCOPE                   ;CHECK FOR ITERATIONS,LOOP
3485
3486
3487                                          ;END OF PASS
3488                                          ;TYPE NAME OF TEST
3489                                          ;UPDATE PASS COUNT
3490                                          ;CHECK FOR EXIT TO ACT-11
3491                                          ;RESTART TEST
3492
3493  016426  104401                  EOP:    TYPE                            ;TYPE NAME OF TEST
3494  016430  020325                          MEPASS
3495  016432  005067  001312                  CLR     LAST                    ;CLEAR LAST ERROR PC
3496  016436  005067  001242                  CLR     ERRFLG                  ;CLEAR ERROR FLAG
3497  016442  005267  001240                  INC     PASCNT                  ;UPDATE PASS COUNT
3498  016446  016767  001234  161114          MOV     PASCNT,LIGHTS           ;DISPLAY PASS COUNT
3499  016454  013701  000042                  MOV     @#42,R1                 ;CHECK FOR ACT-11 OR ODP
3500  016460  001405                          BEQ     RESTRT                  ;IF NOT, CONTINUE TESTING
3501  016462  000005                          RESET
3502  016464  004711                  LOGICAL:        JSR     PC,(R1)
3503  016466  000240                          NOP
3504  016470  000240                          NOP
3505  016472  000240                          NOP
3506  016474  000167  162502          RESTRT: JMP     BEGIN
3507
3508                                          ;CHECK FOR LOOP ON CURRENT TEST
3509                                          ;CHECK FOR ITERATION SUPPRESSION
3510
3511  016500  032767  002000  161062  SCOPER: BIT     #SW10,SWR
3512  016506  001030                          BNE     4$
3513  016510  032767  040000  161052  1$:     BIT     #SW14,SWR
3514  016516  001021                          BNE     3$
3515  016520  032767  004000  161042          BIT     #SW11,SWR
3516  016526  001006                          BNE     2$
3517  016530  005267  001166                  INC     LPCNT
3518  016534  026767  001162  001156          CMP     LPCNT,ICOUNT
3519  016542  001007                          BNE     3$
3520  016544  005067  001152          2$:     CLR     LPCNT
3521  016550  005067  001130                  CLR     ERRFLG
3522  016554  011667  001132                  MOV     (SP),RETRN
3523  016560  000002                          RTI
3524  016562  016716  001124          3$:     MOV     RETRN,(SP)
3525  016566  000002                          RTI
3526  016570  005767  001110          4$:     TST     ERRFLG
3527  016574  001745                          BEQ     1$
3528  016576  000762                          BR      2$
3529
3530                                          ;CHECK FOR FREEZE ON CURRENT DATA
```

```
3531
3532  016600  032767  001000  160762  SCOP1R: BIT     #SW09,SWR
3533  016606  001402                  BEQ     1$
3534  016610  016716  001102          MOV     FREEZ1,(SP)
3535  016614  000002                  1$:     RTI
3536
3537                                  ;ERROR HANDLER
3538
3539  016616  032767  020000  160744  ERRORS: BIT     #SW13,SWR
3540  016624  001051                  BNE     HALTS
3541  016626  021667  001116          CMP     (SP),LAST
3542  016632  001404                  BEQ     1$
3543  016634  011667  001110          MOV     (SP),LAST
3544  016640  005067  001040          CLR     ERRFLG
3545  016644  104406                  1$:     SAV05P
3546  016646  011605                  MOV     (SP),R5
3547  016650  162705  000002          SUB     #2,R5
3548  016654  011504                  MOV     (R5),R4
3549  016656  006304                  ASL     R4
3550  016660  006304                  ASL     R4
3551  016662  042704  177001          BIC     #177001,R4
3552  016666  062704  020436          ADD     #ERRTAB,R4
3553  016672  012467  000034          MOV     (R4)+,ERRMSG
3554  016676  011467  000042          MOV     (R4),DATABP
3555  016702  005767  000776          TST     ERRFLG
3556  016706  001403                  BEQ     TYPMSG
3557  016710  005767  000030          TST     DATABP
3558  016714  001007                  BNE     TYPDAT
3559  016716  104402                  TYPMSG: OCTASC
3560  016720  017012                  ERTAB0
3561  016722  012767  000001  000754  MOV     #1,ERRFLG
3562  016730  104401                  TYPE
3563  016732  000000                  ERRMSG: 0
3564  016734  005767  000004          TYPDAT: TST     DATABP
3565  016740  001402                  BEQ     RESREG
3566  016742  104402                  OCTASC
3567  016744  000000                  DATABP: 0
3568  016746  104407                  RESREG: RES05
3569  016750  005767  160614          HALTS:  TST     SWR
3570  016754  100005                  BPL     EXITER
3571  016756  010046                  PUSHR0
3572  016760  016600  000002          MOV     2(SP),R0
3573  016764  000000                  HALT
3574  016766  012600                  POPR0
3575  016770  005267  000714          EXITER: INC     ERRCNT
3576  016774  032767  002000  160566  BIT     #SW10,SWR
3577  017002  001402                  BEQ     1$
3578  017004  016716  000704          MOV     ESCAPE,(SP)
3579  017010  000002                  1$:     RTI
3580  017012  000001                  ERTAB0: 1
3581  017014    006     002           .BYTE   6,2
3582  017016  017742                  .AVPC
3583                                  ;TRAP DISPATCH SERVICE
3584                                  ;ARGUMENT OF TRAP IS EXTRACTED
3585                                  ;AND USED AS OFFSET TO OBTAIN POINTER
3586                                  ;TO SELECTED SUBROUTINE
```

```
3587
3588  017020  011646                  TRPSRV: MOV     (SP),-(SP)          ;GET PC OF RETURN
3589  017022  162716  000002                  SUB     #2,(SP)             ;=PC OF TRAP
3590  017026  017616  000000                  MOV     @(SP),(SP)          ;GET TRP
3591  017032  006316                  TRPOK:  ASL     (SP)                ;MULTIPLY TRAP ARG BY 2
3592  017034  042716  177001                  BIC     #177001,(SP)        ;CLEAR UNWANTED BITS
3593  017040  062716  020356                  ADD     #TRPTAB,(SP)        ;POINTER TO SUBROUTINE ADDRESS
3594  017044  017616  000000                  MOV     @(SP),(SP)          ;SUBROUTINE ADDRESS
3595  017050  000136                          JMP     @(SP)+              ;GO TO SUBROUTINE
3596
3597                                          ;TELETYPE OUTPUT ROUTINE
3598
3599  017052  017605  000000          TYPER:  MOV     @(SP),R5
3600  017056  062716  000002                  ADD     #2,(SP)
3601  017062  105777  000560          1$:     TSTB    @TPCSR
3602  017066  100375                          BPL     1$
3603  017070  105715                          TSTB    (R5)
3604  017072  001001                          BNE     2$
3605  017074  000002                          RTI
3606  017076  112577  000546          2$:     MOVB    (R5)+,@TPDBR
3607  017102  000767                          BR      1$
3608
3609                                          ;ASCII STRING INPUT ROUTINE
3610
3611  017104  017667  000000  000006  INSTRG: MOV     @(SP),MSG
3612  017112  062716  000002                  ADD     #2,(SP)
3613  017116  104401                  INSTR1: TYPE
3614  017120  000000                  MSG:    0
3615  017122  012704  020400                  MOV     #INBUF,R4
3616  017126  012703  000007                  MOV     #7,R3
3617  017132  105777  000504          1$:     TSTB    @TKCSR
3618  017136  100375                          BPL     1$
3619  017140  117714  000500                  MOVB    @TKDBR,(R4)
3620  017144  142714  000200                  BICB    #200,(R4)
3621  017150  122427  000015                  CMPB    (R4)+,#15
3622  017154  001413                          BEQ     INSTR2
3623  017156  117777  000462  000464          MOVB    @TKDBR,@TPDBR
3624  017164  105777  000456          2$:     TSTB    @TPCSR
3625  017170  100375                          BPL     2$
3626  017172  005303                          DEC     R3
3627  017174  001356                          BNE     1$
3628  017176  104401                  INSTRE: TYPE
3629  017200  020231                          MQM
3630  017202  000745                          BR      INSTR1
3631  017204  000002                  INSTR2: RTI
3632
3633                                          ;CONVERT ASCII STRING TO OCTAL
3634
3635  017206  011605                  PARAMS: MOV     (SP),R5
3636  017210  012567  000146                  MOV     (R5)+,LOLIM
3637  017214  012567  000144                  MOV     (R5)+,HILIM
3638  017220  012567  000142                  MOV     (R5)+,DEVADR
3639  017224  112567  000140                  MOVB    (R5)+,LOBITS
3640  017230  112567  000135                  MOVB    (R5)+,ADRCNT
3641  017234  010516                          MOV     R5,(SP)
3642  017236  005005                  PARAM1: CLR     R5
```

```
3643  017240  012704  020400              MOV     #INBUF,R4
3644  017244  122714  000015              CMPB    #15,(R4)
3645  017250  001420                      BEQ     PARERR
3646  017252  121427  000060      1$:     CMPB    (R4),#60
3647  017256  002415                      BLT     PARERR
3648  017260  121427  000067              CMPB    (R4),#67
3649  017264  003012                      BGT     PARERR
3650  017266  142714  000060              BICB    #60,(R4)
3651  017272  152405                      BISB    (R4)+,R5
3652  017274  122714  000015              CMPB    #15,(R4)
3653  017300  001406                      BEQ     LIMITS
3654  017302  006305                      ASL     R5
3655  017304  006305                      ASL     R5
3656  017306  006305                      ASL     R5
3657  017310  000760                      BR      1$
3658  017312  104404              PARERR: INSTER
3659  017314  000750                      BR      PARAM1
3660
3661                                      ;TEST TO SEE IF NUMBER IS WITHIN LIMITS
3662
3663  017316  020567  000042      LIMITS: CMP     R5,HILIM
3664  017322  101373                      BHI     PARERR
3665  017324  020567  000032              CMP     R5,LOLIM
3666  017330  103770                      BLO     PARERR
3667  017332  136705  000032              BITB    LOBITS,R5
3668  017336  001365                      BNE     PARERR
3669
3670                                      ;STORE NUMBER AT SPECIFIED ADDRESS
3671
3672  017340  016704  000022              MOV     DEVADR,R4
3673  017344  010524              1$:     MOV     R5,(R4)+
3674  017346  062705  000002              ADD     #2,R5
3675  017352  105367  000013              DECB    ADRCNT
3676  017356  001372                      BNE     1$
3677  017360  000002                      RTI
3678  017362  000000              LOLIM:  0
3679  017364  000000              HILIM:  0
3680  017366  000000              DEVADR: 0
3681  017370  000000              LOBITS: 0
3682          017371              ADRCNT=LOBITS+1
3683
3684                                      ;CONVERT OCTAL NUMBER TO ASCII AND OUTPUT TO TELEPRINTER
3685
3686  017372  104401              OCTASN: TYPE
3687  017374  020235                      MCRLF
3688  017376  017601  000000              MOV     @(SP),R1
3689  017402  062716  000002              ADD     #2,(SP)
3690  017406  012167  000130              MOV     (R1)+,WRDCNT
3691  017412  112167  000126      1$:     MOVB    (R1)+,CHRCNT
3692  017416  112167  000123              MOVB    (R1)+,SPACNT
3693  017422  013167  000120              MOV     @(R1)+,BINWRD
3694  017426  016704  000114      2$:     MOV     BINWRD,R4
3695  017432  116705  000106              MOVB    CHRCNT,R5
3696  017436  012700  020412              MOV     #TEMP,R0
3697  017442  010403              3$:     MOV     R4,R3
3698  017444  042703  177770              BIC     #177770,R3
```

```
3699  017450  062703  000260                  ADD     #260,R3
3700  017454  110320                          MOVB    R3,(R0)+
3701  017456  006204                          ASR     R4
3702  017460  006204                          ASR     R4
3703  017462  006204                          ASR     R4
3704  017464  005305                          DEC     R5
3705  017466  001365                          BNE     3$
3706  017470  012703  020424                  MOV     #MDATA,R3
3707  017474  114023              4$:         MOVB    -(R0),(R3)+
3708  017476  105367  000042                  DECB    CHRCNT
3709  017502  001374                          BNE     4$
3710  017504  105767  000035                  TSTB    SPACNT
3711  017510  001405                          BEQ     6$
3712  017512  112723  000240          5$:     MOVB    #240,(R3)+
3713  017516  105367  000023                  DECB    SPACNT
3714  017522  001373                          BNE     5$
3715  017524  105013              6$:         CLRB    (R3)
3716  017526  104401                          TYPE
3717  017530  020424                          MDATA
3718  017532  005367  000004                  DEC     WRDCNT
3719  017536  001325                          BNE     1$
3720  017540  000002                          RTI
3721  017542  000000              WRDCNT: 0
3722  017544  000000              CHRCNT: 0
3723          017545              SPACNT=CHRCNT+1
3724  017546  000000              BINWRD: 0
3725
3726                                          ;SAVE PC OF TEST THAT FAILED AND R0-R5
3727
3728  017550  016667  000004  000164  SV05P:  MOV     4(SP),SAVPC
3729
3730                                          ;SAVE R0-R5
3731
3732  017556  010567  000154          SV05:   MOV     R5,SAVR5
3733  017562  010467  000146                  MOV     R4,SAVR4
3734  017566  010367  000140                  MOV     R3,SAVR3
3735  017572  010267  000132                  MOV     R2,SAVR2
3736  017576  010167  000124                  MOV     R1,SAVR1
3737  017602  010067  000116                  MOV     R0,SAVR0
3738  017606  000002                          RTI
3739                                          ;RESTORE R0-R5
3740
3741  017610  016700  000110          RS05:   MOV     SAVR0,R0
3742  017614  016701  000106                  MOV     SAVR1,R1
3743  017620  016702  000104                  MOV     SAVR2,R2
3744  017624  016703  000102                  MOV     SAVR3,R3
3745  017630  016704  000100                  MOV     SAVR4,R4
3746  017634  016705  000076                  MOV     SAVR5,R5
3747  017640  000002                          RTI
3748                                          ;INDIRECT POINTERS
3749
3750  017642  177560              TKCSR:  177560
3751  017644  177562              TKDBR:  177562
3752  017646  177564              TPCSR:  177564
3753  017650  177566              TPDBR:  177566
3754  017652  000000              DHSCR:  0
```

```
3755  017654  000000                  DHNRC:  0
3756  017656  000000                  DHLPR:  0
3757  017660  000000                  DHBA:   0
3758  017662  000000                  DHBC:   0
3759  017664  000000                  DHBAR:  0
3760  017666  000000                  DHBCR:  0
3761  017670  000000                  DHSSR:  0
3762  017672  000000                  DHSLR:  0
3763  017674  000000                  DHRVEC: 0
3764  017676  000000                  DHRLVL: 0
3765  017700  000000                  DHTVEC: 0
3766  017702  000000                  DHTLVL: 0
3767                                  ;PROGRAM VARIABLES
3768
3769  017704  000000                  ERRFLG: 0               ;ERROR FLAG
3770  017706  000000                  PASCNT: 0               ;PASS COUNT
3771  017710  000000                  ERRCNT: 0               ;ERROR COUNT
3772  017712  000000                  RETRN:  0               ;SCOPE RETURN ADDRESS FOR TEST LOOPING
3773  017714  000000                  ESCAPE: 0               ;ADDRESS FOR ERROR ESCAPE
3774  017716  000000                  FREEZ1: 0               ;DATA LOOPING RETURN ADDRESS
3775  017720  000000                  ILOUNT: 0               ;ITERATION COUNT FOR TEST IN PROGRESS
3776  017722  000000                  LPCNT:  0               ;NUMBER OF ITERATIONS THIS TEST
3777  017724  000000                  SAVR0:  0               ;R0 SAVE AREA
3778  017726  000000                  SAVR1:  0               ;R1 SAVE AREA
3779  017730  000000                  SAVR2:  0               ;R2 SAVE AREA
3780  017732  000000                  SAVR3:  0               ;R3 SAVE ARE
3781  017734  000000                  SAVR4:  0               ;R4 SAVE AREA
3782  017736  000000                  SAVR5:  0               ;R5 SAVE AREA
3783  017740  000000                  SAVSP:  0               ;STACK POINTER SAVE AREA
3784  017742  000000                  SAVPC:  0               ;CALLING ROUTINE SAVE AREA
3785  017744  000000                  INIFLG: 0               ;PROGRAM INITIALIZATION FLAG
3786  017746  000000                  STFLG:  0               ;PROGRAM START FLAG
3787  017750  000000                  LAST:   0               ;LAST ERROR PC
3788                                  ;ENTER HERE ON POWER FAILURE
3789
3790
3791  017752  010046          PFAIL:  MOV     R0,-(SP)        ;SAVE R0-R5 ON PROCESSOR STACK
3792  017754  010146                  MOV     R1,-(SP)
3793  017756  010246                  MOV     R2,-(SP)
3794  017760  010346                  MOV     R3,-(SP)
3795  017762  010446                  MOV     R4,-(SP)
3796  017764  010546                  MOV     R5,-(SP)
3797  017766  016746  160032          MOV     24,-(SP)
3798  017772  010667  177742          MOV     SP,SAVSP        ;SAVE STACK POINTER
3799  017776  012767  020010  160020  MOV     #RESTART,24     ;SET UP FOR POWER UP TRAP
3800  020004  000000                  HALT                    ;HALT ON POWER DOWN NORMAL
3801  020006  000777                  BR      .
3802
3803                                  ;PROCESSOR WILL TRAP HERE WHEN POWER IS RESTORED
3804
3805  020010  016706  177724  RESTAR: MOV     SAVSP,SP        ;RESTORE STACK POINTER
3806  020014  012605                  MOV     (SP)+,R5        ;RESTORE R0-R5
3807  020016  012604                  MOV     (SP)+,R4
3808  020020  012603                  MOV     (SP)+,R3
3809  020022  012602                  MOV     (SP)+,R2
3810  020024  012601                  MOV     (SP)+,R1
```

```
3811  020026  012600                          MOV     (SP)+,R0
3812  020030  012767  017752  157766          MOV     #PFAIL,24               ;SET UP FOR POWER FAILURE
3813  020036  012767  000340  157732          MOV     #340,PS
3814  020044  012706  021360                  MOV     #STACK,SP
3815  020050  005067  000336                  CLR     TEMP
3816  020054  005267  000332                  INC     TEMP
3817  020060  001375                          BNE     .-4
3818  020062  104402                          OCTASC
3819  020064  020106                          PFTAB
3820  020066  104401                          TYPE
3821  020070  020240                          MPFAIL
3822  020072  005067  177606                  CLR     ERRFLG
3823  020076  005067  177646                  CLR     LAST
3824  020102  000177  177604                  JMP     @RETRN
3825  020106  000001                  PFTAB:  1
3826  020110  000006  000002                  6,2
3827  020114  017712                          RETRN
3828  020116  005015  042012  030510  MTITLE: .ASCIZ  <15><12><12>/DH11 STATIC LOGIC TEST /<15><12>
3829  020124  020061  052123  052101
3830  020132  041511  046040  043517
3831  020140  041511  052040  051505
3832  020146  020124  005015     000
3833  020153     015  053012  041505  MVECTO: .ASCIZ  <15><12>/VECTOR ADDRESS-/
3834  020160  047524  020122  042101
3835  020166  051104  051505  026523
3836  020174     000
3837  020175     015  041412  047117  MREGAD: .ASCIZ  <15><12>/CONTROL REGISTER ADDRESS-/
3838  020202  051124  046117  051040
3839  020210  043505  051511  042524
3840  020216  020122  042101  051104
3841  020224  051505  026523     000
3842  020231     040  037440     000  MQM:    .ASCIZ  /  ?/
3843  020235     015  000012          MCRLF:  .ASCIZ   <15><12>
3844  020240  020040  047520  042527  MPFAIL: .ASCIZ  /  POWER FAILURE, PROGRAM RESTART AT TEST IN PROGRESS/
3845  020246  020122  040506  046111
3846  020254  051125  026105  050040
3847  020262  047522  051107  046501
3848  020270  051040  051505  040524
3849  020276  052122  040440  020124
3850  020304  042524  052123  044440
3851  020312  020116  051120  043517
3852  020320  042522  051523     000
3853  020325     015  041412  042132  MEPASS: .ASCIZ  <15><12>/CZDHA-C/
3854  020332  040510  041455     000
3855  020337     015  051012     000  MR:     .ASCIZ  <15><12>/R/
3856  020343     015  052012  051505  MTSTPC: .ASCIZ  <15><12>/TEST PC-/
3857  020350  020124  041520  000055
3858
3859                                          ;TABLE OF POINTERS FOR TRAP DECODING
3860
3861  020356  016500                  TRPTAB: SCOPER
3862  020360  017052                          TYPER
3863  020362  017372                          OCTASN
3864  020364  017104                          INSTRG
3865  020366  017176                          INSTRE
3866  020370  017206                          PARAMS
```

```
3867  020372  017550                          SV05P
3868  020374  017610                          RS05
3869  020376  016600                          SCOP1R
3870
3871                                          ;BUFFERS FOR INPUT-OUTPUT
3872
3873  020400  000000                  INBUF:  0
3874          020412                  .=.+10
3875  020412  000000                  TEMP:   0
3876          020424                  .=.+10
3877  020424  000000                  MDATA:  0
3878          020436                  . .+10
3879
3880                                          ;TABLE OF POINTERS TO ERROR MESSAGES AND DATA
3881
3882  020436                          ERRTAB:
3883  020436  020466                          EM0
3884  020440  021134                          DT0
3885  020442  020530                          EM1
3886  020444  021142                          DT1
3887  020446  020617                          EM2
3888  020450  021142                          DT1
3889  020452  020706                          EM3
3890  020454  021142                          DT1
3891  020456  020774                          EM4
3892  020460  021142                          DT1
3893  020462  021060                          EM5
3894  020464  021142                          DT1
3895  020466  042522  044507  052123  EM0:    .ASCII  /REGISTER DID NOT RESPOND/
3896  020474  051105  042040  042111
3897  020502  047040  052117  051040
3898  020510  051505  047520  042116
3899  020516  005015  042101  051104          .ASCIZ  <15><12>/ADDRESS/
3900  020524  051505  000123
3901  020530  054523  052123  046505  EM1:    .ASCII  /SYSTEM CONTROL REGISTER ERROR/
3902  020536  041440  047117  051124
3903  020544  046117  051040  043505
3904  020552  051511  042524  020122
3905  020560  051105  047522     122
3906  020565     015  042412  050130          .ASCIZ  <15><12>/EXP     REC     ADDRESS/
3907  020572  020040  020040  051040
3908  020600  041505  020040  020040
3909  020606  040440  042104  042522
3910  020614  051523     000
3911  020617     114  047111  020105  EM2:    .ASCII  /LINE PARAMETER REGISTER ERROR/
3912  020624  040520  040522  042515
3913  020632  042524  020122  042522
3914  020640  044507  052123  051105
3915  020646  042440  051122  051117
3916  020654  005015  054105  020120          .ASCIZ  <15><12>/EXP     REC     ADDRESS/
3917  020662  020040  020040  042522
3918  020670  020103  020040  020040
3919  020676  042101  051104  051505
3920  020704  000123
3921  020706  051102  040505  020113  EM3:    .ASCII  /BREAK CONTROL REGISTER ERROR/
3922  020714  047503  052116  047522
```

```
 3923  020722  020114  042522  044507
 3924  020730  052123  051105  042440
 3925  020736  051122  051117
 3926  020742  005015  054105  020120          .ASCIZ  <15><12>/EXP     REC     ADDRESS/
 3927  020750  020040  020040  042522
 3928  020756  020103  020040  020040
 3929  020764  042101  051104  051505
 3930  020772  000123
 3931  020774  044523  047514  051440  EM4:    .ASCII  /SILO STATUS REGISTER ERROR/
 3932  021002  040524  052524  020123
 3933  021010  042522  044507  052123
 3934  021016  051105  042440  051122
 3935  021024  051117
 3936  021026  005015  054105  020120          .ASCIZ  <15><12>/EXP     REC     ADDRESS/
 3937  021034  020040  020040  042522
 3938  021042  020103  020040  020040
 3939  021050  042101  051104  051505
 3940  021056  000123
 3941  021060  040515  052123  051105  EM5:    .ASCII  /MASTER CLEAR ERROR/
 3942  021066  041440  042514  051101
 3943  021074  042440  051122  051117
 3944  021102  005015  054105  020120          .ASCIZ  <15><12>/EXP     REC     ADDRESS/
 3945  021110  020040  020040  042522
 3946  021116  020103  020040  020040
 3947  021124  042101  051104  051505
 3948  021132  000123
 3949                                  .EVEN
 3950  021134  000001                  DTO:    1
 3951  021136     006      000        .BYTE   6,0
 3952  021140  017736                         SAVR5
 3953  021142  000003                  DT1:    3
 3954  021144     006      002        .BYTE   6,2
 3955  021146  017736                         SAVR5
 3956  021150     006      002        .BYTE   6,2
 3957  021152  017734                         SAVR4
 3958  021154     006      000        .BYTE   6,0
 3959  021156  017732                         SAVR3
 3960  021160  000000                  ENDCOD: 0
 3961          000000                  .END
```

```
ADRCNT= 017371          3640* 3675* 3682#
BEGIN   001202           399   428   434#  3506
BINWRD  017546          3693* 3694  3724#
BITC  = 000020          1301# 1326# 1351# 1376# 1401# 1426# 1451# 1476# 1501# 1526# 1551# 1576# 1601#
                        1626# 1651# 1676# 1701# 1726# 1751# 1776# 1801# 1826# 1851# 1876# 1901# 1926#
                        1951# 1976# 2001# 2026# 2051# 2076# 2103# 2130# 2157# 2184# 2211# 2238# 2265#
                        2295# 2325# 2355# 2385# 2415# 2445# 2475# 2505# 2535# 2565# 2595# 2625# 2655#
                        2685# 2715# 2745# 2775# 2805# 2835# 2865# 2895# 2925# 2955# 2985# 3015# 3045#
                        3075# 3105# 3135# 3165# 3195# 3227# 3259# 3291# 3323# 3355# 3387# 3419#
BITCLR- 000077          2265# 2295# 2325# 2355# 2385# 2415# 2445# 2475# 2505# 2535# 2565# 2595# 2625#
                        2655# 2685# 2715# 2745# 2775# 2805# 2835# 2865# 2895# 2925# 2955# 2985# 3015#
                        3045# 3075# 3105# 3135# 3165# 3195# 3227# 3259# 3291# 3323# 3355# 3387#
BITX    000000          1301# 1326# 1351# 1376# 1401# 1426# 1451# 1476# 1501# 1526# 1551# 1576# 1601#
                        1626# 1651# 1676# 1701# 1726# 1751# 1776# 1801# 1826# 1851# 1876# 1901# 1926#
                        1951# 1976# 2001# 2026# 2051# 2076# 2103# 2130# 2157# 2184# 2211# 2238# 2265#
                        2295# 2325# 2355# 2385# 2415# 2445# 2475# 2505# 2535# 2565# 2595# 2625# 2655#
                        2685# 2715# 2745# 2775# 2805# 2835# 2865# 2895# 2925# 2955# 2985# 3015# 3045#
                        3075# 3105# 3135# 3165# 3195# 3227# 3259# 3291# 3323# 3355# 3387# 3419#
BIT00 = 000001            85#   738   739   741   748
BIT01 = 000002            84#   768   769   771   778
BIT02 = 000004            83#   798   799   801   808
BIT03 = 000010            82#   828   829   831   838
BIT04 = 000020            81#   858   859   861   868
BIT05 = 000040            80#   888   889   891   898
BIT06 - 000100            79#   918   919   921   928  3444  3446  3448
BIT07 - 000200            78#  1064  1172  1173  1176  1184  1185  1187  1193
BIT08 - 000400            77#  1084
BIT09 = 001000            76#   948   949   951   958  1171  1173  1176  1183  1192  1194  1197  1219
                        1221  1224  1231  1240  1242  1245  1267  1269  1272  1279  1288  1290  1293
BIT10 = 002000            75#  1104  1220  1221  1224  1232  1233  1235  1241
BIT11 - 004000            74#   649   671   693   715  1124  1311  1336  1361  1386  1411  1436  1461
                        1486  1511  1536  1561  1586  1611  1636  1661  1686  1711  1736  1761  1786
                        1811  1836  1861  1886  1911  1936  1961  1986  2011  2036  2061  2086  2113
                        2140  2167  2194  2221  2248  2276  2306  2336  2366  2396  2426  2456  2486
                        2516  2546  2576  2606  2636  2666  2696  2726  2756  2786  2816  2846  2876
                        2906  2936  2966  2996  3026  3056  3086  3116  3146  3176  3206  3238  3270
                        3302  3334  3366  3398  3433  3466
BIT12   010000            73#   978   979   981   988  3438  3440  3446  3448
BIT13 = 020000            72#  1008  1009  1011  1018  3438  3440  3446  3448
BIT14   040000            71#  1144  1268  1269  1272  1280  1281  1283  1289
BIT15   100000            70#  1038  1039  1041  1048
CBIT    000020          1301# 1676# 2076# 2265# 2715# 3195#
CCRBIT  077777          2265# 2295# 2325# 2355# 2385# 2415# 2445# 2475# 2505# 2535# 2565# 2595# 2625#
                        2655# 2685# 3195# 3227# 3259# 3291# 3323# 3355# 3387#
CHRCNT  017544          3691* 3695  3708* 3722# 3723
CLRBIT  000077          2265# 2295# 2325# 2355# 2385# 2415# 2445# 2475# 2505# 2535# 2565# 2595# 2625#
                        2655# 2685# 2715# 2745# 2775# 2805# 2835# 2865# 2895# 2925# 2955# 2985# 3015#
                        3045# 3075# 3105# 3135# 3165# 3195#  3208  3227#  3240  3259#  3272  3291#  3304
                        3323# 3336  3355# 3368  3387# 3400
DATABP  016744          3554* 3557  3564  3567#
DEVADR  017366          3638* 3672  3680#
DHBA    017660           533   537  3757#
DHBAR   017664           602   606  3759#
DHBC    017662           556   560  3758#
DHBCR   017666           579   583   691*  694   701  1687  1712  1737  1762  1787  1812  1837  1862
                        1887  1912  1937  1962  1987  2012  2037  2062  2727  2757  2787  2817  2847
```

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                    2877    2907    2937    2967    2997    3027    3057    3087    3117    3147    3177    3760#
DHLPR   017656       510     514     669*    672     679    1312    1337    1362    1387    1412    1437    1462    1487
                    1512    1537    1562    1587    1612    1637    1662    2277    2307    2337    2367    2397    2427
                    2457    2487    2517    2547    2577    2607    2637    2667    2697    3756#
DHNRC   017654       487     491    3755#
DHRLVL  017676      3764#
DHRVEC  017674       414    3763#
DHSCR   017652       422     464     468     647*    649*    650     657     671*    693*    715*    737     767     797
                     827     857     887     917     947     977    1007    1037    1064*   1067    1071    1073    1084*
                    1087    1091    1093    1104*   1107    1111    1113    1124*   1127    1131    1133    1144*   1147
                    1151    1153    1170    1218    1266    1311*   1336*   1361*   1386*   1411*   1436*   1461*   1486*
                    1511*   1536*   1561*   1586*   1611*   1636*   1661*   1686*   1711*   1736*   1761*   1786*   1811*
                    1836*   1861*   1886*   1911*   1936*   1961*   1986*   2011*   2036*   2061*   2086*   2113*   2140*
                    2167*   2194*   2221*   2248*   2276*   2306*   2336*   2366*   2396*   2426*   2456*   2486*   2516*
                    2546*   2576*   2606*   2636*   2666*   2696*   2726*   2756*   2786*   2816*   2846*   2876*   2906*
                    2936*   2966*   2996*   3026*   3056*   3086*   3116*   3146*   3176*   3206*   3238*   3270*   3302*
                    3334*   3366*   3398*   3433*   3434    3438    3441    3444*   3446    3449    3466*   3467    3469*
                    3471    3474    3479    3482    3754#
DHSLR   017672       425*    426*   3762#
DHSSR   017670       425     625     629     713*    716     724    2087    2114    2141    2168    2195    2222    2249
                    3207    3239    3271    3303    3335    3367    3399    3761#
DHTLVL  017702      3766#
DHTVEC  017700      3765#
DTO     021134      3884    3950#
DT1     021142      3886    3888    3890    3892    3894    3953#
EM0     020466      3883    3895#
EM1     020530      3885    3901#
EM2     020617      3887    3911#
EM3     020706      3889    3921#
EM4     020774      3891    3931#
EM5     021060      3893    3941#
ENDCOD  021160        57    3960#
EOP     016426      3493#
ERRCNT  017710       390*    3575*   3771#
ERRFLG  017704       391*    392*    3496*   3521*   3526    3544*   3555    3561*   3769#   3822*
ERRMSG  016732      3553*   3563#
ERRORS  016616       350    3539#
ERRTAB  020436      3552    3882#
ERTABO  017012      3560    3580#
ESCAPE  017714       461*    484*    507*    530*    553*    576*    599*    622*    646*    668*    690*    712*    736*
                     766*    796*    826*    856*    886*    916*    946*    976*   1006*   1036*   1063*   1083*   1103*
                    1123*   1143*   1169*   1217*   1265*   1310*   1335*   1360*   1385*   1410*   1435*   1460*   1485*
                    1510*   1535*   1560*   1585*   1610*   1635*   1660*   1685*   1710*   1735*   1760*   1785*   1810*
                    1835*   1860*   1885*   1910*   1935*   1960*   1985*   2010*   2035*   2060*   2085*   2112*   2139*
                    2166*   2193*   2220*   2247*   2275*   2305*   2335*   2365*   2395*   2425*   2455*   2485*   2515*
                    2545*   2575*   2605*   2635*   2665*   2695*   2725*   2755*   2785*   2815*   2845*   2875*   2905*
                    2935*   2965*   2995*   3025*   3055*   3085*   3115*   3145*   3175*   3205*   3237*   3269*   3301*
                    3333*   3365*   3397*   3431*   3464*   3578    3773#
EXITER  016770      3570    3575#
FREEZ1  017716      3534    3774#
HALTS   016750      3540    3569#
HILIM   017364      3637*   3663    3679#
ICOUNT  017720       460*    483*    506*    529*    552*    575*    598*    621*    645*    667*    689*    711*    735*
                     765*    795*    825*    855*    885*    915*    945*    975*   1005*   1035*   1062*   1082*   1102*
                    1122*   1142*   1168*   1216*   1264*   1309*   1334*   1359*   1384*   1409*   1434*   1459*   1484*
                    1509*   1534*   1559*   1584*   1609*   1634*   1659*   1684*   1709*   1734*   1759*   1784*   1809*
```

CROSS REFERENCE TABLE -- USER SYMBOLS

SEQ 0087

```
                    1834*  1859*  1884*  1909*  1934*  1959*  1984*  2009*  2034*  2059*  2084*  2111*  2138*
                    2165*  2192*  2219*  2246*  2274*  2304*  2334*  2364*  2394*  2424*  2454*  2484*  2514*
                    2544*  2574*  2604*  2634*  2664*  2694*  2724*  2754*  2784*  2814*  2844*  2874*  2904*
                    2934*  2964*  2994*  3024*  3054*  3084*  3114*  3144*  3174*  3204*  3236*  3268*  3300*
                    3332*  3364*  3396*  3432*  3465*  3518   3775#
INBUF   020400      3615   3643   3873#
INIFLG  017744       394    427    429*  3785#
INSTER= 104404       367#  3658
INSTR = 104403       366#   409    417    438
INSTRE  017176      3628#  3865
INSTRG  017104      3611#  3864
INSTR1  017116      3613#  3630
INSTR2  017204      3622   3631#
LAST    017750      3495*  3541   3543*  3787#  3823*
LIGHTS= 177570        55#  3498*
LIMITS  017316      3653   3663#
LOBITS  017370      3639*  3667   3681#  3682
LOGICA  016464       373   3502#
LOLIM   017362      3636*  3665   3678#
LPCNT   017722      3517*  3518   3520*  3776#
MCRLF   020235      3687   3843#
MDATA   020424      3706   3717   3877#
MEPASS  020325      3494   3853#
MPFAIL  020240      3821   3844#
MQM     020231      3629   3842#
MR      020337       451   3855#
MREGAD  020175       418   3837#
MSG     017120      3611*  3614#
MTITLE  020116       393   3828#
MTSTPC  020343       439   3856#
MVECTO  020153       410   3833#
N       000001         1#
OCTASC= 104402       365#  3559   3566   3818
OCTASN  017372      3686#  3863
PARAM - 104405       368#   411    419    440
PARAMS  017206      3635#  3866
PARAM1  017236      3642#  3659
PARERR  017312      3645   3647   3649   3658#  3664   3666   3668
PASCNT  017706       389*  3497*  3498   3770#
PFAIL   017752       348    387   3791#  3812
PFTAB   020106      3819   3825#
POPR0   012600        64#  3574
POP1SP- 005726        62#
POP2SP= 022626        66#
PS      177776        56#   385*   434*   459*   482*   505*   528*   551*   574*   597*   620*   644*   666*
                     688*   710*   734*   764*   794*   824*   854*   884*   914*   944*   974*  1004*  1034*
                    1061*  1081*  1101*  1121*  1141*  1167*  1215*  1263*  1308*  1333*  1358*  1383*  1408*
                    1433*  1458*  1483*  1508*  1533*  1558*  1583*  1608*  1633*  1658*  1683*  1708*  1733*
                    1758*  1783*  1808*  1833*  1858*  1883*  1908*  1933*  1958*  1983*  2008*  2033*  2058*
                    2083*  2110*  2137*  2164*  2191*  2218*  2245*  2273*  2303*  2333*  2363*  2393*  2423*
                    2453*  2483*  2513*  2543*  2573*  2603*  2633*  2663*  2693*  2723*  2753*  2783*  2813*
                    2843*  2873*  2903*  2933*  2963*  2993*  3023*  3053*  3083*  3113*  3143*  3173*  3203*
                    3235*  3267*  3299*  3331*  3363*  3395*  3430*  3463*  3813*
PUSHR0- 010046        63#  3571
PUSH1S- 005746        61#
PUSH2S  024646        65#
```

CROSS REFERENCE TABLE -- USER SYMBOLS


```
RESREG  016746            3565    3568#
RESTAR  020010            3799    3805#
RESTRT  016474            3500    3506#
RES05 = 104407             370#   3568
RETRN   017712             443     447*    452    3522*   3524    3772#   3824    3827
RS05    017610            3741#   3868
SAVPC   017742            3582    3728*   3784#
SAVR0   017724            3737*   3741    3777#
SAVR1   017726            3736*   3742    3778#
SAVR2   017730            3735*   3743    3779#
SAVR3   017732            3734*   3744    3780#   3959
SAVR4   017734            3733*   3745    3781#   3957
SAVR5   017736            3732*   3746    3782#   3952    3955
SAVSP   017740            3783#   3798*   3805
SAV05P= 104406             369#   3545
SCOPE - 104400             363#    475     498     521     544     567     590     613     636     659     681     703     726
                           756     786     816     846     876     906     936     966     996    1026    1056    1076    1096
                          1116    1136    1156    1204    1252    1300    1325    1350    1375    1400    1425    1450    1475
                          1500    1525    1550    1575    1600    1625    1650    1675    1700    1725    1750    1775    1800
                          1825    1850    1875    1900    1925    1950    1975    2000    2025    2050    2075    2102    2129
                          2156    2183    2210    2237    2264    2294    2324    2354    2384    2414    2444    2474    2504
                          2534    2564    2594    2624    2654    2684    2714    2744    2774    2804    2834    2864    2894
                          2924    2954    2984    3014    3044    3074    3104    3134    3164    3194    3226    3258    3290
                          3322    3354    3386    3418    3451    3484
SCOPER  016500            3511#   3861
SCOPE1= 104410             371#
SCOP1R  016600            3532#   3869
SPACNT= 017545            3692*   3710    3713*   3723#
STACK = 021360              57#    386     435    3429    3462    3814
START   001000             355     385#
STFLG   017746             388*    448     450*   3786#
SV05    017556            3732#
SV05P   017550            3728#   3867
SWR   = 177570              54#    398     436    3511    3513    3515    3532    3539    3569    3576
SW00  = 000001              37#    398
SW01  = 000002              36#    436
SW02  = 000004              35#
SW03  = 000010              34#
SW04  = 000020              33#
SW05  = 000040              32#
SW06  = 000100              31#
SW08  - 000400              30#
SW09  = 001000              29#   3532
SW10  = 002000              28#   3511    3576
SW11  = 004000              27#   3515
SW12  = 010000              26#
SW13  = 020000              25#   3539
SW14  = 040000              24#   3513
SW15  = 100000              23#
TEMP    020412            3696    3815*   3816*   3875#
TKCSR   017642            3617    3750#
TKDBR   017644            3619    3623    3751#
TPCSR   017646            3601    3624    3752#
TPDBR   017650            3606*   3623*   3753#
TRPOK   017032            3591#
TRPSRV  017020             352    3588#
```

```
TRPTAB  020356            3593    3861#
TYPDAT  016734            3558    3564#
TYPE  = 104401             364#    393      451     3493    3562    3613    3628    3686    3716    3820
TYPER   017052            3599#   3862
TYPMSG  016716            3556    3559#
T1      001274             447     459#
T10     002140             620#
T100    010236            2110#
T101    010336            2137#
T102    010436            2164#
T103    010536            2191#
T104    010636            2218#
T105    010736            2245#
T106    011036            2273#
T107    011142            2303#
T11     002234             644#
T110    011246            2333#
T111    011352            2363#
T112    011456            2393#
T113    011562            2423#
T114    011666            2453#
T115    011772            2483#
T116    012076            2513#
T117    012202            2543#
T12     002314             666#
T120    012306            2573#
T121    012412            2603#
T122    012516            2633#
T123    012622            2663#
T124    012726            2693#
T125    013032            2723#
T126    013136            2753#
T127    013242            2783#
T13     002374             688#
T130    013346            2813#
T131    013452            2843#
T132    013556            2873#
T133    013662            2903#
T134    013766            2933#
T135    014072            2963#
T136    014176            2993#
T137    014302            3023#
T14     002454             710#
T140    014406            3053#
T141    014512            3083#
T142    014616            3113#
T143    014722            3143#
T144    015026            3173#
T145    015132            3203#
T146    015246            3235#
T147    015362            3267#
T15     002540             734#
T150    015476            3299#
T151    015612            3331#
T152    015726            3363#
T153    016042            3395#
```

```
T154    016156          3429#
T155    016302          3462#
T16     002626           764#
T17     002714           794#
T2      001370           482#
T20     003002           824#
T21     003070           854#
T22     003156           884#
T23     003244           914#
T24     003332           944#
T25     003420           974#
T26     003506          1004#
T27     003574          1034#
T3      001464           505#
T30     003662          1061#
T31     003736          1081#
T32     004012          1101#
T33     004066          1121#
T34     004142          1141#
T35     004216          1167#
T36     004346          1215#
T37     004476          1263#
T4      001560           528#
T40     004626          1308#
T41     004716          1333#
T42     005006          1358#
T43     005076          1383#
T44     005166          1408#
T45     005256          1433#
T46     005346          1458#
T47     005436          1483#
T5      001654           551#
T50     005526          1508#
T51     005616          1533#
T52     005706          1558#
T53     005776          1583#
T54     006066          1608#
T55     006156          1633#
T56     006246          1658#
T57     006336          1683#
T6      001750           574#
T60     006426          1708#
T61     006516          1733#
T62     006606          1758#
T63     006676          1783#
T64     006766          1808#
T65     007056          1833#
T66     007146          1858#
T67     007236          1883#
T7      002044           597#
T70     007326          1908#
T71     007416          1933#
T72     007506          1958#
T73     007576          1983#
T74     007666          2008#
T75     007756          2033#
```

CROSS REFERENCE TABLE -- USER SYMBOLS

SEQ 0091

```
T76      010046          2058#
T77      010136          2083#
VEC1     001060           395     398#
VEC2     001070           397     400#
WRDCNT   017542          3690*    3718*   3721#
X      = 000000             1#
XBIT   = 000000          1301#    1676#   2076#   2265#   2715#   3195#
XN     = 000154             1#     459     462#    482     485#    505     508#    528     531#    551     554#    574     577#
                           597     600#    620     623#    644     647#    666     669#    688     691#    710     713#    734
                           737#    764     767#    794     797#    824     827#    854     857#    884     887#    914     917#
                           944     947#    974     977#   1004    1007#   1034    1037#   1061    1064#   1081    1084#   1101
                          1104#   1121    1124#   1141    1144#   1167    1170#   1215    1218#   1263    1266#   1308    1311#
                          1333    1336#   1358    1361#   1383    1386#   1408    1411#   1433    1436#   1458    1461#   1483
                          1486#   1508    1511#   1533    1536#   1558    1561#   1583    1586#   1608    1611#   1633    1636#
                          1658    1661#   1683    1686#   1708    1711#   1733    1736#   1758    1761#   1783    1786#   1808
                          1811#   1833    1836#   1858    1861#   1883    1886#   1908    1911#   1933    1936#   1958    1961#
                          1983    1986#   2008    2011#   2033    2036#   2058    2061#   2083    2086#   2110    2113#   2137
                          2140#   2164    2167#   2191    2194#   2218    2221#   2245    2248#   2273    2276#   2303    2306#
                          2333    2336#   2363    2366#   2393    2396#   2423    2426#   2453    2456#   2483    2486#   2513
                          2516#   2543    2546#   2573    2576#   2603    2606#   2633    2636#   2663    2666#   2693    2696#
                          2723    2726#   2753    2756#   2783    2786#   2813    2816#   2843    2846#   2873    2876#   2903
                          2906#   2933    2936#   2963    2966#   2993    2996#   3023    3026#   3053    3056#   3083    3086#
                          3113    3116#   3143    3146#   3173    3176#   3203    3206#   3235    3238#   3267    3270#   3299
                          3302#   3331    3334#   3363    3366#   3395    3398#
Y      = 000011             '#      363     364#    365#    366#    367#    368#    369#    370#    371#    372#
.      = 021162            87#      88      90      92      94      96      98     100     102     104     106     108     110
                           112     114     116     118     120     122     124     126     128     130     132     134     136
                           138     140     142     144     146     148     150     152     154     156     158     160     162
                           164     166     168     170     172     174     176     178     180     182     184     186     188
                           190     192     194     196     198     200     202     204     206     208     210     212     214
                           216     218     220     222     224     226     228     230     232     234     236     238     240
                           242     244     246     248     250     252     254     256     258     260     262     264     266
                           268     270     272     274     276     278     280     282     284     286     288     290     292
                           294     296     298     300     302     304     306     308     310     312     314     316     318
                           320     322     324     326     328     330     332     334     336     338     340     342     347#
                           354#    372#    374#    376#   3801    3817    3874#   3876#   3878#
```

CROSS REFERENCE TABLE -- MACRO NAMES

SEQ 0092

```
COUEM1   376#  425
HLT       67#  469   492   515   538   561   584   607   630   658   680   702   725   746   754
           776  784   806   814   836   844   866   874   896   904   926   934   956   964   986
           994 1016  1024  1046  1054  1074  1094  1114  1134  1154  1181  1190  1202  1229  1238
          1250 1277  1286  1298  1318  1324  1343  1349  1368  1374  1393  1399  1418  1424  1443
          1449 1468  1474  1493  1499  1518  1524  1543  1549  1568  1574  1593  1599  1618  1624
          1643 1649  1668  1674  1693  1699  1718  1724  1743  1749  1768  1774  1793  1799  1818
          1824 1843  1849  1868  1874  1893  1899  1918  1924  1943  1949  1968  1974  1993  1999
          2018 2024  2043  2049  2068  2074  2094  2101  2121  2128  2148  2155  2175  2182  2202
          2209 2229  2236  2256  2263  2286  2293  2316  2323  2346  2353  2376  2383  2406  2413
          2436 2443  2466  2473  2496  2503  2526  2533  2556  2563  2586  2593  2616  2623  2646
          2653 2676  2683  2706  2713  2736  2743  2766  2773  2796  2803  2826  2833  2856  2863
          2886 2893  2916  2923  2946  2953  2976  2983  3006  3013  3036  3043  3066  3073  3096
          3103 3126  3133  3156  3163  3186  3193  3217  3225  3249  3257  3281  3289  3313  3321
          3345 3353  3377  3385  3409  3417  3442  3450  3475  3483
REGTS1   453#  727   757   787   817   847   877   907   937   967   997  1027
REGTS2   453#  1057  1077  1097  1117  1137
REGTS3   453#  1157  1205  1253
REGTS5   453#  638   660   682   704
REGTS6   453#  1301  1326  1351  1376  1401  1426  1451  1476  1501  1526  1551  1576  1601  1626
          1651 1676  1701  1726  1751  1776  1801  1826  1851  1876  1901  1926  1951  1976  2001
          2026 2051  2076  2103  2130  2157  2184  2211  2238
REGTS7   453#  2265  2295  2325  2355  2385  2415  2445  2475  2505  2535  2565  2595  2625  2655
          2685 2715  2745  2775  2805  2835  2865  2895  2925  2955  2985  3015  3045  3075  3105
          3135 3165  3195  3227  3259  3291  3323  3355  3387
RGADRS   453#  476   499   522   545   568   591   614
TRPDEF     1#  363   364   365   366   367   368   369   370   371
TS         1#  459   482   505   528   551   574   597   620   644   666   688   710   734   764
           794  824   854   884   914   944   974  1004  1034  1061  1081  1101  1121  1141  1167
          1215 1263  1308  1333  1358  1383  1408  1433  1458  1483  1508  1533  1558  1583  1608
          1633 1658  1683  1708  1733  1758  1783  1808  1833  1858  1883  1908  1933  1958  1983
          2008 2033  2058  2083  2110  2137  2164  2191  2218  2245  2273  2303  2333  2363  2393
          2423 2453  2483  2513  2543  2573  2603  2633  2663  2693  2723  2755  2783  2813  2843
          2873 2903  2933  2963  2993  3023  3053  3083  3113  3143  3173  3203  3235  3267  3299
          3331 3363  3395
.BUFFE     1#  3870
.CATCH     1#  86
.ENDCO     1#  3960
.EOP       1#  3486
.ERROR     1#  3536
.ERRTA     1#  3879
.HEADE     1#
.INSTR     1#  3608
.MSG       1#  3828
.OCTAS     1#  3683
.PARAM     1#  3632
.PFAIL     1#  3788
.POINT     1#  3748
.RESRE     1#  3739
.SAVRE     1#  3725
.SCOPE     1#  3507
.SCOP1     1#  3529
.SETVE     1#  344
.START     1#  376
.SYMBO     1#  20
.TRPDE     1#  358
```

```
.TRPSR      1#   3583
.TRPTA      1#   3858
.TYPER      1#   3596
.VARIA      1#   3767


. ABS.  021162     000


 ERRORS DETECTED:  0

 CZDHAC.BIN,CZDHAC.LST/CRF/SOL/NL:TOC=CZDHAC.SML,CZDHAC.P11
 RUN-TIME: 8 13 1 SECONDS
 RUN-TIME RATIO: 101/24=4.2
 CORE USED:  11K  (21 PAGES)
```