PDP11

1080 MEMORY TIMING TEST

MD-11-DBKMA-A

EP-DBKMA-A-DL-A

FICHE 1 OF 1

NOV 1976

digital

MADE IN U.S.A

```
                        .REM    %
```

IDENTIFICATION

PRODUCT CODE:	MAINDEC-1080-BNTT
PRODUCT NAME:	DECSYSTEM-1080 BASIC MEMORY TIMING TEST
DATE RELEASED:	JUNE 20, 1975
MAINTAINED BY:	DIAGNOSTIC ENGINEERING
AUTHOR:	JAMES KELLY

TABLE OF CONTENTS

1.0 ABSTRACT

THE BASIC MEMORY TIMING TEST (BNTT) IS DESIGNED TO VERIFY THAT THE BASIC MEMORY CYCLE TIME OF CORE MEMORY IS WITHIN TOLERANCE. THIS IS ACCOMPLISHED BY COMPARING THE SPEED OF THE KW11-L REAL TIME CLOCK VERSUS THE TIME REQUIRED FOR A SMALL SET OF INSTRUCTIONS TO BE EXECUTED. NO ATTEMPT IS MADE TO COMPUTE ACTUAL MACHINE TIMING. A SHORT VERIFICATION OF THE KW11-L IS DONE PRIOR TO THE TIMING TEST.

2.0 REQUIREMENTS

2.1 EQUIPMENT

A PDP-11/40 EQUIPPED WITH AT LEAST 4KW OF MEMORY.

A DECTAPE DRIVE FOR LOADING THE PROGRAM.

A CONSOLE TELETYPE TO COMMAND THE MONITOR.

A KW11-L REAL TIME CLOCK.

2.2 STORAGE

THIS PROGRAM OCCUPIES MEMORY LOCATIONS 1000(8) THRU 1522(8). IN ADDITION THE STACK POINTER IS SET TO 3200. AND THE APPROPRIATE INTERRUPT VECTORS WILL BE SET UP BY THE SOFTWARE PRIOR TO USE.

2.3 PRELIMINARY PROGRAMS

ALL BASIC CPU INSTRUCTION SET DIAGNOSTIC'S MUST HAVE BEEN SUCCESSFULLY RUN PRIOR TO ATTEMPTING TO RUN THIS PROGRAM.

3.0 PROGRAM PROCEDURES

3.1 LOADING PROCEDURES

1. MOUNT THE DECTAPE CONTAINING THE BNTT DIAGNOSTIC TEST ONTO A WORKING DECTAPE DRIVE.
2. SET THE WRITE LOCK SWITCH TO WRITE LOCK.
3. SET THE DRIVES SELECT TO UNIT #0.
4. SET THE MODE SWITCH TO ONLINE.
5. SET 177072 INTO THE PDP-11/40 SWITCH REGISTER.
6. DEPRESS THE HALT SWITCH ON THE PDP-11/40.
7. DEPRESS THE START KEY ON THE PDP-11/40 SEVERAL TIMES. THIS INITIALIZES THE CPU.
8. SET THE HALT KEY TO THE RUN POSITION (UP).
9. DEPRESS THE START KEY AND RELEASE ONE TIME.
10. THE SELECTED DECTAPE DRIVE WILL BEGIN TO TURN.
11. THE CONSOLE WILL TYPE THE MONITOR'S NAME FOLLOWED BY A "*".
12. TYPE DBKMAA.BIN <CR>.

3.2 STARTING PROCEDURES

TO START THE BNTT PROGRAM PROCEDE AS FOLLOWS:

1. SET THE PDP-11/40 ADDRESS TO 1000.
2. DEPRESS AND RELEASE THE START KEY.
3. THE PROCESSOR WILL RUN FOR LESS THAN A SECOND AND HALT WITH ADDRESS 1514 DISPLAYED IN THE ADDRESS REGISTER.
4. IF THE PROCESSOR HALTS AT ANY ADDRESS OTHER THAN THE ABOVE, IT IS AN ERROR. REFER TO THE LISTING FOR A DETAILED DESCRIPTION OF THE SYMTOM.

4.0 ERRORS

ANY HALT OTHER THAN WITH 1514 DISPLAYED IS AN ERROR AND WILL HAVE TO BE REPAIRED BEFORE ATTEMPTING ANY FURTHER TESTING. TO TROUBLE SHOOT AN ERROR USING BMTT THE ERROR HALT SHOULD BE REPLACED WITH A "NOP" 240. THE PROGRAM CAN THEN BE RESTARTED AT THE BEGINNING OF THE FAILING SUBTEST.

4.1 ERROR PC RANGE

ADDRESS(ES) 1000 THRU 1516 INCLUSIVE ARE LEGAL ERROR HALTS WITH THE SINGLE EXCEPTION OF ADDRESS 1512 DISPLAYED AS 1514.

5.0 CYCLE TIME

THE SPEED OF EXECUTION IS PRACTICALLY INSTANTLY.

6.0 PROGRAM DESCRIPTION

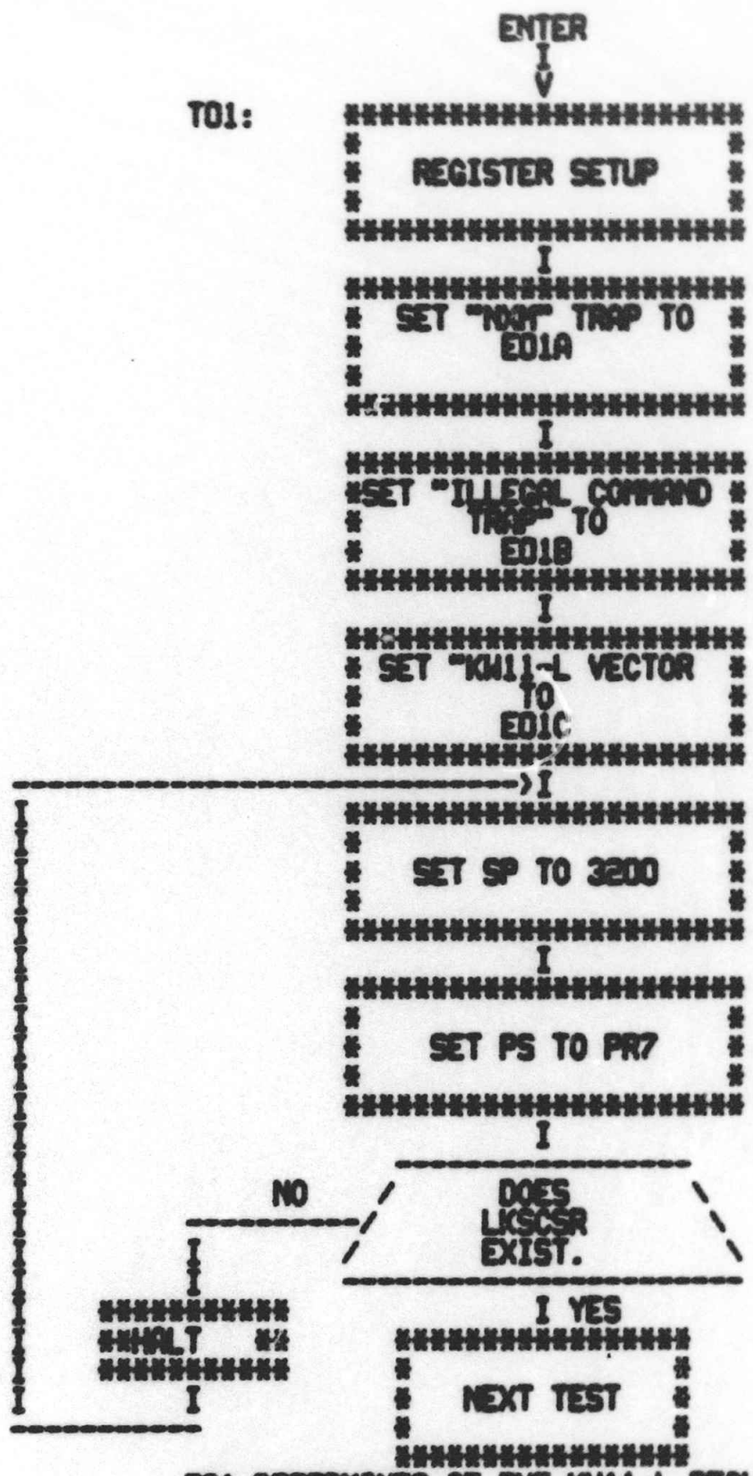
BMTT CONSISTS OF FIVE BASIC TESTS. THE FIRST FOUR ARE A CURSORY CHECK OF THE KW11-L REAL TIME CLOCK, THE FIFTH BEING THE ACTUAL TIMING TEST. THE FIRST FOUR TESTS DETERMINE THAT THE CLOCK EXISTS, THAT IT WILL SET ITS MONITOR BIT, CAUSE INTERRUPTS AND THAT IT CAN BE LOCKED OUT BY CLEARING THE INTERRUPT ENABLE BIT. THE FINAL TEST WAITS FOR THE CLOCK TO SET ITS MONITOR BIT THUS GIVING US A COMPLETE CYCLE FOR OUR TEST, THEN STARTING A SIMPLE TIME OUT LOOP. WHEN THE KW11-L CAUSES AN INTERRUPT THE NUMBER OF ITERATIONS IN THE TIMEOUT LOOP ARE COMPARED TO A PREVIOUSLY CALCULATED NOMINAL RANGE TO DETERMINE THAT THE MACHINE SPEED IS NOMINAL.

FLOW CHART
##########

BASIC MEMORY TIMING TESTS FLOWS

##########

BASIC MEMORY TIMING TESTS FLOWS DECFLO VER 00.0



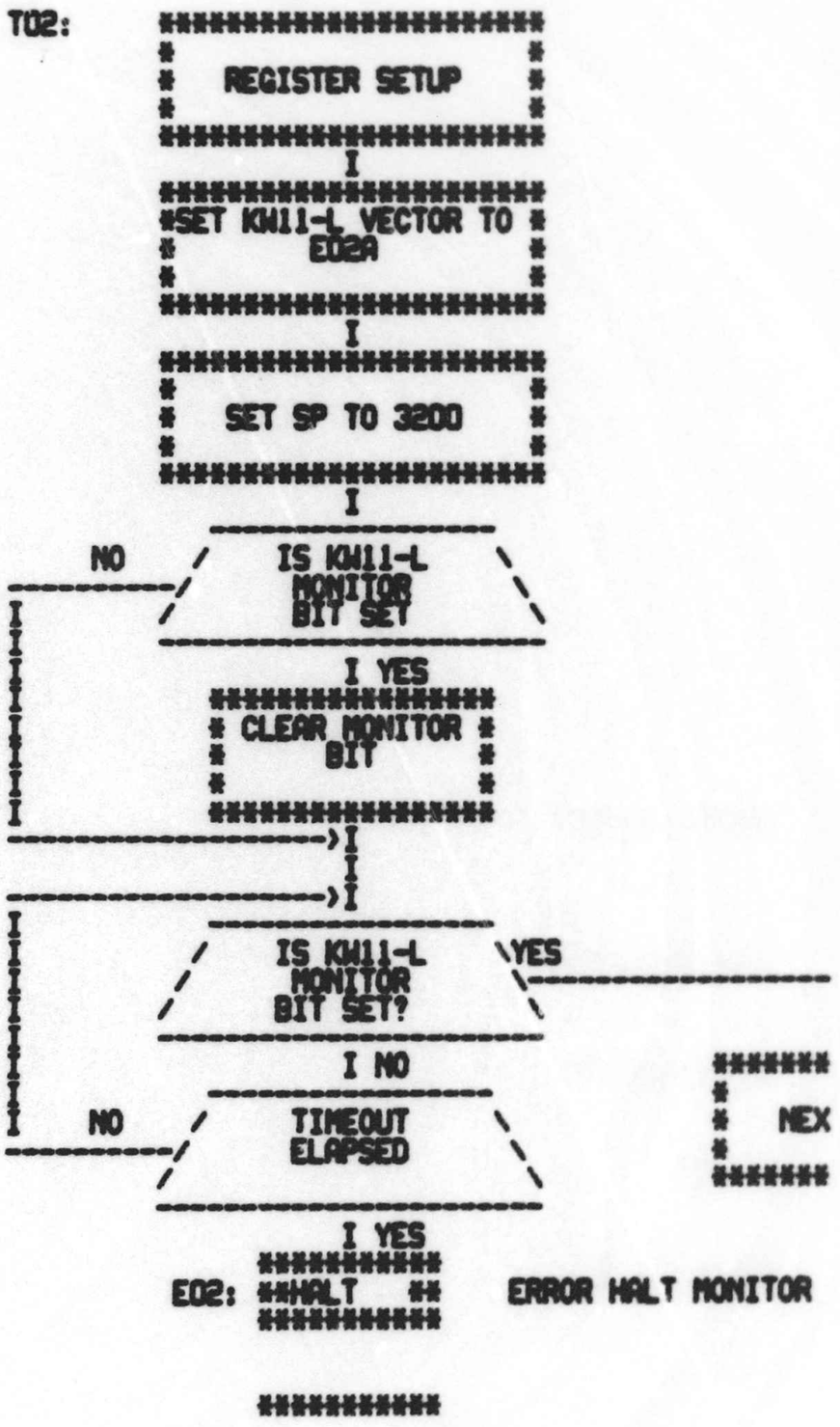
TO1 DETERMINES IF THE KW11-L REAL TIME CSR REGIST
CAUSING A TIME OUT.

NOTE

```
321
322
323
324
```

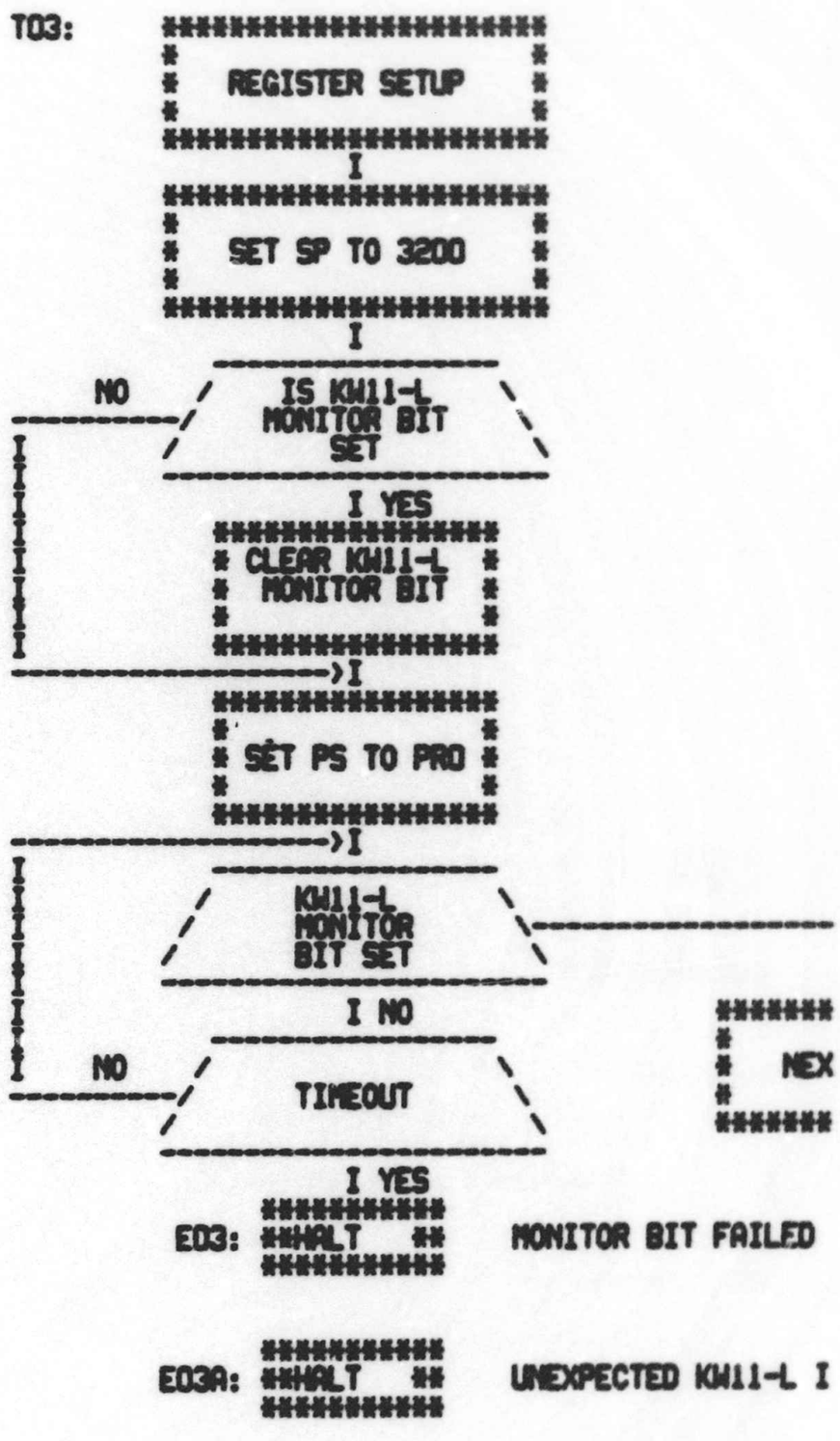
THE RESERVED INSTRUCTION AND NON-EXISTANT MEMORY
SHOWN IN THIS TEST, SHOULD ANY TEST IN THIS DIAGN
HALT WILL BE ON THIS PAGE IT WILL BE NECESSARY TO
STACK TO DETERMINE WHERE THE TRAPPED WAS CAUSED.

BASIC MEMORY TIMING TESTS FLOWS DECFLO VER 00.0



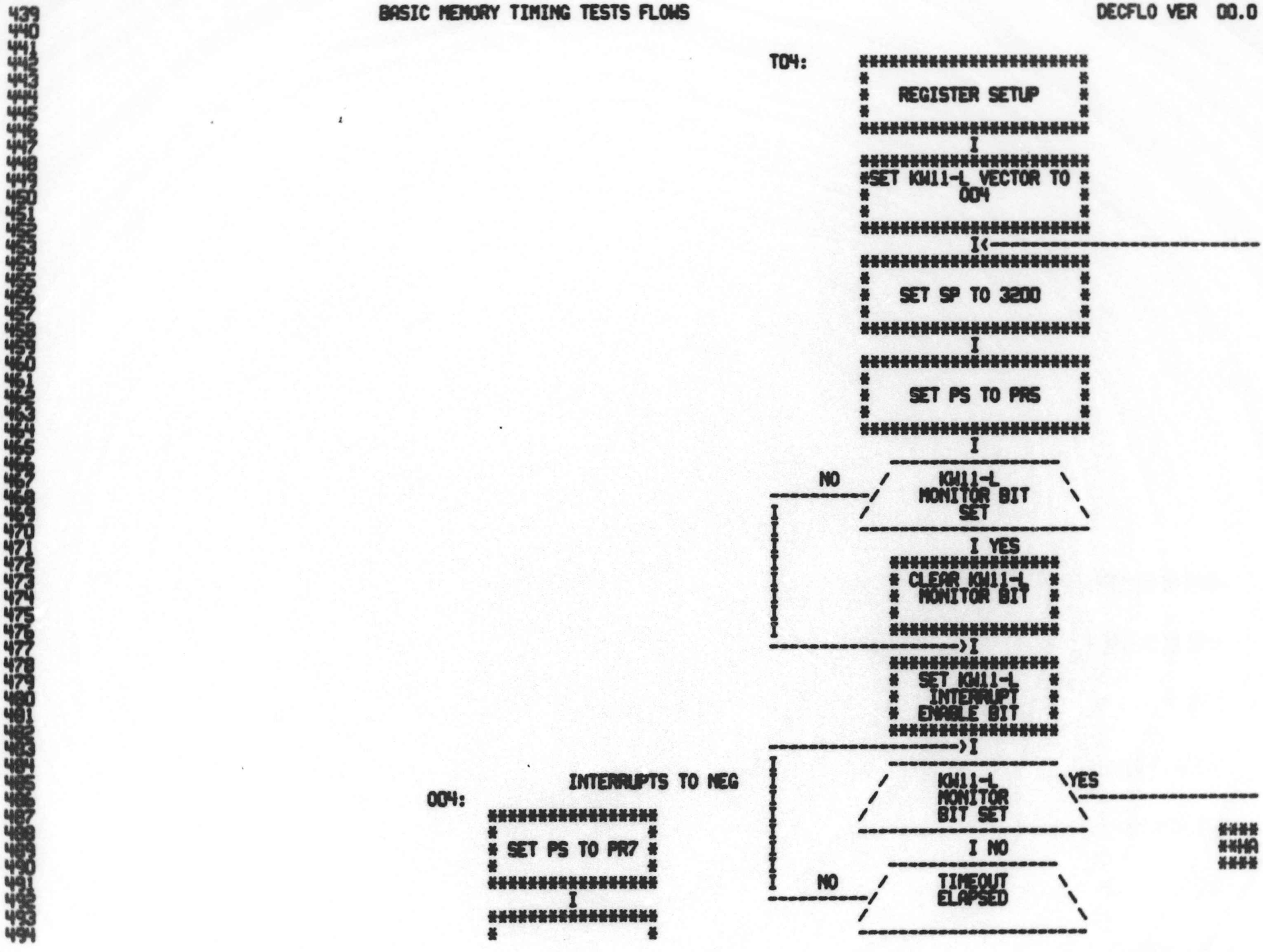
```
381                                                  ED2A: **HALT  **    UNEXPECTED KW11-L I
382                                                        **********
```

BASIC MEMORY TIMING TESTS FLOWS DECFLO VER 00.0



BASIC MEMORY TIMING TESTS FLOWS

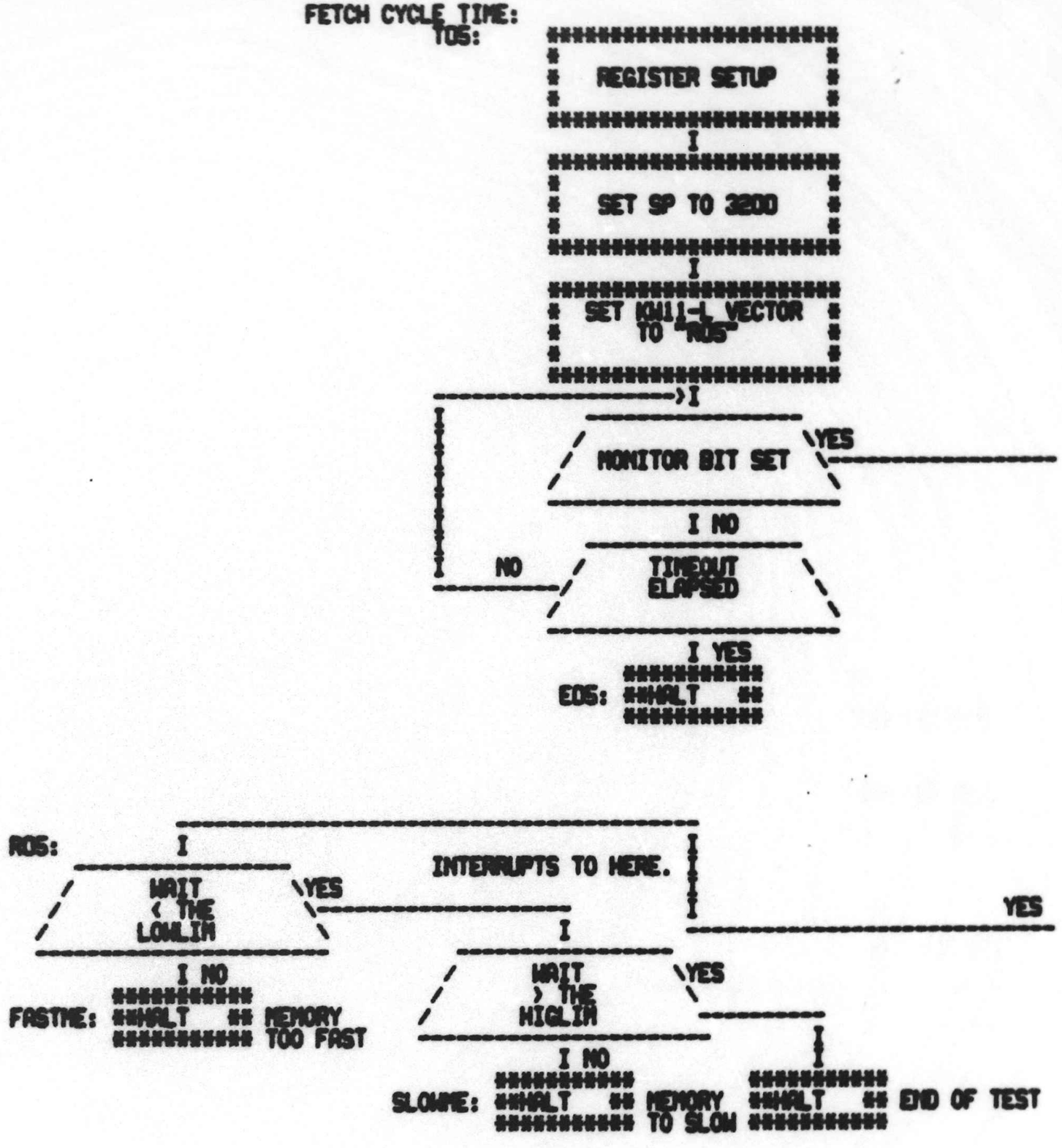
DECFLO VER 00.0



```
                                        *  NEXT TEST  *
                                        *             *
                                        ###############
```

BASIC MEMORY TIMING TESTS FLOWS

DECFLO VER 00.0



```
554
555
556
```

EO

BASIC MEMORY TIMING TESTS FLOWS
FLOW CHART CROSS REFERENCE LIST

DECFLO VER 00.0

HALT	01#	02	02	03	03	04#	05	05	05	05	05

```
                                        %
                                .TITLE  BNTT
                                .ENABL  ABS
001000                          .=1000
                                ;
                                ;KW11-L REAL TIME CLOCK BIT DEFINITIONS
                                ;
000200                          KWLMON=200              ;SET BY THE LINE FREQUENCY CLOCK
000100                          KWLENA=100              ;LINE CLOCK INTERRUPT ENABLE
                                ;
                                ;REGISTER ADDRESSES
                                ;
177546                          LKSCSR=177546           ;COMMAND STATUS REGISTER ADDRESS
                                ;
                                ;DEVICE VECTOR ASSIGNMENTS
                                ;
000100                          LKSVEC=100              ;INTERRUPT VECTOR ADDRESS
000300                          LKSPRT=PR6              ;PRIORITY 6
                                ;
177776                          PS=177776               ;PROCESSOR STATUS.
003200                          STACK=3200              ;STACK PRESET.
                                ;
                                ;PRIORITY LEVELS EQUATES
                                ;
000340                          PR7=340
000300                          PR6=300
000240                          PR5=240
000200                          PR4=200
000140                          PR3=140
000100                          PR2=100
000040                          PRI=040
000000                          PR0=000
                                ;
                                ;
000004                          ERRVEC=4                ;BUS TIMEOUT TRAP (ILLEGAL OR NONEXISTANT MEMORY).
000010                          RESVEC=10               ;RESERVED INTRUCTION TRAP.
```

```
                        .SBTTL  KW11-L DEVICE RESPONSE
                        ;**********************************************************************
                        ;THIS ROUTINE MAKES A BASIC CHECK OF THE KW11-L REAL TIME CLOCK
                        ;THE TESTS TEST AS FOLLOWS:
                        ;
                        ;       (T01)   THAT WE CAN ACCESS THE "LKSCSR" WITHOUT A NXM TIMEOUT.
                        ;
                        ;       (T02)  THAT THE MONITOR BIT IS SET BY THE LINE CURRENT AFTER
                        ;        A REASONABLE PERIOD OF TIME
                        ;
                        ;       (T03)  THAT THE MONITOR BIT SET WITHOUT INTERRUPT ENABLE DOES NOT CAUSE
                        ;        AN INTERRUPT
                        ;
                        ;       (T04)  THAT THE INTERRUPT ENABLE BIT WHEN SET WILL ALLOW INTERRUTS
                        ;
                        ;       (T05)   THIS TEST DETERMINES THAT THE CPU CYCLE TIME IS WITHIN LIMITS.
                        ;
                        ;**********************************************************************
                        ;
001000  012700  000001  T01:    MOV     #1,R0                   ;R0=TEST NUMBER.
001004  012701  000001          MOV     #1,R1                   ;R1=DEVICE (CLOCK #1).
001010  012702  177546          MOV     #LKSCSR,R2              ;R2=TEST ADDRESS.
001014  005003                  CLR     R3                      ;CLEAR WAS ADDRESS.
001016  005004                  CLR     R4                      ;CLEAR SHOULD BE ADDRESS.
                        ;
001020  012737  001102  000004          MOV     #ED1A,@#ERRVEC          ;SET NXM TRAP.
001026  012737  000340  000006          MOV     #PR7,@#ERRVEC+2         ;SET PRIORITY TO #7.
                        ;
001034  012737  001106  000010          MOV     #ED1B,@#RESVEC          ;SET ILLEGAL COMMAND TRAP.
001042  012737  000340  000012          MOV     #PR7,@#RESVEC+2         ;SET PRIORITY TO #7.
                        ;
001050  012737  001112  000100          MOV     #ED1C,@#LKSVEC          ;SET CLOCK INTERRUPT VECTOR.
001056  012737  000300  000102          MOV     #LKSPRT,@#LKSVEC+2      ;SET CLOCK PRIORITY.
                        ;
001064  012706  003200  L01:    MOV     #STACK,SP               ;SET STACK TO 3200.
001070  012737  000340  177776          MOV     #PR7,@#PS               ;SET CPU PRIORITY TO #7.
                        ;
001076  005712  I01:    TST     (R2)                    ;TEST FOR THE CLOCK.
001100  000406          BR      T02                     ;GOTO NEXT TEST.
                        ;
                        ;**********************************************************************
                        ;
                        ;TEST   #1.
                        ;
                        ;(PC)   (PS)    (SP)    TEST    DEV#    ADDRESS WAS     S/B
                        ;
                        ;(R7)   (PSW)   (R6)    (R0)    (R1)    (R2)    (R3)    (R4)
                        ;
                        ;1104   340     3174    1       1       177546  0       0
                        ;
                        ;**********************************************************************
                        ;
001102  000000  ED1A:   HALT                            ;###NON EXISTANT MEMORY TRAP (NO CLOCK).
001104  000767          BR      L01                     ;LOCK ON FATAL ERROR.
                                                        ;THIS ERROR MCOULD BE CAUSED
                                                        ;BY A TEST OTHER THAN "TEST #1"
```

```
                                                ;CHECK THE CONTENTS OF THE STACK
                                                ;TO DETERMINE IT'S ORIGIN.
                        ;*************************************************************
                        ;
                        ;TEST   #1
                        ;(PC)   (PS)    (SP)    TEST    DEV#    ADDRESS WAS     S/B
                        ;(R7)   (PSW)   (R6)    (R0)    (R1)    (R2)    (R3)    (R4)
                        ;1110   340     3174    1       1       177546  0       0
                        ;*************************************************************
001106  000000  ED1B:   HALT
001110  000765          BR      LD1                     ;***ILLEGAL COMMAND.
                                                        ;LOCK ON FATAL ERROR.
                                                        ;SEE COMMENT FOR PREVIOUS ERROR.
                        ;*************************************************************
                        ;TEST   #1
                        ;(PC)   (PS)    (SP)    TEST    DEV#    ADDRESS WAS     S/B
                        ;(R7)   (PSW)   (R6)    (R0)    (R1)    (R2)    (R3)    (R4)
                        ;1114   340     3174    1       1       177546  0       0
                        ;*************************************************************
001112  000000  ED1C:   HALT
001114  000763          BR      LD1                     ;*** UNEXPECTED KW11-L INTERRUPT.
                                                        ;LOCK ON FATAL ERROR.
```

H02


```
                                .SBTTL  KW11-L MONITOR BIT.
                                ;*************************************************************************
                                ;
                                ;       T02 ATTEMPTS TO SEE IF THE LINE CURRENT EVER SETS THE MONITOR
                                ;       BIT. THIS IS ACCOMPLISED AS FOLLOWS:
                                ;
                                ;       1).TEST TO SEE IF THE MONITOR BIT IS ALREADY SET,IT PROBABLY WILL BE.
                                ;
                                ;       2).IF THE MONITOR BIT WAS SET CLEAR IT.
                                ;
                                ;       3).CLEAR A TIMER REGISTER FOR MAXIMUM WAITING TIME.
                                ;
                                ;       4).WAIT AROUND IN A TIME LOOP FOR THE FLAG TO SET.
                                ;
                                ;       5).IF IT FAILS TO SET PRIOR TO TIMEOUT THEN HALT.
                                ;
                                ;*************************************************************************
                                ;
001116  012700  000002          T02:    MOV     #2,R0                   ;R0=TEST NUMBER.
001122  012701  000001                  MOV     #1,R1                   ;R1=DEVICE (CLOCK #1).
001126  012702  177546                  MOV     #LKSCSR,R2              ;ADDRESS TO R2.
001132  012704  000200                  MOV     #KALMON,R4              ;SHOULD BE.
                                ;
001136  012737  001204  000100          MOV     #ET2A,@#LKSVEC          ;SET KW11-L INTERRUPT VECTOR.
001144  012737  000340  000102          MOV     #PR7,@#LKSVEC+2         ;SET PRIORITY TO #7.
                                ;
001152  012706  003200          L02:    MOV     #STACK,SP               ;SET STACK TO 3200.
001156  005005                          CLR     R5                      ;CLEAR TIMER.
                                ;
001160  030412                          BIT     R4,(R2)                 ;MONITOR BIT SET?
001162  001401                          BEQ     R02                     ;NO!
                                ;                                       ;YES!
001164  040412                          BIC     R4,(R2)                 ;CLEAR MONITOR BIT.
                                ;
001166  011203                  R02:    MOV     (R2),R3                 ;CONTENTS OF LKSCSR TO R3.
001170  030412                          BIT     R4,(R2)                 ;MONITOR BIT SET?
001172  001006                          BNE     T03                     ;YES! GOTO "T03"
                                ;                                       ;NO!
001174  005205                          INC     R5                      ;TIMEOUT OVER?
001176  001373                          BNE     R02                     ;NO! CHECK MONITOR BIT AGAIN.
                                ;
                                ;*************************************************************************
                                ;
                                ;TEST   #2
                                ;
                                ;(PC)   (PS)    (SP)    TEST    DEV#    ADDRESS WAS     SHD BE
                                ;
                                ;(R7)   (PSW)   (R6)    (R0)    (R1)    (R2)    (R3)    (R4)
                                ;
                                ;1202   340     3200    2       1       177546  ??????  200
                                ;
                                ;*************************************************************************
                                ;
001200  000000          E02:    HALT                                    ;### MONITOR BIT FAILED TO SET.
001202  000763                  BR      L02                             ;LOCK ON FATAL ERROR.
                                ;
```

```
                                ;*****************************************************************************
                                ;TEST   #2
                                ;(PC)   (PS)    (SP)    TEST    DEV#    ADDRESS WAS     S/B
                                ;(R7)   (PSW)   (R6)    (R0)    (R1)    (R2)    (R3)    (R4)
                                ;1206   340     3174    2       1       177546  ??????  200
                                ;*****************************************************************************
                                ;
001204  000000                  E02A:   HALT                            ;***UNEXPECTED KW11 - L INTERRUPT.
001206  000761                          BR      L02                     ;LOCK ON FATAL ERROR.
```

```
                                .SBTTL  KW11-L INTERRUPT ENABLE BIT.
                                ;*************************************************************************
                                ;
                                ;       T03 VERIFYS THAT THE MONITOR ENABLE BIT BECOMING SET WITH
                                ;       MACHINE PRIORITY AT 0, WILL NOT CAUSE AN INTERRUPT UNLESS INTERRUPT
                                ;       ENABLE IS ALSO SET, AS FOLLOWS:
                                ;
                                ;       1).TEST TO SEE IF MONITOR BIT IS SET.
                                ;
                                ;       2). IF THE MONITOR BIT WAS SET THEN CLEAR IT.
                                ;
                                ;       3).SET CPU PRIORITY TO #0.
                                ;
                                ;       4).CLEAR THE TIMER FOR MAXIMUM WAITING TIME.
                                ;
                                ;       5).WAIT FOR THE MONITOR BIT TO SET IF IT DOESNT SET
                                ;       PRIOR TO THE TIMEOUT THAN HALT.
                                ;
                                ;*************************************************************************
                                ;
001210  012700  000003          T03:    MOV     #3,R0                   ;R0=TEST NUMBER.
001214  012701  000001                  MOV     #1,R1                   ;DEVICE (CLOCK #1).
001220  012702  177546                  MOV     #LKSCSR,R2              ;ADDRESS TO R2.
001224  012704  000200                  MOV     #KWLMON,R4              ;SHOULD BE.
001230  012737  001274  000100          MOV     #E03A,@#LKSVEC          ;SET KW11 - L INTERRUPT VECTOR.
                                ;
001236  012706  003200          L03:    MOV     #STACK,SP               ;SET THE STACK POINTER TO 3200.
                                ;
001242  030412                  N03:    BIT     R4,(R2)                 ;MONITOR BIT SET?
001244  001401                          BEQ     R03                     ;NO!
                                                                        ;YES!
001246  040412                          BIC     R4,(R2)                 ;CLEAR MONITOR BIT.
                                ;
001250  005037  177776          N03:    CLR     @#PS                    ;SET CPU PRIORITY TO PRO.
001254  005005                          CLR     R5                      ;CLEAR TIMER.
                                ;
001256  011203                  R03:    MOV     (R2),R3                 ;CONTENTS OF LKSCSR TO R3.
001260  030412                          BIT     R4,(R2)                 ;MONITOR BIT SET?
001262  001006                          BNE     T04                     ;YES! GOTO "T04"
                                                                        ;NO!
001264  005205                          INC     R5                      ;TIMEOUT OVER?
001266  001373                          BNE     R03                     ;NO! CHECK MONITOR BIT AGAIN.
                                ;
                                ;*************************************************************************
                                ;
                                ;TEST   #3
                                ;
                                ;(PC)   (PS)    (SP)    TEST    DEV#    ADDRESS WAS     SHD BE
                                ;
                                ;(R7)   (PSW)   (R6)    (R0)    (R1)    (R2)    (R3)    (R4)
                                ;
                                ;1272   0       3200    3       1       177546  ??????  200
                                ;
                                ;*************************************************************************
                                ;
001270  000000                  E03:    HALT                            ;### MONITOR BIT FAILED TO SET.
```

```
 816  001272  000761                    BR      L03                     ;LOCK ON FATAL ERROR.
 817                                ;
 818                                ;#########################################################################
 819                                ;
 820                                ;TEST  #3
 821                                ;
 822                                ;(PC)   (PS)   (SP)   TEST   DEV#   ADDRESS WAS     S/B
 823                                ;
 824                                ;(R7)   (PSW)  (R6)   (R0)   (R1)   (R2)    (R3)    (R4)
 825                                ;
 826                                ;1276   340    3174   1      1      177564  ??????  200
 827                                ;
 828                                ;#########################################################################
 829                                ;
 830  001274  000000                ED3A:   HALT                            ;***UNEXPECTED KW11 - L INTERRUPT.
 831  001276  000757                        BR      L03                     ;LOCK ON FATAL ERROR.
```

```
                        .SBTTL  KW11-L INTERRUPT.
                        ;*************************************************************************
                        ;
                        ;       TO4 VERIFYS THAT THE KW11-L WILL CAUSE
                        ;       AN INTERRUPT WHEN THE ENABLE BIT IS SET AND THE LINE
                        ;       CURRENT CAUSES THE MONITOR BIT TO BE SET, AND THE CPU PRIORITY
                        ;       IS SET AT #5 AS FOLLOWS.
                        ;
                        ;       1). SET UP KW11-L CLOCK TO TRAP TO NEXT TEST.
                        ;
                        ;       2). IF MONITOR BIT IS SET. CLEAR IT.
                        ;
                        ;       3). SET INTERRUPT ENABLE BIT.
                        ;
                        ;       4). CLEAR THE TIMER REGISTER FOR MAXIMUM WAITING TIME.
                        ;
                        ;       5). TEST TO SEE IF THE MONITOR BIT IS SET.
                        ;
                        ;       6). IF WE GET INTERRUPTED WE WILL GO TO NEXT TEST.
                        ;       OTHERWISE ERROR HALT.
                        ;
                        ;*************************************************************************
                        ;
001300  012700  000004  TO4:    MOV     #4,R0           ;R0=TEST NUMBER.
001304  012701  000001          MOV     #1,R1           ;R1=DEVICE (CLOCK #1).
001310  012702  177546          MOV     #LKSCSR,R2      ;ADDRESS TO R2.
001314  012704  000200          MOV     #KWLMON,R4      ;SHOULD BE.
001320  012737  001370  000100  MOV     #ED4,@#LKSVEC   ;SET KW11 - L VECTOR.
                        ;
001326  012706  003200  LO4:    MOV     #STACK,SP       ;SET STACK TO 3200.
001332  012737  000240  177776  MOV     #PR5,@#PS       ;SET CPU STATUS TO #5.
                        ;
001340  030412          BIT     R4,(R2)         ;MONITOR BIT SET?
001342  001401          BEQ     NO4             ;NO!
                                                ;YES!
001344  040412          BIC     R4,(R2)         ;CLEAR MONITOR BIT.
                        ;
001346  052712  000100  NO4:    BIS     #KWLENA,(R2)    ;SET ENABLE BIT.
                        ;
001352  011203  RO4:    MOV     (R2),R3         ;CONTENRO4 OF LKSCSR TO R3.
001354  030412          BIT     R4,(R2)         ;MONITOR BIT SET?
001356  001002          BNE     ED4             ;YES! GOTO "ED4" NO INTERRUPTS.
                                                ;NO!
001360  005205          INC     R5              ;TIMEOUT OVER?
001362  001373          BNE     RO4             ;NO!
                        ;
                        ;*************************************************************************
                        ;
                        ;TEST   #4
                        ;
                        ;(PC)   (PS)    (SP)    TEST    DEV#    ADDRESS WAS     SHD BE
                        ;
                        ;(R7)   (PSW)   (R6)    (R0)    (R1)    (R2)    (R3)    (R4)
                        ;
                        ;1366   240     3200    4       1       177546  ??????  200
```

```
                                        ;
                                        ;*****************************************************************
                                        ;
001364  000000                  EO4:   HALT                            ;FATAL ERROR
001366  000757                         BR      LO4                     ;HANG ON FATAL ERROR.

001370  012737  000340  177776  004:   MOV     #PR7,@#PS               ;SET PRIORITY TO #7.
```

```
                        .SBTTL  KW11-L FETCH CYCLE TIMING.
                        ;**********************************************************************
                        ;
                        ;       TO5 DETERMINES THE PROCESSOR CYCLE TIME. THIS IS
                        ;       ACCOMPLISHED AS FOLLOWS:
                        ;
                        ;       1).THE KW11-L IS MONITORED UNTIL WE GET TO THE NEXT MONITOR
                        ;       BIT SET.
                        ;
                        ;       2). CLEAR THE MONITOR BIT.
                        ;
                        ;       3). CLEAR THE TIMER (R5).
                        ;
                        ;       4). SET CPU PRIORITY TO PR5.
                        ;
                        ;       5). WAIT FOR THE INTERRUPT WHILE IN THE TIMEOUT LOOP.
                        ;
                        ;       6). CHECK THAT THE TIME SPENT WAITING FOR THE INTERRUPT
                        ;       WAS WITHIN TOLERANCE.
                        ;
                        ;       7).THE CODE WILL RUN UNTIL WE HAVE SERVICED 1 INTERRUPT
                        ;
                        ;**********************************************************************
                        ;
001376  012700  000005  ;TO5:    MOV     #5,R0           ;R0=TEST ADDRESS.
001402  012701  000001          MOV     #1,R1           ;R1=DEVICE (CLOCK #1).
001406  012702  177546          MOV     #LKSCSR,R2      ;ADDRESS TO R2.
001412  012704  000200          MOV     #KWLMON,R4      ;SHOULD BE.
                        ;
001416  012706  003200  ;L05:    MOV     #STACK,SP       ;RESET STACK POINTER.
001422  005005                  CLR     R5              ;CLEAR TIMER.
                        ;
001424  012737  001476  000100  MOV     #R05,@#LKSVEC   ;SET UP INTERRUPT VECTOR
                        ;
001432  011203  ;P05:    MOV     (R2),R3         ;CONTENTS OF LKSCSR TO R3.
001434  030412          BIT     R4,(R2)         ;MONITOR BIT SET?
001436  001004          BNE     N05             ;YES
                        ;
001440  005205          INC     R5              ;WAIT.
001442  001373          BNE     P05             ;NO!
                        ;
                        ;**********************************************************************
                        ;
                        ;TEST   #5
                        ;
                        ;(PC)   (PS)    (SP)    TEST    DEV#    ADDRESS WAS     SHD BE
                        ;
                        ;(R7)   (PSW)   (R6)    (R0)    (R1)    (R2)    (R3)    (R4)
                        ;
                        ;1446   340     3200    5       1       177546  ??????  200
                        ;
                        ;**********************************************************************
                        ;
001444  000000  ;E05:    HALT                    ;###MONITOR BIT FAILED TO SET.
001446  000763          BR      L05             ;LOCK ON FATAL ERROR.
```

```
001450 010412          MOS:    BIC     R4,(R2)                 ;CLEAR MONITOR BIT
001452 052712 000100           BIS     #KWLENA,(R2)            ;SET INTERRUPT ENABLE BIT.

001456 005005                  CLR     R5                      ;CLEAR TIMER,
001460 012737 000240 177776    MOV     #PRS,@#PS               ;SET CPU TO PRIORITY #5.

001466 005205          1S:     INC     R5                      ;AWAIT AN INTERRUPT.
001470 001376                  BNE     1S

                       ;##################################################################
                       ;TEST   #5
                       ;(PC)   (PS)    (SP)    TEST    DEV#    ADDRESS WAS     SHD BE
                       ;(R7)   (PSW)   (R6)    (R0)    (R1)    (R2)    (R3)    (R4)
                       ;1470   240     3200    5       1       177546  ??????  200
                       ;##################################################################

001472 000000          EOSA:   HALT                            ;### NO KW11-L INTERRUPT.
001474 000750                  BR      LOS                     ;LOCK ON FATAL ERROR.

001476 020527 001520   ROS:    CMP     R5,@#LOWLIM             ;IS MEMORY TO FAST?
001502 103404                  BLO     FASTME                  ;YES!

001504 020527 001522           CMP     R5,@#HIGLIM             ;IS MEMORY TO SLOW?
001510 101002                  BHIS    SLOWME                  ;YES!
001512 000000                  HALT                            ;TEST OKAY. NORMAL HALT

001514 000000          FASTME: HALT
001516 000000          SLOWME: HALT
001520 012000          LOWLIM: 012000
001522 012300          HIGLIM: 012300
000001                 .END
```

```
ERRVEC= 000004          597#    624#  625#
$01A    001102          654     651#
$01B    001106          657     670#
$01C    001112          630     686#
$02     001200          741#
$02A    001204          711     756#
$03     001270          815#
$03A    001274          784     830#
$04     001364          874     891#
$05     001444          919#
$05A    001472          973#
FIXSTK  001514          977     984#
HIGLIM  001532          979     987#
I01     001076          636#
KAMLEN=  000100         571#    870     953
KAMLMN=  000200         570#    709     783     958     923
LICSCR=  177546         575#    520     708     782     857     922
LICSPNT= 000300         580#    531
LICSVEC= 000100         579#    630#    631#    711#    712#    784#    859#    928#
LOWLIM  001520          976     986#
L01     001054          633#    652     671     687
L02     001152          714#    742     757
L03     001236          786#    816     831
L04     001262          851#    882
L05     001416          925#    950     974
M03     001260          709     793#
M04     001346          846     870#
M05     001450          902     952#
P04     001270          859     894#
PRO     =  000000       594#
PR1     =  000040       593#
PR2     =  000100       592#
PR3     =  000140       591#
PR4     =  000200       590#
PR5     =  000240       589#    863     956
PR6     =  000300       588#    898#
PR7     =  000340       587#    638     634     712     894
PS      =  177776       586#    794#    793#    863#    894#    956#
PS      001432          585     596
RESVEC= 000010          627#    638#
R0      =  000000       618#    706#    780#    855#    920#
R02     001166          718     722#    727
R03     001206          796#    801
R04     001246          872#    877
R05     001476          926     926#
R1      =  000001       619#    707#    781#    855#    921#
R2      =  000002       620#    708#    717     720#    722     723     782#    788     791#    796     797     857#
                        869#    870#    872     873     922#    930     931     952#    953#
R3      =  000003       621#    722#    796#    872#    930#
R4      =  000004       622#    709#    717     720     723     783#    788     791     797     858#    865     868     873
                        922#    931     952
R5      =  000005       715#    782#    794#    800#    876#    926#    934#    955#    958#    976     979
SLOWE   001516          960     965#
SP      =  000006       623#    714#    786#    861#    925#
STACK   =  003200       563#    633     714     786     861     925
T01     001000          618#
```

```
BNTT    MACY11 27(732)  14-OCT-76  16:22  PAGE 31
DBKMAA.P11      CROSS REFERENCE TABLE -- USER SYMBOLS

T02      001116              637     706#
T03      001210              724     780#
T04      001300              798     855#
T05      001376              920#
.      = 001524              566#
```

```
COMMEN          18
ENDCOM          18
ESCAPE          18
FILL            18
FOMTST          18
POP             18
PUSH            18
SETUP           18
SKIP            18
SLASH           18
STORS           18
TYPDIN          18
TYPOEC          18
TYPULN          18
TYPOSS          18
TYPOCT          18
TYPTXT          18
.BREAKP         18
.EXIT           18
.HERE           18
.KT11           18
.SETUP          18
.SUBRT          18
.SCRTC          18
.SCRTA          18
.MOVRD          18
.MOVRO          18
.DIV            18
.MUL            18
.SETUP          18
.SUBRT          18
.FILLT          18
.FILL           18
.SKIP           18
.SLASH          18
.STYPB          18
.STYPD          18
.STYPE          18
.STYPO          18
```

F03

```
BNTT    MACY11 27(732)  14-OCT-76  16:22  PAGE 35
DBKMAA.P11      CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

BEQ      718     789     866
BHIS     980
BHIS     720     791     868     952
BHIS     874     953
BHIT     717     723     788     797     865     873     931
BLO      977
BNE      724     727     798     801     874     877     932     935     959
BR       637     643     671     947     742     757     816     831     892     950     974
CLR      631     636     715     743     791     926     955
CMP      976     979
HALT     651     670     686     741     756     815     830     891     949     973     981     984     985
INC      726     800     876     934     958
MOV      618     619     620     624     626     627     628     630     631     633     634     706     707     708     709
         711     712     714     762     780     781     782     783     784     786     796     855     856     857     858
         859     861     863     872     894     920     921     922     923     925     928     930     956
TST      636
.ENABL     1     565
.END     988
.LIST      1
.MACRO     1
.NLIST     1
.REM       1
.SBTTL   599     608     760     832     895
.TITLE   564


ERRORS DETECTED:  0
DEFAULT GLOBALS GENERATED:  0

*,DBKMAA.SEQ/SQL/CRF/PRONUM/NL:TOC/DS:ERFZ=DBKMAA.SML,DBKMAA.P11
RUN-TIME:  14 17  .5 SECONDS
RUN-TIME RATIO:  109/32=3.4
CORE USED:  20K  (39 PAGES)
```