

DJ11

LOGIC TEST
MD-11-DZDJA-D

EP-DZDJA-D-DL-A
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digital
MADE IN USA

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2	1	0	1	1	0	1	0	1	1	0
3	1	1	0	1	1	0	1	1	0	1
4	0	1	1	0	1	0	1	1	0	1
5	1	0	1	1	0	1	0	1	1	0
6	1	1	0	1	1	0	1	1	0	1
7	0	1	1	0	1	0	1	1	0	1
8	1	0	1	1	0	1	0	1	1	0
9	1	1	0	1	1	0	1	1	0	1
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DATA STORE

134

/BATTLES-0-SYSTEMS, 2011-10-13, 15:13:22 Monitor IPC-D 5078 [1A3] #START#

DATA STORE

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/BATTLES-0-SYSTEMS, 2011-10-13, 15:13:22 Monitor IPC-D 5078 [1A3] #START#

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LF 1117 Version 6 (100344) Running on MTA1
+ User: Dave O'Brien (400 2704) Job
Request created: 13-Oct-76 14:51:19

DDJAD Seq. 23 Date 13-Oct-76 15:13:22 Monitor IPC-C 5078 (1A3) *START*
*TO: ML21-4:DRIVES -- distribution to ML21-4, slot 134

E: 55420: 022 JAD: 5501: 08: 2704: 7ICE: 1341: 11: 0: 157: 15: 29: 100: 11: 20: 117: 481: 45: 33: 30: 35: 76: 15: 13: 25
File will be REWIND to (037) protection

.REN :

IDENTIFICATION

PRODUCT CODE: MAINDEC-11-DZDJA-D-D
PRODUCT NAME: DJ11 LOGIC TESTS
PROGRAM DATE: MAY 1976
MAINTAINER: DIAGNOSTIC GROUP

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4.3 PROGRAM AND OPERATOR ACTION

- 1) LOAD PROGRAM INTO MEMORY USING ABS LOADER.
- 2) LOAD ADDRESS 200.
- 3) IF HARDWARE SWITCH REGISTER IS AVAILABLE, SET SWITCHES (SEE SEC. 5.1), ALL DOWN FOR WORST CASE, PRESS START.
- 4) IF SWITCH-LESS PROCESSOR SIMPLY PRESS START.
- 5) ENTER PARAMETERS (SEE SEC. 5.3) AS THEY ARE REQUESTED.
- 6) THE PROGRAM WILL LOOP AND BELL WILL RING ONCE EVERY PASS.
- 7) A MINIMUM OF TWO PASSES SHOULD ALWAYS BE RUN.

5. OPERATING PROCEDURE

5.1 OPERATIONAL SWITCH SETTINGS

AT SA 200, ALL SWITCHES DOWN IS WORST CASE TESTING. EACH SUBTEST WILL BE LOOPED UPON UNTIL COMPLETION OF 16 PASSES OF THAT SUBTEST. THE BELL WILL RING UPON COMPLETION OF A PASS OF THE ENTIRE PROGRAM. ALTERNATE PASS WILL RUN WITH THE 1-BIT SET.

THE SWITCH SETTINGS ARE:

SW<15> = 1 HALT ON ERROR
SW<14> = 1 SCOPE LOOP
SW<13> = 1 INHIBIT PRINTOUT
SW<12> = 1 INHIBIT TRACE TRAPPING
SW<11> = 1 INHIBIT ITERATIONS OF SUBTEST
SW<10> = 1 BELL ON ERROR
 = 0 BELL ON PASS COMPLETE
SW<09> = 1 LOOP ON ERROR
SW<08> = 1 LOOP ON TEST IN SW<7:0>

THIS PROGRAM HAS BEEN MODIFIED TO RUN ON A PROCESSOR WITH OR WITHOUT A HARDWARE SWITCH REGISTER. WHEN FIRST EXECUTED THE PROGRAM TESTS THE EXISTENCE OF A HARDWARE SWITCH REGISTER. IF NOT FOUND A SOFTWARE SWITCH REGISTER LOCATION (SWREG=LOC. 176) IS DEFAULTED TO. IF THIS IS THE CASE, UPON EXECUTION THE CONTENTS OF THE SWREG ARE DUMPED IN OCTAL ON THE CONSOLE TTY AND ANY CHANGES ARE REQUESTED

(I.E.) SWR=XXXXXX NEW=

POSSIBLE RESPONSES ARE:

1. <CR> IF NO CHANGES ARE TO BE MADE.
2. 6 DIGITS 0-7 TO REPRESENT IN OCTAL THE NEW SWITCH REGISTER VALUE; LAST DIGIT FOLLOWED BY <CR>.
3. 1U TO ALLOW REENTERING VALUE IF ERROR IS

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MAINDEX-11-0200A-D
020001.P11

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COMMITTED KEYING IN SWREG VALUE.

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BUILT INTO THE PROGRAM IS THE ABILITY TO DYNAMICALLY CHANGE THE CONTENTS OF SWREG DURING PROGRAM EXECUTION. BY STRIKING ^G (CNTRL G) ON CONSOLE TTY THE OPERATOR SETS A REQUEST FLAG TO CHANGE THE CONTENTS OF SWREG, WHICH IS PROCESSED IN KEY AREAS OF THE PROGRAM CODE (IE) ERROR ROUTINES, AFTER HALTS END OF PASS, AND OTHER APPLICABLE AREAS.

5.2 SUBROUTINE ABSTRACTS

5.2.1 SCOPE

THIS SUBROUTINE CALL (VIA A TRAP INSTRUCTION) IS PLACED BETWEEN EACH SUBTEST IN THE INSTRUCTION SECTION. IT RECORDS THE STARTING ADDRESS OF EACH SUBTEST AS IT IS BEING ENTERED IN LOCATION "LAD". IF A SCOPE LOOP IS REQUESTED, THE CURRENT SUBTEST WILL BE LOOPED UPON. SW<11> ON A 1 INHIBITS ITERATION OF SUBTESTS. THE CONTENTS OF "LAD" MAY BE USED TO DETERMINE THE LAST SUBTEST SUCCESSFULLY COMPLETED.

5.2.2 HLT

THIS ROUTINE (CALLED BY AN EMT INSTRUCTION) PRINTS OUT AN ERROR MESSAGE (SEE 6.1). IF SW<9> IS ON A 1 AND A HLT IS EXECUTED, THE SUBTEST WILL BE LOOPED UPON UNTIL 16 CONSECUTIVE GOOD PASSES ARE COMPLETED. TO INHIBIT TYPEOUTS, PUT SW<13> ON A 1. TO RING THE BELL ON AN ERROR, PUT SW<10> ON A 1.

5.2.4 TRTRAP

IF SW<12> IS ON A 0, THE T-BIT WILL BE SET ON ALTERNATE PASSES. WHEN THE T-BIT IS SET, THE PROCESSOR TRAPS AFTER EACH INSTRUCTION. THE FIRST INSTRUCTION EXECUTED UPON TRAPPING IS AN "RTI" OR "RTT" WHICH RETURNS TO THE INTERRUPTED SEQUENCE OF INSTRUCTIONS. THIS SEQUENCE IS CONTINUED UNTIL THE END OF THE PROGRAM IS REACHED.

5.2.5 TRAPCATCHER

A ".+2" - "HALT" SEQUENCE IS REPEATED FROM 0 - 56 TO DETECT ANY UNEXPECTED TRAPS AND A ".+2" - "IOT" SEQUENCE IS REPEATED FROM 60 - 776 TO DETECT ANY UNEXPECTED INTERRUPTS. THUS ANY UNEXPECTED TRAPS WILL HALT AT THE VECTOR + 2. ANY UNEXPECTED INTERRUPTS WILL RESULT IN AN ERROR "HLT" IN "IOTRAP".

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L01

MAINDEC-11-DZDJA-D
DZDJAD.F11

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(RN) = CONTENTS OF GENERAL REGISTER "N". FROM NONE TO
FOUR OF THESE MAY BE TYPED DEPENDING ON THE NUMBER

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FOLLOWING THE HLT; E.G., HLT+3 WOULD TYPE (R1)
THRU (R3); HLT (BY ITSELF) WOULD STOP AFTER TYPING
ADR AND DJADR.

TO FIND THE FAILING TEST, LOOK AT THE LISTING ABOVE THE
ADDRESS TYPED. IN MOST CASES THE COMMENT BESIDE THE HLT
TELLS WHAT WAS BEING CHECKED AND WHAT WAS EXPECTED. ALSO, A
LIST OF THE PROBABLE FAILING LOGIC IS GIVEN IN THE COMMENTS
AT THE BEGINNING OF THE TEST.

6.2 ERROR RECOVERY

RESTART AT 200 OR 1000.

6.3 ERROR COUNTER

AN ERROR COUNT IS KEPT IN "ERRORS" (LOC 1202). IT CAN BE
CLEARED FROM THE CONSOLE, BY RESTARTING AT 200, OR BY
RELOADING THE PROGRAM.

7. RESTRICTIONS

IF MORE THAN ONE DJ11 IS TESTED AT A TIME, THE DEVICE
ADDRESSES AND THE VECTOR ADDRESSES MUST ALL BE CONTIGUOUS.

IF THIS PROGRAM IS RUN WITH A MONITOR, I.E. ACT11 OR DDP,
THE DEVICE ADDRESSES MUST FOLLOW THE FLOATING ADDRESS
CONVENTION. DJ11'S WILL BE FIRST, STARTING AT 160010,.

8. MISCELLANEOUS

8.1 EXECUTION TIME

DUE TO THE VARIOUS BAUD RATES AVAILABLE AND THE ABILITY TO
CHECK UP TO 8 DJ11'S AT ONCE, THE EXECUTION TIME CAN BE
ANYWHERE FROM 15 SECONDS TO THREE AND A HALF HOURS. THE
FOLLOWING TYPICAL TIMES ARE FOR ONE DJ11 WITH ALL LINES AT
THE SAME SPEED, 8 LEVEL CODE, 2 STOP BITS, AND NO PARITY ON
A PDP-11/20 WITHOUT TRACE TRAPPING. FOR MULTIPLE DJ11'S,
MULTIPLY THESE TIMES BY THE NUMBER OF UNITS SELECTED FOR
TEST.

BAUD RUN TIME

75 00:26:00
110 00:18:00
134.5 00:15:00

NO1

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DZDJAD.P11

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150 00:13:00
300 00:05:30


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001200 BEGIN: MOV #ICNT, SP ;SET UP STACK POINTER
001201 JSR PC, SUSWR ;CHECK FOR SWITCH REGISTER
001202 MOV #14, R0
001203 MOV #YESRT, (R0)+ ;TRACE TRAP VECTOR (14)
001204 MOV #340, (R0)+
001205 MOV #IOTRAP, (R0)+ ;IOT VECTOR (20)
001206 MOV #340, (R0)+
001207 MOV #PDOWN$, (R0)+ ;POWER FAIL VECTOR (24)
001208 MOV #340, (R0)+
001209 MOV #EMT$, (R0)+ ;EMT VECTOR (30)
001210 MOV #340, (R0)+
001211 MOV #TRAPS, (R0)+ ;TRAP VECTOR (34)
001212 MOV #340, (R0)+
001213 MOV #1$, J#10
001214 SXT R0 ;CHECK FOR PDP-11/40 OR 45
001215 MOV #RTT, J#YESRT
001216 MOV #RTT, J#6
001217 MOV #400, J#177774 ;SET UP STACK LIMIT TO 1000
001218 CLR J#6
001219 1$: MOV #12, J#10
001220 CLR ERRORS ;CLEAR ERROR COUNTER
001221 CLR PCNT ;CLEAR PASS COUNTER
001222 CLR PCNT+2
001223 TST J#42 ;CHECK FOR ACT11 OR DDP PRESENT
001224 BEQ GETADR ;BRANCH IF NONE
001225 JSR PC, AUTO ;GO TO SUBROUTINE TO "MAP" DJ11 ON THE SYS
001226 JMP RESTAR ;SKIP OPERATOR ACTION

001506 GETADR: TYPE, MSGADR ;TYPE "FIRST DJ11 ADDRESS"
001507 JSR R5, READIN ;READ INPUT FROM TTY AND SAVE
001508 .WORD DEVADR ;IN DEVADR
001509 BNE GETADR ;BRANCH IF BAD INPUT
001510 TST DEVADR
001511 BNE 1$
001512 MOV DEFADR, DEVADR
001513 1$: BIC #7, DEVADR
001514 CMP #160000, DEVADR
001515 BHI GETADR

001554 GETVEC: TYPE, MSGVEC ;TYPE "VECTOR ADDRESS:"
001555 JSR R5, READIN ;READ INPUT FROM TTY AND SAVE
001556 .WORD VECADR ;IN VECADR
001557 BNE GETVEC ;BRANCH IF BAD INPUT
001558 TST VECADR ;CHECK FOR CR
001559 BNE 1$
001560 MOV #300, VECADR ;SET TO FIRST FLOATING VECTOR
001561 1$: BIC #7, VECADR ;CLEAR TO MODULO 10
001562 CMP #300, VECADR ;CHECK FOR LOW LIMIT
001563 BGT GETVEC
001564 CMP #1000, VECADR ;CHECK FOR UPPER LIMIT
001565 BLE GETVEC

001632 GETNUM: TYPE, MSGNUM ;TYPE "NUMBER OR UNITS:"
001633 JSR PC, READS ;READ INPUT FROM THE TTY
; CHECK STRING FOR VALID DIGITS, TERMINATOR, AND 'P'
001634 MOV #INPUT, R2 ;POINTS TO INPUT STRING

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001646 112201      MOVB      (R2)+,R1      :LOAD 1ST CHAR
001650 001434      BEQ      1$           :BRANCH IF IMMEDIATE TERMINATOR
001652 122701 000120  CMPB     #'P,R1       :CHECK FOR A P
001656 001443      BEQ      CONFIG     :CONFIGURE MODE IF SO
001660 120127 000071  CMPB     R1,#71       :MUST BE A VALID ASCII NUMBER
001664 101362      BHI      GETNUM      :ELSE RETRY
001666 162701 000060  SUB      #60,R1       :STRIP ASCII CODE
001672 003757      BLE      GETNUM      :SHOULDN'T BE ZERO OR NEG
:1ST CHAR IS A VALID DIGIT, 1 THRU 9 - CHECK REST OF STRING
001674 105722      TSTB     (R2)+       :2ND CHAR A TERMINATOR?
001676 001433      BEQ      3$           :YES - R1 HAS THE FINAL # OF UNITS
001700 105712      TSTB     (R2)        :NO - NXT CHAR MUST BE THE TERMINATOR
001702 001353      BNE      GETNUM      :ELSE RETRY.
001704 124227 000071  CMPB     -(R2),#71   :CHECK 2ND CHAR FOR A VALID NUMBER
001710 101350      BHI      GETNUM
001712 111303      MOVB     (R2),R3     :MAKE IT MORE ACCESSIBLE
001714 162702 000060  SUB      #60,R3     :STRIP ASCII CODE
001720 100744      BMI      GETNUM      :SHOULDN'T BE NEGATIVE
:BOTHS LOW AND HIGH ORDER DIGITS ARE OK - CONVERT DECIMAL VALUE.
001722 010146      MOV      R1,-(SP)    :SAVE IT FOR LATER
001724 006201      ASL     R1           :MULT HI ORDER BY 8
001726 006201      ASL     R1
001728 006201      ASL     R1
001730 006201      ASL     R1
001732 006201      ASL     (SP)        :MULTIPLY IT BY 2
001734 062601      ADD     (SP)+,R1    :RESULT IS (HI ORD)*10.
001736 060201      ADD     R3,R1       :NOW ADD IN THE LOW ORDER
001738 000402      BR      3$
001740 012701 000001  1$:      MOV      #1,R1      :LOAD DEFAULT VALUE HERE
:R1 HAS THE CONVERTED VALUE - COMPARE AGAINST MAX ALLOWED.
001746 020127 000020  2$:      CMP      R1,#DJMXNO :TOO BIG?
001748 101327      BHI      GETNUM      :YES - RETRY.
001750 010137 001234      MOV      R1,UNITS   :VALUE OK - STORE RESULT
001752 012737 000100 001304  MOV      #100,DJUUT :PRIME UNIT UNDER TEST NUMBER
:
:CONFIG: TYPE, MSGOON
001766 000004 017343  JSR      PC          :TYPE "STANDARD CONFIG?"
001772 004737 016364  PC      READS      :READ INPUT FROM TTY
001776 122737 000120 016512  CMPB     #'P,INPUT   :CHECK FOR "P"
002004 001536      BEQ      RESTAR     :BRANCH IF PREVIOUS
002006 012700 000022  MOV      #22,R0     :SET UP COUNTER
002012 012701 001236  MOV      #LENGTH,R1 :POINT TO CHAR LEN TABLE
002014 005021  1$:      CLR      (R1)+      :PUT CHAR MASK FOR 8 IN CHAR TABLE
:AND CLR PARITY TABLE
002020 005300      DEC     R0          :COUNT DOWN
002022 001375      BNE     1$         :BRANCH IF NOT DONE
002024 105737 016512  TSTB     INPUT      :CHECK FOR CR
002030 001624      BEQ     RESTAR     :BRANCH IF DEFAULT
002032 122737 000131 016512  CMPB     #131,INPUT  :CHECK FOR "Y"
002040 001620      BEQ     RESTAR     :BRANCH IF DEFAULT
002042 122737 000116 016512  CMPB     #116,INPUT  :CHECK FOR "N"
002050 001346      BNE     CONFIG     :BRANCH IF ILLEGAL ENTRY
002052 005000      CLR     R0          :CLR UNIT COUNTER
002054 005001      CLR     R1          :CLR LINE COUNTER
002056 012702 001236  MOV      #LENGTH,R2 :SET UP POINTER TO CHAR MASK TABLE
002058 012703 001276  MOV      #PARITY,R3  :SET UP POINTER TO PARITY TABLE
002060 012704 000001  MOV      #1,R4       :SET UP MARKER
002062 000004 017377  TYPLIN: TYPE, MSGLIN :TYPE "LINES "

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700	0000076	010105		MOV	R1,TTY	:TYPE R1 IN OCTAL
701	0000100	004737	015572	JSR	PC,PRINTS	:AND SUPPRESS LEADING ZERO'S
702	0000104	000004	017410	TYPE,	MSGDAS	:TYPE A DASH (-)
703	0000110	062701	000003	ADD	#3, R1	:LAST LINE IN GROUP OF 4
704	0000114	010105		MOV	R1,TTY	:TYPE R1 IN OCTAL
705	0000116	004737	015572	JSR	PC,PRINTS	:AND SUPPRESS LEADING ZERO'S
706	0000120	005201		INC	R1	:FIRST LINE NEXT GROUP
707	0000124	000004	017414	GETLEN:	TYPE,	:TYPE "CHAR LENGTH:"
708	0000128	004737	016364	JSR	PC, READS	:READ FROM THE TTY
709	0000132	105737	016512	TSTB	INPUT	:CHECK FOR CR (DEFAULT)
710	0000140	001421		BEQ	GETPAR	:BRANCH IF DEFAULT
711	0000144	105737	016513	TSTB	INPUT+1	:CHECK FOR BAD DATA
712	0000148	001266		BNE	GETLEN	:BRANCH IF BAD
713	0000150	102737	000060	SUB	#60, INPUT	:CONVERT FROM ASCII
714	0000156	112712	177777	MOVB	#-1, (R2)	:SET UP MASK
715	0000160	106312		ASLB	(R2)	:CLEAR MASK BIT BY BIT
716	0000164	102357		BCC	GETLEN	:BAD INPUT, > 8
717	0000168	105337	016512	DECB	INPUT	:COUNT
718	0000172	001273		BNE	2\$:BRANCH IF NOT DONE
719	0000174	122712	000037	BITB	#37, (R2)	:CHECK FOR 5 CHAR
720	0000180	001351		BNE	GETLEN	:BAD INPUT, < 5
721	0000184	005202		INC	R2	:INC TO NEXT LINE GROUP
722	0000188	000004	017435	GETPAR:	TYPE,	:TYPE "PARITY (NO, ODD, EVEN):"
723	0000190	004737	016364	JSR	PC,READS	:READ INPUT FROM TTY
724	0000194	005737	016512	TST	INPUT	:CHECK FOR CR
725	0000198	001415		BEQ	3\$:BRANCH IF DEFAULT
726	0000200	122737	000116	CMPB	#116, INPUT	:CHECK FOR "N"
727	0000204	001411		BEQ	3\$:BRANCH IF "NO"
728	0000208	122737	000105	CMPB	#105, INPUT	:CHECK FOR "E"
729	0000212	001405		BEQ	3\$:BRANCH IF "EVEN"
730	0000216	122737	000117	CMPB	#117, INPUT	:CHECK FOR "O"
731	0000220	001355		BNE	GETPAR	:BRANCH IF NONE
732	0000224	150413		BISB	R4, (R3)	:SET THE ODD PARITY FLAG
733	0000228	005203		INC	R3	:UP DATE PARITY TABLE POINTER
734	0000232	032701	000017	BIT	#17,R1	:CHECK FOR NEXT UNIT
735	0000236	001303		BNE	TYPLIN	:BRANCH IF NOT
736	0000240	012703	001276	MOV	#PARITY,R3	:RESET PARITY TABLE POINTER
737	0000244	006304		ASL	R4	:FLAG TO NEXT UNIT
738	0000248	005200		INC	R0	:COUNT UNITS
739	0000252	020037	001234	CMP	R0,UNITS	:CHECK FOR LAST
740	0000256	001274		BNE	TYPLIN	:BRANCH IF MORE

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002562 012737 000340 000006
002570 005777 176414
002574 005077 176410
002600 005577 176404
002604 001405
002606 104000

002610 000403

002612 012601
002614 104001

002616 005726
002620 012737 000006 000004
002626 005037 000006
002632 104400

: TEST 1: TEST ABILITY TO REFERENCE CSR WITHOUT TRAPPING
: AND ABILITY TO CLR CSR.
: PROBABLE FAULTY LOGIC: M105; M7285 (D2-6) E29

TST1: MOV #1\$, @#4 ;SET UP TIME-OUT TRAP VECTOR
MOV #LEVEL7,@#6
TST @CSR ;REFERENCE CSR (READ)
CLR @CSR ;CLEAR CSR (WRITE)
ADC @CSR ;CHECK CSR (READ AND WRITE)
BEQ 2\$;BRANCH IF OK
HLT ;CSR NOT CLEARED

BR 2\$;SKIP ISR

1\$: MOV (SP)+,R1 ;SAVE RTI ADR FOR TYPING
HLT+1 ;CAN'T REFERENCE CSR!

2\$: TST (SP)+ ;FINISH CLEARING STACK
MOV #5,@#4
CLR @#5
SCOPE

: TEST 2: TEST THAT CSR BIT1 CAN BE SET AND CLEARED
: PROBABLE FAULTY LOGIC: M7285 (D2-2) E25,E7, (D2-4) E47,E64

002634 012777 000002 176346
002642 032777 000002 176340
002650 001001
002652 104000

002654 032777 177775 176326
002662 001401
002664 104000

002666 005077 176316
002672 032777 000002 176310
002700 001401
002702 104000

002704 104400

TST2: MOV #BIT1,@CSR ;SET BIT1
BIT #BIT1,@CSR ;CHECK THAT BIT1 IS SET
BNE .+4 ;BRANCH IF OK
HLT ;CSR BIT1 FAILED TO SET

BIT #177775,@CSR ;CHECK THAT NO OTHER BIT SET
BEQ .+4 ;BRANCH IF OK
HLT ;EXTRA BIT SET IN CSR

CLR @CSR ;CLEAR BIT1
BIT #BIT1,@CSR ;CHECK THAT BIT1 IS CLEARED
BEQ .+4 ;BRANCH IF OK
HLT ;CSR BIT1 FAILED TO CLEAR

SCOPE

: TEST 3: TEST THAT CSR BIT2 CAN BE SET AND CLEARED
: PROBABLE FAULTY LOGIC: M7285 (D2-2) E25,E7, (D2-4) E47,E64

002706 012777 000004 176274
002714 032777 000004 176266
002722 001001
002724 104000

TST3: MOV #BIT2,@CSR ;SET BIT2
BIT #BIT2,@CSR ;CHECK THAT BIT2 IS SET
BNE .+4 ;BRANCH IF OK
HLT ;CSR BIT2 FAILED TO SET

K02

MAINDEC-11-DZDJA-D
DZDJAD.P11

TST3: DJ11 LOGIC TESTS
TEST BIT2 OF CSR

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```

002726 032777 177773 176254 BIT #177773, QCSR ;CHECK THAT NO OTHER BIT SET
002734 001401 BEQ .+4 ;BRANCH IF OK
002736 104000 HLT ;EXTRA BIT SET IN CSR

002740 005077 176244 CLR QCSR ;CLEAR BIT2
002744 032777 000004 176236 BIT #BIT2, QCSR ;CHECK THAT BIT2 IS CLEARED
002752 001401 BEQ .+4 ;BRANCH IF OK
002754 104000 HLT ;CSR BIT2 FAILED TO CLEAR

002756 104400 SCOPE

```

```

:*****
:TEST 4: TEST THAT CSR BIT6 CAN BE SET AND CLEARED
:PROBABLE FAULTY LOGIC: M7285 (D2-2) E4,E18, (D2-4) E47,E64
:*****

```

```

002760 012777 000100 176222 TST4: MOV #BIT6, QCSR ;SET BIT6
002766 032777 000100 176214 BIT #BIT6, QCSR ;CHECK THAT BIT6 IS SET
002774 001001 BNE .+4 ;BRANCH IF OK
002776 104000 HLT ;CSR BIT6 FAILED TO SET

003000 032777 177677 176202 BIT #177677, QCSR ;CHECK THAT NO OTHER BIT SET
003006 001401 BEQ .+4 ;BRANCH IF OK
003010 104000 HLT ;EXTRA BIT SET IN CSR

003012 005077 176172 CLR QCSR ;CLEAR BIT6
003016 032777 000100 176164 BIT #BIT6, QCSR ;CHECK THAT BIT6 IS CLEARED
003024 001401 BEQ .+4 ;BRANCH IF OK
003026 104000 HLT ;CSR BIT6 FAILED TO CLEAR

003030 104400 SCOPE

```

```

:*****
:TEST 5: TEST THAT CSR BIT8 CAN BE SET AND CLEARED
:PROBABLE FAULTY LOGIC: M7285 (D2-2) E6,E18, (D2-4) E47,E31
:*****

```

```

003032 012777 000400 176150 TST5: MOV #BIT8, QCSR ;SET BIT8
003040 032777 000400 176142 BIT #BIT8, QCSR ;CHECK THAT BIT8 IS SET
003046 001001 BNE .+4 ;BRANCH IF OK
003050 104000 HLT ;CSR BIT8 FAILED TO SET

003052 032777 177377 176130 BIT #177377, QCSR ;CHECK THAT NO OTHER BIT SET
003060 001401 BEQ .+4 ;BRANCH IF OK
003062 104000 HLT ;EXTRA BIT SET IN CSR

003064 005077 176120 CLR QCSR ;CLEAR BIT8
003070 032777 000400 176112 BIT #BIT8, QCSR ;CHECK THAT BIT8 IS CLEARED
003076 001401 BEQ .+4 ;BRANCH IF OK
003100 104000 HLT ;CSR BIT8 FAILED TO CLEAR

003102 104400 SCOPE

```

```

:*****
:TEST 6: TEST THAT CSR BIT10 CAN BE SET AND CLEARED
:PROBABLE FAULTY LOGIC: M7285 (D2-2) E30,E24, (D2-4) E47,E31
:*****

```

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000037

```

TST6:  MOV    #BIT10, @CSR    ;SET BIT10
        BIT    #BIT10, @CSR    ;CHECK THAT BIT10 IS SET
        BNE   .+4             ;BRANCH IF OK
        HLT                               ;CSR BIT10 FAILED TO SET

        BIT    #175777, @CSR    ;CHECK THAT NO OTHER BIT SET
        BEQ   .+4             ;BRANCH IF OK
        HLT                               ;EXTRA BIT SET IN CSR

        CLR    @CSR            ;CLEAR BIT10
        BIT    #BIT10, @CSR    ;CHECK THAT BIT10 IS CLEARED
        BEQ   .+4             ;BRANCH IF OK
        HLT                               ;CSR BIT10 FAILED TO CLEAR

        SCOPE

```

TEST 7: TEST THAT CSR BIT12 CAN BE SET AND CLEARED
PROBABLE FAULTY LOGIC: M7285 (D2-2) E5, E1, (D2-4) E47, E31

```

TST7:  MOV    #BIT12, @CSR    ;SET BIT12
        BIT    #BIT12, @CSR    ;CHECK THAT BIT12 IS SET
        BNE   .+4             ;BRANCH IF OK
        HLT                               ;CSR BIT12 FAILED TO SET

        BIT    #167777, @CSR    ;CHECK THAT NO OTHER BIT SET
        BEQ   .+4             ;BRANCH IF OK
        HLT                               ;EXTRA BIT SET IN CSR

        CLR    @CSR            ;CLEAR BIT12
        BIT    #BIT12, @CSR    ;CHECK THAT BIT12 IS CLEARED
        BEQ   .+4             ;BRANCH IF OK
        HLT                               ;CSR BIT12 FAILED TO CLEAR

        SCOPE

```

TEST 10: TEST THAT CSR BIT14 CAN BE SET AND CLEARED
PROBABLE FAULTY LOGIC: M7285 (D2-2) E3, E1, (D2-4) E47, E31

```

TST10: MOV    #BIT14, @CSR    ;SET BIT14
        BIT    #BIT14, @CSR    ;CHECK THAT BIT14 IS SET
        BNE   .+4             ;BRANCH IF OK
        HLT                               ;CSR BIT14 FAILED TO SET

        BIT    #137777, @CSR    ;CHECK THAT NO OTHER BIT SET
        BEQ   .+4             ;BRANCH IF OK
        HLT                               ;EXTRA BIT SET IN CSR

        CLR    @CSR            ;CLEAR BIT14
        BIT    #BIT14, @CSR    ;CHECK THAT BIT14 IS CLEARED
        BEQ   .+4             ;BRANCH IF OK

```

003276 104000

HLT

;CSR BIT14 FAILED TO CLEAR

003300 104400

SCOPE

:TEST 11: TEST THAT RECEIVER ENABLE (BIT0 OF THE CSR) CAN BE SET
: AND CLEARED, AND THAT CLEAR MOS (BIT3) IS WRITE ONLY.
:PROBABLE FAULTY LOGIC: M7285 (D2-2) E26,E36,E7,E24, (D2-8) E17,E14,E15
:*****

003302 012777 000004 175700

TST11: MOV #BIT2, @CSR

;SET MAINTENANCE MODE (BIT2)

003310 005005

CLR R5

;SET UP COUNTER

003312 052777 000010 175670

1\$: BIS #BIT3, @CSR

;SET CLEAR MOS (BIT3)

003320 017701 175664

MOV @CSR, R1

;SAVE CSR

003324 032701 000010

BIT #BIT3, R1

;CHECK CLEAR MOS (BIT3)

003330 001401

BEQ .+4

;BRANCH IF OK

003332 104001

HLT+1

;CLEAR MOS (BIT3) SET (WRITE-ONLY)

003334 032701 000020

BIT #BIT4, R1

;CHECK CLEAR MOS FLAG

003340 001403

BEQ 2\$

;BRANCH IF CLEARED

003342 105305

DECB R5

;WAIT FOR MOS TO CLEAR

003344 001365

BNE 1\$

;BRANCH IF MORE TIME

003346 104001

HLT+1

;CLEAR MOS FLAG (BIT4) FAILED TO CLEAR

003350 022701 000004

2\$: CMP #BIT2, R1

;CHECK THAT ONLY MAINTENANCE BIT SET

003354 001401

BEQ .+4

;BRANCH IF OK

003356 104001

HLT+1

;CLEAR MOS CLEARED MAINTENANCE

003360 052777 000001 175622

BIS #BIT0, @CSR

;SET RECEIVER ENABLE

003366 017701 175616

MOV @CSR, R1

;SAVE CSR

003372 032777 000001 175610

BIT #BIT0, @CSR

;CHECK THAT RECEIVER ENABLE SET

003400 001001

BNE .+4

;BRANCH IF OK

003402 104001

HLT+1

;RECEIVER ENABLE FAILED TO SET

003404 022777 000005 175576

OMP #5, @CSR

;CHECK REST OF CSR

003412 001401

BEQ .+4

;BRANCH IF OK

003414 104001

HLT+1

;CSR ERROR

003416 042777 000001 175564

NOTE: BIC #BIT0, @CSR

;IF THE TTY MODULE IS BEING USED AND DONE (BIT7) IS SET,
; THE ERROR COULD BE DUE TO MAINTENANCE OR CLEAR MOS NOT WORKING.

003424 017701 175560

MOV @CSR, R1

;CLEAR RECEIVER ENABLE

003430 022777 000004 175552

OMP #BIT2, @CSR

;CHECK CSR

003436 001401

BEQ .+4

;BRANCH IF OK

003440 104001

HLT+1

;RECEIVER ENABLE DIDN'T CLEAR

003442 104400

SCOPE

;OR OTHER CSR BIT SET

003442 104400

SCOPE

;R1 = CONTENTS OF CSR

:TEST 12: TEST THAT CSR RESPONDS PROPERLY TO BYTE COMMANDS
:PROBABLE FAULTY LOGIC: M7285 (D2-4) E47
:*****

```

00000000 003444 012777 052506 175536 TST12:
00000000 003444 017701 175536
00000000 003444 022701 175526
00000000 003444 001401 052400
00000000 003470 104001
00000000 003472 012777 052506 175510
00000000 003500 005237 001210
00000000 003500 105077 175500
00000000 003510 005337 001210
00000000 003514 017701 175470
00000000 003524 022701 000106
00000000 003524 001401
00000000 003526 104001

```

```

MOV #052506, @CSR ;SET TEST NUMBER IN CSR
CLR @CSR ;CLR EVEN BYTE
MOV @CSR, R1 ;SAVE CSR
CMP #052400, R1 ;CHECK CSR
BEQ .+4 ;BRANCH IF OK
HLT+1 ;EVEN BYTE CLR FAILED ON CSR
;R1 = CONTENTS OF CSR

MOV #052506, @CSR ;SET TEST NUMBER IN CSR
INC CSR ;INC TO ODD BYTE
CLR @CSR ;CLR ODD BYTE
DEC CSR ;RESTORE TO EVEN
MOV @CSR, R1 ;SAVE CSR
CMP #000106, R1 ;CHECK CSR
BEQ .+4 ;BRANCH IF OK
HLT+1 ;ODD BYTE CLR FAILED ON CSR
;R1 = CONTENTS OF CSR

```

003530 104400

SCOPE

```

:*****
:TEST 13: TEST THAT THE BIS AND BIC INSTRUCTIONS SET AND CLEAR R/W
:BITS OF CSR
:PROBABLE FAULTY LOGIC: M7285 (D2-4) E47
:*****

```

```

10100000 003532 005077 175452
10200000 003536 017701 175446
10300000 003542 001401
10400000 003544 104001
10500000 003546 052777 052506 175434
10600000 003554 022777 052506 175426
10700000 003562 001401
10800000 003564 104000
10900000 003566 042777 052506 175414
11000000 003574 017701 175410
11100000 003600 001401
11200000 003602 104001

```

```

TST13: CLR @CSR ;CLEAR THE CSR
MOV @CSR, R1 ;CHECK AND SAVE CSR
BEQ .+4 ;BRANCH IF CLEARED OK
HLT+1 ;RESET FAILED TO CLR CSR

BIS #052506, @CSR ;SET ALL R/W BITS OF CSR
CMP #052506, @CSR ;CHECK THAT THEY GOT SET
BEQ .+4 ;BRANCH IF OK
HLT ;REG FAILED CMP

BIC #052506, @CSR ;CLEAR CSR
MOV @CSR, R1 ;CHECK AND SAVE CSR
BEQ .+4 ;BRANCH IF CLEARED OK
HLT+1 ;CLR FAILED TO CLR CSR

```

003604 104400

SCOPE

```

:*****
:TEST 14: TEST BITS OF TCR FOR READ/WRITE CAPABILITY
:PROBABLE FAULTY LOGIC: M7285 (D2-2) ALL, (D2-3) E8, E20, E21, E43, E41
:*****

```

```

10400000 003606 012777 177777 175400 TST14:
10410000 003614 017701 175374
10420000 003620 022701 177777
10430000 003624 001401
10440000 003626 104001
10450000 003630 005077 175360
10460000 003634 017701 175354
10470000 003640 001401

```

```

MOV #177777, @TCR ;SET ALL BITS OF TCR
MOV @TCR, R1 ;CHECK AND SAVE TCR
CMP #177777, R1 ;CHECK THAT ALL THE BITS ARE SET
BEQ .+4 ;BRANCH IF OK
HLT+1 ;BIT(S) OF TCR FAILED TO SET

CLR @TCR ;CLEAR TCR
MOV @TCR, R1 ;CHECK THAT IT CLEARED AND SAVE
BEQ .+4 ;BRANCH IF CLR

```


D03

TEST TRANSMIT READY

TEST NO	START	STOP	TEST
0000	00000000	00000000	TEST
0001	00000000	00000000	TEST
0002	00000000	00000000	TEST
0003	00000000	00000000	TEST
0004	00000000	00000000	TEST
0005	00000000	00000000	TEST
0006	00000000	00000000	TEST
0007	00000000	00000000	TEST
0008	00000000	00000000	TEST
0009	00000000	00000000	TEST
0010	00000000	00000000	TEST
0011	00000000	00000000	TEST
0012	00000000	00000000	TEST
0013	00000000	00000000	TEST
0014	00000000	00000000	TEST
0015	00000000	00000000	TEST
0016	00000000	00000000	TEST
0017	00000000	00000000	TEST
0018	00000000	00000000	TEST
0019	00000000	00000000	TEST
0020	00000000	00000000	TEST
0021	00000000	00000000	TEST
0022	00000000	00000000	TEST
0023	00000000	00000000	TEST
0024	00000000	00000000	TEST
0025	00000000	00000000	TEST
0026	00000000	00000000	TEST
0027	00000000	00000000	TEST
0028	00000000	00000000	TEST
0029	00000000	00000000	TEST
0030	00000000	00000000	TEST
0031	00000000	00000000	TEST
0032	00000000	00000000	TEST
0033	00000000	00000000	TEST
0034	00000000	00000000	TEST
0035	00000000	00000000	TEST
0036	00000000	00000000	TEST
0037	00000000	00000000	TEST
0038	00000000	00000000	TEST
0039	00000000	00000000	TEST
0040	00000000	00000000	TEST

```

00: BR 08 :SKIP LINE # CHECK ON ERROR
01: BS 08 :SET UP TIMER
02: TBUF 08 :SAVE LINE NUMBER
03: R1 :CHECK THAT THE XMTR STOPPED ON RIGHT LINE
04: R1 :BRANCH IF OK
05: R1 :WRONG LINE NUMBER APPEARED IN TBUF
06: R1 :R1=LINE # (SHOULD BE)
07: R1 :R2=LINE # (TBUF)
08: MOV 08 :CHECK AND SAVE XMTR READY
09: TBUF 08 :BRANCH IF OK
10: R1 :READING THE TBUF CLEARED XMTR READY
11: BS 08 :CLR XMTR CONTROL BIT, EACH LINE
12: BS 08 :CHECK AND SAVE XMTR READY
13: BS 08 :BRANCH IF OK
14: BS 08 :XMTR READY FAILED TO CLEAR WHEN
15: BS 08 :XMTR CONTROL FOR LINE .LINE WAS CLEARED
16: BS 08 :R1 = LINE #
17: BS 08 :R2 = CONTENTS OF CSR
18: INC 08 :INC LINE COUNTER TO NEXT LINE
19: BS 08 :SHIFT MARKER TO NEXT LINE
20: BS 08 :BRANCH IF NOT LAST LINE
21: BS 08 :SCORE

```

```

*****
TEST R1: TEST THAT MASTER TRANSMIT SCAN ENABLE (CSR BIT 8) ON A C
          DISABLES TRANSMITTER READY (CSR BIT 15)
          WHEN TCR BIT LINE 0 IS SET
PROBABLE FAULTY LOGIC: 0000 (00-6) 049,023,032,033
*****

```

```

00: BS 08 :CLEAR CONTROL STATUS
01: BS 08 :SET XMTR CONTROL BIT, LINE 0
02: BS 08 :GET TIMER FROM PREVIOUS TEST
03: BS 08 :CHECK AND SAVE XMTR READY
04: BS 08 :BRANCH IF NOT SET
05: BS 08 :XMTR READY SET WITHOUT
06: BS 08 :MASTER TRANS SCAN ENABLE
07: BS 08 :WAIT A WHILE
08: BS 08 :AND CHECK AGAIN
09: BS 08 :SET MASTER TRAN SCAN ENABLE
10: BS 08 :CHECK AND SAVE XMTR READY
11: BS 08 :TRAN READY NEVER CAME UP
12: BS 08 :TCR BIT WAS SET FIRST

```


TST23:

```

004554 013777 001226 174442
004552 012777 000004 174436
004570 005077 174420
004574 005077 174410
004600 042737 000340 177776
004606 104400

```

```

END23: MOV XMTLVL, @XMTVEC
MOV #IOT, @XMTLVL
CLR @TCR
CLR @CSR
BIC #340, @#PS

```

SCOPE

```

:*****
:TEST 24: TEST THAT INTERRUPT DOES NOT OCCUR AT LEVEL 5
:PROBABLE FAULTY LOGIC: M7821 WIRING, PROPER PRIORITY CHIP
:*****

```

```

004610 012777 004664 174406
004616 012777 000340 174402
004624 042737 000340 177776
004632 052737 000240 177776
004640 012777 040400 174342
004646 012777 000001 174340
004654 017701 174330
004660 100375
004662 000404

```

```

TST24: MOV #ISR24, @XMTVEC ;SET UP XMTR INTERRUPT VECTOR
MOV #340, @XMTLVL ;AT LEVEL 7
BIC #340, @#PS ;CLEAR PS LEVEL
BIS #240, @#PS ;SET PS TO LEVEL 5
MOV #040400, @CSR ;SET TRAN MASTER INT. ENABLE
MOV #BIT0, @TCR ;SET TRAN CONTROL BIT, LINE 0
IS: MOV @CSR, R1 ;WAIT
BPL IS ;OK, BRANCH IF NO INTERRUPT
BR END24

```

```

004664 104000
004666 012716 004674
004672 000002

```

```

ISR24: HLT ;SHOULDN'T HAVE INTERRUPTED AT LEVEL 5
MOV #END24, (SP) ;MOVE NEW RTI ADR ONTO STACK
RTI

```

```

004674 013777 001226 174322
004702 012777 000004 174316
004710 005077 174300
004714 005077 174270
004720 042737 000340 177776
004726 104400

```

```

END24: MOV XMTLVL, @XMTVEC
MOV #IOT, @XMTLVL
CLR @TCR
CLR @CSR
BIC #340, @#PS

```

SCOPE

```

:*****
:TEST 25: TEST THAT INTERRUPT OCCURS AT LEVEL 4
:PROBABLE FAULTY LOGIC: M7821 WIRING, PROPER PRIORITY CHIP
:*****

```

```

004730 012777 005006 174266
004736 012777 000340 174262
004744 042737 000340 177776
004752 052737 000200 177776
004760 012777 040400 174222
004766 012777 000001 174220
004774 017701 174210
005000 100375
005002 104000
005004 000403

```

```

TST25: MOV #ISR25, @XMTVEC ;SET UP XMTR INTERRUPT VECTOR
MOV #340, @XMTLVL ;AT LEVEL 7
BIC #340, @#PS ;CLEAR PS LEVEL
BIS #200, @#PS ;SET PS TO LEVEL 4
MOV #040400, @CSR ;SET TRAN MASTER INT. ENABLE
MOV #BIT0, @TCR ;SET TRAN CONTROL BIT, LINE 0
IS: MOV @CSR, R1 ;WAIT
BPL IS ;SHOULD HAVE INTERRUPTED AT LEVEL 4
HLT ;CONTINUE
BR END25

```

```

005006 012716 005014
005012 000002

```

```

ISR25: MOV #END25, (SP) ;MOVE NEW RTI ADR ONTO STACK
RTI

```


TST25:

```

13630 005014 013777 001226 174202
13631 005022 012777 000004 174176
13632 005030 005077 174160
13633 005034 005077 174150
13634 005040 042737 000340 177776
13635
13636 005046 104400

```

```

END25: MOV XMTLVL, @XMTVEC
        MOV #IOT, @XMTLVL
        CLR @TCR
        CLR @CSR
        BIC #340, @#PS

```

SCOPE

```

:*****
:TEST 26: TEST THAT INTERRUPT OCCURS AT LEVEL 3
:PROBABLE FAULTY LOGIC: M7821 WIRING, PROPER PRIORITY CHIP
:*****

```

```

13637 005050 012777 005126 174146
13638 005056 012777 000340 174142
13639 005064 042737 000340 177776
13640 005072 052737 000140 177776
13641 005100 012777 040400 174102
13642 005106 012777 000001 174100
13643 005114 017701 174070
13644 005120 100375
13645 005126 104000
13646 005134 000403

```

```

TST26: MOV #ISR26, @XMTVEC :SET UP XMTR INTERRUPT VECTOR
        MOV #340, @XMTLVL :AT LEVEL 7
        BIC #340, @#PS :CLEAR PS LEVEL
        BIS #140, @#PS :SET PS TO LEVEL 3
        MOV #040400, @CSR :SET TRAN MASTER INT. ENABLE
        MOV #BIT0, @TCR :SET TRAN CONTROL BIT, LINE 0
1$: MOV @CSR, R1 :WAIT
        BPL 1$
        HLT :SHOULD HAVE INTERRUPTED AT LEVEL 3
        BR END26 :CONTINUE

```

```

13647 005136 012716 005134
13648 005138 000002

```

```

ISR26: MOV #END26, (SP) :MOVE NEW RTI ADR ONTO STACK
        RTI

```

```

13649 005134 013777 001226 174062
13650 005142 012777 000004 174056
13651 005150 005077 174040
13652 005154 005077 174030
13653 005160 042737 000340 177776
13654
13655 005166 104400

```

```

END26: MOV XMTLVL, @XMTVEC
        MOV #IOT, @XMTLVL
        CLR @TCR
        CLR @CSR
        BIC #340, @#PS

```

SCOPE

```

:*****
:TEST 27: TEST THAT INTERRUPT OCCURS AT LEVEL 2
:PROBABLE FAULTY LOGIC: M7821 WIRING, PROPER PRIORITY CHIP
:*****

```

```

13656 005170 012777 005246 174026
13657 005176 012777 000340 174022
13658 005204 042737 000340 177776
13659 005212 052737 000100 177776
13660 005220 012777 040400 173762
13661 005226 012777 000001 173760
13662 005234 017701 173750
13663 005240 100375
13664 005242 104000
13665 005244 000403

```

```

TST27: MOV #ISR27, @XMTVEC :SET UP XMTR INTERRUPT VECTOR
        MOV #340, @XMTLVL :AT LEVEL 7
        BIC #340, @#PS :CLEAR PS LEVEL
        BIS #100, @#PS :SET PS TO LEVEL 2
        MOV #040400, @CSR :SET TRAN MASTER INT. ENABLE
        MOV #BIT0, @TCR :SET TRAN CONTROL BIT, LINE 0
1$: MOV @CSR, R1 :WAIT
        BPL 1$
        HLT :SHOULD HAVE INTERRUPTED AT LEVEL 2
        BR END27 :CONTINUE

```

```

13666 005246 012716 005254
13667 005252 000002

```

```

ISR27: MOV #END27, (SP) :MOVE NEW RTI ADR ONTO STACK
        RTI

```

```

1.4.0.000 005306 012777 001226 173742
1.4.0.001 005306 012777 000004 173736
1.4.0.002 005306 005077 173720
1.4.0.003 005306 005077 173710
1.4.0.004 005306 042737 000340 177776
1.4.0.005 005306 104400

```

```

END27: MOV XMTLVL, @XMTVEC
        MOV #IOT, @XMTLVL
        CLR @TCR
        CLR @CSR
        BIC #340, @#PS

```

SCOPE

```

:*****
:TEST 30: TEST THAT INTERRUPT OCCURS AT LEVEL 1
:PROBABLE FAULTY LOGIC: M7821 WIRING, PROPER PRIORITY CHIP
:*****

```

```

1.4.0.006 005310 012777 005366 173706
1.4.0.007 005316 012777 000340 173702
1.4.0.008 005324 042737 000340 177776
1.4.0.009 005332 052737 000040 177776
1.4.0.010 005340 012777 040400 173642
1.4.0.011 005346 012777 000001 173640
1.4.0.012 005354 017701 173630
1.4.0.013 005360 100375
1.4.0.014 005362 104000
1.4.0.015 005364 000403

```

```

TST30: MOV #ISR30, @XMTVEC ;SET UP XMTR INTERRUPT VECTOR
        MOV #340, @XMTLVL ;AT LEVEL 7
        BIC #340, @#PS ;CLEAR PS LEVEL
        BIS #040, @#PS ;SET PS TO LEVEL 1
        MOV #040400, @CSR ;SET TRAN MASTER INT. ENABLE
        MOV #BIT0, @TCR ;SET TRAN CONTROL BIT, LINE 0
1$: MOV @CSR, R1 ;WAIT
        BPL 1$
        HLT ;SHOULD HAVE INTERRUPTED AT LEVEL 1
        BR END30 ;CONTINUE

```

```

ISR30: MOV #END30, (SP) ;MOVE NEW RTI ADR ONTO STACK
        RTI

```

```

1.4.0.016 005374 013777 001226 173622
1.4.0.017 005402 012777 000004 173616
1.4.0.018 005410 005077 173600
1.4.0.019 005414 005077 173570
1.4.0.020 005420 042737 000340 177776
1.4.0.021 005426 104400

```

```

END30: MOV XMTLVL, @XMTVEC
        MOV #IOT, @XMTLVL
        CLR @TCR
        CLR @CSR
        BIC #340, @#PS

```

SCOPE

```

:*****
:TEST 31: TEST THAT INTERRUPT OCCURS AT LEVEL 0
:PROBABLE FAULTY LOGIC: M7821 WIRING, PROPER PRIORITY CHIP
:*****

```

```

1.4.0.022 005430 012777 005506 173566
1.4.0.023 005436 012777 000340 173562
1.4.0.024 005444 042737 000340 177776
1.4.0.025 005452 052737 000000 177776
1.4.0.026 005460 012777 040400 173522
1.4.0.027 005466 012777 000001 173520
1.4.0.028 005474 017701 173510
1.4.0.029 005500 100375
1.4.0.030 005502 104000
1.4.0.031 005504 000403

```

```

TST31: MOV #ISR31, @XMTVEC ;SET UP XMTR INTERRUPT VECTOR
        MOV #340, @XMTLVL ;AT LEVEL 7
        BIC #340, @#PS ;CLEAR PS LEVEL
        BIS #000, @#PS ;SET PS TO LEVEL 0
        MOV #040400, @CSR ;SET TRAN MASTER INT. ENABLE
        MOV #BIT0, @TCR ;SET TRAN CONTROL BIT, LINE 0
1$: MOV @CSR, R1 ;WAIT
        BPL 1$
        HLT ;SHOULD HAVE INTERRUPTED AT LEVEL 0
        BR END31 ;CONTINUE

```

```

ISR31: MOV #END31, (SP) ;MOVE NEW RTI ADR ONTO STACK
        RTI

```

```

1442 005514 013777 001226 173502
1443 005522 012777 000004 173476
1444 005530 005077 173460
1445 005534 005077 173450
1446 005540 042737 000340 177776
1447
1448 005546 104400
1449
1450 005550 005037 001302
1451 005554 012737 005562 015770

```

```

END31: MOV XMTLVL, @XMTVEC
MOV #IOT, @XMTLVL
CLR @TCR
CLR @CSR
BIC #340, @#PS

SCOPE

CLR TIMER ; INITIALIZE TIMER
MOV #.+6, LAD ; RESET LOOP ADDRESS

```

```

*****
TEST 32: TEST THAT LINE 0 CAN TRANSMIT AND
RECEIVE A CHARACTER. (377)
1$: CHECKS THAT DONE SETS IN REASONABLE TIME.
2$: CHECKS THAT CHAR PRESENT IS IN FI/FO
3$: CHECKS THAT NO ERRORS IN FI/FO
4$: CHECKS THAT RIGHT LINE # (0) IN FI/FO
5$: CHECKS FOR RIGHT CHARACTER LENGTH
6$: CHECKS THAT CORRECT DATA WAS RECEIVED
7$: CHECKS THAT CHARACTER PRESENT CLEARS
8$: CHECKS THAT DONE CLEARS
PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD D03 SERIES
*****

```

INITIALIZE
DEVICE"CSR"REGISTER

```

1452 005562 004737 015566
1453
1454
1455 005566 052777 000001 173420
1456 005574 017701 173410
1457 005600 100375
1458 005602 012777 000377 173406
1459 005610 005000
1460 005612 105305
1461 005614 001376
1462 005616 105777 173366
1463 005622 100405
1464 005624 005200
1465 005626 001371
1466 005630 017701 173354
1467 005634 104001
1468
1469 005636 050037 001302
1470 005642 017701 173344
1471 005646 100401
1472 005650 104001
1473
1474 005652 032701 070000
1475 005656 001401

```

```

TST32: JSR PC, @#INITD
SET:
:BIT2 = MAINTENANCE
:BIT3 = CLEAR MOS
:BIT8 = MASTER XMTR SCAN ENB

:WAIT FOR MOS TO CLEAR
SET:
:BIT0 = RECEIVER ENABLE

LOP32: BIS #BIT0, @TCR ; SET XMTR CONTROL BIT, LINE 0
MOV @CSR, R1 ; WAIT FOR XMTR READY
BPL LOP32
MOV #377, @TBUF ; SEND A RUBOUT
CLR R0 ; CLEAR COUNTER
1$: DECB R5 ; SHORT WAIT LOOP
BNE 1$
TSTB @CSR ; WAIT FOR DONE
BMI 2$ ; BRANCH WHEN DONE
INC R0 ; TIME COUNTER
BNE 1$ ; BRANCH IF NOT TIME-OUT
MOV @CSR, R1 ; SAVE CSR
HLT+1 ; DONE NEVER CAME UP
2$: BIS R0, TIMER ; R1 = CONTENTS OF CSR
MOV @RBUF, R1 ; SAVE TIMER
BMI .+4 ; READ THE FI/FO
HLT+1 ; BRANCH IF CHARACTER READY
3$: BIT #70000, R1 ; CHARACTER READY DIDN'T SET
BEQ .+4 ; R1 = CONTENTS OF RBUF
; CHECK FOR ERROR BITS
; BRANCH IF NONE

```

```

1498 005660 104001
1499
1500
1501
1502
1503 005662 010102
1504 005664 042702 170377
1505 005670 000302
1506 005672 122702 000000
1507 005676 001401
1508 005700 104001
1509
1510
1511 005702 117702 173400
1512 005706 130201
1513 005710 001401
1514 005712 104002
1515
1516
1517 005714 105102
1518 005716 120102
1519 005720 001401
1520 005722 104002
1521
1522
1523 005724 017701 173262
1524 005730 100001
1525 005732 104001
1526
1527 005734 017701 173250
1528 005740 022701 100405
1529 005744 001401
1530 005746 104001
1531
1532 005750 005077 173240
1533 005754 005077 173230
1534 005760 104400

```

```

HLT+1
4$: MOV R1, R2
SIC #170377, R2
SWAB R2
CMPB #0., R2
BEQ .+4
HLT+1
5$: MOVB @DJLEN, R2
BITB R2, R1
BEQ .+4
HLT+2
6$: COMB R2
CMPB R1, R2
BEQ .+4
HLT+2
7$: MOV @RBUF, R1
BPL .+4
HLT+1
8$: MOV @CSR, R1
CMP #100405, R1
BEQ .+4
HLT+1
CLR @TCR
CLR @CSR
SCOPE

```

```

:ERROR IN RECEIVED CHAR
:R1 = CONTENTS OF RBUF
:BIT14=UART OVERRUN
:BIT13=FRAMING ERROR
:BIT12=PARITY ERROR
:DUPLICATE DATA WORD
:MASK LINE#
:LINE # IN LOW BYTE
:CHECK LINE #
:BRANCH IF OK
:WRONG LINE # RECEIVED
:R1 = CONTENTS OF RBUF
:BITS8-11 = LINE #
:GET MASK OF CHARACTER
:CHECK CHAR LENGTH.
:BRANCH IF OK
:WRONG CHARACTER LENGTH
:R1=DATA FROM FI/FO
:R2=MASK (BITS SET NOT EXPECTED)
:REVERSE THE MASK
:CHECK THE ACTURAL DATA
:BRANCH IF OK
:WRONG CHAR LEN OR DATA ERROR
:R1=DATA FROM FI/FO (COMPLETE WORD)
:R2=DATA (LOW BYTE) EXPECTED
:READ FI/FO
:BRANCH IF CHAR PRESENT NOT SET
:CHARACTER PRESENT STAYED SET
:R1 = CONTENTS OF RBUF
:SAVE THE CSR
:CHECK THE CSR
:BRANCH IF OK
:DONE DIDN'T CLEAR OR OTHER CSR ERROR
:R1 = CONTENTS OF CSR
:CLEAR TCR
:CLEAR CSR

```

```

*****
:TEST 33: TEST THAT LINE 1 CAN TRANSMIT AND
RECEIVE A CHARACTER. (377)
:
: 1$: CHECKS THAT DONE SETS IN REASONABLE TIME.
: 2$: CHECKS THAT CHAR PRESENT IS IN FI/FO
: 3$: CHECKS THAT NO ERRORS IN FI/FO
: 4$: CHECKS THAT RIGHT LINE # (1) IN FI/FO
: 5$: CHECKS FOR RIGHT CHARACTER LENGTH
: 6$: CHECKS THAT CORRECT DATA WAS RECEIVED
: 7$: CHECKS THAT CHARACTER PRESENT CLEARS
: 8$: CHECKS THAT DONE CLEARS
:PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD 003 SERIES
*****

```

```

:
: INITIALIZE
: DEVICE"CSR"REGISTER
:
: SET:
TST33: JSR FC, @#INITD :BIT2 = MAINTENANCE

```

```

1553 005762 004737 015566

```



```

1610 006134 017701 173050
1611 006140 022701 100405
1612 006144 001401
1613 006146 104001
1614
1615 006150 005077 173040
1616 006154 005077 173030
1617 006160 104400

```

```

9$: MOV QCSR, R1 ;SAVE THE CSR
    CMP #100405,R1 ;CHECK THE CSR
    BEQ .+4 ;BRANCH IF OK
    HLT+1 ;DONE DIDN'T CLEAR OR OTHER CSR ERROR
                    ;R1 = CONTENTS OF CSR
1615 CLR QTCR ;CLEAR TCR
1616 CLR QCSR ;CLEAR CSR
1617 SCOPE

```

```

*****
:TEST 34: TEST THAT LINE 2 CAN TRANSMIT AND
          RECEIVE A CHARACTER. (377)

```

```

1$: CHECKS THAT DONE SETS IN REASONABLE TIME.
2$: CHECKS THAT CHAR PRESENT IS IN FI/FO
3$: CHECKS THAT NO ERRORS IN FI/FO
4$: CHECKS THAT RIGHT LINE # (2) IN FI/FO
5$: CHECKS FOR RIGHT CHARACTER LENGTH
6$: CHECKS THAT CORRECT DATA WAS RECEIVED
7$: CHECKS THAT CHARACTER PRESENT CLEARS
8$: CHECKS THAT DONE CLEARS

```

```

:PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD D03 SERIES
*****

```

```

:INITIALIZE
:DEVICE"CSR"REGISTER

```

```

1636 006162 004737 015566

```

```

TST34: JSR PC, Q#INITD ;SET:
                    ;BIT2 = MAINTENANCE
                    ;BIT3 = CLEAR MOS
                    ;BIT8 = MASTER XMTR SCAN ENB

```

```

:WAIT FOR MOS TO CLEAR

```

```

SET:
:BIT0 = RECEIVER ENABLE

```

```

1643 006166 052777 000004 173020

```

```

LOP34: BIS #BIT2, QTCR ;SET XMTR CONTROL BIT, LINE 2
        MOV QCSR, R1 ;WAIT FOR XMTR READY

```

```

1644 006174 017701 173010

```

```

1645 006200 100375

```

```

1646 006202 012777 000377 173006

```

```

        MOV #377, QTBUF ;SEND A RUBOUT
        CLR RD ;CLEAR COUNTER
1$: DECB R5 ;SHORT WAIT LOOP
    BNE 1$

```

```

1647 006210 005000

```

```

1648 006212 105305

```

```

1649 006214 001376

```

```

1650 006216 105777 172766

```

```

        TSTB QCSR ;WAIT FOR DONE
        BMI 2$ ;BRANCH WHEN DONE
        INC RD ;TIME COUNTER
        BNE 1$ ;BRANCH IF NOT TIME-OUT
        MOV QCSR, R1 ;SAVE CSR
        HLT+1 ;DONE NEVER CAME UP
                    ;R1 = CONTENTS OF CSR

```

```

1651 006222 100405

```

```

1652 006224 005200

```

```

1653 006226 001371

```

```

1654 006230 017701 172754

```

```

1655 006234 104001

```

```

1656

```

```

1657 006236 050037 001302

```

```

2$: BIS RD, TIMER ;SAVE TIMER
    MOV QRBUF, R1 ;READ THE FI/FO
    BMI .+4 ;BRANCH IF CHARACTER READY
    HLT+1 ;CHARACTER READY DIDN'T SET
                    ;R1 = CONTENTS OF RBUF

```

```

1658 006242 017701 172744

```

```

1659 006246 100401

```

```

1660 006250 104001

```

```

3$: BIT #70000, R1 ;CHECK FOR ERROR BITS
    BEQ .+4 ;BRANCH IF NONE
    HLT+1 ;ERROR IN RECEIVED CHAR
                    ;R1 = CONTENTS OF RBUF

```

```

1661

```

M03

MAINDEC-11-DZDJA-D
DZDJD.P11

DJ11 LOGIC TESTS
TST34: TEST ALL OF LINE 2 TRANSMIT AND RECEIVE LOGIC

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006262 010102
006264 042702
006270 000302
006272 122702
006276 001401
006300 104001

006302 117702
006306 130201
006310 001401
006312 104002

006314 105102
006316 120102
006320 001401
006322 104002

006324 017701
006330 100001
006332 104001

006334 017701
006340 022701
006344 001401
006346 104001

006350 005077
006354 005077
006360 104400

170377
000002
173000
172662
172650
172640
172630

4\$: MOV R1, R2
BIC #170377, R2
SWAB R2
CMPB #2, R2
BEQ .+4
HLT+1

5\$: MOVB @DJLEN, R2
BITB R2, R1
BEQ .+4
HLT+2

6\$: COMB R2
CMPB R1, R2
BEQ .+4
HLT+2

7\$: MOV @RBUF, R1
BPL .+4
HLT+1

8\$: MOV @CSR, R1
CMP #100405, R1
BEQ .+4
HLT+1

CLR @TCR
CLR @CSR
SCOPE

:BIT14=UART OVERRUN
:BIT13=FRAMING ERROR
:BIT12=PARITY ERROR
:DUPLICATE DATA WORD
:MASK LINE#
:LINE # IN LOW BYTE
:CHECK LINE #
:BRANCH IF OK
:WRONG LINE # RECEIVED
:R1 = CONTENTS OF RBUF
:BITS8-11 = LINE #
:GET MASK OF CHARACTER
:CHECK CHAR LENGTH.
:BRANCH IF OK
:WRONG CHARACTER LENGTH
:R1=DATA FROM FI/FO
:R2=MASK (BITS SET NOT EXPECTED)
:REVERSE THE MASK
:CHECK THE ACTURAL DATA
:BRANCH IF OK
:WRONG CHAR LEN OR DATA ERROR
:R1=DATA FROM FI/FO (COMPLETE WORD)
:R2=DATA (LOW BYTE) EXPECTED
:READ FI/FO
:BRANCH IF CHAR PRESENT NOT SET
:CHARACTER PRESENT STAYED SET
:R1 = CONTENTS OF RBUF
:SAVE THE CSR
:CHECK THE CSR
:BRANCH IF OK
:DONE DIDN'T CLEAR OR OTHER CSR ERROR
:R1 = CONTENTS OF CSR
:CLEAR TCR
:CLEAR CSR

:TEST 35: TEST THAT LINE 3 CAN TRANSMIT AND
RECEIVE A CHARACTER. (377)
:1\$: CHECKS THAT DONE SETS IN REASONABLE TIME.
:2\$: CHECKS THAT CHAR PRESENT IS IN FI/FO
:3\$: CHECKS THAT NO ERRORS IN FI/FO
:4\$: CHECKS THAT RIGHT LINE # (3) IN FI/FO
:5\$: CHECKS FOR RIGHT CHARACTER LENGTH
:6\$: CHECKS THAT CORRECT DATA WAS RECEIVED
:7\$: CHECKS THAT CHARACTER PRESENT CLEARS
:8\$: CHECKS THAT DONE CLEARS
:PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD D03 SERIES

: INITIALIZE
: DEVICE"CSR"REGISTER

006362 004737 015566

TST35: JSR PC, @#INITD

SET:
:BIT2 = MAINTENANCE
:BIT3 = CLEAR MOS
:BITS = MASTER XMTR SCAN ENB

TST35:

```

1722                                     ;WAIT FOR MOS TO CLEAR
1723                                     ;
1724                                     ;
1725                                     ;
1726                                     ;
1727 006366 052777 000010 172620     BIS      #BIT3,  @TOR    ;SET XMTR CONTROL BIT, LINE 3
1728 006374 017701 172610     LOP35:  MOV     @CSR,  R1    ;WAIT FOR XMTR READY
1729 006400 100375         SPL     LOP35
1730 006402 012777 000377 172606     MOV     #377,  @TBUF    ;SEND A RUBOUT
1731 006410 005000         CLR     RO          ;CLEAR COUNTER
1732 006412 105305     1$:    DECB   R5          ;SHORT WAIT LOOP
1733 006414 001376         BNE     1$
1734 006416 105777 172566     TSTB   @CSR        ;WAIT FOR DONE
1735 006422 100405         BMI     2$          ;BRANCH WHEN DONE
1736 006424 005200         INC     RO          ;TIME COUNTER
1737 006426 001371         BNE     1$          ;BRANCH IF NOT TIME-OUT
1738 006430 017701 172554     MOV     @CSR,   R1    ;SAVE CSR
1739 006434 104001         HLT+1   ;DONE NEVER CAME UP
1740 006436 050037 001302     2$:    BIS     RO,     TIMER ;SAVE TIMER
1741 006442 017701 172544     MOV     @RBUF, R1    ;READ THE FI/FO
1742 006446 100401         BMI     .+4         ;BRANCH IF CHARACTER READY
1743 006450 104001         HLT+1   ;CHARACTER READY DIDN'T SET
1744                                     ;
1745 006452 032701 070000     3$:    BIT     #70000, R1 ;CHECK FOR ERROR BITS
1746 006456 001401         BEQ     .+4         ;BRANCH IF NONE
1747 006460 104001         HLT+1   ;ERROR IN RECEIVED CHAR
1748                                     ;
1749                                     ;
1750                                     ;
1751                                     ;
1752 006462 010102     4$:    MOV     R1,     R2    ;R1 = CONTENTS OF RBUF
1753 006464 042702 170377     BIC     #170377, R2   ;BIT14=UART OVERRUN
1754 006470 000302         SWAB   R2          ;BIT13=FRAMING ERROR
1755 006472 122702 000003     CMPB   #3,     R2    ;BIT12=PARITY ERROR
1756 006476 001401         BEQ     .+4         ;DUPLICATE DATA WORD
1757 006500 104001         HLT+1   ;MASK LINE#
1758                                     ;
1759                                     ;
1760 006502 117702 172600     5$:    MOVB  @DJLEN, R2  ;LINE # IN LOW BYTE
1761 006506 130201         BITB   R2,     R1    ;CHECK LINE #
1762 006510 001401         BEQ     .+4         ;CHECK LINE #
1763 006512 104002         HLT+2   ;BRANCH IF OK
1764                                     ;
1765                                     ;
1766 006514 105102     6$:    COMB   R2          ;WRONG LINE # RECEIVED
1767 006516 120102     CMPB   R1,     R2    ;R1 = CONTENTS OF RBUF
1768 006520 001401         BEQ     .+4         ;BITS8-11 = LINE #
1769 006522 104002         HLT+2   ;GET MASK OF CHARACTER
1770                                     ;
1771                                     ;
1772 006524 017701 172462     7$:    MOV     @RBUF, R1  ;CHECK CHAR LENGTH.
1773 006530 100001         BPL     .+4         ;BRANCH IF OK
1774 006532 104001         HLT+1   ;WRONG CHARACTER LENGTH
1775                                     ;
1776 006534 017701 172450     8$:    MOV     @CSR,   R1  ;R1=DATA FROM FI/FO
1777 006540 022701 100405     CMP     #100405, R1  ;R2=DATA (LOW BYTE) EXPECTED

```


LOGIC TESTS TRANSMIT AND RECEIVE LOGIC

Vertical column of hex addresses and data values, including labels like 'DATA', 'COUNT', and 'ADDRESS'.

Main body of assembly code with comments, including instructions like 'LDR', 'STR', and 'JMP', and comments such as 'BRANCH IF OK' and 'DONE DIDN'T CLEAR OR OTHER CSR ERROR'.

Section titled 'INITIALIZE' containing initialization code and comments, including 'WAIT FOR MOS TO CLEAR' and 'RECEIVER ENABLE'.

E04

MAINDEC-11-D2DJA-D
D2DJA.D.P11

DJ11 LOGIC TESTS
TEST ALL OF LINE 5 TRANSMIT AND RECEIVE LOGIC

MAY11 27(732) 21-SEP-76 13:43 PAGE 41

TST37:

007156 001401
007156 104001
007156 005037
007156 005037
007156 104400

BEG .+4
HLT+1
CLS BTOR
CLR BCSR
SCOPE

:BRANCH IF OK
:DONE DIDN'T CLEAR OR OTHER CSR ERROR
:R1 = CONTENTS OF CSR
:CLEAR TOR
:CLEAR CSR

:TEST 40: TEST THAT LINE 5 CAN TRANSMIT AND
RECEIVE A CHARACTER. (377)

- 1\$: CHECKS THAT DONE SETS IN REASONABLE TIME.
- 2\$: CHECKS THAT CHAR PRESENT IS IN FI/FO
- 3\$: CHECKS THAT NO ERRORS IN FI/FO
- 4\$: CHECKS THAT RIGHT LINE # (6) IN FI/FO
- 5\$: CHECKS FOR RIGHT CHARACTER LENGTH
- 6\$: CHECKS THAT CORRECT DATA WAS RECEIVED
- 7\$: CHECKS THAT CHARACTER PRESENT CLEARS
- 8\$: CHECKS THAT DONE CLEARS

:PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD DOB SERIES

: INITIALIZE
DEVICE"CSR"REGISTER

007174 004737 016566

TST40: JSR PC, @#INITD

SET:
:BIT2 = MAINTENANCE
:BIT3 = CLEAR MOS
:BIT8 = MASTER XMTR SCAN ENB

:WAIT FOR MOS TO CLEAR

SET:
:BIT0 = RECEIVER ENABLE

007200 052777 000100 172006
007200 017701 171776

LOP40: BIS #BIT6, BTOR
MOV @BCSR, R1

:SET XMTR CONTROL BIT, LINE 6
:WAIT FOR XMTR READY

007200 0100375
007200 012777 000377 171774

BPL LOP40
MOV #377, @BBUF

:SEND A RUSOUT
:CLEAR COUNTER

007200 005000
007200 105305
007200 001376
007200 105777 171754

1\$: DECB RS
BNE 1\$
TSTB @BCSR

:SHORT WAIT LOOP
:WAIT FOR DONE
:BRANCH WHEN DONE

007200 100405
007200 005200
007200 001371

BMI RS
INC RD

:TIME COUNTER
:BRANCH IF NOT TIME-OUT

007200 001371
007200 017701 171742
007200 104001

BNE 1\$
MOV @BCSR, R1
HLT+1

:SAVE CSR
:DONE NEVER CAME UP
:R1 = CONTENTS OF CSR

007200 050037 001302
007200 017701 171732

2\$: BIS RD, TIMER
MOV @RBUF, R1

:SAVE TIMER
:READ THE FI/FO
:BRANCH IF CHARACTER READY

007200 100401
007200 104001

BMI .+4
HLT+1

:CHARACTER READY DIDN'T SET
:R1 = CONTENTS OF RBUF
:CHECK FOR ERROR BITS

007200 032701 070000
007200 001401
007200 104001

3\$: BIT #70000, R1
BEG .+4
HLT+1

:BRANCH IF NONE
:ERROR IN RECEIVED CHAR
:R1 = CONTENTS OF RBUF
:BIT14=UART OVERRUN
:BIT13=FRAMING ERROR

:R1 = CONTENTS OF CSR
:CLEAR TCR
:CLEAR CSR

CLR BCR
CLR BCSR
SCOPE
INC DJLEN
MOV #.+6, LAD

00000000 171416
00000000 171416
00000000 001306
00000000 007506 015770

TEST 42: TEST THAT LINE 8 CAN TRANSMIT AND
RECEIVE A CHARACTER. (377)
1\$: CHECKS THAT DONE SETS IN REASONABLE TIME.
2\$: CHECKS THAT CHAR PRESENT IS IN FI/FO
3\$: CHECKS THAT NO ERRORS IN FI/FO
4\$: CHECKS THAT RIGHT LINE # (8) IN FI/FO
5\$: CHECKS FOR RIGHT CHARACTER LENGTH
6\$: CHECKS THAT CORRECT DATA WAS RECEIVED
7\$: CHECKS THAT CHARACTER PRESENT CLEARS
8\$: CHECKS THAT DONE CLEARS

PROBABLE FAULTY LOGIC: M7295 (D2-7) ALL; M7279 ALL; UART CARD D03 SERIES

INITIALIZE
DEVICE"CSR"REGISTER

007506 004737 015556

TEST42: JSR PC, @#INITD SET:
:BIT2 = MAINTENANCE
:BIT3 = CLEAR MOS
:BIT8 = MASTER XMTR SCAN ENB

:WAIT FOR MOS TO CLEAR

SET:
:BIT0 = RECEIVER ENABLE

007512 052777 000400 171374
007520 017701 171364
007524 100375
007526 012777 000377 171362
007534 005000
007536 105305
007540 001376
007542 105777 171342
007546 100405
007550 005200
007552 001371
007554 017701 171330
007560 104001

LOP42: BIS #BIT8, BCR :SET XMTR CONTROL BIT, LINE 8
MOV BCSR, R1 :WAIT FOR XMTR READY
BFL LOP42
MOV #377, BBUF :SEND A RUBOUT
CLR RD :CLEAR COUNTER
1\$: DECB R5 :SHORT WAIT LOOP
BNE 1\$
TSTB BCSR :WAIT FOR DONE
BMI 2\$:BRANCH WHEN DONE
INC RD :TIME COUNTER
BNE 1\$:BRANCH IF NOT TIME-OUT
MOV BCSR, R1 :SAVE CSR
HLT+1 :DONE NEVER CAME UP
:R1 = CONTENTS OF CSR

007562 050037 001302
007566 017701 171320
007572 100401
007574 104001

2\$: BIS RD, TIMER :SAVE TIMER
MOV BBUF, R1 :READ THE FI/FO
BMI .+4 :BRANCH IF CHARACTER READY
HLT+1 :CHARACTER READY DIDN'T SET
:R1 = CONTENTS OF RBUF

007576 032701 070000
007702 001401
007704 104001

3\$: BIT #70000, R1 :CHECK FOR ERROR BITS
BEQ .+4 :BRANCH IF NONE
HLT+1 :ERROR IN RECEIVED CHAR
:R1 = CONTENTS OF RBUF
:BIT14=UART OVERRUN
:BIT13=FRAMING ERROR

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116099
116100

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0170 007706 010102 4$: MOV R1 R2 ;BIT12=PARITY ERROR
0171 007710 042702 170377 BIC #170377,R2 ;DUPLICATE DATA WORD
0172 007714 000302 SWAB R2 ;MASK LINE#
0173 007716 122702 000010 CMPB #8., R2 ;LINE # IN LOW BYTE
0174 007722 001401 BEQ .+4 ;CHECK LINE #
0175 007724 104001 HLT+1 ;BRANCH IF OK
;WRONG LINE # RECEIVED
;R1 = CONTENTS OF RBUF
;BITS9-11 = LINE #
0176 007726 117702 171354 5$: MOVB @DJLEN, R2 ;GET MASK OF CHARACTER
0177 007732 130201 BITB R2, R1 ;CHECK CHAR LENGTH.
0178 007734 001401 BEQ .+4 ;BRANCH IF OK
0179 007736 104002 HLT+2 ;WRONG CHARACTER LENGTH
;R1=DATA FROM FI/FO
;R2=MASK (BITS SET NOT EXPECTED)
0180 007740 105102 6$: COMB R2 ;REVERSE THE MASK
0181 007742 120102 CMPB R1, R2 ;CHECK THE ACTUAL DATA
0182 007744 001401 BEQ .+4 ;BRANCH IF OK
0183 007746 104002 HLT+2 ;WRONG CHAR LEN OR DATA ERROR
;R1=DATA FROM FI/FO (COMPLETE WORD)
;R2=DATA (LOW BYTE) EXPECTED
0184 007750 017701 171236 7$: MOV @RBUF, R1 ;READ FI/FO
0185 007754 100001 BPL .+4 ;BRANCH IF CHAR PRESENT NOT SET
0186 007756 104001 HLT+1 ;CHARACTER PRESENT STAYED SET
;R1 = CONTENTS OF RBUF
0187 007760 017701 171224 8$: MOV @CSR, R1 ;SAVE THE CSR
0188 007764 022701 100405 CMP #100405,R1 ;CHECK THE CSR
0189 007770 001401 BEQ .+4 ;BRANCH IF OK
0190 007772 104001 HLT+1 ;DONE DIDN'T CLEAR OR OTHER CSR ERROR
;R1 = CONTENTS OF CSR
0191 007774 005077 171214 CLR @TCR ;CLEAR TCR
0192 010000 005077 171204 CLR @CSR ;CLEAR CSR
0193 010004 104400 SCOPE

```

```

*****
:TEST 43: TEST THAT LINE 9 CAN TRANSMIT AND
: RECEIVE A CHARACTER. (377)
:
: 1$: CHECKS THAT DONE SETS IN REASONABLE TIME.
: 2$: CHECKS THAT CHAR PRESENT IS IN FI/FO
: 3$: CHECKS THAT NO ERRORS IN FI/FO
: 4$: CHECKS THAT RIGHT LINE # (9) IN FI/FO
: 5$: CHECKS FOR RIGHT CHARACTER LENGTH
: 6$: CHECKS THAT CORRECT DATA WAS RECEIVED
: 7$: CHECKS THAT CHARACTER PRESENT CLEARS
: 8$: CHECKS THAT DONE CLEARS
:PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD D03 SERIES
*****

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: INITIALIZE
: DEVICE"CSR"REGISTER
010006 004737 015566 TST43: JSR PC, @#INITD SET:
;BIT2 = MAINTENANCE
;BIT3 = CLEAR MOS
;BIT8 = MASTER XMTR SCAN ENB
:WAIT FOR MOS TO CLEAR SET:
:
```



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:BIT0 = RECEIVER ENABLE
:
:SET XMTR CONTROL BIT, LINE 9
:WAIT FOR XMTR READY
:
:SEND A RUBOUT
:CLEAR COUNTER
:SHORT WAIT LOOP
:
:WAIT FOR DONE
:BRANCH WHEN DONE
:TIME COUNTER
:BRANCH IF NOT TIME-OUT
:SAVE CSR
:DONE NEVER CAME UP
:R1 = CONTENTS OF CSR
:SAVE TIMER
:READ THE FI/FO
:BRANCH IF CHARACTER READY
:CHARACTER READY DIDN'T SET
:R1 = CONTENTS OF RBUF
:CHECK FOR ERROR BITS
:BRANCH IF NONE
:ERROR IN RECEIVED CHAR
:R1 = CONTENTS OF RBUF
:BIT14=UART OVERRUN
:BIT13=FRAMING ERROR
:BIT12=PARITY ERROR
:DUPLICATE DATA WORD
:MASK LINE#
:LINE # IN LOW BYTE
:CHECK LINE #
:BRANCH IF OK
:WRONG LINE # RECEIVED
:R1 = CONTENTS OF RBUF
:BITS8-11 = LINE #
:GET MASK OF CHARACTER
:CHECK CHAR LENGTH.
:BRANCH IF OK
:WRONG CHARACTER LENGTH
:R1=DATA FROM FI/FO
:R2=MASK (BITS SET NOT EXPECTED)
:REVERSE THE MASK
:CHECK THE ACTURAL DATA
:BRANCH IF OK
:WRONG CHAR LEN OR DATA ERROR
:R1=DATA FROM FI/FO (COMPLETE WORD)
:R2=DATA (LOW BYTE) EXPECTED
:READ FI/FO
:BRANCH IF CHAR PRESENT NOT SET
:CHARACTER PRESENT STAYED SET
:R1 = CONTENTS OF RBUF
:SAVE THE CSR
:CHECK THE CSR
:BRANCH IF OK
:DONE DIDN'T CLEAR OR OTHER CSR ERROR

```

010012	052777	001000	171174	:	BIS	#BIT9,	QTCR		
010020	017701	171164		LOP43:	MOV	QCSR,	R1		
010024	100375				BPL	LOP43			
010026	012777	000377	171162		MOV	#377,	QTBUF		
010034	005000				CLR	R0			
010036	105305			1\$:	DECB	R5			
010040	001376				SNE	1\$			
010042	105777	171142			TSTB	QCSR			
010046	100405				BMI	2\$			
010050	005200				INC	R0			
010052	001371				SNE	1\$			
010054	017701	171130			MOV	QCSR,	R1		
010060	104001				HLT+1				
010062	050037	001302		2\$:	BIS	R0,	TIMER		
010066	017701	171120			MOV	QRBUF,	R1		
010072	100401				BMI	+.4			
010074	104001				HLT+1				
010076	032701	070000		3\$:	BIT	#70000,	R1		
010102	001401				BEQ	+.4			
010104	104001				HLT+1				
010106	010102			4\$:	MOV	R1,	R2		
010110	042702	170377			BIC	#170377,	R2		
010114	000302				SWAB	R2			
010116	122702	000011			CMPB	#9.,	R2		
010122	001401				BEQ	+.4			
010124	104001				HLT+1				
010126	117702	171154		5\$:	MOVB	QDJLEN,	R2		
010132	130201				BITB	R2,	R1		
010134	001401				BEQ	+.4			
010136	104002				HLT+2				
010140	105102			6\$:	COMB	R2			
010142	120102				CMPB	R1,	R2		
010144	001401				BEQ	+.4			
010146	104002				HLT+2				
010150	017701	171036		7\$:	MOV	QRBUF,	R1		
010154	100001				BPL	+.4			
010156	104001				HLT+1				
010160	017701	171024		8\$:	MOV	QCSR,	R1		
010164	022701	100405			CMP	#100405,	R1		
010170	001401				BEQ	+.4			
010172	104001				HLT+1				

;R1 = CONTENTS OF CSR
;CLEAR TCR
;CLEAR CSR

010174 005077 171014
010200 005077 171004
010204 104400

CLR JTCR
CLR JCSR
SCOPE

TEST 44: TEST THAT LINE 10 CAN TRANSMIT AND
RECEIVE A CHARACTER. (377)
1\$: CHECKS THAT DONE SETS IN REASONABLE TIME.
2\$: CHECKS THAT CHAR PRESENT IS IN FI/FO
3\$: CHECKS THAT NO ERRORS IN FI/FO
4\$: CHECKS THAT RIGHT LINE # (10) IN FI/FO
5\$: CHECKS FOR RIGHT CHARACTER LENGTH
6\$: CHECKS THAT CORRECT DATA WAS RECEIVED
7\$: CHECKS THAT CHARACTER PRESENT CLEARS
8\$: CHECKS THAT DONE CLEARS
PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD DC3 SERIES

INITIALIZE
DEVICE"CSR"REGISTER

010206 004737 015566

TST44: JSR PC, J#INITD

SET:
;BIT2 = MAINTENANCE
;BIT3 = CLEAR MOS
;BITS = MASTER XMTR SCAN ENB

;WAIT FOR MOS TO CLEAR

SET:
;BIT0 = RECEIVER ENABLE

010212 052777 002000 170774
010220 017701 170764
010224 100375
010226 012777 000377 170762
010234 005000
010236 105305
010240 001376
010242 105777 170742
010246 100405
010250 005200
010252 001371
010254 017701 170730
010260 104001

LOP44: BIS #BIT10, JTCR
MOV JCSR, R1
BPL LOP44
MOV #377, JTBUF
CLR RD
1\$: DECB R5
BNE 1\$
TSTB JCSR
BMI 2\$
INC RD
BNE 1\$
MOV JCSR, R1
HLT+1

;SET XMTR CONTROL BIT, LINE 10
;WAIT FOR XMTR READY
;SEND A RUBOUT
;CLEAR COUNTER
;SHORT WAIT LOOP
;WAIT FOR DONE
;BRANCH WHEN DONE
;TIME COUNTER
;BRANCH IF NOT TIME-OUT
;SAVE CSR
;DONE NEVER CAME UP
;R1 = CONTENTS OF CSR

010262 050037 001302
010266 017701 170720
010272 100401
010274 104001

2\$: BIS RD, TIMER
MOV JRBUF, R1
BMI .+4
HLT+1

;SAVE TIMER
;READ THE FI/FO
;BRANCH IF CHARACTER READY
;CHARACTER READY DIDN'T SET
;R1 = CONTENTS OF RBUF

010276 032701 070000
010302 001401
010304 104001

3\$: BIT #70000, R1
BEQ .+4
HLT+1

;CHECK FOR ERROR BITS
;BRANCH IF NONE
;ERROR IN RECEIVED CHAR
;R1 = CONTENTS OF RBUF

010306 010102

4\$: MOV R1, R2

;BIT14=UART OVERRUN
;BIT13=FRAMING ERROR
;BIT12=PARITY ERROR
;DUPLICATE DATA WORD

```

2338 010310 042702 170377
2339 010314 000302
2340 010316 122702 000012
2341 010322 001401
2342 010324 104001
2343
2344
2345 010326 117702 170754
2346 010332 130201
2347 010334 001401
2348 010336 104002
2349
2350
2351 010340 105102
2352 010342 120102
2353 010344 001401
2354 010346 104002
2355
2356
2357 010350 017701 170636
2358 010354 100001
2359 010356 104001
2360
2361 010360 017701 170624
2362 010364 022701 100405
2363 010370 001401
2364 010372 104001
2365
2366 010374 005077 170614
2367 010400 005077 170604
2368 010404 104400
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2387 010406 004737 015566
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BIC #170377,R2
SWAB R2
CMPB #10., R2
BEQ .+4
HLT+1

5$: MOVB @DJLEN, R2
BITB R2, R1
BEQ .+4
HLT+2

6$: COMB R2
CMPB R1, R2
BEQ .+4
HLT+2

7$: MOV @RBUF, R1
BPL .+4
HLT+1

8$: MOV @CSR, R1
CMP #100405,R1
BEQ .+4
HLT+1

CLR @TCR
CLR @CSR
SCOPE

```

```

;MASK LINE#
;LINE # IN LOW BYTE
;CHECK LINE #
;BRANCH IF OK
;WRONG LINE # RECEIVED
;R1 = CONTENTS OF RBUF
;BITS8-11 = LINE #
;GET MASK OF CHARACTER
;CHECK CHAR LENGTH.
;BRANCH IF OK
;WRONG CHARACTER LENGTH
;R1=DATA FROM FI/FO
;R2=MASK (BITS SET NOT EXPECTED)
;REVERSE THE MASK
;CHECK THE ACTURAL DATA
;BRANCH IF OK
;WRONG CHAR LEN OR DATA ERROR
;R1=DATA FROM FI/FO (COMPLETE WORD)
;R2=DATA (LOW BYTE) EXPECTED
;READ FI/FO
;BRANCH IF CHAR PRESENT NOT SET
;CHARACTER PRESENT STAYED SET
;R1 = CONTENTS OF RBUF
;SAVE THE CSR
;CHECK THE CSR
;BRANCH IF OK
;DONE DIDN'T CLEAR OR OTHER CSR ERROR
;R1 = CONTENTS OF CSR
;CLEAR TCR
;CLEAR CSR

```

```

*****
:TEST 45: TEST THAT LINE 11 CAN TRANSMIT AND
: RECEIVE A CHARACTER. (C)
:
: 1$: CHECKS THAT DONE SETS IN REASONABLE TIME.
: 2$: CHECKS THAT CHAR PRESENT IS IN FI/FO
: 3$: CHECKS THAT NO ERRORS IN FI/FO
: 4$: CHECKS THAT RIGHT LINE # (11) IN FI/FO
: 5$: CHECKS FOR RIGHT CHARACTER LENGTH
: 6$: CHECKS THAT CORRECT DATA WAS RECEIVED
: 7$: CHECKS THAT CHARACTER PRESENT CLEARS
: 8$: CHECKS THAT DONE CLEARS
:PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD D03 SERIES
*****

```

```

:
: INITIALIZE
: DEVICE"CSR"REGISTER
:
: TST45: JSR PC, @#INITD SET:
: ;BIT2 = MAINTENANCE
: ;BIT3 = CLEAR MOS
: ;BIT8 = MASTER XMTR SCAN ENB
:
: ;WAIT FOR MOS TO CLEAR
:
: SET:
: ;BIT0 = RECEIVER ENABLE
:

```

TST45:

2394	010412	052777	004000	170574		BIS	#BIT11, @TCR		:SET XMTR CONTROL BIT, LINE 11
2395	010420	017701	170564		LOP45:	MOV	@CSR, R1		:WAIT FOR XMTR READY
2396	010424	100375				BPL	LOP45		
2397	010426	012777	000377	170562		MOV	#377, @TBUF		:SEND A RUBOUT
2398	010434	005000				CLR	R0		:CLEAR COUNTER
2399	010436	105305			1\$:	DECB	R5		:SHORT WAIT LOOP
2400	010440	001376				SNE	1\$		
2401	010442	105777	170542			TSTB	@CSR		:WAIT FOR DONE
2402	010446	100405				BMI	2\$:BRANCH WHEN DONE
2403	010450	005200				INC	R0		:TIME COUNTER
2404	010452	001371				BNE	1\$:BRANCH IF NOT TIME-OUT
2405	010454	017701	170530			MOV	@CSR, R1		:SAVE CSR
2406	010460	104001				HLT+1			:DONE NEVER CAME UP
2407									:R1 = CONTENTS OF CSR
2408	010462	050037	001302		2\$:	BIS	R0, TIMER		:SAVE TIMER
2409	010466	017701	170520			MOV	@RBUF, R1		:READ THE FI/FO
2410	010472	100401				BMI	+.4		:BRANCH IF CHARACTER READY
2411	010474	104001				HLT+1			:CHARACTER READY DIDN'T SET
2412									:R1 = CONTENTS OF RBUF
2413	010476	032701	070000		3\$:	BIT	#70000, R1		:CHECK FOR ERROR BITS
2414	010502	001401				BEQ	+.4		:BRANCH IF NONE
2415	010504	104001				HLT+1			:ERROR IN RECEIVED CHAR
2416									:R1 = CONTENTS OF RBUF
2417									:BIT14=UART OVERRUN
2418									:BIT13=FRAMING ERROR
2419									:BIT12=PARITY ERROR
2420	010506	010102			4\$:	MOV	R1, R2		:DUPLICATE DATA WORD
2421	010510	042702	170377			BIC	#170377, R2		:MASK LINE#
2422	010514	000302				SWAB	R2		:LINE # IN LOW BYTE
2423	010516	122702	000013			CMPB	#11., R2		:CHECK LINE #
2424	010522	001401				BEQ	+.4		:BRANCH IF OK
2425	010524	104001				HLT+1			:WRONG LINE # RECEIVED
2426									:R1 = CONTENTS OF RBUF
2427									:BITS8-11 = LINE #
2428	010526	117702	170554		5\$:	MOVB	@DJLEN, R2		:GET MASK OF CHARACTER
2429	010532	130201				BITB	R2, R1		:CHECK CHAR LENGTH.
2430	010534	001401				BEQ	+.4		:BRANCH IF OK
2431	010536	104002				HLT+2			:WRONG CHARACTER LENGTH
2432									:R1=DATA FROM FI/FO
2433									:R2=MASK (BITS SET NOT EXPECTED)
2434	010540	105102			6\$:	COMB	R2		:REVERSE THE MASK
2435	010542	120102				CMPB	R1, R2		:CHECK THE ACTURAL DATA
2436	010544	001401				BEQ	+.4		:BRANCH IF OK
2437	010546	104002				HLT+2			:WRONG CHAR LEN OR DATA ERROR
2438									:R1=DATA FROM FI/FO (COMPLETE WORD)
2439									:R2=DATA (LOW BYTE) EXPECTED
2440	010550	017701	170436		7\$:	MOV	@RBUF, R1		:READ FI/FO
2441	010554	100001				BPL	+.4		:BRANCH IF CHAR PRESENT NOT SET
2442	010556	104001				HLT+1			:CHARACTER PRESENT STAYED SET
2443									:R1 = CONTENTS OF RBUF
2444	010560	017701	170424		8\$:	MOV	@CSR, R1		:SAVE THE CSR
2445	010564	022701	100405			CMP	#100405, R1		:CHECK THE CSR
2446	010570	001401				BEQ	+.4		:BRANCH IF OK
2447	010572	104001				HLT+1			:DONE DIDN'T CLEAR OR OTHER CSR ERROR
2448									:R1 = CONTENTS OF CSR
2449	010574	005177	170414			CLR	@TCR		:CLEAR TCR

```

010600 005077 170404 CLR QCSR ;CLEAR CSR
010604 104400 SCOPE
010606 005237 001306 INC DJLEN
010612 012737 010620 015770 MOV #.+6, LAD

```

```

*****
TEST 46: TEST THAT LINE 12 CAN TRANSMIT AND
RECEIVE A CHARACTER. (377)
1$: CHECKS THAT DONE SETS IN REASONABLE TIME.
2$: CHECKS THAT CHAR PRESENT IS IN FI/FO
3$: CHECKS THAT NO ERRORS IN FI/FO
4$: CHECKS THAT RIGHT LINE # (12) IN FI/FO
5$: CHECKS FOR RIGHT CHARACTER LENGTH
6$: CHECKS THAT CORRECT DATA WAS RECEIVED
7$: CHECKS THAT CHARACTER PRESENT CLEARS
8$: CHECKS THAT DONE CLEARS
PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD DC3 SERIES
*****

```

INITIALIZE
DEVICE"CSR"REGISTER

```

010620 004737 015566 TST46: JSR PC, Q#INITD SET:
;BIT2 = MAINTENANCE
;BIT3 = CLEAR MOS
;BITS = MASTER XMTR SCAN ENB
;WAIT FOR MOS TO CLEAR SET:
;BIT0 = RECEIVER ENABLE
010624 052777 010000 170362 LOP46: BIS #BIT12, QTCR ;SET XMTR CONTROL BIT, LINE 12
010632 017701 170352 MOV QCSR, R1 ;WAIT FOR XMTR READY
010636 100375 BPL LOP46
010640 012777 000377 170350 MOV #377, QTBUF ;SEND A RUBOUT
010646 005000 CLR RO ;CLEAR COUNTER
1$: DECB R5 ;SHORT WAIT LOOP
010650 105305 BNE 1$
010652 001376 TSTB QCSR ;WAIT FOR DONE
010654 105777 170320 BMI 2$ ;BRANCH WHEN DONE
010662 005200 INC RO ;TIME COUNTER
010664 001371 BNE 1$ ;BRANCH IF NOT TIME-OUT
010666 017701 170316 MOV QCSR, R1 ;SAVE CSR
010672 104001 HLT+1 ;DONE NEVER CAME UP
;R1 = CONTENTS OF CSR
010674 050037 001302 2$: BIS RO, TIMER ;SAVE TIMER
010700 017701 170306 MOV QRBUF, R1 ;READ THE FI/FO
010704 100401 BMI .+4 ;BRANCH IF CHARACTER READY
010706 104001 HLT+1 ;CHARACTER READY DIDN'T SET
;R1 = CONTENTS OF RBUF
010710 032701 070000 3$: BIT #70000, R1 ;CHECK FOR ERROR BITS
010714 001401 BEQ .+4 ;BRANCH IF NONE
010716 104001 HLT+1 ;ERROR IN RECEIVED CHAR
;R1 = CONTENTS OF RBUF
;BIT14=UART OVERRUN
;BIT13=FRAMING ERROR
;BIT12=PARITY ERROR
010720 010102 4$: MOV R1, R2 ;DUPLICATE DATA WORD

```

TRANSMIT AND RECEIVE LOGIC

Vertical column of characters on the left side of the page, possibly a scan artifact or a specific data stream.

Main body of text containing hex addresses and binary data, likely representing register values or data points.

Vertical column of text on the right side, containing error messages and status indicators such as 'MASK LINE', 'CHECK LINE', and 'BRANCH OK'.

Block of text containing a series of asterisks and a list of error conditions, including 'PROBLEMS FAULTY LOGIC' and 'M7285 (02-7) ALL'.

Text block containing the label 'INITIALIZE REGISTER' and a list of bit definitions for the 'M7279' register, such as 'M7279 = MAINTENANCE' and 'M7279 = RECEIVER ENABLE'.

TEST LOGIC TESTS

TEST ALL OF LINE 13 TRANSMIT AND RECEIVE LOGIC

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ADDRESS	DATA	OPERATION	REGISTER	COMMENT
000000	170163	MOV R1, BITCR	R1	:SET XMTR CONTROL BIT, LINE 13
000001	170164	MOV R1, R1	R1	:WAIT FOR XMTR READY
000002	170165	MOV R1, STBUF	R1	:SEND A RUBOUT
000003		MOV R1, R1	R1	:CLEAR COUNTER
000004		MOV R1, R1	R1	:SHORT WAIT LOOP
000005	170160	MOV R1, R1	R1	:WAIT FOR DONE
000006		MOV R1, R1	R1	:BRANCH WHEN DONE
000007		MOV R1, R1	R1	:TIME COUNTER
000008	170116	MOV R1, R1	R1	:BRANCH IF NOT TIME-OUT
000009		MOV R1, R1	R1	:GIVE CSR
000010		MOV R1, R1	R1	:DONE NEVER CAME UP
000011		MOV R1, R1	R1	:X1 = CONTENTS OF CSR
000012		MOV R1, R1	R1	:GIVE TIMER
000013	170108	MOV R1, R1	R1	:READ THE FI/FO
000014		MOV R1, R1	R1	:BRANCH IF CHARACTER READY
000015		MOV R1, R1	R1	:CHARACTER READY DIDN'T SET
000016		MOV R1, R1	R1	:R1 = CONTENTS OF RBUF
000017		MOV R1, R1	R1	:CHECK FOR ERROR BITS
000018		MOV R1, R1	R1	:BRANCH IF NONE
000019		MOV R1, R1	R1	:ERROR IN RECEIVED CHAR
000020		MOV R1, R1	R1	:R1 = CONTENTS OF RBUF
000021		MOV R1, R1	R1	:BIT 14 = SHORT OVERRUN
000022		MOV R1, R1	R1	:BIT 15 = STARTING ERROR
000023		MOV R1, R1	R1	:BIT 16 = PARITY ERROR
000024		MOV R1, R1	R1	:DUPLICATE DATA WORD
000025	170377	MOV R1, R1	R1	:X1 = LINE * 8
000026		MOV R1, R1	R1	:X1 = X1 - 1
000027		MOV R1, R1	R1	:CHECK LINE *
000028		MOV R1, R1	R1	:BRANCH IF OK
000029		MOV R1, R1	R1	:X1 = LINE * RECEIVED
000030		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000031		MOV R1, R1	R1	:X1 = LINE *
000032		MOV R1, R1	R1	:GET MASK OF CHARACTER
000033		MOV R1, R1	R1	:CHECK CHAR LENGTH.
000034		MOV R1, R1	R1	:BRANCH IF OK
000035		MOV R1, R1	R1	:X1 = CHAR CHARACTER LENGTH
000036		MOV R1, R1	R1	:X1 = DATA FROM FI/FO
000037		MOV R1, R1	R1	:X1 = MASK (BITS SET NOT EXPECTED)
000038		MOV R1, R1	R1	:CHECK IF X1 IN MASK
000039		MOV R1, R1	R1	:CHECK THE ACTUAL DATA
000040		MOV R1, R1	R1	:BRANCH IF OK
000041		MOV R1, R1	R1	:X1 = LONG CHAR LEN OR DATA ERROR
000042		MOV R1, R1	R1	:X1 = DATA FROM FI/FO (COMPLETE WORD)
000043		MOV R1, R1	R1	:X1 = DATA (LOW BYTE) EXPECTED
000044		MOV R1, R1	R1	:READ FI/FO
000045		MOV R1, R1	R1	:BRANCH IF CHAR PRESENT NOT SET
000046		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000047		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000048		MOV R1, R1	R1	:CHECK THE CSR
000049		MOV R1, R1	R1	:BRANCH IF OK
000050		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000051		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000052		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000053		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000054		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000055		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000056		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000057		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000058		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000059		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000060		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000061		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000062		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000063		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000064		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000065		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000066		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000067		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000068		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000069		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000070		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000071		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000072		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000073		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000074		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000075		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000076		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000077		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000078		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000079		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000080		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000081		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000082		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000083		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000084		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000085		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000086		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000087		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000088		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000089		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000090		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000091		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000092		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000093		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000094		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000095		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000096		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000097		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000098		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000099		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF
000100		MOV R1, R1	R1	:X1 = CONTENTS OF RBUF

001110 0000000
001110 0000000
001110 0000000
167772

CLR DOBR :CLEAR CSR
SCOPE

```

*****
TEST 50: TEST THAT LINE 14 CAN TRANSMIT AND
          RECEIVE A CHARACTER. (377)
          CHECKS THAT DONE SETS IN REASONABLE TIME.
          CHECKS THAT CHAR PRESENT IS IN FI/FO
          CHECKS THAT NO ERRORS IN FI/FO
          CHECKS THAT RIGHT LINE # (14) IN FI/FO
          CHECKS FOR RIGHT CHARACTER LENGTH
          CHECKS THAT CORRECT DATA WAS RECEIVED
          CHECKS THAT CHARACTER PRESENT CLEARS
          CHECKS THAT DONE CLEARS
PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD DO3 SERIES
*****

```

011100 004707 015566

```

INITIALIZE
DEVICE "CSR" REGISTER
TESTED: JSR PC, @INITD SFT:
          :BITS = MAINTENANCE
          :BITS = CLEAR MOS
          :BITS = MASTER XMTR SCAN ENB

```

WAIT FOR MOS TO CLEAR

SFT: :BITS = RECEIVER_ENABLE

000000 000000 040000 167762
000000 000000 167750
000377 167750

```

LOF50: BIT #BIT14, @PCR :SET XMTR CONTROL BIT, LINE 14
        MOV @PCR, R1 :WAIT FOR XMTR READY
        CLR @PCR

```

000000 000000 167730

```

16: MOV @RBUF, @RBUF :SEND A RUBOUT
     CLR @COUNTER :CLEAR COUNTER
     JMP @SHORT_WAIT :SHORT WAIT LOOP

```

000000 000000 167716

```

16: MOV @CSR, @CSR :WAIT FOR DONE
     JMP @BRANCH_WHEN_DONE :BRANCH WHEN DONE
     INC @TIMER :TIME COUNTER
     JMP @BRANCH_IF_NOT_TIME_OUT :BRANCH IF NOT TIME-OUT
     MOV @CSR, R1 :SAVE CSR
     DONE_NEVER_CAME_UP :DONE NEVER CAME UP
     R1 = CONTENTS_OF_CSR :R1 = CONTENTS OF CSR
     SAVE_TIMER :SAVE TIMER

```

000000 000000 001300 28:
000000 000000 167708

```

28: MOV @RBUF, R1 :READ THE FI/FO
     INCR R1, #4 :BRANCH IF CHARACTER READY
     CHARACTER_READY_DIDNT_SET :CHARACTER READY DIDN'T SET
     R1 = CONTENTS_OF_RBUF :R1 = CONTENTS OF RBUF

```

000000 000000 070000 36:
000000 000000

```

36: BIT #70000, R1 :CHECK FOR ERROR BITS
     INCR R1, #4 :BRANCH IF NONE
     ERROR_IN_RECEIVED_CHAR :ERROR IN RECEIVED CHAR
     R1 = CONTENTS_OF_RBUF :R1 = CONTENTS OF RBUF

```

000000 000000 170377 48:
000000 000000

```

48: MOV R1, R2 :DUPLICATE DATA WORD
     BIC #170377, R2 :MASK LINE#
     SWAB R2 :LINE # IN LOW BYTE

```


0111330 102702
0111334 001401
0111336 104001

0111340 117702
0111344 100001
0111348 104001
0111352 104001

0111356 104001
0111360 104001
0111364 104001
0111368 104001
0111372 104001
0111376 104001
0111380 104001
0111384 104001
0111388 104001
0111392 104001
0111396 104001
0111400 104001

000016

167742

167864

167812

167860

167862

CMPB #14., R2
BEQ .+4
HLT+1

58: MOVB DDJLEN, R2
BITB R2, R1
BFO .+4
HLT+2

68: COMB R2
CMPB R1, R2
BFO .+4
HLT+2

78: MOV RBUF, R1
BPL .+4
HLT+1

88: MOV RCSR, R1
CMP #100405, R1
BFO .+4
HLT+1

CLR RCSR
CLR RCSR
SCOPE

:CHECK LINE #
:BRANCH IF OK
:WRONG LINE # RECEIVED
:R1 = CONTENTS OF RBUF
:BITS8-11 = LINE #
:GET MASK OF CHARACTER
:CHECK CHAR LENGTH.
:BRANCH IF OK
:WRONG CHARACTER LENGTH
:R1=DATA FROM FI/FO
:R2=MASK (BITS SET NOT EXPECTED)
:REVERSE THE MASK
:CHECK THE ACTUAL DATA
:BRANCH IF OK
:WRONG CHAR LEN OR DATA ERROR
:R1=DATA FROM FI/FO (COMPLETE WORD)
:R2=DATA (LOW BYTE) EXPECTED
:READ FI/FO
:BRANCH IF CHAR PRESENT NOT SET
:CHARACTER PRESENT STAYED SET
:R1 = CONTENTS OF RBUF
:SAVE THE CSR
:CHECK THE CSR
:BRANCH IF OK
:DONE DIDN'T CLEAR OR OTHER CSR ERROR
:R1 = CONTENTS OF CSR
:CLEAR RCSR
:CLEAR CSR

:TEST 51: TEST THAT LINE 15 CAN TRANSMIT AND
RECEIVE A CHARACTER. (377)
1: CHECKS THAT DONE SETS IN REASONABLE TIME.
2: CHECKS THAT CHAR PRESENT IS IN FI/FO
3: CHECKS THAT NO ERRORS IN FI/FO
4: CHECKS THAT RIGHT LINE # (15) IN FI/FO
5: CHECKS FOR RIGHT CHARACTER LENGTH
6: CHECKS THAT CORRECT DATA WAS RECEIVED
7: CHECKS THAT CHARACTER PRESENT CLEARS
8: CHECKS THAT DONE CLEARS
:PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD 003 SERIES

011420 004737 015566

011424 052777 100000
011430 017701 167862

INITIALIZE
DEVICE"CSR"REGISTER
TEST1: JSR PC, @INITD

:WAIT FOR MOS TO CLEAR

LOP51: BIS #BIT15, RCSR
MOV RCSR, R1

SET:
:BIT2 = MAINTENANCE
:BIT3 = CLEAR MOS
:BIT8 = MASTER XMTR SCAN ENB

SET:
:BIT0 = RECEIVER ENABLE

:SET XMTR CONTROL BIT, LINE 15
:WAIT FOR XMTR READY

ADDRESS	OPCODE	OPERAND	TEST	DESCRIPTION
000377	BPL	LOP51	167550	: SEND A RUBOUT
	MOV	#377, R0		: CLEAR COUNTER
	CLR	R0		: SHORT WAIT LOOP
	DFCB	R5	15:	
	BNE	R5		
167530	TSTB	QCSR		: WAIT FOR DONE
	BMI	R5		: BRANCH WHEN DONE
	INC	R0		: TIME COUNTER
	SNE	R5		: BRANCH IF NOT TIME-OUT
167516	MOV	QCSR, R1		: SAVE CSR
	HLT+1			: DONE NEVER CAME UP
				: R1 = CONTENTS OF CSR
	BIS	R0, TIMER	25:	: SAVE TIMER
	MOV	QRBUF, R1		: READ THE FI/FO
	BMI	.+4		: BRANCH IF CHARACTER READY
	HLT+1			: CHARACTER READY DIDN'T SET
				: R1 = CONTENTS OF RBUF
	BIT	#70000, R1	35:	: CHECK FOR ERROR BITS
	BEQ	.+4		: BRANCH IF NONE
	HLT+1			: ERROR IN RECEIVED CHAR
				: R1 = CONTENTS OF RBUF
				: BIT14=UART OVERRUN
				: BIT13=FRAMING ERROR
				: BIT12=PARITY ERROR
	MOV	R1, R2	45:	: DUPLICATE DATA WORD
	BIC	#170377, R2		: MASK LINE #
	SWAB	R2		: LINE # IN LOW BYTE
	CMPS	#15., R2		: CHECK LINE #
	BEQ	.+4		: BRANCH IF OK
	HLT+1			: WRONG LINE # RECEIVED
				: R1 = CONTENTS OF RBUF
				: BITS8-11 = LINE #
	MOVB	QDJLEN, R2	55:	: GET MASK OF CHARACTER
	BITB	R2, R1		: CHECK CHAR LENGTH.
	BEQ	.+4		: BRANCH IF OK
	HLT+2			: WRONG CHARACTER LENGTH
				: R1=DATA FROM FI/FO
				: R2=MASK (BITS SET NOT EXPECTED)
	COMB	R2	65:	: REVERSE THE MASK
	CMPS	R1, R2		: CHECK THE ACTUAL DATA
	BEQ	.+4		: BRANCH IF OK
	HLT+2			: WRONG CHAR LEN OR DATA ERROR
				: R1=DATA FROM FI/FO (COMPLETE WORD)
				: R2=DATA (LOW BYTE) EXPECTED
	MOV	QRBUF, R1	75:	: READ FI/FO
	BPL	.+4		: BRANCH IF CHAR PRESENT NOT SET
	HLT+1			: CHARACTER PRESENT STAYED SET
				: R1 = CONTENTS OF RBUF
	MOV	QCSR, R1	85:	: SAVE THE CSR
	CMP	#100405, R1		: CHECK THE CSR
	BEQ	.+4		: BRANCH IF OK
	HLT+1			: DONE DIDN'T CLEAR OR OTHER CSR ERROR
				: R1 = CONTENTS OF CSR
	CLR	QTCR		: CLEAR TCR
	CLR	QCSR		: CLEAR CSR
	SCOPE			

```

011620 162737 000003 001306 SUB #3, DJLEN
011621 005237 001302 INC TIMER :WORSE CASE TIME, ONE CHARACTER
011622 012700 001302 MOV TIMER, R0 :DUP TIMER
011623 006200 RO /2
011624 006200 RO /4
011625 005237 RO +1
011626 006137 001302 ROL TIMER :TIMER * 2
011627 000000 001302 ADD R0, TIMER :2.25 TIMES ONE CHARACTER TIME
011628 012737 011622 MOV #.46, LAD :RESET LOOP ADDRESS

```

```

*****
:TEST 52: TEST THAT CHARACTER PRESENT (BIT15) OF RBUF
: IS CLEARED (BY CLEAR MOS).
:PROBABLE FAULTY LOGIC: M7285 (D2-9) E17,E14,E15; M7279; M7280
*****

```

INITIALIZE

```

011629 004737 015556 :TEST 52: JSR FC, @INITD
:SET:
:BIT2 = MAINTENANCE
:BIT3 = CLEAR MOS
:BIT4 = TRANS SCAN ENABLE
:WAIT FOR BIT4 = MOS CLEAR
:SET:
:BIT0 = RECEIVER ENABLE
011630 012777 000001 167320 MOV #BIT0, @CSR :TRANS CONTROL LINED
011631 012704 000004 MOV #4, R4 :SET UP COUNTER
011632 017701 167304 18: MOV @CSR, R1 :WAIT FOR TRANS READY
011633 100278 BPL 18
011634 010277 167304 MOV R4, @TBUF :TRANSMIT COUNT
011635 000204 DFC R4 :COUNT DOWN
011636 001278 BNE 18
011637 105777 167266 28: TSTB @CSR :MAKE SURE DONE IS SET
011638 100278 BPL 28
011639 000277 000010 167286 38: BIT #BIT3, @CSR :CLEAR MOS
011640 000277 000020 167280 38: BIT #BIT4, @CSR :WAIT FOR CLAMOS TO FINISH
011641 001278 BNE 38
011642 017701 167244 MOV @RBUF, R1 :CHECK RBUF AND SAVE
011643 100001 BPL .+4
011644 104001 HLT +1
011645 001700 167230 MOV @CSR, R1 :SAVE CSR
011646 002701 100405 48: CMP #100405, R1 :CHECK CSR
011647 001401 BPL .+4 :BRANCH IF OK
011648 104001 HLT +1 :CSR ERROR, POSSIBILITIES:
: (1) DONE DIDN'T CLEAR
: (2) TRANSMITTER UART DIDN'T CLR.
: R1=CONTENTS OF CSR
011649 012700 001302 48: MOV TIMER, R0 :SET UP TIMER
011650 000000 000000 DFC R0 :SHORT WAIT LOOP
011651 001278 BNE 48

```

H05

MAINTENANCE - 11-0200A-D
020000.000000

LOGIC TESTS
TEST CASE MOS

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012000 017701 167206 MOV @CSR,R1 :SAVE CSR
012001 100375 BPL R1 :CHECK FOR DONE
012002 104001 HLT+1 :BRANCH IF OK
012003 005200 :DONE CAME UP!
012004 001367 :MOS MUST NOT HAVE CLEARED
012005 001367 :TIMER COUNT
012006 002701 100406 CMP #100405,R1 :CHECK CSR
012007 001401 BFC .+4 :BRANCH IF OK
012008 104001 HLT+1 :CSR ERROR
012009 017701 167162 MOV @RBUF,R1 :CHECK RBUF
012010 100001 BPL .+4 :BRANCH IF OK
012011 104001 HLT+1 :RBUF NOT EMPTY!
012012 005077 167154 CLR @TOR
012013 005077 167144 CLR @CSR
012014 104400 SCOPE

```

```

*****
:TEST 53: TEST THAT TRANSMITTER READY CLEARS WHEN TBUF IS LOADED
:NOTE: DUE TO THE DOUBLE BUFFERING BY THE UART, TWO CHARACTERS
: MUST BE LOADED TO INSURE SEEING TRANSMITTER READY CLEAR
:PROBABLE FAULTY LOGIC: M7285 (D2-6) E39, E23, E49
*****

```

```

: INITIALIZE
: DEVICE"CSR"REGISTER
TST53: JSR PC, @#INITO SET:
:BIT0 = MAINTENANCE
:BIT1 = CLEAR MOS
:BIT2 = MASTER XMTR SCAN ENB

```

```

:WAIT FOR MOS TO CLEAR
:
: SET:
:BIT0 = RECEIVER ENABLE

```

```

012052 052777 000001 167134 18: BIS #BIT0, @TOR :TRANS CONTROL, LINE 0
012060 017701 167124 MOV @CSR, R1 :WAIT FOR XMTR READY
012064 100375 BPL R1
012066 012777 000001 167122 28: MOV #1, @TBUF :TRANSMIT A 1
012074 017701 167110 MOV @CSR, R1 :WAIT FOR XMTR READY
012100 100375 BPL R1
012102 012777 000002 167106 MOV #2, @TBUF :TRANSMIT A 2
012110 017701 MOV @CSR, R1 :CHECK FOR XMTR READY
012114 100001 BPL .+4 :BRANCH IF XMTR READY CLEARED
012116 104001 HLT+1 :TRANSMITTER READY FAILED TO CLEAR
:R1 = CONTENTS OF CSR
012120 013700 001302 38: MOV TIMER, R0 :SET UP TIMER
012124 105305 DECB R5 :SHORT WAIT LOOP
012126 001376 BNE 38
012130 017701 167054 MOV @CSR, R1 :SAVE CSR FOR THE RECORD
012134 000400 BR .+2 :NOP FOR TIMING

```

MAINDEC-11-DZDJA-D
DZDJD.P11 TST53:

DJ11 LOGIC TESTS
TEST TRANSMIT READY

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```

00000000 012136 005300 DEC R0 :TIMER COUNT
00000000 012140 001371 BNE 3$ :BRANCH IF MORE TIME
00000000 012142 022701 100605 CMP #100605,R1 :CHECK CSR
00000000 012146 001401 BEQ .+4 :BRANCH IF OK
00000000 012150 104001 HLT+1 :DONE DIDN'T SET OR OTHER CSR ERROR
00000000 012152 017701 167034 MOV @RBUF, R1 :R1 = CONTENTS OF CSR
00000000 012156 100401 BMI .+4 :CHECK RBUF FOR CHAR PRESENT
00000000 012160 104001 HLT+1 :BRANCH IF CHAR PRESENT
00000000 012162 022701 100001 CMP #100001,R1 :CHAR PRESENT MISSING
00000000 012166 001401 BEQ .+4 :R1 = CONTENTS OF RBUF
00000000 012170 104001 HLT+1 :CHECK THE DATA
00000000 012172 017701 167014 MOV @RBUF, R1 :BRANCH IF OK
00000000 012176 100401 BMI .+4 :RECEIVER ERROR
00000000 012200 104001 HLT+1 :R1 = CNTENTS OF RBUF
00000000 012202 022701 100002 CMP #100002,R1 :CHECK RBUF FOR SECOND CHAR
00000000 012206 001401 BEQ .+4 :BRANCH IF CHAR PRESENT
00000000 012210 104001 HLT+1 :CHAR PRESENT MISSING
00000000 012212 017701 166774 MOV @RBUF, R1 :R1 = CONTENTS OF RBUF
00000000 012216 100001 BPL .+4 :CHECK FOR NO MORE CHARACTERS
00000000 012220 104001 HLT+1 :BRANCH IF CHAR PRESENT CLEARED
00000000 012222 017701 166762 MOV @CSR, R1 :CHAR PRESENT NOT CLEAR!
00000000 012226 022701 100405 CMP #100405,R1 :R1 = CONTENTS OF RBUF
00000000 012230 001401 BEQ .+4 :SAVE CSR
00000000 012234 104001 HLT+1 :CHECK CSR
00000000 012236 005077 166752 CLR @TCR :BRANCH IF OK
00000000 012240 005077 166742 CLR @CSR :CSR ERROR
00000000 012246 104400 SCOPE :R1 = CONTENTS OF CSR
: CLEAR TCR
: CLEAR CSR

```

```

:*****
:TEST 54: TEST THAT RECEIVER ENABLE ON A 0 INHIBITS DONE
: AND CHARACTER PRESENT.
:PROBABLE FAULTY LOGIC: M7285 (D2-7) E32, E15
:*****

```

```

012250 012777 000414 166732 TST54: MOV #414, @CSR :BIT2 = MAINTENANCE
012256 032777 000020 166724 10$: BIT #BIT4, @CSR :BIT3 = CLEAR MOS
012264 001374 BNE 10$ :BIT0 = MASTER TRAN SCAN ENB
012266 052777 000000 166720 1$: BIS #BIT0, @TCR :WAIT FOR MOS TO CLEAR
012274 017701 166710 1$: MOV @CSR, R1 :SET XMTR CONTROL BIT, LINED
012300 100375 BPL 1$ :WAIT FOR XMTR READY
012302 012777 000252 166706 2$: MOV #252, @TBUF :SEND AN "*"
012310 013700 001302 2$: MOV TIMER, R0 :SET UP TIMER
012314 105305 2$: DECB R5 :SHORT WAIT LOOP
012316 001376 BNE 2$
012320 017701 166664 MOV @CSR, R1 :SAVE CSR FOR TYPING

```

```

2954 012324 105701 TSTB R1 ;CHECK FOR DONE
2955 012326 100002 BPL 3$ ;BRANCH IF NOT SET
2956 012330 104001 HLT+1 ;DONE SET WHEN RCV ENB CLR
2957 ;R1=CONTENTS OF CSR
2958 012332 000402 BR 4$
2959 012334 005300 3$: DEC RO ;TIMER COUNT
2960 012336 001366 BNE 2$ ;BRANCH IF MORE TIMER
2961
2962 012340 017701 166646 4$: MOV @RBUF, R1 ;CHECK AND SAVE FI/FO
2963 012344 100001 BPL .+4 ;BRANCH IF OK
2964 012346 104001 HLT+1 ;CHARACTER PRESENT IN FI/FO
2965 ;R1=DATA FROM FI/FO
2966 012350 005277 166634 5$: INC @CSR ;SET RECEIVER ENABLE
2967 012354 017701 166630 MOV @CSR, R1 ;SAVE CSR
2968 012360 105701 TSTB R1 ;CHECK FOR DONE
2969 012362 100403 BMI 6$ ;BRANCH IF OK
2970 012364 105300 DECB RO ;SHORT TIMER
2971 012366 001372 BNE 5$
2972 012370 104001 HLT+1 ;DONE DIDN'T COME UP WHEN RECEIVER ENABLED
2973 ;UART SHOULD HAVE HELD A CHARACTER
2974 ;R1 = CONTENTS OF CSR
2975 012372 017701 166614 6$: MOV @RBUF, R1 ;CHECK FOR CHARACTER PRESENT
2976 012376 100401 BMI .+4 ;BRANCH IF OK
2977 012400 104001 HLT+1 ;CHARACTER PRESENT MISSING
2978 ;R1 = CONTENTS OF RBUF
2979 012402 005077 166606 CLR @TCR ;CLR TRANS CONTROL REG
2980
2981 012406 104400 SCOPE

```

```

:*****
:TEST 55: TEST THAT HALF DUPLEX (BIT1) DISABLES THE RECEIVER UARTS.
:PROBABLE FAULTY LOGIC: M7285 (D2-4) E32, E17, E22, (D2-2) E5, E1
:*****

```

```

2982 012410 004737 015556 TST55: JSR PC, @#INITC ;INITIALIZE
2983 ;BIT1 = HALF DUPLEX
2984 ;BIT2 = MAINTENANCE
2985 ;BIT3 = CLEAR MOS
2986 ;BIT8 = MASTER TRAN SCAN ENB
2987 ;WAIT FOR MOS TO CLEAR
2988 ;BITC = RECEIVER ENABLE
2989 012414 012777 000001 166572 1$: MOV #BITC, @TCR ;SET XMTR CONTROL BIT, LINED
2990 012422 017701 166562 MOV @CSR, R1 ;WAIT FOR XMTR READY
2991 012426 100375 BPL !$
2992 012430 012777 000252 166560 2$: MOV #252, @TBUF ;SEND AN "*"
2993 012436 013700 001302 MOV TIMER, RO ;SET UP TIMER
2994 012442 105305 DECB R5 ;SHORT WAIT LOOP
2995 012444 001376 BNE 2$
2996 012446 017701 166536 3$: MOV @CSR, R1 ;SAVE CSR
2997 012452 105701 TSTB R1 ;CHECK FOR DONE
2998 012454 100002 BPL 3$ ;BRANCH IF NOT SET
2999 012456 104001 HLT+1 ;DONE SET WHEN HALF DUPLEX (BIT1) SET
3000 ;R1=CONTENTS OF CSR
3001
3002 012460 000402 BR 4$
3003 012462 005300 3$: DEC RO ;TIMER COUNT
3004 012464 001366 BNE 2$ ;BRANCH IF MORE TIMER

```

```

3010
3011 012466 017701 166520 4$: MOV  @RBUF, R1 ;CHECK AND SAVE FI/FO
3012 012472 100001 BPL  .+4 ;BRANCH IF OK
3013 012474 104001 HLT+1 ;CHARACTER PRESENT IN FI/FO
3014 ;R1=DATA FROM FI/FO
3015 012476 042777 000002 166504 BIC  #BIT1, @CSR ;CLEAR HALF DUPLEX BIT
3016 012504 000240 NOP
3017 012506 000240 NOP
3018 012510 000240 NOP
3019 012512 000240 NOP
3020 012514 017701 166472 5$: MOV  @RBUF, R1 ;CHECK FOR CHAR PRESENT
3021 012520 100001 BPL  .+4 ;BRANCH IF CHAR NOT PRESENT
3022 012522 104001 HLT+1 ;CHAR PRESENT AFTER H/D CLEARED
3023 ;R1 = CONTENTS OF RBUF
3024 012524 005077 166464 CLR  @TCR ;CLR TRANS CONTROL REG
3025
3026 012530 104400 SCOPE
3027
3028
3029
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3034
3035
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3037
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3045
3046 012566 012777 000001 166420 1$: MOV  #BIT0, @TCR ;SET TRAN CONTROL BIT, LINE 0
3047 012574 017701 166410 MOV  @CSR, R1 ;WAIT
3048 012600 100375 BPL  1$
3049 012602 012777 000025 166406 2$: MOV  #25, @TBUF ;SEND #25
3050 012610 105777 166374 TSTB @CSR ;WAIT FOR DONE
3051 012614 100375 BPL  2$
3052 012616 000404 BR   END56 ;OK, BRANCH IF NO INTERRUPT
3053 012620 104000 ISR56: HLT ;SHOULDN'T HAVE INTERRUPTED AT LEVEL 5
3054 012622 012716 012630 MOV  #END56, (SP) ;MOVE NEW RTI ADR ONTO STACK
3055 012626 000002 RTI
3056
3057 012630 017701 166356 END56: MOV  @RBUF, R1 ;READ THE CHARACTER
3058 012634 100401 BMI  .+4 ;BRANCH IF CHAR PRESENT
3059 012636 104001 HLT+1 ;CHAR PRESENT MISSING
3060 ;R1 = CONTENTS OF RBUF
3061 012640 022701 100025 CMP  #100025, R1 ;CHECK THE DATA
3062 012644 001401 BEQ  .+4 ;BRANCH IF OK
3063 012646 104001 HLT+1 ;RECEIVED DATA ERROR
3064 ;R1 = CONTENTS OF RBUF
3065 012650 013777 001222 166342 MOV  RCVLVL, @RCVVEC

```

```

:*****
:TEST 56: TEST THAT RECEIVER INTERRUPT DOES NOT OCCUR AT LEVEL 5
:PROBABLE FAULTY LOGIC: M7821 WIRING, PROPER PRIORITY CHIP
:*****

```

```

3066 012656 012777 000004 166336      MOV      #IOT,  @RCVLVL
3067 012664 005077 166324      CLR      @TCR
3068 012670 005077 166314      CLR      @CSR
3069 012674 042737 000340 177776      BIC      #340,@#PS
3070
3071 012702 104400      SCOPE
3072
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3120

```

```

:*****
:TEST 57:      TEST THAT RECEIVER INTERRUPT OCCURES AT LEVEL 4
:PROBABLE FAULTY LOGIC:  M7821 WIRING,  PROPER PRIORITY CHIP
:*****

```

```

3079 012704 012777 012774 166306  TST57:  MOV      #ISR57, @RCVVEC ;SET UP XMTR INTERRUPT VECTOR
3080 012712 012777 000340 166302      MOV      #340,  @RCVLVL ;AT LEVEL 7
3081 012720 042737 000340 177776      BIC      #340,  @#PS ;CLEAR PS LEVEL
3082 012726 052737 000200 177776      BIS      #200,  @#PS ;SET PS TO LEVEL 4
3083 012734 004737 015546      JSR      PC,    @#INITB ;SET:

```

```

;BIT2 = MAINTENANCE
;BIT3 = CLEAR MOS
;BIT6 = RECEIVER INTERRUPT ENABLE
;BIT8 = MASTER TRANS SCAN ENABLE
;WAIT FOR MOS TO CLEAR
;BIT0 = RECEIVER ENABLE
;SET TRAN CONTROL BIT, LINE 0
;WAIT

```

```

3090 012740 012777 000001 166246      MOV      #BIT0, @TCR ;SET TRAN CONTROL BIT, LINE 0
3091 012746 017701 166236      1$:     MOV      @CSR,  R1 ;WAIT
3092 012752 100375      BPL      1$
3093 012754 012777 000025 166234      MOV      #25,   @TBUF ;SEND #25
3094 012762 105777 166222      2$:     TSTB   @CSR ;WAIT FOR DONE
3095 012766 100375      BPL      2$
3096 012770 104000      HLT
3097 012772 000403      BR      ENDS7 ;SHOULD HAVE INTERRUPTED AT LEVEL 4
3098 ;CONTINUE

```

```

;SHOULD HAVE INTERRUPTED AT LEVEL 4
;CONTINUE

```

```

3099 012774 012716 013002      ISR57:  MOV      #ENDS7,(SP) ;MOVE NEW RTI ADR ONTO STACK
3100 013000 000002      RTI

```

```

3102 013002 017701 166204      ENDS7:  MOV      @RBUF,  R1 ;READ THE CHARACTER
3103 013006 100401      BMI     .+4 ;BRANCH IF CHAR PRESENT
3104 013010 104001      HLT+1 ;CHAR PRESENT MISSING
3105 ;R1 = CONTENTS OF RBUF
3106 013012 022701 100025      CMP     #100025,R1 ;CHECK THE DATA
3107 013016 001401      BEQ     .+4 ;BRANCH IF OK
3108 013020 104001      HLT+1 ;RECEIVED DATA ERROR
3109 ;R1 = CONTENTS OF RBUF

```

```

3110 013022 013777 001222 166170      MOV      RCVLVL,@RCVVEC
3111 013030 012777 000004 166164      MOV      #IOT,  @RCVLVL
3112 013036 005077 166152      CLR      @TCR
3113 013042 005077 166142      CLR      @CSR
3114 013046 042737 000340 177776      BIC      #340,@#PS
3115
3116 013054 104400      SCOPE
3117
3118
3119
3120

```

```

:*****
:TEST 60:      TEST FI/FO OVERRUN
:               THE FI/FO BUFFER SHOULD HOLD 64 CHARACTERS.
:

```


M05

MAINDEC-11-DZDJA-D
DZDJA0.P11 TST60:

DJ11 LOGIC TESTS
TEST FI/FO OVERRUN

MACY11 27(732) 21-SEP-76 13:43 PAGE 62

:PROBABLE FAULTY LOGIC: M7285 (D1-7) E32, E17, E22 (D2-2) E5, E1
:*****

: INITIALIZE
: DEVICE"CSR"REGISTER

013056 004737 015566

TST60: JSR PC, @#INITD

SET:
:BIT2 = MAINTENANCE
:BIT3 = CLEAR MOS
:BIT8 = MASTER XMTR SCAN ENB

:WAIT FOR MOS TO CLEAR

SET:
:BIT0 = RECEIVER ENABLE

013062 012777 177777 166124

MOV #177777,@TCR

:TRANS CONTROL BIT, ALL LINES
:SET UP COUNTER - 64. CHAR FI/FO BUFF
:SAVE AND WAIT FOR TRANS READY

013070 012700 000100

MOV #100, R0

013074 017701 166110

1\$: MOV @CSR, R1

013100 100375

BPL 1\$

013102 000377 166110

SWAB @TBUF

:TRANSMIT LINE # ON LINE

013106 032701 020000

BIT #BIT13, R1

:CHECK FI/FO OVERRUN

013112 001401

BEQ .+4

:BRANCH IF OK

013114 104001

HLT+1

:FI/FO OVERRUN TOO SOON

013116 005300

DEC R0

:R1=CONTENTS OF CSR

013120 001365

BNE 1\$

:COUNT DOWN

013122 013700 001302

MOV TIMER, R0

:SET UP TIMER

013126 017701 166056

2\$: MOV @CSR, R1

:WAIT FOR XMTR READY

013132 100375

BPL 2\$

013134 105305

3\$: DECB R5

:SHORT WAIT LOOP

013136 001376

BNE 3\$

013140 017701 166044

MOV @CSR, R1

:SAVE CSR FOR THE RECORD

013144 100401

BMI .+4

:BRANCH IF TRANS READY

013146 104001

HLT+1

:TRANS READY MISTERIOUSLY DISAPPEARED

013150 005300

DEC R0

:R1=CONTENTS OF CSR

013152 001370

BNE 3\$

:TIME 3 CHARACTER LENGTHS

:BRANCH IF MORE TIME

:FI/FO SHOULD NOW BE FULL

013154 105701

TSTB R1

:CHECK THAT DONE IS SET

013156 100401

BMI .+4

:BRANCH IF OK

013160 104001

HLT+1

:DONE DIDN'T COME UP!

013162 022701 100605

CMP #100605,R1

:R1 = CONTENTS OF CSR

013166 001401

BEQ .+4

:CHECK THAT FI/FO NOT OVERRUN

013170 104001

HLT+1

:BRANCH IF OK

:FI/FO OVERRUN SET

:OR SOME OTHER CSR ERROR

:R1=CONTENTS OF CSR

:*****
:TEST 60A: TEST THAT FI/FO OVERRUN COMES UP WHEN 65TH CHARACTER
: IS RECEIVED WITHOUT READING FI/FO
:*****

013172 000377 166020

T60A: SWAB @TBUF

:SEND 65TH CHARACTER

013176 013700 001302

MOV TIMER, R0

:SET UP TIMER

TEST TEST FOR OVERRUN

Assembly code listing with addresses, instructions, and comments. Includes instructions like BFC, BR, CMP, MOV, and BIC.

::TEST 61: TEST THAT UART OVERRUN IS DETECTED ON ALL LINES
::PROBABLE FAULTY LOGIC: M7285 (DR-2) E3, E1; M7279; M7280

Assembly code listing with addresses, instructions, and comments. Includes instructions like MOV, BIT, CLR, and BFC.


```

014312 017701 164676 MOV BCSR, R1 :CHECK AND SAVE BCSR
014316 022701 177777 CMP #177777,R1 :CHECK THAT ALL THE BITS ARE SET
014320 001401 BEQ .+4 :BRANCH IF OK
014324 104001 HLT+1 :BIT(S) OF BCSR FAILED TO SET

014326 005077 164662 CLR BCSR :CLEAR BCSR
014330 017701 164656 MOV BCSR, R1 :CHECK THAT IT CLEARED AND SAVE
014334 001401 BEQ .+4 :BRANCH IF CLR
014340 104001 HLT+1 :BIT(S) OF BCSR FAILED TO CLEAR

014342 104400 SCOPE

```

```

*****
:TEST 63: TEST THAT LINED CAN TRANSMIT AND RECEIVE A BREAK
: ALSO CHECKS FRAMING ERROR(RBUF BIT13)
: ALSO CHECKS PARITY ERROR(RBUF BIT12)
: IF ODD PARITY IS SELECTED
:PROBABLE FAULTY LOGIC: M7295 (D2-2) E5, E1, (D2-3) E16, E2, E19, E35
*****

```

```

014344 004737 015536 TST63: JSR PC, @#INITA :INITIALIZE
:BIT2 = MAINTENANCE
:BIT3 = CLEAR MOS
:BIT10= R/W BCSR
:WAIT FOR MOS TO CLEAR
:BIT0 = RECEIVER ENABLE
:SEND BREAKS, LINE 0
:SET UP TIMER
:SHORT WAIT LOOP

014350 012777 000001 164636 MOV #1, BCSR
014356 013700 001302 MOV TIMER, R0
18: DECB R5
BNE 18
014362 105305 MOV BCSR, R1 :SAVE CSR
014364 001376 TSTB R1 :CHECK FOR DONE
014366 017701 164616 BMI R2 :BRANCH WHEN DONE
014372 105701 INC R0 :WAIT A WHILE
014374 100404 BNE 18
014376 005200 HLT+1 :DONE NEVER CAME UP
:R1=CONTENTS OF CSR

014404 000430 BR 48
014406 022701 002205 28: CMP #2205, R1 :CHECK REST OF CSR
014410 001401 BEQ .+4 :BRANCH IF OK
014414 104001 HLT+1 :CSR ERROR
:R1=CONTENTS OF CSR

014416 017701 164570 MOV RBUF, R1 :GET DATA FROM FI/FO
014420 100401 BMI .+4 :BRANCH IF OK
014424 104001 HLT+1 :CHARACTER PRESENT NOT UP
:R1=CONTENTS OF RBUF

014426 032701 020000 BIT #020000,R1 :CHECK FOR FRAMING ERROR
014430 001001 BNE .+4 :BRANCH IF OK
014434 104001 HLT+1 :FRAMING ERROR NOT UP
:R1=CONTENTS OF RBUF

014436 133737 001310 001276 BITB DJPAR, PARITY :CHECK ODD PARITY FLAG
014444 001404 BEQ 38 :BRANCH IF NOT
014446 032701 010000 BIT #010000,R1 :CHECK PARITY ERROR
014452 001005

```

```

014454 104001          HLT+1          ;ODD PARITY SHOULD CAUSE PARITY ERROR
                                ;R1=CONTENTS OF RBUF
014456 032701 010000 3$: BIT      #010000,R1      ;CHECK PARITY ERROR
014458 001401          BEQ          ;BRANCH IF OK
014454 104001          HLT+1          ;EVEN PARITY OR NO PARITY
                                ;SHOULDN'T CAUSE PARITY ERROR
014456 032701 040000 4$: BIT      #040000,R1      ;R1=CONTENTS OF RBUF
014458 001401          BEQ          ;CHECK UART OVERRUN
014454 104001          HLT+1          ;BRANCH IF OK
                                ;UART OVERRUN SET!!
014456 032701 007400 BIT      #007400,R1      ;R1=CONTENTS OF RBUF
014458 001401          BEQ          ;CHECK LINE #
014454 104001          HLT+1          ;BRANCH IF OK
                                ;WRONG LINE# IN FI/FO
014456 105701          TSTB     R1          ;R1=CONTENTS OF RBUF
014458 001401          BEQ          ;CHECK DATA
014454 104001          HLT+1          ;BRANCH IF OK
                                ;WRONG DATA RECEIVED
014456 017701 164472 MOV     R2,RBUF, R1      ;READ FI/FO AGAIN
014458 001401          BEQ          ;BRANCH IF OK
014454 104001          HLT+1          ;EXTRA CHAR IN FI/FO
014456 005077 164464 5$: CLR     R2,0CSR      ;R1 = CONTENTS OF RBUF
014458 105305          DECIB    R2,0CSR      ;CLEAR BREAK CONTROL REG
014454 104001          HLT+1          ;SHORT WAIT LOOP-REGISTER # MARK
014456 104400          SCOPE

```

```

*****
:TEST 64:      TEST THAT EACH LINE CAN TRANSMIT AND RECEIVE A BREAK
:              ALSO CHECK FOR PARITY ERROR(RBUF BIT12)
:              ALSO CHECK FOR ODD PARITY ERROR(RBUF BIT13)
:              ALSO CHECK FOR ODD PARITY IN REGISTER
:PROBABLE FAULTY LOGIC:  MARKS (0A-3) R5, R1, (0A-3) R16, R2, R10, R20
*****

```

```

014536 004737 015536  TST64:  JGR     R0,     R=INITA  ;INITIALIZE
                                ;BITS = MAINTENANCE
                                ;BITS = CLEAR MOS
                                ;BIT10 = R/W BCSR
                                ;BIT11 = FOR MOS TO CLEAR
                                ;BIT12 = RECEIVER ENABLE
                                ;COUNT UP LINE COUNTER
                                ;COUNT UP LINE MARKER
                                ;COUNT UP TIMER
                                ;SET BREAK CONTROL BIT, LINE # IN R1
                                ;SHORT WAIT LOOP
014542 005001          CLR     R1          ;SAVE CSR
014544 012704 000001 MOV     R1,0CSR, R1      ;CHECK FOR DONE
014546 013700 001302 MOV     R1,TIMER, R0     ;BRANCH WHEN DONE
014548 050477 164434 BIT     R1,0CSR          ;WAIT A WHILE
014550 105305          DECIB    R1,0CSR
014552 001376          BNE     R1,0CSR
014554 017702 164420 MOV     R2,0CSR, R2
014556 105702          TSTB     R2
014558 100404          BMI     R2
014560 005200          INC     R2

```


014576	001370			BNE	18				:DONE NEVER CAME UP
014600	104002			HLT+2					:R1 = LINE #
									:R2 = CONTENTS OF CSR
014608	000420			BNE	4				:CHECK REST OF CSR
014604	000700	002805	33:	CMR	#0205, R2				:BRANCH IF OK
014610	001401			BNE	.+4				:CSR ERROR
014610	104002			HLT+2					:R1 = LINE #
									:R2 = CONTENTS OF CSR
014614	017700			MOV	R2, R2				:GET DATA FROM FI/FO
014610	102401	164372		BNE	.+4				:BRANCH IF OK
014610	104002			HLT+2					:CHARACTER PRESENT NOT UP
									:R1 = LINE #
									:R2 = CONTENTS OF RBUF
014624	002700			BNE	#020000, R2				:CHECK FOR FRAMING ERROR
014620	001001	020000		BNE	.+4				:BRANCH IF OK
014620	104002			HLT+2					:FRAMING ERROR NOT UP
									:R1 = LINE #
									:R2 = CONTENTS OF RBUF
014634	001010			MOV	R3, R3				:GET LINE #
014630	000300			BNE	.+4				:BRANCH IF OK
014630	000300			BNE	.+4				:BRANCH IF OK
014630	133763	001310	001275	BNE	DUPAR, PARITY(3)				:CHECK ODD PARITY FLAG
014630	001404			BNE	38				:BRANCH IF NOT
014630	002700	010000		BNE	#010000, R2				:CHECK PARITY ERROR
014630	001005			BNE	.+4				:CHECK PARITY ERROR
014630	104002			HLT+2					:ODD PARITY SHOULD CAUSE PARITY ERROR
									:R1 = LINE #
									:R2 = CONTENTS OF RBUF
014660	002700			BIT	#010000, R2				:CHECK PARITY ERROR
014660	001401	010000	33:	BNE	.+4				:BRANCH IF OK
014670	104002			HLT+2					:EVEN PARITY OR NO PARITY
									:SHOULDN'T CAUSE PARITY ERROR
									:R1 = LINE #
									:R2 = CONTENTS OF RBUF
014672	002700			BIT	#040000, R2				:CHECK UART OVERRUN
014676	001401	040000	46:	BEO	.+4				:BRANCH IF OK
014700	104002			HLT+2					:UART OVERRUN SET!!
									:R1 = LINE #
									:R2 = CONTENTS OF RBUF
014702	010203			MOV	R2, R3				:DUP DATA
014704	000303			SWAB	R3				:LINE # IN LOW BYTE
014706	042703	177760		BIC	#177760, R3				:MASK ALL BUT LINE #
014712	020103			CMR	R1, R3				:CHECK FOR RIGHT LINE #
014714	001401			BEO	.+4				:BRANCH IF OK
014716	104002			HLT+2					:WRONG LINE# IN FI/FO
									:R1 = LINE #
									:R2 = CONTENTS OF RBUF
014720	105702			TSTB	R2				:CHECK DATA

TST64:

```

3626 014722 001401      BEQ      .+4      :BRANCH IF OK
3627 014724 104002      HLT+2                :WRONG DATA RECEIVED
3628                                :R1 = LINE #
3629                                :R2 = CONTENTS OF RBUF
3630 014726 017702 164260  MOV      @RBUF, R2  :READ FI/FO AGAIN
3631 014732 100001      BPL      .+4      :BRANCH IF OK
3632 014734 104002      HLT+2                :EXTRA CHAR IN FI/FO
3633                                :R1 = LINE #
3634                                :R2 = CONTENTS OF RBUF
3635 014736 005077 164252  CLR      @BCSR      :CLEAR BREAK CONTROL REG
3636 014742 005201      INC      R1          :COUNT LINES
3637 014744 006304      ASL      R4          :UPDATE LINE MARKER
3638 014746 103300      BCC      LOP64      :BRANCH IF MORE LINES
3639
3640 014750 005077 164234  CLR      @CSR       :CLEAR CSR
3641 014754 104400
3642
3643 014756 012737 000002 015772  MOV      #2,        TIMES

```

```

:*****
:TEST 65:      TEST THAT RESET CLEARS ALL BUFFERS
:NOTE:        THE FI/FO BUFFER IS NOT COMPLETELY CLEARED
:              BY RESET; ONLY CHARACTER PRESENT IS CLEARED.
:PROBABLE FAULTY LOGIC: M7285 (D2-8) E13
:*****

```

```

3644 014764 052737 000340 177776  TST65:  BIS      #340,@#PS  :SET PROCESSOR TO LEVEL 7
3645 014772 012777 177777 164214  MOV      #177777,@TCR :SET ALL TOR BITS
3646 015000 012777 052507 164202  MOV      #052507,@CSR :SET ALL R/W BITS OF CSR
3647 015006 012777 177777 164200  MOV      #177777,@BCSR :SET ALL BREAK CONTROL BITS (SEND BREAKS)
3648 :NOTE: ALL LINES SHOULD BE SENDING BREAKS, BUT NONE SHOULD BE RECEIVING
3649 :       BECAUSE THE HALF DUPLEX BIT IS SET
3650 015014 012777 177777 164174  MOV      #177777,@TBUF :LOADING TRANS BUFF WHEN BREAK BIT SET
3651 :       SHOULD DO NOTHING
3652 015022 000005      RESET              :CLEAR THE WORLD
3653 015024 013737 001210 015034  MOV      CSR,1$     :CHECK CSR AND SAVE
3654 015032 013701      MOV      @PC)+,R1
3655 015034 000000 1$: 000000
3656 015036 001401      BEQ      .+4
3657 015040 104001      HLT+1
3658
3659 015042 017701 164146  MOV      @TCR,R1    :CHECK TOR AND SAVE
3660 015046 001401      BEQ      .+4
3661 015050 104001      HLT+1
3662
3663 015052 017701 164136  MOV      @BCSR,R1   :CHECK BCSR AND SAVE
3664 015056 001401      BEQ      .+4
3665 015060 104001      HLT+1
3666
3667 015062 017701 164124  MOV      @RBUF,R1   :CHECK RBUF AND SAVE
3668 015066 100001      BPL      .+4
3669 015070 104001      HLT+1
3670
3671 015072 017701 164120  MOV      @TBUF,R1   :CHECK TBUF AND SAVE
3672 015076 001401      BEQ      .+4
3673 015100 104001      HLT+1

```

015102 104400

SCOPE

:TEST 66: SEND A BINARY COUNT PATTERN ON EACH LINE
:PROBABLE FAULTY LOGIC: COULD BE ALMOST ANYWHERE!

015104 005001
015106 012703 100000
015112 005004
015114 042737 000340 177776
015122 052737 000200 177776
015130 012700 000001
015134 012777 000010 164046
015142 012777 010505 164040

TST66: CLR R1 ;SET UP LINE COUNTER
MOV #100000,R3 ;SET UP RCV DATA
CLR R4 ;SET UP TRANS DATA
BIC #340, @#PS ;CLEAR PROCESSOR PRIORITY
BIS #200, @#PS ;SET PRIORITY TO 4
MOV #1, R0 ;SET UP LINE MARKER
MOV #10, @CSR ;CLEAR MOS
MOV #010505, @CSR ;BIT0 = RECEIVE ENABLE
;BIT2 = MAINTENANCE
;BIT6 = RECEIVER INTERRUPT ENB
;BIT8 = TRANS SCAN ENABLE
;BIT12= STATUS ENABLE

015150 032777 000020 164032 10\$:
015156 001374
015160 012777 015274 164032
015166 012777 000240 164026
015174 010077 164014 1\$:
015200 005777 164004 2\$:
015204 100375
015206 010477 164004
015212 105204
015214 001371
015216 105703 3\$:
015220 001376
015222 017702 163762
015226 022702 110505
015232 001401
015234 104002

BIT #BIT4, @CSR ;WAIT FOR MOS TO CLEAR
BNE 10\$
MOV #ISR66, @RCVVEC ;SET UP RECEIVER INTERRUPT VECTOR
MOV #240, @RCVVLV
MOV R0, @TCR ;TRANS CONTROL, ONE LINE AT A TIME
TST @CSR ;WAIT FOR TRANS READY
BPL 2\$
MOV R4, @TBUF ;SEND DATA
INCB R4 ;BINARY COUNT
BNE 2\$
TSTB R3 ;WAIT FOR RECEIVER DONE
BNE 3\$
MOV @CSR, R2 ;SAVE CSR
CMP #110505, R2 ;CHECK CSR
BEQ .+4 ;BRANCH IF OK
HLT+2 ;CSR ERROR
R1=LINE #
R2=CONTENTS OF CSR

015236 017702 163750
015242 100001
015244 104002
015246 062703 000400
015252 005201
015254 032701 000003
015260 001002
015262 005237 001306
015266 006300
015270 103341
015272 000417

MOV @RBUF, R2 ;CHECK CHARACTER PRESENT
BPL .+4 ;BRANCH IF OK
HLT+2 ;CHARACTER PRESENT SET!!
R1=LINE #
R2=CONTENTS OF CSR
ADD #400, R3 ;UPDATE LINE # IN EXPECTED DATA
INC R1 ;UPDATE LINE #
BIT #3, R1 ;CHECK FOR FOURTH LINE
BNE 4\$;BRANCH IF NOT
INC DJLEN ;MOVE CHARACTER LENGTH POINTER
ASL R0 ;UPDATE LINE MARKER
BCC 1\$;BRANCH IF MORE
BR END66 ;SKIP ISR

015274 017702 163712
015300 100401
015302 104003

ISR66: MOV @RBUF, R2 ;READ FIRST DATA
BMI 11\$;BRANCH IF CHARACTER PRESENT
HLT+3 ;INTERRUPT BUT NO CHAR PRESENT

```

3738 ;R1=LINE #
3739 ;R2=CONTENTS OF RBUF
3740 ;R3=EXPECTED DATA
3741 015304 020203 11$: CMP R2 R3 ;CHECK THE DATA
3742 015306 001401 BEQ .+4 ;BRANCH IF OK
3743 015310 104003 HLT+3 ;DATA ERROR
3744 ;R1=LINE #
3745 ;R2=CONTENTS OF RBUF
3746 ;R3=EXPECTED DATA
3747 015312 105203 INCB R3 ;UPDATE EXPECTED DATA
3748 015314 147703 163766 BICB @DJLEN, R3 ;MASK CHARACTER LENGTH
3749 015320 001403 BEQ 12$ ;BRANCH OUT IF DATA=0
3750 015322 017702 163664 MOV @RBUF, R2 ;READ MORE DATA
3751 015326 100766 BMI 11$ ;BRANCH IF MORE
3752 015330 000002 12$: RTI ;RETURN
3753
3754 015332 162737 000004 001306 END66: SUB #4, DJLEN ;RESET CHAR LENGTH POINTER
3755 015340 013777 001222 163652 MOV RCVLVL, @RCVVEC ;RESTORE RECEIVER INT. VEC
3756 015346 012777 000004 163646 MOV #IOT, @RCVLVL
3757 015354 005077 163634 CLR @TCR ;CLEAR TCR
3758 015360 005077 163624 CLR @CSR ;CLEAR CSR
3759 015364 104400 SCOPE
3760
3761 015366 012737 000020 015772 MOV #20, TIMES
3762 015374 023737 001304 001234 CMP DJUIT, UNITS ;CHECK FOR LAST UNIT
3763 015402 002002 BGE DONE ;BRANCH IF LAST UNIT
3764 015404 000137 002302 JMP RESTAR ;JUMP IF NOT
3765
3766 015410 DONE:
3767 015410 004737 017640 JSR PC, KBDINT
3768 015414 062737 000001 001206 ADD #1, PCNT+2 ;ADD 1 TO THE PASS COUNT
3769 015422 005537 001204 ADC PCNT ;MAKE IT DOUBLE PREC.
3770 015426 032777 002000 163662 BIT #SW10, @SWR ;RING THE BELL?
3771 015434 001004 BNE 1$ ;NO!
3772 015436 000004 000007 TYPE ,BELL ;RING THE BELL
3773 015442 000004 000177 TYPE ,177 ;TYPE A FILLER FOR 11/05
3774 015446 005046 1$: CLR -(6) ;CLEAR TRACE TRAP
3775 015450 032777 010000 163640 BIT #SW12, @SWR ;RUN WITH TRT?
3776 015456 001010 BNE 2$ ;SKIP T BIT
3777 015460 005137 015532 COM .TBIT ;COMPLIMENT FLAG
3778 015464 100005 BPL 2$ ;SKIP IF PLUS
3779 015466 052716 000020 BIS #20, (6) ;SET TRACE TRAP
3780 015472 012746 015526 MOV #3$, -(6) ;JUMP TO START OF TEST
3781 015476 000002 RTI ;RETURN
3782 015500 012746 015506 2$: MOV #4$, -(6) ;JUMP TO START OF TEST
3783 015504 000002 RTI ;RETURN
3784 015506 013700 000042 4$: MOV @#42, R0 ;GET MONITOR ADDRESS
3785 015512 001405 BEQ 3$ ;IF NONE
3786 015514 000005 RESET ;RESET AND
3787 015516 $ENDAD =
3788 015516 004710 JSR 7, (0) ;GO TO MONITOR
3789 015520 000240 NOP ;SAVE ROOM
3790 015522 000240 NOP ;FOR
3791 015524 000240 NOP ;ACT11
3792 015526 000137 002302 3$: JMP RESTAR ;RETURN
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015532 000000
015534 000002

015536 012777 002014 163444
015544 000413

015546 012777 000514 163434
015554 000407

015556 012777 000416 163424
015564 000403

015566 012777 000414 163414
015574 005000

015576 005200
015600 001004

015602 011600
015604 162700 000002

015610 104000

015612 032777 000020 163370
015620 001366

015622 052777 000001 163360
015630 000207

```
.TBIT: 0 ;T BIT FLAG
YESRT: RTI ;RETURN FROM TRACE TRAP
INITIALIZATION ROUTINE
DEVICE CSR REGISTER
ON FAILURE: REGISTER 0 CONTAINS ERROR ADDRESS
SET:
BIT01 = HALF DUPLEX
BIT02 = MAINTENANCE
BIT03 = CLEAR MOS
BIT06 = RECEIVER INTERRUPT ENABLE
BIT08 = MASTER XMTR SCAN ENS
BIT10 = R/W BCSR
WAIT FOR MOS TO CLEAR
SET:
BIT00 = RECEIVER ENABLE
INITA: MOV #2014,0CSR SET
BR INTR ;BIT(S)2,3,10 THEN 0
INITB: MOV #514,0CSR ;BIT(S)2,3,6,8 THEN 0
BR INTR
INITC: MOV #416,0CSR ;BIT(S)1,2,3,9 THEN 0
BR INTR
INITD: MOV #414,0CSR ;BIT(S)2,3,8 THEN 0
INITR: CLR R0
1$: INC R0 ;ANTI HANG
BNE 2$ ;ROUTINE
MOV (SP),R0 ;RECORD SUBROUTINE CALL RETURN
SUB #2,R0 ;FORM CALL ADDRESS FOR DISPLAY
HLT ;BIT#4 OF DEVICE CSR FAILED TO CLEAR
2$: BIT #BIT4,0CSR ;TEST HAS MOS CLEARED
BNE 1$ ;NO BRANCHES
SET:
;BIT00 RECEIVE ENABLE
RTS PC ;CONTINUE
;
; $SCOPE SCOPE LOOP HANDLER
;THIS ROUTINE HANDLES THE ITERATIONS, LOOPING, ERROR
;LOOPING, AND THE DISPLAYING OF THE TEST NUMBER.
```

M06

MAINDEC-11-DZDJA-D
DZDJD.F11

DJ11 LOGIC TESTS
SCOPE LOOP HANDLER

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```

3850          : "SCOPE" IS PLACED BETWEEN EACH SUBTEST IN THE TEST AND
3851          : RECORDS THE STARTING ADDRESS OF THE SUBTEST IN "LAD:"
3852          :
3853          TRAPS: JSR      PC,      KBDINT
3854          015632 004737 017640          BIT      #SW8, @SWR      : LOOP ON SPEC. TEST?
3855          015636 032777 000400 163452          BEQ      1$          : NO LOOP ON SPEC. TEST
3856          015644 001404          CMPB     @SWR, ICNT   : ON RIGHT TEST? *SW7-0*
3857          015646 127737 163444 001200          BEQ      OVER$      : NOT RIGHT TEST
3858          015654 001434          BIT      #SW14, @SWR : LOOP ON TEST?
3859          015656 032777 040000 163432 1$:          BNE     KITS$      : LOOP ON TEST IS SET
3860          015664 001026          BIT      #SW11, @SWR : KILL ITERATIONS
3861          015666 032777 004000 163422          BNE     SVLAD$     : YES - KILL ITERATIONS
3862          015674 001012          TSTB    ICNT+1     : FIRST ONE?
3863          015676 105737 001201          BEQ      2$          : BRANCH IF FIRST
3864          015702 001404          CMPB    TIMES, ICNT+1 : DONE?
3865          015712 001013          BNE     KITS$      : BRANCH IF NOT
3866          015714 112737 000001 001201 2$:          MOVB    #1, ICNT+1 : FIRST ITERATION
3867          015722 105237 001200          SVLAD$: INCB     ICNT   : COUNT TEST NUMBERS
3868          015726 011637 015770          MOV     (6), LAD   : SAVE LOOP ADDRESS
3869          015732 013737 001200 001320          MOV     ICNT, @#DISPLAY : DISPLAY TEST NO. AND ITERATION COUNT
3870          015740 000002          RTI                                : RETURN
3871          :
3872          015742 105237 001201          KITS$: INCB     ICNT+1   : INC THE ITERATION COUNT
3873          015746 013737 001200 001320 OVER$: MOV     ICNT, @#DISPLAY : SET UP DISPLAY
3874          015754 005737 015770          TST     LAD        : FIRST ONE?
3875          015760 001760          BEQ     SVLAD$     : YES
3876          015762 013716 015770          MOV     LAD, (6)   : FUDGE RETURN ADDRESS
3877          015766 000002          RTI                                : FIXES PS
3878          :
3879          015770 000000          LAD:    0          : LOOP ADDRESS
3880          015772 000020          TIMES: 20         : RUN 20 TIMES

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015774 004737 017640
016000 032777 002000 163310
016006 001402
016010 000004 000007
016014 005237 001202
016020 032777 020000 163270
016026 001026
016030 000004 016034
016040 011637 016144
016044 162737 000002 016144
016052 117737 000066 016142
016060 013705 016144
016064 004737 016562
016070 000004 016074
016100 004737 016146
016104 005777 163206
016110 100001
016112 000000
016114 004737 017640
016120 032777 001000 163170
016126 001001
016130 000002
016132 105037 001201
016136 000137 015742
016142 000000
016144 000000
016146
016146 013705 001210
016152 004737 016562
016156 042737 007700 016204
016164 105337 016142
016170 100411
016172 062737 000100 016204
016200 000004 017241
016204 010005
016206 004737 016562
016212 000764
016214 000207
    
```

```

; $HLT ERROR TIMEOUT HANDLER
; THIS ROUTINE PRINTS OUT ERROR MESSAGES STARTING WITH THE
; ADDRESS OF THE "HLT". IT ALSO COUNTS THE NUMBER OF ERRORS
; AND HAS THE CAPABILITY OF LOOPING ON ERROR, BELL ON ERROR,
; "HALT" ON ERROR, AND INHIBIT TIMEOUTS. AN OPTIONAL ARGUMENT
; (HLT+3) WILL BE PLACED IN "HLTCT$:" FOR ADITIONAL TIMEOUTS.

EMTS: JSR PC, KBDINT
      BIT #SW10, QSWR ; BELL ON ERROR?
      BEQ 1$ ; NO - SKIP
      TYPE ,BELL ; RING BELL
      INC ERRORS ; COUNT THE NUMBER OF ERRORS
      BIT #SW13, QSWR ; SKIP TIMEOUT IF SET
      BNE 2$ ; SKIP TIMEOUTS
      TYPE ,.+2 ; .ASCIZ <15><12>
      MOV (6), HLTADR ; PUT ADDRESS OF INSTRUCTION ON STACK
      SUB #2, HLTADR ; FUDGE ADDRESS
      MOVSB QHLTADR, HLTCT$ ; GET HLT ARGUMENT
      MOV HLTADR, TTY ; TYPE HLTADR IN OCTAL
      JSR PC, PRINTR ; TYPE LEADING ZERO'S
      TYPE ,.+2 ; .ASCIZ " "
      JSR PC, ERRORS$ ; GO TO USER ERROR ROUTINE
      TST QSWR ; HALT ON ERROR
      BPL .+4 ; SKIP IF CONTINUE
      HALT ; HALT ON ERROR!
      JSR PC, KBDINT
      BIT #SW9, QSWR ; CHECK FOR INHIBIT LOOP ON ERROR
      BNE .+4 ; SKIP IF LOOP ON ERROR
      RTI ; RETURN
      CLRB ICNT+1 ; CLEAR ITERATION COUNT
      JMP KITS ; LOOP ON TEST UNTIL NO ERRORS

HLTCT$: 0 ; HLT ARGUMENT
HLTADR: 0 ; LAST HLT INSTRUCTION EXECUTED

ERRORS:
      MOV CSR, TTY ; TYPE CSR IN OCTAL
      JSR PC, PRINTR ; TYPE LEADING ZERO'S
      BIC #7700, 2$
      1$: DECB HLTCT$
      BMI 3$
      ADD #100, 2$
      TYPE ,SPACE
      2$: MOV %0, TTY ; TYPE REGISTER X IN OCTAL
      JSR %7, PRINTR
      BR 1$
      3$: RTS PC
    
```



```

017072 000126 PDOWN: MOV #ILLUP,SPUVECS :GET FOR FAST UP
000240 000126 MOV #40,SPUVECS+2 :PRIO:7
MOV R0,-(6) :PUSH R0 ON STACK
MOV R1,-(6) :PUSH R1 ON STACK
MOV R2,-(6) :PUSH R2 ON STACK
MOV R3,-(6) :PUSH R3 ON STACK
MOV R4,-(6) :PUSH R4 ON STACK
MOV R5,-(6) :PUSH R5 ON STACK
MOV R6,-(6) :SAVE SP
017076 000072 MOV #ILLUP,SPUVECS :SET UP VECTOR
017010 000072 HLT :WAIT FOR PF

017076 PUPS: MOV #SAVE,SP :GET SP
16: MOV #0,SP :WAIT LOOP FOR THE TTY
MOV #0,SP :WAIT FOR THE INC
MOV #0,SP :OF WORD
MOV #0,SP :POP STACK INTO R5
MOV #0,SP :POP STACK INTO R4
MOV #0,SP :POP STACK INTO R3
MOV #0,SP :POP STACK INTO R2
MOV #0,SP :POP STACK INTO R1
MOV #0,SP :POP STACK INTO R0
MOV #0,SP :SET UP THE POWER DOWN VECTOR
MOV #0,SP :PRIO:7
MOV #0,SP :ASCIZ <15><12>"POWER"
MOV #0,SP :JMP TO USER ADDRESS

017072 000000 ILLUP: HLT :THE POWER UP SEQUENCE WAS STARTED
017074 000072 BR 16 : BEFORE THE POWER DOWN WAS COMPLETE

017072 000000 .SAVE,SP: 0 :PUT THE SP HERE
017074 000000 PUPFOR: BR 16 :POWER UP VECTOR

```

017104	022716	001000	
017104	002740		
017104	162716	000004	
017104	012750		
017104	005700		
017104	011600		
017104	104002		
017166	000002		
017173	010546		
017173	017646	000002	
017173	032700	177400	
017173	001004		
017173	010537	017234	
017173	105715	017234	
017173	001406		
017173	112537	177566	
017173	105737	177564	
017173	100375		
017173	000770		
017173	017646	000002	
017200	062766	000002	000004
017200	022666	000002	
017200	001006		
017200	052700	000002	
017200	042700	000001	
017200	010566	000002	
017200	012600		
017200	000002		
017200	000000		
017236	005016	000	
017241	000040	000040	
017244	005016	044506	051522
017244	020124	045104	030461
017244	040440	042104	042522
017244	051522	020072	000040
017244	005016	042522	052103
017244	051117	040440	042104

```

*****
:NOT HANDLER. REENTERENT ROUTINE TO EITHER TYPE MESSAGES OR
:INDICATE A FAULSE INTERUPT OR TRAP.
*****

```

```

IOTRAP: CMP      #1000, (SP) ;CHECK RETURN ADDRESS FOR FAULSE TRAP
        BLT     IOTS ;BRANCH IF "TYPE" COMMAND INTENDED
        SUB     #4, (SP) ;GET VECTOR ADDRESS FROM RETURN ADDRESS
        MOV     (SP)+, R1 ;PUT IN R1 FOR TYPING
        TST    (SP)+ ;POP STACK
        MOV     (SP), R2 ;SAVE RETURN ADDRESS FOR TYPING
        HLT+2 ;UNEXPECTED INTERUPT OR TRAP
          ;R1 = VECTOR ADDRESS
          ;R2 = RETURN PC
          ;CONTINUE THE PROGRAM

```

```

:MOCALL $TYPE
:      $TYPE MESSAGE TYPEOUT ROUTINE

```

```

:THIS ROUTINE IS USE TO TYPE ASCII MESSAGES ON THE TTY. THE
:CALL CAN BE IN ONE OF 3 FORMS: 1) "TYPE ADR" - TYPES THE
:MESSAGE STARTING IN LOCATION "ADR:" 2) "TYPE CHAR" - TYPES
:THE ASCII "CHAR", AND 3) "PRINT <<15><12>"MESSAGE" - TYPES
:THE MESSAGE WHICH IS INLINE ASCII.

```

```

IOTS:  MOV     TTY, -(6) ;SAVE TTY
        MOV     22(6), TTY ;GET ADDRESS TO BE TYPED
        BIT     #177400, TTY ;IS IT A TYPEN?
        BNE    16 ;NO
        MOV     TTY, TYPE ;GET THE CHARACTER
        MOV     #TYPE, TTY ;FUDGE THE ADDRESS
16:     TSTB   (TTY) ;TERMINATOR?
        BEQ    26 ;GET OUT IF SO
        MOVB   (TTY)+, 2#177566 ;LOAD AND TYPE THE CHARACTER
        TSTB   2#177564 ;IS THE PRINTER READY
        BPL    14 ;WAIT UNTIL IT IS
        MOVB   22(6), -(6) ;GET THE NEXT CHARACTER
26:     ADD     #2, 4(6) ;GET ADDRESS TO BE TYPED
        CMP     (6)+, 2(6) ;ADD 2 TO THE ADDRESS
        BNE    36 ;IS IT "+2"?
        ADD    #2, TTY ;ADD 2 TO THE ADDRESS
        BIC    #1, TTY ;BACK UP TO AN EVEN BYTE
        MOV     TTY, 2(6) ;RESTORE ADDRESS
36:     MOV     (6)+, TTY ;RESTORE TTY
        RTI    ;RETURN
        .TYPE  0 ;CHARACTER TYPE LOCATION

```

```

RETURN: .ASCIZ (15)<12>
SPACE:  .ASCIZ " "
MSGADR: .ASCIZ (15)<12>"FIRST DJ11 ADDRESS: "

```

```

MSGVEC: .ASCIZ (15)<12>"VECTOR ADDRESS: "

```


Line	Code	Description	Unit	Rate	Quantity	Amount	Balance
101	00
102	00
103	00
104	00
105	00
106	00
107	00
108	00
109	00
110	00
111	00
112	00
113	00
114	00
115	00
116	00
117	00
118	00
119	00
120	00
121	00
122	00
123	00
124	00
125	00
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134	00
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136	00
137	00
138	00
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141	00
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143	00
144	00
145	00
146	00
147	00
148	00
149	00
150	00

