

DR11B

DIAGNOSTIC
MD-11-DZDRB-D

EP-DZDRB-D-DL-A
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FICHE 1 OF 1

NOV 1976
digital
MADE IN USA

This microfiche card contains a grid of frames, likely representing a diagnostic test sequence or data log. The frames are arranged in approximately 10 columns and 15 rows. Each frame contains text that is too small to read clearly but appears to be organized into columns and rows, possibly representing test results, error codes, or system status indicators. The text is printed in a light color against a dark background, typical of microfiche technology.

LOAD PROGRAM INTO MEMORY.
LOAD STARTING ADDRESS
PRESS START.
THE PROGRAM WILL LOOP, BELL WILL RING ONCE
PER PASS OF THE PROGRAM.

NOTE: IF SOFTWARE SWITCH REGISTER IS SELECTED THEN THE
FOLLOWING WILL BE PRINTED:

SWR= XXXXXX NEW=
(REFER TO SECTION 5.1 FOR OPERATOR OPTIONS)

5. DR11B OPERATING PROCEDURE
5.1 OPERATIONAL SWITCH SETTINGS

5.1.1 AT SA 200 ... THE INSTRUCTION AND LOGIC TEST.
WITH ALL SWITCHES DOWN THE PROGRAM WILL PRINT
OUT ON ERRORS AND CONTINUE IN TEST. (BELL
WILL RING AT COMPLETION OF A PASS)

5.1.2 SWITCH SETTINGS ARE

SW15 = 1 OR UP ... HALT ON ERROR
SW14 = 1 OR UP ... SCOPE LOOP
SW13 = 1 OR UP ... INHIBIT PRINTOUT
SW12 = 1 OR UP ... INHIBIT TRACE TRAP
SW11 = 1 OR UP ... INHIBIT ITERATIONS

5.1.3

IF THE DIAGNOSTIC IS RUN ON A CPU WITHOUT A SWITCH
REGISTER THEN A SOFTWARE SWITCH REGISTER IS USED WHICH ALLOWS
THE USER THE SAME SWITCH OPTIONS AS THE HARDWARE SWITCH REGISTER.
IF THE HARDWARE SWITCH REGISTER DOES NOT EXIST OR IF ONE DOES
AND IT CONTAINS ALL ONES (177777) THEN THE SOFTWARE SWITCH
REGISTER (LOC. 176) IS USED.

CONTROL:

THIS PROGRAM ALSO SUPPORTS THE DYNAMIC LOADING OF THE SOFTWARE SWITCH
REGISTER (LOC. 176) FROM THE TTY. THIS CAN BE ACCOMPLISHED BY
DOING THE FOLLOWING:

- 1) TYPE CONTROL G (<g>); THIS WILL ALLOW THE TTY TO ENTER DATA INTO
LOC. 176 AT SELECTED POINTS WITHIN THE PROGRAM.
- 2) THE MACHINE WILL THEN TYPE: SWR=XXXXXXXXNEW= (XXXXXX IS THE OCTAL CONTENTS
OF THE SOFTWARE SWITCH REGISTER.)
- 3) AFTER THE "NEW=" HAS BEEN TYPED THEN THE OPERATOR CAN DO ONE
OF THE FOLLOWING AT THE TTY:
 - A) TYPE A NUMBER TO BE LOADED INTO LOC. 176 FOLLOWED BY A <CR>.
(ONLY NUMBERS BETWEEN 0-7 WILL BE ACCEPTED AND ONLY 6 NUMBERS
WILL BE ALLOWED)

IF A <CR> IS THE FIRST KEY DEPRESSED THE SOFTWARE SWITCH REGISTER CONTENTS WILL NOT BE CHANGED.

B) IF A CONTROL U <↑U> IS DEPRESSED THEN THE PROGRAM WILL SEND YOU BACK TO STEP 2.

5.2. SUBROUTINE ABSTRACTS

BEGIN SA 200

5.2.1 SCOPE

THIS SUBROUTINE CALL IS PLACED BETWEEN EACH SUBTEST IN THE INSTRUCTION SECTION. IT RECORDS THE STARTING ADDRESS OF EACH SUB-TEST AS IT IS BEING ENTERED. IF A SCOPE LOOP IS REQUESTED, IT WILL JUMP TO THE START OF THE SUBTEST THAT THE SCOPE LOOP IS REQUESTED FOR. IF SCOPE LOOP IS NOT REQUESTED, THERE WILL BE EITHER A FIXED OR RANDOM NUMBER OF ITERATIONS ON THAT SUBTEST BEFORE THE NEXT SUBTEST IS ENTERED. SWITCH 11 ON A 1 INHIBITS ITERATION OF SUBTESTS.
NOTE: SUPPORTS ↑G ROUTINE FOR DYNAMIC LOADING OF SOFTWARE SWITCH REGISTER

5.2.2 HALT

IS A ROUTINE THAT PRINTS-OUT AN ADDRESS THAT TAGS THE FAILING SUBTEST, THE CP STATUS REGISTER AND THE DR11B STATUS REGISTER AT THE TIME OF FAILURE.
NOTE: SUPPORTS ↑G ROUTINE FOR DYNAMIC LOADING OF SOFTWARE SWITCH REGISTER

5.2.3 LODBUF

THE INBUF BUFFER IS LOADED WITH AN INCREMENTING PATTERN (0,1,2,3,...) BEGINNING AT THE STARTING ADDRESS OF INBUF. THE NUMBER OF WORDS LOADED IS DETERMINED BY THE CONTENTS OF BUFLN.

5.2.4 CHKBFF

THE CHKBUFF BUFFER IS LOADED WITH A MODIFIED INCREMENTING PATTERN (0,0,2,2,4,4,6,6,...) BEGINNING AT THE STARTING ADDRESS OF CHKBUFF. THE NUMBER OF WORDS LOADED IS DETERMINED BY THE CONTENTS OF BUFLN. THIS BUFFER IS LOADED ONLY FOR TESTS WHICH USE THE MAINTENANCE MODE OF THE DR11-B WHICH HAS A SPECIAL ALTERNATING DATI-DATO SEQUENCE OF OPERATION.

5.2.5 INTA

THE IE BIT IS CLEARED IN THE DRST THEN THE DRST IS CHECKED FOR THE ABSENCE OF AN ERROR AND THE PRESENCE OF READY. THE DRWC IS CHECKED TO SEE THAT IT IS EQUAL TO ZERO. THE CORRECT CONTENTS

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12.4 SLAVE COMPUTER, PUT THE HALT KEY UP AND PRESS CONTINUE.

12.5 MASTER COMPUTER, PUT THE HALT KEY PU AND PRESS CONTINUE.

13. DA11B OPERATING PROCEDURE

13.1 THE PROGRAM WILL LOOP AFTER STARTING AND PRINT OUT ANY ERRORS. THE PROGRAM WILL HALT AFTER NON RECOVERABLE ERRORS.

13.2 THE MAINT MODULE MUST BE IN A02/B02 AND THE THE DA11B MUST BE IN C04/D04 .

14. DA11B PROGRAM DISCRPTION

14.1 THE SLAVE COMPUTER STARTS BY ENTERING A BACKGROUND TO WAIT FOR AN INTERRUPT WITH THE INTERRUPT ENABLED. THE FIRST INTERRUPT THAT COMES SHOULD BE THE READY INTERRUPT SET UP WHEN THE MASTER HIT THE START KEY. THE INTERRUPT CAUSES THE SLAVE TO ENTER THE INTERRUPT SERVICE ROUTINE.

14.2 THE INTERRUPT SERVICE ROUTINE DETERMINS WHAT INTERRUPT CAME UP AND IF IT SHOULD HAVE COME UP. IF THE INTERRUPT WAS THE ONE EXPECTED THAN THE THAN THE PROGRAM GOES TO THE TO THE PROPER JOB ROUTINE, SJOBXX FOR SLAVE SERVICE AND JOBXX FOR THE MASTER ROUTINE.

14.3 THE NEXT THING THAT SHOULD HAPPEN IS THE MASTER SHOULD ISSUE AN INTERRUPT TO THE SLAVE THIS IS A SIGNAL FOR THE SLAVE TO ACCEPT THE WORD COUNT, OFFSET AND TWO CHECK SUM WORDS. THE SLAVE ACCEPTS A WORD AT A TIME FROM THE DATA BUFFER EACH TIME THE MASTER TOGGLES FUNCTION BIT 3. EACH TIME IT READS A WORD THE SLAVE SENDS THE WORD BACK TO THE MASTER FOR VERIFICATION.

14.4 AFTER THE SLAVE HAS RECIEVED ALL THE PARAMETERS IT SETS ITS DIRECTION BIT TO THE OPPOSIT DIRECTION AS THE MASTER AND STARTS THE NPR TRANSFER.

14.5 THE MASTER SETS UP THE TYPE OF TRANSFERS AND CHECKS THE DATA WHEN IT COMES BACK FROM THE SLAVE.

15. DA11B ERRORS

15.1 THE PC OF THE FAILING TEST, THE CP STATUS AND THE DR11B STATUS REGISTER WILL BE PRINTED AFTER AN ERROR.

15.2 THERE IS NO ERROR RECOVERY FOR THE DA11B TEST BECAUSE THE OTHER COMPUTER WILL GET OUT OF SINC WHEN AN ERROR OCCURS.

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002000
004000
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020000
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100000

000004

000000
000030
000032 011072
000340

```

%
      .ABS
      .MCALL .HEADER,STARS
*****
*****
:TITLE MAINDEC-11-DZDRB-D
: *COPYRIGHT (C) 1971,1976
: *DIGITAL EQUIPMENT CORP.
: *MAYNARD, MASS. 01754
: *
: *PROGRAM BY POMFRET, JONES, CONDON
: *
: *THIS PROGRAM WAS ASSEMBLED USING THE PDP-11 MAINDEC SYSMAC
: *PACKAGE (MAINDEC-11-DZQAC-C2), SEPT 14, 1976.
: *
$TN=1
$SWR=160000      ;;HALT ON ERROR, LOOP ON TEST, INHIBIT ERROR TYP0UT
*****
:      REVISED BY ALAN BOSTICK JUNE 1976
:      MODIFIED FOR SOFTWARE SWITCH REGISTER
:      INCLUDING DYNAMIC LOADING OF SWR
*****
*****
      NOP=000240
      SCOPE=TRAP
      HLT=EMT
      BIT0=000001
      BIT1=000002
      BIT2=000004
      BIT3=000010
      BIT4=000020
      BIT5=000040
      BIT6=000100
      BIT7=000200
      BIT8=000400
      BIT9=001000
      BIT10=002000
      BIT11=004000
      BIT12=010000
      BIT13=020000
      BIT14=040000
      BIT15=100000

      BUSERR=000004

;LOAD TRAP CATCHER INTO 0 THRU 777.

      .=0
      .=30
      PRINT
      340

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490 000034 000034
491 000034 011650
492 000036 000340
493 000176 000176
494 000176 000000
495 000200 000200
496 000200 012706 013566
497 000204 005077 000604
498 000210 005002
499 000212 012702 012433
500 000216 004767 012240
501 000222 012702 012403
502 000226 004767 012230
503 000232 000167 000634
504 001000 001000

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.=34
SCOPEC
340
.=176
SWREG: 0
.=200
MOV #BUFF,%6 ;SET UP STACK LIMIT
CLR @PSW
CLR %2
MOV #SHEAD,%2
JSR %7,TTOUT
MOV #SMAIN,%2
JSR %7,TTOUT
JMP SUSWR
.=1000

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```

*****
: START OF BACK-TO-BACK DR11-B
*****

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505 001000 000402
506 001002 000167 006276
507 001006 000167 006212
508 001012 177570
509 001014 177776
510 001016 172410
511 001020 172412
512 001022 172414
513 001024 172416
514 001026 000126
515 001030 000240
516 001032 000124
517 001034 052525
518 001036 173000
519 001040 013570
520 001042 014572
521 001044 000000
522 001046 000000
523 001050 000000
524 001052 000000
525 001054 000000
526 001056 177560
527 001060 177562
528 001062 177564
529 001064 177566
530 001066 000000
531 001070 000000
532 001072 013746 000006
533 001076 013746 000004
534 001102 012737 001122 000004
535 001110 022777 177777 177674
536 001116 001402
537 001120 000404

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```

MSTART: BR MSX ;MASTER START
SSTART: JMP SS1 ;SLAVE START
MSX: JMP MS1
SR: 177570
PSW: 177776
DRWC: 172410
DRBA: 172412
DRST: 172414
DRDB: 172416
DRVS: 126
DRINL: 240
DRINV: 124
NPR1: 52525
DIOMEM: 173000
INBUF: XINBUF
CHKBUF: XCHKBU
BUFLN: HALT
LENCHK: HALT
BRWAIT: HALT
WLEN: HALT
RDYCHK: HALT
TKS: 177560
TKB: 177562
TPS: 177564
TPB: 177566
FNCCNT: HALT
INBUF1: HALT

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SUSWR: MOV @#6,-(SP) ;SAVE VECTORS
MOV @#4,-(SP)
MOV #64,@#4 ;SET UP FOR TIMEOUT
CMP #-1,@SR ;REFERENCE HARDWARE SWITCH REGISTER
BEQ 65$
BR 66$

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546 001122 022626          54$:  CMP      (SP)+,(SP)+      ;ADJUST STACK
547 001124 012767 000176 177660 55$:  MOV      #SWREG,SR      ;POINT TO SOFTWARE SWITCH REG
548 001132 012637 000004          56$:  MOV      (SP)+,@#4      ;RESTORE VECTORS
549 001136 012637 000006          MOV      (SP)+,@#6
550 001142 022767 000176 177642  CMP      #SWREG,SR      ;IS SWREG USED
551 001150 001002          BNE      BEGIN
552 001152 004767 010646          JSR      PC,CNTLU      ;ALLOW SWREG TO BE LOADED
553 001156 012777 000340 177630 BEGIN:  MOV      #340,@PSW     ;PROC. AT LEVEL #7
554 001164 012767 001156 010542  MOV      #BEGIN,RETURN

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:*****
:      TEST 0 CAN ALL DR11-B REG BE ADDRESSED WITHOUT ERROR?
:*****

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561 001172 104400          SCOPE
562 001174 012767 001234 176602  MOV      #ERRA,BUSERR  ;BUS ERROR VECTOR TO ERRA
563 001202 010700          MOV      %7,%0         ;PC TO R0
564 001204 005277 177606          INC      @DRWC         ;ADDRESS DRWC
565 001210 010700          MOV      %7,%0         ;PC TO R0
566 001212 005277 177602          INC      @DRBA         ;ADDRESS DRBA
567 001216 010700          MOV      %7,%0         ;PC TO R0
568 001220 005077 177576          CLR      @DRST        ;ADDRESS DRST
569 001224 010700          MOV      %7,%0         ;PC TO R0
570 001226 005277 177572          INC      @DRDB        ;ADDRESS DRDB
571 001232 000401          BR       .+4           ;MADE IT - BRANCH OVER HALT
572 001234 104000          HLT
573 001236 012767 000006 176540  ERRA:  MOV      #6,BUSERR  ;BUS ERROR, R0 HAS PC OF ERROR
574 001244 104400          SCOPE                 ;RESTORE #6 TO BUS ERROR VECTOR

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:*****
:      TEST 1 DOES RESET CLEAR DRWC?
:*****

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583 001246 012767 000010 010454  MOV      #10,ICOUNT
584 001254 012777 177777 177534  MOV      #-1,@DRWC    ;ALL ONES TO DRWC
585 001262 004767 010464          JSR      %7,CKSWR
586 001266 000005          RESET          ;INIT
587 001270 005777 177522          TST      @DRWC        ;LOOKING FOR Z-BIT TO SET
588 001274 001401          BEQ      .+4         ;DID DRWC GET CLEARED?
589 001276 104000          HLT
590 001300 104400          SCOPE                 ;DRWC NOT CLEAR

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:*****
:      TEST2 DOES RESET CLEAR DRBA?
:*****

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599 001302 104400          SCOPE
600 001304 012777 177777 177506  MOV      #-1,@DRBA    ;ALL ONES TO DRBA
601 001312 004767 010434          JSR      %7,CKSWR

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602 001316 000005          RESET          ;INIT
603 001320 005777 177474  TST          @DRBA      ;LOOKING FOR Z-BIT TO SET
604 001324 001401          BEQ          .+4        ;DID DRBA GET CLEARED?
605 001326 104000          HLT                    ;DRBA NOT CLEAR
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614 001330 104400          SCOPE
615 001332 012767 004000 010370  MOV          #4000,ICOUNT
616 001340 012777 177777 177450  MOV          #-1,@DRWC    ;SET ALL BITS IN DRWC
617 001346 022777 177777 177442  CMP          #-1,@DRWC    ;LOOKING FOR Z-BIT TO SET
618 001354 001401          BEQ          .+4        ;SEE IF ALL BITS GOT SET
619 001356 104000          HLT                    ;ALL BITS AREN'T SET
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626 001360 104400          SCOPE
627 001362 012777 177776 177430  MOV          #-2,@DRBA    ;SET BITS 15-01 IN DRBA
628 001370 022777 177776 177422  CMP          #-2,@DRBA    ;LOOKING FOR Z-BIT TO SET
629 001376 001401          BEQ          .+4        ;SEE IF BITS 15-01 GOT SET
630 001400 104000          HLT                    ;BITS 15-01 AREN'T SET
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639 001402 104400          SCOPE
640 001404 052777 000002 177410  BIS          #BIT1,@DRST   ;SET FNCT1
641 001412 032777 000002 177402  BIT          #BIT1,@DRST   ;TEST FNCT1
642 001420 001001          BNE          .+4        ;IS IT SET?
643 001422 104000          HLT                    ;FNCT1 IS CLEAR
644 001424 042777 000002 177370  BIC          #BIT1,@DRST   ;CLEAR FNCT1
645 001432 032777 000002 177362  BIT          #BIT1,@DRST   ;TEST FNCT1
646 001440 001401          BEQ          .+4        ;WAS IT CLEAR
647 001442 104000          HLT                    ;FNCT1 WAS SET
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656 001444 104400          SCOPE
657 001446 052777 000004 177346  BIS          #BIT2,@DRST   ;SET FNCT2
658 001454 032777 000004 177340  BIT          #BIT2,@DRST   ;TEST FNCT2

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*****
TEST3 CAN ALL DRWC BITS BE SET?
*****

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*****
TEST4 CAN BITS 15-01 IN DRBA BE SET?
*****

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*****
TEST6 TEST THAT FNCT1 CAN BE SET AND CLEARED
*****

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*****
TEST7 TEST THAT FNCT2 CAN BE SET AND CLEARED
*****

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658 001462 001001
659 001464 104000
660 001466 042777 000004 177326
661 001474 032777 000004 177320
662 001502 001401
663 001504 104000

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BNE .+4 ;IS IT SET?
HLT ;FNCT2 IS CLEAR
BIC #BIT2,@DRST ;CLEAR FNCT2
BIT #BIT2,@DRST ;TEST FNCT2
BEQ .+4 ;WAS IT CLEAR?
HLT ;FNCT2 WAS SET

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*****
TEST10 TEST THAT FNCT3 CAN BE SET AND CLEARED
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664 001506 104400
665 001508 052777 000010 177304
666 001510 032777 000010 177276
667 001512 001001
668 001514 104000
669 001516 042777 000010 177264
670 001518 032777 000010 177256
671 001520 001401
672 001522 104000

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```

SCOPE
BIS #BIT3,@DRST ;SET FNCT3
BIT #BIT3,@DRST ;TEST FNCT3
BNE .+4 ;IS IT SET?
HLT ;FNCT3 IS CLEAR
BIC #BIT3,@DRST ;CLEAR FNCT3
BIT #BIT3,@DRST ;TEST FNCT3
BEQ .+4 ;WAS IT CLEAR?
HLT ;FNCT3 WAS SET

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*****
TEST11 TEST THAT XBA16 CAN BE SET AND CLEARED
*****

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```

673 001550 104400
674 001552 052777 000020 177242
675 001554 032777 000020 177234
676 001556 001001
677 001558 104000
678 001560 042777 000020 177222
679 001562 032777 000020 177214
680 001564 001401
681 001566 104000

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```

SCOPE
BIS #BIT4,@DRST ;SET XBA16
BIT #BIT4,@DRST ;TEST XBA16
BNE .+4 ;IS IT SET?
HLT ;XBA16 IS CLEAR
BIC #BIT4,@DRST ;CLEAR XBA16
BIT #BIT4,@DRST ;TEST XBA16
BEQ .+4 ;IS IT CLEAR?
HLT ;XBA16 WAS SET

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```

*****
TEST12 TEST THAT XBA17 CAN BE SET AND CLEARED
*****

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682 001610 104400
683 001612 052777 000040 177200
684 001614 032777 000040 177172
685 001616 001001
686 001618 104000
687 001620 042777 000020 177160
688 001622 032777 000020 177152
689 001624 001401
690 001626 104000

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SCOPE
BIS #BIT5,@DRST ;SET XBA17
BIT #BIT5,@DRST ;TEST XBA17
BNE .+4 ;IS IT SET?
HLT ;XBA17 IS CLEAR
BIC #BIT4,@DRST ;CLEAR XBA17
BIT #BIT4,@DRST ;TEST XBA17
BEQ .+4 ;IS IT CLEAR?
HLT ;XBA17 WAS SET

```

```

*****
TEST13 TEST THAT IE CAN BE SET AND CLEARED
*****

```

```

691 001630 104400
692 001632 052777 000100 177136
693 001634 032777 000100 177130

```

```

SCOPE
BIS #BIT6,@DRST ;SET IE
BIT #BIT6,@DRST ;TEST IE

```

```

714 001672 001001      BNE      .+4      : IS IT SET?
715 001674 104000      HLT      : IE IS CLEAR
716 001676 042777 000100 177116      BIC      #BIT6,DRST : CLEAR IE
717 001700 032777 000100 177110      BIT      #BIT6,DRST : TEST IE
718 001714 001401      BEQ      .+4      : IS IT CLEAR?
719 001714 104000      HLT      : IE WAS SET
720
721 *****
722 TEST14 TEST THAT CYCLE CAN BE SET AND CLEARED
723 *****
724 SCOPE
725 001716 104400      BIS      #BIT8,DRST : SET CYCLE
726 001718 052777 000400 177074      BIT      #BIT8,DRST : TEST CYCLE
727 001720 032777 000400 177066      BNE      .+4      : IS IT SET?
728 001722 001001      HLT      : CYCLE WAS CLEAR
729 001724 104000      BIC      #BIT8,DRST : CLEAR CYCLE
730 001726 042777 000400 177054      BIT      #BIT8,DRST : TEST CYCLE
731 001728 032777 000400 177046      BEQ      .+4      : IS IT CLEAR?
732 001730 001401      HLT      : CYCLE WAS SET
733
734 *****
735 TEST15 TEST THAT MAINT CAN BE SET AND CLEARED
736 *****
737 SCOPE
738 001760 104400      BIS      #BIT12,DRST : SET MAINT
739 001762 052777 010000 177032      BIT      #BIT12,DRST : TEST MAINT
740 001770 032777 010000 177024      BNE      .+4      : IS IT SET?
741 001776 001001      HLT      : MAINT WAS CLEAR
742 002000 104000      BIC      #BIT12,DRST : CLEAR MAINT
743 002002 042777 010000 177012      BIT      #BIT12,DRST : TEST MAINT
744 002010 032777 010000 177004      BEQ      .+4      : IS MAINT CLEAR?
745 002016 001401      HLT      : MAINT WAS SET
746
747 *****
748 TEST 16 TEST THAT ALL DRST R/W BITS CAN BE SET AND CLEARED
749 *****
750 SCOPE
751 002022 104400      BIS      #10576,DRST : SET FOLLOWING: MAINT(12), CYCLE(08), IE(06), XBA17(05),
752 002024 052777 010576 176770      : XBA16(04), FNCT3(03), FNCT2(02), FNCT1(01)
753 002032 032777 000002 176762      BIT      #BIT1,DRST : TEST FNCT1
754 002040 001001      BNE      .+4      : IS IT SET?
755 002042 104000      HLT      : FNCT1 IS CLEAR
756 002044 032777 000004 176750      BIT      #BIT2,DRST : TEST FNCT2
757 002052 001001      BNE      .+4      : IS IT SET?
758 002054 104000      HLT      : FNCT2 IS CLEAR
759 002056 032777 000010 176736      BIT      #BIT3,DRST : TEST FNCT3
760 002064 001001      BNE      .+4      : IS IT SET?
761 002066 104000      HLT      : FNCT3 IS CLEAR
762 002070 032777 000020 176724      BIT      #BIT4,DRST : TEST XBA16
763 002076 001001      BNE      .+4      : IS IT SET?
764 002100 104000      HLT      : XBA16 IS CLEAR
765 002102 032777 000040 176712      BIT      #BIT5,DRST : TEST XBA17
766 002110 001001      BNE      .+4      : IS IT SET?
767 002112 104000      HLT      : XBA17 IS CLEAR
768 002114 032777 000100 176700      BIT      #BIT6,DRST : TEST IE
769 002122 001001      BNE      .+4      : IS IT SET?

```

```

777 00000000 104000 HLT :IE IS CLEAR
777 00000000 032777 BIT #BIT8,DRST :TEST CYCLE
777 00000000 001001 .+4 :IS CYCLE SET?
777 00000000 104000 HLT :CYCLE IS CLEAR
777 00000000 032777 BIT #BIT12,DRST :TEST MAINT
777 00000000 001001 .+4 :IS MAINT SET?
777 00000000 104000 HLT :MAINT IS CLEAR
777 00000000 042777 BIC #10576,DRST :CLEAR ALL R/W BITS IN DRST
777 00000000 032777 BIT #BIT1,DRST :TEST FNCT1
777 00000000 001401 .+4 :IS FNCT1 CLEAR?
777 00000000 104000 HLT :FNCT1 IS SET
777 00000000 032777 BIT #BIT2,DRST :TEST FNCT2
777 00000000 001401 .+4 :IS FNCT2 CLEAR?
777 00000000 104000 HLT :FNCT2 IS SET
777 00000000 032777 BIT #BIT3,DRST :TEST FNCT3
777 00000000 001401 .+4 :IS FNCT3 CLEAR?
777 00000000 104000 HLT :FNCT3 IS SET
777 00000000 032777 BIT #BIT4,DRST :TEST XBA16
777 00000000 001401 .+4 :IS XBA16 CLEAR
777 00000000 104000 HLT :XBA16 IS SET
777 00000000 032777 BIT #BIT5,DRST :TEST XBA17
777 00000000 001401 .+4 :IS XBA17 CLEAR?
777 00000000 104000 HLT :XBA17 IS SET

777 00000000 032777 BIT #BIT6,DRST :TEST IE
777 00000000 001401 .+4 :IS IE CLEAR?
777 00000000 104000 HLT :IE IS SET
777 00000000 032777 BIT #BIT8,DRST :TEST CYCLE
777 00000000 001401 .+4 :IS CYCLE CLEAR?
777 00000000 104000 HLT :CYCLE IS SET
800 00000000 032777 BIT #BIT12,DRST :TEST MAINT
800 00000000 001401 .+4 :IS MAINT CLEAR?
800 00000000 104000 HLT :MAINT IS SET

*****
: TEST17 ALL R/W BITS IN DRST CAN BE SET AND RESET TO ZERO, THAT READY
: IS SET, NEX IS CLEAR, AND GO IS READ AS A 0.
*****
000 002300 104400 SCOPE
000 002302 012767 MOV #10,ICOUNT
000 002310 052777 BIS #10576,DRST :SET FOLLOWING: MAINT(12),CYCLE(09),IE(06),XBA17(05),
: XBA16(04),FNCT3(03),FNCT2(02),FNCT1(01)
000 002316 017701 MOV DRST,%1 :MOVE (DRST) TO R1
000 002322 052701 BIS #167201,%1 :SETS BITS IN R1 THAT WERE NOT SET IN DRST
000 002326 005201 INC %1 :R1 SHOULD GO FROM -1 TO ZERO
000 002330 001401 BEQ .+4 :WERE ALL DRST R/W BITS SET?
000 002332 104000 HLT :NOT ALL BITS WERE SET
000 002334 004767 JSR %7,CKSWR
000 002340 000005 RESET :CLEAR ALL DRST R/W BITS
000 002342 017701 MOV DRST,%1 :MOVE (DRST) TO R1
000 002346 042701 BIC #127200,%1 :CLEAR ALL BITS EXCEPT R/W BITS, NEX, AND GO
000 002352 001401 BEQ .+4 :SHOULD EQUAL ZERO
000 002354 104000 HLT :RESET DIDN'T LEAVE DRST AS IT SHOULD HAVE

*****
: TEST20 CAN DRWC HOLD ALTERNATE ONE'S AND ZERO'S

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003036 104400
003040 012777 000200 175746
003046 032777 000200 175746
003054 001010
003056 004767 006670
003062 000005
003064 032777 000200 175730
003072 001001
003074 104000
003076 012777 003116 175726 P4INV:
003104 052777 000100 175710
003112 000240
003114 104000
003116 005077 175700 P4INT:
003122 022626
003124 012777 000126 175700
```

```
::*****
:: TEST30 TEST THAT DR11-B DOES INTERRUPT WITH PROC AT LEVEL 4
::*****
SCOPE
MOV #200, @PSW ; STATUS AT LEVEL 4
BIT #BIT7, @DRST ; CHECK READY BIT
BNE P4INV ; IS IT SET?
JSR %7, CKSWR
RESET ; INIT TO SET READY
BIT #BIT7, @DRST ; SEE IF READY IS SET NOW
BNE .+4 ; IS IT SET
HLT ; READY CAN'T BE SET BY INIT
MOV #P4INT, @DRINV ; SET UP INT VECTOR
BIS #BIT6, @DRST ; SET IE
NOP
HLT ; DR11-B DIDN'T INTERRUPT
CLR @DRST ; CLEAR IE
CMP (%6)+, (%6)+ ; REPOSITION THE STACK AFTER AN INTERRUPT
MOV #126, @DRINV ; RESTORE INTERRUPT VECTOR
```

```
::*****
:: TEST31 TEST THAT FNCT BITS CONTROL DSTAT BITS (M968 MUST BE USED IN USER SLOTS)
::*****
```

```
003132 104400
003134 005077 175662
003140 032777 000016 175654
003146 001401
003150 104000
003152 052777 000002 175642
003160 032777 001000 175634
003166 001001
003170 104000
003172 032777 006000 175622
003200 001401
003202 104000
003204 005077 175612
003210 052777 000004 175604
003216 032777 002000 175576
003224 001001
003226 104000
003230 032777 005000 175564
003236 001401
003240 104000
003242 005077 175554
003246 052777 000010 175546
003254 032777 004000 175540
003262 001001
003264 104000
003266 032777 003000 175526
003274 001401
003276 104000
003300 005077 175516
```

```
SCOPE
CLR @DRST ; CLEAR FUNCTION BITS
BIT #16, @DRST ; CHECK FUNCTION BITS
BEQ .+4 ; FUNCTION BITS CLEAR?
HLT ; FUNCTION BITS NOT CLEAR
BIS #BIT1, @DRST ; SET FNCT1
BIT #BIT9, @DRST ; CHECK DSTAT C
BNE .+4 ; IS IT SET?
HLT ; DSTAT C IS CLEAR
BIT #6000, @DRST ; CHECK THAT DSTAT A AND DSTAT B ARE CLEAR
BEQ .+4 ; ARE THEY CLEAR?
HLT ; DSTAT A AND/OR DSTAT B IS SET
CLR @DRST ; CLEAR DRST
BIS #BIT2, @DRST ; SET FNCT2
BIT #BIT10, @DRST ; CHECK DSTAT B
BNE .+4 ; IS IT SET?
HLT ; DSTAT B IS CLEAR
BIT #5000, @DRST ; CHECK THAT DSTAT A AND DSTAT C ARE CLEAR
BEQ .+4 ; ARE THEY CLEAR?
HLT ; DSTAT A AND/OR DSTAT B IS SET
CLR @DRST ; CLEAR DRST
BIS #BIT3, @DRST ; SET FNCT3
BIT #BIT11, @DRST ; CHECK DSTAT A
BNE .+4 ; IS IT SET?
HLT ; DSTAT A IS CLEAR
BIT #3000, @DRST ; CHECK THAT DSTAT B AND DSTAT C ARE CLEAR
BEQ .+4 ; ARE THEY CLEAR?
HLT ; DSTAT B AND/OR DSTAT C IS SET
CLR @DRST ; CLR DRST
```

```
::*****
:: TEST 33 TEST FOR 1 DATI NPR TRANSFER (WITH M968 IN USER SLOTS)
::*****
```

```

994 003304 104400
995 003306 005777 175510
996 003312 100027
997 003314 032777 020000 175500
998 003322 001401
999 003324 104000
1000 003326 032777 040000 175466
1001 003334 001410
1002 003336 042777 040000 175456
1003 003344 032777 040000 175450
1004 003352 001401
1005 003354 104000
1006 003356 005077 175436
1007 003362 005777 175434
1008 003366 001401
1009 003370 104000
1010 003372 012777 177777 175416
1011 003400 012777 001034 175412
1012 003406 005077 175412
1013 003412 012767 052525 175414
1014 003420 012777 003464 175404
1015 003426 012777 000005 175372
1016 003434 005077 175354
1017 003440 012777 000101 175354
1018 003446 005067 000002
1019 003452 005227 000001
1020 003456 001375
1021 003460 104000
1022 003462 000424
1023 003464 004767 003312
1024 003470 005777 175322
1025 003474 001401
1026 003476 104000
1027 003500 022777 001036 175312
1028 003506 001401
1029 003510 104000
1030 003512 022777 052525 175304
1031 003520 001401
1032 003522 104000
1033 003524 004767 003162
1034 003530 022626
1035 003532 000403
1036 003534 005077 175262
1037 003540 000662
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1041 003542 104400
1042 003544 012777 177777 175244
1043 003552 012777 001034 175240
1044 003560 005067 175250
1045 003564 012777 052525 175232
1046 003572 012777 003636 175232
1047 003600 016777 175224 175220
1048 003606 005077 175202
1049 003612 012777 000103 175202

```

SCOPE

TNPR1: TST @DRST ;CHECK ERROR BIT
BPL NPRRDY ;IS IT CLEAR?
BIT #BIT13,@DRST ;CHECK ATTN
BEQ .+4 ;IS ATTN CLEAR
HLT ;ATTN IS SET
BIT #BIT14,@DRST ;CHECK NEX
BEQ N1413 ;IS NEX CLEAR?
BIC #BIT14,@DRST ;TRY TO CLEAR NEX
BIT #BIT14,@DRST ;CHECK AGAIN
BEQ .+4 ;NEX STILL SET
HLT ;NEX CAN'T BE CLEARED BY MOVING A 0 TO IT
N1413: CLR @DRBA ;TRY TO CLEAR BAOF
TST @DRST ;CHECK ERROR BIT AGAIN
BEQ .+4 ;IS IT CLEAR
HLT ;ERROR CAUSED BY SOMETHING OTHER THAN NEX,ATTN, OR BAOF
NPRRDY: MOV #-1,@DRWC ;SET UP FOR 1 TRANSFER
MOV #NPR1,@DRBA ;TRANSFER FROM BUS ADDRESS IN NPR1
CLR @DRDB ;GET READY TO RECEIVE DATA
MOV #52525,NPR1 ;SET UP TRANSFER DATA
MOV #INTB,@DRINV ;INTERRUPT VECTOR TO INTB
MOV #5,@DRVS ;INTERRUPT PRIORITY TO LEVEL 5
CLR @PSW ;LET THE DR11-B INTERRUPT
MOV #101,@DRST ;IE AND DO TO DRST
CLR 1\$+2 ;WAIT FOR NPR AND INTERRUPT
1\$: INC #1
BNE 1\$
HLT ;NO DR11-B INTERRUPT
BR T33CLR ;CLEAR IE
INTB: JSR %7,ERRCHK ;TEST DRWC
TST @DRWC ;IS DRWC EQUAL TO ZERO?
BEQ .+4 ;DRWC NOT EQUAL TO ZERO
HLT ;COMPARE CORRECT DRBA WITH DRBA
CMP #NPR1+2,@DRBA ;IS THE DRBA CORRECT?
BEQ .+4 ;DRBA IS WRONG
HLT ;CHECK FOR CORRECT DATA
CMP #52525,@DRDB ;DATA GET TRANSFERRED?
BEQ .+4 ;BAD DATA IN DRDB
HLT
JSR %7,NORMAL
CMP (%6)+,(%6)+ ;RESTORE STACK
BR TNPRO ;GO TO NEXT TEST (NPR OUT)
T33CLR: CLR @DRST ;CLEAR IE
BR TNPR1 ;TRY TEST AGAIN

: TEST 34 TEST FOR 1 DATO NPR TRANSFER (WITH M968 IN USER SLOTS)

TNPRO: SCOPE
MOV #-1,@DRWC ;SET UP FOR 1 TRANSFER
MOV #NPR1,@DRBA ;TRANSFER TO BUS ADDRESS IN NPR1
CLR NPR1 ;GET READY TO RECEIVE DATA
MOV #52525,@DRDB ;SET UP TO TRANSFER DATA
MOV #INTC,@DRINV ;INTERRUPT VECTOR TO INTC
MOV DRINL,@DRVS ;INTERRUPT STATUS TO LEVEL DRINL
CLR @PSW ;PROC STATUS TO ZERO
MOV #103,@DRST ;IE, FNCT1(C1 CONTROL), AND DO TO DRST

```

1050 003620 005067 000002          CLR      15+2          ;WAIT FOR NPR AND INTER
1051 003624 005227 000001          IS:      INC      #1
1052 003630 001375          BNE      15
1053 003632 104000          HLT
1054 003634 000424          BR      T34CLR          ;NO DR11-B INTERRUPT
1055 003636 004767 003140          INTC:   JSR      %7,ERRCHK          ;CLEAR IE
1056 003642 005777 175150          TST      @DRWC          ;TEST DRWC
1057 003646 001401          BEQ      .+4          ;IS DRWC EQUAL TO ZERO?
1058 003650 104000          HLT          ;DRWC EQUAL TO ZERO
1059 003652 022777 001036 175140          CMP      #NPR1+2,@DRBA          ;COMPARE CORRECT DRBA WITH DRBA
1060 003660 001401          BEQ      .+4          ;IS THE DRBA CORRECT?
1061 003662 104000          HLT          ;DRBA IS WRONG
1062
1063 003664 026727 175144 052525          CMP      NPR1,#52525          ;CHECK FOR CORRECT DATA
1064 003672 001401          BEQ      .+4          ;CORRECT DATA TRANSFERRED?
1065 003674 104000          HLT          ;BAD DATA
1066 003676 004767 003010          JSR      %7,NORMAL
1067 003702 022626          CMP      (%6)+,(%6)+          ;RESTORE STACK
1068 003704 000403          BR      T35          ;GO TO NEXT TEST
1069 003706 005077 175110          T34CLR: CLR      @DRST          ;CLEAR IE
1070 003712 000713          BR      TNPRO          ;TRY TEST AGAIN
1071
1072          ;:*****
1073          ;:TEST 35 STRING OF 10 DATI'S (WITH M968 IN USER SLOTS)
1074          ;:*****
1075 003714 104400          T35:    SCOPE
1076 003716 012767 000020 175120          MOV      #20,BUFLEN          ;LENGTH OF BUFFER=20
1077 003724 004767 002524          JSR      %7,LODBUF          ;LOAD THE BUFFER WITH INCREMENTING PATTERN
1078 003730 006267 175110          ASR      BUFLEN          ;BUFLEN=10
1079 003734 016767 175104 175110          MOV      BUFLEN,WLEN          ;PREPARE NUMBER FOR DRWC
1080 003742 005467 175104          NEG      WLEN          ;2'S COMPLEMENT OF BUFLEN
1081 003746 016777 175100 175042          MOV      WLEN,@DRWC          ;SET UP DRWC
1082 003754 016777 175060 175036          MOV      INBUF,@DRBA          ;SET UP DRBA
1083 003762 012777 177777 175034          MOV      #-1,@DRDB          ;MAINT AIDE
1084 003770 012777 006556 175034          MOV      #INTA,@DRINV          ;INT VECTOR TO INTA
1085 003776 016777 175026 175022          MOV      DRINL,@DRVS          ;INT VECTOR TO PRIORITY DRINL
1086 004004 005077 175004          CLR      @PSW          ;LET THE DR11-B INTERRUPT
1087 004010 012777 000101 175004          MOV      #101,@DRST          ;IE AND DO TO DRST
1088 004016 000777          BR          ;WAIT FOR INTERRUPT
1089 004020 022777 000007 174776          CMP      #7,@DRDB          ;CHECK THAT WORD #10 OF INBUF IS IN DRBA
1090 004026 001401          BEQ      .+4          ;IS IT?
1091 004030 104000          HLT          ;BAD DATA IN DRDB
1092
1093          ;:*****
1094          ;:TEST 36 STRING OF 10 DATO'S (WITH M968 IN USER SLOTS)
1095          ;:*****
1096 004032 104400          SCOPE
1097 004034 012767 000020 175002          MOV      #20,BUFLEN          ;LENGTH OF BUFFER=20
1098 004042 004767 002406          JSR      %7,LODBUF          ;LOAD THE BUFFER WITH INCREMENTING PATTERN
1099 004046 006267 174772          ASR      BUFLEN          ;BUFLEN=10
1100 004052 016767 174766 174772          MOV      BUFLEN,WLEN          ;PREPARE NUMBER FOR DRWC
1101 004060 005467 174766          NEG      WLEN          ;2'S COMPLEMENT OF BUFLEN
1102 004064 016777 174762 174724          MOV      WLEN,@DRWC          ;SET UP DRWC
1103 004072 016777 174742 174720          MOV      INBUF,@DRBA          ;SET UP DRBA
1104 004100 012777 052525 174716          MOV      #52525,@DRDB          ;SET UP DRDB
1105 004106 012777 006556 174716          MOV      #INTA,@DRINV          ;INTERRUPT VECTOR TO INTA

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1106 004114 016777 174710 174704 MOV DRINL,DRVS ;INTERRUPT VECTOR TO PRIORITY DRINL
1107 004122 005077 174666 CLR DRPSW ;LET THE DR11-B INTERRUPT
1108 004126 012777 000103 174666 MOV #103,DRST ;IE, FNCT1(C1 CONTROL), AND DO TO DRST
1109 004134 000777 BR ;WAIT FOR INTERRUPT
1110 004136 004767 002572 JSR %7,DATOCK ;CHECK INBUF
1111
1112 ;*****
1113 ; TEST 37 STRING OF 200 DATI'S
1114 ;*****
1115 004142 104400 SCOPE
1116 004144 012767 000200 174672 MOV #200,BUFLEN ;LENGTH OF BUFFER=200
1117 004152 004767 002276 JSR %7,LODBUF ;LOAD THE BUFFER WITH INCREMENTING PATTERN
1118 004156 016767 174662 174666 MOV BUFLN,WCLN ;PREPARE NUMBER FOR DRWC
1119 004164 005467 174662 NEG WCLN ;2'S COMPLEMENT OF BUFLN
1120 004170 016777 174656 174620 MOV WCLN,DRWC ;SET UP DRWC
1121 004176 016777 174636 174614 MOV INBUF,DRBA ;SET UP DRBA
1122 004204 012777 177777 174612 MOV #-1,DRDB ;MAINT AIDE
1123 004212 012777 006556 174612 MOV #INTA,DRINV ;INT VECTOR TO INTA
1124 004220 016777 174604 174600 MOV DRINL,DRVS ;INT VECTOR TO PRIORITY DRINL
1125 004226 005077 174562 CLR DRPSW ;LET THE DR11-B INTERRUPT
1126 004232 012777 000101 174562 MOV #101,DRST ;IE AND DO TO DRST
1127 004240 000777 BR ;WAIT FOR INTERRUPT
1128 004242 022777 000177 174554 CMP #177,DRDB ;CHECK THAT WORD #200 OF INBUF IS IN DRBA
1129 004250 001401 BEQ .+4 ;IS IT?
1130 004252 104000 HLT ;BAD DATA IN DRDB
1131
1132 ;*****
1133 ; TEST 40 STRING OR 200 DATO'S
1134 ;*****
1135 004254 104400 SCOPE
1136 004256 012767 000201 174560 MOV #201,BUFLEN ;LENGTH OF BUFFER=201
1137 004264 004767 002164 JSR %7,LODBUF ;LOAD THE BUFFER WITH INCREMENTING PATTERN
1138 004270 005367 174550 DEC BUFLN ;BUFLN=200
1139 004274 016767 174544 174550 MOV BUFLN,WCLN ;PREPARE NUMBER FOR DRWC
1140 004302 005467 174544 NEG WCLN ;2'S COMPLEMENT OF BUFLN
1141 004306 016777 174540 174502 MOV WCLN,DRWC ;SET UP DRWC
1142 004314 016777 174520 174476 MOV INBUF,DRBA ;SET UP DRBA
1143 004322 012777 052525 174474 MOV #52525,DRDB ;SET UP DRDB
1144 004330 012777 006556 174474 MOV #INTA,DRINV ;INTERRUPT VECTOR TO INTA
1145 004336 016777 174466 174462 MOV DRINL,DRVS ;INTERRUPT VECTOR TO PRIORITY DRINL
1146 004344 005077 174444 CLR DRPSW ;LET THE DR11-B INTERRUPT
1147 004350 012777 000103 174444 MOV #103,DRST ;IE, FNCT1, AND DO TO DRST
1148 004356 000777 BR ;WAIT FOR INTERRUPT
1149 004360 004767 002350 JSR %7,DATOCK ;CHECK INBUF
1150
1151 ;*****
1152 ; TEST 42 TEST THAT DOING A DATO TO THE DIODE MEMORY CAUSES NEX
1153 ;*****
1154 004364 104400 SCOPE
1155 004366 012777 177776 174422 MOV #-2,DRWC ;SET UP DRWC
1156 004374 016777 174436 174416 MOV DIOMEM,DRBA ;SET UP DRBA
1157 004402 012777 004436 174422 MOV #NEXCHK,DRINV ;INTERRUPT VECTOR TO NEXCHK
1158 004410 016777 174414 174410 MOV DRINL,DRVS ;INTERRUPT STATUS TO LEVEL DRINL
1159 004416 005077 174372 CLR DRPSW ;LET THE DR11-B INTERRUPT
1160 004422 012777 000163 174372 MOV #163,DRST ;IE, FNCT1, XBA17, XBA16, AND GO TO DRST
1161 004430 005237 177560 INC #177560 ;WAIT FOR INTERRUPT
1162 004434 104000 HLT ;NO DR11-B INTERRUPT

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1162 004436 005777 174360 NEXCHK: TST @DRST ;TEST DRST
1163 004442 001001 BNE .+4 ;ERROR SET?
1164 004444 104000 HLT ;ERROR NOT SET
1165 004446 105777 174350 TSTB @DRST ;TEST FOR READY
1166 004452 001001 BNE .+4 ;READY SET?
1167 004454 104000 HLT ;READY ISN'T SET
1168 004456 032777 040000 174336 BIT #BIT14,@DRST ;CHECK NEX
1169 004464 001001 BNE .+4 ;NEX SET?
1170 004466 104000 HLT ;NEX IS CLEAR
1171 004470 022626 CMP (%B)+,(%B)+ ;RESTORE THE STACK
1172 004472 004767 002214 JSR %7,NORMAL
1173
1174 ;*****
1175 ; TEST 43 TEST THAT BAOF FORCES ERROR AND READY AND THAT BAOF IS
1176 ; CLEARED BY CLEARING THE DRBA OR A RESET
1177 ;*****
1178 004476 104400 SCOPE
1179 004500 012767 000010 005222 MOV #10,ICOUNT
1180 004506 012777 177760 174302 MOV #-20,@DRWC ;SET UP DRWC
1181 004514 012777 177776 174276 MOV #-2,@DRBA ;SET UP DRBA FOR PROC STATUS ADDRESS
1182 004522 012777 004556 174302 MOV #BAOFCK,@DRINV ;INTERRUPT VECTOR TO BAOFCK
1183 004530 016777 174274 174270 MOV DRINL,@DRVS ;INTERRUPT STATUS TO LEVEL DRINL
1184 004536 005077 174252 CLR @PSW ;LET THE DR11-B INTERRUPT
1185 004542 012777 000163 174252 MOV #163,@DRST ;I.E. FNCT1, XBA17, XBA16, AND GO TO DRST
1186 004550 005237 177560 INC @#177560 ;WAIT FOR INTERRUPT
1187 004554 104000 HLT ;NO DR11-B INTERRUPT
1188 004556 022626 BAOFCK: CMP (%B)+,(%B)+ ;RESTORE THE STACK
1189 004560 005777 174236 TST @DRST ;TEST DRST
1190 004564 100401 BMI .+4 ;ERROR SET?
1191 004566 104000 HLT ;ERROR NOT SET
1192 004570 105777 174226 TSTB @DRST ;TEST FOR READY
1193 004574 100401 BMI .+4 ;READY SET?
1194 004576 104000 HLT ;READY ISN'T SET
1195 004600 042777 040000 174214 BIC #BIT14,@DRST ;CLEAR NEX
1196 004606 032777 060000 174206 BIT #60000,@DRST ;CHECK NEX AND ATTN
1197 004614 001401 BEQ .+4 ;ARE THEY CLEAR?
1198 004616 104000 HLT ;NEX AND/OR ATTN IS SET
1199 004620 005777 174176 TST @DRST ;TEST FOR ERROR
1200 004624 100401 BMI .+4 ;IS ERROR SET?
1201 004626 104000 HLT ;ERROR IS CLEAR
1202 004630 005077 174164 CLR @DRBA ;CLEAR BAOF
1203 004634 005777 174162 TST @DRST ;CHECK ERROR
1204 004640 100001 BPL .+4 ;SHOULD BE CLEAR
1205 004642 104000 HLT ;CLEARING DRBA DIDN'T CLEAR BAOF
1206
1207 004644 012777 177776 174146 MOV #-2,@DRBA ;SET UP DRBA FOR PROC STATUS ADDRESS
1208 004652 012777 004706 174152 MOV #BAOCK1,@DRINV ;INTERRUPT VECTOR TO BAOCK1
1209 004660 016777 174144 174140 MOV DRINL,@DRVS ;INTERRUPT STATUS TO LEVEL DRINL
1210 004666 005077 174122 CLR @PSW ;LET THE DR11-B INTERRUPT
1211 004672 012777 000163 174122 MOV #163,@DRST ;I.E., XBA17,XBA16, FNCT1, AND GO TO DRST
1212 004700 005237 177560 INC @#177560 ;WAIT FOR INTERRUPT
1213 004704 104000 HLT ;NO DR11-B INTERRUPT
1214 004706 022626 BAOCK1: CMP (%B)+,(%B)+ ;RESTORE THE STACK
1215 004710 005777 174106 TST @DRST ;TEST DRST
1216 004714 100401 BMI .+4 ;ERROR SET?
1217 004716 104000 HLT ;ERROR NOT SET

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1218 004720 105777 174076 TSTB QDRST :TEST FOR READY
1219 004724 100401 BMI .+4 :READY SET?
1220 004726 104000 HLT :READY ISN'T SET
1221 004730 042777 040000 174064 BIC #BIT14,QDRST :CLEAR NEX
1222 004736 032777 060000 174056 BIT #60000,QDRST :CHECK NEX AND ATTN
1223 004744 001401 BEQ .+4 :ARE THEY CLEAR?
1224 004746 104000 HLT :NEX AND/OR ATTN IS SET
1225 004750 005777 174046 TST QDRST :TEST FOR ERROR
1226 004754 100401 BMI .+4 :IS ERROR SET?
1227 004756 104000 HLT :ERROR IS CLEAR
1228 004760 004767 004766 JSR %7,CKSWR
1229 004764 000005 RESET :INIT
1230 004766 005777 174030 TST QDRST :CHECK ERROR
1231 004772 100001 BPL .+4 :SHOULD BE CLEAR
1232 004774 104000 HLT :RESET DIDN'T CLEAR BAOF
1233 004776 004767 001710 JSR %7,NORMAL
1234
1235
1236 :*****
1237 :TEST 44 TEST THAT RESET CLEARS DRDB
1238 :*****
1238 005002 104400 SCOPE
1239 005004 012767 000010 004716 MOV #10,ICOUNT
1240 005012 012777 177777 174004 MOV #-1,QDRDB :ALL ONES TO DRDB
1241 005020 004767 004726 JSR %7,CKSWR
1242 005024 000005 RESET :INIT
1243 005026 005777 173772 TST QDRDB :LOOKING FOR Z-BIT TO SET
1244 005032 001401 BEQ .+4 :DID DRDB GET CLEARED?
1245 005034 104000 HLT :DRDB NOT CLEAR
1246
1247
1248 :*****
1249 :TEST 45 TEST THAT ALL DRDB BITS CAN BE SET
1250 :*****
1250 005036 104400 SCOPE
1251 005040 012767 004000 004662 MOV #4000,ICOUNT
1252 005046 012777 177777 173750 MOV #-1,QDRDB :SET ALL BITS IN DRDB
1253 005054 022777 177777 173742 CMP #-1,QDRDB :LOOKING FOR Z-BIT TO SET
1254 005062 001401 BEQ .+4 :SEE IF ALL BITS GOT SET
1255 005064 104000 HLT :ALL DRDB BITS AREN'T SET
1256
1257
1258 :*****
1259 :TEST 46 TEST THAT DRDB CAN HOLD ALTERNATE ONE'S AND ZERO'S
1260 :*****
1260 005066 104400 SCOPE
1261 005070 012777 052525 173726 MOV #052525,QDRDB :ALT 0'S AND 1'S TO DRDB
1262 005076 022777 052525 173720 CMP #052525,QDRDB :LOOKING FOR Z-BIT TO SET
1263 005104 001401 BEQ .+4 :DOES DRDB HAVE THE CORRECT PATTERN?
1264 005106 104000 HLT :DRDB IS WRONG
1265 005110 012777 125252 173706 MOV #125252,QDRDB :ALT 1'S AND 0'S TO DRDB
1266 005116 022777 125252 173700 CMP #125252,QDRDB :LOOKING FOR Z-BIT TO SET
1267 005124 001401 BEQ .+4 :DOES DRDB HAVE THE CORRECT PATTERN
1268 005126 104000 HLT :DRDB IS WRONG
1269
1270 :*****
1271 :TEST 47 INCREMENTING PATTERN TO WRAP-AROUND IN DRDB
1272 :*****
1273 005130 104400 SCOPE

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1274 005132 005067 004572          CLR      ICOUNT
1275 005136 005001          CLR      %1          ;SET-UP
1276 005140 005077 173660        CLR      @DRDB      ;SET-UP
1277 005144 020177 173654        INCDB:  CMP      %1,@DRDB ;SEE IF THEY ARE EQUAL
1278 005150 001401          BEQ      .+4         ;ARE THEY EQUAL?
1279 005152 104000          HLT                     ;THEY'RE NOT EQUAL
1280 005154 005277 173644        INC      @DRDB      ;GET NEXT NUMBER
1281 005160 005201          INC      %1          ;GET NEXT NUMBER
1282 005162 001370          BNE      INCDB       ;DONE WITH TEST? IF NOT CONTINUE
1283
1284
1285 ;*****
1286 ;TEST 50 TEST THAT RESET SETS READY AND CLEARS ALL OTHER
1287 ;DRST BITS (WITH M968 INSERTED)
1288 ;*****
1289 005164 104400          SCOPE
1290 005166 004767 004560        JSR      %7,CKSWR
1291 005172 000005          RESET
1292 005174 032777 000200 173620  BIT      #BIT7,@DRST ;INIT
1293 005202 001001          BNE      .+4         ;CHECK DRST
1294 005204 104000          HLT                     ;IS READY SET?
1295 005206 032777 177577 173606  BIT      #177577,@DRST ;READY IS CLEAR
1296 005214 001401          BEQ      .+4         ;CHECK DRST
1297 005216 104000          HLT                     ;ARE THEY ALL CLEAR?
1298 ;*****
1299 ;TEST 51 TEST THAT BA00 READS AS A ZERO WITH MAINT BOARD INSERTED
1300 ;*****
1301 005220 104400          SCOPE
1302 005222 012767 004000 004500  MOV      #4000,ICOUNT
1303 005230 032777 000001 173562  BIT      #BIT0,@DRBA ;TEST BIT 0 OF DRBA
1304 005236 001401          BEQ      .+4         ;IS IT CLEAR?
1305 005240 104000          HLT                     ;BA00 IS SET
1306
1307
1308
1309 ;*****
1310 ;TEST 52 TEST THAT GO CLEARS READY
1311 ;*****
1312 005242 104400          SCOPE
1313 005244 012767 004000 004456  MOV      #4000,ICOUNT
1314 005252 012777 177600 173536  MOV      #-200,@DRWC ;SET-UP DRWC
1315 005260 016777 173554 173532  MOV      INBUF,@DRBA ;SET-UP DRBA
1316 005266 105777 173530          TSTB     @DRST      ;CHECK READY
1317 005272 100401          BMI      .+4         ;IS READY SET?
1318 005274 104000          HLT                     ;READY IS CLEAR
1319 005276 012777 000011 173516  MOV      #11,@DRST ;FNCT3 (NON-BURST) AND GO TO DRST
1320 005304 105777 173512          TSTB     @DRST      ;CHECK READY
1321 005310 100001          BPL      .+4         ;IS READY CLEAR?
1322 005312 104000          HLT                     ;READY IS STILL SET
1323 005314 005067 173534          CLR      RDYCHK      ;CLEAR READY CHECK
1324 005320 105777 173476        TSTRDY: TSTB     @DRST ;CHECK READY
1325 005324 100406          BMI      DONE        ;CHECK READY
1326 005326 062767 000004 173520  ADD      #4,RDYCHK    ;IF SET GO TO DONE
1327 005334 100401          BMI      .+4         ;CHECKING TIME FOR READY TO BE SET
1328 005336 000770          BR       TSTRDY      ;IF RDYCHK GETS NEGATIVE IT TOOK TOO LONG
1329 005340 104000          HLT                     ;CHECK AGAIN
;READY GOT CLEARED BUT NEVER SET AGAIN

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1330 005342 000240      DONE:  NOP                      ;GO TO NEXT TEST
1331                    ;:*****
1332                    ;:TEST 55 TEST THAT GIVING A DO WITHOUT CLEARING A PREVIOUS ERROR
1333                    ;:CAUSES ANOTHER INTERRUPT
1334                    ;:*****
1335 005344 104400      SCOPE
1336 005346 012777 177760 173442      MOV      #-20,DRWC      ;SET-UP DRWC
1337 005354 016777 173456 173436      MOV      DIOMEM,DRBA   ;SET-UP DRBA
1338 005362 012777 005416 173442      MOV      #ERRDO,DRINV  ;INTERRUPT VECTOR TO ERRDO
1339 005370 012777 000200 173430      MOV      #200,DRVS     ;INTERRUPT STATUS TO LEVEL 4
1340 005376 005077 173412              CLR      DRPSW         ;LET THE DR11-B INTERRUPT
1341 005402 012777 000163 173412      MOV      #163,DRST    ;IE, XBA17,XBA16, FNCT1 AND GO TO DRST
1342 005410 005277 173442              INC      DRTKS        ;WAIT FOR INTERRUPT
1343 005414 104000              HLT                      ;NO DR11-B INTERRUPT
1344 005416 005777 173400      ERRDO:  TST      DRST   ;TEST DRST
1345 005422 100401              BMI      .+4          ;ERROR SET?
1346 005424 104000              HLT                      ;ERROR IS CLEAR - SHOULD HAVE NEX
1347 005426 012777 005474 173376      MOV      #ERRDO1,DRINV ;INTERRUPT VECTOR TO ERRDO1
1348 005434 005077 173360              CLR      DRBA         ;PREVENT CAUSING ANOTHER ERROR
1349 005440 042777 000062 173354      BIC      #62,DRST     ;CLEAR XBA17, XBA16, AND FNCT1
1350 005446 012777 177777 173342      MOV      #-1,DRWC     ;SET-UP DRWC
1351 005454 005277 173342              INC      DRST         ;DO TO DRST
1352 005460 005067 000002              CLR      DRPSW+2
1353 005464 005227 000001      1$:      INC      #1
1354 005470 001375              BNE      1$
1355 005472 104000              HLT
1356 005474 005777 173322      ERRDO1: TST      DRST   ;NO DR11-B INTERRUPT
1357 005500 100401              BMI      .+4          ;CHECK ERROR
1358 005502 104000              HLT                      ;ERROR SET?
1359                    ;:ERROR IS CLEAR - SHOULD BE SET BECAUSE
1360 005504 062706 000010              ADD      #10,%6       ;PREVIOUS ERROR WAS NOT CLEARED
1361 005510 004767 001176              JSR      %7,NORMAL    ;REPOSITION THE STACK
1362
1363                    ;:*****
1364                    ;:TEST 56 STRING OF 200 DATI'S NON-BURST MODE
1365                    ;:*****
1366 005514 104400      SCOPE
1367 005516 012767 000200 173320      MOV      #200,BUFLEN   ;LENGTH OF BUFFER=200
1368 005524 004767 000724              JSR      %7,LODBUF    ;LOAD THE BUFFER WITH INCREMENTING PATTERN
1369 005530 016767 173310 173314      MOV      BUFLN,WCLN   ;PREPARE NUMBER FOR DRWC
1370 005536 005467 173310              NEG      WCLN         ;2'S COMPLEMENT OF BUFLN
1371 005542 016777 173304 173246      MOV      WCLN,DRWC    ;SET-UP DRWC
1372 005550 016777 173264 173242      MOV      INBUF,DRBA   ;SET-UP DRBA
1373 005556 012777 177777 173240      MOV      #-1,DRDB     ;MAINT AIDE
1374 005564 012777 006556 173240      MOV      #INTA,DRINV  ;INT VECTOR TO INTA
1375 005572 016777 173232 173226      MOV      DRINL,DRVS   ;INT VECTOR TO PRIORITY DRINL
1376 005600 005077 173210              CLR      DRPSW         ;LET THE DR11-B INTERRUPT
1377 005604 012777 000111 173210      MOV      #111,DRST    ;IE, FNCT3, AND DO TO DRST
1378 005612 005267 173232              INC      BRWAIT       ;USE A WAIT OR BR. INSTRUCTION
1379 005616 032767 000001 173224      BIT      #BIT0,BRWAIT ;SEE WHICH ONE
1380 005624 001403              BEQ      DATINB      ;BIT 0 CLEAR=BR.
1381 005626 000001              WAIT                      ;WAIT FOR INTERRUPT
1382 005630 000240              NOP
1383 005632 000401      DATINB: BR      .+4
1384 005634 000777              BR
1385 005636 022777 000177 173160      CMP      #177,DRDB   ;CHECK THAT WORD #200 OF INBUF IS IN DRBA

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1386 005644 001401          BEQ      .+4          ;IS IT?
1387 005646 104000          HLT      ;BAD DATA IN DRDB
1388
1389
1390
1391
1392 005650 104400          ;*****
1393 005652 012767 000201 173164  MOV     #201,BUFLEN ;LENGTH OF BUFFER=201
1394 005660 004767 000570          JSR     %7,LODBUF   ;LOAD THE BUFFER WITH INCREMENTING PATTERN
1395 005664 005367 173154          DEC     BUFLEN     ;BUFLEN=200
1396 005670 016767 173150 173154  MOV     BUFLEN,WLEN ;PREPARE NUMBER FOR DRWC
1397 005676 005467 173150          NEG     WLEN       ;2'S COMPLEMENT OF BUFLEN
1398 005702 016777 173144 173106  MOV     WLEN,DRWC  ;SET UP DRWC
1399 005710 016777 173124 173102  MOV     INBUF,DRBA ;SET UP DRBA
1400 005716 012777 052525 173100  MOV     #52525,DRDB ;SET UP DRDB
1401 005724 012777 006556 173100  MOV     #INTA,DRINV ;INTERRUPT VECTOR TO INTA
1402 005732 016777 173072 173066  MOV     DRINL,DRVS ;INTERRUPT VECTOR TO PRIORITY DRINL
1403 005740 005077 173050          CLR     DRPSW      ;LET THE DR11-B INTERRUPT
1404 005744 012777 000113 173050  MOV     #113,DRST  ;IE, FNCT3, FNCT1, AND DO TO DRST
1405 005752 005267 173072          INC     BRWAIT     ;USE A WAIT OR BR. INSTRUCTION
1406 005756 032767 000001 173064  BIT     #BIT0,BWAIT ;BIT 0 CLEAR=BR.
1407 005764 001403          BEQ     DATONB
1408 005766 000001          WAIT          ;WAIT FOR INTERRUPT
1409 005770 000240          NOP
1410 005772 000401          BR      .+4
1411 005774 000777          DATONB: BR      .+4
1412 005776 004767 000732          JSR     %7,DATOK  ;CHECK INBUF
1413
1414
1415
1416
1417 006002 104400          ;*****
1418 006004 012767 000010 173032  MOV     #10,BUFLEN ;SET-UP BUFLEN FOR LODBUF AND CHKBUFF
1419 006012 016777 173022 173000  MOV     INBUF,DRBA ;SET-UP DRBA
1420 006020 004767 000430          JSR     %7,LODBUF  ;LOAD INBUF
1421 006024 004767 000462          JSR     %7,CHKBFF  ;LOAD CHKBUFF
1422 006030 005077 172766          CLR     DRST      ;INIT FOR STARTING
1423 006034 012767 000001 173024  MOV     #1,FNCNT   ;GET READY FOR CHECKING
1424 006042 012767 000001 172774  MOV     #1,BUFLEN  ;CHANGE IS NECESSARY FOR INTA ROUTINE
1425 006050 016767 172764 173012  MOV     INBUF,INBUF1 ;SAVE INBUF
1426 006056 012777 006556 172746  MFL0OP: MOV    #INTA,DRINV ;INTERRUPT VECTOR TO INTA
1427 006064 016777 172740 172734  MOV     DRINL,DRVS ;INTERRUPT VECTOR PRIORITY TO DRINL
1428 006072 005077 172716          CLR     DRPSW     ;LET THE DR11-B INTERRUPT
1429 006076 012777 177777 172712  MOV     #-1,DRWC  ;SET-UP FOR I TRANSFER
1430 006104 052777 010101 172710  BIS     #10101,DRST ;MAINT, IE, AND DO TO DRST
1431 006112 000001          WAIT          ;WAIT FOR INTERRUPT
1432 006114 000240          NOP            ;FAKE-OUT RETURN ADDRESS CHANGING
1433 006116 117701 172700          MOVB   DRST,%1    ;LOWER BYTE OF DRST TO R1
1434 006122 042701 000600          BIC   #600,%1    ;GET RID OF READY AND CYCLE BECAUSE OF MAINT MODE
1435 006126 006201          ASR   %1         ;MOVE IT RIGHT ONE PLACE
1436 006130 126701 172732          CMPB  FNCNT,%1   ;CHECK AGAINST FNCNT
1437 006134 001401          BEQ   .+4        ;SHOULD BE EQUAL
1438 006136 104000          HLT          ;FUNCTION BITS DIDN'T INCREMENT IN MAINT MODE
1439 006140 005267 172722          INC   FNCNT      ;GET READY FOR NEXT PASS
1440 006144 022767 000010 172714  CMP   #10,FNCNT  ;ONLY 10 BECAUSE FNCT3-1 GO TO ZERO
1441 006152 001404          BEQ   MFCHK     ;IF ITS EQUAL GO CHECK DATA

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000002 172656 ADD #2,INBUF ;FAKE-OUT INTA ROUTINE
000003 172657 BR MFLOOP ;DO IT AGAIN
000007 172652 MFCBK: MOV #7,BUFLEN ;SET UP FOR DATCHK (10 FNCT CHECKS, 7 TRANSFERS)
000008 172640 MOV INBUF1,INBUF ;RESTORE INBUF
000009 000446 JSR %7,DATCHK ;CHECK DATA

;*****
; TEST 61 TEST FOR 10 MAINT MODE TRANSFERS
;*****
000010 172630 SCOPE
000011 172630 MOV #10,BUFLEN ;BUFLEN=10
000012 172630 MOV BUFLEN,WLEN ;PREPARE NUMBER FOR DRWC
000013 172630 NEG WLEN ;2'S COMPLEMENT OF BUFLEN
000014 000254 JSR %7,LODBUF ;LOAD IN BUFFER WITH INCREMENTING PATTERN
000015 000254 JSR %7,CHKBUF ;LOAD CHECK BUFFER WITH MODIFIED INCREMENTING PATTERN
000016 172610 MOV WLEN,DRWC ;SET UP DRWC
000017 172646 MOV INBUF,DRBA ;SET UP DRBA
000018 172644 MOV #1,DRDB ;MAINT AIDE
000019 172644 MOV #INTA,DRINV ;INTERRUPT VECTOR TO INTA
000020 172632 MOV DRINL,DRVS ;INTERRUPT STATUS AT PRIORITY DRINL
000021 172614 CLR DRPSW ;LET DR11-B INTERRUPT
000022 010101 MOV #10101,DRST ;MAINT, IE, AND DO TO DRST
000023 000777 BR ;WAIT FOR INTERRUPT
000024 000336 JSR %7,DATCHK

;*****
; TEST 62 TEST FOR 200 NPR TRANSFERS IN MAINT MODE
;*****
000200 172520 SCOPE
000201 172514 MOV #200,BUFLEN ;LENGTH OF BUFFER = 200
000202 172514 MOV BUFLEN,WLEN ;PREPARE NUMBER FOR DRWC
000203 172514 NEG WLEN ;2'S COMPLEMENT OF BUFLEN
000204 000112 JSR %7,LODBUF ;LOAD INBUF WITH INCREMENTING PATTERN
000205 000144 JSR %7,CHKBUF ;LOAD CHKBUFF WITH MODIFIED INCREMENTED PATTERN
000206 172442 MOV WLEN,DRWC ;SET UP DRWC
000207 172436 MOV INBUF,DRBA ;SET UP DRBA
000208 172434 MOV #1,DRDB ;MAINT AIDE
000209 172434 MOV #INTA,DRINV ;INT VECTOR TO INTA
000210 172422 MOV DRINL,DRVS ;INT VECTOR AT PRIORITY DRINL
000211 172404 CLR DRPSW ;LET THE DR11-B INTERRUPT
000212 172404 MOV #010101,DRST ;FOLLOWING TO DRST: MAINT(12),IE(06),DO(00)
000213 172426 INC BRWAIT ;USE A WAIT OR BR. INSTRUCTION
000214 172420 BIT #BIT0,BRWAIT ;SEE WHICH ONE
000215 000001 BRANCH ;BIT 0 CLEAR = BR.
000216 000001 WAIT
000217 000240 NOP
000218 000401 BR
000219 000777 BR
000220 0004767 BRANCH: JSR %7,DATCHK ;CHECK THAT CORRECT DATA WAS TRANSFERRED
000221 000204 JSR %7,DATCHK
000356 SCOPE
000357 172360 JMP BELL ;DO IT ALL AGAIN.
000358 172362 LODBUF: MOV INBUF,%2 ;MOVE STARTING ADDRESS OF INBUF TO R2
000359 172362 CLR LENCHK ;CLEAR LENGTH CHECK
000360 0005022 CLR (%2)+ ;CLEAR STARTING ADDRESS OF INBUFF AND INC BY 2
000361 172354 LOADA: INC LENCHK ;INC LENGTH CHECK BY 1
000362 172344 CMP LENCHK,BUFLEN ;CHECK FOR DONE

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Address	Label	Instruction	Comment
001403		BEG	LDEXIT
016702	172340	MOV	LENCHK, (%2)+
000767		BR	LOADA
000307		RTS	%7
016703	172324	MOV	CHKBUF, %2
005067	172324	CLR	LENCHK
005003		CLR	%3
010303		MOV	%3, (%2)+
010303		MOV	%3, (%2)+
062767	000002 172310	ADD	#2, LENCHK
026767	172304 172300	CMP	LENCHK, BUFLN
100003		BPL	.+10
062767	000002	ADD	#2, %3
000767		BR	CHKA
000207		RTS	%7
042777	000100 172236	BIC	#BIT6, %DRST
005777	172232	TST	%DRST
100001		BPL	.+4
104000		HLT	
105777	172222	TSTB	%DRST
100401		BMI	.+4
104000		HLT	
005777	172206	TST	%DRWC
001401		BEG	.+4
104000		HLT	
016702	172224	MOV	BUFLN, %2
066702	172220	ADD	BUFLN, %2
066702	172210	ADD	INBUF, %2
027702	172164	CMP	%DRBA, %2
001401		BEG	.+4
104000		HLT	
062716	000002	ADD	#2, (%6)
004767	000042	JSR	%7, NORMAL
000002		RTI	
006652	172164	MOV	CHKBUF, %2
006656	172156	MOV	INBUF, %3
005067	172160	CLR	LENCHK
005267	172154	INC	LENCHK
022223		CMP	(%2)+, (%3)+
001401		BEG	.+4
104000		HLT	
026767	172142 172136	CMP	LENCHK, BUFLN
001367		BNE	COMPAR
000207		RTS	%7
012777	001026 172112	MOV	#DRVS, %DRINV
005077	172102	CLR	%DRVS
012777	000340 172062	MOV	#340, %PSW
000207		RTS	%7
012702	052525	MOV	#52525, %2
016703	172074	MOV	INBUF, %3
005067	172076	CLR	LENCHK
005267	172072	INC	LENCHK
020223		CMP	%2, (%3)+
001401		BEG	.+4
104000		HLT	

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: IS INBUF FILLED?
: LOAD NEXT BUFFER WORD
: CONTINUE CHECKING
: EXIT
: STARTING ADDRESS OF CHECK-BUFFER TO R2
: CLEAR LENGTH CHECK
: CLEAR R3
: MOVE R3 TO CHKBUF ADDRESS AND INC BY 2
: MOVE R3 TO NEXT CHKBUF ADDRESS AND INC BY 2
: ADD 2 TO LENGTH CHECK
: CHECK FOR DONE
: IS CHECK-BUFFER FILLED?
: NEXT NUMBER FOR BUFFER
: CONTINUE FILLING
: EXIT
: CLEAR IE
: CHECKING FOR ERROR
: ERROR SET?
: ERROR BIT IS SET
: CHECKING READY BIT
: IS READY SET
: FALSE INTERRUPT - ERROR AND READY ARE CLEAR
: TEST1 FOR DRWC=0
: WAS IT EQUAL?
: DRWC NOT =0
: BUFFER LENGTH TO R2
: NUMBER OF TRANSFERS TIMES 2
: CORRECT DRBA
: CHECKING DRBA
: IS DRBA CORRECT?
: DRBA NOT CORRECT
: RETURN ADDRESS TO RETURN ADDRESS +2
: EXIT
: STARTING ADDRESS OF CHECK BUFFER TO R2
: STARTING ADDRESS OF IN BUFFER TO R3
: CLEAR LENGTH CHECK
: MAKE A COMPARISON
: IS THE DATA CORRECT?
: BRANCH IF OK
: BAD DATA
: SEE IF THE BUFFER HAS BEEN CHECKED
: BUFFER CHECKED?
: RESTORE DR11-8 INTERRUPT VECTOR
: RESTORE DR11-8 INTERRUPT STATUS
: RESTORE PROC TO PRIORITY LEVEL 7
: EXIT
: DATO NUMBER TO R2
: STARTING ADDRESS OF IN BUFFER TO R3
: CLEAR LENGTH CHECK
: MAKE A COMPARISON
: IS THE DATA CORRECT?
: BRANCH IF OK
: BAD DATA

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1604 006762 026767 172060 172054 CMP LENCHK,BUFLEN ;SEE IF THE BUFFER HAS BEEN CHECKED
1605 006770 001367 BNE COMP RR ;BUFFER CHECKED?
1606 006772 020223 CMP %2,(%3)+ ;CHECK END OF BUFFER + 1
1607 006774 001001 BNE .+4 ;SEE IF TOO MANY WORDS WERE TRANSFERRED
1608 006776 104000 HLT ;TOO MANY
1609 007000 000207 RTS ;EXIT
1610 007002 042777 000100 172012 ERRCHK: BIC #BIT6,%DRST ;CLEAR IE
1611 007010 005777 172006 TST %DRST ;CHECKING FOR ERROR
1612 007014 100001 BPL .+4 ;ERROR SET?
1613 007016 104000 HLT ;ERROR BIT IS SET
1614 007020 105777 171776 TSTB %DRST ;CHECKING READY BIT
1615 007024 100401 BMI .+4 ;IS RDY SET
1616 007026 104000 HLT ;FALSE ENTRY - ERROR AND READY ARE CLEAR
1617 007030 000207 RTS ;EXIT

*****
: BELL ON PASS COMPLETE
*****
1618 007032 012737 000207 177566 BELL: MOV #207,%DRST ;%DRST = 177566
1619 007040 105737 177564 TSTB %DRST
1620 007044 100375 BPL .-4
1621 007046 012702 012365 MOV #%DR11,%2
1622 007052 004767 003404 JSR %7,TTOUT

*****
: ROUTINE TO CHECK FOR TRACE TRAP TO BE RUN WITH PROGRAM
*****

1623 007056 004767 002670 TRTRAP: JSR %7,CKSWR ;CHECK FO CONT G
1624 007062 032777 010000 171722 BIT #10000,%DR ;SHOULD WE RUN WITH TRACE TRAP
1625 007070 001417 BEQ YESTR ;YES
1626 007072 005767 000104 TST YESTR1 ;NO HAVE WE RAN WITH TRACE TRAP ON
1627 007076 001411 BEQ TRPA ;IF SO RESTORE PREVIOUS CONTENTS
1628 007100 016767 000076 170706 MOV YESTR1,14
1629 007106 016767 000072 170702 MOV YESTR2,16
1630 007114 042777 000020 171672 BIC #20,%PSW ;CLEAR TRACE TRAP
1631 007122 000167 172030 TRPA: JMP BEGIN ;START OF TEST WITH TRACE OFF
1632 007126 000000 TRPB: 0

*****
: SAVE OLD CONTENTS. SET UP FOR TRACE TRAP
*****
1633 007130 016767 170660 000044 YESTR: MOV 14,YESTR1 ;SAVE ODT PC
1634 007136 016767 170654 000040 MOV 16,YESTR2 ;SAVE ODT STATUS
1635 007144 012767 007206 170642 MOV #YESTR,14 ;NEW TRAP VECTOR
1636 007152 005067 170640 CLR 16 ;NEW CONDITION CODES
1637 007156 005077 171632 CLR %PSW
1638 007162 005167 177740 COM TRPB
1639 007166 100403 BMI .+10
1640 007170 052777 000020 171616 BIS #20,%PSW ;SET TRACE TRAP
1641 007176 000167 171754 JMP BEGIN ;START OF TEST WITH TRACE ON

1642 007202 000000 YESTR1: 0 ;STORAGE FOR ODT PC
1643 007204 000000 YESTR2: 0 ;STORAGE FOR ODT STATUS
1644 007206 000002 YESRT: RTI ;RETURN TO PROGRAM FROM TRAP
1645 007210 000000 HALT ;RTI FAILED

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004000
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100000

::*****
: BUS TO BUS TEST (DR11-B TO DR11-B)
:*****

R0=%0
R1=%1
R2=%2
R3=%3
R4=%4
R5=%5
R6=%6
R7=%7
PC=%7
SP=%6

GO=1
FNCT1=2 : OUTPUT MODE
FNCT2=4 : OUTPUT DIRECTION
FNCT3=10 : OUTPUT INTER REQ
XBA16=20
XBA17=40
IE=100
READY=200
CYCLE=400
DSTAT=1000 : INPUT MODE
DSTATB=2000 : INPUT DIRECTION
DSTATC=4000 : INPUT INTR REQ
MAINT=10000
ATTN=20000
NEX=40000
ERROR=100000

007212 000004
007214 000000
007216 000000
007220 000000
007222 000000

NWRDXF: 4 : # OF WORDS TRANSFERRED UNDER FLAG CONTROL PRIOR TO NPR
NEXJOB: 0 : HOLDS ADDRESS OF READY INTERRUPT ROUTINE
 0 : HOLDS ADDRESS OF ERROR INTERRUPT ROUTINE
JBFLAG: 0 : JOB FLAG
JBCNT: 0 : JOB COUNT

::*****
: MASTER START
:*****

007224 000240
007226 005067 177770
007232 012706 013566
007236 004767 000256
007242 005067 177752
007246 012767 007700 177740
007254 012767 000000 177734
007262 012777 000340 171524
007270 012777 000100 171524
007276 005077 171512
007302 000425

MS1: NOP
 CLR JBCNT : CLEAR JOB COUNT
 MOV #BUFF,R6 : SETUP STACK
 JSR R7,SETVEC : SET UP INTERRUPT VECTORS
 CLR JBFLAG : CLEAR JOB FLAG
 MOV #JOBAD,NEXJOB : DO JOBAD FIRST
 MOV #0,NEXJOB+2 : NO ERROR RECOVERY
 MOV #340,APSW : LOCK OUT INTERRUPTS
 MOV #IE,JDRST : SET INTERRUPT ENABLE
 CLR APSW : DROP PRIOTIRY TO ZERO
 BR BACKGD : WAIT FOR JOBS IN BACKGROUND

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007304 000240
007306 012706 013566
007312 004767 000202
007316 005067 177676
007322 012767 010122 177664
007330 012767 010140 177660
007336 012777 000340 171450
007344 012777 000100 171450
007352 005077 171436

: SLAVE START

SS1: NOP
MOV #BUFF, R6
JSR R7, SETVEC ;SET UP INTERRUPT VECTORS
CLR JBFLAG
MOV #SJOB1, NEXJOB ;FOR READY INTERRUPT
MOV #SJOB2, NEXJOB+2 ;FOR ERROR INTERRUPT
MOV #340, DPSW ;RAISE CP PRIORITY TO 7
MOV #IE, DIRST ;SET INTERRUPT ENABLE
CLR DPSW ;DROP CP PRIORITY TO 0 AND ENTER BACKGROUND

: BACKGROUND PROGRAM; WAITS FOR JBFLAG TO SET

BACKGD: INC R0
INC R1
INC R2
INC R3
INC R4
INC R5
CMP R0, R5
BEQ .+6
HLT ;BACKGROUND TEST FAILED
CMP R1, R4
BEQ .+6
HLT ;BACKGROUND TEST FAILED
CMP R2, R3
BEQ .+6
HLT ;BACKGROUND TEST FAILED
TST JBFLAG ;ANY JOBS?
BEQ BACKGD ;BRANCH IF NONE
JSR R5, SAVALL ;YES & EXECUTE JOB WHOSE ADDRESS IS IN JBFLAG
CLR NEXJOB
CLR NEXJOB+2
MOV JBFLAG, 34
CLR JBFLAG
TRAP ;TRAP THROUGH JBFLAG AT 34
JSR R5, RESALL
BR BACKGD

170362

007466 010446
007470 010346
007472 010246

: SUBROUTINE TO PUSH ALL REGISTERS ONTO THE STACK

SAVALL: MOV R4, -(R6) ;R5 WAS PUSHED BY JSR
MOV R3, -(R6)
MOV R2, -(R6)


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1722 007474 010146
1723 007476 010046
1724 007500 000115
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1730 007502 005726
1731 007504 012600
1732 007506 012601
1733 007510 012602
1734 007512 012603
1735 007514 012604
1736 007516 000205
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1742 007520 016700 171306
1743 007524 012720 007600
1744 007530 016710 171274
1745 007534 012767 011072 170256
1746 007542 016767 171262 170262
1747 007550 005067 170260
1748 007554 016767 171250 170254
1749 007562 005000
1750 007564 005001
1751 007566 005002
1752 007570 005003
1753 007572 005004
1754 007574 005005
1755 007576 000207
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1761 007600 005767 177414
1762 007604 001402
1763 007606 104000
1764 007610 000000
1765 007612 032777 004000 171202
1766 007620 001411
1767 007622 005767 177370
1768 007626 001002
1769 007630 104000
1770 007632 000000
1771 007634 016767 177356 177356
1772 007642 000002
1773 007644 105777 171152
1774 007650 100402
1775 007652 104000
1776 007654 000000
1777 007656 005767 177332

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MOV R1,-(R6)
MOV R0,-(R6)
JMP (R5) ;R5 HOLDS RETURN ADDRESS

*****
SUBROUTINE TO POP ALL REGISTERS OFF THE STACK
*****

RESALL: TST (R6)+
MOV (R6)+,R0
MOV (R6)+,R1
MOV (R6)+,R2
MOV (R6)+,R3
MOV (R6)+,R4
RTS R5

*****
ROUTINE TO SET UP INTERRUPT VECTORS
*****

SETVEC: MOV DRINV,R0 ;R0 IS VECTOR ADDRESS
MOV #DRINS,(R0)+ ;PUT SERVICE ADDRESS INTO VECTOR
MOV DRINL,(R0) ;PUT PRIORITY INTO VECTOR+2
MOV #PRINT,30 ;SET UP EMT ADDRESS
MOV DRINL,32 ;SET UP EMT PRIORITY LEVEL
CLR 34
MOV DRINL,36 ;SET UP TRAP ADDRESS
CLR R0 ;INITIALIZE REGISTERS
CLR R1
CLR R2
CLR R3
CLR R4
CLR R5
RTS R7

*****
PRIMARY INTERRUPT SERVICE ROUTINE.
SETS UP JBLFAG WITH ADDRESS OF JOB TO BE RUNSTARS
*****

DRINS: TST JBFLAG ;HAS THE PREVIOUS INTERRUPT BEEN SERVICED?
BEQ DRINO
HLT
HALT ;NO
DRINO: BIT #DSTATC,DRST ;CHECK FOR ERROR
BEQ DRIN3 ;BRANCH IF NO ERROR
TST NEXJOB+2 ;IS THERE AN ERROR SERVICE ROUTINE?
BNE DRIN1 ;BRANCH IF THERE IS.
HLT ;ERROR INTERRUPT, NO ERROR SERVICE.
DRIN1: MOV NEXJOB+2,JBFLAG ;SET UP JOBFLAG WITH ADDRESS OF SERVICE ROUTINE
RTI
DRIN3: TSTB DRST ;CHECK READY
BMI DRIN2 ;BRANCH IF SET
HLT
DRIN2: TST NEXJOB ;INTERRUPT WITHOUT ERROR OR READY
;IS THERE A READY SERVICE ROUTINE

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1778 007662 001002          BNE      .+6          ;BRANCH IF THERE IS.
1779 007664 104000          HLT
1780 007666 000000          HALT
1781 007670 016767 177320 177322  MOV      NEXJOB,JBFLAG ;READY INTERRUPT, NO READY SERVICE
1782 007676 000002          RTI      ;SET UP JOBFLAG WITH SERVICE ROUTINE ADDRESS
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1800 007700 012700 011034  JOBAB:  MOV      #LISTA,RO      ;RO IS XMIT LIST ADDRESS
1799 007704 012701 011046  MOV      #LISTA1,R1      ;LISTA1 WILL BE REC LIST
1791 007710 012021          MOV      (RO)+,(R1)+    ;START WITH BUS ADDRESSES EQUAL
1792 007712 012002          MOV      (RO)+,R2      ;R2 HOLDS WORD COUNT OF XMIT
1793 007714 010211          MOV      R2,(R1)      ;MAKE REC WORD COUNT THE SAME
1794 007716 005402          NEG      R2            ;MAKE WORD COUNT POSITIVE
1795 007720 006302          ASL      R2            ;TRANSFORM INTO BYTE COUNT
1796 007722 060241          ADD      R2,-(R1)      ;ADD TO REC BUS ADDRESS
1797 007724 005010          CLR      (RO)         ;CLEAR OFFSET IN XMIT LIST
1798 007726 024040          CMP      -(RO),-(RO)   ;LEAVE RO=LISTA=XMIT LIST
1799
1800 007730 022767 000100 177264  CMP      #100,JBCNT     ;ENOUGH PASSES FOR BELL?
1801 007736 003010          BGT      JOBA0A        ;BRANCH IF NOT ENOUGH
1802 007740 105737 177564  JOBA0B: TSTB      @#177564 ;TTY READY?
1803 007744 100375          BPL      JOBA0B
1804 007746 012737 000207 177566  MOV      #207,@#177566 ;RING BELL
1805 007754 005067 177242  CLR      JBCNT         ;RESET JOB COUNT
1806 007760 004767 000704  JOBA0A: JSR      R7,SETBUF   ;FILL UP XMIT BUFFER WITH SPECIAL BINARY COUNT
1807 007764 012700 011034  MOV      #LISTA,RO
1808 007770 004767 000370  JSR      R7,MXMIT      ;TRANSMIT DATA TO SLAVE
1809 007774 012767 010012 177212  MOV      #JOB1,NEXJOB  ;JOB1 IS NEXT
1810 010002 012767 000000 177206  MOV      #0,NEXJOB+2  ;NO ERROR RECOVERY
1811 010010 000002          RTI      ;RETURN TO BACKGROUND VIA TRAP
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1831 010050 012700 011034  JOBA1:  MOV      #LISTA1,RO ;PUT REC LIST ADDRESS INTO RO
1829 010016 004767 000574  JSR      R7,FLUSH      ;FLUSH BUFFER
1820 010022 012700 011046  MOV      #LISTA1,RO
1821 010026 004767 000406  JSR      R7,MREC       ;RECEIVE DATA FROM SLAVE
1822 010032 012767 010050 177154  MOV      #JOB2,NEXJOB  ;JOB2 IS NEXT
1823 010040 012767 000000 177150  MOV      #0,NEXJOB+2  ;NO ERROR RECOVERY
1824 010046 000002          RTI
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1931 010050 012700 011034  JOBA2:  MOV      #LISTA,RO      ;XMIT BUFFER LIST
1932 010054 012701 011046  MOV      #LISTA1,R1    ;REC BUFFER LIST
1933 010060 004767 000642  JSR      R7,BUFCHK    ;COMPARE THE TWO BUFFERS

```

```

*****
MASTER'S INTERRUPT SERVICE ROUTINES
ROUTINE A, SEGMENT 0
FILL BUFFER AND TRANSMIT
*****

```

```

*****
ROUTINE A, SEGMENT 1
FLUSH A BUFFER AND RECEIVE DATA
*****

```

```

*****
ROUTINE A, SEGMENT 2
CHECKS TRANSMITTED DATA WITH RECEIVED
*****

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```

1824 010064 042777 000100 170730
1825 010072 012777 000100 170722
1826 010100 012767 007700 177106
1827 010106 012767 000000 177102
1828 010114 005267 177102
1829 010120 000002

```

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BIC #IE,ADRST ;GLITCH INTERRUPT
MOV #IE,ADRST
MOV #JOBAD,NEXJOB ;REPEAT JOBAD
MOV #0,NEXJOB+2
INC JBCNT ;ADVANCE COUNT
RTI

```

```

;*****
;SLAVE'S INTERRUPT SERVICE ROUTINES

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JOB1: IGNORE FIRST READY INTERRUPT

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;*****

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1847 010122 012767 000000 177064
1848 010130 012767 010140 177060
1849 010136 000002

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SJOB1: MOV #0,NEXJOB ;NO MORE READY INTERRUPTS
MOV #SJOB2,NEXJOB+2 ;UNTIL ATTN INTERRUPT
RTI

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;*****
;JOB2: WAIT FOR COMMAND
;*****

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```

1855 010140 032777 004000 170654
1856 010146 001002
1857 010150 104000
1858 010152 000000
1859 010154 005001
1860 010156 016702 170640
1861 010162 012703 000010
1862 010166 012704 004000
1863 010172 016705 170626
1864 010176 012700 011062
1865 010202 004767 000122
1866 010206 012700 011060
1867 010212 016010 000004
1868 010216 066710 170616
1869 010222 012077 170572
1870 010226 012077 170564
1871 010232 005077 170564
1872 010236 032777 002000 170556
1873 010244 001405
1874 010246 032777 000400 170546
1875 010254 001774
1876 010256 000412
1877 010260 012700 011060
1878 010264 004767 000356
1879 010270 052777 000004 170524
1880 010276 042777 000400 170516
1881 010304 052777 000101 170510
1882 010312 012767 010122 176674
1883 010320 012767 010140 176670
1884 010326 000002

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SJOB2: BIT #DSTATC,ADRST ;TEST FOR INTER
BNE SJOB2A
HLT
HALT ;ERROR OTHER THAN DSTATC
SJOB2A: CLR R1 ;SET UP FOR PARAMETERS
MOV DRST,R2 ;R2 IS STATUS ADDRESS
MOV #FNCT3,R3 ;R3 IS FUNCTION BIT 3
MOV #DSTATC,R4 ;R4 IS INTERRUPT BIT
MOV DRDB,R5 ;R5 IS DATA BUFFER ADDRESS
MOV #LISTB+2,R0 ;STORE PARAMETERS HERE STARTING WITH WORD COUNT
JSR R7,HNDSHK ;GET PARAMETERS
MOV #LISTB,R0 ;R0 IS TOP OF LIST
MOV 4(R0),(R0) ;MOVE OFFSET TO TOP
ADD INBUF,(R0) ;TOP OF LIST IS BUFFER START + OFFSET
MOV (R0)+,ADRBA ;SET UP BUS ADDRESS
MOV (R0)+,ADRWC ;SET UP WORD COUNT
CLR ADRST ;CLEAR ALL FUNCTION BITS
BIT #DSTATB,ADRST ;WHICH DIRECTION
BEQ SJOB2C ;BRANCH IF RECIEVE (LEAVE FNCT1 CLEAR FOR DATI'S)
SJOB2B: BIT #CYCLE,ADRST ;WAIT FOR MASTER TO SET CYCLE
BEQ SJOB2B ;BRANCH IF NOT SET
BR SJOB2D ;GO DO THE COMAND
SJOB2C: MOV #LISTB,R0 ;BLUSH THE BUFFER
JSR R7,BLUSH ;BLUSH THE BUFFER
BIS #FNCT2,ADRST ;SET FNCT2 FOR DATO'S
BIC #CYCLE,ADRST ;CLEAR CYCLE
SJOB2D: BIS #IE!GO,ADRST ;EXECUTE COMMAND AND INTERRUPT WHEN DONE
MOV #SJOB1,NEXJOB ;IGNORE READY INTERRUPT
MOV #SJOB2,NEXJOB+2 ;WAIT FOR ATTN INTERRUPT
RTI

```

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;*****
;SLAVE ROUTINE TO ACCEPT PARAMETERS FROM MASTER
;*****

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1890 010330 011515
1891 010332 011520
1892 010334 050312
1893 010336 030412
1894 010340 001376
1895 010342 040312
1896 010344 005201
1897 010346 020167 176640
1898 010352 002401
1899 010354 000207
1900 010356 030412
1901 010360 001776
1902 010362 000762
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1909 010364 005777 170432
1910 010370 100002
1911 010372 104000
1912 010374 000000
1913 010376 105777 170420
1914 010402 100402
1915 010404 104000
1916 010406 000000
1917 010410 012777 000000 170404
1918 010416 004767 000102
1919 010422 042777 000400 170372
1920 010430 052777 000101 170364
1921 010436 000207
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1927 010440 005777 170356
1928 010444 100002
1929 010446 104000
1930 010450 000000
1931 010452 105777 170344
1932 010456 100402
1933 010460 104000
1934 010462 000000
1935 010464 012777 000004 170330
1936 010472 004767 000026
1937 010476 032777 002000 170316
1938 010504 001374
1939 010506 042777 000400 170306
1940 010514 052777 000101 170300
1941 010522 000207
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HNDSHK: MOV (R5), (R5) ;ECHO PARAMETER
          MOV (R5), (R0)+ ;STORE PARAMETER
          BIS R3, (R2) ;REPLY WITH FNCT3
HNDSH1: BIT R4, (R2) ;WAIT FOR ATTN TO DROP
          BNE HNDSH1
          BIC R3, (R2) ;DROP FNCT3
          INC R1 ;CHECK NUMBER
          CMP R1, NWRDXF
          BLT HNDSH2 ;BRANCH IF NOT DONE YET
          RTS R7
HNDSH2: BIT R4, (R2) ;WAIT FOR NEXT WORD
          BEQ HNDSH2 ;BRANCH IF ATTN CLEAR
          BR HNDSHK ;GET ANOTHER PARAMETER

```

```

;*****
; MASTER TRANSMIT ROUTINE
; ENTER WITH TRANSFER LIST IN R0
;*****

```

```

MXMIT: TST @DRST ;MAKE SURE ERROR IS CLEAR
        BPL MXMIT1 ;AND READY IS SET
        HLT ;ERROR IS SET
MXMIT1: TSTB @DRST
        BMI MXMIT2
        HLT
MXMIT2: MOV #0, @DRST ;READY NOT SET
        JSR R7, PRMXFR ;SET UP FUNCTION FOR DATI'S
        BIC #CYCLE, @DRST ;TRANSFER PARAMETERS OF LIST WHOSE ADDRESS IS IN R0
        BIS #IE!GO, @DRST ;MAKE SURE CYCLE IS CLEAR
        RTS R7 ;EXECUTE COMMAND AND INTERRUPT WHEN DONE

```

```

;*****
; MASTER RECEIVE ROUTINE
; ENTER WITH TRANSFER LIST IN R0
;*****

```

```

MREC: TST @DRST ;MAKE SURE ERROR IS CLEAR
       BPL MREC1 ;AND READY SET.
       HLT ;ERROR SET
MREC1: TSTB @DRST
       BMI MREC2
       HLT
MREC2: MOV #FNCT2, @DRST ;READY CLEAR
       JSR R7, PRMXFR ;SET UP FUNCTION FOR DATO'S
       BIT #DSTATB, @DRST ;TRANSFER PARAMETERS OF LIST WHOSE ADDRESS IS IN R0
       BNE MREC3 ;WAIT FOR SLAVE TO CLEAR DIRECTION
       BIC #CYCLE, @DRST ;BRANCH IF SET
       BIS #IE!GO, @DRST ;CLEAR CYCLE
       RTS R7 ;EXECUTE COMMAND AND INTERRUPT WHEN DONE.

```

```

;*****
; ROUTINE TO TRANSFER AND CHECK PARAMETERS UNDER FLAG CONTROL
; ENTER WITH R0 POINTING TO TRANSFER LIST
;*****

```

```

1946
1947
1948 010524 012077 170270 PRMXFR: MOV (R0)+,DRBA ;FIRST WORD IN LIST IS ADDRESS
1949 010530 011077 170262 MOV (R0),DRWC ;SECOND WORD IN LIST IS WORD COUNT
1950 010534 005001 CLR R1 ;R1 COUNTS PARAMETERS TRANSFERRED
1951 010536 016702 170260 MOV DRST,R2 ;R2 IS THE STATUS ADDRESS
1952 010542 012703 000010 MOV #FNCT3,R3 ;R3 USED FOR FUNCTION BIT 3
1953 010546 012704 004000 MOV #DSTATC,R4 ;R4 USED FOR INTERRUPT BIT
1954 010552 016705 170246 MOV DRDB,R5 ;R5 IS THE DATA BUFFER ADDRESS
1955 010556 011015 PRMXF1: MOV (R0),(R5) ;SET UP DRDB WITH PARAMETER
1956 010560 050312 BIS R3,(R2) ;CALL SLAVE'S ATTN
1957 010562 030412 PRMXF2: BIT R4,(R2) ;WAIT FOR REPLY
1958 010554 001776 BEQ PRMXF2 ;BRANCH IF ATTN CLEAR
1959 010566 022015 CMP (R0)+,(R5) ;COMPARE PARAMETER SENT WITH SLAVE'S ECHO
1960 010570 001402 BEQ PRMXF3 ;BRANCH IF EQUAL
1961 010572 104000 HLT ;PARAMETER DID NOT ECHO
1962 010574 000000 PRMXF3: BIC R3,(R2) ;DROP SLAVE'S ATTN
1963 010576 040312 PRMXF4: BIT R4,(R2) ;WAIT FOR REPLY
1964 010600 030412 BNE PRMXF4 ;BRANCH IF ATTN SET
1965 010602 001376 INC R1 ;ADVANCE PARAMETER COUNT
1966 010604 005201 CMP R1,NWRDXF ;ALL PARAMETER XFERRED?
1967 010606 020167 176400 BLT PRMXF1 ;BRANCH IF NOT DONE
1968 010612 002761 RTS R7 ;RETURN WHEN ALL PARAMETERS TRANSFERRED AND CHECKED.
1969 010614 000207
1970
1971
1972
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1975
1976 010616 005005 FLUSH: CLR R5 ;SET R5 TO ZIP
1977 010620 004767 000030 JSR R7,BSETUP ;SET UP REGISTERS
1978 010624 004767 000004 FLUSH1: JSR R7,BUFPUT ;STORE ITEM IN BUFFER
1979 010630 002775 BLT FLUSH1
1980 010632 000432 BR BUFOUT ;STOP WHEN BUFFER FULL
1981
1982 010634 010521 BUFPUT: MOV R5,(R1)+ ;PUT R5 INTO BUFFER
1983 010636 060503 ADD R5,R3 ;INCLUDE IN CHECKSUM
1984 010640 005504 ADC R4
1985 010642 005202 INC R2 ;ADVANCE WORD COUNT
1986 010644 000207 RTS R7 ;RETURN WITH STATUS SET
1987
1988
1989
1990
1991
1992 010646 012705 177777 BLUSH: MOV #-1,R5 ;SET R5 TO ALL ONE'S
1993 010652 000762 BR FLUSH+2
1994
1995
1996 010654 012001 ;REGISTER SETUP ROUTINE
1997 010656 012002 BSETUP: MOV (R0)+,R1 ;R1 IS BUS ADDRESS
1998 010660 005720 MOV (R0)+,R2 ;R2 IS WORD COUNT
1999 010662 005003 TST (R0)+ ;SKIP OVER OFFSET
2000 010664 005004 CLR R3 ;CLEAR LOW CHECKSUM
2001 010666 000207 CLR R4 ;CLEAR HIGH CHECKSUM
RTS R7 ;RETURN

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010670 004767 177760
010674 005005
010676 004767 177732
010702 002006
010704 005105
010706 004767 177722
010712 002002
010714 005405
010716 000767
010720 010320
010722 010420
010724 000207

010726 010046
010730 010146 000036
010732 004767
010736 012600
010740 012001
010742 012002
010744 012600
010746 012003
010750 020220
010752 003402
010754 104000
010756 000000

010760 022123
010762 001401
010764 104000
010766 005202
010770 002773
010772 000207

010774 004767 177654
011000 004767 000016
011004 002775
011006 020320
011010 001003
011012 020420
011014 001001

ROUTINE TO FILL BUFFER WITH SPECIAL BINARY COUNT
ENTER WITH R0 POINTING TO TRANSFER LIST

```
SETBUF: JSR R7,BSETUP ;SET UP REGISTERS
        CLR R5
SETBF1: JSR R7,BUFPUT ;NUMBER TO BUFFER
        BGE BUFOUT
        COM R5
        JSR R7,BUFPUT ;COMPLEMENT OF NUMBER TO BUFFER
        BGE BUFOUT
        NEG R5 ;INCREMENT NUMBER
        BR SETBF1
BUFOUT: MOV R3,(R0)+ ;MOVE LOW CHECK TO LIST
        MOV R4,(R0)+ ;MOVE HIGH CHECK TO LIST
        RTS R7 ;RETURN
```

ROUTINE TO COMPARE TWO BUFFERS
BUFFER LIST #1 IS IN R1
BUFFER LIST #2 IS IN R0. #2 CHECKED FOR PROPER CHECKSUM

```
BUFCHK: MOV R0,-(R6) ;SAVE LIST#2 ON STACK
        MOV R1,-(R6) ;SAVE LIST#1 ON STACK
        JSR R7,CHKSUM ;VERIFY INTEGRITY OF CHECK BUFFER (#2)
        MOV (R6)+,R0 ;RECOVER 1ST LIST POINTER
        MOV (R0)+,R1 ;BUS ADDRESS #1
        MOV (R0)+,R2 ;WORD COUNT #1
        MOV (R6)+,R0 ;RECOVER 2ND LIST POINTER
        MOV (R0)+,R3 ;BUS ADDRESS #2
        CMP R2,(R0)+ ;COMPARE WORD COUNTS
        BLE BUFCK1 ;BRANCH IF EQUAL OR LESS THAN
        HLT ;BUFFER 2 IS LONGER THAN 1
        HALT

BUFCK1: CMP (R1)+,(R3)+ ;COMPARE BUFFERS
        BEQ BUFCK2
        HLT ;DATA ERROR

BUFCK2: INC R2 ;ADVANCE COUNT
        BLT BUFCK1 ;BRANCH IF NOT DONE
        RTS R7 ;RETURN; STACK IS CLEAR
```

ROUTINE TO CHECK SUM OF BUFFER
ENTER WITH R0 POINTING TO TRANSFER LIST

```
CHKSUM: JSR R7,BSETUP ;SET UP REGISTERS
CHKSM1: JSR R7,GETBUF ;GET ITEM FROM BUFFER
        BLT CHKSM1 ;BRANCH IF NOT DONE
        CMP R3,(R0)+ ;COMPARE LOW ORDER CHECKS
        BNE CHKSM2
        CMP R4,(R0)+ ;COMPARE HIGH ORDER CHECKS
        BNE CHKSM2
```

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2058 011016 000207          RTS      R7          ;RETURN IF CHECKSUM OK.
2059 011020 104000        CHKSM2: HLT          ;ORIGINAL BUFFER CHECKSUM DOES NOT AGREE WITH PRESENT
2060
2061 011022 012105        GETBUF: MOV      (R1)+,R5      ;GET ITEM OUT OF BUFFER
2062 011024 060503          ADD      R5,R3          ;ADD TO CHECKSUM
2063 011026 005504          ADC      R4
2064 011030 005202          INC      R2
2065 011032 000207          RTS      R7          ;ADVANCE WORD COUNT
2066
2067 011034 013570        LISTA: XINBUF          ;START OF XMIT BUFFER
2068 011036 177605          -123.          ;WORD COUNT
2069 011040 000000          0              ;OFFSET
2070 011042 000000          0              ;CHECKSUM LOW
2071 011044 000000          0              ;CHECKSUM HIGH
2072
2073 011046 000000        LISTA1: 0           ;START OF REC BUFFER
2074 011050 000000          0              ;WORD COUNT
2075 011052 000000          0              ;OFFSET
2076 011054 000000          0              ;CHECKSUM LOW
2077 011056 000000          0              ;CHECKSUM HIGH
2078
2079 011060 013570        LISTB: XINBUF          ;SLAVE'S ECHO BUFFER
2080 011062 000000          0
2081 011064 000000          0
2082 011066 000000          0
2083 011070 000000          0
2084
2085
2086
2087
2088
2089
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2091
2092 011072 004767 000654  PRINT: JSR      %7,CKSWR
2093 011076 037727 167710 020000 BIT      @SR,#20000 ;TEST FOR INHIBIT PRINT OU
2094 011104 001401          BEQ      .+4          ;BRANCH TO PRINT
2095 011106 000002          RTI          ;INHIBIT, RETURN TO MAIN STREAM
2096 011110 012667 000172 MOV      (6)+,SAVPC   ;PC OF FAILING ROUTINE
2097 011114 012667 000170 MOV      (6)+,SAVCC   ;CC OF ERROR CONDITION
2098 011120 024646          CMP      -(6),-(6)   ;REPOSITION THE STACK
2099 011122 012777 000215 167734 MOV      #215,@TPB   ;CR
2100 011130 105777 167726 TSTB    @TPS
2101 011134 100375          BPL      .-4
2102 011136 012777 000212 167720 MOV      #212,@TPB   ;LINE FEED
2103 011144 105777 167712 TSTB    @TPS
2104 011150 100375          BPL      .-4
2105 011152 010267 000122 MOV      %2,SAVR2    ;SAVE R2
2106 011156 010367 000120 MOV      %3,SAVR3    ;SAVE R3
2107 011162 010467 000116 MOV      %4,SAVR4    ;SAVE R4
2108 011166 016702 000114 MOV      SAVPC,%2
2109 011172 004767 000114 JSR      %7,PRTAB    ;PRINT OCTAL NUMBER
2110 011176 012777 000240 167660 MOV      #240,@TPB
2111 011204 105777 167652 TSTB    @TPS
2112 011210 100375          BPL      .-4
2113 011212 016702 000072 MOV      SAVCC,%2

```

```

;*****
; ENTERED WITH SYSTEM TRAP CALL(HLT)
; PRINT OUT THE ERROR PC AND STATUS REGISTER
;*****

```

2114	011216	004767	000070			JSR	%7, PRTAB	:PRINT OCTAL NUMBER
2115	011222	012777	000240	167634		MOV	#240, JTPB	:PRINT SPACE
2116	011230	105777	167626			TSTB	JTPS	:PRINTER DONE
2117	011234	100375				BPL	-4	:BRANCH WHEN NOT DONE
2118	011236	017702	167560			MOV	JDRST, %2	:GET DR11B STATUS
2119	011242	004767	000044			JSR	%7, PRTAB	:PRINT OCTAL NUMBER
2120	011246	016702	000026			MOV	SAVR2, %2	
2121	011252	016703	000024			MOV	SAVR3, %3	
2122	011256	016704	000022			MOV	SAVR4, %4	
2123	011262	004767	000464			JSR	%7, CKSWR	
2124	011266	005777	167520			TST	JSR	:CHECK SR FOR HALT SWITCH
2125	011272	100001				BPL	.+4	
2126	011274	000000				HALT		:HALT ON ERROR UP
2127	011276	000002				RTI		:RETURN TO MAINLINE
2128	011300	000000			SAVR2:	0		
2129	011302	000000			SAVR3:	0		
2130	011304	000000			SAVR4:	0		
2131	011306	000000			SAVPC:	0		
2132	011310	000000			SAVCC:	0		
2133								
2134	011312	005067	000260		PRTAB:	CLR	BINCT	
2135	011316	005067	000252			CLR	WGTCT	
2136	011322	012704	011602			MOV	#LIST, %4	:GET LIST ADDRESS
2137	011326	142777	000177	167526		BICB	#177, JTPS	:CLR INT FLAG
2138	011334	012767	000005	000236		MOV	#5, ASCNT	
2139	011342	012767	000007	000220		MOV	#7, SEVEN	
2140	011350	012767	000001	000214		MOV	#1, DECML	
2141	011356	105777	167500		WAIT1:	TSTB	JTPS	
2142	011362	100375				BPL	WAIT1	
2143	011364	005702				TST	%2	
2144	011366	100404				BMI	MINUS	:NEG SIGN PRINT 1
2145	011370	012777	000260	167466		MOV	#260, JTPB	:POS SIGN PRINT 0
2146	011376	000403				BR	START	
2147	011400	012777	000261	167456	MINUS:	MOV	#261, JTPB	
2148	011406	016703	000156		START:	MOV	SEVEN, %3	:PUT MASK IN R3
2149	011412	010267	000150			MOV	%2, TOODLE	:GET READY TO DOODLE NUMBER IN TOODLE
2150	011416	005167	000144			COM	TOODLE	:COMPENSATES FOR COMPLEMENT DURING BIC
2151	011422	046703	000140			BIC	TOODLE, %3	:AND IN OCTAL CHARACTER
2152	011426	001410				BEQ	WRTOC	:ZERO, WRITE 0 IN LIST
2153	011430	066767	000136	000136	MKNUM:	ADD	DECML, WGTCT	:COUNT UP TO
2154	011436	005267	000134			INC	BINCT	:AND RECORD
2155	011442	026703	000126			CMP	WGTCT, %3	:SAME BINARY WEIGHT
2156	011446	001370				BNE	MKNUM	:KEEP COUNTN
2157	011450	062767	000260	000120	WRTOC:	ADD	#260, BINCT	:ADD ASCII PREFIX
2158	011456	016724	000114			MOV	BINCT, (4)+	:WRITE ASCII CHAR IN LIST
2159	011462	066767	000102	000102		ADD	SEVEN, DECML	:EXPAND BINARY WEIGHT
2160	011470	005067	000100			CLR	WGTCT	
2161	011474	005067	000076			CLR	BINCT	
2162	011500	005367	000074			DEC	ASCNT	
2163	011504	001410				BEQ	XLIST	:5 CHAR IN LIST
2164	011506	012703	000003			MOV	#3, %3	:SET X3 FOR ADD LOOP
2165	011512	066767	000052	000050	MOADD:	ADD	SEVEN, SEVEN	:MAKING SEVENTY BY SEVEN
2166	011520	005303				DEC	%3	
2167	011522	001373				BNE	MOADD	
2168	011524	000730				BR	START	:NX SEVEN SET GET NX OCTAL
2169	011526	012767	000005	000044	XLIST:	MOV	#5, ASCNT	:SEND 5 CHAR TO TTY


```

011736 000167 166236 JMP 200
*****
CHECK SWITCH REGISTER ROUTINE. CHECKS FOR IG TO ALLOW CHANGING
OF LOC. 176.
*****
011742 000000 TEMPST: .WORD 0
011744 000000 COUNT: .WORD 0
011746 000000 RDSW: .WORD 0
011750 000000 TIB: .WORD 0

011752 022767 000176 167032 CKSWR: CMP #SWREG,SR ;SOFTWARE SWITCH REGISTER PRESENT
011754 001133 OUT
011756 109777 167070 TSTB #TKS ;YES, WAIT FOR
011758 100130 OUT ;READY, GET CHARACTER
011760 017767 167064 177752 BPL #TKB,TIB ;AND STRIP OFF
011762 042767 177600 177744 BIC #177600,TIB ;THE GARBAGE
011764 022767 000007 177736 CMP #7,TIB ;IS IT A <IG>
011766 001116 OUT
011768 002702 012324 MOV #SCNTG,%2
011770 004767 000426 JSR PC,TTOUT
011772 002702 012336 CNTLU: MOV #SMSWR,%2
011774 004767 000426 JSR PC,TTOUT
011776 017702 166752 MOV #SR,%2
011778 004767 177246 JSR %7,PRTAB
011780 012702 012346 MOV #SMNEW,%2
011782 004767 000406 JSR PC,TTOUT
011784 005037 011742 CLR #TEMPST
011786 005067 177656 SREAD: CLR TEMPST
011788 012767 000007 177652 MOV #7,COUNT
011790 004767 000154 16: JSR PC,TTIN ;GO READ A CHARACTER
011792 042767 177600 177644 BIC #177600,TIB ;STRIP OFF GARBAGE
011794 122767 000025 177636 CMPB #25,TIB ;IS IT A 'U'?
011796 001001 BNE 25 ;BRANCH IF NOT
011798 000743 BR CNTLU ;START OVER
011800 122767 000015 177624 25: CMPB #15,TIB ;IS IT A <CR>?
011802 001011 BNE 45 ;BRANCH IF NOT
011804 012702 012332 MOV #SCRLF,%2
011806 004767 000324 JSR %7,TTOUT
011808 022767 000007 177600 CMP #7,COUNT ;WAS IT FIRST CHARACTER
011810 001036 BNE 75 ;CHANGE SWR IF NOT FIRST ONE
011812 000440 BR OUT ;GET OUT
011814 122767 000060 177572 85: CMPB #60,TIB
011816 003004 BGT 55
011818 122767 000067 177562 45: CMPB #67,TIB
011820 002005 BGE 65
011822 012702 012357 55: MOV #SQUEST,%2
011824 004767 000262 JSR PC,TTOUT
011826 000745 BR 35 ;START OVER IF NOT LEGAL CHARACTER
011828 006367 177534 65: ASL TEMPST
011830 006367 177530 ASL TEMPST
011832 006367 177524 ASL TEMPST
011834 142767 000060 177524 BICB #60,TIB ;GET NITTY-GRITTY
011836 166767 177520 177510 BICB TIB,TEMPST
011838 005367 177506 DEC COUNT ;ONLY WANT 6 DIGITS

```

```

012333 000207 177474 166542 7S: BEQ 5S
012334 000714 000714 BR 1S
012335 016777 177474 166542 MOV TEMPST,DSR ;CHANGE SWITCH REGISTER CONTENTS
012336 000207 000207 OUT: RTS %7 ;RETURN TO PROGRAM
:*****
: TTY READ SUBROUTINE*****
:*****

012337 005077 166600 TTIN: CLR @TKS
012338 005077 166576 CLR @TKB
012339 005067 :774626 CLR TIB
012340 005277 166564 INC @TKS
012341 105777 166560 TTIN1: TSTB @TKS
012342 100375 BPL TTIN1
012343 017767 166554 177442 MOV @TKB,TIB
012344 105777 166550 TTIN2: TSTB @TPS
012345 100375 BPL TTIN2
012346 116777 177430 166542 MOVB TIB,@TPB

012347 000207 OUT: RTS %7
012348 057127 020107 000046 $CNTG: .ASCIZ '+G 3'
012349 020127 000046 $CRLF: .ASCIZ '+ 3'
012350 051527 051127 020075 $MSWR: .ASCIZ '+SWR= 3'
012351 000046
012352 020040 042516 036527 $MNEW: .ASCIZ ' NEW= 3'
012353 023040 000
012354 137 020077 023137 $QUEST: .ASCIZ '+? +3'
012355 000
012356 137 051104 030461 $DR11: .ASCIZ '+DR11B OK 3'
012357 020102 045517 020040
012358 000
012359 137 046440 044501 $MAIN: .ASCIZ '+ MAINDEC-11-DZDRB-D +3'
012360 042116 041505 030455
012361 022546 055104 051104
012362 020104 020104 023137
012363 000
012364 137 042040 030522 $HEAD: .ASCIZ '+ DR11B LOGIC TEST 3'
012365 041061 046040 043517
012366 041511 052040 051505
012367 020124 000046

.EVEN

012460 000000 OFL: 0 ;FIRST CHAR FLAG

:*****
: TTY ASCII OUTPUT ROUTINE
:*****

012463 105712 TTOUT: TSTB (2) ;CHECK FOR NULL CHARACTER
012464 001403 BEQ 1S ;IF NOT, TYPE THE CHARACTER
012465 122712 000046 CMPB #'S,(2) ;CHECK FOR TERMINATOR
012472 001005 BNE .EMPTY

```

```

000100 166360 1S:      BIC      #100, @TPS
                        CLR      %2
                        RTS      %7
                        .EMPTY: CMPB  #'+ (2)
                        BEQ      .RET
                        CMPB  #'! (2)
                        BEQ      .REST
166334 1S:      TSTB  @TPS
166330      SPL  1S
                        MOV  (2)+, @TPB
                        BR   TTOUT
                        .RET: INC  %2
                        MOV  %2, .SAV
                        MOV  #.RETR, %2
                        BR   .RET-6
000006  .REST:  MOV  .SAV, %2
                        BR   TTOUT

012560 012 041 .RETR: .BYTE 15, 12, '!'
                        .EVEN
012564 .SAV:  0
                        .=. +1000
012566 BUFF:  0
                        .FOR STACK POINTER 100 LOCATIONS
012570 XINBUF: .
                        .=. +1000
014572 XCHKBU: .
                        .END
000001

```


DECM	011572	2140*	2153	2159*	2181#									
DIOMEM	001036	525#	1155	1337										
DONE	005343	1325#	1330#											
DRBA	001020	518#	567*	600*	603	626*	627	842*	843	846*	847	870*	871	874*
		1006*	1011*	1027	1043*	1059	1082*	1103*	1121*	1141*	1155*	1181*	1202*	1207*
DRDB	001024	1303	1315*	1337*	1348*	1372*	1399*	1419*	1458*	1477*	1526	1869*	1948*	
		520#	571*	1012*	1030	1045*	1083*	1089	1104*	1122*	1128	1142*	1240*	1243
		1252*	1253	1261*	1262	1265*	1266	1276*	1277	1280*	1373*	1385	1400*	1459*
		1478*	1863	1954										
DRINL	001030	522#	1047	1085	1106	1124	1144	1157	1183	1209	1375	1402	1427	1461
		1480	1744	1746	1748									
DRINS	007600	1743	1761#											
DRINV	001032	523#	892*	911*	931*	950*	956*	1014*	1046*	1084*	1105*	1123*	1143*	1156*
		1182*	1208*	1338*	1347*	1374*	1401*	1426*	1460*	1479*	1543*	1742		
DRIND	007612	1762	1765#											
DRINI	007634	1768	1771#											
DRIN2	007656	1774	1777#											
DRIN3	007644	1766	1773#											
DRST	001022	519#	569*	639*	640	643*	644	656*	657	660*	661	673*	674	677*
		678	686*	687	690*	691	699*	700	703*	704	712*	713	716*	717
		725*	726	729*	730	738*	739	742*	743	751*	753	756	759	762
		765	768	771	774	777*	778	781	784	787	790	794	797	800
		810*	812	819	885	889	893*	895*	904	908	912*	914*	924	928
		932*	934*	943	947	951*	954*	963*	964	967*	968	971	974*	975*
		976	979	982*	983*	984	987	990*	995	997	1000	1002*	1003	1007
		1017*	1036*	1049*	1069*	1087*	1108*	1126*	1146*	1159*	1162	1165	1168	1185*
		1189	1192	1195*	1196	1199	1203	1211*	1215	1218	1221*	1222	1225	1230
		1291	1294	1316	1319*	1320	1324	1341*	1344	1349*	1351*	1356	1377*	1404*
		1422*	1430*	1433	1463*	1482*	1513*	1514	1517	1560*	1561	1564	1663*	1679*
		1765	1773	1834*	1835*	1855	1860	1871*	1872	1874	1879*	1880*	1881*	1909
		1913	1917*	1919*	1920*	1927	1931	1935*	1937	1939*	1940*	1951	2118	
DRVS	001026	521#	1015*	1047*	1085*	1106*	1124*	1144*	1157*	1183*	1209*	1339*	1375*	1402*
		1427*	1461*	1480*	1543	1544*								
DRWC	001016	517#	565*	584*	587	615*	616	829*	830	833*	834	857*	858	861*
		1010*	1024	1042*	1056	1081*	1102*	1120*	1140*	1154*	1180*	1314*	1336*	1350*
		1371*	1398*	1429*	1457*	1476*	1520	1870*	1949*					
DSTAT=	001000	1637#												
DSTATB=	002000	1638#	1872	1937										
DSTATC=	004000	1639#	1765	1855	1862	1953								
ERRA	001234	563	573#											
ERRCHK	007002	1023	1055	1560#										
ERRDO	005416	1338	1344#											
ERRDO1	005474	1347	1356#											
ERROR =	100000	1643#												
FLUSH	010616	1819	1976#	1993										
FLUSH1	010624	1978#	1979											
FNCNT	001066	537#	1423*	1436	1439*	1440								
FNCT1 =	000002	1629#												
FNCT2 =	000004	1630#	1879	1935										
FNCT3 =	000010	1631#	1861	1952										
GETBUF	011022	2052	2061#											
GO =	000001	1628#	1881	1920	1940									
HDFHM	011556	2174	2176#											
HLT =	104000	464#	573	589	605	618	629	642	646	659	663	676	680	689
		693	702	706	715	719	728	732	741	745	755	758	761	764
		767	770	773	776	780	783	786	789	792	796	799	802	816

J04

SAVCC	0111310	2097*	2113	2132#											
SAVPC	0111306	2098*	2108	2131#											
SAVR2	0111300	2105*	2120	2128#											
SAVR3	0111302	2106*	2121	2129#											
SAVR4	0111304	2107*	2122	2130#											
SCOPF =	104400	453#	562#	575#	590	599	613	625	638	655	672	685	698	711	
		724	737	750	808	827	841	854	868	882	902	922	941	962	
		994	1041	1075	1096	1115	1134	1153	1178	1238	1250	1260	1273	1288	
		1301	1312	1335	1366	1392	1417	1451	1470	1491					
SCOPEA	0111614	2195#													
SCOPEB	0111636	2197#	2200#	2211	2218										
SCOPEC	0111650	491	2209#												
SCOPEF	0111732	2215	2217*	2219*	2223#										
SCOPEG	0111716	2214	2216	2219#											
SETBFI	010676	2010#	2016												
SETBUF	010670	1806	2008#												
SETVEC	007520	1658	1674	1742#											
SEVEN	011570	2139*	2148	2159	2165*	2180#									
SJOB1	010122	1676	1847#	1882											
SJOB2	010140	1677	1848	1855#	1883										
SJOB2A	010154	1856	1859#												
SJOB2B	010246	1874#	1875												
SJOB2C	010260	1873	1877#												
SJOB2D	010304	1876	1891#												
SUP =	%000006	540*	541*	546	548	549	1626#								
USR	001012	515#	543	547*	550	1583	2093	2124	2196	2210	2213	2238	2250	2284*	
SSTART	001002	513#													
SS1	007304	513	1672#												
START	011406	2146	2148#	2168											
SUSWR	001072	503	540#												
SWREG	000176	494#	547	550	2238	2276*	2277*	2278*	2280*	2284					
TEMPST	011742	2233#	2254*	2255*	2276*	2277*	2278*	2280*	2284						
TIB	011750	2236#	2242*	2243*	2244	2258*	2259	2262	2269	2271	2279*	2280	2294*	2298*	
		2301													
TKB	001060	534#	2242	2293*	2298										
TKS	001056	533#	1342*	2240	2292*	2295*	2296								
TNPRO	003542	1035	1041#	1070											
TNPR1	003306	995#	1037												
TOODLE	011566	2149*	2150*	2151	2179#										
TPB	001064	536#	2099*	2102*	2110*	2115*	2145*	2147*	2172*	2301*	2347*				
TPS	001062	535#	2100	2103	2111	2116	2137*	2141	2170	2176	2299	2338*	2345		
TRPA	007122	1586	1590#												
TRPB	007126	1591#	1601*												
TRTRAP	007056	1582#													
TSTRDY	005320	1324#	1328												
TTIN	012252	2257	2292#												
TTIN1	012272	2296#	2297												
TTIN2	012306	2299#	2300												
TTOUT	012462	500	502	1576	2247	2249	2253	2265	2274	2334#	2348	2354			
T33CLR	003534	1022	1036#												
T34CLR	003706	1054	1069#												
T35	003714	1068	1075#												
WAIT1	011356	2141#	2142												
WAIT2	011534	2170#	2171	2175											
WLEN	001052	531#	1079*	1080*	1081	1100*	1101*	1102	1118*	1119*	1120	1138*	1139*	1140	
		1369*	1370*	1371	1396*	1397*	1398	1453*	1454*	1457	1472*	1473*	1476		

ADC	1994	2063													
ADD	21974	8755	1326	1360	1442	1507	1510	1524	1525	1529	1796	1868	1982	2062	2153
ASL	21574	21595	21655												
ASR	11795	22776	22777	2278											
BFC	10745	10999	1435												
BFD	97844	5688	604	617	628	645	662	679	692	705	718	731	744	779	792
BGE	97255	7688	791	795	798	801	815	821	831	835	844	848	859	872	965
BGT	1197	980	988	998	1001	1004	1008	1025	1028	1031	1057	1060	1064	1090	1129
BIC	11498	1223	1244	1254	1263	1267	1278	1295	1304	1380	1386	1407	1437	1441	1485
BIS	11901	1552	1527	1538	1552	1584	1586	1693	1697	1701	1705	1762	1766	1873	1875
BISB	2011	22014	2272												
BIT	1801	2270													
BLE	1801	660	677	690	703	716	729	742	777	820	895	914	934	1002	1195
BLT	12338	1349	1434	1513	1560	1589	1834	1880	1895	1919	1939	1963	2151	2243	2258
BMI	2137														
BNE	2639	2273	673	686	699	712	725	738	751	810	813	893	912	932	951
BPL	967	975	983	1430	1603	1879	1881	1852	1920	1940	1956				
BR	2280														
CLR	644	644	657	661	674	678	687	691	700	704	713	717	726	730	739
CMP	744	753	756	759	762	765	768	771	774	778	781	784	787	790	794
COM	797	800	885	889	904	909	924	928	943	947	964	969	971	976	979
DEC	797	997	997	1000	1003	1168	1196	1222	1291	1294	1303	1379	1406	1484	1583
EMT	1765	1855	1872	1874	1893	1900	1937	1957	1964	2093	2196	2210	2213		
HALT	2036	1968	1979	2044	2053										
INC	1899	1193	1200	1216	1219	1226	1317	1325	1327	1345	1357	1518	1565	1632	1774
	1914	1932	2144												
	551	641	658	675	688	701	714	727	740	754	757	760	763	766	769
	772	775	863	876	886	890	905	909	925	929	944	948	969	977	995
	1020	1052	1163	1166	1169	1282	1292	1354	1541	1555	1557	1768	1778	1856	1894
	1938	1965	2055	2057	2156	2167	2197	2211	2214	2239	2245	2260	2263	2267	2337
	99	1204	1231	1321	1509	1515	1562	1574	1803	1910	1928	2101	2104	2112	2117
	2125	214	2171	2177	2241	2297	2300	2346							
	51	54	572	896	915	935	1022	1035	1037	1054	1068	1070	1088	1109	1127
	1147	1328	1383	1384	1410	1411	1443	1464	1488	1489	1500	1511	1665	1713	1876
	1902	1980	1993	2016	2146	2168	2175	2218	2261	2268	2275	2283	2348	2352	2354
	497	498	569	855	856	857	869	870	954	962	974	982	990	1006	1012
	1016	1018	1036	1044	1048	1050	1069	1086	1107	1129	1145	1158	1184	1202	1210
	1274	1275	1276	1323	1340	1348	1352	1376	1403	1422	1428	1462	1481	1494	1495
	1503	1504	1535	1544	1549	1599	1600	1656	1659	1664	1675	1680	1707	1708	1710
	1747	1749	1750	1751	1752	1753	1754	1797	1805	1859	1871	1950	1976	1999	2000
	2009	2134	2135	2160	2161	2219	2254	2255	2292	2293	2294	2339			
	543	546	550	616	627	830	834	843	847	858	871	955	1027	1030	1034
	1059	1063	1067	1089	1128	1171	1188	1214	1253	1262	1266	1277	1385	1440	1497
	1500	1526	1537	1540	1551	1554	1556	1692	1696	1700	1798	1800	1897	1959	1967
	2033	22040	22054	22056	22098	2155	2200	2215	2238	2244	2266				
	1436	22054	22054	2269	2271	2336	2341	2343							
	1601	22012	2150												
	1137	1395	2162	2166	2173	2261									
	464														
	487	528	529	530	531	532	537	538	1609	1695	1699	1703	1764	1770	1776
	1780	1898	1912	1916	1930	1934	1952	2038	2126						
	188	1967	1971	1914	1961	1962	1019	1091	1150	1186	1212	1280	1281	1342	1351
	165	1378	1405	1439	1483	1496	1536	1550	1686	1687	1688	1689	1690	1691	1838

LIBRARY	NAME	LIBRARY	NAME	LIBRARY	NAME	LIBRARY	NAME	LIBRARY	NAME	LIBRARY	NAME
N	LIBRARY	N	LIBRARY	N	LIBRARY	N	LIBRARY	N	LIBRARY	N	LIBRARY
2026	SYMBOL	2040	SYMBOL	2051	SYMBOL	2087	SYMBOL	2090	SYMBOL	2191	SYMBOL
2026	SYMBOL	2040	SYMBOL	2051	SYMBOL	2087	SYMBOL	2090	SYMBOL	2191	SYMBOL
2026	SYMBOL	2040	SYMBOL	2051	SYMBOL	2087	SYMBOL	2090	SYMBOL	2191	SYMBOL
2026	SYMBOL	2040	SYMBOL	2051	SYMBOL	2087	SYMBOL	2090	SYMBOL	2191	SYMBOL
2026	SYMBOL	2040	SYMBOL	2051	SYMBOL	2087	SYMBOL	2090	SYMBOL	2191	SYMBOL
2026	SYMBOL	2040	SYMBOL	2051	SYMBOL	2087	SYMBOL	2090	SYMBOL	2191	SYMBOL
2026	SYMBOL	2040	SYMBOL	2051	SYMBOL	2087	SYMBOL	2090	SYMBOL	2191	SYMBOL
2026	SYMBOL	2040	SYMBOL	2051	SYMBOL	2087	SYMBOL	2090	SYMBOL	2191	SYMBOL

ERRORS DETECTED: 0
DEFAULT GLOBALS GENERATED: 0

* DZDRB SEQ/SOL/CRF/PAGNUM*LIB: SYSMAC.SML.DSK:DZDRB
RUN-TIME: 30.37 4 SECONDS
RUN-TIME RATIO: 171/71=2.42
CORE USED: 33K (65 PAGES)

