

# DT11

DIAGNOSTIC  
MD-11-DZDTA-B

EP-DZDTA-B-DL-A  
COPYRIGHT © 1976  
FICHE 1 OF 1

NOV 1976  
**digital**  
MADE IN U.S.A.

The image displays a grid of 144 small diagnostic charts or data tables arranged in 12 rows and 12 columns. Each cell contains technical information, likely related to the MD-11 aircraft diagnostic system. The charts vary in layout, including tables, flowcharts, and lists of data points. The text is small and difficult to read, but the overall structure is organized and systematic.

DT11

801

DZDTA-B MACY11 27(732) 27-OCT-76 15:57 PAGE 2  
DZDTA.B

.REM \*

IDENTIFICATION

PRODUCT CODE: MAINDEC-11-DZDTA-B  
PRODUCT NAME: DT11 DIAGNOSTIC  
DATE CREATED: 15 AUGUST 1972  
MAINTAINER: DIAGNOSTIC GROUP  
AUTHOR: RICK FADDEN

## 1. ABSTRACT

THIS PROGRAM IS DESIGNED TO TEST ALL THE FUNCTIONS OF THE DT11-A AND B BUS SWITCHES WHICH CAN BE TESTED WITHOUT ASSUMING SPECIFIC DEVICES TO BE ON THE SWITCHED BUS. A GREAT DEAL OF OPERATOR INTERVENTION IS REQUIRED DUE TO THE DUAL-PROCESSOR NATURE OF THE SWITCH AND THE VARIOUS MODES OF OPERATION CONTROLLED BY TWO TWO-POSITION SWITCHES. THIS OPERATOR INTERVENTION IS DIRECTED BY PRINTOUTS ON THE TELETYPE.

## 2. REQUIREMENTS

## 2.1 EQUIPMENT

PDP-11 FAMILY STANDARD COMPUTER(S)  
DT11-A OR -B BUS SWITCH

## 2.2 STORAGE

THE PROGRAM USES THE FIRST 5K OF MEMORY.  
THIS IS IN ACCORD WITH THE CURRENT RESTRICTION THAT BUS SWITCH SYSTEMS MUST HAVE AT LEAST 8K OF MEMORY ON THE PROCESSOR BUS(ES).

## 3. LOADING PROCEDURE

PROCEDURE FOR NORMAL ABSOLUTE TAPES SHOULD BE FOLLOWED.

## 4. STARTING PROCEDURE

## 4.1 CONTROL SWITCH SETTINGS

BASIC SWITCH REGISTER SETTINGS ARE:

SW15=1 OR UP --- HALT ON ERROR  
 SW14=1 OR UP --- SCOPE LOOP  
 SW13=1 OR UP --- INHIBIT ERROR PRINTOUT IF SCOPE LOOP IS REQUESTED  
 SW12=1 OR UP --- INHIBIT TRACE TRAPPING  
 SW11=1 OR UP --- INHIBIT SUBTEST ITERATION  
 SW10=1 OR UP --- INHIBIT POWER FAIL TESTING  
 SW09=1 OR UP --- INHIBIT MOST SWITCHED BUS POWER FAIL TESTING  
 (ONLY CHECK TO SEE THAT AC LO SETS)  
 SW08=1 OR UP --- INHIBIT ALL SWITCHED BUS POWER FAIL TESTING  
 (SET THIS SWITCH ONLY IF THERE IS NO DEVICE  
 ON THE SWITCHED BUS WHICH CAN BE POWERED DOWN)

## 4.2 STARTING ADDRESSES

200= BASIC LOGIC TESTING OF THE DT11-B  
 210= STARTING ADDRESS OF THE ROUTINE RUN ON THE OTHER  
 PROCESSOR WHEN A DT11-B IS BEING TESTED.

- 220= RESTART ADDRESS FOR BASIC LOGIC TESTING STARTING HERE SKIPS THE INITIAL REQUESTS FOR AN ADDRESS ON THE SWITCHED BUS, AND ASSUMES THE PREVIOUSLY GIVEN INFORMATION. USE FOR DT11-A OR B.
- 230= RESTART ADDRESS FOR SA 210. STARTING HERE ASSUMES THE INFORMATION PREVIOUSLY GIVEN.
- 240= SINGLE SUBTEST LOOP. ALLOWS RUNNING ANY DESIRED SUBTEST WITHOUT GOING THRU THE REST OF THE PROGRAM FIRST.
- 250= TIMER ADJUSTMENT LOOP. CODE REPEATEDLY FIRES THE TIMEOUT AND BUS INIT ONE-SHOTS.
- 260= BASIC LOGIC TESTING OF THE DT11-A

#### 4.3 PROGRAM AND/OR OPERATOR ACTION

##### 4.3.1 SA 200 (NORMAL TESTING, DT11-B)

1. LOAD THE PROGRAM INTO MEMORY OF PROCESSOR A.
2. LOAD THE PROGRAM INTO MEMORY OF PROCESSOR B.
3. PUT THE "MANUAL-PROGRAMMABLE" SWITCH IN "PROGRAMMABLE" POSITION.
4. PUT THE "INIT-INHIBIT INIT" SWITCH IN "INIT" POSITION.
5. PUT THE "HALT-ENABLE" SWITCH ON PROCESSOR B IN "HALT" POSITION, AND THEN PRESS "START" ON PROCESSOR B.
6. LOAD STARTING ADDRESS 200 ON PROCESSOR A.
7. SET DYNAMIC SWITCH REGISTER SWITCHES AS DESIRED ON PROCESSOR A (SEE 4.1).
8. PRESS START ON PROCESSOR A.
9. FOLLOW THE INSTRUCTIONS AS THEY ARE PRINTED OUT.
10. WHEN THE END OF PASS MESSAGE IS FINISHED PRINTING OUT, HALT PROCESSOR B.
11. PUT THE "HALT-ENABLE" SWITCH ON PROCESSOR A IN "HALT" POSITION.
12. PRESS "START" ON PROCESSOR A.
13. PUT THE "INIT-INHIBIT INIT" SWITCH IN "INIT" POSITION.
14. LOAD STARTING ADDRESS 200 ON PROCESSOR B.
15. SET SWITCH REGISTER SWITCHES AS DESIRED ON PROCESSOR B.
16. PRESS "START" ON PROCESSOR B.
17. FOLLOW THE INSTRUCTIONS AS THEY ARE PRINTED. WHEN THE END OF PASS MESSAGE IS FINISHED PRINTING, THE TEST IS COMPLETE.

SEE SECTION 5.3.1 FOR FURTHER OPERATING DETAILS.

##### 4.3.2 SA 210 (SWITCH REGISTER MONITOR - SARMON)

WHEN THE MAIN DIAGNOSTIC (SA 200) REACHES A POINT WHERE IT NEEDS TO HAVE OPERATIONS DONE TO THE OTHER SIDE OF THE SWITCH, A MESSAGE IS PRINTED REQUESTING THE OPERATOR TO START THE OTHER PROCESSOR AT SA 210. WHEN THE OTHER PROCESSOR IS STARTED AT 210, A GROUP OF PRINTOUTS WILL OCCUR REQUESTING INFORMATION. THIS INFORMATION MUST BE THE SAME AS THAT GIVEN TO THE PROCESSOR RUNNING THE MAIN DIAGNOSTIC WHEN IT WAS STARTED. SEE SECTION 5.2.9 FOR A COMPLETE DESCRIPTION OF THE INFORMATION NEEDED. NOTE THAT ONCE THIS INFORMATION HAS BEEN GIVEN, RESTART ADDRESS 230 MAY BE USED INSTEAD OF SA 210.

#### 4.3.3 SA 220 (RESTART NORMAL TESTING, DT11-A OR -B)

SA 220 IS THE SAME AS SA 200 OR 260, EXCEPT THAT INFORMATION INITIALLY REQUESTED WHEN USING SA 200 OR 260 IS ASSUMED TO BE PRESENT ALREADY WHEN SA 220 IS USED. THUS SA 220 SKIPS THE INITIAL TYPEOUTS.

#### 4.3.4 SA 230 (RESTART ADDRESS FOR SWITCH REGISTER MONITOR)

THIS RESTART ADDRESS SKIPS THE INITIAL REQUEST FOR INFORMATION MADE WHEN THE PROGRAM IS STARTED AT SA 210. THE INFORMATION GIVEN PREVIOUSLY IS USED.

#### 4.3.5 SA 240 (SINGLE SUBTEST LOOP)

1. LOAD SA 240 AND PRESS "START"
2. AT THE FIRST HALT, LOAD THE ADDRESS OF THE TEST DESIRED (THE ADDRESS OF THE TESTXX TAG) INTO THE SWITCH REGISTER. THEN PRESS "CONTINUE"
3. AT THE SECOND HALT, SET THE CONTROL SWITCH REGISTER SETTING DESIRED. (SM11 MUST BE SET TO ZERO). THEN PRESS CONTINUE.
4. THE DESIRED SUBTEST WILL BE REPEATEDLY EXECUTED. SETTING SM11 WILL RETURN THE PROGRAM TO THE NORMAL FLOW.

#### 4.3.6 SA 250 (ADJUST TIMERS LOOP)

LOAD BOTH PROCESSORS WITH STARTING ADDRESS 250, THEN PRESS "START" ON BOTH PROCESSORS. THE LOOP WILL NOT FUNCTION IF RUN ON ONLY ONE PROCESSOR.

#### 4.3.7 SA 260 (NORMAL TESTING, DT11-A)

1. LOAD THE PROGRAM USING THE ABS LOADER
2. PUT THE "MANUAL-PROGRAMMABLE" SWITCH IN "PROGRAMMABLE"
3. PUT THE "INIT-INHIBIT INIT" SWITCH IN "INIT"
4. LOAD STARTING ADDRESS 260
5. SET DYNAMIC SWITCH REGISTER SWITCHES (SEE 4.1)
6. PRESS START
7. FOLLOW THE INSTRUCTIONS AS THEY ARE PRINTED OUT

#### 5. OPERATING PROCEDURE

##### 5.1 OPERATIONAL SWITCH SETTINGS

SEE SECTION 4.1

5.2 SUBROUTINE ABSTRACTS

5.2.1 BEGIN SA 200 FOR DT11-B, SA 260 FOR DT11-A

5.2.2 SCOPEC

THIS SUBROUTINE IS CALLED BY A TRAP CALL (SCOPE) PLACED BETWEEN EACH SUBTEST. IT RECORDS THE STARTING ADDRESS OF EACH SUB-TEST AS IT IS BEING ENTERED. IF A SCOPE LOOP IS REQUESTED, IT WILL JUMP TO THE START OF THE SUBTEST THAT THE SCOPE LOOP IS REQUESTED FOR. IF SCOPE LOOP IS NOT REQUESTED, THERE WILL BE 64 ITERATIONS ON THAT SUBTEST BEFORE THE NEXT SUBTEST IS ENTERED. SWITCH 11 ON A 1 INHIBITS ITERATION OF SUBTESTS.

5.2.3 PRINT

THIS ROUTINE IS CALLED BY A TRAP CALL (HLT) WHEN AN ERROR IS DETECTED. IT PRINTS OUT THE LOCATION COUNTER AND THE CONTENTS OF THE PROCESSOR STATUS REGISTER AT THE TIME OF FAILURE. NOTE THAT THE LOCATION COUNTER WILL BE THE ADDRESS OF THE HLT PLUS TWO.

5.2.4 TTRAP AND TRCK

THESE ROUTINES ALLOW THE TRACE BIT TO BE SET ON ALTERNATE LOOPS OF THE PROGRAM. THE FIRST INSTRUCTION EXECUTED UPON TRAPPING IS AN "RTI" (OR "RTT" ON THE 11/45) WHICH RETURNS TO THE INTERRUPTED SEQUENCE. THIS CONTINUES UNTIL THE END OF THE PROGRAM LOOP IS REACHED.

5.2.5 TRAPCATCHER

THIS IS A SERIES OF INSTRUCTIONS STARTING AT LOCATION 0 DESIGNED TO DETECT AND ISOLATE UNEXPECTED TRAPS AND INTERRUPTS TO THE TRAP AND INTERRUPT VECTOR AREA OF MEMORY.

EACH VECTOR ENTRANCE ADDRESS IS LOADED WITH THE ADDRESS OF THE NEXT LOCATION. THE NEXT LOCATION IS LOADED WITH A HALT (000000). THIS AN ILLEGAL TRAP OR INTERRUPT WILL CAUSE A HALT AT THE TRAP LOCATION PLUS TWO.

IF A HALT OCCURS IN THE TRAP OR INTERRUPT AREA, EXAMINE REGISTER SIX. IT WILL CONTAIN THE CURRENT STACK ADDRESS. THE CONTENTS OF THE CURRENT STACK ADDRESS IS THE VALUE OF THE LOCATION COUNTER WHEN THE TRAP OR INTERRUPT OCCURRED.

5.2.6 TESTX (SINGLE TEST LOOP)

THIS ROUTINE ALLOWS A SINGLE SUBTEST TO BE RUN CONTINUOUSLY FOR SCOPE LOOP PURPOSES. WHILE A SCOPE LOOP SWITCH OPTION EXISTS, IT REQUIRES THAT YOU ARE WITHIN THE TEST IN WHICH YOU WISH TO LOOP. THIS SUBROUTINE ALLOWS YOU TO LOAD THE ADDRESS OF ANY SUBTEST AND THEN GO DIRECTLY TO THAT TEST.

5.2.7 SRMON (SWITCH REGISTER MONITOR)

THIS ROUTINE IS RUN ON PROCESSOR B WHILE THE A SIDE OF THE SWITCH IS BEING CHECKED, AND ON PROCESSOR A WHILE THE B SIDE OF THE SWITCH IS BEING CHECKED. IT MONITORS THE PROCESSOR SWITCH REGISTER, AND RUNS VARIOUS ROUTINES DEPENDING ON WHICH SWITCH IS SET.

5.2.8 TOUT AND TYPE

THESE ROUTINES PRINT ASCII MESSAGES. TOUT IS CALLED REPEATEDLY BY THE ROUTINE TYPE TO OUTPUT MESSAGES COMPOSED OF ASCII STRINGS. EACH MESSAGE IS GIVEN A MESSAGE TABLE, WHICH IS SIMPLY A LIST OF THE ADDRESSES OF THE ASCII STRINGS WHICH MUST BE TYPED TO CREATE THE FULL MESSAGE. CORE IS THUS CONSERVED BY ELIMINATING DUPLICATE PORTIONS OF STORED MESSAGES.

5.2.9 INFORM

THIS ROUTINE REQUESTS AND STORES THE INFORMATION NECESSARY TO CHECK A LOCATION ON THE SWITCHED BUS. IF ANY NPR DEVICES ARE ON THE SWITCHED BUS, THE ADDRESS OF ONE OF THE WORD COUNT OR BUS ADDRESS REGISTERS SHOULD BE GIVEN. THIS WILL ALLOW INIT ON THE SWITCHED BUS TO BE CHECKED, SINCE THE REGISTER CAN BE SET TO MINUS ONE AND THEN CLEARED BY INIT. IF NO WORD COUNT OR BUS ADDRESS REGISTER IS LOCATED ON THE SWITCHED BUS, GIVE THE ADDRESS OF ANY REGISTER WHICH HAS AT LEAST ONE BIT THAT CAN BE SET BY THE PROGRAM AND CLEARED BY INIT. IF THERE ARE NO LOCATIONS ON THE SWITCHED BUS SATISFYING THIS, GIVE AN ADDRESS OF A READ/WRITE LOCATION ON THE SWITCHED BUS (SUCH AS A MEMORY LOCATION). IN THIS CASE, INIT CANNOT BE TESTED ON THE SWITCHED BUS, BUT TESTS CAN BE MADE TO SEE IF THE SWITCH CAN CONNECT THE SWITCHED BUS TO THE PROCESSOR BUS.

THERE ARE 3 HALTS REQUESTING INFORMATION. AT THESE HALTS, SET THE NUMBER REQUIRED IN THE SWITCH REGISTER SWITCHES, AND THEN PRESS CONTINUE. THE INFORMATION NEEDED IS:

- 1ST HALT - ADDRESS OF A SWITCHED BUS LOCATION, AS DESCRIBED IN THE PREVIOUS PARAGRAPH
- 2ND HALT - THE BITS THAT ARE READ/WRITE IN THAT LOCATION (THOSE BITS THAT CAN BE SET TO ONE AND CLEARED TO ZERO BY A DATO FROM THE CPU- DON'T INCLUDE INTERRUPT ENABLE)
- 3RD HALT - THE BITS THAT ARE CLEARED BY INIT IN THAT LOCATION.

NOTE THAT AT THE SECOND HALT, IF THE ADDRESS GIVEN WAS THAT OF A CONTROL STATUS REGISTER, INTERRUPT ENABLE SHOULD NOT BE INCLUDED AS A READ/WRITE BIT.

#### 5.2.10 EMTSRV (EMT DECODER)

ALL MESSAGE PRINTOUTS ARE CALLED BY EMTS. THESE EMT CALLS ARE DECODED BY EMTSRV, WHICH SETS UP THE ADDRESS OF THE MESSAGE REQUESTED AND THEN CALLS THE TYPE ROUTINE.

#### 5.2.11 TRPSRV (TRAP DECODER)

HLT (ERROR PRINTOUT CALL) AND SCOPE (SCOPE AND ITERATION LOOP CALL) ARE BOTH CODED AS TRAPS. TRPSRV DECODES THESE CALLS AND GOES TO THE DESIRED ROUTINE. THERE IS ALSO ROOM AVAILABE TO USE TRAP CALLS 104400, 104402, AND 104404 AS CALLS ON ROUTINES SETUP BY THE USER. THE ADDRESS OF THE CORRESPONDING ROUTINE IS LOADED IN THE 1ST, 2ND, OR 3RD LOCATION OF THE TRAP TABLE (TPTAB) AND TRPSRV WILL ESSENTIALLY JUMP TO THE DESIRED ROUTINE WHEN THE TRAP CALL OCCURS. THE ROUTINE ADDED BY THE USER SHOULD PASS CONTROL BACK TO THE LOCATION AFTER THE CALL BY ENDING WITH AN RTI.

#### 5.3 PROGRAM AND/OR OPERATOR ACTION

##### 5.3.1 SA 200 (BASIC LOGIC TEST FOR THE DT11-B)

FOR A BASIC OUTLINE OF OPERATOR ACTION REQUIRED TO TEST THE DT11-B, SEE SECTION 4.3.1.



5.3.1 CONTINUED

THE PROGRAM INITIALLY CHECKS ALL FEATURES OF THE SWITCH WHICH CAN BE TESTED WITHOUT OPERATOR INTERVENTION. WHEN THESE TESTS ARE COMPLETE, THE PROGRAM PRINTS DIRECTIONS ON THE TELETYPE. AFTER A FEW TESTS OF FUNCTIONS RELATED TO THE "INIT-INHIBIT INIT" SWITCH, THE OPERATOR IS INSTRUCTED TO START THE OTHER PROCESSOR AT SA 210. THIS IS THE STARTING ADDRESS OF THE SWITCH REGISTER MONITOR ROUTINE (SRMON). SRMON RUNS VARIOUS SUBROUTINES DEPENDING ON WHICH SWITCHES ARE SET IN THE SWITCH REGISTER. THE REMAINING TESTS IN THE PROGRAM DIRECT THE OPERATOR TO SET AND CLEAR VARIOUS SWITCHES IN THE SWITCH REGISTER OF THE PROCESSOR RUNNING THE SRMON ROUTINE. WHEN THE OPERATOR FOLLOWS THESE INSTRUCTIONS, HE CAUSES THE NECESSARY SUBROUTINES TO BE SELECTED. THE SUBROUTINES PERFORM SUCH FUNCTIONS AS REQUESTING AND RELEASING THE BUS SWITCH, SETTING AND CLEARING THE COMMUNICATION BIT, CHECKING AC LO (BIT 4 IN THE DT11 CSR), AND RUNNING VARIOUS POWER FAIL TESTS. AT THE END OF THESE TESTS, THE PROGRAM REQUESTS THAT THE "INIT-INHIBIT INIT" SWITCH BE SET TO "INHIBIT INIT". MOST OF THE PROGRAM IS THEN REPEATED WITH THE SWITCH SET TO "INHIBIT INIT" TO MAKE SURE THAT ALL OTHER BUS SWITCH FUNCTIONS STILL WORK IN THIS MODE. WHEN THE PROGRAM PRINTS OUT "END OF PASS", A FULL TEST PASS HAS BEEN COMPLETED ON ONE SIDE OF THE SWITCH.

A NUMBER OF TESTS ARE INCLUDED WHICH CHECK POWER FAIL. THESE TESTS REQUIRE THE SYSTEM TO HAVE EACH BUS SEPARATELY POWERED, SO THAT POWERING DOWN ONE PROCESSOR, FOR EXAMPLE, DOES NOT ALSO POWER DOWN A DEVICE ON THE SWITCHED BUS. IF THE SYSTEM IS NOT SET UP IN THIS FASHION, THESE TESTS WILL FAIL. IF THE SYSTEM IS NOT INTENDED TO FUNCTION IN POWER FAIL APPLICATIONS SUCH AS THOSE REQUIRING HIGH RELIABILITY, THESE TESTS DO NOT NEED TO BE RUN. SETTING SWITCH 10 WILL INHIBIT POWER FAIL TESTING.

5.3.2 TO ADJUST THE TIMEOUT, NO MASTER SYNC, AND SWITCHED BUS INIT TIMERS, USE SA 250. (SEE 4.3.3). THIS ROUTINE, WHEN RUN ON BOTH PROCESSORS, WILL REPEATEDLY RETRIGGER EACH OF THESE ONE-SHOTS, SO THAT THEIR OUTPUTS CAN BE SCOPED EASILY.

5.3.3 TO GO DIRECTLY TO A SINGLE SUBTEST AND RUN IT CONTINUOUSLY, USE SA 240. INPUT THE STARTING ADDRESS OF THE DESIRED TEST (I.E., THE ADDRESS OF THE CORRESPONDING TESTXX TAG) AT THE INITIAL HALT AND PRESS CONTINUE. AT THE NEXT HALT, SET THE SWITCH REGISTER OPTIONS AS DESIRED (SWITCH 11 MUST BE DOWN), THEN PRESS CONTINUE. THIS FEATURE IS ESPECIALLY USEFUL WHEN FAILURES OCCUR WHILE RUNNING THE SECTION REQUIRING OPERATOR INTERVENTION.

6. ERRORS

6.1 ERROR PRINTOUT

PRINTOUTS ARE IN A STANDARD TWO WORD FORMAT. THE FIRST WORD IS THE OCTAL VALUE OF THE PC+2 OF THE DETECTED ERROR. THE SECOND IS THE CONTENTS OF THE PROCESSOR STATUS REGISTER WHEN THE ERROR WAS DETECTED.

6.2 ERROR RECOVERY

IN GENERAL, TEST FAILURES WILL PRINTOUT AN ERROR MESSAGE AND CONTINUE. IF THE "HALT ON ERROR" SWITCH IS SET, HITTING CONTINUE WILL RECOVER. IF THE PROGRAM HANGS UP IN A LOOP, THE ERROR IS LIKELY TO BE A SIGNAL WHICH WAS NEVER RECEIVED. IF A HALT OCCURS IN THE TRAP AND VECTOR AREA THE PROGRAM MUST BE RESTARTED. IF THE PROGRAM HALTS IN THE MAIN FLOW, CONSULT THE LISTING IF NO MESSAGE IS TYPED OUT.

7. RESTRICTIONS

7.1 STARTING PROCEDURE

NONE

7.2 OPERATIONAL RESTRICTIONS

NONE

8. MISCELLANEOUS

8.1 EXECUTION TIME

OPERATOR DEPENDENT. WHEN DONE, THE PROGRAM PRINTS OUT "END OF PASS".

8.2 TESTING SYSTEMS WITH MORE THAN ONE DT11

BY SUBSTITUTING INTO THE LOCATIONS BUSCSR, BUSCRH, BUSIV1, BUSST1, BUSIV2, AND BUSST2, THE ADDRESSES OF THE CSR, THE CSR HIGH BYTE, INTERRUPT VECTOR AND INTERRUPT STATUS ONE, AND INTERRUPT VECTOR AND INTERRUPT STATUS TWO, A DT11 MAY BE TESTED AT ANY ADDRESS ASSIGNED TO IT.

8.3 MESSAGE PRINTOUTS

THE DUAL-PROCESSOR NATURE OF THE BUS SWITCH REQUIRES A GREAT DEAL OF OPERATOR INTERVENTION TO TEST THE SWITCH. THE MESSAGES DIRECTING THIS OPERATOR ACTION MAY AT TIMES BE REDUNDANT, REQUESTING THE OPERATOR TO CLEAR A SWITCH REGISTER THAT ALREADY IS CLEAR. FOR EXAMPLE, THESE REDUNDANT MESSAGES ARE ACTUALLY IN SEPARATE TESTS, AND ARE INCLUDED ONLY TO ALLOW CORRECT OPERATOR ACTION IF SCOPE LOOPING ON A SINGLE SUBTEST IS REQUESTED. WHEN THEY OCCUR, SIMPLY MAKE SURE THAT THE CONDITIONS REQUESTED ARE CORRECTLY SETUP AND THEN GO ON.

9. PROGRAM DESCRIPTION

THIS SET OF TESTS IS DESIGNED TO TEST ALL OPERATIONS OF THE DT11-A AND B BUS SWITCHES, WITH THE NECESSARY EXCEPTION THAT FEATURES INVOLVING USE OF A SPECIFIC DEVICE ON THE SWITCHED BUS ARE NOT TESTED (I.E., ADDRESS AND DATA LINES ARE NOT FULLY TESTED). THE FEATURES NOT FULLY TESTED BY THE PROGRAM MAY BE TESTED BY PLACING THE SWITCH IN "MANUAL" AND RUNNING THE STANDARD DIAGNOSTICS OF ALL DEVICES ON THE SWITCHED BUS.

10. LISTING

SEE FOLLOWING PAGES.

11. FLOWCHART

NOT APPLICABLE - TEST BASICALLY IS STRAIGHT-LINE CODING.

\*  
:DIAGNOSTIC FOR DT11-A AND -B BUS SWITCHES  
:COPYRIGHT 1972, DIGITAL EQUIPMENT CORP., MAYNARD, MASS.

\*\*\*\*\*  
:OPERATING INSTRUCTIONS - BASIC LOGIC TEST FOR THE DT11-B (SA 200, RESTART 220)  
1. LOAD TAPE WITH THE ABSOLUTE LOADER INTO BOTH PROCESSORS  
2. LOAD STARTING ADDRESS 200 ON THE SIDE BEING TESTED.  
3. SET THE "INIT-INHIBIT INIT" SWITCH TO "INIT"  
4. SET THE "MANUAL-PROGRAMMABLE" SWITCH TO "PROGRAMMABLE"  
5. PUT THE HALT SWITCH ON THE OTHER PROCESSOR IN "HALT" POSITION  
AND THEN PRESS START ON THAT PROCESSOR (TO INIT THE BUS SWITCH)  
6. SET THE DESIRED DYNAMIC SWITCH REGISTER SWITCHES.  
7. PRESS START ON THE PROCESSOR RUNNING THE TEST  
8. FOLLOW THE DIRECTIONS AS THEY ARE PRINTED OUT.  
9. WHEN THE PROCESSOR BEGINS THE SECTION REQUIRING BOTH CPU'S,  
A MESSAGE REQUESTING THAT THE OTHER CPU BE STARTED  
AT 210 IS PRINTED OUT. AT THAT TIME, LOAD  
STARTING ADDRESS 210 ON THE OTHER PROCESSOR AND PRESS START.  
10. WHEN THE END OF PASS MESSAGE IS PRINTED OUT, STOP THE PROCESSOR BEING TESTED  
AND START THE OTHER PROCESSOR AT 200. REPEAT THE PROCEDURE FROM (3) THRU (9),  
NOW TESTING THE SECOND SIDE OF THE SWITCH.  
\*\*\*\*\*

:OPERATING INSTRUCTIONS - BASIC LOGIC TEST FOR THE DT11-A (SA 260, RESTART 220)  
1. LOAD TAPE WITH THE ABS LOADER  
2. LOAD STARTING ADDRESS 260  
3. SET THE "INIT-INHIBIT INIT" SWITCH TO "INIT"  
4. SET THE "MANUAL-PROGRAMMABLE" SWITCH TO "PROGRAMMABLE"  
5. SET THE DESIRED DYNAMIC SWITCH REGISTER SWITCHES  
6. PRESS START  
7. FOLLOW THE DIRECTIONS AS THEY ARE PRINTED OUT

:OPERATING INSTRUCTIONS - SINGLE SUBTEST LOOP (SA 240)  
1. LOAD SA 240  
2. PRESS "START"  
3. AT THE FIRST HALT, LOAD THE ADDRESS OF THE TEST DESIRED  
(THE ADDRESS OF THE TESTXX TAG) INTO THE SWITCH  
REGISTER, THEN PRESS "CONTINUE"  
4. AT THE SECOND HALT, SET THE CONTROL SWITCH REGISTER SETTING  
DESIRED, THEN PRESS "CONTINUE" (SW11 MUST BE = 0)  
5. THE DESIRED SUBTEST WILL BE REPEATEDLY EXECUTED. SETTING  
SWITCH 11 WILL RETURN THE PROGRAM TO THE NORMAL  
FLOW.

:OPERATING INSTRUCTIONS - TIMER ADJUSTMENT LOOP (SA 250)  
1. PUT THE "INIT-INHIBIT INIT" SWITCH IN "INIT" POSITION  
2. PUT THE "MANUAL - PROGRAMMABLE" SWITCH IN "PROGRAMMABLE"  
3. LOAD SA 250 ON ONE PROCESSOR AND PRESS "START"  
4. LOAD SA 250 ON THE OTHER PROCESSOR AND PRESS "START".  
5. THE ROUTINE WILL SWITCH THE SWITCH BACK AND FORTH  
BETWEEN THE PROCESSORS, USING TIMEOUT ON EACH SIDE.  
THE USE OF A WAIT INSTRUCTION AND INTERRUPT ENABLE ON  
THE SIDE THAT DOESN'T HAVE THE SWITCH SIMPLIFIES  
ADJUSTMENT OF THE NO MSYN TIMER.

;STARTING ADDRESSES ARE:

- 200 - STANDARD STARTING ADDRESS FOR MAIN DIAGNOSTIC
- 210 - STARTING ADDRESS OF THE ROUTINE RUN ON THE OTHER PROCESSOR WHEN A DT11-B IS BEING TESTED
- 220 - DIAGNOSTIC RESTART ADDRESS. STARTING HERE SKIPS THE INITIAL REQUESTS FOR AN ADDRESS ON THE SWITCHED BUS, AND ASSUMES THE PREVIOUSLY GIVEN INFORMATION (USE AFTER SA 200 OR SA 260)
- 230 - RESTART ADDRESS OF THE ROUTINE RUN ON THE OTHER PROCESSOR WHEN A DT11-B IS BEING TESTED. THE PREVIOUSLY GIVEN INFORMATION IS ASSUMED.
- 240 - SINGLE SUBTEST LOOP. ALLOWS RUNNING ANY DESIRED SUBTEST WITHOUT GOING THRU THE REST OF THE PROGRAM FIRST.
- 250 - TIMER ADJUSTMENT LOOP. CODE REPEATEDLY FIRES THE TIMEOUT AND BUS INIT ONE - SHOTS.
- 260 - BASIC LOGIC TEST OF THE DT11-A

;SWITCH REGISTER SETTINGS

- ;SW15=1 OR UP - HALT ON ERROR
- ;SW14=1 OR UP - LOOP ON CURRENT TEST (SCOPE LOOP)
- ;SW13=1 OR UP - INHIBIT PRINT OUT IF LOOPING
- ;SW12=1 OR UP - INHIBIT TRACE TRAPPING
- ;SW11=1 OR UP - INHIBIT ITERATIONS OF SUBTESTS
- ;SW10=1 OR UP - INHIBIT POWER FAIL TESTS
- ;SW09=1 OR UP - INHIBIT MOST SWITCHED BUS POWER FAIL TESTING  
 ;(JUST CHECK TO SEE THAT AC LO SETS SOMETIME)
- ;SW08=1 OR UP - INHIBIT ALL SWITCHED BUS POWER FAIL TESTING  
 ;(USE ONLY IF NO DEVICE ON THE SWITCHED BUS CAN  
 ;BE POWERED DOWN)

;DEFINITIONS

- NOP=240
- R0=%0
- R1=%1
- R2=%2
- R3=%3
- R4=%4
- R5=%5
- SP=%6
- PC=%7

;LOAD TRAP CATCHER IN LOCATIONS 0 TO 377  
 ;EACH VECTOR ENTRANCE ADDRESS IS LOADED WITH THE ADDRESS OF THE  
 ;NEXT LOCATION. THE NEXT LOCATION IS LOADED WITH A HALT (000000).  
 ;THUS AN ILLEGAL TRAP OR INTERRUPT WILL CAUSE A HALT AT THE TRAP LOCATION  
 ;PLUS TWO.

;LOAD VECTOR AREA

000030 021236  
 000032 000340  
 000034 021432  
 000036 000340  
 000014

.=30  
 EMTSRV  
 340  
 TRPSRV  
 340  
 .=14

000014 001044  
000016 000340

TTRAP  
340

;LOAD STARTING AREA

000200	000200		. = 200	
000204	012706	001000	MOV	#STACK, SP
	000167	000724	JMP	START
000210	000210		. = 210	
000214	012706	001000	MOV	#STACK, SP
	000167	015672	JMP	SRMONX
000220	000220		. = 220	
000224	012706	001000	MOV	#STACK, SP
	000167	000726	JMP	RSTART
000230	000230		. = 230	
000234	012706	001000	MOV	#STACK, SP
	000167	015660	JMP	SRMONX+6
000240	000240		. = 240	
000244	012706	001000	MOV	#STACK, SP
	000167	021234	JMP	TESTX
000250	000250		. = 250	
000254	012706	001000	MOV	#STACK, SP
	000167	020716	JMP	TIMERS
000260	000260		. = 260	
000264	012706	001000	MOV	#STACK, SP
	000167	000620	JMP	DT11A

;LOAD DATA AREA

001000	001000		. = 1000	
	000000		STACK:	0
	0C1012		. = +10	
001012	177420		BUSCSR:	177420
001014	177421		BUSCRH:	177421
001016	000300		BSIV1:	300
001020	000302		BSST1:	302
001022	000304		BSIV2:	304
001024	000306		BSST2:	306
001026	177564		TCSR:	177564
001030	177566		TDBR:	177566
001032	177560		TKR:	177560
001034	177776		PSR:	177776
001036	177570		SR:	177570
001040	177772		PIRQ:	177772
001042	000000		INTFLG:	0
001044	000002		TTRAP:	RTI
001046	000000		CNT40:	0
001050	000000		CNT40A:	0
001052	000000		SBINH:	0
001054	000000		DVADRS:	0
001056	000000		RMBITS:	0
001060	000000		INBITS:	0
001062	000000		ANDBTS:	0
001064	000000		ANDCOM:	0
001066	000000		COUNT:	0
001070	000000		SPSAV:	0
001072	000000		PFSAV:	0

; IN CASE STACK OVERRUNS  
; ADDRESS OF DT11 CSR  
; ADDRESS OF DT11 CSR, HIGH BYTE  
; ADDRESS OF INTERRUPT VECTOR 1  
  
; ADDRESS OF INTERRUPT VECTOR 2  
  
; TELETYPE REGISTERS  
  
; PROCESSOR STATUS REGISTER  
; SWITCH REGISTER  
  
; INTERRUPT TEST INFORMATION  
; TRACE TRAP RETURN (SET TO RTT IF 11/45)

; FLAG INDICATING SR9 IS SET (IF LOW BYTE IS NOT ZERO)  
; FLAG INDICATING SR8 IS SET (IF HIGH BYTE IS NOT ZERO)  
; LOADED WITH ADDRESS OF A DEVICE REGISTER ON THE SWITCHED BUS  
; INDICATES THE BITS THAT ARE R/W IN THE DEVICE REGISTER  
; INDICATES THE BITS THAT ARE CLEARED BY INIT  
; LOGICAL AND OF INBITS AND RMBITS  
; COMPLEMENT OF ANDBTS

; STORAGE FOR STACK POINTER IN POWER FAIL TESTS  
; STORAGE FOR CONTENTS OF CSR WHEN POWER DOWN OCCURS

001074	000000			SHORTF:	0				:INDICATES FULL TEST HAS ALREADY BEEN RUN
001076	000000			INITF:	0				:INDICATES THAT CURRENT PASS IS BEING RUN
									:WITH "INHIBIT-INIT" SET
001100	000000			TFLAG:	0				:INDICATES TRACE BIT SHOULD BE SET ON CURRENT PASS
001102	000000			NOPF:	0				:INDICATES POWER FAIL IS NOT BEING TESTED
001104	000000			DT11AF:	0				:SET NONZERO TO INDICATE TESTING A DT11-A
001106	000000			TSTX:	0				:SET TO INDICATE RUNNING SINGLE SUBTEST STARTUP

001110	012767	000001	177766	DT11A:	MOV	#1,DT11AF			:SET FLAG INDICATING TESTING A DT11-A
001116	005067	177720			CLR	INTFLG			
001122	004767	000036			JSR	X7,SETUP			
001126	004767	017742			JSR	X7,INFORM			
001132	000515				BR	BEGIN			
001134	005067	177744		START:	CLR	DT11AF			
001140	005067	177676			CLR	INTFLG			
001144	004767	000014			JSR	X7,SETUP			
001150	004767	017720			JSR	X7,INFORM			:REQUEST INFORMATION ABOUT A LOCATION
									:ON THE SWITCHED BUS
001154	000504				BR	BEGIN			
001156	004767	000002		RSTART:	JSR	X7,SETUP			
001162	000501				BR	BEGIN			
001164	005067	177704		SETUP:	CLR	SHORTF			:CLEAR FLAGS
001170	005067	177702			CLR	INITF			
001174	005067	177700			CLR	TFLAG			
001200	005067	177702			CLR	TSTX			
001204	005077	177624			CLR	SPSR			:INITIALIZE PROCESSOR STATUS
001210	005067	020516			CLR	ERR			:INITIALIZE FLAG TO INDICATE NO ERRORS SO FAR
001214	032777	002000	177614		BIT	#2000,JSR			:CK SR10
001222	001404				BEG	.+12			:SKIP IF NOT SET
001224	012767	177777	177650		MOV	#-1,NOPF			:SET FLAG IF SET
001232	000402				BR	.+6			
001234	005067	177642			CLR	NOPF			:CLEAR FLAG IF NOT SET
001240	005067	177506			CLR	SBINH			
001244	032777	001000	177564		BIT	#1000,JSR			
001252	001402				BEG	.+6			
001254	005267	177572			INC	SBINH			:SET LOW BYTE IF SW9 IS SET
001260	032777	000400	177550		BIT	#400,JSR			
001266	001402				BEG	.+6			
001270	105267	177557			INCB	SBINH+1			:SET HIGH BYTE IF SW8 IS SET
001274	016777	177520	177514		MOV	BSS:1,JSIV1			
001302	016777	177516	177512		MOV	BSS:2,JSIV2			
001310	005077	177504			CLR	BSS:1			
001314	005077	177504			CLR	BSS:2			
001320	012737	001346	000004		MOV	#TRET,#4			:SETUP BUS ADDRESS TRAP RETURN
001326	005037	000006			CLR	#6			
001332	005777	177502			TST	#PIRQ			
001336	012737	000006	001044		MOV	#ATT,#ATTRAP			:IF NO TRAP THIS IS AN 11/45
001344	000404				BR	.+12			
001346	012737	000002	001044	TRET:	MOV	#ATT,#ATTRAP			:IF TRAP, NOT AN 11/45
001354	022626				CHP	(SP)+,(SP)+			:RESTORE STACK POINTER
001356	012737	000006	000004		MOV	#6,#4			

```

001364 000207
001366 012767 000100 020722 BEGIN: RTS X7
001374 012767 001414 020720 MOV #100,ICOUNT
MOV #TEST1+2,RETURN

;CHECK FOR CSR CORRECTLY INITIALIZED VIA START SWITCH - NO SCOPE LOOP
001402 005777 177404 TST #BUSCSR ;TEST CSR FOR ALL ZERO
001406 001401 BEQ .+4
001410 104410 HLT ;NOT ALL ZEROES IN CSR

;CHECK TO SEE IF ALL BITS RESPOND CORRECTLY TO DATO OF A ONE TO EACH BIT
;CHECK CSR INITIALIZED CORRECTLY VIA RESET, AND THAT RESET DISCONNECTS THE SWITCH
;IF IT WAS PREVIOUSLY CONNECTED
;SHOW THAT BIT 9 STAYS SET FOR SEVERAL MICROSECONDS, THEN CLEARS
001412 104406 TEST1: SCOPE
001414 012777 176177 177370 MOV #176177,#BUSCSR ;DATO ALL ONES EXCEPT IE1, DONE, AND RESET
001422 005767 177456 TST DT11AF ;IS THIS A DT11-A?
001426 001406 BEQ CNT1 ;NO- BRANCH
001430 022777 020203 177354 CMP #20203,#BUSCSR ;CHECK FOR CORRECT BITS SET IF DT11-A
001436 001401 BEQ .+4
001440 104410 HLT ;INCORRECT BITS SET
001442 000405 BR CNT1A
001444 022777 026203 177340 CNT1: CMP #26203,#BUSCSR ;CHECK FOR CORRECT BITS SET,DT11-B
001452 001401 BEQ .+4
001454 104410 HLT ;BITS SET INCORRECTLY
001456 105777 177344 CNT1A: TSTB #TCSR ;MAKE SURE TTY IS INACTIVE BEFORE ISSUING RESET
001462 100375 BPL .-4
001464 000005 RESET ;RESET SHOULD CLEAR ALL BITS IN THE CSR
001466 032777 001000 177316 BIT #1000,#BUSCSR ;WAIT FOR SB INIT TO CLEAR IN CASE OF VERY LONG INIT
001474 001374 BNE .-6
001476 005777 177310 TST #BUSCSR ;CSR ALL ZERO?
001502 001401 BEQ .+4 ;YES - CONTINUE
001504 104410 HLT ;NO - PROCESSOR RESET DIDN'T CLEAR CSR
001506 052777 000600 177276 BIS #600,#BUSCSR ;SET INTERRUPT ENABLE AND TRY TO SET BIT 7
001514 022777 000400 177270 CMP #400,#BUSCSR ;CHECK FOR ONLY INTERRUPT ENABLE (BIT 8) SET
001522 001401 BEQ .+4
001524 104410 HLT ;BITS INCORRECTLY SET IN CSR
001526 105777 177274 TSTB #TCSR ;MAKE SURE TTY IS INACTIVE BEFORE ISSUING RESET
001532 100375 BPL .-4
001534 000005 RESET ;RESET SHOULD CLEAR ALL BITS IN THE CSR
001536 005777 177250 TST #BUSCSR ;CSR ALL ZERO?
001542 001401 BEQ .+4 ;YES - CONTINUE
001544 104410 HLT ;NO - RESET DIDN'T CLEAR CSR
001546 032777 000020 177260 BIT #20,#PSR ;CHECK TRACE BIT
001554 001026 BNE CONT1 ;IF SET, SKIP TEST OF BIT 9 (DUE TO TIMING)
001556 016701 177230 MOV #BUSCSR,R1 ;LOAD R1 WITH ADDRESS OF CSR
001562 012777 000001 177222 MOV #1,#BUSCSR ;REQUEST SWITCH
001570 052777 001000 177214 BIS #1000,#BUSCSR ;SET BUS SWITCH RESET
001576 031127 001000 BIT #R1,#1000 ;BIT 9 SHOULD STAY SET AT LEAST 10 US.
001602 001001 BNE .+4
001604 104410 HLT ;BIT 9 DIDN'T STAY SET AT LEAST 10 US.
001606 005027 000000 CLR #0 ;STALL
001612 005367 177772 DEC .-2
001616 001375 BNE .-4
001620 032777 001000 177164 BIT #1000,#BUSCSR ;CHECK BIT 9 - SHOULD BE CLEAR BY NOW
001626 001401 BEQ .+4
001630 104410 HLT ;BIT 9 DIDN'T CLEAR
    
```



```

001632 005077 177154 CONT1: CLR      2BUSCSR      ;REINITIALIZE
001636 032777 001000 177146 BIT      81000,2BUSCSR ;WAIT FOR BIT 9 TO CLEAR
001644 001374 BNE     .-6
001646 012767 000010 020442 MOV     810,ICOUNT   ;DROP ITERATION COUNT SINCE RESETS TAKE SO LONG

;CLEAR INSTRUCTION SHOULD CLEAR LOW BYTE OF
;CSR (BITS 0 AND 1 DIRECTLY, BIT 7 INDIRECTLY)
001654 104406 TEST2: SCOPE
001656 012767 000100 020432 MOV     8100,ICOUNT ;RESTORE ITERATION COUNT
001664 005077 177122 CLR     2BUSCSR     ;INITIALIZE CSR
001670 012777 000003 177114 MOV     83,2BUSCSR  ;SET REQUEST BITS
001676 105777 177110 TSTB   2BUSCSR     ;WAIT FOR CONNECTED TO SET
001702 100375 BPL    .-4
001704 005077 177102 CLR     2BUSCSR     ;CLEAR CSR - CONNECTED SHOULD
001710 105777 177076 TSTB   2BUSCSR     ;CLEAR SINCE REQUEST BITS WERE CLEARED
001714 001401 BEQ    .+4
001716 104410 HLT
001720 032777 001000 177064 BIT      81000,2BUSCSR ;LOWER BYTE NOT ALL ZEROES
001726 001374 BNE     .-6

;SHOW THAT CLEAR INSTRUCTION WILL CLEAR UPPER BYTE (EXCEPT BITS 14 AND 15,
;WHICH CAN'T BE SET WITHOUT OPERATOR INTERVENTION)
001730 104406 TEST3: SCOPE
001732 012777 177400 177052 MOV     8177400,2BUSCSR ;DATO ALL ONES TO HIGH BYTE
001740 005077 177046 CLR     2BUSCSR     ;CLEAR CSR
001744 005777 177042 TST    2BUSCSR     ;CHECK
001750 001401 BEQ    .+4
001752 104410 HLT    ;UPPER BYTE NOT ALL ZEROES

;CLRB TO LOW BYTE SHOULD CLEAR LOWER BYTE OF CSR, AND NOT HIGH BYTE
001754 104406 TEST4: SCOPE
001756 052777 000340 177050 BIS     8340,2PSR   ;PREVENT INTERRUPTS
001764 012777 177403 177020 MOV     8177403,2BUSCSR ;SET BITS
001772 105777 177014 TSTB   2BUSCSR     ;WAIT FOR CONNECTED TO SET
001776 100375 BPL    .-4
002000 105077 177006 CLRB   2BUSCSR     ;CLEAR LOW BYTE
002004 032777 001000 177000 BIT      81000,2BUSCSR ;WAIT FOR SB INIT TO COMPLETE
002012 001374 BNE     .-6
002014 005767 177064 TST    DT11AF     ;IS THIS A DT11-A?
002020 001006 BNE     CNT4      ;YES, BRANCH
002022 022777 006400 176762 CMP     86400,2BUSCSR ;CHECK CSR, DT11-B
002030 001401 BEQ    .+4
002032 104410 HLT    ;CSR INCORRECT
002034 000405 BR     CNT4A
002036 022777 000400 176746 CNT4:  CMP     8400,2BUSCSR ;CHECK CSR, DT11-A
002044 001401 BEQ    .+4
002046 104410 HLT    ;CSR INCORRECT
002050 005077 176736 CNT4A: CLR     2BUSCSR
002054 032777 001000 176730 BIT      81000,2BUSCSR
002062 001374 BNE     .-6

;CLRB TO HIGH BYTE SHOULD CLEAR HIGH BYTE, LEAVE LOW BYTE SET
002064 104406 TEST5: SCOPE
002066 052777 000340 176740 BIS     8340,2PSR   ;SET BITS IN CSR
002074 012777 177403 176710 MOV     8177403,2BUSCSR ;CLEAR HIGH BYTE
002102 105077 176706 CLRB   2BUSCSR

```

# E02

DZDTR-B NACY11 27(732) 27-OCT-76 15:57 PAGE 18  
 DZDTR.B

```

002106 022777 020203 176676      CMP      @20203,@BUSCSR ;CHECK - SHOULDN'T CLEAR NON-NEUTRAL BIT (13)
002114 001401                      BEQ      .+4
002116 104410                      HLT
002120 005077 176666      CLR      @BUSCSR      ;CSR INCORRECT
002124 032777 001000 176660      BIT      @1000,@BUSCSR ;RELEASE BUS SWITCH
002132 001374                      BNE      .-6          ;WAIT FOR SB INIT TO COMPLETE
  
```

;SHOW THAT SETTING REQUEST BITS CAUSES SWITCH CONNECTED  
 ;TO SET IMMEDIATELY IF SB INIT IS NOT PRESENT  
 ;SHOW THAT THE SWITCH IS ACTUALLY CONNECTED BY ADDRESSING  
 ;A LOCATION ON THE SWITCHED BUS

```

002134 104406                      TEST6:  SCOPE
002136 012777 000003 176646      MOV      @3,@BUSCSR  ;SET REQUEST BITS
002144 105777 176642      TSTB    @BUSCSR     ;CHECK CSR
002150 100401                      BHI      .+4
002152 104410                      HLT      ;BIT 7 NOT SET
002154 012737 002212 000004      MOV      @RET6,@4   ;SETUP TIMEOUT RETURN IN CASE
002162 017737 176646 000006      MOV      @PSR,@6
002170 016777 176662 176656      MOV      @BITS,@VADR ;WRITE IN A LOCATION ON THE SWITCHED BUS
002176 026777 176654 176650      CMP      @BITS,@VADR ;CHECK RESULTS
002204 001401                      BEQ      .+4
002206 104410                      HLT      ;BITS INCORRECT IN LOCATION ON SWITCHED BUS
                                           ;IS EITHER A SWITCH DATA LINE OR ADDRESS LINE ERROR,
                                           ;OR INFORMATION SUPPLIED BY USER IS
                                           ;INCORRECT
  
```

```

002210 000402                      RET6:   BR      CONT6
002212 022626                      CMP      (SP)+,(SP)+ ;RESTORE STACK POINTER AFTER TIMEOUT TRAP
002214 104410                      HLT      ;SWITCH NOT ACTUALLY CONNECTED
                                           ;OR ADDRESS OF DEVICE GIVEN BY USER
                                           ;INCORRECT
                                           ;RESTORE TRAP CATCHER
  
```

```

002216 012737 000006 000004  CONT6:  MOV      @6,@4
002224 005037 000006      CLR      @6
002230 005077 176556      CLR      @BUSCSR
002234 032777 001000 176550      BIT      @1000,@BUSCSR ;RELEASE SWITCH
002242 001374                      BNE      .-6          ;WAIT FOR SB INIT TO COMPLETE
002244 005767 176626      TST     INITF
002250 100424                      BHI     TEST7        ;IF THIS PASS IS BEING RUN WITH INIT
                                           ;INHIBITED, SKIP THE NEXT TEST
  
```

;SHOW THAT BIT 9 OF THE CSR (RESET) SETS WHEN THE SWITCH IS RELEASED  
 ;SINCE INIT IS ON THE SWITCHED BUS FOR SEVERAL MICROSECONDS.

```

002252 104406                      TEST6A: SCOPE
002254 032777 000020 176552      BIT      @20,@PSR   ;TRACE BIT SET?
002262 001017                      BNE     TEST7      ;YES-SKIP TEST
002264 012777 000003 176520      MOV      @3,@BUSCSR ;REQUEST SWITCH
002272 016701 176514      MOV      @BUSCSR,R1 ;SETUP R1 FOR FAST REFERENCE TO CSR
002276 005077 176510      CLR      @BUSCSR   ;RELEASE SWITCH
002302 031127 001000      BIT      @R1,@1000 ;FAST CK OF BIT 9 BEING SET
002306 001001                      BNE      .+4
002310 104410                      HLT      ;BIT 9 (RESET) NOT SET IN CSR
                                           ;WHEN THE SWITCH WAS RELEASED
002312 032777 001000 176472      BIT      @1000,@BUSCSR ;WAIT FOR SB INIT TO COMPLETE
002320 001374                      BNE      .-6
  
```

;SHOW THAT SETTING BIT 0 CAUSES SWITCH CONNECTED (BIT 7) TO SET IMMEDIATELY  
 ;SHOW THAT THE SWITCH IS CONNECTED (ADDRESS A LOCATION ON THE SWITCHED BUS)

```

002322 104406                      TEST7:  SCOPE
  
```

```

002324 105277 176462      INCB      @BUSCSR      ;SET BIT 0 OF CSR
002330 105777 176456      TSTB      @BUSCSR      ;CHECK CONNECTED BIT
002334 100401      BMI      .+4
002336 104410      HLT
002340 012737 002356 000004      MOV      @RET7,@#4      ;BIT 7 NOT SET
002346 016777 176504 176500      MOV      RMBITS,@VDADR  ;SETUP TIMEOUT RETURN IN CASE
002354 000402      BR      CONT7          ;REFERENCE AN ADDRESS ON THE SWITCHED BUS
002356 022626      RET7:    CMP      (SP)+,(SP)+ ;RESTORE STACK POINTER AFTER TIMEOUT TRAP
002360 104410      HLT
                                ;SWITCH NOT ACTUALLY CONNECTED
                                ;OR ADDRESS OF A SWITCHED BUS LOCATION
                                ;GIVEN BY USER INCORRECT
                                ;RESTORE TRAP CATCHER

002362 012737 000006 000004      CONT7:   MOV      #6,@#4
002370 005037 000006      CLR      @#6
002374 005077 176412      CLR      @BUSCSR      ;RELEASE SWITCH
002400 032777 001000 176404      BIT      #1000,@BUSCSR ;WAIT FOR SB INIT TO COMPLETE
002406 001374      BNE      .-6

                                ;SHOW THAT SETTING BIT 1 CAUSES SWITCH CONNECTED TO SET IMMEDIATELY
                                ;SHOW THAT THE SWITCHED BUS IS NOT ACTUALLY CONNECTED SINCE IT IS IN POSITION 2(4)
002410 104406      TEST8:  SCOPE
002412 012777 000002 176372      MOV      #2,@BUSCSR      ;SET BIT 1
002420 105777 176366      TSTB      @BUSCSR      ;CHECK BIT 7 (CONNECTED BIT)
002424 100401      BMI      .+4
002426 104410      HLT
002430 012737 002450 000004      MOV      @RET8,@#4      ;BIT 7 NOT SET
002436 016777 176414 176410      MOV      RMBITS,@VDADR  ;SETUP TIMEOUT TRAP RETURN
                                ;REFERENCE AN ADDRESS ON THE SWITCHED BUS
                                ;SHOULD TRAP SINCE SWITCH IS IN
                                ;CONTROLLED BUT NOT CONNECTED POSITION
                                ;SWITCHED BUS IS CONNECTED TO
                                ;THE PROCESSOR BUS AFTER BEING
                                ;REQUESTED TO GO TO POSITION 2(4)
002444 104410      HLT
                                ;RESTORE STACK POINTER AFTER TIMEOUT TRAP
                                ;RESTORE TRAP CATCHER
002446 000401      RET8:   BR      CONT8
002450 022626      CONT8:  CMP      (SP)+,(SP)+
002452 012737 000006 000004      MOV      #6,@#4
002460 005037 000004      CLR      @#4
002464 005077 176322      CLR      @BUSCSR      ;RELEASE SWITCH
002470 032777 001000 176314      BIT      #1000,@BUSCSR ;WAIT FOR SB INIT TO COMPLETE
002476 001374      BNE      .-6

                                ;SHOW THAT SETTING BIT 7 (CONNECTED) TO ZERO DOESN'T CLEAR IT
002500 104406      TEST9:  SCOPE
002502 005277 176304      INC      @BUSCSR      ;REQUEST SWITCH
002506 042777 000200 176276      BIC      #200,@BUSCSR ;TRY TO CLEAR BIT 7
002514 105777 176272      TSTB      @BUSCSR
002520 100401      BMI      .+4
002522 104410      HLT
002524 005077 176262      CLR      @BUSCSR      ;BIT 7 WAS CLEARED VIA BIC - SHOULD BE READ ONLY
002530 032777 001000 176254      BIT      #1000,@BUSCSR ;RELEASE SWITCH
002536 001374      BNE      .-6
                                ;WAIT FOR SB INIT TO CLEAR

                                ;CLEARING BIT 1 WITH BIT 0 SET SHOULD LEAVE BIT 7 SET
002540 104406      TEST10: SCOPE
002542 052777 000003 176242      BIS      #3,@BUSCSR      ;REQUEST SWITCH
002550 042777 000002 176234      BIC      #2,@BUSCSR      ;CLEAR BIT 1 (SWITCH STILL REQUESTED SINCE BIT 0 IS SET)
002556 105777 176230      TSTB      @BUSCSR      ;CHECK CONNECTED BIT
002562 100401      BMI      .+4
002564 104410      HLT
                                ;BIT 7 NOT SET

```

DZDTA-B MACY11 27(732) 27-OCT-76 15:57 PAGE 20  
DZDTA.B

```
002566 005077 176220          CLR      2BUSCSR      ;RELEASE SWITCH
002572 032777 001000 176212      BIT      2000,2BUSCSR ;WAIT FOR SB INIT TO CLEAR
002600 001374          BNE      .-6
```

:CLEARING BIT 0 WITH BIT 1 SET SHOULD LEAVE BIT 7 SET

```
TEST11: SCOPE
002602 104406          ;SET BITS 0 AND 1
002604 052777 000003 176200      BIS      23,2BUSCSR
002612 042777 000001 176172      BIC      21,2BUSCSR ;CLEAR BIT 0 (SWITCH IS STILL REQUESTED
                                ;SINCE BIT 1 IS SET)
                                ;CHECK CONNECTED BIT
002620 105777 176166          TSTB     2BUSCSR
002624 100401          BMI      .+4
002626 104410          HLT
002630 005077 176156          CLR      2BUSCSR      ;BIT 7 NOT SET
002634 032777 001000 176150      BIT      21000,2BUSCSR ;RELEASE SWITCH
002642 001374          BNE      .-6          ;WAIT FOR SB INIT TO CLEAR
```

:BIT 13 SHOULD BE SET IF THE SWITCH IS IN POSITIONS 1(5) OR 2(4), AND CLEARED  
:IF IT'S IN POSITION 3  
:SHOW THAT THE SWITCHED BUS IS NOT CONNECTED  
:WHEN THE SWITCH IS IN POSITION 3

```
TEST12: SCOPE
002644 104406          INC      2BUSCSR      ;REQUEST POSITION 1
002646 005277 176140          BIT      22000,2BUSCSR ;CHECK BIT 13
002652 032777 020000 176132      BNE      .+4
002660 001001          HLT      ;POSITION 1, BIT 13 NOT SET
002662 104410          INC      2BUSCSR      ;REQUEST POSITION 2
002664 005277 176122          BIT      22000,2BUSCSR ;CHECK BIT 13
002670 032777 020000 176114      BNE      .+4
002676 001001          HLT      ;POSITION 2, BIT 13 NOT SET
002700 104410          INC      2BUSCSR      ;REQUEST POSITION 1, BITS 0 AND 1 SET
002702 005277 176104          BIT      22000,2BUSCSR ;CHECK BIT 13
002706 032777 020000 176076      BNE      .+4
002714 001001          HLT      ;POSITION 1, BIT 13 NOT SET
002716 104410          INC      2BUSCSR      ;REQUEST POSITION 3
002720 005277 176066          BIT      22000,2BUSCSR ;CHECK BIT 13
002724 032777 020000 176060      BNE      .+4
002732 001401          BEQ
002734 104410          HLT      ;POSITION 3, BIT 13 SET
002736 012737 002764 000004      MOV      2RET12,224 ;SETUP TIMEOUT TRAP RETURN
002744 017737 176064 000006      MOV      2PSR,226
002752 016777 176100 176074      MOV      2RMBITS,20VADR5 ;REFERENCE TO SWITCHED BUS ADDRESS SHOULD TRAP
002760 104410          HLT      ;SWITCHED BUS IS CONNECTED WHILE THE SWITCH IS IN
002762 000401          BR       .+4          ;NEUTRAL, OR THE ADDRESS ON THE SWITCHED BUS GIVEN BY
                                ;THE USER IS ACTUALLY ON THE PROCESSOR BUS
                                ;RESTORE STACK POINTER
                                ;RESTORE TRAP CATCHER
RET12: 002764 022626          CMP      (SP)+,(SP)+
002766 012737 000006 000004      MOV      26,224
002774 005037 000006          CLR      226
003000 032777 001000 176004      BIT      21000,2BUSCSR ;WAIT FOR SB INIT TO COMPLETE
003006 001374          BNE      .-6
```

:BIT 13 IS READ ONLY

```
TEST13: SCOPE
003010 104406          ;CHECK BIT 13, SW IN NEUTRAL
003012 032777 020000 175772      BIT      22000,2BUSCSR ;BRANCH IF CLEAR
003020 001401          BEQ      .+4
003022 104410          HLT      ;SWITCH SHOULD BE IN NEUTRAL, BUT BIT 13 IS SET
003024 052777 020000 175760      BIS      22000,2BUSCSR ;TRY TO SET BIT 13
```

```

003032 032777 020000 175752 BIT #20000,2BUSCSR ;CHECK BIT 13
003040 001401 BEQ .+4
003042 104410 HLT ;BIT 13 SET VIA BIS
003044 005277 175742 INC 2BUSCSR ;REQUEST SWITCH
003050 042777 020000 175734 BIC #20000,2BUSCSR ;TRY TO CLEAR BIT 13
003056 032777 020000 175726 BIT #20000,2BUSCSR ;CHECK BIT 13
003064 001001 BNE .+4
003066 104410 HLT ;BIT 13 CLEARED VIA BIC
003070 005077 175716 CLR 2BUSCSR ;RELEASE SWITCH
003074 032777 001000 175710 BIT #1000,2BUSCSR ;WAIT FOR SB INIT TO CLEAR
003102 001374 BNE .-6

```

;SHOW THAT AN INTERRUPT WILL OCCUR IF THE SWITCH IS REQUESTED BY SETTING BIT 0,  
;WITH BIT 8 SET AND THE PROCESSOR STATUS AT LEVEL 0

```

003104 104406 TEST14: SCOPE
003106 005077 175700 CLR 2BUSCSR ;INITIALIZE CSR
003112 052777 000340 175714 BIS #340,2PSR ;SET PSR TO LEVEL 7
003120 012777 003174 175670 MOV #TINT14,2BSIV1 ;SETUP INTERRUPT RETURN
003126 017777 175702 175664 MOV 2PSR,2BSST1
003134 042777 000340 175672 BIC #340,2PSR ;SET PSR TO 0
003142 012777 000401 175642 MOV #401,2BUSCSR ;INTERRUPT ENABLE AND REQUEST
003150 105777 175636 TSTB 2BUSCSR ;WAIT FOR CONNECTED TO SET
003154 100375 BPL .-4
003156 017777 175636 175650 MOV 2BSST1,2PSR ;RESTORE PROCESSOR TO LEVEL 7
003164 104410 HLT ;NO INTERRUPT OCCURRED
003166 005077 175620 CLR 2BUSCSR ;RELEASE SWITCH, CLEAR IE1
003172 000407 BR CONT14
003174 105777 175612 TINT14: TSTB 2BUSCSR ;CHECK CONNECTED BIT
003200 100401 BHI .+4
003202 104410 HLT ;CONNECTED BIT NOT SET AFTER CONNECTED INTERRUPT
003204 022626 CMP (SP)+,(SP)+ ;RESTORE STACK POINTER
003206 005077 175600 CLR 2BUSCSR ;DISABLE INTERRUPT
003212 016777 175602 175576 CONT14: MOV BSST1,2BSIV1 ;RESTORE TRAP CATCHER
003220 005077 175574 CLR 2BSST1
003224 032777 001000 175560 BIT #1000,2BUSCSR
003232 001374 BNE .-6

```

;SHOW THAT NO INTERRUPT WILL OCCUR WHEN THE SWITCH IS REQUESTED  
;AND INTERRUPT ENABLE 1 IS SET IF THE PROCESSOR IS AT LEVEL 7

```

003234 104406 TEST15: SCOPE
003236 052777 000340 175570 BIS #340,2PSR ;SET PROCESSOR TO LEVEL 7
003244 012777 003276 175544 MOV #TINT15,2BSIV1 ;SETUP INTERRUPT VECTOR RETURN
003252 017777 175556 175540 MOV 2PSR,2BSST1
003260 012777 000401 175524 MOV #401,2BUSCSR ;SET INTERRUPT ENABLE AND REQUEST SWITCH
003266 105777 175520 TSTB 2BUSCSR ;WAIT FOR SWITCH CONNECTED TO SET
003272 100375 BPL .-4
003274 000402 BR .+6
003276 104410 TINT15: HLT ;IF OK, SKIP ERROR HALT
003300 022626 CMP (SP)+,(SP)+ ;INTERRUPT OCCURRED WITH PROCESSOR AT LEVEL 7
003302 005077 175504 CLR 2BUSCSR ;RESTORE STACK POINTER
003306 016777 175506 175502 MOV BSST1,2BSIV1 ;CLEAR INTERRUPT; ENABLE AND RELEASE SWITCH
003314 005077 175500 CLR 2BSST1 ;CHANGE INTERRUPT RETURN ADDRESS
003320 032777 001000 175464 BIT #1000,2BUSCSR ;TO CAUSE A HALT ON A FALSE INTERRUPT
003326 001374 BNE .-6 ;WAIT FOR SB INIT TO CLEAR

```

;FIND THE LEVEL AT WHICH AN INTERRUPT OCCURS

```

:PRINT OUT A MESSAGE STATING THIS LEVEL IF IT IS OTHER THAN STANDARD
:(LEVEL 7). MAKE CERTAIN THAT IT ALWAYS OCCURS AT THIS LEVEL
:THE MESSAGE STATING THE LEVEL IS PRINTED ONLY ONCE, AND THE PROGRAM
:MUST BE STARTED OVER FOR IT TO BE PRINTED AGAIN
    
```

```

:TEST FOR AN INTERRUPT ON LEVEL 7
: SINCE THIS IS WHERE THE BUS SWITCH NORMALLY IS, DON'T PRINT OUT A
: MESSAGE IF IT IS FOUND HERE
    
```

```

003330 104406
003332 052777 000340 175474
003340 012777 003454 175450
003346 017777 175462 175444
003354 042777 00040 175452
003362 012777 000401 175422
003370 105777 175416
003374 100375
003376 052777 00040 175430
003404 005077 175402
003410 032777 001000 175374
003416 001374
003420 016777 175374 175370
003426 005077 175366
003432 005767 175404
003436 100042
003440 026727 175376 100007
003446 100401
003450 104410

003452 000434
003454 105777 175332
003460 100401
003462 104410
003464 005077 175322
003470 032777 001000 175314
003476 001374
003500 016777 175314 175310
003506 005077 175306
003512 022626
003514 005767 175322
003520 100404
003522 012767 100007 175312
003530 000405
003532 026727 175304 100007
003540 100001
003542 104410

TEST16: SCOPE
        BIS      #340,2PSR      ;SET PSR TO LEVEL 7
        MOV      @TINT16,2BSIV1 ;SETUP RETURN
        MOV      2PSR,2BSST1
        BIC      #40,2PSR      ;SET PSR TO LEVEL 6
        MOV      #401,2BUSCSR  ;INTERRUPT ENABLE AND REQUEST
CONT16: TSTB    2BUSCSR        ;CHECK CONNECTED
        BPL      CONT16        ;LOOP TILL SET
        BIS      #40,2PSR      ;RESTORE PSR TO LEVEL 7
        CLR      2BUSCSR        ;DISABLE INTERRUPTS AND RELEASE SWITCH
        BIT      #1000,2BUSCSR ;WAIT FOR SB INIT TO CLEAR
        BNE      -6
        MOV      BSST1,2BSIV1  ;CHANGE INTERRUPT RETURN ADDRESS
        CLR      2BSST1        ;TO CAUSE A HALT IF AN INTERRUPT OCCURS
        TST      INTFLG        ;CHECK FLAG INDICATING LEVEL HAS ALREADY BEEN RECORDED
        BPL      TEST17        ;IF NOT SET, GO TO NEXT TEST
        CMP      INTFLG,#100007 ;CHECK FOR RECORDED LEVEL
        BMI      .+4           ;BRANCH IF LESS THAN 7
        HLT
        ;NO INTERRUPT OCCURRED THIS TIME,
        ;BUT PREVIOUSLY OCCURRED AT THIS LEVEL (?)

TINT16: BR      TEST17
        TSTB    2BUSCSR        ;CHECK FOR CONNECTED BIT SET
        BMI      .+4
        HLT
        ;BIT 7 NOT SET AFTER CONNECTED INTERRUPT
        CLR      2BUSCSR        ;DISABLE INTERRUPTS AND RELEASE SWITCH
        BIT      #1000,2BUSCSR ;WAIT FOR SB INIT TO CLEAR
        BNE      -6
        MOV      BSST1,2BSIV1  ;CHANGE INTERRUPT RETURN ADDRESS
        CLR      2BSST1        ;TO CAUSE A HALT IF AN INTERRUPT OCCURS
        CMP      (SP)+,(SP)+    ;RESTORE STACK POINTER
        TST      INTFLG        ;CHECK FOR PREVIOUS INTERRUPT FLAG
        BMI      SET16         ;BRANCH IF FLAG SET
        MOV      #100007,INTFLG ;SET FLAG AND LEVEL
        BR      TEST17         ;GO TO NEXT TEST
SET16:  CMP      INTFLG,#100007 ;CHECK PREVIOUS LEVEL
        BPL      TEST17
        HLT
        ;INTERRUPT PREVIOUSLY OCCURRED ONLY AT
        ;A LOWER LEVEL
    
```

```

:TEST FOR AN INTERRUPT ON LEVEL 6
    
```

```

TEST17: SCOPE
        MOV      @TINT17,2BSIV1 ;SETUP RETURN ADDRESS
        BIS      #340,2PSR      ;SET PROCESSOR PRIORITY TO 7
        MOV      2PSR,2BSST1  ;SETUP RETURN STATUS
        BIC      #340,2PSR      ;SET PSR TO LEVEL 0
        BIS      #240,2PSR      ;SET PROCESSOR TO LEVEL 5 PRIORITY
    
```

```

003604 012777 000401 175200      MOV      #401, @BUSCSR      ;SET INTERRUPT ENABLE AND REQUEST
003612 105777 175174      TSTB    @BUSCSR           ;CHECK BIT 7 - WAIT FOR CONNECTED TO SET
003616 100375      BPL     .-4
003620 017777 175174 175206      MOV      @BSST1, @PSR      ;RESTORE PROCESSOR STATUS TO LEVEL 7
003626 005077 175160      CLR     @BUSCSR           ;DISABLE INTERRUPTS AND RELEASE SWITCH
003632 032777 001000 175152      BIT     #1000, @BUSCSR     ;WAIT FOR SB INIT TO CLEAR
003640 001374      BNE     .-6
003642 016777 175152 175146      MOV      @BSST1, @BSIV1    ;CHANGE INTERRUPT RETURN ADDRESS TO
003650 005077 175144      CLR     @BSST1            ;CAUSE A HALT IF AN INTERRUPT OCCURS
003654 005767 175162      TST     INTFLG            ;CHECK FLAG INDICATING THAT AN INTERRUPT LEVEL
                                ;HAS ALREADY BEEN RECORDED
                                ;IF NOT, GO TO NEXT TEST
003660 100047      BPL     TEST18            ;CHECK PREVIOUS LEVEL
003662 026727 175154 100006      CMP     INTFLG, #100006
003670 100401      BMI     .+4
003672 104410      HLT
                                ;NO INTERRUPT OCCURRED,
                                ;BUT PREVIOUSLY OCCURRED
                                ;AT THIS LEVEL OR HIGHER

003674 000441      BR      TEST18
003676 105777 175110      TINT17: TSTB    @BUSCSR           ;CHECK CONNECTED BIT
003702 100401      BMI     .+4
003704 104410      HLT
                                ;BIT 7 NOT SET AFTER INTERRUPT
003706 005077 175100      CLR     @BUSCSR           ;DISABLE FURTHER INTERRUPTS AND RELEASE SWITCH
003712 032777 001000 175072      BIT     #1000, @BUSCSR     ;WAIT FOR SB INIT TO CLEAR
003720 001374      BNE     .-6
003722 016777 175072 175066      MOV      @BSST1, @BSIV1    ;CHANGE INTERRUPT RETURN ADDRESS TO
003730 005077 175064      CLR     @BSST1            ;CAUSE A HALT IF AN INTERRUPT OCCURS
003734 022626      CMP     (SP)+, (SP)+       ;RESTORE STACK POINTER
003736 005767 175100      TST     INTFLG            ;CHECK FOR PREVIOUS FLAG
003742 100411      BMI     SET6              ;BRANCH IF FLAG SET
003744 012767 100006 175070      MOV      #100006, INTFLG   ;SET FLAG AND LEVEL
003752 104002      PMSG1
                                ;PRINT "THE INTERRUPT LEVEL WAS"
003754 012702 000006      MOV     #6, R2
003760 004767 016000      JSR    X7, PROCT          ;PRINT LEVEL NUMBER
003764 000405      BR      TEST18
003766 026727 175050 100006      SET6:  CMP     INTFLG, #100006 ;CHECK PREVIOUS LEVEL
003774 100001      BPL     TEST18
003776 104410      HLT
                                ;INTERRUPT PREVIOUSLY OCCURRED ONLY AT A
                                ;LOWER LEVEL

                                ;TEST FOR AN INTERRUPT ON LEVEL 5
                                TEST18: SCOPE
004000 104406      MOV     @TINT18, @BSIV1    ;SETUP RETURN ADDRESS
004002 012777 004132 175006      BIS     #340, @PSR         ;SET PROCESSOR PRIORITY TO 7
004010 052777 000340 175016      MOV     @PSR, @BSST1      ;SETUP RETURN STATUS
004016 017777 175012 174774      BIC     #340, @PSR         ;SET PSR TO LEVEL 0
004024 042777 000340 175002      BIS     #200, @PSR        ;SET PROCESSOR TO LEVEL 4 PRIORITY
004032 052777 000200 174774      MOV     #401, @BUSCSR     ;SET INTERRUPT ENABLE AND REQUEST
004040 012777 000401 174744      TSTB    @BUSCSR           ;CHECK BIT 7 - WAIT FOR CONNECTED TO SET
004046 105777 174740      BPL     .-4
004052 100375      BPL     .-4
004054 017777 174740 174752      MOV     @BSST1, @PSR      ;RESTORE PROCESSOR STATUS TO LEVEL 7
004062 005077 174724      CLR     @BUSCSR           ;DISABLE INTERRUPTS AND RELEASE SWITCH
004066 032777 001000 174716      BIT     #1000, @BUSCSR     ;WAIT FOR SB INIT TO CLEAR
004074 001374      BNE     .-6
004076 016777 174716 174712      MOV     @BSST1, @BSIV1    ;CHANGE INTERRUPT RETURN ADDRESS TO
004104 005077 174710      CLR     @BSST1            ;CAUSE A HALT IF AN INTERRUPT OCCURS
004110 005767 174726      TST     INTFLG            ;CHECK FLAG INDICATING THAT AN INTERRUPT LEVEL

```

```

004114 100047          BPL      TEST19      ;HAS ALREADY BEEN RECORDED
004116 026727 174720 100005  CMP      INTFLG,#100005 ;IF NOT, GO TO NEXT TEST
004124 100401          BMI      .+4         ;CHECK PREVIOUS LEVEL
004126 104410          HLT

;NO INTERRUPT OCCURRED,
;BUT PREVIOUSLY OCCURRED
;AT THIS LEVEL OR HIGHER

004130 000441          BR       TEST19
004132 105777 174654      TINT18: TSTB     2BUSCSR    ;CHECK CONNECTED BIT
004136 100401          BMI      .+4
004140 104410          HLT
004142 005077 174644      CLR     2BUSCSR    ;BIT 7 NOT SET AFTER INTERRUPT
004146 032777 001000 174636  BIT     2BUSCSR    ;DISABLE FURTHER INTERRUPTS AND RELEASE SWITCH
004154 001374          BNE     .-6        ;WAIT FOR SB INIT TO CLEAR
004156 016777 174636 174632  MOV     BSST1,2BSIV1 ;CHANGE INTERRUPT RETURN ADDRESS TO
004164 005077 174630      CLR     2BSST1     ;CAUSE A HALT IF AN INTERRUPT OCCURS
004170 022626          CMP     (SP)+,(SP)+ ;RESTORE STACK POINTER
004172 005767 174644      TST     INTFLG     ;CHECK FOR PREVIOUS FLAG
004176 100411          BMI     SET5      ;BRANCH IF FLAG SET
004200 012767 100005 174634  MOV     #100005,INTFLG ;SET FLAG AND LEVEL
004206 104002          PMSG1
004210 012702 000005      MOV     #5,R2      ;PRINT "THE INTERRUPT LEVEL WAS"
004214 004767 015544      JSR     %7,PROCT   ;PRINT LEVEL NUMBER
004220 000405          BR       TEST19
004222 026727 174614 100005  SET5:  CMP      INTFLG,#100005 ;CHECK PREVIOUS LEVEL
004230 100001          BPL     TEST19
004232 104410          HLT

;INTERUPT PREVIOUSLY OCCURRED ONLY AT A
;LOWER LEVEL

;TEST FOR AN INTERRUPT ON LEVEL 4
TEST19: SCOPE
004234 104406          MOV     #TINT19,2BSIV1 ;SETUP RETURN ADDRESS
004236 012777 004366 174552  BIS     #340,2PSR    ;SET PROCESSOR PRIORITY TO 7
004244 052777 000340 174562  MOV     2PSR,2BSST1 ;SETUP RETURN STATUS
004252 017777 174556 174540  BIC     #340,2PSR    ;SET PSR TO LEVEL 0
004260 042777 000340 174546  BIS     #140,2PSR    ;SET PROCESSOR TO LEVEL 3 PRIORITY
004266 052777 000140 174540  MOV     #401,2BUSCSR ;SET INTERRUPT ENABLE AND REQUEST
004274 012777 000401 174510  TSTB   2BUSCSR     ;CHECK BIT 7 - WAIT FOR CONNECTED TO SET
004302 105777 174504      BPL     .-4
004306 100375          MOV     2BSST1,2PSR ;RESTORE PROCESSOR STATUS TO LEVEL 7
004310 017777 174504 174516  CLR     2BUSCSR     ;DISABLE INTERRUPTS AND RELEASE SWITCH
004316 005077 174470      BIT     #1000,2BUSCSR ;WAIT FOR SB INIT TO CLEAR
004322 032777 001000 174462  BNE     .-6
004330 001374          MOV     BSST1,2BSIV1 ;CHANGE INTERRUPT RETURN ADDRESS TO
004332 016777 174462 174456  CLR     2BSST1     ;CAUSE A HALT IF AN INTERRUPT OCCURS
004340 005077 174454      TST     INTFLG     ;CHECK FLAG INDICATING THAT AN INTERRUPT LEVEL
004344 005767 174472      ;HAS ALREADY BEEN RECORDED
;IF NOT, GO TO NEXT TEST
;CHECK PREVIOUS LEVEL

004350 100047          BPL     TEST20
004352 026727 174464 100004  CMP     INTFLG,#100004 ;CHECK PREVIOUS LEVEL
004360 100401          BMI     .+4
004362 104410          HLT

;NO INTERRUPT OCCURRED,
;BUT PREVIOUSLY OCCURRED
;AT THIS LEVEL OR HIGHER

004364 000441          BR       TEST20
004366 105777 174420      TINT19: TSTB     2BUSCSR    ;CHECK CONNECTED BIT
004372 100401          BMI     .+4

```



```

004374 104410          HLT
004376 005077 174410  CLR          @BUSCSR          ;BIT 7 NOT SET AFTER INTERRUPT
004402 032777 001000 174402  BIT          #1000,@BUSCSR ;DISABLE FURTHER INTERRUPTS AND RELEASE SWITCH
004410 001374          BNE          -6              ;WAIT FOR SB INIT TO CLEAR
004412 016777 174402 174376  MOV          BSST1,@BSIV1    ;CHANGE INTERRUPT RETURN ADDRESS TO
004420 005077 174374          CLR          @BSST1         ;CAUSE A HALT IF AN INTERRUPT OCCURS
004424 022626          CMP          (SP)+,(SP)+     ;RESTORE STACK POINTER
004426 005767 174410          TST          INTFLG         ;CHECK FOR PREVIOUS FLAG
004432 100411          BMI          SET4          ;BRANCH IF FLAG SET
004434 012767 100004 174400  MOV          #100004,INTFLG ;SET FLAG AND LEVEL
004442 104002          PMSG1
004444 012702 000004          MOV          #4,R2          ;PRINT "THE INTERRUPT LEVEL WAS"
004450 004767 015310          JSR          %7,PROCT       ;PRINT LEVEL NUMBER
004454 000405          BR          TEST20
004456 026727 174360 100004 SET4:  CMP          INTFLG,#100004 ;CHECK PREVIOUS LEVEL
004464 100001          BPL          TEST20
004466 104410          HLT

;TEST FOR AN INTERRUPT ON LEVEL 3
TEST20: SCOPE
004470 104406          MOV          #TINT20,@BSIV1 ;SETUP RETURN ADDRESS
004472 012777 004622 174316  BIS          #340,@PSR      ;SET PROCESSOR PRIORITY TO 7
004500 052777 000340 174326  MOV          @PSR,@BSST1    ;SETUP RETURN STATUS
004506 017777 174322 174304  MOV          #340,@PSR      ;SET PSR TO LEVEL 0
004514 042777 000340 174312  BIC          #100,@PSR      ;SET PROCESSOR TO LEVEL 2 PRIORITY
004522 052777 000100 174304  BIS          #100,@PSR      ;SET INTERRUPT ENABLE AND REQUEST
004530 012777 000401 174254  MOV          #401,@BUSCSR   ;CHECK BIT 7 - WAIT FOR CONNECTED TO SET
004536 105777 174250          TSTB         @BUSCSR
004542 100375          BPL          -4
004544 017777 174250 174262  MOV          @BSST1,@PSR    ;RESTORE PROCESSOR STATUS TO LEVEL 7
004552 005077 174234          CLR          @BUSCSR        ;DISABLE INTERRUPTS AND RELEASE SWITCH
004556 032777 001000 174226  BIT          #1000,@BUSCSR  ;WAIT FOR SB INIT TO CLEAR
004564 001374          BNE          -6
004566 016777 174226 174222  MOV          BSST1,@BSIV1    ;CHANGE INTERRUPT RETURN ADDRESS TO
004574 005077 174220          CLR          @BSST1         ;CAUSE A HALT IF AN INTERRUPT OCCURS
004600 005767 174236          TST          INTFLG         ;CHECK FLAG INDICATING THAT AN INTERRUPT LEVEL
;HAS ALREADY BEEN RECORDED
004604 100047          BPL          TEST21         ;IF NOT, GO TO NEXT TEST
004606 026727 174230 100003  CMP          INTFLG,#100003 ;CHECK PREVIOUS LEVEL
004614 100401          BMI          .+4
004616 104410          HLT

;NO INTERRUPT OCCURRED,
;BUT PREVIOUSLY OCCURRED
;AT THIS LEVEL OR HIGHER

TINT20: BR          TEST21
004620 000441          TSTB         @BUSCSR        ;CHECK CONNECTED BIT
004622 105777 174164          BMI          .+4
004626 100401          HLT
004630 104410          CLR          @BUSCSR        ;BIT 7 NOT SET AFTER INTERRUPT
004632 005077 174154          CLR          @BUSCSR        ;DISABLE FURTHER INTERRUPTS AND RELEASE SWITCH
004636 032777 001000 174146  BIT          #1000,@BUSCSR  ;WAIT FOR SB INIT TO CLEAR
004644 001374          BNE          -6
004646 016777 174146 174142  MOV          BSST1,@BSIV1    ;CHANGE INTERRUPT RETURN ADDRESS TO
004654 005077 174140          CLR          @BSST1         ;CAUSE A HALT IF AN INTERRUPT OCCURS
004660 022626          CMP          (SP)+,(SP)+     ;RESTORE STACK POINTER
004662 005767 174154          TST          INTFLG         ;CHECK FOR PREVIOUS FLAG
004666 100411          BMI          SET3          ;BRANCH IF FLAG SET
004670 012767 100003 174144  MOV          #100003,INTFLG ;SET FLAG AND LEVEL

```



```

005160 104406          TEST22: SCOPE
005162 012777 005312 173626      MOV    #TINT22, @BSIV1 ;SETUP RETURN ADDRESS
005170 052777 000340 173636      BIS    #340, @PSR      ;SET PROCESSOR PRIORITY TO 7
005176 017777 173632 173614      MOV    @PSR, @BSST1   ;SETUP RETURN STATUS
005204 042777 000340 173622      BIC    #340, @PSR      ;SET PSR TO LEVEL 0
005212 052777 000000 173614      BIS    #00, @PSR      ;SET PROCESSOR TO LEVEL 0 PRIORITY
005220 012777 000401 173564      MOV    #401, @BUSCSR  ;SET INTERRUPT ENABLE AND REQUEST
005226 105777 173560          TSTB   @BUSCSR        ;CHECK BIT 7 - WAIT FOR CONNECTED TO SET
005232 100375          BPL    .-4
005234 017777 173560 173572      MOV    @BSST1, @PSR   ;RESTORE PROCESSOR STATUS TO LEVEL 7
005242 005077 173544          CLR    @BUSCSR        ;DISABLE INTERRUPTS AND RELEASE SWITCH
005246 032777 001000 173536      BIT    #1000, @BUSCSR ;WAIT FOR SB INIT TO CLEAR
005254 001374          BNE    .-6
005256 016777 173536 173532      MOV    @BSST1, @BSIV1 ;CHANGE INTERRUPT RETURN ADDRESS TO
005264 005077 173530          CLR    @BSST1        ;CAUSE A HALT IF AN INTERRUPT OCCURS
005270 005767 173546          TST    INTFLG        ;CHECK FLAG INDICATING THAT AN INTERRUPT LEVEL
                                ;HAS ALREADY BEEN RECORDED
                                ;IF NOT, GO TO NEXT TEST
005274 100047          BPL    TEST23        ;CHECK PREVIOUS LEVEL
005276 026727 173540 100001      CMP    INTFLG, #100001
005304 100401          BMI    .+4
005306 104410          HLT

                                ;NO INTERRUPT OCCURRED,
                                ;BUT PREVIOUSLY OCCURRED
                                ;AT THIS LEVEL OR HIGHER

005310 000441          BR     TEST23
005312 105777 173474          TINT22: TSTB   @BUSCSR ;CHECK CONNECTED BIT
005316 100401          BMI    .+4
005320 104410          HLT
005322 005077 173464          CLR    @BUSCSR        ;BIT 7 NOT SET AFTER INTERRUPT
                                ;DISABLE FURTHER INTERRUPTS AND RELEASE SWITCH
005326 032777 001000 173456      BIT    #1000, @BUSCSR ;WAIT FOR SB INIT TO CLEAR
005334 001374          BNE    .-6
005336 016777 173456 173452      MOV    @BSST1, @BSIV1 ;CHANGE INTERRUPT RETURN ADDRESS TO
005344 005077 173450          CLR    @BSST1        ;CAUSE A HALT IF AN INTERRUPT OCCURS
005350 022626          CMP    (SP)+, (SP)+   ;RESTORE STACK POINTER
005352 005767 173464          TST    INTFLG        ;CHECK FOR PREVIOUS FLAG
005356 100411          BMI    SET1          ;BRANCH IF FLAG SET
005360 012767 100001 173454      MOV    #100001, INTFLG ;SET FLAG AND LEVEL
005366 104002          PMSG1 ;PRINT "THE INTERRUPT LEVEL WAS"
005370 012702 000001          MOV    #1, R2
005374 004767 014364          JSR    %7, PROCT     ;PRINT LEVEL NUMBER
005400 000405          BR     TEST23
005402 026727 173434 100001      SET1:  CMP    INTFLG, #100001 ;CHECK PREVIOUS LEVEL
005410 100001          BPL    TEST23
005412 104410          HLT

                                ;INTERRUPT PREVIOUSLY OCCURRED ONLY AT A
                                ;LOWER LEVEL
  
```

;SHOW THAT AN INTERRUPT WILL OCCUR IF THE SWITCH IS REQUESTED VIA SETTING  
 ;BITS 0 AND 1, WITH INTERRUPT ENABLE SET, THE PROCESSOR AT LEVEL 0,  
 ;AND THE SWITCH PREVIOUSLY IN NEUTRAL

```

005414 104406          TEST23: SCOPE
005416 052777 000340 173410      BIS    #340, @PSR      ;SET PSR TO LEVEL 7
005424 012777 005474 173364      MOV    #TINT23, @BSIV1 ;SETUP INTERRUPT RETURN
005432 017777 173376 173360      MOV    @PSR, @BSST1
005440 042777 000340 173366      BIC    #340, @PSR      ;SET PSR TO LEVEL 0
005446 012777 000403 173336      MOV    #403, @BUSCSR  ;SET INTERRUPT ENABLE AND REQUEST
005454 105777 173332          TSTB   @BUSCSR        ;WAIT FOR SWITCH CONNECTED TO SET
005460 100375          BPL    .-4
  
```

```

005462 017777 173332 173344      MOV      @BSST1,@PSR      ;RESTORE PSR TO LEVEL 7
005470 104410                      HLT                      ;NO INTERRUPT OCCURRED WHEN SWITCH CONNECTED
005472 000405                      BR                       CONT23
005474 105777 173312      TINT23: TSTB      @BUSCSR      ;CHECK CONNECTED BIT AFTER CONNECTED INTERRUPT
005500 100401                      BMI      .+4
005502 104410                      HLT                      ;CONNECTED BIT NOT SET AFTER CONNECTED INTERRUPT
005504 022626                      CMP      (SP)+,(SP)+      ;RESTORE STACK POINTER
005506 005077 173300      CONT23: CLR      @BUSCSR      ;DISABLE INTERRUPT AND RELEASE SWITCH
005512 016777 173302 173276      MOV      BSST1,@BSIV1      ;CHANGE INTERRUPT RETURN ADDRESS TO
005520 005077 173274                      CLR      @BSST1          ;CAUSE A HALT ON A FALSE INTERRUPT
005524 032777 001000 173260      BIT      #1000,@BUSCSR      ;WAIT FOR SB INIT TO COMPLETE
005532 001374                      BNE      .-6

```

;SHOW THAT AN INTERRUPT WILL OCCUR IF THE SWITCH IS REQUESTED VIA SETTING  
 ;BIT 1, WITH INTERRUPT ENABLE SET, THE PROCESSOR AT LEVEL 0, AND THE SWITCH  
 ;PREVIOUSLY IN NEUTRAL

```

005534 104406                      TEST24: SCOPE
005536 052777 000340 173270      BIS      #340,@PSR      ;SET PROCESSOR PRIORITY TO LEVEL 7
005544 012777 005614 173244      MOV      @TINT24,@BSIV1 ;SETUP INTERRUPT RETURN
005552 017777 173256 173240      MOV      @PSR,@BSST1
005560 042777 000340 173246      BIC      #340,@PSR      ;SET PSR TO LEVEL 0
005566 012777 000402 173216      MOV      #402,@BUSCSR ;SET INTERRUPT ENABLE AND REQUEST
005574 105777 173212      TSTB      @BUSCSR      ;WAIT FOR SWITCH CONNECTED TO SET
005600 100375                      BPL      .-4
005602 017777 173212 173224      MOV      @BSST1,@PSR      ;RESTORE PROCESSOR PRIORITY TO LEVEL 7
005610 104410                      HLT                      ;NO INTERRUPT OCCURRED WHEN SWITCH CONNECTED
005612 000405                      BR                       CONT24
005614 105777 173172      TINT24: TSTB      @BUSCSR      ;CHECK CONNECTED BIT AFTER CONNECTED INTERRUPT
005620 100401                      BMI      .+4
005622 104410                      HLT                      ;CONNECTED BIT NOT SET AFTER INTERRUPT
005624 022626                      CMP      (SP)+,(SP)+      ;RESTORE STACK POINTER
005626 005077 173160      CONT24: CLR      @BUSCSR      ;DISABLE INTERRUPT AND RELEASE SWITCH
005632 016777 173162 173156      MOV      BSST1,@BSIV1      ;CHANGE INTERRUPT RETURN ADDRESS TO
005640 005077 173154                      CLR      @BSST1          ;CAUSE A HALT ON A FALSE INTERRUPT
005644 032777 001000 173140      BIT      #1000,@BUSCSR      ;WAIT FOR SB INIT TO COMPLETE
005652 001374                      BNE      .-6

```

;SHOW THAT AN INTERRUPT WILL NOT OCCUR IF IE1 IS SET AFTER SWITCH IS CONNECTED  
 ;SHOW THAT BIT 7 REMAINS SET ON GOING FROM POSITION 2 TO POSITION 1  
 ;SHOW THAT AN INTERRUPT WILL NOT OCCUR WHEN CHANGING FROM POSITION 2 TO  
 ;POSITION 1 IF INTERRUPT ENABLE 1 IS SET AND THE PROCESSOR IS AT LEVEL 0

```

005654 104406                      TEST25: SCOPE
005656 042777 000340 173150      BIC      #340,@PSR      ;ALLOW FALSE INTERRUPTS IF THEY OCCUR
005664 012777 000002 173120      MOV      #2,@BUSCSR      ;REQUEST POSITION 2
005672 105777 173114      TSTB      @BUSCSR      ;CONNECTED BIT SHOULD BE SET
005676 100401                      BMI      .+4
005700 104410                      HLT                      ;CONNECTED BIT NOT SET
005702 052777 000340 173124      BIS      #340,@PSR      ;SET PROCESSOR PRIORITY TO LEVEL 7
005710 012777 005752 173100      MOV      @TINT25,@BSIV1 ;SETUP INTERRUPT RETURN
005716 017777 173112 173074      MOV      @PSR,@BSST1
005724 042777 000340 173102      BIC      #340,@PSR      ;SET PROCESSOR PRIORITY TO LEVEL 0
005732 052777 000400 173052      BIS      #400,@BUSCSR ;ENABLE INTERRUPT
005740 000240                      NOP
005742 017777 173052 173064      MOV      @BSST1,@PSR      ;RESTORE PROCESSOR PRIORITY TO LEVEL 7
005750 000402                      BR                       CNT25
005752 104410      TIN25: HLT                      ;INTERRUPT OCCURRED WHEN IE1 WAS SET AFTER SWITCH

```

```

005754 022626          CMP      (SP)+,(SP)+      ;WAS CONNECTED
005756 012777 006022 173032 CNT25: MOV      @TINT25,@BSIV1    ;RESTORE STACK POINTER
005764 042777 000340 173042          BIC      @340,@PSR      ;CHANGE RETURN POINTER
005772 005277 173014          INC      @BUSCSR      ;SET PROCESSOR PRIORITY TO LEVEL 0
005776 000240          NOP                      ;REQUEST POSITION 1, IE1 ALREADY SET
006000 017777 173014 173026          MOV      @BSST1,@PSR    ;RESTORE PROCESSOR PRIORITY TO LEVEL 7
006006 022777 020603 172776          CMP      @20603,@BUSCSR ;CHECK CSR
006014 001401          BEQ      .+4
006016 104410          HLT
006020 000402          BR      CONT25          ;CSR INCORRECT
006022 104410          TINT25: HLT
006024 022626          CMP      (SP)+,(SP)+    ;INTERRUPT OCCURRED GOING FROM POSITION 2 TO POSITION 1
006026 005077 172760          CONT25: CLR      @BUSCSR    ;RESTORE STACK POINTER
006032 016777 172762 172756          MOV      @BSST1,@BSIV1  ;DISABLE INTERRUPT, RELEASE SWITCH
006040 005077 172754          CLR      @BSST1        ;CHANGE INTERRUPT RETURN ADDRESS TO
006044 032777 001000 172740          BIT      @1000,@BUSCSR  ;CAUSE A HALT ON A FALSE INTERRUPT
006052 001374          BNE      .-6           ;WAIT FOR SB INIT TO COMPLETE

```

;SHOW THAT THE SWITCH DOES NOT INTERRUPT ON 2 OR MORE LEVELS  
;SIMULTANEOUSLY

```

006054 104406          TEST26: SCOPE
006056 052777 000340 172750          BIS      @340,@PSR      ;SET PROCESSOR PRIORITY TO LEVEL 7
006064 012777 006134 172724          MOV      @TINT26,@BSIV1 ;SETUP RETURN
006072 017777 172736 172720          MOV      @PSR,@BSST1
006100 042777 000340 172726          BIC      @340,@PSR      ;SET PSR TO 0
006106 012777 000401 172676          MOV      @401,@BUSCSR   ;SET INTERRUPT ENABLE AND REQUEST
006114 105777 172672          TSTB    @BUSCSR        ;WAIT FOR CONNECTED TO SET
006120 100375          BPL      .-4
006122 017777 172672 172704          MOV      @BSST1,@PSR    ;RESTORE TO LEVEL 7
006130 104410          HLT
006132 000422          BR      CONT26          ;NO INTERRUPT OCCURRED WHEN SWITCH CONNECTED
006134 105777 172652          TINT26: TSTB    @BUSCSR   ;CHECK CONNECTED BIT
006140 100401          BMI      .+4
006142 104410          HLT
006144 022626          CMP      (SP)+,(SP)+    ;CONNECTED BIT NOT SET AFTER INTERRUPT
006146 012777 006174 172642          MOV      @TINT26,@BSIV1 ;RESTORE STACK POINTER
006154 042777 000340 172652          BIC      @340,@PSR      ;SETUP FOR DOUBLE INTERRUPT
006162 000240          NOP                      ;SET LEVEL TO 0
006164 017777 172630 172642          MOV      @BSST1,@PSR    ;RESTORE STATUS TO LEVEL 7
006172 000402          BR      CONT26
006176 104410          TIN26:  HLT
006178 022626          CMP      (SP)+,(SP)+    ;DOUBLE INTERRUPT OCCURRED
006200 005077 172606          CONT26: CLR      @BUSCSR   ;RESTORE STACK POINTER
006204 005077 172610          CLR      @BSST1        ;CLEAR INTERRUPT ENABLE AND RELEASE SWITCH
006210 016777 172604 172600          MOV      @BSST1,@BSIV1  ;CHANGE INTERRUPT RETURN ADDRESS
006216 032777 001000 172566          BIT      @1000,@BUSCSR  ;TO CAUSE A HALT ON A FALSE INTERRUPT
006224 001374          BNE      .-6           ;WAIT FOR SB INIT TO CLEAR

```

;SETTING INTERRUPT ENABLE 1 SHOULD NOT CAUSE AN INTERRUPT IF THE SWITCH IS  
;NOT REQUESTED

```

006226 104406          TEST27: SCOPE
006230 012767 000010 014060          MOV      @10,@ICOUNT    ;DROP ICOUNT DUE TO STALL LOOP
006236 052777 000340 172570          BIS      @340,@PSR      ;SET PROCESSOR PRIORITY TO LEVEL 7
006244 017777 172564 172546          MOV      @PSR,@BSST1    ;SETUP INTERRUPT RETURN
006252 012777 006316 172536          MOV      @TINT27,@BSIV1

```

```

006260 042777 000340 172546      BIC      #340, 2PSR      ;SET PROCESSOR PRIORITY TO LEVEL 0
006266 052777 000400 172516      BIS      #400, 2BUSCSR ;SET IE1
006274 005027 000000                CLR      #0          ;WAIT TO SEE IF AN INTERRUPT WILL OCCUR
                006276                WAIT27=-2
006300 005367 177772                DEC      WAIT27
006304 001375                BNE     -4
006306 017777 172506 172520      MOV     2BSST1, 2PSR ;RESTORE STATUS
006314 000402                BR      CONT27
006316 104410                TINT27: HLT
006320 022626                CMP     (SP)+, (SP)+ ;CONNECTED INTERRUPT OCCURRED WITHOUT SWITCH REQUESTED
006322 005077 172464                CONT27: CLR 2BUSCSR ;RESTORE STACK POINTER
006326 005077 172466                CLR 2BSST1 ;CLEAR IE1
006332 016777 172462 172456      MOV     BSST1, 2BSIV1 ;CHANGE INTERRUPT RETURN ADDRESS
                ;TO CAUSE A HALT ON A FALSE INTERRUPT

;SHOW THAT NO INTERRUPT OCCURS ON GOING FROM POSITION 1(5) TO POSITION 3
006340 104406                TEST28: SCOPE
006342 012767 000100 013746      MOV     #100, ICOUNT ;RESTORE ICOUNT
006350 005277 172436                INC     2BUSCSR      ;SET SWITCH TO POSITION 1
006354 052777 000340 172452      BIS     #340, 2PSR   ;SET PROCESSOR PRIORITY TO LEVEL 7
006362 017777 172446 172430      MOV     2PSR, 2BSST1 ;SETUP RETURN
006370 012777 006430 172420      MOV     #TINT28, 2BSIV1
006376 042777 000340 172430      BIC     #340, 2PSR   ;SET PROCESSOR PRIORITY TO LEVEL 0
006404 052777 000400 172400      BIS     #400, 2BUSCSR ;SET IE1
006412 105077 172374                CLRB   2BUSCSR      ;RELEASE SWITCH
006416 000240                NOP
006420 017777 172374 172406      MOV     2BSST1, 2PSR ;RESTORE STATUS
006426 000402                BR      CONT28
006430 104410                TINT28: HLT
006432 022626                CMP     (SP)+, (SP)+ ;INTERRUPT OCCURRED GOING FROM CONNECTED TO NEUTRAL
006434 005077 172352                CONT28: CLR 2BUSCSR ;RESTORE STACK POINTER
006440 005077 172354                CLR 2BSST1 ;CLEAR IE1
006444 016777 172350 172344      MOV     BSST1, 2BSIV1 ;CHANGE INTERRUPT RETURN ADDRESS TO
006452 032777 001000 172332      BIT     #1000, 2BUSCSR ;CAUSE A HALT ON A FALSE INTERRUPT
006460 001374                BNE     -6          ;WAIT FOR SB INIT TO CLEAR

;SHOW THAT BIT 7 STAYS SET GOING FROM POSITION 1 TO POSITION 2
;SHOW THAT NO INTERRUPT OCCURS GOING FROM POSITION 1 TO POSITION 2
006462 104406                TEST29: SCOPE
006464 005277 172322                INC     2BUSCSR      ;SET SWITCH TO POSITION 1
006470 052777 000340 172336      BIS     #340, 2PSR   ;SET PROCESSOR PRIORITY TO LEVEL 7
006476 017777 172332 172314      MOV     2PSR, 2BSST1 ;SETUP RETURN
006504 012777 006554 172304      MOV     #TINT29, 2BSIV1
006512 042777 000340 172314      BIC     #340, 2PSR   ;SET PROCESSOR PRIORITY TO LEVEL 0
006520 052777 000400 172264      BIS     #400, 2BUSCSR ;SET IE1
006526 005277 172260                INC     2BUSCSR      ;SET SWITCH TO POSITION 2
006532 000240                NOP
006534 017777 172260 172272      MOV     2BSST1, 2PSR ;RESTORE STATUS
006542 105777 172244                TSTB   2BUSCSR      ;CHECK CONNECTED BIT
006546 100401                BMT     +4
006550 104410                HLT
                ;CONNECTED (BIT 7) CLEARED GOING
                ;FROM POSITION 1 TO POSITION 2

006552 000402                BR      CONT29
006554 104410                TINT29: HLT
006556 022626                CMP     (SP)+, (SP)+ ;INTERRUPT OCCURRED
006560 005077 172226                CONT29: CLR 2BUSCSR ;RESTORE STACK POINTER
006564 005077 172230                CLR 2BSST1 ;CLEAR IE1 AND RELEASE SWITCH
                ;CHANGE INTERRUPT RETURN ADDRESS TO

```

DZDTA-B NACY11 27(732) 27-OCT-76 15:57 PAGE 31  
DZDTA.B

```

006570 016777 172224 172220      MOV      BSST1,BSIV1      ;CAUSE A HALT ON A FALSE INTERRUPT
006576 032777 001000 172206      BIT      @1000,@BUSCSR  ;WAIT FOR SB INIT TO CLEAR
006604 001374                      BNE      .-6

;SHOW THAT BIT 7 CLEARS GOING FROM POSITION 2(4) TO POSITION 3
;SHOW THAT NO INTERRUPT OCCURS GOING FROM POSITION 2(4) TO POSITION 3
TEST30: SCOPE
006606 104406                      MOV      @2,@BUSCSR     ;SET SWITCH TO POSITION 2(4)
006610 012777 000002 172174      BIS      @340,@PSR      ;SET PSR TO LEVEL 7
006616 052777 000340 172210      MOV      @PSR,@BSST1    ;SETUP INTERRUPT RETURN IN CASE
006624 017777 172204 172166      MOV      @TINT30,@BSIV1
006632 012777 006702 172156      BIC      @340,@PSR      ;SET PSR TO LEVEL 0
006640 042777 000340 172166      BIS      @400,@BUSCSR   ;SET IE1
006646 052777 000400 172136      CLRB    @BUSCSR        ;SET SWITCH TO POSITION 3
006654 105077 172132                      NOP
006660 000240                      MOV      @BSST1,@PSR    ;RESTORE STATUS
006662 017777 172132 172144      TSTB    @BUSCSR        ;CHECK BIT 7
006670 105777 172116                      BPL     .+4
006674 100001                      HLT
006676 104410                      BR      CONT30          ;CONNECTED (BIT 7) STILL SET AFTER RELEASING SWITCH
006700 000402                      TINT30: HLT
006702 104410                      ;INTERRUPT OCCURRED GOING FROM-
;POSITION 2(4) TO POSITION 3
;RESTORE STACK POINTER
006704 022626                      CMP      (SP)+,(SP)+
006706 005077 172100      CONT30: CLR      @BUSCSR     ;CLEAR IE1
006712 005077 172102      CLR      @BSST1        ;CHANGE INTERRUPT RETURN ADDRESS TO
006716 016777 172076 172072      MOV      BSST1,BSIV1    ;CAUSE A HALT ON A FALSE INTERRUPT
006724 032777 001000 172060      BIT      @1000,@BUSCSR  ;WAIT FOR SB INIT TO CLEAR
006732 001374                      BNE      .-6

;TESTS OF RESET ON THE SWITCHED BUS

;SETTING BIT 9 OF THE CSR SHOULD GENERATE AN INIT ON THE SWITCHED BUS
;WHEN THE SWITCH IS IN POSITION 1(5), AND SHOULD NOT CAUSE INIT ON THE PROCESSOR BUS
TEST31: SCOPE
006734 104406                      INC      @BUSCSR        ;REQUEST SWITCH
006736 005277 172050      MOV      AND@TS,@DVADR  ;SET BITS IN DEVICE REGISTER
006742 016777 172114 172104      MOV      @DVADR,R1      ;READ BACK DEVICE REGISTER TO CHECK
006750 017701 172100      MOV      @DVADR,R1
006754 046701 172104      BIC      AND@CN,R1      ;MASK OFF OTHER BITS
006760 026701 172076      CMP      AND@TS,R1      ;MAKE SURE THAT THOSE
006764 001402                      BEQ     .+6             ;BITS REALLY DID SET
006766 104410                      HLT
006770 000426                      BR      CNT31A         ;NOT ALL GIVEN BITS SET IN THE
;GIVEN ADDRESS (SEE DOCUMENT, SECTION 5.2.9)
006772 052777 000100 172032      BIS      @100,@TKR      ;SET TTY IE
007000 052777 001000 172004      BIS      @1000,@BUSCSR  ;SET SWITCHED BUS RESET (BIT 9)
007006 032777 001000 171776      BIT      @1000,@BUSCSR  ;WAIT FOR COMPLETION OF SB INIT
007014 001374                      BNE     .-6
007016 036777 172040 172030      BIT      AND@TS,@DVADR  ;SEE IF THE BITS WERE CLEARED
007024 001401                      BEQ     .+4             ;IN THE DEVICE REGISTER
007026 104410                      HLT
;BIT9 DIDN'T CAUSE SWITCHED BUS
;RESET IN POSITION 1(5)
007030 032777 000100 171774      BIT      @100,@TKR      ;CHECK IE OF TELETYPE READER
007036 001001                      BNE     .+4
007040 104410                      HLT
007042 005077 171764      CLR      @TKR           ;BRANCH IF STILL SET
007046 005077 171740      CNT31A: CLR      @BUSCSR  ;SETTING BIT 9 CAUSED INIT ON THE
;PROCESSOR BUS IN POSITION 1(5)
;RELEASE SWITCH

```

# F03

```

007052 032777 001000 171732      BIT      #1000,2BUSCSR ;WAIT FOR SB INIT TO COMPLETE
007060 001374      BNE      .-6

;SETTING BIT 9 OF THE CSR SHOULD GENERATE AN INIT ON THE SWITCHED BUS
;WHEN THE SWITCH IS IN POSITION 2(4), AND SHOULD NOT CAUSE AN INIT ON THE
;PROCESSOR BUS
TEST32: SCOPE
007062 104406      MOV      #3,2BUSCSR ;REQUEST SWITCH
007064 012777 000003 171720      MOV      ANDBTS,2DVADR5 ;SET BITS IN DEVICE REGISTER
007072 016777 171764 171754      MOV      2DVADR5,R1 ;CHECK BITS SET
007100 017701 171750      MOV      2DVADR5,R1 ;CHECK BITS SET
007104 046701 171754      BIC      ANDCON,R1 ;MASK OFF REST
007110 026701 171746      CMP      ANDBTS,R1
007114 001402      BEQ      .+6 ;BRANCH IF OK
007116 104410      HLT ;NOT ALL GIVEN BITS SET (SEE DOCUMENT, SECTION 5.2.9)
007120 000432      BR
007122 012777 000100 171702      MOV      #100,2TKR ;SET IE OF TTY READER
007130 005377 171656      DEC      2BUSCSR ;PUT SWITCH IN POSITION 2(4)
007134 052777 001000 171650      BIS      #1000,2BUSCSR ;SET SWITCHED BUS RESET
007142 032777 001000 171642      BIT      #1000,2BUSCSR ;WAIT FOR COMPLETION OF SB INIT
007150 001374      BNE      .-6
007152 005277 171634      INC      2BUSCSR ;SWITCH TO POSITION 1(5)
007156 036777 171700 171670      BIT      ANDBTS,2DVADR5 ;CHECK THE BITS IN THE DEVICE REGISTER
007164 001401      BEQ      .+4 ;BRANCH IF CLEARED
007166 104410      HLT ;SETTING BIT 9 DIDN'T CAUSE
;SWITCHED BUS RESET IN POSITION 2(4)
007170 032777 000100 171634      BIT      #100,2TKR ;CHECK IE IN TTY READER CSR
007176 001001      BNE      .+4 ;BRANCH IF OK
007200 104410      HLT ;SETTING BIT 9 OF THE CSR CAUSED
;INIT ON THE PROCESSOR BUS WITH
;THE SWITCH IN POSITION 2(4)
007202 005077 171624      CLR      2TKR ;REINITIALIZE TTY
007206 005077 171600      CLR      2BUSCSR ;REINITIALIZE SWITCH
007212 032777 001000 171572      BIT      #1000,2BUSCSR ;WAIT FOR SB INIT TO COMPLETE
007220 001374      BNE      .-6
007222 005767 171650      TST      INITF ;IF THIS PASS IS BEING RUN WITH THE
007226 100003      BPL      .+10 ;"INIT-INHIBIT INIT" SWITCH IN "INHIBIT INIT"
007230 104406      SCOPE ;POSITION, SKIP TO THE NEXT APPROPRIATE TEST
007232 000167 000156      JMP      CNT34

;IF THE BUS SWITCH IS USED WITH THE "INIT" - INHIBIT INIT" SWITCH IN THE "INIT"
;POSITION, AN INIT SHOULD BE GENERATED WHEN THE SWITCH IS SWITCHED
;INTO POSITION 3
TEST33: SCOPE
007236 104406      INC      2BUSCSR ;REQUEST SWITCH - POSITION 1(5)
007240 005277 171546      MOV      ANDBTS,2DVADR5 ;SET BITS IN DEVICE REGISTER
007244 016777 171612 171602      MOV      2DVADR5,R1 ;CHECK BITS SET
007252 017701 171576      MOV      2DVADR5,R1 ;CHECK BITS SET
007256 046701 171602      BIC      ANDCON,R1 ;MASK OFF REST
007262 026701 171574      CMP      ANDBTS,R1
007266 001402      BEQ      .+6 ;BRANCH IF OK
007270 104410      HLT ;NOT ALL GIVEN BITS SET
007272 000427      BR
007274 012777 000100 171530      MOV      #100,2TKR ;SET IE OF TTY READER
007302 005077 171504      CLR      2BUSCSR ;PUT SWITCH INTO POSITION 3
007306 032777 001000 171476      BIT      #1000,2BUSCSR ;WAIT FOR COMPLETION OF SB INIT
007314 001374      BNE      .-6
007316 005277 171470      INC      2BUSCSR ;REQUEST SWITCH

```



```

007322 036777 171534 171524      BIT      ANDBTS,ADVADR5  ;CHECK THE BITS SET IN THE DEVICE REGISTER
007330 001401      BEQ      .+4      ;BRANCH IF CLEARED
007332 104410      HLT
                                ;NO RESET ON GOING INTO POSITION 3 WITH
                                ;"INIT - INHIBIT INIT" SET IN THE "INIT" POSITION
007334 032777 000100 171470      BIT      @100,@TKR  ;CHECK TTY IE
007342 001001      BNE      .+4
007344 104410      HLT      ;INIT OCCURRED ON PROCESSOR BUS
007346 005077 171460      CLR      @TKR
007352 005077 171434      CLR      @BUSCSR  ;RELEASE SWITCH
007356 032777 001000 171426      BIT      @1000,@BUSCSR ;WAIT FOR SB INIT TO COMPLETE
007364 001374      BNE      .-6
007366 005767 171502      TST     SHORTF
007372 100002      BPL     .+6
007374 000167 006444      JNP     END
                                ;IF THE ENTIRE TEST HAS ALREADY BEEN RUN,
                                ;SKIP THE SECTION REQUIRING OPERATOR INTERVENTION

```

;WITH THE "INIT - INHIBIT INIT" SWITCH SET TO "INHIBIT INIT," SWITCHING INTO POSITION 3 SHOULD'N'T CAUSE AN INIT TO OCCUR ON THE SWITCHED BUS

```

007400 104406      TEST34: SCOPE
007402 012767 007414 012712      MOV     @CNT34,RETURN ;EXCLUDE MESSAGE PRINTOUT FROM SCOPE LOOP
007410 104030      PMSG12 ;PRINT MESSAGE: "PUT THE 'INIT - INHIBIT INIT' SWITCH
                                ;IN THE 'INHIBIT INIT' POSITION. THEN
                                ;PRESS 'CONTINUE' ON THIS PROCESSOR,"
007412 000000      HALT
007414 005277 171372      INC     @BUSCSR      ;PUT SWITCH IN POSITION 1 (5)
007420 016777 171436 171426      MOV     ANDBTS,ADVADR5 ;SET BITS IN THE REGISTER ON THE SWITCHED BUS
007426 017701 171422      MOV     ADVADR5,R1
007432 046701 171426      BIC     ANDCOM,R1    ;CHECK BITS SET
007436 026701 171420      CMP     ANDBTS,R1    ;MASK OFF REST
007442 001402      BEQ     .+6          ;BRANCH IF OK
007444 104410      HLT      ;NOT ALL GIVEN BITS SET IN ADDRESS ON SWITCHED BUS
007446 000421      BR     CNT34A
007450 005077 171336      CLR     @BUSCSR      ;PUT SWITCH INTO POSITION 3
007454 032777 001000 171330      BIT     @1000,@BUSCSR ;CHECK SWITCHED BUS RESET - SHOULD NOT OCCUR
007462 001401      BEQ     .+4
007464 104410      HLT
007466 005277 171320      INC     @BUSCSR      ;SB RESET (BIT 9) WAS SET
007472 017701 171356      MOV     ADVADR5,R1   ;PUT SWITCH BACK IN 1(5)
007476 046701 171362      BIC     ANDCOM,R1    ;GET REGISTER CONTENTS
007502 026701 171354      CMP     ANDBTS,R1    ;MASK OFF BITS NOT USED
007506 001401      BEQ     .+4          ;CHECK BITS IN DEVICE REGISTER
007510 104410      HLT      ;BRANCH IF OK
007512 005077 171274      CLR     @BUSCSR      ;INIT OCCURRED ON THE SWITCHED BUS
007516 032777 001000 171266      BIT     @1000,@BUSCSR ;RELEASE SWITCH
007524 001374      BNE     .-6          ;WAIT FOR SB INIT TO COMPLETE

```

;WITH THE "INIT - INHIBIT INIT" SWITCH SET TO "INHIBIT INIT," SETTING BIT 9 OF THE CSR DOESN'T CAUSE A SWITCHED BUS RESET IN POSITION 3, AND DOESN'T CAUSE AN INIT ON THE PROCESSOR BUS

```

007526 104406      TEST35: SCOPE
007530 012777 000001 171254      MOV     @1,@BUSCSR   ;PUT SWITCH IN POSITION 1(5)
007536 016777 171320 171310      MOV     ANDBTS,ADVADR5 ;SET BITS IN DEVICE REGISTER
007544 017701 171304      MOV     ADVADR5,R1   ;CHECK BITS SET
007550 046701 171310      BIC     ANDCOM,R1    ;MASK OFF REST
007554 026701 171302      CMP     ANDBTS,R1
007560 001402      BEQ     .+6          ;BRANCH IF OK
007562 104410      HLT      ;NOT ALL GIVEN BITS SET IN ADDRESS ON SWITCHED BUS
007564 000431      BR     CNT35

```

```

007566 012777 000100 171236      MOV      #100, @TKR      ;SET TTY READER IE
007574 005077 171212      CLR      @BUSCSR       ;PUT SWITCH IN POSITION 3
007600 052777 001000 171204      BIS      #1000, @BUSCSR ;SET BIT 9 IN CSR
007606 005277 171200      INC      @BUSCSR       ;PUT SWITCH IN POSITION 1(5)
007612 017701 171236      MOV      @DVAORS, R1   ;CHECK BITS IN THE DEVICE REGISTER
007616 046701 171242      BIC      ANDCOM, R1
007622 026701 171234      CMP      ANDBTS, R1
007626 001401      BEQ      .+4
007630 104410      HLT
007632 032777 000100 171172      BIT      #100, @TKR    ;BRANCH IF OK
007640 001001      BNE      .+4           ;AN INIT OCCURRED ON THE SWITCHED BUS
007642 104410      HLT                   ;CHECK TTY READER IE
007644 005077 171162      CLR      @TKR          ;BRANCH IF OK
007650 005077 171136      CLR      @BUSCSR       ;INIT OCCURRED ON PROCESSOR BUS
007654 005767 171224      TST      DT11AF        ;CLEAR TTY READER CSR
007660 001411      BEQ      TST35A        ;RELEASE SWITCH
007662 005067 012430      CLR      ICOUNT        ;IS THIS A DT11-A?
007666 005767 171204      TST      INITF         ;NO, CONTINUE
007672 100402      BMI      .+6           ;YES, DROP ITERATION COUNT
007674 104032      PMSG13                ;SKIP MESSAGE IF SECOND PASS (RUNNING WITH
                                ;INIT INHIBITED)
                                ;PRINT MESSAGE: "PUT THE 'INIT-INHIBIT
                                ;INIT' SWITCH IN THE 'INIT' POSITION. THEN
                                ;PRESS 'CONTINUE' ON THIS PROCESSOR."
007676 000000      HALT
007700 000167 001262      JNP      TEST42        ;SKIP TO TEST42

```

```

;WITH THE SWITCH CONTROLLED BY BUT NOT CONNECTED TO THE OTHER CPU,
;SETTING BIT 9 IN THIS SIDE'S CSR DOESN'T CAUSE A SWITCHED BUS RESET

```

```

007704 104406      TST35A: SCOPE
007706 005067 012404      CLR      ICOUNT
007712 005767 171160      TST      INITF
007716 100402      BMI      .+6
007720 104020      PMSG8
007722 000000      HALT
007724 005767 171146      TST      INITF
007730 100402      BMI      .+6
007732 104112      PMSG37
007734 000401      BR      .+4
007736 104070      PMSG28
007740 000000      HALT
007742 052777 001000 171042      BIS      #1000, @BUSCSR ;SET BIT 9
007750 032777 001000 171034      BIT      #1000, @BUSCSR ;CHECK BIT 9 - SHOULDN'T STAY SET
007756 001401      BEQ      .+4
007760 104410      HLT                   ;BIT 9 STAYED SET INDICATING SB INIT WAS ISSUED
007762 005077 171024      CLR      @BUSCSR
007766 104012      PMSG5
007770 000000      HALT
                                ;"CLEAR SR OF OTHER CPU, THEN PRESS 'CONT'"

```

```

;WITH THE SWITCH CONNECTED TO THE OTHER CPU,
;SETTING BIT 9 IN THIS SIDE'S CSR DOESN'T CAUSE A SWITCHED BUS RESET

```

```

007772 104406      TST35B: SCOPE
007774 104072      PMSG29
007776 000000      HALT
010000 052777 001000 171004      BIS      #1000, @BUSCSR ;REQUEST OPERATOR TO CLEAR SWITCH REGISTER
010006 032777 001000 170776      BIT      #1000, @BUSCSR ;OF OTHER CPU, THEN SET SWITCH 11
010014 001401      BEQ      .+4           ;SET BIT 9
010016 104410      HLT                   ;CHECK BIT 9- SHOULDN'T BE SET
                                ;BIT 9 STAYED SET INDICATING SB INIT WAS ISSUED

```

```

010020 104012          PMSG5          ;"CLEAR SR OF OTHER CPU, THEN PRESS 'CONT'"
010022 000000          HALT
010024 005767 171046  TST          INITF
010030 100402          BMI          TEST36
010032 104032          PMSG13
010034 000000          HALT

;CHECK BIT 13
;IT SHOULD BE SET WHENEVER THE SWITCH IS CONTROLLED BY THE OTHER PROCESSOR
010036 104406          TEST36: SCOPE
010040 104004          PMSG2
;PRINT MESSAGE: "CHANGE SWITCH REGISTER OF OTHER
;PROCESSOR - CLEAR IT AND THEN SET
;SWITCH ZERO TO A ONE, THEN PRESS
;'CONTINUE' ON THIS PROCESSOR."
010042 000000          HALT
010044 032777 020000 170740 BIT          @20000,@BUSCSR
010052 001001          BNE          .+4
010054 104410          HLT
;CHECK BIT 13
;BRANCH IF SET
;BIT 13 NOT SET WHEN OTHER PROCESSOR
;HAS SWITCH CONNECTED AND CONTROLLED
010056 104006          PMSG3
010060 000000          HALT
;PRINT MESSAGE: "CHANGE SWITCH REGISTER OF OTHER
;PROCESSOR - CLEAR IT AND THEN SET SWITCH 1 TO A ONE
;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."
010062 032777 020000 170722 BIT          @20000,@BUSCSR
010070 001001          BNE          .+4
010072 104410          HLT
;BIT 13 NOT SET WHEN OTHER PROCESSOR
;HAS SWITCH CONTROLLED BUT NOT CONNECTED

;CHECK OPERATION OF BIT 15
;IT SHOULD SET IF EITHER PROCESSOR TIMES OUT
;ANY DATA TO THE CSR SHOULD CLEAR IT
;SHOW THAT THE SWITCHED BUS ACTUALLY IS CONNECTED
;AFTER THE OTHER PROCESSOR TIMES OUT
010074 104406          TEST37: SCOPE
010076 104004          PMSG2
;PRINT MESSAGE: "CHANGE SWITCH REGISTER OF OTHER
;PROCESSOR-CLEAR IT AND THEN SET SWITCH ZERO
;TO A ONE, THEN PRESS 'CONTINUE' ON
;THIS PROCESSOR."
010100 000000          HALT
;THIS CAUSES THE OTHER SIDE TO
;REQUEST THE SWITCH
010102 005777 170704  TST          @BUSCSR
010106 100001          BPL          .+4
010110 104410          HLT
010112 012777 000003 170672 MOV          @3,@BUSCSR
;CHECK BIT 15
;BRANCH IF NOT SET
;TIMEOUT WAS SET AFTER CSR WAS CLEARED
;REQUEST SWITCH-OTHER PROCESSOR
;ISN'T REREQUESTING
;WAIT FOR CONNECT TO SET
010120 105777 170666  TSTB         @BUSCSR
010124 100375          BPL          .-4
010126 012737 010152 000004 MOV          @RET37,@#4
010134 017737 170674 000006 MOV          @PSR,@#6
010142 016777 170710 170704 MOV          @BITS,@VDADR
;MAKE SURE SWITCHED BUS IS ACTUALLY CONNECTED
;BY REFERENCING ADDRESS ON THE SWITCHED BUS
010150 000402          BR          .+6
010152 022626          CMP          (SP)+,(SP)+
010154 104410          HLT
;RESTORE STACK POINTER
;SWITCHED BUS NOT ACTUALLY CONNECTED
;RESTORE TRAP CATCHER
010156 012737 000006 000004 MOV          @6,@#4
010164 005037 000006          CLR          @#6
010170 005777 170616  TST          @BUSCSR
010174 100401          BMI          .+4
;CHECK TIMEOUT BIT

```

010176	104410			HLT			: TIMEOUT NOT SET AFTER OTHER SIDE LOST SWITCH BY TIMEOUT
010200	052777	100000	170604	BIS	#100000, 2BUSCSR		: DATO SHOULD CLEAR TIMEOUT BIT
010206	005777	170600		TST	2BUSCSR		
010212	100001			BPL	.+4		
010214	104410			HLT			: DATO DIDN'T CLEAR TIMEOUT BIT
010216	104004			PHSG2			: PRINT MESSAGE: "CHANGE SWITCH REGISTER OF OTHER
							: PROCESSOR-CLEAR IT AND THEN SET SWITCH 0
							: TO A ONE, THEN PRESS 'CONTINUE'
							: ON THIS PROCESSOR."
010220	000000			HALT			: WAIT FOR CONNECT TO CLEAR DUE TO
010222	105777	170564		TSTB	2BUSCSR		: REQUEST BY OTHER PROCESSOR
010226	100775			BNI	.-4		: CHECK TIMEOUT
010230	005777	170556		TST	2BUSCSR		
010234	100401			BNI	.+4		
010236	104410			HLT			: TIMEOUT DIDN'T SET WHEN THIS SIDE
							: LOST THE SWITCH BY TIMING OUT
010240	022777	120003	170544	CMP	#120003, 2BUSCSR		: TIMEOUT SHOULDN'T CLEAR BITS 0 AND 1
010246	001401			BEQ	.+4		
010250	104410			HLT			: STATUS REGISTER INCORRECT
010252	105077	170534		CLRB	2BUSCSR		: DATOB TO LOW BYTE SHOULD CLEAR BIT 15
010256	022777	020000	170526	CMP	#20000, 2BUSCSR		: TIMEOUT SHOULD NOW BE ZERO
010264	001401			BEQ	.+4		
010266	104410			HLT			: BIT 15 STAYED SET OR ANOTHER BIT IS
							: SET INCORRECTLY
010270	005277	170516		INC	2BUSCSR		: REQUEST SWITCH AGAIN
010274	105777	170512		TSTB	2BUSCSR		: WAIT FOR CONNECT TO SET
010300	100375			BPL	.-4		
010302	005777	170504		TST	2BUSCSR		: TIMEOUT SHOULD BE SET SINCE OTHER SIDE LOST SWITCH
010306	100401			BNI	.+4		
010310	104410			HLT			: TIMEOUT NOT SET
010312	112777	000200	170474	MOVB	#200, 2BUSCSR		: DATOB TO HIGH BYTE SHOULD CLEAR BIT 15
010320	022777	020201	170464	CMP	#20201, 2BUSCSR		: CHECK CSR
010326	001401			BEQ	.+4		
010330	104410			HLT			: SWITCH CSR INCORRECT
010332	005077	170454		CLR	2BUSCSR		: RELEASE SWITCH
010336	032777	001000	170446	BIT	#1000, 2BUSCSR		: WAIT FOR SB INIT TO COMPLETE
010344	001374			BNE	.-6		
							: CHECK THAT REREQUESTING THE SWITCH WILL PREVENT TIMEOUT
010346	104406			TST37A:	SCOPE		
010350	104122				PHSG41		: "WHEN THIS PRINTOUT IS FINISHED, PRESS 'CONTINUE.' THEN
							: CHANGE SR OF OTHER CPU:
							: TOGGLE SWITCH ZERO AT LEAST TEN TIMES.
							: THEN SET SWITCH ZERO IN THIS CPU'S SR."
010352	000000			HALT			
010354	012777	000001	170430	MOV	#1, 2BUSCSR		: REQUEST SWITCH
010362	012777	000001	170422	MOV	#1, 2BUSCSR		: REREQUEST SWITCH
010370	017701	170416		MOV	2BUSCSR, R1		: SAVE CONTENTS OF CSR IN R1
010374	020127	020201		CMP	R1, #20201		: CHECK SAVED CSR
010400	001401			BEQ	.+4		: BRANCH IF CORRECT
010402	104410			HLT			: CSR INCORRECT, SEE CONTENTS SAVED IN R1
010404	032777	000001	170424	BIT	#1, CSR		: CHECK SWITCH REGISTER SWITCH ONE
010412	001763			BEQ	LOP37A		: LOOP IF NOT SET
010414	005077	170372		CLR	2BUSCSR		
010420	032777	001000	170364	BIT	#1000, 2BUSCSR		: WAIT FOR SB INIT TO COMPLETE
010426	001374			BNE	.-6		
010430	104124			PHSG42			: "CLEAR SWITCH REGISTER OF OTHER CPU
							: THEN CLEAR SWITCH ZERO IN THIS CPU'S SR"

```

010432 032777 000001 170376      BIT      #1,SR      ;WAIT FOR SR TO CLEAR
010440 001374      BNE      -6
;CHECK OPERATION OF BITS 11 AND 12
;WHEN OTHER PROCESSOR SETS BIT 11, 12 SHOULD SET HERE
;WHEN OTHER PROCESSOR CLEARS BIT 11, 12 SHOULD CLEAR HERE
;12 SHOULD BE READ ONLY
;NO INTERRUPT SHOULD OCCUR WITH BIT 10 CLEAR
010442 104406      TEST38: SCOPE
010444 104010      PMSG4      ;REQUEST OPERATOR TO CLEAR SWITCH REGISTER OF OTHER CPU,
;THEN SET SWITCH TWO
;ALLOW FALSE INTERRUPTS
010446 042777 000340 170360      BIC      #340,SPSR
010454 000000      HALT
010456 022777 010000 170326      CMP      #10000,ABUSCSR ;BIT 12 SET?
010464 001401      BEQ      +4          ;YES
010466 104410      HLT              ;BIT 12 NOT SET AFTER BIT 11 WAS SET IN THE OTHER
;PROCESSOR'S CSR, OR ANOTHER BIT INCORRECT
;BIT 12 SHOULD BE READ ONLY
010470 005077 170316      CLR      ABUSCSR
010474 022777 010000 170310      CMP      #10000,ABUSCSR
010502 001401      BEQ      +4
010504 104410      HLT
010506 104012      PMSG5      ;BIT 12 CLEARED VIA A DATO OR ANOTHER BIT INCORRECT
;REQUEST OPERATOR TO CLEAR SWITCH REGISTER OF OTHER CPU
;THEN PRESS "CONTINUE" ON THIS PROCESSOR
010510 000000      HALT
010512 005777 170274      TST      ABUSCSR
010516 001401      BEQ      +4          ;BIT 12 SHOULD BE ZERO SINCE OTHER
;PROCESSOR CLEARED BIT 11
;BIT 12 STILL SET, OR ANOTHER BIT INCORRECT
010522 104406      ;IF BIT 10 (IE2) IS SET WHEN 11 ISN'T SET ON OTHER SIDE, NO INTERRUPT SHOULD OCCUR
010524 104012      ;IF BIT 10 IS SET WHEN 11 IS ALREADY SET ON OTHER SIDE, AN INTERRUPT SHOULD OCCUR
;IF BIT 10 IS SET AND THEN BIT 11 IS SET ON THE OTHER SIDE, AN INTERRUPT SHOULD OCCUR
TEST39: SCOPE
;PRINT MESSAGE: "CHANGE SWITCH REGISTER OF OTHER
;PROCESSOR-CLEAR IT. THEN PRESS
;'CONTINUE' ON THIS PROCESSOR."
;CLEARS SWITCH CSR OF OTHER SIDE
;SET PROCESSOR TO LEVEL 0 TO
;CATCH ANY FALSE INTERRUPT
010526 000000      HALT
010530 042777 000340 170276      BIC      #340,SPSR
010536 012777 010726 170256      MOV      #TINT39,ABSIV2
010544 017777 170264 170252      MOV      SPSR,ABSST2
010552 052777 000340 170244      BIS      #340,ABSST2
010560 012777 002000 170224      MOV      #2000,ABUSCSR ;SET IE2 ONLY
010566 000240      NOP          ;ALLOW MINDON IN CASE
010570 000240      NOP
010572 052777 000340 170234      BIS      #340,SPSR ;SET PROCESSOR BACK TO LEVEL 7
010600 012777 010634 170214      MOV      #TINT39A,ABSIV2 ;CHANGE INTERRUPT RETURN FOR NEXT CHECK
010606 104010      PMSG4      ;PRINT MESSAGE: "CHANGE SWITCH REGISTER OF OTHER
;PROCESSOR-CLEAR IT AND THEN SET SWITCH 2 TO A ONE.
;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."
;SETS BIT 11 OF OTHER CSR
;SET PROCESSOR TO LEVEL 0
010610 000000      HALT
010612 042777 000340 170214      BIC      #340,SPSR
010620 000240      NOP
010622 052777 000340 170204      BIS      #340,SPSR ;SET PROCESSOR BACK TO LEVEL 7
010630 104410      HLT          ;NO INTERRUPT OCCURRED WHEN BIT
;11 WAS SET ON OTHER PROCESSOR AFTER
;BIT 10 WAS SET ON THIS SIDE
010632 000401      BR      +4
010634 022626      TNT39A: CMP      (SP)+,(SP)+ ;RESTORE STACK
010636 005077 170150      CLR      ABUSCSR ;CLEAR INTERRUPT ENABLE

```

```

010642 032777 010000 170142      BIT      #10000,2BUSCSR      ;CHECK BIT 12
010650 001002                      BNE      .+6           ;BRANCH IF STILL SET
010652 104410                      HLT                               ;BIT 12 NO LONGER SET AFTER CLEARING IE2
010654 000426                      BR       CNT39A
010656 012777 010722 170136      MOV      #TNT39B,2BSIV2 ;SETUP RETURN
010664 017777 170144 170132      MOV      2PSR,2BSST2
010672 052777 002000 170112      BIS      #2000,2BUSCSR ;SET BIT 10 (IE2)
010700 042777 000340 170126      BIC      #340,2PSR     ;SET PROCESSOR TO LEVEL 0
010706 000240                      NOP                               ;SWITCH SHOULD INTERRUPT SINCE
010710 052777 000340 170116      BIS      #340,2PSR     ;BIT 11 ON OTHER SIDE STILL SET
010716 104410                      HLT                               ;RESTORE PROCESSOR PRIORITY TO LEVEL 7
010720 000404                      BR       CNT39A          ;NO INTERRUPT OCCURRED WHEN IE2 WAS SET
010722 022626      TNT39B: CMP      (SP)+,(SP)+ ;WITH BIT 12 ALREADY SET
010724 000402      BR       CNT39A          ;RESTORE STACK POINTER
010726 104410      TINT39: HLT                               ;SETTING BIT 10 CAUSED INTERRUPT WITHOUT
010730 022626                      CMP      (SP)+,(SP)+ ;BIT 11 SET ON OTHER SIDE
010732 005077 170066      CNT39A: CLR      2BSST2 ;RESTORE STACK POINTER
010736 016777 170062 170056      MOV      BSST2,2BSIV2 ;CHANGE INTERRUPT RETURN TO CAUSE
010744 005077 170042      CLR      2BUSCSR      ;A HALT ON A FALSE INTERRUPT
010750 104406                      ;SHOW THAT REREQUESTING THE BUS SWITCH WHEN THE OTHER PROCESSOR HAS NOT
010752 104004      TEST40: SCOPE ;REQUESTED IT WILL NOT CAUSE THE TIMER TO START
010754 000000                      PMSG2
010756 032777 020000 170026      HALT
010764 001774                      BIT      #20000,2BUSCSR ;HAVE OPERATOR CAUSE THE OTHER PROCESSOR
010766 012777 000001 170016      BEQ      .-6           ;TO CLEAR THE BUS SWITCH CSR AND THEN
010774 005067 170046      MOV      #1,2BUSCSR   ;REQUEST THE SWITCH
011000 005067 170044      CLR      CNT40        ;INITIALIZE COUNTER
011004 062767 000001 170034      CLR      CNT40A
011012 005567 170032      LOOP40: ADD     #1,CNT40
011016 005777 167770      ADC      CNT40A
011022 100370      TST     2BUSCSR      ;TIMEOUT SET?
011024 006367 170016      BPL     LOOP40       ;NO-CONTINUE COUNTING
011030 006167 170014      ASL     CNT40        ;YES, INCREASE COUNT TO ALLOW MARGIN
011034 032777 001000 167750      ROL     CNT40A
011042 001374      BIT     #1000,2BUSCSR ;WAIT FOR SB INIT TO CLEAR
011044 105777 167742      BNE     .-6
011050 100401      TSTB   2BUSCSR      ;CONNECTED SET?
011052 104410      BMI     .+4         ;YES-OK
011054 012777 000001 167730      HLT
011062 005777 167724      MOV     #1,2BUSCSR   ;NO-TIMEOUT SET BUT CONNECTED DIDN'T
011066 100001      TST     2BUSCSR      ;REREQUEST SWITCH, CLEAR TIMEOUT
011070 104410      BPL     .+4         ;DID TIMEOUT CLEAR?
011072 005467 167750      HLT     ;YES-OK
011076 005267 167746      HLT     ;NO-DATO DIDN'T CLEAR TIMEOUT
011102 062767 000001 167736      NEG     CNT40        ;COUNT DOWN
011110 005667 167734      LOP40A: ADD    #1,CNT40 ;LOOP SET UP TO TAKE SAME LENGTH
011114 005737 001050      SBC    CNT40A       ;OF TIME AS PREVIOUS ONE
011120 001370      TST    2CNT40A      ;TOTAL TIMING TWICE THAT
011122 022777 020201 167662      BNE    LOP40A       ;WHICH WAS MEASURED FOR TIMEOUT
011122 022777 020201 167662      CMP    #20201,2BUSCSR ;CHECK CSR NOW

```

```

011130 001401          BEQ      .+4
011132 104410          HLT
011134 005077 167652   CLR      @BUSCSR          ;TIMEOUT OCCURRED OR ANOTHER BIT IN CSR INCORRECT
011140 032777 001000 167644 BIT      #1000,@BUSCSR   ;INITIALIZE SWITCH
011146 001374          BNE      .-6              ;WAIT FOR SB INIT TO COMPLETE
011150 005767 167726   TST      NOPF            ;IS FLAG SET TO INHIBIT POWER FAIL
011154 100004          BPL      .+12            ;TESTING?-IF NOT, CONTINUE
011156 104012          PMSG5
011160 000000          HALT
011162 000167 004442   JMP      DONE            ;IF SET, REQUEST OPERATOR TO CLEAR SR
                                ;OF OTHER CPU
                                ;SKIP POWER FAIL TESTS

```

```

;TEST POWER FAIL ON THE PROCESSOR BUS (TEST42 THRU TEST49)
;RUNNING TEST ROUTINES ON BOTH PROCESSORS, POWER DOWN THIS PROCESSOR
;DO THIS TEST ONCE FOR EACH SWITCH POSITION
;NOTE THAT THESE TESTS ALSO SHOW THAT
;THE A AND B PROCESSOR INITS ARE CORRECT

```

```

;SHOW THAT THE SWITCH GOES TO NEUTRAL IF IT WAS CONNECTED TO THIS PROCESSOR
;WHEN THE POWER FAIL OCCURRED, AND THAT BIT 14 DOESN'T SET

```

```

011166 104406          TEST42: SCOPE
011170 005767 167706   TST      NOPF            ;IF DT11-A, THE PREVIOUS CHECK OF POWER
                                ;FAIL TESTING BEING INHIBITED WILL BE SKIPPED
                                ;SO CHECK IT HERE
                                ;BRANCH IF NOT INHIBITED
011174 100002          BPL      .+6              ;SKIP TESTS IF INHIBITED
011176 000167 004426   JMP      DONE            ;IF DT11-A, SKIP MESSAGE
011202 005767 167676   TST      DT11AF
011206 001002          BNE      .+6
011210 104034          PMSG14          ;REQUEST OPERATOR TO CLEAR SWITCH REGISTER OF OTHER
                                ;PROCESSOR, THEN SET SWITCH 3,
                                ;AND PRESS CONTINUE ON THIS PROCESSOR
011212 000000          HALT
011214 012777 000001 167570 MOV      #1,@BUSCSR      ;REQUEST SWITCH
011222 105777 167564   TSTB    @BUSCSR        ;WAIT FOR SWITCH TO CONNECT
011226 100375          BPL      .-4
011230 012737 011250 000024 MOV      @RET42,@#24    ;SETUP POWER FAIL RETURN
011236 017737 167572 000026 MOV      @PSR,@#26
011244 104052          PMSG21          ;PRINT MESSAGE: "POWER DOWN THIS PROCESSOR AND
                                ;THEN POWER THIS PROCESSOR BACK UP"
                                ;WAIT FOR POWER FAIL TRAP
011246 000777          BR
011250 012737 011300 000024 RETA42: MOV    @RET42,@#24    ;SETUP POWER UP RETURN
011256 017767 167530 167606 MOV      @BUSCSR,PFSAV  ;SAVE CONTENTS OF CSR FOR CHECKING
011264 010667 167600   MOV      SP,SPSAV      ;SAVE STACK POINTER
011270 000000          HALT
011272 016706 167572   MOV      SPSAV,SP      ;HALT ON POWER DOWN
011276 104410          HLT
011300 016706 167564   RETB42: MOV    SPSAV,SP  ;NO POWER UP RESTART OCCURRED
011304 022626          CMP      (SP)+,(SP)+   ;RESTORE STACK POINTER ON POWER UP
011306 012737 000026 000024 MOV      #26,@#24      ;RESTORE TRAP CATCHER IN POWER
011314 005037 000026   CLR      @#26          ;FAIL VECTOR ADDRESS
011320 005027 000000   CLR      #0            ;STALL SO THAT TTY
011324 005367 177772   DEC      .-2           ;OUTPUT WON'T BE
011330 001375          BNE      .-4           ;GARBLED
011332 022767 020201 167532 CMP      @20201,PFSAV  ;CHECK SAVED CONTENTS OF CSR AT
011340 001401          BEQ      .+4           ;TIME OF POWER FAIL-SHOULD NOT HAVE
                                ;CHANGED AT THAT POINT
                                ;CONTENTS OF CSR AT TIME OF
                                ;POWER FAIL INCORRECT - SAVED IN
011342 104410          HLT

```





```

011606 012737 011634 000004      MOV      @RET43, @#4      ;SETUP TRAP RETURN
011614 017737 167214 000006      MOV      @PSR, @#6
011622 016777 167230 167224      MOV      @RMBITS, @OVADR5 ;REFERENCE ADDRESS ON SWITCHED BUS - SHOULD TRAP
011630 104410      HLT
011632 000401      BR
011634 022626      RET43:  CMP      (SP)+, (SP)+ ;RESTORE STACK POINTER
011636 012737 000006 000004  CONT43: MOV      @#6, @#4      ;RESTORE TRAP CATCHER
011644 005037 000006      CLR      @#6
011650 005077 167136      CLR      @BUSCSR        ;MAKE SURE SWITCH IS RELEASED
011654 032777 001000 167130      BIT      @1000, @BUSCSR ;WAIT FOR SB INIT TO COMPLETE
011662 001374      BNE      .-6

;CHECK PROCESSOR POWER FAIL WITH SWITCH IN NEUTRAL
011664 104406      TEST44: SCOPE
011666 005767 167212      TST      DT11AF        ;IF DT11-A, SKIP MESSAGE
011672 001002      BNE      .+6
011674 104034      PMSG14      ;REQUEST OPERATOR TO CLEAR SWITCH REGISTER OF OTHER
;PROCESSOR, SET SWITCH 3, AND
011676 000000      HALT
011700 005077 167106      CLR      @BUSCSR        ;PRESS CONTINUE ON THIS PROCESSOR
011704 012737 011724 000024      MOV      @RET44, @#24 ;PUT SWITCH IN NEUTRAL
011712 017737 167116 000026      MOV      @PSR, @#26 ;SETUP POWER FAIL RETURN
011720 104052      PMSG21      ;PRINT MESSAGE: "POWER DOWN THIS PROCESSOR AND
;THEN POWER THIS PROCESSOR BACK UP"
011722 000777      BR
011724 012737 011754 000024  RET44:  MOV      @RET44, @#24 ;WAIT FOR POWER FAIL TRAP
011732 017767 167054 167132      MOV      @BUSCSR, PFSAV ;SETUP POWER UP RETURN
011740 010667 167124      MOV      SP, SPSAV      ;SAVE CONTENTS OF CSR FOR CHECKING
011744 000000      HALT
011746 016706 167116      MOV      SPSAV, SP      ;SAVE STACK POINTER
011752 104410      HLT
011754 016706 167110      RET44:  MOV      SPSAV, SP ;HALT ON POWER DOWN
011760 022626      CMP      (SP)+, (SP)+ ;NO POWER UP RESTART OCCURRED
011762 012737 000026 000024  RET44:  MOV      @#26, @#24 ;RESTORE STACK POINTER ON POWER UP
011770 005037 000026      CLR      @#26
011774 005027 000000      CLR      @#0
012000 005367 177772      DEC      .-2
012004 001375      BNE      .-4
012006 005767 167060      TST      PFSAV
012012 001401      BEQ      .+4
;RESTORE TRAP CATCHER IN POWER
;FAIL VECTOR ADDRESS
;STALL SO THAT TTY
;OUTPUT WON'T BE
;GARBLED
;CHECK SAVED CONTENTS OF CSR AT
;TIME OF POWER FAIL - SHOULD HAVE BEEN
;CLEARED SINCE CSR WAS PREVIOUSLY CLEARED
;CONTENTS OF CSR AT TIME OF POWER
;DOWN INCORRECT (SAVED IN PFSAV)
;CHECK CSR CONTENTS AFTER POWER UP
012014 104410      HLT
012016 005777 166770      TST      @BUSCSR
012022 001401      BEQ      .+4
;CSR INCORRECT AFTER POWER DOWN AND UP
012024 104410      HLT
012026 005767 167052      TST      DT11AF        ;IF DT11-A, SKIP TO TEST50
012032 001402      BEQ      .+6
012034 000167 001002      JMP      TEST50

;CHECK PROCESSOR POWER FAIL WITH SWITCH CONTROLLED BY BUT NOT CONNECTED TO
;THE OTHER PROCESSOR
012040 104406      TEST45: SCOPE
012042 104036      PMSG15      ;REQUEST OPERATOR TO CLEAR SWITCH REGISTER OF OTHER
;PROCESSOR, SET SWITCH FOUR, AND
012044 000000      HALT      ;PRESS CONTINUE ON THIS PROCESSOR

```



```

012324 104410          HLT          ;CSR INCORRECT AT TIME OF POWER DOWN
                                           ;(SAVED IN PFSAV)
012326 022777 020000 166456  CMP      @20000,@BUSCSR ;CHECK CSR CONTENTS AFTER POWER UP
012334 001401          BEQ      .+4
012336 104410          HLT          ;CSR INCORRECT AFTER POWER UP

;TEST THAT WHEN POWER DOWN OCCURS ON THIS PROCESSOR, THE OTHER PROCESSOR
;CAN GET THE SWITCH

;CHECK WITH SWITCH IN THE CONNECTED AND CONTROLLED POSITION
TEST47: SCOPE
        MSG17
012340 104406          HLT          ;REQUEST OPERATOR TO CLEAR SWITCH REGISTER OF OTHER
012342 104042          HLT          ;PROCESSOR, SET SWITCH 6, AND THEN
                                           ;PRESS CONTINUE ON THIS PROCESSOR
012344 000000          HLT          ;SETUP POWER DOWN RETURN
012346 012737 012400 000024  RET47:  MOV      @RET47,@24
012354 017737 166454 000026  MOV      @PSR,@26
012362 104074          MSG30
012364 104052          MSG21
012366 000000          HLT

012370 012777 000001 166414  MOV      @1,@BUSCSR
012376 000774          BR      .-6
                                           ;REQUEST SWITCH
                                           ;REREQUEST SWITCH UNTIL POWER DOWN OCCURS
                                           ;TO AVOID TIMEOUT
012400 012737 012430 000024  RET47:  MOV      @RET47,@24
012406 017767 166400 166456  MOV      @BUSCSR,PFSAV
012414 010667 166450          MOV      SP,SPSAV
012420 000000          HLT
012422 016706 166442          MOV      SPSAV,SP
012426 104410          HLT
012430 016706 166434  RET47:  MOV      SPSAV,SP
012434 022626          CMP      (SP)+,(SP)+
012436 012737 000026 000024  MOV      @26,@24
012444 005037 000026          CLR      @26
012450 005027 000000          CLR      @0
012454 005367 177772          DEC      .NT
012460 001375          BNE      .NT
012462 022767 020201 166402  CMP      @20201,PFSAV
012470 001401          BEQ      .+4
012472 104410          HLT
                                           ;NO POWER UP RESTART OCCURRED
                                           ;RESTORE STACK POINTER ON POWER UP
012474 022777 020000 166310  CMP      @20000,@BUSCSR
012502 001401          BEQ      .+4
012504 104410          HLT
                                           ;RESTORE TRAP CATCHER IN POWER
                                           ;FAIL VECTOR ADDRESS
                                           ;STALL SO THAT TTY
                                           ;OUTPUT WON'T BE
                                           ;GARBLED
                                           ;CHECK SAVED CONTENTS OF CSR
                                           ;AT TIME OF POWER DOWN
                                           ;CSR INCORRECT AT TIME OF POWER DOWN TRAP
                                           ;(PFSAV CONTAINS SAVED CONTENTS)
                                           ;CHECK CSR AFTER POWER UP
012506 005077 166300          CLR      @BUSCSR
012512 032777 001000 166272  BIT      @1000,@BUSCSR
012520 001374          BNE      .-6
                                           ;CSR INCORRECT AFTER POWER UP - SHOULD BE
                                           ;CONNECTED TO THE OTHER CPU

;CHECK WITH SWITCH IN THE CONTROLLED BUT NOT CONNECTED POSITION
TEST48: SCOPE
        CLR      @BUSCSR
        MSG17
012522 104406          HLT          ;INITIALIZE CSR
012524 005077 166262          HLT          ;REQUEST OPERATOR TO CLEAR SWITCH REGISTER OF OTHER
012530 104042          HLT          ;PROCESSOR, SET SWITCH 6, AND THEN
                                           ;PRESS CONTINUE ON THIS PROCESSOR
012532 000000          HLT          ;SETUP POWER DOWN RETURN
012534 012737 012566 000024  MOV      @RET48,@24

```

```

012542 017737 166266 000026      MOV      @PSR,@26
012550 104074      PMSG30
012552 104052      PMSG21
012554 000000      HALT

012556 012777 000002 166226      MOV      @2,@BUSCSR
012564 000774      BR      .-6

012566 012737 012616 000024  RETA48: MOV      @RETB48,@24
012574 017767 166212 166270      MOV      @BUSCSR,PFSAV
012582 010667 166262      MOV      SP,SPSAV
012586 000000      HALT
012590 016706 166254      MOV      SPSAV,SP
012594 104410      HLT
012596 016706 166246  RETB48: MOV      SPSAV,SP
012598 022626      CMP      (SP)+,(SP)+
012602 012737 000026 000024      MOV      @26,@24
012606 005037 000026      CLR      @26
012610 005027 000000      CLR      @0
012614 005367 177772      DEC      .-2
012618 001375      BNE      .-1
012622 022767 020202 166214      CMP      @20202,PFSAV
012626 001401      BEQ      .+4
012630 104410      HLT

012662 022777 020000 166122      CMP      @20000,@BUSCSR
012670 001401      BEQ      .+4
012674 104410      HLT
012678 005077 166112      CLR      @BUSCSR
012700 032777 001000 166104      BIT      @1000,@BUSCSR
012706 001374      BNE      .-6

:CHECK WITH SWITCH IN NEUTRAL
012710 104406  TEST49: SCOPE
012712 104012      PMSG5
012714 000000      HALT

012716 012737 012736 000024      MOV      @RETB49,@24
012724 017737 166104 000026      MOV      @PSR,@26
012732 104054      PMSG22

012734 000777      BR
012736 012737 012766 000024  RETA49: MOV      @RETB49,@24
012744 017767 166042 166120      MOV      @BUSCSR,PFSAV
012752 010667 166112      MOV      SP,SPSAV
012756 000000      HALT
012760 016706 166104      MOV      SPSAV,SP
012764 104410      HLT
012766 016706 166076  RETB49: MOV      SPSAV,SP
012772 022626      CMP      (SP)+,(SP)+
012774 012737 000026 000024      MOV      @26,@24
013002 005037 000026      CLR      @26

```

```

:PRINT MESSAGE: "WHEN THIS
:PRINTOUT IS FINISHED, PRESS
:"CONTINUE", THEN POWER DOWN
:THIS PROCESSOR AND THEN POWER
:THIS PROCESSOR BACK UP."
:REQUEST SWITCH
:REREQUEST SWITCH UNTIL POWER DOWN OCCURS
:TO AVOID TIMEOUT
:SETUP POWER UP RETURN
:SAVE CONTENTS OF CSR FOR CHECKING
:SAVE STACK POINTER
:HALT ON POWER DOWN

:NO POWER UP RESTART OCCURRED
:RESTORE STACK POINTER ON POWER UP

:RESTORE TRAP CATCHER IN POWER
:FAIL VECTOR ADDRESS
:STALL SO THAT TTY
:OUTPUT WON'T BE
:GARBLED
:CHECK SAVED CONTENTS OF CSR
:AT TIME OF POWER DOWN
:CSR INCORRECT AT TIME OF POWER
:DOWN (PFSAV CONTAINS SAVED CONTENTS)
:CHECK CSR AFTER POWER UP

:CSR INCORRECT AFTER POWER UP

:REQUEST OPERATOR TO CLEAR
:SWITCH REGISTER OF OTHER PROCESSOR
:AND THEN PRESS "CONTINUE" ON THIS PROCESSOR
:SETUP POWER DOWN RETURN

:PRINT MESSAGE: "POWER DOWN THIS PROCESSOR,
:CHANGE THE SWITCH REGISTER OF THE
:OTHER PROCESSOR - SET SWITCH NINE
:TO A ONE AND THEN POWER THIS
:PROCESSOR BACK UP."
:WAIT FOR POWER FAIL TRAP TO OCCUR
:SETUP POWER UP RETURN
:SAVE CONTENTS OF CSR FOR CHECKING
:SAVE STACK POINTER
:POWER DOWN HALT

:POWER UP RESTART NEVER OCCURRED AFTER POWER DOWN
:RESTORE STACK ON POWER UP

:RESTORE TRAP CATCHER IN POWER
:FAIL VECTOR ADDRESS

```



```

013174 005777 165612          TST      2BUSCSR      ;AND SWITCH SHOULD STILL HAVE BEEN IN POSITION REQUESTED
013200 001401                    BEQ      .+4          ;CSR SHOULD BE CLEARED ON POWER UP
013202 104410                    HLT

013204 012737 000026 000024    MOV      226,224    ;CSR NOT CLEAR (ZERO) AFTER
013212 005037 000026          CLR      226        ;SWITCH POWERED DOWN AND BACK UP
013216 012737 013244 000004    MOV      2RETSOC,224 ;RESTORE TRAP CATCHER IN
013224 017737 165604 000006    MOV      2PSR,226   ;POWER FAIL TRAP VECTOR
013232 016777 165620 165614    MOV      2RMBITS,20VADRS ;SETUP ADDRESS TIMEOUT RETURN

013240 104410                    HLT          ;CHECK TO SEE IF SWITCHED BUS IS STILL CONNECTED
;BY REFERENCING AN ADDRESS ON THE SWITCHED BUS
;SWITCHED BUS STILL CONNECTED
;AFTER SWITCH WAS POWERED DOWN AND BACK UP

013242 000401                    BR       CONT50
013244 022626                    RET50C:  CMP      (SP)+,(SP)+ ;RESTORE STACK POINTER AFTER TIMEOUT TRAP
013246 012737 000006 000004    CONT50:  MOV      26,224 ;RESTORE TRAP CATCHER
013254 005037 000006          CLR      226
013260 005077 165526          CLR      2BUSCSR    ;REINITIALIZE SWITCH
013264 032777 001000 165520    BIT      21000,2BUSCSR
013272 001374                    BNE     .-6

;NOW CHECK SWITCH POWER FAIL WITH THE
;SWITCH INITIALLY CONTROLLED BY BUT NOT
;CONNECTED TO THIS PROCESSOR
013274 104406                    TEST51:  SCOPE
013276 005767 165602          TST      DT11AF    ;IF DT11-A, SKIP MESSAGE
013302 001002                    BNE     .+6
013304 104044                    PMSG18

;PRINT MESSAGE: "CHANGE SWITCH REGISTER
;OF OTHER PROCESSOR. CLEAR IT AND THEN
;SET SWITCH SEVEN TO A ONE. THEN PRESS
;'CONTINUE' ON THIS PROCESSOR."
013306 000000                    HALT
013310 012777 000002 165474    MOV      22,2BUSCSR ;REQUEST THE SWITCH
013316 105777 165470          TSTB    2BUSCSR    ;WAIT FOR SWITCH TO
013322 100375                    BPL     .-4        ;CONNECT
013324 012737 013344 000024    MOV      2RETSOC,24 ;SETUP POWER FAIL RETURN
013332 017737 165476 000026    MOV      2PSR,226
013340 104056                    PMSG23

;PRINT MESSAGE: "POWER DOWN THE BUS SWITCH, THEN POWER
;THE BUS SWITCH BACK UP."
;WAIT FOR POWER FAIL TRAP
;SETUP POWER UP RETURN
013342 000777                    BR       .
013344 012737 013374 000024    RET51A:  MOV      2RETS1B,224 ;SAVE CSR ON POWER DOWN
013352 017767 165434 165512    MOV      2BUSCSR,PFSAV ;SAVE STACK POINTER
013360 010667 165504          MOV      SP,SPSAV  ;POWER DOWN HALT
013364 000000                    HALT
013366 016706 165476          MOV      SPSAV,SP
013372 104410                    HLT
013374 016706 165470          RET51B:  MOV      SPSAV,SP ;POWER UP RESTART NEVER OCCURRED AFTER POWER DOWN
013400 022626                    CMP      (SP)+,(SP)+ ;RESTORE STACK POINTER ON POWER UP
013402 005027 000000          CLR      20
013406 005367 177772          DEC     .-2
013412 001375                    BNE     .-4
013414 022767 060202 165450    CMP      260202,PFSAV ;CHECK SAVED CONTENTS OF
;CSR ON POWER DOWN

013422 001401                    BEQ     .+4
013424 104410                    HLT
;CSR INCORRECT ON POWER DOWN
;BIT 14 SHOULD HAVE BEEN SET
;AND SWITCH SHOULD STILL HAVE BEEN IN POSITION REQUESTED

```



DZDTA-B MACY11 27(732) 27-OCT-76 15:57 PAGE 48  
DZDTA.B

```

013670 104410          HLT          ;CSR NOT CLEAR (ZERO) AFTER
                                ;SWITCH POWERED DOWN AND BACK UP
013672 012737 000026 000024      MOV      #26, @24      ;RESTORE TRAP CATCHER IN
013700 005037 000026             CLR      @26          ;POWER FAIL TRAP VECTOR
013704 005077 165102             CLR      @BUSCSR     ;REINITIALIZE SWITCH
013710 032777 001000 165074      BIT      @1000, @BUSCSR
013716 001374             BNE      .-6

;SHOW THAT IF A DEVICE ON THE SWITCHED BUS IS POWERED DOWN,
;THE SWITCH WILL GO TO NEUTRAL AND, AFTER DC LO HAS OCCURRED
;ON THE SWITCHED BUS, THE SWITCH CANNOT BE CONNECTED TO
;EITHER PROCESSOR UNTIL THE DEVICE IS POWERED BACK UP.
;BIT 14 SHOULD REMAIN SET UNTIL THE DEVICE IS POWERED UP
;THESE TESTS ARE PARTIALLY INHIBITED IF SW9 IS SET SINCE THAT INDICATES
;THAT THE POWER SUPPLIES ON THE SWITCHED BUS WON'T HOLD DOWN AC AND
;DC LO WHEN POWERED DOWN
013720 105767 165127          TSTB     SBINH+1      ;IF SW 8 WAS SET, INHIBIT ALL SWITCHED BUS
                                ;POWER FAIL TESTING
013724 001407          BEQ      CNTSB
013726 005767 165152          TST      DT11AF      ;SKIP MESSAGE IF DT11-A
013732 001002             BNE      .+6
013734 104012          PMSG5
013736 000000          HALT
013740 000167 001664          JMP      DONE
013744 105767 165102      CNTSB: TSTB     SBINH      ;SWITCHED BUS POWER DOWN INHIBITED?
013750 001402          BEQ      TEST53      ;NO-RUN TESTS
013752 000167 001354          JMP      TEST55      ;YES, SKIP TESTS

;FIRST, CHECK IT WITH THE SWITCH CONNECTED TO THIS PROCESSOR
TEST53: SCOPE
013756 104406          TST      DT11AF
013760 005767 165120          BNE      .+6
013764 001002          PMSG19
013766 104046          ;PRINT MESSAGE: "CHANGE SWITCH REGISTER OF THE
                                ;OTHER PROCESSOR, CLEAR IT
                                ;AND THEN SET SWITCH EIGHT TO A ONE.
                                ;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."
013770 000000          HALT
013772 012777 000001 165012      MOV      #1, @BUSCSR
014000 012737 014044 000024      MOV      @RET53A, @24
014006 017737 165022 000026      MOV      @PSR, @26
014014 104014          PMSG6
                                ;PRINT MESSAGE: "POWER DOWN ONE DEVICE ON THE SWITCHED
                                ;BUS. AND THEN SET SWITCH 0 IN THIS
                                ;PROCESSOR'S SWITCH REGISTER."
                                ;WAIT FOR SWITCH REGISTER SWITCH 0 TO SET
                                ;SHOULD TRAP OUT DUE TO POWER FAIL
                                ;NO POWER FAIL TRAP ON POWERING DOWN A
                                ;SWITCHED BUS DEVICE WHEN THIS PROCESSOR
                                ;HAD THE SWITCH
014016 032777 000001 165012      BIT      #1, @SR
014024 001774             BEQ      .-6
014026 104410          HLT

014030 012737 000026 000024      MOV      #26, @24
014036 005037 000026             CLR      @26
014042 000474             BR      CONT53
014044 012737 014074 000024      RET53A: MOV     @RET53B, @24
014052 010667 165012          MOV     SP, SPSAV
014056 017767 164730 165006      MOV     @BUSCSR, PPSAV
014064 000000          HALT
                                ;SETUP POWER UP RETURN
                                ;SAVE STACK POINTER
                                ;SAVE CSR AT TIME OF POWER DOWN TRAP
                                ;NO POWER UP OCCURRED AFTER SWITCHED BUS
                                ;DEVICE WAS POWERED DOWN. THE SWITCH SHOULD
                                ;HAVE GONE TO NEUTRAL AND ALLOWED THE CPU

```





```

014346 005037 000026          CLR      2#26
014352 032777 001000 164432        BIT      #1000,2BUSCSR
014360 001374          BNE     .-6
014362 000470          BR      TEST54
014364 012737 014414 000024  RET53D: MOV     #RET53E,2#24 ;SETUP POWER UP RETURN AFTER ILLEGAL POWER FAIL
014372 010667 164472          MOV     SP,SPSAV
014376 017767 164410 164466        MOV     2BUSCSR,PFSAV ;SAVE CSR CONTENTS IN CASE NEEDED
014404 000000          HALT   ;POWER DOWN HALT AFTER SWITCH RECONNECTED WITH A
                                ;SWITCHED BUS DEVICE STILL POWERED DOWN

014406 016706 164456          MOV     SPSAV,SP
014412 104410          HLT
014414 016706 164450          RET53E: MOV     SPSAV,SP ;NO POWER UP RESTART OCCURRED
014420 022626          CMP     (SP)+,(SP)+ ;RESTORE STACK POINTER AFTER POWER UP
014422 012737 000026 000024        MOV     #26,2#24 ;RESTORE TRAP CATCHER TO POWER FAIL VECTOR
014430 005037 000026          CLR     2#26
014434 005027 000000          CLR     #0 ;STALL SO THAT TTY OUTPUT WON'T BE GARBLED
014440 005367 177772          DEC     .-2
014444 001375          BNE     .-4
014446 104410          HLT   ;POWER FAIL TRAP OCCURRED WHEN THE SWITCH
                                ;WAS REQUESTED AFTER A SWITCHED BUS DEVICE
                                ;HAD BEEN POWERED DOWN

014450 000671          BR      CONT53
014452 012737 014474 000024  RET53F: MOV     #RET53H,2#24 ;SETUP POWER UP AFTER ILLEGAL POWER DOWN
014460 010667 164404          MOV     SP,SPSAV
014464 017767 164322 164400        MOV     2BUSCSR,PFSAV ;SAVE CSR CONTENTS IN CASE NEEDED
014472 000000          HALT   ;POWER DOWN HALT- TRAP OCCURRED
                                ;WHEN THE SWITCH CONNECTED WHEN
                                ;REQUESTED AFTER A SWITCHED BUS DEVICE
                                ;WAS POWERED DOWN AND BACK UP
                                ;RESTORE STACK POINTER AFTER POWERUP

014474 016706 164370          RET53H: MOV     SPSAV,SP
014500 022626          CMP     (SP)+,(SP)+ ;RESTORE TRAP CATCHER
014502 012737 000026 000024        MOV     #26,2#24
014510 005037 000026          CLR     2#26
014514 005027 000000          CLR     #0 ;STALL SO THAT TTY OUTPUT WON'T BE GARBLED
014520 005367 177772          DEC     .-2
014524 001375          BNE     .-4
014526 104410          HLT   ;POWER FAIL TRAP OCCURRED WHEN SWITCH WAS
                                ;REQUESTED AFTER A SWITCHED BUS DEVICE WAS POWERED
                                ;DOWN AND BACK UP

014530 005077 164256          CLR     2BUSCSR
014534 032777 001000 164250        BIT     #1000,2BUSCSR
014542 001374          BNE     .-6

                                ;THEN CHECK IT WITH THE SWITCH CONTROLLED BY BUT NOT CONNECTED TO THIS
                                ;PROCESSOR
014544 104406          TEST54: SCOPE
014546 005767 164332          TST    DT11AF
014552 001002          BNE     .+6
014554 104046          PMSG19 ;PRINT MESSAGE:"CHANGE SWITCH REGISTER OF THE
                                ;OTHER PROCESSOR. CLEAR IT
                                ;AND THEN SET SWITCH EIGHT TO A ONE.
                                ;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."

014556 000000          HALT
014560 012777 000002 164224        MOV     #2,2BUSCSR
014566 012737 014632 000024        MOV     #RET54A,2#24 ;REQUEST SWITCH
014574 017737 164234 000026        MOV     2PSR,2#26 ;SETUP POWER FAIL RETURN

```

```

014602 104014          PMSG6          ;PRINT MESSAGE: "POWER DOWN ONE DEVICE ON THE SWITCHED
                                ;BUS. AND THEN SET SWITCH 0 IN THIS
                                ;PROCESSOR'S SWITCH REGISTER."
014604 032777 000001 164224      BIT      #1,2SR          ;WAIT FOR SWITCH REGISTER SWITCH 0 TO SET
014612 001774          BEQ      #-6             ;SHOULD TRAP OUT DUE TO POWER FAIL
014614 104410          HLT                    ;NO POWER FAIL TRAP ON POWERING DOWN A
                                ;SWITCHED BUS DEVICE WHEN THIS PROCESSOR
                                ;HAD THE SWITCH
                                ;RESTORE TRAP CATCHER
014616 012737 000026 000024      MOV      #26,2#24
014624 005037 000026          CLR      2#26
014630 000474          BR       CONT54
014632 012737 014662 000024  RET54A: MOV    #RET54B,2#24  ;SETUP POWER UP RETURN
014640 010667 164224          MOV    SP,SPSAV      ;SAVE STACK POINTER
014644 017767 164142 164220      MOV    2BUSCSR,PFSAV ;SAVE CSR AT TIME OF POWER DOWN TRAP
014652 000000          HLT                    ;NO POWER UP OCCURRED AFTER SWITCHED BUS
                                ;DEVICE WAS POWERED DOWN. THE SWITCH SHOULD
                                ;HAVE GONE TO NEUTRAL AND ALLOWED THE CPU
                                ;TO POWER BACK UP.
014654 016706 164210          MOV    SPSAV,SP      ;NO POWER UP RESTART OCCURRED
014660 104410          HLT                    ;RESTORE STACK POINTER
014662 016706 164202          RET54B: MOV   SPSAV,SP
014666 022626          CMP    (SP)+,(SP)+  ;SETUP NEW POWER FAIL VECTOR IN CASE
014670 012737 015152 000024      MOV    #RET54D,2#24 ;SWITCH CONNECTS WHEN REQUESTED
                                ;STALL SO THAT TTY
                                ;OUTPUT WILL BE OK
014676 005027 000000          CLR    #0
014702 005367 177772          DEC    #-2
014706 001375          BNE    #-4
014710 032777 000001 164120      BIT    #1,2SR       ;WAIT FOR SWITCH REGISTER SWITCH 0 TO BE SET
014716 001774          BEQ    #-6
014720 022767 060202 164144      CMP    #60202,PFSAV ;CHECK SAVED CONTENTS OF CSR AT TIME OF
                                ;POWER DOWN TRAP
014726 001401          BEQ    .+4
014730 104410          HLT                    ;CSR INCORRECT WHEN THE POWER FAIL OCCURRED
014732 022777 040000 164052      CMP    #40000,2BUSCSR ;CHECK CSR NOW - BIT 14 SHOULD BE SET
014740 001401          BEQ    .+4
014742 104410          HLT                    ;CSR INCORRECT - ONLY BIT 14 SHOULD BE SET
014744 012777 000001 164040      MOV    #1,2BUSCSR   ;REQUEST SWITCH - SHOULDN'T CONNECT SINCE
                                ;SB DEVICE IS POWERED DOWN
                                ;STALL
014752 005327 000000          DEC    #0
014756 001375          BNE    #-4
014760 022777 040001 164024      CMP    #40001,2BUSCSR ;CK CSR
014766 001401          BEQ    .+4
014770 104410          HLT                    ;CSR INCORRECT - ONLY REQUEST AND BIT 14
                                ;SHOULD BE SET
014772 012737 015012 000004      MOV    #RET54C,2#4   ;SETUP ADDRESS TIMEOUT RETURN
015000 016777 164052 164046      MOV    RWBITS,2VADR  ;REFERENCE A LOCATION ON THE SWITCHED BUS
                                ;SHOULD TRAP SINCE SWITCH IS NOT CONNECTED
                                ;SWITCHED BUS ACTUALLY CONNECTED
015006 104410          HLT                    ;CLEAR REQUEST
015010 000401          BR       CNT54A
015012 022626          CMP    (SP)+,(SP)+
015014 012737 000006 000004  RET54C: CNT54A: MOV  #6,2#4
015022 105077 163764          CNT54A: CLR    2BUSCSR
015026 032777 001000 163756      CNT54C: BIT    #1000,2BUSCSR
015034 001374          BNE    #-6
015036 052777 004000 163746      BIS    #4000,2BUSCSR ;SET COM1- THE OTHER SIDE SHOULD SEE IT
015044 012737 015240 000024      MOV    #RET54F,2#24

```

015052	104016				PMSG7				:PRINT MESSAGE: "POWER THE DEVICE :BACK UP, AND THEN CLEAR SWITCH 0 IN THIS :PROCESSOR'S SWITCH REGISTER." :WAIT FOR OPERATOR TO CLEAR SWITCH REGISTER SWITCH 0
015054	032777	000001	163754		BIT	#1,CSR			
015062	001374				BNE	.-6			
015064	042777	004000	163720		BIC	#4000,ABUSCSR			:OTHER SIDE SHOULD HAVE SEEN COM BIT SET BY NOW
015072	005777	163714			TST	ABUSCSR			:CHECK CSR AFTER POWER UP OF SWITCHED BUS :DEVICE
015076	001401				BEQ	+.4			:CSR INCORRECT AFTER POWER UP OF SWITCHED :BUS DEVICE - SHOULD HAVE BEEN CLEARED
015100	104410				HLT				:TRY TO CONNECT SWITCH
015102	012777	000001	163702		MOV	#1,ABUSCSR			
015110	000240				NOP				
015112	105777	163674			TSTB	ABUSCSR			:CHECK SWITCH CONNECTED BIT
015116	100401				BMI	+.4			:BRANCH IF SET
015120	104410				HLT				:SWITCH DIDN'T CONNECT AFTER BIT 0 WAS SET
015122	005077	163664			CLR	ABUSCSR			:INITIALIZE CSR
015126	012737	000026	000024		MOV	#26,ABUSCSR			:RESTORE TRAP CATCHER
015134	005037	000026			CLR	ABUSCSR			
015140	032777	001000	163644		BIT	#1000,ABUSCSR			
015146	001374				BNE	.-6			
015150	000470				BR	TEST55			
015152	012737	015202	000024	RETS4D:	MOV	#RETS4E,ABUSCSR			:SETUP POWER UP RETURN AFTER ILLEGAL POWER FAIL
015160	010667	163704			MOV	SP,SPSAV			
015164	017767	163622	163700		MOV	ABUSCSR,PFSAV			:SAVE CSR CONTENTS IN CASE NEEDED
015172	000000				HALT				:POWER DOWN HALT AFTER SWITCH RECONNECTED WITH A :SWITCHED BUS DEVICE STILL POWERED DOWN
015174	016706	163670			MOV	SPSAV,SP			
015200	104410				HLT				:NO POWER UP RESTART OCCURRED
015202	016706	163662		RETS4E:	MOV	SPSAV,SP			:RESTORE STACK POINTER AFTER POWER UP
015206	022626				CMR	(SP)+,(SP)+			
015210	012737	000026	000024		MOV	#26,ABUSCSR			:RESTORE TRAP CATCHER TO POWER FAIL VECTOR
015216	005037	000026			CLR	ABUSCSR			
015222	005027	000000			CLR	#0			:STALL SO THAT TTY OUTPUT WON'T BE GARBLED
015226	005367	177772			DEC	.-2			
015232	001375				BNE	.-4			
015234	104410				HLT				:POWER FAIL TRAP OCCURRED WHEN THE SWITCH :WAS REQUESTED AFTER A SWITCHED BUS DEVICE :HAD BEEN POWERED DOWN
015236	000671				BR	CONT54			
015240	012737	015262	000024	RETS4F:	MOV	#RETS4H,ABUSCSR			:SETUP POWER UP AFTER ILLEGAL POWER DOWN
015246	010667	163616			MOV	SP,SPSAV			
015252	017767	163534	163612		MOV	ABUSCSR,PFSAV			:SAVE CSR CONTENTS IN CASE NEEDED
015260	000000				HALT				:POWER DOWN HALT- TRAP OCCURRED :WHEN THE SWITCH CONNECTED WHEN :REQUESTED AFTER A SWITCHED BUS DEVICE :WAS POWERED DOWN AND BACK UP
015262	016706	163602		RETS4H:	MOV	SPSAV,SP			:RESTORE STACK POINTER AFTER POWERUP
015266	022626				CMR	(SP)+,(SP)+			
015270	012737	000026	000024		MOV	#26,ABUSCSR			:RESTORE TRAP CATCHER
015276	005037	000026			CLR	ABUSCSR			
015302	005027	000000			CLR	#0			:STALL SO THAT TTY OUTPUT WON'T BE GARBLED
015306	005367	177772			DEC	.-2			
015312	001375				BNE	.-4			
015314	104410				HLT				:POWER FAIL TRAP OCCURRED WHEN SWITCH WAS :REQUESTED AFTER A SWITCHED BUS DEVICE WAS POWERED :DOWN AND BACK UP

015316 005077 163470  
 015322 032777 001000 163462  
 015330 001374

CLR 0BUSCSR  
 BIT 01000,0BUSCSR  
 BNE .-6

: FINALLY, CHECK IT WITH THE SWITCH IN NEUTRAL  
 : SHOW THAT WHEN THE SWITCH IS IN NEUTRAL, BIT 14 GETS SET WHEN A DEVICE  
 : IS POWERED DOWN ON THE SWITCHED BUS, AND BIT 14 GETS CLEARED WHEN IT IS  
 : POWERED BACK UP  
 : SHOW THAT NO POWER FAIL TRAP OCCURS  
 : ALSO SHOW THAT BIT 14 OF THE CSR IS READ ONLY

015332 104406  
 015334 005077 163452  
 015340 012737 015560 000024  
 015346 017737 163462 000026  
 015354 005767 163524  
 015360 001007  
 015362 105767 163464  
 015366 001402  
 015370 104062  
 015372 000402  
 015374 104046  
 015376 000000

TEST55: SCOPE  
 CLR 0BUSCSR  
 MOV #RET55,0#24  
 MOV 0PSR,0#26  
 TST DT11AF  
 BNE CNT55  
 TSTB SBINH  
 BEQ .+6  
 PMSG25  
 BR .+6  
 PMSG19  
 HALT

: PUT SWITCH IN NEUTRAL  
 : SETUP POWER FAIL RETURN IN CASE  
 : SR 9 SET?  
 : IF NOT SET, ALLOW FULL TESTING  
 : REQUEST OPERATOR TO CLEAR SWITCH  
 : REGISTER OF OTHER PROCESSOR  
 : REQUEST OPERATOR TO CLEAR SWITCH  
 : REGISTER OF OTHER PROCESSOR, AND  
 : THEN SET SWITCH 8  
 : REQUEST OPERATOR TO POWER DOWN ONE DEVICE ON THE  
 : SWITCHED BUS, AND THEN SET SWITCH  
 : ZERO IN THIS PROCESSOR'S SWITCH REGISTER  
 : WAIT FOR BIT 14 TO SET OR FOR  
 : SWITCH REGISTER SWITCH 0 TO  
 : BE SET  
 : CSR INCORRECT WHEN SWITCHED BUS  
 : DEVICE WAS POWERED DOWN - AC LO  
 : NEVER SET

015400 104014  
 015402 032777 040000 163402  
 015410 001006  
 015412 032777 000001 163416  
 015420 001770  
 015422 104410

CNT55: PMSG6  
 LOP55A: BIT #40000,0BUSCSR  
 BNE LOP55B  
 BIT 01,0SR  
 BEQ LOP55A  
 HLT

015424 000404  
 015426 032777 000001 163402  
 015434 001774  
 015436 032777 040000 163346  
 015444 001413  
 015446 105767 163400  
 015452 001010

BR CNT55A  
 LOP55B: BIT 01,0SR  
 BEQ .-6  
 CNT55A: BIT #40000,0BUSCSR  
 BEQ CNT55B  
 TSTB SBINH  
 BNE CNT55B

: WAIT FOR SWITCH REGISTER SWITCH 0  
 : TO BE SET  
 : IF BIT 14 IS SET, SHOW THAT IT IS RDO  
 : SKIP IF ONLY CHECKING THAT AC LO CAN BE SET  
 : SINCE IT MAY GO CLEAR WHEN POWER  
 : SUPPLY LETS IT FLOAT  
 : BIC TO CSR SHOULDN'T AFFECT BIT 14  
 : CHECK BIT 14

015454 042777 040000 163330  
 015462 032777 040000 163322  
 015470 001001  
 015472 104410  
 015474 052777 004000 163310  
 015502 012737 000026 000024  
 015510 005037 000026  
 015514 104016

BIC #40000,0BUSCSR  
 BIT #40000,0BUSCSR  
 BNE .+4  
 HLT  
 CNT55B: BIS #4000,0BUSCSR  
 MOV #26,0#24  
 CLR 0#26  
 PMSG7

: BIT 14 CLEARED VIA A BIC  
 : SET COM1 - SHOULD BE SEEN BY OTHER SIDE  
 : RESTORE TRAP CATCHER  
 : REQUEST OPERATOR TO POWER THE DEVICE BACK UP AND  
 : THEN CLEAR SWITCH ZERO IN THIS  
 : PROCESSOR'S SWITCH REGISTER  
 : WAIT FOR SWITCH ZERO TO BE  
 : CLEARED  
 : CLEAR COM1- SHOULD HAVE BEEN SEEN BY NOW  
 : CK CSR

015516 032777 000001 163312  
 015524 001374  
 015526 042777 004000 163256  
 015534 005777 163252  
 015540 001401

BIT 01,0SR  
 BNE .-6  
 BIC #4000,0BUSCSR  
 TST 0BUSCSR  
 BEQ .+4

015542	104410			HLT					:CSR INCORRECT AFTER SB DEVICE :POWERED BACK UP
015544	005767	163334		TST	DT11AF				
015550	001027			BNE	DONE				
015552	104012			PMSG5					:REQUEST OPERATOR TO CLEAR SWITCH REGISTER :OF THE OTHER CPU
015554	000000			HALT					:SKIP ERROR SECTION
015556	000424			BR	DONE				
015560	012737	015602	000024	RET55: MOV	#RET55A, #124				
015566	010667	163276		MOV	SP, SPSAV				
015572	000000			HALT					:POWER FAIL TRAP OCCURRED ON POWERING :DOWN A SWITCHED BUS DEVICE WITH :THE SWITCH IN NEUTRAL TO :RECOVER, PRESS CONTINUE
015574	016706	163270		MOV	SPSAV, SP				
015600	104410			HLT					:NO POWER UP RESTART OCCURRED
015602	016706	163262		RET55A: MOV	SPSAV, SP				
015606	022626			CMP	(SP)+, (SP)+				
015610	005027	000000		CLR	#0				:STALL SO THAT TTY :OUTPUT WON'T BE :GARBLED
015614	005367	177772		DEC	.-2				:POWER FAIL TRAP OCCURRED :WHEN A DEVICE ON THE :SWITCHED BUS WAS POWERED DOWN :WITH THE SWITCH IN NEUTRAL
015620	001375			BNE	.-4				
015622	104410			HLT					
015624	000167	177644		JMP	CNT55B				
015630	104406			DONE: SCOPE					
015632	005167	163240		COM	INITF				:TOGGLE FLAG THAT INDICATES WHETHER :OR NOT THE TEST IS BEING RUN :IN THE "INHIBIT INIT" STATE :BRANCH IF THIS PASS WAS RUN WITH "INIT-INHIBIT INIT" :IN THE "INHIBIT INIT" POSITION :REQUEST THAT "INIT-INHIBIT INIT" :SWITCH BE PUT IN THE "INHIBIT :INIT" POSITION
015636	100012			BPL	INITPS				
015640	104030			PMSG12					
015642	000000			HALT					
015644	005077	163142		CLR	#BUSCSR				
015650	032777	001000	163134	BIT	#1000, #BUSCSR				
015656	001374			BNE	.-6				
015660	000167	000164		JMP	TRCK				:RUN A PASS WITH THE SWITCH :IN "INHIBIT INIT" STATE AND T-BIT SET
015664	005767	163214		INITPS: TST	DT11AF				
015670	001013			BNE	INITPB				
015672	104110			PMSG36					:REQUEST OPERATOR TO SET SR SWITCH :12 OF THE OTHER CPU
015674	000000			HALT					:CHECK CSR BIT 12- IF SET, ERRORS OCCURRED :ON THE OTHER SIDE
015676	032777	010000	163106	BIT	#10000, #BUSCSR				
015704	001403			BEG	.-10				
015706	012767	177777	004016	MOV	#-1, ERR				:SET FLAG INDICATING ERRORS OCCURRED ON :THE OTHER SIDE :REQUEST OPERATOR TO CLEAR SR OF :THE OTHER CPU
015714	104012			PMSG5					:PRINT MESSAGE: "END OF PASS"
015716	000000			HALT					:DID ANY ERRORS OCCUR? :YES - BRANCH :NO - PRINT MESSAGE "NO ERRORS OCCURRED"
015720	104076			INITPB: PMSG31					
015722	005767	004004		TST	ERR				
015726	100402			BMI	.-6				
015730	104100			PMSG32					
015732	000401			BR	.-4				
015734	104102			PMSG33					:PRINT MESSAGE "ERRORS OCCURRED"



```

016146 005067 002720 CLR FLAGS
016152 005777 162660 TST 2SR ;ANY SR SWITCHES SET?
016156 001775 BEQ .-4 ;NO, WAIT

;SET BIT 0 OF THE DT11 CSR IF SWITCH REGISTER SWITCH 0 IS SET
016160 032777 000001 162650 SRM1: BIT 01,2SR ;CHECK SWITCH REGISTER SWITCH ZERO
016166 001414 BEQ SRM2 ;GO TO NEXT IF NOT SET
016170 005327 000000 DEC 80 ;STALL TO IGNORE SWITCH REGISTER BOUNCE
016174 001375 BNE .-4
016176 012777 000001 162606 MOV 01,2BUSCSR ;REQUEST BUS SWITCH BY SETTING BIT 0 OF THE CSR
016204 032777 000001 162624 BIT 01,2SR
016212 001374 BNE .-6
016214 000167 177704 JMP SRMEX

;SET BIT 1 OF THE DT11 CSR IF SWITCH REGISTER SWITCH 1 IS SET
016220 032777 000002 162610 SRM2: BIT 02,2SR ;EXECUTE THIS SECTION IF SWITCH 1 IS SET
016226 001414 BEQ SRM3
016230 005327 000000 DEC 80 ;STALL TO AVOID SWITCH REGISTER BOUNCE
016234 001375 BNE .-4
016236 012777 000002 162546 MOV 02,2BUSCSR ;REQUEST BUS SWITCH BY SETTING BIT 1 OF THE CSR
016244 032777 000002 162564 BIT 02,2SR
016252 001374 BNE .-6
016254 000167 177644 JMP SRMEX

;SET COMMUNICATION BIT OF THE CSR IF SWITCH REGISTER SWITCH 2 IS SET
016260 032777 000004 162550 SRM3: BIT 04,2SR ;EXECUTE THIS SECTION IF SWITCH 2 IS SET
016266 001414 BEQ SRM4
016270 005327 000000 DEC 80 ;STALL TO IGNORE SWITCH REGISTER BOUNCE
016274 001375 BNE .-4
016276 052777 004000 162506 BIS 04000,2BUSCSR ;SET COMMUNICATION BIT (CSR BIT 11)
016304 032777 000004 162524 BIT 04,2SR
016312 001374 BNE .-6
016314 000167 177604 JMP SRMEX

;IF SWITCH REGISTER SWITCH 3 IS SET, EXECUTE THIS ROUTINE
;CK PROCESSOR POWER FAIL IF OTHER SIDE HAS THE SWITCH
;OR IF THE SWITCH IS IN NEUTRAL
016320 032777 000010 162510 SRM4: BIT 010,2SR ;EXECUTE THIS SECTION IF SWITCH 3 IS SET
016326 001502 BEQ SRM5
016330 005327 000000 DEC 80 ;STALL TO IGNORE SWITCH REGISTER BOUNCE
016334 001375 BNE .-4
016336 012777 002400 162446 MOV 02400,2BUSCSR ;SET BOTH INTERRUPT ENABLES IN CASE
016344 012737 016424 000024 MOV 0RETH4A,2824 ;SETUP POWER FAIL RETURN IN CASE
016352 005037 000026 CLR 2826
016356 032777 040000 162426 SRM4A: BIT 040000,2BUSCSR ;CHECK BIT 14-SHOULDN'T SET
016364 001401 BEQ .+4
016366 104410 HLT ;BIT 14 IN CSR SET DUE TO POWER
;FAIL ON OTHER PROCESSOR BUS
;CHECK SWITCH REGISTER
;IF SWITCH IS DOWN, BUS SWITCH
;SHOULD HAVE GONE TO NEUTRAL

016370 032777 000010 162440 BIT 010,2SR
016376 001367 BNE SRM4A
016400 032777 020000 162404 BIT 020000,2BUSCSR
016406 001401 BEQ .+4
016410 104410 HLT ;NON-NEUTRAL BIT STILL SET AFTER
;POWER FAIL ON OTHER BUS SHOULD
;HAVE DISCONNECTED THE BUS SWITCH

016412 012737 000026 000024 MOV 026,2824
  
```



```

016420 000167 177500          JMP          SRMEX
016424 012737 016470 000024 RETM4A: MOV      @RETM4B, @24      ; SETUP POWER UP RETURN
016432 010667 162432          MOV      SP, SPSAV      ; SAVE STACK POINTER
016436 000000          HALT
016440 016706 162424          MOV      SPSAV, SP      ; POWER DOWN HALT (NO POWER FAIL
016444 104410          HLT                    ; SHOULD HAVE OCCURRED)
                                ; POWER FAIL TRAP (DOWN ONLY)
                                ; OCCURRED
                                ; RESTORE TRAP CATCHER

016446 012737 000026 000024      MOV      @26, @24
016454 032777 000010 162354      BIT      @10, @SR
016462 001374          BNE      .-6
016464 000167 177434          JMP      SRMEX
016470 016706 162374          RETM4B: MOV      SPSAV, SP      ; RESTORE STACK POINTER
016474 005027 000000          CLR      @0
016500 005367 177772          DEC      .-2
016504 001375          BNE      .-4
016506 104410          HLT                    ; POWER FAIL TRAP OCCURRED - CHECK
016510 012737 000026 000024      MOV      @26, @24      ; STACK TO SEE WHERE IT OCCURRED
016516 032777 000010 162312      BIT      @10, @SR
016524 001374          BNE      .-6
016526 022626          CMP      (SP)+, (SP)+
016530 000167 177370          JMP      SRMEX      ; RESTORE STACK POINTER

                                ; IF SWITCH REGISTER SWITCH 4 IS SET
                                ; CHECK PROCESSOR POWER FAIL WHEN THIS SIDE HAS SWITCH CONTROLLED BUT NOT
                                ; CONNECTED, AND OTHER CPU IS POWERED DOWN
016534 032777 000020 162274      SAMS:  BIT      @20, @SR      ; EXECUTE THIS SECTION IF SW 4 IS SET
016542 001512          BEQ      SRM6
016544 005327 000000          DEC      @0
                                ; STALL TO IGNORE SWITCH REGISTER BOUNCE
016550 001375          BNE      .-4
016552 012737 016660 000024      MOV      @RETM5A, @24
016560 005037 000026          CLR      @26
016564 012777 000002 162220      MOV      @2, @BUSCSR
016572 105777 162214          TSTB    @BUSCSR
016576 100375          BPL      .-4
016600 052777 002400 162204      BIS      @2400, @BUSCSR
                                ; REQUEST SWITCH TO GO TO CONTROLLED
                                ; BUT NOT CONNECTED POSITION
                                ; WAIT FOR "CONNECTED" BIT TO SET
                                ; ONCE SWITCH IS IN POSITION 2 (4)
                                ; SET BOTH INTERRUPT ENABLES
016606 022777 022602 162176      SRM5A: CMP      @22602, @BUSCSR
016614 001410          BEQ      SRM5B
016616 032767 000020 002246      BIT      @20, @FLAGS
016624 001004          BNE      SRM5B
016626 052767 000020 002236      BIS      @20, @FLAGS
016634 104410          HLT                    ; CSR INCORRECT DURING POWER FAIL
                                ; TEST
                                ; CONTINUE CHECKING UNTIL SWITCH
                                ; REGISTER IS CLEARED

016636 032777 000020 162172      SRM5B: BIT      @20, @SR
016644 001360          BNE      SRM5A
016646 012737 000026 000024      MOV      @26, @24
016654 000167 177244          JMP      SRMEX
016660 012737 016724 000024      RETM5A: MOV      @RETM5B, @24
016666 010667 162176          MOV      SP, SPSAV
016672 000000          HALT
016674 016706 162170          MOV      SPSAV, SP
016700 104410          HLT

016702 012737 000026 000024      MOV      @26, @24
016710 032777 000020 162120      BIT      @20, @SR
016716 001374          BNE      .-6

```

```

016720 000167 177200
016724 016706 162140
016730 005027 000000
016734 005367 177772
016740 001375
016742 104410
016744 012737 000026 000024
016752 032777 000020 162056
016760 001374
016762 022626
016764 000167 177134

RETMSB: JMP SRMEX
MOV SPSAV, SP ;RESTORE STACK POINTER
CLR #0 ;STALL SO THAT TTY OUTPUT WON'T
DEC #-2 ;BE GARBLED
BNE #-4
HLT ;POWER FAIL TRAP OCCURRED - CHECK
MOV #26, #24 ;STACK TO SEE WHERE IT OCCURRED
BIT #20, #SR
BNE #-6
CMP (SP)+, (SP)+ ;RESTORE STACK POINTER
JMP SRMEX

; IF SWITCH REGISTER SWITCH 5 IS SET
; CHECK PROCESSOR POWER FAIL WHEN THIS SIDE HAS THE SWITCH CONNECTED
; AND THE OTHER CPU IS POWERED DOWN
016770 032777 000040 162040 SRM6: BIT #40, #SR ;EXECUTE THIS SECTION IF SWS IS SET
REQ SRM7
DEC #0 ;STALL TO IGNORE SWITCH REGISTER BOUNCE
BNE #-4
MOV #RETM6A, #24
CLR #26
MOV #1, #BUSCSR ;REQUEST SWITCH
TSTB #BUSCSR ;WAIT FOR SWITCH TO CONNECT
BPL #-4
BIS #2400, #BUSCSR ;SET BOTH INTERRUPT ENABLES
SRM6A: CMP #22601, #BUSCSR ;CHECK CSR-POWER FAIL ON OTHER
REQ SRM6B ;PROCESSOR BUS SHOULDN'T AFFECT IT
BIT #40, #FLAGS ;PRINT ERROR ONLY ONCE
BNE SRM6B
BIS #40, #FLAGS
HLT ;CSR INCORRECT DURING TEST OF POWER FAIL
; ON THE OTHER PROCESSOR BUS
; CONTINUE CHECKING UNTIL SWITCH
; REGISTER IS CLEARED
017072 032777 000040 161736 SRM6B: BIT #40, #SR
BNE SRM6A
MOV #26, #24
JMP SRMEX
RETM6A: MOV #RETM6B, #24 ;SETUP POWER UP RETURN
MOV SP, SPSAV ;SAVE STACK POINTER
HALT ;POWER DOWN HALT (NO POWER FAIL
; SHOULD HAVE OCCURRED)
MOV SPSAV, SP ;POWER FAIL TRAP (DOWN ONLY)
; OCCURRED
; RESTORE TRAP CATCHER
017136 012737 000026 000024
017144 032777 000040 161664
017152 001374
017154 000167 176744
017160 016706 161704
017164 005027 000000
017170 005367 177772
017174 001375
017176 104410
017200 012737 000026 000024
017206 032777 000040 161622
017214 001374
017216 022626
017220 000167 176700

RETMSB: MOV SPSAV, SP ;RESTORE STACK POINTER
CLR #0 ;STALL SO THAT TTY OUTPUT WON'T
DEC #-2 ;BE GARBLED
BNE #-4
HLT ;POWER FAIL TRAP OCCURRED - CHECK
MOV #26, #24 ;STACK TO SEE WHERE IT OCCURRED
BIT #40, #SR
BNE #-6
CMP (SP)+, (SP)+ ;RESTORE STACK POINTER
JMP SRMEX

```

```

; IF SWITCH REGISTER SWITCH 6 IS SET
; SHOW THAT WHEN OTHER CPU IS POWERED DOWN AND HAD BUS SWITCH,
; THIS SIDE CAN GET THE SWITCH
017224 032777 000100 161604 SRM7: BIT #100,SR ;EXECUTE THIS SECTION IF SM6 IS SET
017232 001516 BEQ SRM8 ;STALL TO IGNORE SWITCH REGISTER BOUNCE
017234 005327 000000 DEC #0
017240 001375 BNE .-4
017242 012737 017360 000024 NOV #RETH7A,2#24
017250 005037 000026 CLR #26
017254 032777 020000 161530 BIT #20000,2BUSCSR ;WAIT FOR NON NEUTRAL (BIT 13) TO SET
017262 001774 BEQ .-6 ;INDICATING OTHER PROCESSOR HAS THE SWITCH
017264 012777 000001 161520 NOV #1,2BUSCSR ;REQUEST SWITCH-SHOULD CONNECT
017272 105777 161514 SRM7A: TSTB 2BUSCSR ;WHEN OTHER PROCESSOR IS POWERED
; DOWN
017276 100412 BMI SRM7B ;BRANCH IF NOW CONNECTED TO THIS SIDE
017300 032777 000100 161530 BIT #100,SR ;CHECK SWITCH REGISTER
017306 001371 BNE SRM7A ;LOOP IF NOT CLEARED
017310 104410 HLT ;CONNECTED BIT NEVER SET, ALTHOUGH
; SWITCH WAS REQUESTED AND OTHER
; PROCESSOR WAS POWERED DOWN
017312 012737 000026 000024 NOV #26,2#24
017320 000167 176500 JMP SRMEX
017324 032777 040000 161460 SRM7B: BIT #40000,2BUSCSR ;CHECK BIT 14 - SHOULDN'T
017332 001401 BEQ .+4 ;BE SET
017334 104410 HLT ;BIT 14 SET IN CSR AFTER
; OTHER PROCESSOR WAS POWERED DOWN
017336 032777 000100 161472 BIT #100,SR ;WAIT FOR OPERATOR TO CLEAR SWITCH REGISTER
017344 001374 BNE .-6 ;INDICATING END OF TEST
017346 012737 000026 000024 NOV #26,2#24
017354 000167 176544 JMP SRMEX
017360 012737 017424 000024 RETH7A: NOV #RETH7B,2#24 ;SETUP POWER UP RETURN
017366 010667 161476 NOV SP,SPSAV ;SAVE STACK POINTER
017372 000000 HALT ;POWER DOWN HALT (NO POWER FAIL
; SHOULD HAVE OCCURRED)
017374 016706 161470 NOV SPSAV,SP ;POWER FAIL TRAP (DOWN ONLY)
017400 104410 HLT ;OCCURRED
; RESTORE TRAP CATCHER
017402 012737 000026 000024 NOV #26,2#24
017410 032777 000100 161420 BIT #100,SR
017416 001374 BNE .-6
017420 000167 176500 JMP SRMEX
017424 016706 161440 RETH7B: NOV SPSAV,SP ;RESTORE STACK POINTER
017430 005027 000000 CLR #0 ;STALL SO THAT TTY OUTPUT WON'T
017434 005327 177772 DEC .-2 ;BE GARGLED
017440 001375 BNE .-4
017442 104410 HLT
017444 012737 000026 000024 NOV #26,2#24 ;POWER FAIL TRAP OCCURRED - CHECK
017452 032777 000100 161356 BIT #100,SR ;STACK TO SEE WHERE IT OCCURRED
017460 001374 BNE .-6
017462 022626 CMP (SP)+,(SP)+ ;RESTORE STACK POINTER
017464 000167 176434 JMP SRMEX

; IF SWITCH REGISTER SWITCH 7 IS SET, EXECUTE THIS ROUTINE
; POWER FAIL TEST RUN WHEN THE SWITCH IS POWERED DOWN
017470 032777 000200 161340 SRM8: BIT #200,SR ;EXECUTE THIS SECTION IF SW7 IS SET
017476 001477 BEQ SRM9

```

```

017500 012737 017544 000024      MOV      #SRET8,2#24      ;SET UP POWER FAIL TRAP RETURN
017506 005037 000026      CLR      2#26            ;STALL TO IGNORE SWITCH REGISTER BOUNCE
017512 005327 000000      DEC      #0              ;STALL TO IGNORE SWITCH REGISTER BOUNCE
017516 001375      BNE     .-4              ;STALL TO IGNORE SWITCH REGISTER BOUNCE
017520 032777 000200 161310      BIT      #200,2SR       ;WAIT FOR SWITCH REGISTER TO BE CLEARED
017526 001374      BNE     .-6              ;POWER FAIL TRAP SHOULD OCCUR FIRST
017530 104410      HLT                               ;NO POWER FAIL TRAP ON SWITCH POWERING DOWN OR UP
017532 012737 000026 000024      MOV      #26,2#24       ;RESTORE TRAP CATCHER IN POWER FAIL TRAP
017540 000167 176360      JMP      SRMEX           ;LOCATION
017544 012737 017604 000024      SRET8:  MOV      #SRET8A,2#24 ;SET UP POWER UP RETURN
017552 017767 161234 161312      MOV      #BUSCSR,PFSAV ;STORE CURRENT CSR CONTENTS
017560 010667 161304      MOV      SP,SPSAV       ;SAVE STACK POINTER
017564 032767 040000 161300      BIT      #40000,PFSAV   ;CHECK FOR AC LO
017572 001767      BEQ     SRET8+6         ;IF NOT SET, GO BACK TO REREAD CSR
017574 000000      HLT                               ;POWER DOWN HALT
017576 016706 161266      MOV      SPSAV,SP
017602 104410      HLT                               ;NO POWER UP RESTART AFTER POWER DOWN
017604 016706 161260      SRET8A: MOV      SPSAV,SP ;RESTORE STACK POINTER ON POWER UP
017610 022626      CMP     (SP)+,(SP)+
017612 005027 000000      CLR      #0              ;STALL SO THAT TTY OUTPUT WILL BE OK
017616 005367 177772      DEC     .-2
017622 001375      BNE     .-4
017624 042767 020000 161240      BIC     #20000,PFSAV   ;CLEAR NOT NEUTRAL BIT IN SAVED CSR CONTENTS
017632 022767 040000 161232      CMP     #40000,PFSAV   ;CHECK CONTENTS OF CSR SAVED WHEN
017640 001401      BEQ     .+4              ;POWER DOWN OCCURRED (EXCEPT FOR NOT NEUTRAL)
017642 104410      HLT                               ;CSR INCORRECT AT POWER DOWN - ONLY BIT 14
;AND POSSIBLY 13 SHOULD HAVE BEEN SET - SEE
;ACTUAL VALUE SAVED IN PFSAV (NOTE THAT
;NOT NEUTRAL HAS BEEN CLEARED SINCE IT MAY
;HAVE BEEN SET OR CLEAR DEPENDING ON THE
;POSITION THE SWITCH WAS IN)
017644 005777 161142      TST     #BUSCSR         ;CSR SHOULD BE CLEARED ON POWER UP
017650 001401      BEQ     .+4
017652 104410      HLT
;CSR NOT CLEAR (ZERO) AFTER SWITCH
;POWERED DOWN AND BACK UP
017654 012737 000026 000024      MOV      #26,2#24       ;RESTORE TRAP CATCHER IN POWER FAIL
017662 032777 000200 161146      BIT      #200,2SR       ;TRAP LOCATION
017670 001374      BNE     .-6              ;WAIT FOR SWITCH 7 TO BE CLEARED
017672 000167 176226      JMP      SRMEX

;IF SWITCH REGISTER SWITCH 8 IS SET, EXECUTE THIS ROUTINE
;POWER FAIL TEST RUN WHEN A SWITCHED BUS DEVICE IS POWERED DOWN
017676 032777 000400 161132      SRM9:  BIT      #400,2SR   ;EXECUTE THIS SECTION IF S#8 IS SET
017704 001562      BEQ     SRM10
017706 005327 000000      DEC      #0              ;STALL TO IGNORE SWITCH REGISTER BOUNCE
017712 001375      BNE     .-4              ;STALL TO IGNORE SWITCH REGISTER BOUNCE
017714 012737 020142 000024      MOV      #SRET#9A,2#24 ;SETUP POWER FAIL RETURN IN CASE
017722 005037 000026      CLR      2#26
017726 032777 040000 161056      BIT      #40000,2BUSCSR ;CK BIT 14 - SHOULDN'T BE SET YET
017734 001401      BEQ     .+4
017736 104410      HLT
017740 032777 040000 161044      SRM9A: BIT      #40000,2BUSCSR ;BIT 14 SET BEFORE POWER DOWN OCCURRED
;WAIT FOR 14 TO SET OR SWITCH REGISTER
;TO BE CLEARED (NO POWER FAIL TRAP SHOULD OCCUR)
017746 001012      BNE     SRM9B           ;IF AC LO IS SET, BRANCH OUT
017750 032777 000400 161060      BIT      #400,2SR

```

017756	001370			BNE	SRM9A	
017760	104410			HLT		:BIT 14 NEVER SET DURING POWER
017762	012737	000026	000024	MOV	#26, @#24	:DOWN AND UP OF A SWITCHED BUS DEVICE
017770	000167	176130		JMP	SRMEX	
017774	032777	020000	161010	SRM9B: BIT	#20000, @BUSCSR	:WAIT FOR SWITCH TO DISCONNECT DUE TO
020002	001374			BNE	.-6	:DC LO
020004	005327	000000		DEC	#0	:STALL IN CASE DC LO WAS GENERATED BY CPU
020010	001375			BNE	.-4	:AND NOT YET ON SB
020012	012777	000001	160772	MOV	#1, @BUSCSR	:REQUEST SWITCH AFTER SWITCHED BUS DEVICE HAS
						:BEEN POWERED DOWN-SHOULDN'T CONNECT
020020	005327	000000		DEC	#0	:STALL
020024	001375			BNE	.-4	
020026	105777	160760		TSTB	@BUSCSR	:CHECK CONNECTED BIT
020032	100001			BPL	.-4	
020034	104410			HLT		:SWITCH CONNECTED TO THIS PROCESSOR
						:AFTER POWER DOWN OF SB DEVICE
020036	105077	160750		CLRB	@BUSCSR	:CLEAR REQUEST
020042	032777	001000	160742	BIT	#1000, @BUSCSR	:WAIT FOR SB INIT TO COMPLETE
020050	001374			BNE	.-6	
020052	032777	010000	160732	SRM9C1: BIT	#10000, @BUSCSR	:WAIT FOR THE OTHER SIDE TO SET COM1 BIT
020060	001005			BNE	SRM9C	:FALL THRU WHEN SET
020062	032777	000400	160746	BIT	#400, @SR	:WAIT FOR OPERATOR TO CLEAR SWITCH REGISTER
020070	001370			BNE	SRM9C1	
020072	104410			HLT		:OTHER SIDE SET COM1 BIT AFTER THE SWITCHED BUS
						:DEVICE WAS POWERED DOWN, BUT COM2 WAS NEVER SET ON
						:THIS SIDE
020074	032777	040000	160710	SRM9C: BIT	#40000, @BUSCSR	:WAIT FOR AC LO TO CLEAR WHEN DEVICE
020102	001406			BEQ	SRM9D	:ON SWITCHED BUS IS POWERED BACK UP
020104	032777	000400	160724	BIT	#400, @SR	:IF NOT CLEAR CHECK SWITCH REGISTER
020112	001370			BNE	SRM9C	:LOOP IF OPERATOR HASN'T CLEARED IT YET
020114	104410			HLT		:BIT 14 DIDN'T CLEAR WHEN THE
020116	000404			BR	.-12	:SWITCHED BUS DEVICE WAS POWERED
						:BACK UP
020120	032777	000400	160710	SRM9D: BIT	#400, @SR	
020126	001374			BNE	.-6	
020130	012737	000026	000024	MOV	#26, @#24	:RESTORE TRAP CATCHER
020136	000167	175762		JMP	SRMEX	:RETURN TO SWITCH MONITOR
020142	012737	020206	000024	RETM9A: MOV	#RETM9B, @#24	:SETUP POWER UP RETURN
020150	010667	160714		MOV	SP, SPSAV	:SAVE STACK POINTER
020154	000000			HALT		:POWER DOWN HALT (NO POWER FAIL
020156	016706	160706		MOV	SPSAV, SP	:SHOULD HAVE OCCURRED)
020162	104410			HLT		:POWER FAIL TRAP (DOWN ONLY)
						:OCCURRED
020164	012737	000026	000024	MOV	#26, @#24	:RESTORE TRAP CATCHER
020172	032777	000400	160636	BIT	#400, @SR	
020200	001374			BNE	.-6	
020202	000167	175716		JMP	SRMEX	
020206	016706	160656		RETM9B: MOV	SPSAV, SP	:RESTORE STACK POINTER
020212	005027	000000		CLR	#0	:STALL SO THAT TTY OUTPUT WON'T
020216	005367	177772		DEC	.-2	:BE GARBLED
020222	001375			BNE	.-4	
020224	104410			HLT		:POWER FAIL TRAP OCCURRED - CHECK
020226	012737	000026	000024	MOV	#26, @#24	:STACK TO SEE WHERE IT OCCURRED
020234	032777	000400	160574	BIT	#400, @SR	
020242	001374			BNE	.-6	
020244	022626			CHP	(SP)+, (SP)+	:RESTORE STACK POINTER

```

020246 000167 175652          JMP      SRMEX
                                ; IF SWITCH REGISTER SWITCH 9 IS SET, EXECUTE THIS ROUTINE
                                ; POWER FAIL TEST RUN WHEN OTHER CPU IS POWERED DOWN
                                ; AND THE SWITCH WAS IN NEUTRAL
020252 032777 001000 160556 SRM10: BIT      #1000,SR      ; EXECUTE THIS SECTION IF SW9 IS SET
020254 001512                BEQ      SRM11
020256 005327 000000                DEC      #0          ; STALL TO IGNORE SWITCH REGISTER BOUNCE
020266 001375                BNE      #-4
020270 012737 020376 000024        MOV      RETMOA,SR24
020276 005037 000026                CLR      SR26
020302 012777 000001 160502        MOV      SR1,SRBUSCSR ; REQUEST SWITCH - SHOULD CONNECT IMMEDIATELY
020310 105777 160476                TSTB    SRBUSCSR    ; SINCE OTHER PROCESSOR HAS ALREADY BEEN
                                ; POWERED DOWN
020314 100412                BMI      SRM10B
020316 104410                HLT
                                ; CONNECTED BIT NOT SET, ALTHOUGH
                                ; THE SWITCH WAS REQUESTED AND THE OTHER
                                ; PROCESSOR WAS POWERED DOWN
020320 012737 000026 000024        MOV      SR26,SR24
020326 032777 001000 160502        BIT      #1000,SR
020334 001374                BNE      #-6
020336 000167 175562                JMP      SRMEX
020342 032777 140000 160442 SRM10B: BIT    #140000,SRBUSCSR ; CHECK BITS 14 AND 15 - SHOULDN'T
020350 001401                BEQ      +4          ; BE SET
020352 104410                HLT
                                ; BIT 14 AND/OR 15 SET IN CSR AFTER
                                ; OTHER PROCESSOR WAS POWERED DOWN
                                ; WAIT FOR OPERATOR TO CLEAR SR
                                ; INDICATING END OF TEST
020354 032777 001000 160454        BIT      #1000,SR
020362 001374                BNE      #-6
020364 012737 000026 000024        MOV      SR26,SR24
020372 000167 175526                JMP      SRMEX
020376 012737 020442 000024 RETMOA: MOV    RETMOB,SR24 ; SETUP POWER UP RETURN
020404 010667 160460                MOV      SP,SPSAV ; SAVE STACK POINTER
020410 000000                HALT
020412 016706 160452                MOV      SPSAV,SP ; POWER DOWN HALT (NO POWER FAIL
                                ; SHOULD HAVE OCCURRED)
020416 104410                HLT                ; POWER FAIL TRAP (DOWN ONLY)
                                ; OCCURRED
                                ; RESTORE TRAP CATCHER
020420 012737 000026 000024        MOV      SR26,SR24
020426 032777 001000 160402        BIT      #1000,SR
020434 001374                BNE      #-6
020436 000167 175462                JMP      SRMEX
020442 016706 160422                RETMOB: MOV   SPSAV,SP ; RESTORE STACK POINTER
020446 005027 000000                CLR      #0          ; STALL SO THAT TTY OUTPUT WON'T
020452 005367 177772                DEC      #-2        ; BE GARBLED
020456 001375                BNE      +4
020460 104410                HLT
020462 012737 000026 000024        MOV      SR26,SR24 ; POWER FAIL TRAP OCCURRED - CHECK
020470 032777 001000 160340        BIT      #1000,SR    ; STACK TO SEE WHERE IT OCCURRED
020476 001374                BNE      #-6
020500 022626                CMP      (SP)+,(SP)+ ; RESTORE STACK POINTER
020502 000167 175416                JMP      SRMEX

```

```

; IF SWITCH REGISTER SWITCH 10 IS SET, EXECUTE THIS ROUTINE
; TEST THAT NO INIT OCCURS ON THE
; SWITCHED BUS IF THIS PROCESSOR HAS THE SWITCH
; IN THE CONTROLLED BUT NOT CONNECTED POSITION (2 OR 4)
; AND BIT 9 IS SET IN THE CSR ON THE OTHER SIDE

```

```

020506 032777 002000 160322 SRM11: BIT #2000,SR ;EXECUTE THIS SECTION IF SW10 IS SET
020514 001455 BEQ SRM12
020516 005327 000000 SRM11A: DEC #0 ;STALL TO IGNORE SWITCH REGISTER BOUNCE
020522 001375 BNE .-4
020524 012777 000001 160260 MOV #1,SBUSCSR ;REQUEST SWITCH
020532 105777 160254 TSTB SBUSCSR ;WAIT FOR CONNECTED TO SET
020536 100375 BPL .-4
020540 016777 160316 160306 MOV ANDBTS,SDVADRS ;SET UP LOCATION ON SWITCHED BUS
020546 017701 160302 MOV SDVADRS,R1 ;READ BACK SAME TO VALIDATE
020552 046701 160306 BIC ANDCOM,R1 ;BEFORE EXECUTING TEST
020556 026701 160300 CMP ANDBTS,R1
020562 001401 BEQ .+4
020564 104410 HLT
020566 012777 000002 160216 MOV #2,SBUSCSR ;LOCATION ON SWITCHED BUS DID NOT LOAD CORRECTLY
;PUT SWITCH IN CONTROLLED BUT
;NOT CONNECTED POSITION
;WAIT FOR SWITCH REGISTER TO CLEAR
020574 005777 160236 TST SR
020600 001375 BNE .-4
020602 012777 000001 160202 MOV #1,SBUSCSR ;CONNECT THE SWITCH
020610 017701 160240 MOV SDVADRS,R1 ;READ CONTENTS OF LOCATION ON SWITCHED BUS
020614 046701 160244 BIC ANDCOM,R1 ;MASK OFF BITS NOT SET
020620 026701 160236 CMP ANDBTS,R1 ;CHECK BITS IN THE DEVICE REGISTER
020624 001401 BEQ .+4
020626 104410 HLT ;BITS IN LOCATION ON SWITCHED BUS
;INCORRECT AFTER BIT 9 WAS SET
020630 005077 160156 CLR SBUSCSR
020634 032777 001000 160150 BIT #1000,SBUSCSR
020642 001374 BNE .-6
020644 000167 175254 JMP SRMEX ;IN OTHER PROCESSOR'S CSR

;IF SWITCH REGISTER SWITCH 11 IS SET, EXECUTE THIS ROUTINE
;TEST THAT NO INIT OCCURS ON THE
;SWITCHED BUS IF THIS PROCESSOR HAS THE SWITCH IN
;THE CONNECTED POSITION (1 OR 5) AND BIT 9 IS
;SET IN THE CSR ON THE OTHER SIDE
020650 032777 004000 160160 SRM12: BIT #4000,SR ;EXECUTE THIS SECTION IF SW11 IS SET
020656 001450 BEQ SRM13
020660 005327 000000 DEC #0 ;STALL TO IGNORE SWITCH REGISTER BOUNCE
020664 001375 BNE .-4
020666 012777 000001 160116 MOV #1,SBUSCSR ;REQUEST SWITCH
020674 105777 160112 TSTB SBUSCSR ;WAIT FOR CONNECTED TO SET
020700 100375 BPL .-4
020702 016777 160154 160144 MOV ANDBTS,SDVADRS ;SET UP LOCATION ON SWITCHED BUS
020710 017701 160140 MOV SDVADRS,R1 ;CHECK LOCATION BEFORE TESTING
020714 046701 160144 BIC ANDCOM,R1
020720 026701 160136 CMP ANDBTS,R1
020724 001401 BEQ .+4
020726 104410 HLT ;SWITCHED BUS LOCATION DIDN'T LOAD CORRECTLY
020730 032777 004000 160100 BIT #4000,SR ;WAIT FOR SWITCH REGISTER TO CLEAR
020736 001374 BNE .-6
020740 017701 160110 MOV SDVADRS,R1 ;CHECK CONTENTS OF THE SWITCHED BUS LOCATION
020744 046701 160114 BIC ANDCOM,R1
020750 026701 160106 CMP ANDBTS,R1
020754 001401 BEQ .+4
020756 104410 HLT ;BITS IN LOCATION ON SWITCHED BUS
;INCORRECT AFTER BIT 9 WAS SET
020760 005077 160026 CLR SBUSCSR

```

```

020764 032777 001000 160020      BIT      #1000, @BUSCSR ;WAIT FOR SB INIT TO COMPLETE
020772 001374      BNE      -6
020774 000167 175124      JMP      SRMEX

;IF SWITCH REGISTER SWITCH 12 IS SET, EXECUTE THIS ROUTINE
;SET COMMUNICATION BIT IF ANY ERRORS OCCURRED ON THIS SIDE
021000 032777 010000 160030 SRM13: BIT      #10000, @SR
021006 001417      BEQ      SRM14
021010 005767 000716      TST      ERR
021014 100003      BPL      +10
021016 052777 004000 157766      BIS      #4000, @BUSCSR ;BRANCH IF NO ERRORS OCCURRED
;SET COMMUNICATION BIT IF ANY
;ERRORS OCCURRED
;STALL TO IGNORE SWITCH REGISTER BOUNCE
021024 005327 000000      DEC      #0
021030 001375      BNE      -4
021032 032777 010000 157776      BIT      #10000, @SR
021040 001374      BNE      -6
021042 000167 175056      JMP      SRMEX

```

```

;IF SWITCH REGISTER SWITCH 13 IS SET, EXECUTE THIS ROUTINE
021046 032777 020000 157762 SRM14: BIT      #20000, @SR
021054 001404      BEQ      SRM15
021056 005067 000650      CLR      ERR ;INITIALIZE ERROR FLAG
021062 000167 177430      JMP      SRM11A
021066 000167 175040      SRM15: JMP      SRMON
021072 000000      FLAGS: 0

```

```

;INPUT OF INFORMATION NECESSARY TO TEST THE SWITCH
;AN ADDRESS OF SOMETHING OUT ON THE SWITCHED BUS MUST BE GIVEN TO RUN
;SOME OF THE TESTS. IF ANY NPR DEVICES ARE ON THE SWITCHED BUS, THE
;ADDRESS OF ONE OF THE WORD COUNT OR BUS ADDRESS REGISTERS SHOULD BE GIVEN.
;SPECIFICALLY, THE PROGRAM NEEDS THE ADDRESS OF A LOCATION WHICH HAS AT LEAST 1
;BIT WHICH IS READ/WRITE AND IS CLEARED BY INIT. IF NO SUCH LOCATION
;EXISTS ON THE SWITCHED BUS, THEN THE BEST YOU CAN DO IS GIVE THE ADDRESS OF
;A LOCATION WHICH IS READ/WRITE ON THE SWITCHED BUS, SUCH AS A MEMORY
;LOCATION. IN THIS CASE, INIT ON THE SWITCHED BUS WILL NOT BE TESTED.
021074 104022      INFORM: PMSG9
021076 000000      HALT

```

```

021100 017767 157732 157746      MOV      @SR, DVADRS
021106 104024      PMSG10
021110 000000      HALT

```

```

021112 017767 157720 157736      MOV      @SR, RWBITS
021120 104060      PMSG24
021122 000000      HALT

```

```

021124 017767 157706 157726      MOV      @SR, INBITS

```

```

; "SET THE ADDRESS OF THE WORD COUNT
; REGISTER OR BUS ADDRESS REGISTER OF AN
; NPR DEVICE WHICH IS ON THE
; SWITCHED BUS IN THE SWITCH REGISTER SWITCHES.
; SEE SECTION 9 OF THE DOCUMENT
; FOR THE CONDITIONS THAT THIS
; ADDRESS MUST SATISFY. THEN PRESS
; 'CONTINUE' ON THIS PROCESSOR."
; SAVE THE DEVICE ADDRESS
; "SET THE SWITCH REGISTER SWITCHES
; CORRESPONDING TO THE BITS IN THAT
; ADDRESS THAT ARE READ/WRITE.
; THEN PRESS 'CONTINUE' ON THIS
; PROCESSOR."
; SAVE RW LOCATION INFORMATION
; "SET THE SWITCH REGISTER SWITCHES
; CORRESPONDING TO THE BITS IN THAT
; ADDRESS THAT ARE CLEARED BY
; INIT. THEN PRESS 'CONTINUE' ON
; THIS PROCESSOR."
; SAVE INFORMATION

```



```

021132 016767 157720 157722 MOV RMBITS,ANDBTS ;SETUP TO FIND WHICH BITS ARE BOTH
021140 005167 157714 COM INBITS ;RW AND CLEARED BY INIT
021144 046767 157710 157710 BVC INBITS,ANDBTS ;ANDBTS IS NOW THE LOGICAL AND
021152 005167 157702 COM INBITS ;OF INBITS AND RMBITS
021156 016767 157700 157700 MOV ANDBTS,ANDCOM
021164 005167 157674 COM ANDCOM ;SETUP COMPLEMENT TO MASK OFF REST
021170 104026 PMSG11 ;"RESTORE THE SWITCH REGISTER TO DYNAMIC SWITCH SETTINGS
021172 000000 HALT ;THEN PRESS CONTINUE ON THIS PROCESSOR"
021174 000207 RTS x7

```

```

;ROUTINE TO ALLOW SCOPING OF ONE-SHOT DELAYS FOR SETTING
;TIMEOUT TIMER AND SWITCHED BUS INIT TIMER
;BOTH PROCESSORS MUST RUN THE ROUTINE AT THE SAME TIME, AND THE BUS SWITCH
;SHOULD HAVE THE "INIT-INHIBIT INIT" SWITCH SET TO THE "INIT" POSITION

```

```

021176 012777 021224 157612 TIMERS: MOV #TIMRET,ABSIV1 ;SETUP "SWITCH CONNECTED"
021204 005077 157610 CLR ABSST1 ;INTERRUPT RETURN
021210 005077 157620 CLR APSR ;SET PROCESSOR STATUS TO 0
021214 012777 000401 157570 TIMREQ: MOV #401,ABUSCSR ;REQUEST SWITCH AND SET INTERRUPT
;ENABLE 1
021222 000001 WAIT ;UNTIL SWITCH CONNECTS NO
;MASTER SYNCs WILL OCCUR
021224 022626 TIMRET: CMP (SP)+,(SP)+ ;WHEN SWITCH CONNECTS,RESTORE
;STACK POINTER
021226 105777 157560 TSTB ABUSCSR ;CHECK CONNECTED BIT-SWITCH WILL
021232 100775 BMI -4 ;SWITCH DUE TO TIME OUT, AND
;SWITCHED BUS INIT WILL OCCUR
;WHEN IT SWITCHES
021234 000767 BR TIMREQ ;LOOP TO REQUEST SWITCH AGAIN

```

;ENT HANDLER

```

021236 011667 001106 EMTSRV: MOV @SP, TYTMP ;GET CALL
021242 162767 000002 001100 SUB #2, TYTMP
021250 017767 001074 001072 MOV @TYTMP, TYTMP
021256 105067 001067 CLRB TYTMP+1 ;SAVE OFFSET ONLY
021262 062767 021304 001060 ADD @ENTAB, TYTMP
021270 017767 001054 001052 MOV @TYTMP, TYTMP ;SETUP MESSAGE ADDRESS
021276 004767 JSR %7, TYPE ;TYPE MESSAGE
021302 000002 RTI ;RETURN
021304 000000 ENTAB: 0
021306 025074 MSG1
021310 025100 MSG2
021312 025110 MSG3
021314 025120 MSG4
021316 025130 MSG5
021320 025136 MSG6
021322 025152 MSG7
021324 025166 MSG8
021326 025174 MSG9
021330 025202 MSG10
021332 025212 MSG11
021334 025220 MSG12
021336 025230 MSG13
021340 025240 MSG14
021342 025250 MSG15
021344 025260 MSG16
021346 025270 MSG17

```

021350 025300  
021352 025310  
021354 025320  
021356 025330  
021360 025336  
021362 025354  
021364 025362  
021366 025372  
021370 025376  
021372 025404  
021374 025410  
021376 025420  
021400 025430  
021402 025434  
021404 025440  
021406 025444  
021410 025450  
021412 025456  
021414 025466  
021416 025476  
021420 025506  
021422 025516  
021424 025526  
021426 025536  
021430 025556

MSG18  
MSG19  
MSG20  
MSG21  
MSG22  
MSG23  
MSG24  
MSG25  
MSG26  
MSG27  
MSG28  
MSG29  
MSG30  
MSG31  
MSG32  
MSG33  
MSG34  
MSG35  
MSG36  
MSG37  
MSG38  
MSG39  
MSG40  
MSG41  
MSG42

104002  
104004  
104006  
104010  
104012  
104014  
104016  
104020  
104022  
104024  
104026  
104030  
104032  
104034  
104036  
104040  
104042  
104044  
104046  
104050  
104052  
104054  
104056  
104060  
104062  
104064  
104066  
104070  
104072  
104074

PMSG1=EMT+2  
PMSG2=EMT+4  
PMSG3=EMT+6  
PMSG4=EMT+10  
PMSG5=EMT+12  
PMSG6=EMT+14  
PMSG7=EMT+16  
PMSG8=EMT+20  
PMSG9=EMT+22  
PMSG10=EMT+24  
PMSG11=EMT+26  
PMSG12=EMT+30  
PMSG13=EMT+32  
PMSG14=EMT+34  
PMSG15=EMT+36  
PMSG16=EMT+40  
PMSG17=EMT+42  
PMSG18=EMT+44  
PMSG19=EMT+46  
PMSG20=EMT+50  
PMSG21=EMT+52  
PMSG22=EMT+54  
PMSG23=EMT+56  
PMSG24=EMT+60  
PMSG25=EMT+62  
PMSG26=EMT+64  
PMSG27=EMT+66  
PMSG28=EMT+70  
PMSG29=EMT+72  
PMSG30=EMT+74

104076  
104100  
104102  
104104  
104106  
104110  
104112  
104114  
104116  
104120  
104122  
104124

PHSG31=EMT+76  
PHSG32=EMT+100  
PHSG33=EMT+102  
PHSG34=EMT+104  
PHSG35=EMT+106  
PHSG36=EMT+110  
PHSG37=EMT+112  
PHSG38=EMT+114  
PHSG39=EMT+116  
PHSG40=EMT+120  
PHSG41=EMT+122  
PHSG42=EMT+124

021432 011667 000032  
021436 162767 000002 000024  
021444 017767 000020 000016  
021452 105067 000013  
021456 062767 021472 000004  
021464 017707 000000  
021470 000000  
104400  
104402  
104404  
104406  
104410  
021472 000000  
021474 000000  
021476 000000  
021500 022224  
021502 021570

:TRAP HANDLER  
:DECODES SCOPE AND HLT CALLS  
:FIRST 3 CALLS LEFT OPEN FOR EASY PATCHES  
TRPSRV: MOV @SP,TPC ;GET CALL  
SUB @2,TPC  
MOV @TPC,TPC  
CLR@ TPC+1 ;SAVE OFFSET ONLY  
ADD @TPTAB,TPC  
MOV @TPC,PC ;GO TO ROUTINE CALLED  
TPC: 0  
PATCH1=TRAP  
PATCH2=TRAP+2  
PATCH3=TRAP+4  
SCOPE=TRAP+6  
HLT=TRAP+10  
TPTAB: 0  
0  
0  
SCOPEC  
PRINT

021504 005077 157324  
021510 000000  
021512 017767 157320 000602  
021520 062767 000002 000574  
021526 000000  
021530 012767 177777 157350  
021536 032777 010000 157272  
021544 001404  
021546 042777 000020 157260  
021554 000403  
021556 062777 000020 157250  
021564 000177 000532

:ROUTINE TO LOOP THRU A SINGLE INSTRUCTION TEST  
:LOAD THE STARTING ADDRESS OF THE TEST  
:YOU WISH TO RUN (THE ADDRESS OF THE TESTXX  
:TAG) AT THE 1ST HALT, SET SWITCH REGISTER  
:OPTIONS AT THE 2ND HALT.  
:NOTE THAT SW11 MUST BE DOWN AFTER THE 2ND HALT  
TESTX: CLR @PSR  
HALT ;WAIT FOR STARTING ADDRESS  
MOV @SR,RETURN ;LOAD STARTING ADDRESS IN RETURN  
ADD @2,RETURN ;ADD 2 TO POINT TO INSTRUCTION AFTER  
HALT ;SET SR OPTIONS  
MOV @-1,TESTX ;SET FLAG  
BIT @10000,@SR ;CHECK SW12  
BEQ .+12 ;BRANCH IF NOT SET  
BIC @20,@PSR ;CLEAR TRACE BIT  
BR .+10 ;SKIP NEXT INSTRUCTION  
BIS @20,@PSR ;SET TRACE BIT  
JMP @RETURN ;JUMP TO TEST

:ENTERED WITH SYSTEM TRAP CALL (HLT)  
:PRINT OUT THE ERROR PC+2 AND STATUS REGISTER

```

: (USES REGISTERS)
021570 012767 177777 000134 PRINT: MOV      8-1,ERR      ; SET FLAG INDICATING ERROR OCCURRED
021576 037727 157234 020000 BIT        JSR, 820000  ; TEST FOR INHIBIT PRINT OUT
021604 001404 BEQ        +12       ; BRANCH TO PRINT
021606 037727 157224 040000 BIT        JSR, 840000  ; ONLY INHIBIT IF SCOPE LOOP WAS REQUESTED
021614 001034 BNE        CK       ; INHIBIT, CHECK FOR HALT
021616 012667 000104 MOV        (6)+,SAVPC  ; PC OF FAILING ROUTINE
021622 012667 000102 MOV        (6)+,SAVPSR ; PSR OF ERROR CONDITION
021626 024646 CMP        -(6),-(6) ; RESTORE STACK
021630 012777 000200 157176 MOV        8200,3PSR
021636 004767 000330 JSR        X7,CALF    ; OUTPUT CARRIAGE RETURN AND LINE FEED
021642 010267 000052 MOV        X2,SAVR2   ; SAVE R2
021646 016702 000054 MOV        SAVPC,X2   ; LOAD REGISTER WITH FAILING PC+2
021652 004767 000106 JSR        X7,PROCT   ; PRINT FAILING PC+2
021656 105777 157144 TSTB       3TCSR      ; WAIT FOR TTY READY
021662 100375 BPL        .-4
021664 012777 000240 157136 MOV        8240,3TDBR ; OUTPUT A SPACE
021672 016702 000032 MOV        SAVPSR,X2 ; LOAD PROCESSOR STATUS
021676 004767 000062 JSR        X7,PROCT   ; PRINT PROCESSOR STATUS
021702 016702 000012 MOV        SAVR2,X2  ; RESTORE REGISTER
021706 005777 157124 CK: TST       3SR      ; CHECK SR FOR HALT SWITCH
021712 100001 BPL        .+4       ; BRANCH IF NOT SET
021714 000000 HALT
021716 000002 RTI
021720 000000 SAVR2: 0
021722 000000 SAVR3: 0
021724 000000 SAVR4: 0
021726 000000 SAVPC: 0
021730 000000 SAVPSR: 0
021732 000000 ERR: 0

: SUBROUTINE TO PRINT OUT OCTAL NUMBER
: PRSHRT DELETES LEADING ZEROS
: PROCT PRINTS OUT 6 OCTAL DIGITS
: BOTH USE REGISTERS
021734 012767 000001 000206 PRSHRT: MOV      81,PRFLG  ; SET FLAG TO INDICATE SHORT PRINTOUT
021742 005702 TST       R2        ; CHECK FOR ZERO
021744 001011 BNE        PROCT+4   ; BRANCH IF NOT ZERO
021746 105777 157054 TSTB       3TCSR      ; WAIT FOR TTY READY
021752 100375 BPL        .-4
021754 012777 000260 157046 MOV        8260,3TDBR ; OUTPUT A SINGLE ZERO
021762 000207 RTS        X7        ; RETURN
021764 005067 000160 PROCT: CLR      PRFLG  ; CLEAR FLAG TO INDICATE FULL PRINTOUT
021770 010367 177726 MOV        R3,SAVR3  ; SAVE REGISTERS
021774 010467 177724 MOV        X4,SAVR4
022000 005004 CLR        X4        ; CLEAR R4 FOR COUNTING CHARACTERS OUTPUT
022002 005067 000144 CLR        PRFLG    ; INITIALIZE CARRY FLAG FOR ROTATES
022006 012703 000260 MOV        8260,X3  ; SETUP R3
022012 005702 TST       X2        ; CHECK BIT 15 OF NUMBER
022014 100001 BPL        .+4       ; BRANCH IF ZERO
022016 005203 INC        X3        ; INCREMENT R3 IF ONE
022020 006102 ROL        X2        ; ROTATE LEFT MOST OCTAL TO RIGHT END
022022 006102 ROL        X2
022024 005567 000122 ROC        PRFLG    ; STORE CARRY
022030 005767 000114 P.CK: TST      PRFLG  ; CHECK FOR SHORT PRINTOUT
022034 001403 BEQ        P.WAIT   ; BRANCH IF NOT SET

```

```

022036 020327 000260          CMP      X3, #260          ;CHECK FOR ZERO IF SET
022042 001407          BEQ      P.CONT          ;IF SET, GO TO NEXT CHARACTER

022044 105777 156756          P.WAIT: TSTB     @TCSR          ;WAIT FOR TTY READY
022050 100375          BPL      P.WAIT
022052 010377 156752          MOV      X3, @TDBR          ;OUTPUT NEXT CHARACTER
022054 005067 000066          CLR      PRSFLG          ;PRINT REST OF NUMBER AFTER A NON-ZERO DIGIT
022062 005264          P.CONT: INC      X4          ;COUNT
022064 020427 000006          CMP      X4, #6          ;CHECK FOR DONE
022070 001005          BNE      P.CNT1          ;BRANCH IF NOT DONE
022072 016703 177624          MOV      SAVR3, R3          ;RESTORE REGISTERS
022076 016704 177622          MOV      SAVR4, X4
022102 000207          RTS
022104 000241          P.CNT1: CLC          ;CLEAR CARRY
022106 005767 000040          TST      PRFLG          ;CHECK FOR PREVIOUS CARRY
022112 001403          BEQ      .+10          ;BRANCH IF PREVIOUSLY ZERO
022114 005067 000032          CLR      PRFLG          ;INITIALIZE FLAG
022120 000261          SEC          ;SET CARRY
022122 006102          ROL      X2          ;ROTATE NEXT CHARACTER INTO RIGHT END OF REGISTER
022124 006102          ROL      X2
022126 006102          ROL      X2
022130 005567 000016          ADC      PRFLG          ;STORE CARRY
022134 010203          MOV      X2, X3          ;LOAD DATA INTO R3
022136 042703 177770          BIC      #177770, X3          ;CLEAR ALL BUT LOWEST OCTAL DIGIT
022142 052703 000260          BIS      #260, X3          ;SET TO ASCII EQUIVALENT
022146 000730          BR
022150 000000          PRSFLG: 0
022152 000000          PRFLG: 0

;BELL ON PASS COMPLETE
022154 105777 156646          BELL:  TSTB     @TCSR
022160 100375          BPL      .-4
022162 012777 000207 156640          MOV      #207, @TDBR
022170 000207          RTS

;SUBROUTINE TO OUTPUT CARRIAGE RETURN AND LINE FEED
022172 105777 156630          CALF:  TSTB     @TCSR          ;WAIT FOR TTY READY
022176 100375          BPL      .-4
022200 012777 000215 156622          MOV      #215, @TDBR          ;OUTPUT CARRIAGE RETURN
022206 105777 156614          TSTB     @TCSR          ;WAIT FOR TTY READY
022212 100375          BPL      .-4
022214 012777 000212 156606          MOV      #212, @TDBR          ;OUTPUT LINEFEED
022222 000207          RTS          ;RETURN

;SCOPE AND/OR ITERATION LOOP FOR EACH TEST 64 TIMES
;A SETUP ROUTINE SHOULD INITIALIZE RETURN AND ICOUNT
022224 032777 040000 156604          SCOPEC: BIT      #40000, SR          ;TEST SR FOR SCOPE
022232 001015          BNE      SCOPEB          ;YES, SCOPE
022234 032777 004000 156574          BIT      #4000, SR          ;NO-TEST FOR ITERATION
022242 001016          BNE      SCOPEC          ;INHIBIT ITERATION
022244 005767 156636          TST      TSTX          ;USING SINGLE SUBTEST STARTUP?
022250 001006          BNE      SCOPEB          ;YES, LOOP
022252 026767 000042 000036          CMP      SCOPEF, ICOUNT          ;COMPARE CURRENT COUNT TO MAX NUMBER
022254 001007          BPL      SCOPEC          ;EXIT-DONE
022256 005267 000032          INC      SCOPEF          ;INCREMENT COUNT
022266 022606          SCOPEB: CMP      (6)+, %6          ;REPOSITION STACK
  
```

```

022270 012677 156540      MOV      (6),@PSR      ;RESTORE PREVIOUS PROCESSOR STATUS
022274 000177 000022      JMP      @RETURN      ;REPEAT TEST
022300 005067 156602      SCOPEG: CLR      !STX      ;IF USING TESTX STARTUP, RETURN TO NORMAL FLOW
022304 005067 000010      CLR      SCOPEF      ;CLEAR COUNT
022310 011667 000006      MOV      @%6,RETURN  ;SAVE SCOPE RETURN POINTER
022314 000002      RTI                    ;RETURN INLINE-NEXT TEST
022316 000100      ICOUNT: 100          ;ITERATION COUNT
022320 000000      SCOPEF: 0           ;COUNT LOCATION FOR ITERATION LOOP
022322 000000      RETURN: 0          ;ADDRESS OF LAST TEST

```

```

022324 017702 000020      ;MESSAGE TABLE HANDLER
022330 001001      TYPE:  MOV      @TYTMP,R2      ;PUT ADDRESS OF ASCII IN R2
022332 000207      BNE      .+4              ;IF ZERO, EXIT
022334 062767 000002 000006      RTS      %7              ;OTHERWISE, MOVE POINTER
022342 004767 000004      ADD      @2,TYTMP        ;TYPE ASCII
022346 000766      JSR      %7,TOUT        ;LOOP TILL ALL SUB-MESSAGES HAVE BEEN PRINTED
022350 000000      BR      TYPE
TYTMP:  0

```

```

022352 142777 000177 156446      ;MESSAGE SUBROUTINE
022354 105712      ;TO USE, MOVE ADDRESS OF MESSAGE TO REGISTER 2
022356 001001      ;THEN JSR %7, TOUT
022358 000207      TOUT:  BICB      @177,@TCSR      ;CLR INT FLAG
022360 001001      A.TOUT: TSTB      @R2          ;COMPARE FOR EOM
022362 000207      BNE      .+4              ;BRANCH IF NOT END OF MESSAGE
022364 000207      RTS      %7              ;RETURN IF EOM
022366 121227 000100      CMPB      @%2,@'a        ;CHECK FOR CR, LF REQUEST
022372 001003      BNE      .+10            ;BRANCH IF NOT
022374 004767 177572      JSR      %7,CRLF        ;OUTPUT CARRIAGE RETURN, LINEFEED
022400 000405      BR      A.INC          ;NEXT CHARACTER
022402 105777 156420      TSTB      @TCSR        ;WAIT FOR TTY
022406 100375      BPL      .-4            ;
022410 111277 156414      MOVB      (2),@TDBR      ;OUTPUT NEXT CHARACTER
022414 005202      A.INC: INC      R2
022416 000760      BR      A.TOUT        ;CONTINUE

```

```

022420 052100 042510 044440      S1:  .ASCIZ  /@THE INTERRUPT LEVEL WAS /
022422 052116 051105 052522
022434 052120 046040 053105
022442 046105 053440 051501
022450 000040

```

```

022452 041500 040510 043516      S2:  .ASCIZ  /@CHANGE SR OF OTHER CPU:2/
022460 020105 051123 047440
022466 020106 052117 042510
022474 020122 050103 035125
022502 000100

```

```

022504 041500 042514 051101      S3:  .ASCIZ  /@CLEAR SR OF OTHER CPU/
022512 051440 020122 043117
022520 047440 044124 051105
022526 041440 052520      000

```

```

022533      123 052105 051440      S4:  .ASCIZ  /SET SWITCH /
022540 044527 041524 020110
022546      000

```

022547	040	047524	040440	55:	.ASCIZ / TO A ONE/
022554	047440	042516	000		
022561	100	046103	040505	56:	.ASCIZ /ACLEAR SWITCH /
022566	020122	053523	052111		
022574	044103	000040			
022600	042532	047522	000	5N0:	.ASCIZ /ZERO/
022605	117	042516	000	5N1:	.ASCIZ /ONE/
022611	124	047527	000	5N2:	.ASCIZ /TWO/
022615	124	051110	042505	5N3:	.ASCIZ /THREE/
022622	000				
022623	106	052517	000122	5N4:	.ASCIZ /FOUR/
022630	044506	042526	000	5N5:	.ASCIZ /FIVE/
022635	123	054111	000	5N6:	.ASCIZ /SIX/
022641	123	053105	047105	5N7:	.ASCIZ /SEVEN/
022646	000				
022647	105	043511	052110	5N8:	.ASCIZ /EIGHT/
022654	000				
022655	116	047111	000105	5N9:	.ASCIZ /NINE/
022662	040440	042116	052040	58:	.ASCIZ / AND THEN /
022670	042510	020116	000		
022675	100	044124	047105	59:	.ASCIZ /ATHEN PRESS "CONT" ON THIS CPU333/
022702	050040	042522	051523		
022710	021040	047503	052116		
022716	020042	047117	052040		
022724	044510	020123	050103		
022732	040125	040100	000		
022737	124	047105	000	5N10:	.ASCIZ /TEN/
022743	105	042514	042526	5N11:	.ASCIZ /ELEVEN/
022750	000116				
022752	053524	046105	042526	5N12:	.ASCIZ /TWELVE/
022760	000				
022761	124	044510	052122	5N13:	.ASCIZ /THIRTEEN/
022766	042505	000116			
022772	050100	053517	051105	510:	.ASCIZ /POWER DOWN ONE DEVICE ON THE SWITCHED BUS3/
023000	042040	053517	020116		
023006	047117	020105	042504		
023014	044526	042503	047440		

023022	020116	044124	020105		
023030	053523	052111	044103		
023036	042105	041040	051525		
023044	000100				
023046	050100	053517	051105	S11:	.ASCIZ /POWER THE DEVICE BACK UP/
023054	052040	042510	042040		
023062	053105	041511	020105		
023070	040502	045503	052440		
023076	000120				
023100	051500	040524	052122	S12:	.ASCII /START THE OTHER CPU AT SA 210/
023106	052040	042510	047440		
023114	044124	051105	041440		
023122	052520	040440	020124		
023130	040523	031040	030061		
023136	040500	042116	044440		.ASCIZ /AND INPUT THE INFORMATION REQUESTED/
023144	050116	052125	052040		
023152	042510	044440	043116		
023160	051117	040515	044524		
023166	047117	051040	050505		
023174	042525	052123	042105		
023202	000				
023203	100	042523	020124	S13:	.ASCII ;SET THE ADDRESS OF THE WORD COUNT REGISTER OR BUS ;
023210	044124	020105	042101		
023216	051104	051505	020123		
023224	043117	052040	042510		
023232	053440	051117	020104		
023240	047503	047125	020124		
023246	042523	044507	052123		
023254	051105	047440	020122		
023262	052502	020123			
023266	042101	051104	051505		.ASCII ;ADDRESS REGISTER OF AN NPR DEVICE WHICH IS ON ;
023274	020123	042522	044507		
023302	052123	051105	040040		
023310	043117	040440	020116		
023316	050116	020122	042504		
023324	044526	042503	053440		
023332	044510	044103	044440		
023340	020123	047117	040		
023345	124	042510	051440		.ASCII ;THE SWITCHED BUS IN THE SWITCH REGISTER (SR) SWITCHES.;
023352	044527	041524	042510		
023360	020104	052502	020123		
023366	044500	020116	044124		
023374	020105	053523	052111		
023402	044103	051040	043505		
023410	051511	042524	020122		
023416	051450	024522	051440		
023424	044527	041524	042510		
023432	027123	100			
023435	123	042505	051440		.ASCII ;SEE SECTION 5.2.9 OF THE DOCUMENT FOR THE CONDITIONS ;



023442 041505 044524 047117  
 023450 032440 031056 034456  
 023456 047440 020106 044124  
 023464 020105 047504 052503  
 023472 042515 052116 043040  
 023500 051117 052040 042510  
 023506 041440 047117 044504  
 023514 044524 047117 020123  
 023522 100

023523 124 040510 020124  
 023530 044124 051511 040440  
 023536 042104 042522 051523  
 023544 046440 051525 020124  
 023552 040523 044524 043123  
 023560 027131 000

.ASCIZ ; THAT THIS ADDRESS MUST SATISFY.;

023563 100 042523 020124  
 023570 044124 020105 051123  
 023576 051440 044527 041524  
 023604 042510 020123 047503  
 023612 051122 051505 047520  
 023620 042116 047111 020107  
 023626 047524 052100 042510  
 023634 040

S14: .ASCII /SET THE SR SWITCHES CORRESPONDING TO THE /

023635 102 052111 020123  
 023642 047111 052040 040510  
 023650 020124 042101 051104  
 023656 051505 020123 000

.ASCIZ /BITS IN THAT ADDRESS /

023663 124 040510 020124  
 023670 051101 020105 042522  
 023676 042101 053457 044522  
 023704 042524 000

S14A: .ASCIZ @ THAT ARE READ/WRITE@

023707 100 042522 052123  
 023714 051117 020105 051123  
 023722 052040 020117 054504  
 023730 040516 044516 020103  
 023736 053523 052111 044103  
 023744 051440 052105 044524  
 023752 043516 000123

S15: .ASCIZ /RESTORE SR TO DYNAMIC SWITCH SETTINGS/

023756 050100 052125 052040  
 023764 042510 021040 047111  
 023772 052111 044456 044116  
 024000 041111 052111 044440  
 024006 044516 021124 051440  
 024014 044527 041524 020110  
 024022 047111 052040 042510  
 024030 000040

S16: .ASCIZ /PUT THE "INIT-INHIBIT INIT" SWITCH IN THE /

024032 044442 044116 041111  
 024040 052111 044440 044516  
 024046 021124 050040 051517

S17: .ASCIZ /"INHIBIT INIT" POSITION/

DZDTA-B MACY11 27(732) 27-OCT-76 15:57 PAGE 74  
 DZDTA.B

024054	052111	047511	000116		
024062	044442	044516	021124	S18:	.ASCIZ /"INIT" POSITION/
024070	050040	051517	052111		
024076	047511	000116			
024102	050100	053517	051105	S19:	.ASCIZ /@POWER DOWN THIS CPU/
024110	042040	053517	020116		
024116	044124	051511	041440		
024124	052520	000			
024127	100	047520	042527	S20:	.ASCIZ /@POWER THIS CPU BACK UP@@@/
024134	020122	044124	051511		
024142	041440	052520	041040		
024150	041501	020113	050125		
024156	040100	000100			
024162	050100	053517	051105	S21:	.ASCIZ /@POWER DOWN THE DT11/
024170	042040	053517	020116		
024176	044124	020105	052104		
024204	030461	000			
024207	100	044124	047105	S22:	.ASCIZ /@THEN POWER THE DT11 BACK UP@@@/
024214	050040	053517	051105		
024222	052040	042510	042040		
024230	030524	020061	040502		
024236	045503	052440	040120		
024244	040100	000			
024247	040	047111	052040	S23:	.ASCIZ / IN THIS CPU'S SR@@@/
024254	044510	020123	050103		
024262	023525	020123	051123		
024270	040100	000100			
024274	044124	052101	040440	S24:	.ASCIZ /THAT ARE CLEARED BY INIT./
024302	042522	041440	042514		
024310	051101	042105	041040		
024316	020131	047111	052111		
024324	000056				
024326	044500	050116	052125	S25:	.ASCIZ /@INPUT THE SAME INFORMATION AS INITIALLY REQUESTED ON THE OTHER SIDE/
024334	052040	042510	051440		
024342	046501	020105	047111		
024350	047506	046522	052101		
024356	047511	020116	051501		
024364	044440	044516	044524		
024372	046101	054514	051040		
024400	050505	042525	052123		
024406	042105	047440	020116		
024414	044124	020105	052117		
024422	042510	020122	044523		
024430	042504	000			
024433	100	046103	040505	S26:	.ASCIZ /@CLEAR SR OF OTHER CPU, THEN SET SWITCH /
024440	020122	051123	047440		
024446	020106	052117	042510		

024454	020122	050103	026125		
024462	052040	042510	020116		
024470	042523	020124	053523		
024476	052111	044103	000040		
024504	053500	042510	020116	S27:	.ASCIZ /WHEN THIS PRINTOUT IS FINISHED PRESS "CONTINUE." THEN/
024512	044124	051511	050040		
024520	044522	052116	052517		
024526	020124	051511	043040		
024534	047111	051511	042510		
024542	020104	051120	051505		
024550	020123	041442	047117		
024556	044524	052516	027105		
024564	020042	044124	047105		
024572	000				
024573	100	040100	047105	S28:	.ASCIZ /END OF PASS3/
024600	020104	043117	050040		
024606	051501	040123	000		
024613	116	020117		S29:	.ASCII /NO /
024616	051105	047522	051522	S30:	.ASCIZ /ERRORS OCCURRED/
024624	047440	041503	051125		
024632	042522	000104			
024636	050100	053517	051105	S31:	.ASCIZ /POWER FAIL WAS /
024644	043040	044501	020114		
024652	040527	020123	000		
024657	116	052117	000040	S32:	.ASCIZ /NOT /
024664	042524	052123	042105	S33:	.ASCIZ /TESTED/
024672	000				
024673	100	051123	051440	S34:	.ASCIZ /SR SWITCH NINE WAS/
024700	044527	041524	020110		
024706	044516	042516	053440		
024714	051501	000			
024717	040	042523	040124	S35:	.ASCIZ / SET333/
024724	040100	000100			
024730	041440	042514	051101	S36:	.ASCIZ / CLEAR333/
024736	040100	040100	000		
024743	100	053523	052111	S37:	.ASCIZ /SWITCHED BUS POWER FAIL WAS /
024750	044103	042105	041040		
024756	051525	050040	053517		
024764	051105	043040	044501		
024772	020114	040527	020123		
025030	000				
025001	106	046125	054514	S38:	.ASCIZ /FULLY /
025006	000040				

```

025010 040520 052122 040511 S39: .ASCIZ /PARTIALLY /
025016 046114 020131 000

025023 100 047524 043507 S40: .ASCIZ /@TOGGLE SWITCH ZERO AT LEAST TEN TIMES@/
025030 042514 051440 044527
025036 041524 020110 042532
025044 047522 040440 020124
025052 042514 051501 020124
025060 042524 020116 044524
025066 042515 040123 000

025074

;MSG1: .EVEN
;MSG1: "THE INTERRUPT LEVEL WAS"

025074 022420 000000 MSG1: .WORD S1,0

;MSG2: "CLEAR SR OF OTHER CPU
;THEN SET SWITCH 0.
;THEN PRESS 'CONTINUE' ON THIS
;PROCESSOR."

025100 024433 022600 022675 MSG2: .WORD S26,SND,S9,0
025106 000000

;MSG3: "CLEAR SR OF OTHER CPU
;THEN SET SWITCH ONE. THEN PRESS
;'CONTINUE' ON THIS PROCESSOR."

025110 024433 022605 022675 MSG3: .WORD S26,SN1,S9,0
025116 000000

;MSG4: "CLEAR SR OF OTHER CPU.
;THEN SET SWITCH 2. THEN PRESS
;'CONTINUE' ON THIS PROCESSOR."

025120 024433 022611 022675 MSG4: .WORD S26,SN2,S9,0
025126 000000

;MSG5: "CLEAR SR OF OTHER CPU.
;THEN PRESS 'CONT' ON THIS CPU."

025130 022504 022675 000000 MSG5: .WORD S3,S9,0

;MSG6: "POWER DOWN ONE DEVICE ON
;THE SWITCHED BUS, AND THEN SET SWITCH 0
;IN THIS PROCESSOR'S SWITCH REGISTER."

025136 022772 022662 022533 MSG6: .WORD S10,S8,S4,SND,S23,0
025144 022600 024247 000000

;MSG7: "POWER THE DEVICE BACK UP, AND THEN CLEAR SWITCH 0 IN
;THIS PROCESSOR'S SWITCH REGISTER"

025152 023046 022662 022561 MSG7: .WORD S11,S8,S6,SND,S23,0
025160 022600 024247 000000

```

```

;MSG8: "START THE OTHER PROCESSOR AT STARTING ADDRESS 210. THEN
;PRESS 'CONTINUE' ON THIS PROCESSOR."
025166 023100 022675 000000 MSG8: S12,S9,0
;MSG9: "SET THE ADDRESS OF THE WORD COUNT REGISTER OR BUS ADDRESS
;REGISTER OF AN NPR DEVICE WHICH IS ON THE SWITCHED BUS IN
;THE SWITCH REGISTER SWITCHES. SEE SECTION 8 OF THE DOCUMENT
;FOR THE CONDITIONS THAT THIS ADDRESS MUST SATISFY. THEN PRESS
;'CONTINUE' ON THIS PROCESSOR."
025174 023203 022675 000000 MSG9: S13,S9,0
;MSG10: "SET THE SWITCH REGISTER SWITCHES CORRESPONDING TO THE BITS IN
;THAT ADDRESS THAT ARE READ/WRITE. THEN PRESS 'CONTINUE' ON THIS
;PROCESSOR."
025202 023563 023663 022675 MSG10: S14,S14A,S9,0
025210 000000
;MSG11: "RESTORE SWITCH REGISTER TO DYNAMIC SWITCH SETTINGS.
;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."
025212 023707 022675 000000 MSG11: S15,S9,0
;MSG12: "PUT THE 'INIT-INHIBIT INIT' SWITCH IN THE 'INHIBIT INIT' POSITION.
;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."
025220 023756 024032 022675 MSG12: S16,S17,S9,0
025226 000000
;MSG13: "PUT THE 'INIT-INHIBIT INIT' SWITCH IN THE 'INIT' POSITION.
;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."
025230 023756 024062 022675 MSG13: S16,S18,S9,0
025236 000000
;MSG14: "CLEAR SR OF OTHER CPU,
;THEN SET SWITCH 3.
;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."
025240 024433 022615 022675 MSG14: S26,SN3,S9,0
025246 000000
;MSG15: "CLEAR SR OF OTHER CPU,
;THEN SET SWITCH 4.
;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."
025250 024433 022623 022675 MSG15: S26,SN4,S9,0
025256 000000
;MSG16: "CLEAR SR OF OTHER CPU,
;THEN SET SWITCH 5.
;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."
025260 024433 022630 022675 MSG16: S26,SN5,S9,0

```

025266 000000

```

;MSG17: "CLEAR SR OF OTHER CPU,
;THEN SET SWITCH 6.
;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."

```

```

025270 024433 022635 022675 MSG17: S26,SN6,S9,0
025276 000000

```

```

;MSG18: "CLEAR SR OF OTHER CPU,
;THEN SET SWITCH 7.
;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."

```

```

025300 024433 022641 022675 MSG18: S26,SN7,S9,0
025306 000000

```

```

;MSG19: "CLEAR SR OF OTHER CPU,
;THEN SET SWITCH 8.
;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."

```

```

025310 024433 022647 022675 MSG19: S26,SN8,S9,0
025316 000000

```

```

;MSG20: "SR SWITCH 9 WAS SET"

```

```

025320 024673 024717 000000 MSG20: S34,S35,0

```

```

;MSG21: "POWER DOWN THIS PROCESSOR. AND THEN
;POWER THIS PROCESSOR BACKUP."

```

```

025326 024102 022662 024127 MSG21: S19,S8,S20,0
025334 000000

```

```

;MSG22: "POWER DOWN THIS PROCESSOR
;CHANGE SWITCH REGISTER OF OTHER PROCESSOR:
;SET SWITCH 9.
;AND THEN POWER THIS PROCESSOR BACKUP."

```

```

025336 024102 022452 022533 MSG22: S19,S2,S4,SN9,S8,S20,0
025344 022655 022662 024127
025352 000000

```

```

;MSG23: "POWER DOWN THE BUS SWITCH.
;THEN POWER THE BUS SWITCH BACK UP."

```

```

025354 024162 024207 000000 MSG23: S21,S22,0

```

```

;MSG24: "SET THE SWITCH REGISTER SWITCHES CORRESPONDING TO THE
;BITS IN THAT ADDRESS THAT ARE CLEARED BY INIT.
;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."

```

```

025362 023563 024274 022675 MSG24: S14,S24,S9,0
025370 000000

```

```

;MSG25: "CLEAR SR OF OTHER CPU."

```

025372 022504 000000 MSG25: S3,0  
;MSG26: "SR SWITCH 9 WAS CLEAR."

025376 024673 024730 000000 MSG26: S34,S36,0  
;MSG27: "INPUT THE SAME INFORMATION AS INITIALLY REQUESTED ON  
;THE OTHER SIDE."

025404 024326 000000 MSG27: S25,0  
;MSG28: "CLEAR SR OF OTHER CPU,  
;THEN SET SWITCH 10.  
;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."

025410 024433 022737 022675 MSG28: S26,SN10,S9,0  
025416 000000  
;MSG29: "CLEAR SR OF OTHER CPU,  
;THEN SET SWITCH 11.  
;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."

025420 024433 022743 022675 MSG29: S26,SN11,S9,0  
025426 000000  
;MSG30: "WHEN THIS PRINTOUT IS FINISHED, PRESS 'CONTINUE'. THEN"

025430 024504 000000 MSG30: S27,0  
;MSG31: "END OF PASS"

025434 024573 000000 MSG31: S28,0  
;MSG32: "NO ERRORS OCCURRED"

025440 024613 000000 MSG32: S29,0  
;MSG33: "ERRORS OCCURRED"

025444 024616 000000 MSG33: S30,0  
;MSG34: "POWER FAIL WAS TESTED"

025450 024636 024664 000000 MSG34: S31,S33,0  
;MSG35: "POWER FAIL WAS NOT TESTED"

025456 024636 024657 024664 MSG35: S31,S32,S33,0  
025464 000000  
;MSG36: "CLEAR SR OF OTHER CPU,  
;THEN SET SWITCH TWELVE.  
;THEN PRESS 'CONTINUE' ON THIS PROCESSOR."

025466 024433 022752 022675 MSG36: S26,SN12,S9,0

025474 000000

;MSG37: "CLEAR SR OF OTHER CPU,  
;THEN SET SWITCH THIRTEEN,  
;THEN PRESS 'CONT' ON THIS CPU."025476 024433 022761 022675 MSG37: S26,SN13,S9,0  
025504 000000

;MSG38: "SWITCHED BUS POWER FAIL WAS FULLY TESTED"

025506 024743 025001 024664 MSG38: S37,S38,S33,0  
025514 000000

;MSG39: "SWITCHED BUS POWER FAIL WAS NOT TESTED"

025516 024743 024657 024664 MSG39: S37,S32,S33,0  
025524 000000

;MSG40: "SWITCHED BUS POWER FAIL WAS PARTIALLY TESTED"

025526 024743 025010 024664 MSG40: S37,S39,S33,0  
025534 000000;MSG41: ;"WHEN THIS PRINTOUT IS FINISHED, PRESS "CONTINUE." THEN  
;CHANGE SR OF OTHER CPU:  
;TOGGLE SWITCH ZERO AT LEAST TEN TIMES  
;THEN SET SWITCH ZERO IN THIS CPU'S SR"025536 024504 022452 025023 MSG41: S27,S2,S40,S8,S4,SND,S23,0  
025544 022662 022533 022600  
025552 024247 000000;MSG42: "CLEAR SR OF OTHER CPU AND THEN  
;CLEAR SWITCH ZERO IN THIS CPU'S SR."025556 022504 022662 022561 MSG42: S3,S8,S6,SND,S23,0  
025564 022600 024247 000000

000001

.END





CNT1	001444	685	690#																	
CNT1A	001456	689	693#																	
CNT25	005756	1395	1399#																	
CNT31A	007046	1551	1554#																	
CNT32A	007206	1579	1596#																	
CNT33A	007352	1615	1629#																	
CNT34	007414	1602	1639	1643#																
CNT34A	007512	1650	1661#																	
CNT35	007650	1676	1690#																	
CNT39A	010732	1904	1914	1916	1920#															
CNT4	002036	764	769#																	
CNT4A	002050	768	772#																	
CNT40	001046	601#	1933#	1935#	1939#	1950#	1952#													
CNT40A	001050	602#	1934#	1936#	1940#	1951#	1953#	1954												
CNT53A	014226	2654#	2650#																	
CNT54A	015014	2677	2679#																	
CNT55	015400	2756	2764#																	
CNT55A	015436	2774	2777#																	
CNT55B	015474	2778	2780	2786#	2821															
CONT1	001632	712	725#																	
CONT14	003212	975	981#																	
CONT16	003370	1020#	1021																	
CONT23	005506	11343	11348#																	
CONT24	005626	11367	11372#																	
CONT25	006026	11407	11410#																	
CONT26	006200	11428	11437	1440#																
CONT27	006322	11460	11463#																	
CONT28	006434	11479	11482#																	
CONT29	006560	11504	11507#																	
CONT30	006706	11528	11532#																	
CONT42	011404	2022	2024#																	
CONT43	011636	2073	2075#																	
CONT50	013246	2362	2364#																	
CONT51	013500	2417	2419#																	
CONT53	014234	2510	2551#	2594																
CONT54	015022	2639	2680#	2723																
CONT6	002216	806	811#																	
CONT7	002362	843	848#																	
CONT8	002452	867	872#																	
COUNT	001066	610#																		
CRLF	022172	2858	2859	3591	3673#	3721														
DONE	015630	1966	1981	2484	2800	2803	2822#													
DT11A	001110	581	625#																	
DT11AF	001104	618#	625#	631#	684	763	1691	1982	2033	2083	2115	2319	2374	2428						
DVARDS	001054	2480	2491	2620	2755	2799	2836													
		605#	799#	800	842#	862#	933#	1545#	1546	1556	1573#	1574	1586	1609#						
		1610	1621	1644#	1645#	1656	1670#	1671	1681	1781#	2020#	2071#	2358#	2413#						
		3054#	3074#	3308#	3309	3319	3342#	3343	3350	3400#										
ENTAB	021304	3447	3451#																	
ENTSRV	021236	3452	3451#																	
END	016044	1634	1631#																	
ERR	021732	2944#	2984#	2948	2903#	3365	3378#	3582#	3610#											
FLAGS	021072	2909#	3003#	3005#	3048	3050#	3381#													
HLT	* 104410	676	688	692	700	704	710	718	724	741	752	767	771	783						
		796	802	808	829	840	845	860	865	881	892	904	918	922						
		926	930	934	947	951	956	973	978	996	1032	1037	1050	1075						







RET16A	017114	3040	3057#											
RET16B	017160	3057	3067#											
RET17A	017360	3085	3108#											
RET17B	017424	3108	3118#											
RET19A	020142	3180	3226#											
RET19B	020206	3226	3236#											
RETURN	022322	671#	1639#	3568#	3569#	3577	3694	3697#	3701#					
RET12	002764	931	937#											
RET37	010152	1779	1783#											
RET42	011402	2018	2023#											
RET43	011634	2069	2074#											
RETS0A	013112	2328	2333#											
RETS0B	013142	2333	2339#											
RETS0C	013244	2356	2363#											
RETS1A	013344	2383	2388#											
RETS1B	013374	2388	2394#											
RETS1C	013476	2411	2418#											
RETS2A	013600	2437	2442#											
RETS2B	013630	2442	2448#											
RETS2C	014044	2498	2511#											
RETS2D	014074	2511	2520#											
RETS2E	014224	2544	2549#											
RETS2F	014264	2572	2577#											
RETS2G	014414	2777	2784#											
RETS2H	014452	2805	2808#											
RETS2I	014474	2805	2808#											
RETS4A	014630	2977	2980#											
RETS4B	014660	2980	2989#											
RETS4C	015012	3073	3078#											
RETS4D	015115	3051	3056#											
RETS4E	015220	3076	3081#											
RETS4F	015240	3081	3086#											
RETS4G	015260	3081	3086#											
RETS4H	015260	3081	3086#											
RETS5	015560	2804	2804#											
RETS5A	015602	2804	2812#											
RET6	002212	797	807#											
RET7	002356	841	844#											
RET8	002450	861	868#											
RSTART	001156	569	637#											
RMBITS	001056	606#	799	800	842	862	933	1781	2020	2071	2358	2413	2545	2674
RO	%000000	3406#	3413											
R1	%000001	535#												
		536#	713#	716	825#	827	1546#	1547#	1548	1574#	1575#	1576	1610#	1611#
		1612	1645#	1646#	1647	1656#	1657#	1658	1671#	1672#	1673	1681#	1682#	1683
		1834#	1835	2871#	2874	3309#	3310#	3311	3319#	3320#	3321	3343#	3344#	3345
		3350#	3351#	3352										
R2	%000002	537#	1092#	1138#	1184#	1230#	1276#	1322#	3617	3704#	3716	3726#		
R3	%000003	538#	3624	3647#										
R4	%000004	539#												
R5	%000005	540#												
SAVPC	021726	3587#	3593	3608#										
SAVPSA	021730	3588#	3598	3609#										
SAVR2	021720	3592#	3600	3605#										
SAVR3	021722	3606#	3624#	3647										
SAVR4	021724	3607#	3625#	3648										
SBINH	001052	603#	650#	653#	656#	2477	2485	2757	2779	2861	2865			

DZDTA-B MACY11 27(732) 27-OCT-76 15:57 PAGE 88  
DZDTA.B CROSS REFERENCE TABLE -- USER SYMBOLS

SCOPE = 104406

SCOPEB 022266  
SCOPEB 022224  
SCOPEB 022320  
SCOPEB 022300  
SCOPEB 001164  
SCOPEB 005402  
SCOPEB 003532  
SCOPEB 005146  
SCOPEB 004712  
SCOPEB 004456  
SCOPEB 004222  
SCOPEB 003766  
SHORTF 001074  
GND 022600  
GND 022605  
GND 022737  
GND 022743  
GND 022752  
GND 022761  
GND 022611  
GND 022615  
GND 022623  
GND 022630  
GND 022635  
GND 022641  
GND 022647  
GND 022655  
=X000006

682	732	747	755	777	792	821	836	856	876	887	898	914
944	963	988	1014	1055	1101	1147	1193	1239	1285	1333	1357	1382
1418	1448	1468	1490	1515	1543	1571	1601	1607	1638	1668	1703	1726
1743	1765	1827	1853	1875	1926	1976	2032	2082	2121	2154	2191	2231
2271	2318	2373	2427	2490	2619	2751	2822	3551#				
3684	3688	3692#										
3556	3683#											
3689	3691#	3696#	3700#									
3686	3690	3695#										
627	633	637	639#									
1319	1325#											
1045	1048#											
1273	1279#											
1227	1233#											
1181	1187#											
1135	1141#											
1089	1095#											
613#	639#	1632	2881#									
3757#	4050	4076	4082	4282	4289							
3759#	4057											
3790#	4213											
3792#	4220											
3795#	4252											
3798#	4259											
3761#	4064											
3763#	4126											
3766#	4133											
3768#	4140											
3770#	4147											
3772#	4154											
3775#	4161											
3778#	4179											
541#	562#	565#	568#	571#	574#	577#	580#	667	807	844	868	937
979	997	1043	1087	1133	1179	1225	1271	1317	1347	1371	1398	1409
1432	1439	1462	1481	1506	1531	1783	1899	1915	1919	1997	1999#	2001#
2002	2023	2048	2050#	2052#	2053	2074	2096	2098#	2100#	2101	2133	2135#
2137#	2138	2167	2169#	2171#	2172	2207	2209#	2211#	2212	2248	2250#	2252#
2253	2285	2287#	2289#	2290	2335	2337#	2339#	2340	2363	2390	2392#	2394#
2395	2418	2444	2446#	2448#	2449	2512	2518#	2520#	2521	2549	2578	2582#
2584#	2585	2596	2602#	2603	2641	2647#	2649#	2650	2678	2707	2711#	2713#
2714	2725	2731#	2732	2805	2810#	2812#	2813	2890#	2892#	2893#	2967	2969#
2976#	2984	3013	3015#	3022#	3030	3058	3060#	3067#	3075	3109	3111#	3118#
3126	3144	3148#	3150#	3151	3227	3229#	3236#	3244	3276	3278#	3285#	3293
3434	3443	3541										
611#	1997#	1999	2001	2048#	2050	2052	2096#	2098	2100	2133#	2135	2137
2167#	2169	2171	2207#	2209	2211	2248#	2250	2252	2285#	2287	2289	2335#
2337	2339	2390#	2392	2394	2444#	2446	2448	2512#	2518	2520	2578#	2582
2584	2596#	2602	2641#	2647	2649	2707#	2711	2713	2725#	2731	2805#	2810
2812	2967#	2969	2976	3013#	3015	3022	3058#	3060	3067	3109#	3111	3118
3144#	3148	3150	3227#	3229	3236	3276#	3278	3285				
597#	645	651	654	1838	1845	2503	2527	2559	2632	2656	2688	2769
2775	2792	2888	2910	2914	2919	2924	2929	2934	2939	2946	2957	2973
2982	2990	3008	3019	3028	3036	3053	3064	3073	3081	3093	3104	3115
3124	3131	3137	3170	3176	3188	3210	3217	3222	3233	3242	3250	3264
3271	3282	3291	3301	3316	3335	3348	3363	3371	3376	3400	3406	3412
3568	3572	3583	3585	3601	3683	3685						

SPSAV 001070

SR 001036











COMMEN	10						
ENDCOM	10						
ESCAPE	10						
GETPRI	10						
GETSMR	10						
INT	10530	1054	1100	1146	1192	1238	1284
MULT	10						
NEWTST	10						
PFAIL1	6210	1990	2041	2089	2126	2160	
PFAIL2	6220	2195	2236				
POP	10						
PUSH	10						
REPORT	10						
SBFAIL	24770	2490	2619				
SETPRI	10						
SETUP	10						
SKIP	10						
SLASH	10						
SPPFCK	6240	2966	3012	3057	3108	3226	3275
STARS	10						
SMFAIL	23150	2318	2373	2427			
SMRSU	10						
TYPBIN	10						
TYPDEC	10						
TYPNAM	10						
TYPNUM	10						
TYPDCS	10						
TYPDCT	10						
TYPTXT	10						
SSESCA	10						
SSNEWT	10						
SSSKIP	10						
.EQUAT	10						
.HEADE	10						
.KT11	10						
.SETUP	10						
.SMRHI	10						
.SACT1	10						
.SAPT8	10						
.SAPTH	10						
.SAPTY	10						
.SASTA	10						
.SCATC	10						
.SCHTA	10						
.SDB2D	10						
.SDB20	10						
.SDIV	10						
.SEOP	10						
.SERRO	10						
.SERRT	10						
.SMULT	10						
.SOME	10						
.SFAND	10						
.SHDE	10						
.SRDOC	10						
.SREAD	10						

.SR2AZ	18
.SSAVE	18
.SSB2D	18
.SSB20	18
.SSCOP	18
.SSIZE	18
.SSUPR	18
.STRAP	18
.STYPB	18
.STYPD	18
.STYPE	18
.STYPO	18
.S4DCA	18
.1170	18

BR	629	636	638	648	665	689	768	806	843	867	935	975	995	1034	1047
BPL	3674 3626 3211 3338 694 1155 1526 1084 1749 2084 2429 2837 2993 3116 3211 3338 694 1155 1526 1084 1749 2084 2429 2837 2993 3116 3211 3338	3677 2897 1600 1164 706 3349 3218 3121 3004 2886 2406 2076 1748 1486 1113 884 712 2849 1386 817 3577 3215 3104 2982 2659 2275 1955 1618 1351 1001 851 651 1907 1475 1152 715	3690 2895 1633 1188 737 3358 3223 3125 3009 2891 2467 2143 1824 1511 895 717 2854 1430 839 3363 3217 3115 2990 2574 1930 1621 1375 1024 872 654 1911 1492 1195 756	3724 2998 1773 1201 759 3370 3234 3136 3020 2908 2704 2481 2177 1843 1536 907 721 2889 1501 859 3371 3222 3124 3003 2888 2613 1941 1625 1413 1039 883 696 2554 1496 1198 778	665 3044 1778 1210 971 3372 3239 3138 3025 2917 2719 2492 2177 1846 1555 917 727 3049 1695 880 3376 3233 3131 3008 2907 2632 1960 1630 1443 1066 894 711 2683 1241 888	689 3202 1792 1234 994 3586 3243 3154 3029 2920 2737 2492 2177 1846 1555 917 743 3259 1706 891 3572 3242 3137 3019 2914 2656 2027 1652 1485 1083 906 716 2786 1244 899	768 3307 1814 1247 1021 3618 3253 3171 3039 2927 2743 2492 2177 1846 1555 917 764 3259 1736 891 3583 3250 3145 3028 2919 2681 2078 1662 1510 1112 920 726 2938 1290 965	806 3341 1938 1256 1029 3646 3272 3187 3054 2940 2756 2492 2177 1846 1555 917 774 3272 1788 1031 3683 3267 3176 3048 2929 2703 2267 1717 1554 1158 924 761 3005 1334 989	843 3366 1948 1280 1049 3684 3272 3187 3054 2940 2756 2492 2177 1846 1555 917 786 3288 1799 1036 3685 3271 3182 3053 2934 2742 2367 1730 1556 1175 928 761 3045 1358 1015	867 3596 1980 1302 1072 3688 3288 3194 3070 2949 2784 2492 2177 1846 1555 917 815 3288 1801 1074 3685 3291 3188 3073 2946 2769 2436 1755 1221 945 785 3367 1392 1057	935 3602 1989 1326 1096 3705 3200 3196 3074 2958 2793 2492 2177 1846 1555 917 823 3200 1816 1074 3705 3291 3188 3073 2946 2769 2436 1755 1221 945 785 3367 1392 1057	975 3630 2040 1340 1109 3717 3200 3196 3074 2958 2793 2492 2177 1846 1555 917 823 3200 1816 1074 3717 3291 3188 3073 2946 2769 2436 1755 1221 945 785 3367 1392 1057	995 3641 2327 1364 1118 3720 3207 3193 3081 2953 2775 2466 1823 1583 1250 949 814 3576 1419 1060 3351 1657 1337 3088 2842 2531 2223 1864 1622 740	1034 3641 2327 1364 1118 3720 3207 3193 3081 2953 2775 2466 1823 1583 1250 949 814 3576 1419 1060 3351 1657 1337 3088 2842 2531 2223 1864 1622 740	1047 3668 2382 1425 1142 3727 3209 3105 2983 2743 2492 2177 1846 1555 917 852 3209 1444 1067 852 3335 3208 3093 2959 2783 2527 1841 1590 1296 958 827 1106 1103 1450 1883 1790 1419 1060 3351 1657 1337 3088 2842 2531 2223 1864 1622 740







DZDTA-B MACY11 27(732) 27-OCT-76 15:57 PAGE 100  
 DZDTA.B CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

	3778	3780	3783	3790	3792	3795	3798	3801	3810	3822	3871	3887	3892	3897	3905
	3914	3919	3923	3928	3934	3939	3946	3951	3957	3970	3978	3989	3995	3999	4003
	4005	4008	4013	4016	4019	4026	4029	4032							
.ENABL	4293														
.END	2328	2366	2383	2421	2437	2465									
.ENOC	4040														
.EVEN	2328	2383	2434												
.IFF	2325	2356	2380	2411	2434	2465									
.IFNZ	1	549													
.LIST	621	622	624	1053	2315	2477									
.MACR	1														
.MACRO	1	549													
.MLIST	1														
.REN	549	2336	2391	2445											
.REPT	1														
.TITLE	4043	4050	4057	4064	4070	4076	4082								
.WORD															

ERRORS DETECTED: 0  
 DEFAULT GLOBALS GENERATED: 0

#, NOM. SEQ/SOL/CRF/NL: TOC/PAGNUM=SYSNAC.CO, DZDTA.B  
 RUN-TIME: 33 46 5 SECONDS  
 RUN-TIME RATIO: 342/87=3.9  
 CORE USED: 36K (71 PAGES)

