

# DUV/LSI-11

DUV11 OFF-LINE LOGIC  
MD-11-DZDUQ-A

EP-DZDUQ-A-DL-A

APR 1977

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MADE IN USA

Small technical diagram or table located in the bottom right corner of the page.



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I D E N T I F I C A T I O N

PRODUCT CODE: MAINDEC-11-DZDU0-A-D

PRODUCT NAME: DUV11 OFFLINE LOGIC TESTS

RELEASE DATE: FEB. 1977

MAINTAINER : DIAGNOSTICS

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## GENERAL DESCRIPTION

THIS DIAGNOSTIC CAN CHAIN 16 DUV11'S. THIS MEANS THAT 16 DEVICES CAN BE SEQUENTIALLY EXERCISED. THE DIAGNOSTIC MAKES ONE PASS BEFORE PROCEEDING TO THE NEXT DEVICE AND CONTINUES EXERCISING ALL DEVICES IN THIS FASHION UNTIL HALTED.

1. THE DUV11 OFFLINE LOGIC TESTS VERIFY THAT ALL REGISTERS EXIST AND ALL RESPECTIVE BITS CAN BE MASTER CLEARED, READ, WRITTEN AND/OR READ/WRITTEN

\* .REM \*

## 2. REQUIREMENTS

PDP-11/03 COMPUTER (LSI)

DUV11 SYNCHRONOUS/ISOCRONOUS OPTION

ONE CONSOLE TELETYPE OR EQUIVALENT

- 2.2 STORAGE  
THE PROGRAM LOADS INTO 4K OF MEMORY WITH BOOTSTRAP

\* .REM \*

## 3. LOADING PROCEDURE

THE STANDARD PROCEDURE FOR LOADING ABSOLUTE BINARY TAPES IS TO BE USED.

STARTING ADDRESS  
FOR ABSOLUTE LOADER

4K	017500
8K	037500
12K	057500
16K	077500
20K	117500
24K	137500
28K	157500

## 4. STARTING PROCEDURE

## 4.1 CONTROL SWITCH SETTINGS

NOTE: ALL SWITCHES RESIDE INTERNAL TO THE CPU AT ADDRESS 176. THESE MAY BE SET VIA THE CONSOLE TTY BY DIRECTLY MODIFYING LOC. 176.

NOTE: RUNNING UNDER APT-11, THERE IS A USER SWITCH REGISTER CALLED "SUSWR". IN ORDER TO BE FLEXIBLE ON THE AVAILABILITY OF THE 4315 CONNECTOR, ONE BIT PASSES STATUS TO APT-11. BIT 0 IN SUSWR REFLECTS THIS STATUS, A 0 = CONNECTOR PRESENT, A 1 = CONNECTOR NOT AVAILIBLE.

- 4.1.1 AFTER PROGRAM LOAD (INITIAL PROGRAM START)  
ALL CONSOLE SWITCHES DOWN
- 4.1.2 TO MODIFY DEVICE VECTOR AND CONTROL REGISTER ADDRESSES  
AFTER PROGRAM RESTART OR TO RUN MULTIPLE DEVICES  
SW00=1
- 4.1.3 TO START PROGRAM AT SELECTED TEST AFTER A PROGRAM RESTART  
(ONLY IN SINGLE DEVICE TESTS)  
SW01=1
- 4.1.4 TO LOCK ON SELECTED TEST AFTER A PROGRAM RESTART  
(ONLY IN SINGLE DEVICE TESTS)  
SW02=1  
NOTE1: IN GENERAL SW01 WILL BE USED WHEN SW02=1 IS USED  
NOTE2: WITHOUT SW01=1 "LOCK ON TEST" WILL DEFAULT TO TEST 1
- 4.2 STARTING ADDRESS

THE STARTING ADDRESS FOR ALL TESTS IS 000200  
 THE RETARTING ADDRESS FOR ALL TESTS IS 000200  
 THE STARTING ADDRESS TO ENTER A SELECTED TEST IS 000200  
 THE STARTING ADDRESS TO LOCK ON TEST IS 000200

4.3 PROGRAM AND/OR OPERATOR ACTION

4.3.1 INITIAL PROGRAM START

- 4.3.1.1 LOAD PROGRAM INTO MEMORY WITH ABSOLUTE LOADER
- 4.3.1.2 SET SWITCH REGISTER (LOC. 176) TO ZERO.
- 4.3.1.3 TYPE 200G.
- 4.3.1.4 PROGRAM WILL START.

4.3.1.5 THE PROGRAM WILL TYPE "DUV11 DZDUQ-A TAPE A" (ONCE ONLY)

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4.3.1.6 THE PROGRAM WILL TYPE "R" TO INDICATE THAT IT IS ABOUT TO START TESTING ,AND THEN TESTING WILL BEGIN

4.3.2 PROGRAM RESTART WITH ALL SWITCHES DOWN

4.3.2.1 THE PROGRAM WILL TYPE "R" AND WILL COMMENCE TESTING

4.3.3 PROGRAM RESTART WITH SW00=1

4.3.3.1 SET SWITCH REGISTER (LOC. 176) TO A 000001.

4.3.3.2 TYPE 200G.

4.3.3.3 PROGRAM WILL START.

4.3.3.4 THE PROGRAM WILL TYPE " 1ST DEVICE: RECEIVER CONTROL REGISTER ADDRESS" AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.3.5 TYPE IN THE ADDRESS OF THE FIRST RECEIVER CONTROL REGISTER ADDRESS OF THE DUV11 TO BE TESTED FOLLOWED BY A <CARRIAGE RETURN>

IF AN INCORRECT ADDRESS IS TYPED ,THE PROGRAM WILL TYPE "?" AND WILL THEN REPEAT THE MESSAGE OF 4.3.3.4

4.3.3.6 THE PROGRAM WILL TYPE "VECTOR ADDRESS-" AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.3.7 TYPE IN THE BASE RECEIVER INTERRUPT VECTOR ADDRESS FOR THE DUV11 TO BE TESTED FOLLOWED BY A <CARRIAGE RETURN>

IF AN INCORRECT ADDRESS IS TYPED ,THE PROGRAM WILL TYPE "?" AND WILL THEN REPEAT THE MESSAGE OF 4.3.3.6

4.3.3.8 THE PROGRAM WILL TYPE "ARE YOU RUNNING MULTIPLE DEVICES ?" (Y OR N)-" AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.3.9 TYPE IN THE APPROPRIATE ANSWER YES OR NO FOLLOWED BY A <CARRIAGE RETURN>

IF AN INCORRECT ANSWER IS GIVEN, THE PROGRAM WILL TYPE "?" AND WILL THEN REPEAT THE MESSAGE OF 4.3.3.8

IF A "NO" ANSWER IS GIVEN: JUMP TO SECTION 4.3.3.12  
 IF A "YES" ANSWER IS GIVEN: THE NEXT QUESTION IS ASKED

4.3.3.10 THE PROGRAM WILL TYPE "LAST DEVICE:RECEIVER CONTROL REGISTER ADDRESS-" AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.3.11 TYPE IN THE ADDRESS OF THE LAST RECEIVER CONTROL REGISTER ADDRESS OF THE DUV11 TO BE TESTED FOLLOWED BY A <CARRIAGE RETURN>

IF AN INCORRECT ANSWER IS TYPED ,THE PROGRAM WILL TYPE "?" AND WILL THEN REPEAT THE MESSAGE OF 4.3.3.10  
 NOTE:ALL ADDRESSES SHALL BE CONTIGUOUS

4.3.3.11.1 IF AN "OUT OF RANGE" ADDRESS IS TYPED  
 IE. MORE THAN 16 (10) DEVICES AWAY (UPWARDS).....THE PROGRAM WILL TYPE "OUT OF RANGE:RETYPE LAST DEVICE RXCSR ADDRESS-" AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.3.11.2 TYPE IN THE ADDRESS OF THE LAST RECEIVER CONTROL

REGISTER ADDRESS OF THE DUV11 TO BE TESTED FOLLOWED  
BY A <CARRIAGE RETURN>

IF AN INCORRECT ANSWER IS TYPED ,THE PROGRAM WILL TYPE "?"  
AND WILL REPEAT THE MESSAGE OF 4.3.3.11.1

IF A DEVICE ADDRESS LOWER THAN 1ST DEVICE ADDRESS IS TYPED.....  
...SCHOOLS OUT..... THERE IS NO PROTECTION FOR THIS.  
THE PROGRAM WILL DEFAULT TO TWO DEVICES ACTIVE (UPWARDS FROM  
1ST DEVICE ADDRESS).THE SAME APPLIES TO IDENTICAL ADDRESSES  
TYPED FOR FIRST AND LAST DEVICE.  
OBSERVE LOCATION @ ACTREG: SEE SECTION 7.2

4.3.3.12 THE PROGRAM WILL TYPE "# OF SYNC CHARS  
SELECTED (1 OR 2)-" AND WAIT FOR AN INPUT FROM THE TELETYPE  
KEYBOARD. REFER TO MANUAL FOR PROPER SWITCH SETTINGS OF  
SWITCH E55-4.

4.3.3.13 TYPE IN THE APPROPRIATE ANSWER "1" OR "2" FOLLOWED  
BY A <CARRIAGE RETURN>. (NOTE:ALL MULTIPLE DEVICES MUST  
BE THE SAME)

IF AN INCORRECT ANSWER IS TYPED ,THE PROGRAM WILL TYPE "?"  
AND WILL REPEAT THE MESSAGE OF 4.3.3.12

4.3.3.14 THE PROGRAM WILL TYPE " IS SEC XMIT SWITCH E55-2 ON? (Y OR N)-"  
AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.3.15 TYPE IN THE APPROPRIATE ANSWER YES OR NO FOLLOWED  
BY A <CARRIAGE RETURN>. (NOTE THAT ALL MULTIPLE DEVICES  
MUST BE THE SAME)

IF AN INCORRECT ANSWER IS TYPED ,THE PROGRAM WILL TYPE "?"  
AND WILL REPEAT THE MESSAGE OF 4.3.3.14

4.3.3.16 THE PROGRAM WILL TYPE "IS SEC REC SWITCH E55-3 ON?  
(Y OR N)-" AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.3.17 TYPE IN THE APPROPRIATE ANSWER YES OR NO FOLLOWED  
BY A <CARRIAGE RETURN>. (NOTE: ALL MULTIPLE DEVICES MUST BE THE SAME)

IF AN INCORRECT ANSWER IS TYPED ,THE PROGRAM WILL TYPE "?"  
AND WILL REPEAT THE MESSAGE OF 4.3.3.16

4.3.3.18 THE PROGRAM WILL TYPE "IS OPT CLR ENABLE SWITCH  
E55-1 ON? (Y OR N)-" AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.3.19 TYPE IN THE APPROPRIATE ANSWER YES OR NO FOLLOWED  
BY A <CARRIAGE RETURN>. (NOTE: ALL MULTIPLE DEVICES MUST BE THE SAME)

IF AN INCORRECT ANSWER IS TYPED ,THE PROGRAM WILL TYPE "?"  
AND WILL REPEAT THE MESSAGE OF 4.3.3.18

4.3.3.20 THE PROGRAM WILL TYPE "ARE YOU RUNNING IN MAINT.  
MODE EXTERNAL ? AND .....DO YOU HAVE THE EXTERNAL MODEM  
BYPASS JUMPER CONNECTOR ON ? (Y OR N)-" AND WAIT FOR AN  
INPUT FROM THE TELETYPE KEYBOARD

4.3.3.21 TYPE IN THE APPROPRIATE ANSWER YES OR NO FOLLOWED BY  
A <CARRIAGE RETURN>. (NOTE: ALL MULTIPLE DEVICES MUST BE THE SAME)

IF AN INCORRECT ANSWER IS TYPED ,THE PROGRAM WILL TYPE "?"  
AND WILL REPEAT THE MESSAGE OF 4.3.3.20

4.3.3.22 THE PROGRAM WILL TYPE "R" TO INDICATE THAT IT  
HAS STARTED AND WILL COMMENCE TESTING AT TEST 1

4.3.4 PROGRAM RESTART WITH SW01=1  
NOTE: THIS WILL ONLY WORK WHEN A SINGLE DEVICE IS SELECTED  
,,,IT WILL NOT WORK IF MULTIPLE DEVICES ARE SELECTED

IF MULTIPLE DEVICES WERE PREVIOUSLY SELECTED,LOAD 000200,  
AND SELECT SW00=1 AND ANSWER "NO" TO THE MULTIPLE DEVICE QUESTION  
SEE 4.3.3

4.3.4.1 SET SW01=1 IN SWITCH REG (LOC. 176)

4.3.4.2 TYPE 200G.

4.3.4.3 PROGRAM WILL START.

4.3.4.4 THE PROGRAM WILL TYPE "TEST PC-" AND WAIT FOR AN INPUT FROM  
THE TELETYPE KEYBOARD

4.3.4.5 TYPE IN THE ADDRESS OF THE TEST AT WHICH THE PROGRAM IS TO  
BE STARTED FOLLOWED BY A <CARRIAGE RETURN>

4.3.4.6 THE PROGRAM WILL TYPE "R" TO INDICATE THAT IT HAS STARTED  
TESTING AT THE SELECTED TEST

NOTE: CARE MUST BE TAKEN WHEN THIS FEATURE IS USED  
SINCE THERE IS NO PROTECTION AGAINST SELECTING AN ADDRESS  
THAT IS IN THE MIDDLE OF A TEST

4.3.5 PROGRAM RESTART WITH SW02 =1  
NOTE: THIS WILL ONLY WORK WHEN A SINGLE DEVICE IS SELECTED  
SEE NOTE IN 4.3.4 FOR MORE DETAILS

4.3.5.1 SET SW02=1 IN SWITCH REG. (LOC. 176)

4.3.5.2 TYPE 200G.

4.3.5.3 PROGRAM WILL START.

4.3.5.4 THE PROGRAM WILL TYPE "LOCK ON SELECTED TEST ? (Y OR N)-"

AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.5.5 TYPE IN THE APPROPRIATE ANSWER YES OR NO FOLLOWED BY A  
(CARRIAGE RETURN)

IF A NO ANSWER IS GIVEN: THIS LOCK ON TEST WILL BE IGNORED  
AND THE PROGRAM WILL TYPE "R" TO INDICATE THAT IT HAS STARTED  
TESTING AT TEST 1

4.3.5.6 IF A YES ANSWER WAS GIVEN: THE PROGRAM WILL ACT AS FOLLOWS...  
THE PROGRAM WILL TYPE "R" TO INDICATE THAT IT HAS STARTED  
TESTING AT TEST 1 AND WILL REMAIN IN TEST 1 UNTIL HALTED  
OR IF ANY KEY IS STRUCK ON THE TELETYPE, THE PROGRAM  
WILL FREEZE ON THE NEXT TEST UNTIL A KEY IS STRUCK ON  
THE TELETYPE AND SO FORTH THRU THE PROGRAM. IF SW01 = 1 IT  
WILL PERFORM AS IN SECTION 4.3.4 ALLOWING ONE TO FREEZE  
ON A SELECTED TEST RATHER THAN DEFAULTING TO TEST 1

## 5. OPERATING PROCEDURE

### 5.1 OPERATIONAL SWITCH SETTINGS (INTERNAL TO THE CPU, ACCESSED VIA LOC. 176).

SW15 = 1 HALT ON ERROR  
SW14 = 1 LOOP ON CURRENT TEST  
SW13 = 1 INHIBIT ERROR TYPEOUT  
SW11 = 1 INHIBIT ITERATIONS  
SW10 = 1 ESCAPE TO NEXT TEST ON ERROR  
SW09 = 1 LOOP ON ERROR  
SW02 = 1 LOCK ON TEST  
SW01 = 1 RESTART PROGRAM AT SELECTED TEST  
SW00 = 1 RESELECT VECTOR AND CONTROL REGISTER ADDRESSES  
& PARAMETERS AFTER A PROGRAM RESTART

TO INHIBIT "END OF PASS" TYPEOUT - TURN TELETYPE OFF

## 6. ERRORS

### 6.1 ERROR HALTS (UNDER LSI ALL HALT ERRORS RETURN CONTROL TO O.D.T.) THERE ARE FOUR DISTINCT ERROR TYPEOUTS

#### 6.1.1 PC+2 = ERROR PC WHERE PC +2 IS THE ADDRESS OF THE CALL TO THE ERROR HANDLER +2

REFER TO THE ABOVE "HLT" IN DIAGNOSTIC FOR ERROR DESCRIPTION

CHECK ADDRESS @ RXCSR: TO LOCATE THE DEVICE PRESENTLY UNDER  
TEST WHEN RUNNING MULTIPLE DEVICES

#### 6.1.2 PC +2 = REGISTER ERROR PC

REGISTER	EXPECTED	ACTUAL
16XXXX	YYYYYY	ZZZZZZ

WHERE 16XXXX IS THE ADDRESS OF THE FAILING DEVICE REGISTER

WHERE YYYYYY IS THE EXPECTED CONTENTS OF THAT REGISTER

WHERE ZZZZZZ IS THE ACTUAL CONTENTS OF THAT REGISTER



- 6.1.3 PC +2 = RECEIVER ERROR PC  
REGISTER                      EXPECTED                      ACTUAL  
16XXXX                      YYYYYY                      ZZZZZZ
- WHERE 16XXXX IS THE ADDRESS OF THE FAILING RECEIVER (RXDBUF) REGISTER  
WHERE YYYYYY IS THE EXPECTED DATA CONTENTS OF THAT REGISTER  
WHERE ZZZZZZ IS THE ACTUAL DATA CONTENTS OF THAT REGISTER
- 6.1.4 PC +2 = TRANSMITTER ERROR PC  
REGISTER                      EXPECTED                      ACTUAL  
16XXXX                      YYYYYY                      ZZZZZZ
- WHERE 16XXXX IS THE ADDRESS OF THE FAILING TRANSMITTER (TXCSR) REGISTER  
WHERE YYYYYY IS THE EXPECTED CONTENTS OF THAT REGISTER  
WHERE ZZZZZZ IS THE ACTUAL CONTENTS OF THAT REGISTER
- 6.1.5 ERROR DESCRIPTIONS  
SEE LISTINGS FOR DETAILS OF ERRORS
- 6.2 ERROR RECOVERY
- 6.2.1 SW15 =0  
IF THE PROGRAM IS RUN WITH SW15 =0 ,NO OPERATOR ACTION IS  
REQUIRED TO CONTINUE TESTING
- 6.2.2 SW15 =1  
IF THE PROGRAM IS RUN WITH SW15 =1 ,TO CONTINUE TESTING  
AFTER THE PROGRAM HAS HALTED ,PRESS THE PROCESSOR  
CONSOLE "CONTINUE SWITCH"
- NOTE: THE PC + 2 OF THE "HLT" WILL BE DISPLAYED IN THE DATA LIGHTS
- 6.2.3 ILLEGAL INTERRUPTS  
IF AN INTERRUPT OCCURS TO A VECTOR ADDRESS NOT SELECTED  
DURING PROGRAM INITIALIZATION, THE PROGRAM WILL HALT IN  
THE TRAPCATCHER. THE ADDRESS AT WHICH THE PROGRAM  
HALTS IS 2 GREATER THAN THE ADDRESS TO WHICH THE INTERRUPT  
OCCURED. THE PROGRAM MUST BE RESTARTED AT 000200 TO  
RECOVER FROM THIS ERROR.
- 6.2.4 ADDITIONAL TROUBLESHOOTING AIDS    ERRCNT: & PASCNT:  
CHECK THESE TWO TAG LOCATIONS FOR TOTAL # OF ERRORS AND PASSES RESPECTIVELY.  
LOADING 000200 AND RESTARTING WILL CLEAR THESE LOCATIONS.
- 6.3 END OF PASS ROUTINE  
THIS TYPEOUT IS MENTIONED HERE FOR CONVENIENCE  
IT IS IN THE FORM:
- END OF PASS TAPE Y  
16XXXX = DEVICE

WHERE Y IS THE TAPE LOADED

WHERE 16XXXX IS THE DEVICE'S BASE REGISTER ADDRESS

TO INHIBIT THIS TYPEOUT - TURN TELETYPE OFF

7. RESTRICTIONS

7.1 MULTIPLE DEVICES  
 UP TO 16(10) DEVICES MAY BE TESTED. HOWEVER, THEY  
 MUST HAVE CONTIGUOUS ADDRESSES AND VECTORS

NOTE: IF ALL DEVICES UNDER TEST HAVE THE SAME INTERRUPT VECTOR  
 YOU CAN CHANGE "ZERO: ADD #10, BASEIV ;NEXT BLOCK  
 (VECTORS)" TO "ZERO: ADD #0, BASEIV";  
 THEREBY THE VECTOR ADDRESSES WILL NOT BE  
 UPDATED AFTER EACH PASS.

7.2 DISQUALIFYING DEVICES WHEN RUNNING MULTIPLE DEVICES

WHEN RUNNING MULTIPLE DEVICES AN ACTIVE BIT IS SET  
 FOR EACH DEVICE RUNNING UNDER TEST IE. BIT 0 FOR  
 DEVICE 0 BIT 15 FOR DEVICE 15  
 TO DISQUALIFY DEVICES:

7.2.1 IF DEVICE 0 IS TO BE DISQUALIFIED, SIMPLY RESTART  
 PROGRAM WITH SW00 =1 AND OMIT THE FIRST DEVICE.

7.2.2 IF HOWEVER, DEVICES 1 THRU 15 OR ANY COMBINATION THEREOF  
 ARE TO BE DISQUALIFIED....LOAD THE LOCATION OF ACTREG:  
 OBSERVE THE ACTIVE BITS (ACTIVE =1, NONACTIVE = 0)  
 AND DEPOSIT 0 WHERE THOSE DEVICES ARE TO BE DISQUALIFIED

7.2.2.1 TO RESTART...TYPE 200G...  
 THE PROGRAM WILL CONTINUE WITH THE DEVICE IT WAS IN BEFORE HALTING.

7.2.2.2 .....OR .....SET SW00=1 IN SWITCH REG (LOC. 176) AND TYPE 200G....  
 ANSWER THE QUESTION :1ST DEVICE : ETC.....  
 ....THE PROGRAM WILL CONTINUE WITH DEVICE 0

7.2.2.3 IF ALL DEVICES ARE DISQUALIFIED BY MISTAKE THE PROGRAM  
 WILL TYPEOUT AN ERROR MESSAGE.....TYPE 200G.

7.3 CABLE DELAYS

NOTE: EXTERNAL LOOP BACK TESTS ONLY (MODEM CABLE WITH H315 CONNECTOR ON)

7.3.1 TO PROVIDE SUFFICIENT DELAY FOR CLOCK SIGNAL OVER THE CABLE,  
 LOCATION "HOLD:" MUST BE MODIFIED TO ACCOMODATE FOR FASTER MACHINES.  
 PRESENTLY "HOLD:" =20 IS SUFFICIENT TIME ON AN 11/03 MACHINE.

BASICALLY DON'T TRY TO EXCEED 10K TO 12K RATE USING THE EIA DRIVERS

7.4 TO USE THE "XOR" TESTER, THE BRANCH AROUND THE "XOR"  
 CODE MUST BE PATCHED TO A "NOP". (SEE LISTINGS FOR DETAILS)

8. DEFAULT PARAMETERS:  
 1ST DEVICE: RECEIVER CONTROL REGISTER ADDRESS- RXCSR: 160010  
 VECTOR ADDRESS- DURIV: 770  
 ARE YOU RUNNING MULTIPLE DEVICES ?- NO MULTD: 0  
 LAST DEVICE: RECEIVER CONTROL REGISTER ADDRESS- LASTADD: 0  
 # OF SYNC CHARS SELECTED - 2 SYNC#0: 377  
 IS SEC XMIT SWITCH E55-2 ON?- YES SEXMIT: 377  
 IS SEC REC SWITCH E55-3 ON?- YES SEREC: 377  
 IS OPT CLR ENABLE SWITCH E55-1 ON?- YES OPTCLR: 377  
 DO YOU HAVE THE EXTERNAL MODEM BYPASS JUMPER  
 CONNECTOR ON (H315)- YES JMRBY: 377

9. PROGRAM DESCRIPTION

9.1 THIS PROGRAM PERFORMS THE OFFLINE LOGIC BIT BANGING  
 OF THE DEVICE  
 SEE LISTING FOR DETAILS

10. FLOW CHARTS: RECEIVER FLOW, TRANSMITTER FLOW, TRANSMITTER & RECEIVER FLOW

11. LISTINGS

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DZDU0-A MACY11 27(1006) 03-FEB-77 07:44 PAGE 12  
DZDU02.M11 27-JAN-77 09:45

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STN=1

# MO1

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 DZDUQA.M11 27-JAN-77 09:46

## APT COMMUNICATIONS ROUTINE

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000340  
  
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.ENABLE ABS

;DUV11 DZDUQ-A TAPE A
;COPYRIGHT 1977, DIGITAL EQUIPMENT CORP., MAYNARD, MASS. 01754

;STARTING PROCEDURE
;TYPE 200G
;PROGRAM WILL TYPE "DUV11 DZDUQ-A TAPE A"
;PROGRAM WILL TYPE "R" TO INDICATE THAT TESTING HAS STARTED
;AT THE END OF A PASS, PROGRAM WILL TYPE "END OF PASS TAPE A"
;AND THEN RESUME TESTING

.SBTTL BASIC DEFINITIONS

;#INITIAL ADDRESS OF THE STACK POINTER *** 1100 ***
STACK= 1100
.EQUIV EMT,ERROR      ;;BASIC DEFINITION OF ERROR CALL
.EQUIV IOT,SCOPE      ;;BASIC DEFINITION OF SCOPE CALL

;#MISCELLANEOUS DEFINITIONS
MT= 11                ;;CODE FOR HORIZONTAL TAB
LF= 12                ;;CODE FOR LINE FEED
CR= 15                ;;CODE FOR CARRIAGE RETURN
CRLF= 200             ;;CODE FOR CARRIAGE RETURN-LINE FEED
PS= 177776           ;;PROCESSOR STATUS WORD
.EQUIV PS,PSW
STKLMT= 177774        ;;STACK LIMIT REGISTER
PIRQ= 177772          ;;PROGRAM INTERRUPT REQUEST REGISTER
DSWR= 177570          ;;HARDWARE SWITCH REGISTER
DDISP= 177570         ;;HARDWARE DISPLAY REGISTER

;#GENERAL PURPOSE REGISTER DEFINITIONS
R0= %0                ;;GENERAL REGISTER
R1= %1                ;;GENERAL REGISTER
R2= %2                ;;GENERAL REGISTER
R3= %3                ;;GENERAL REGISTER
R4= %4                ;;GENERAL REGISTER
R5= %5                ;;GENERAL REGISTER
R6= %6                ;;GENERAL REGISTER
R7= %7                ;;GENERAL REGISTER
SP= %6                ;;STACK POINTER
PC= %7                ;;PROGRAM COUNTER

;#PRIORITY LEVEL DEFINITIONS
PR0= 0                ;;PRIORITY LEVEL 0
PR1= 40               ;;PRIORITY LEVEL 1
PR2= 100              ;;PRIORITY LEVEL 2
PR3= 140              ;;PRIORITY LEVEL 3
PR4= 200              ;;PRIORITY LEVEL 4
PR5= 240              ;;PRIORITY LEVEL 5
PR6= 300              ;;PRIORITY LEVEL 6
PR7= 340              ;;PRIORITY LEVEL 7

;#"SWITCH REGISTER" SWITCH DEFINITIONS
SW15= 100000
SW14= 40000

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612 020000  
 613 010000  
 614 004000  
 615 002000  
 616 001000  
 617 000400  
 618 000200  
 619 000100  
 620 000040  
 621 000020  
 622 000010  
 623 000004  
 624 000002  
 625 000001  
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 640 020000  
 641 010000  
 642 004000  
 643 002000  
 644 001000  
 645 000400  
 646 000200  
 647 000100  
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 666 000004  
 667 000010

SW13= 20000  
 SW12= 10000  
 SW11= 4000  
 SW10= 2000  
 SW09= 1000  
 SW08= 400  
 SW07= 200  
 SW06= 100  
 SW05= 40  
 SW04= 20  
 SW03= 10  
 SW02= 4  
 SW01= 2  
 SW00= 1  
 .EQUIV SW09, SW9  
 .EQUIV SW08, SW8  
 .EQUIV SW07, SW7  
 .EQUIV SW06, SW6  
 .EQUIV SW05, SW5  
 .EQUIV SW04, SW4  
 .EQUIV SW03, SW3  
 .EQUIV SW02, SW2  
 .EQUIV SW01, SW1  
 .EQUIV SW00, SW0

.\*DATA BIT DEFINITIONS (BIT00 TO BIT15)

BIT15= 100000  
 BIT14= 40000  
 BIT13= 20000  
 BIT12= 10000  
 BIT11= 4000  
 BIT10= 2000  
 BIT09= 1000  
 BIT08= 400  
 BIT07= 200  
 BIT06= 100  
 BIT05= 40  
 BIT04= 20  
 BIT03= 10  
 BIT02= 4  
 BIT01= 2  
 BIT00= 1  
 .EQUIV BIT09, BIT9  
 .EQUIV BIT08, BIT8  
 .EQUIV BIT07, BIT7  
 .EQUIV BIT06, BIT6  
 .EQUIV BIT05, BIT5  
 .EQUIV BIT04, BIT4  
 .EQUIV BIT03, BIT3  
 .EQUIV BIT02, BIT2  
 .EQUIV BIT01, BIT1  
 .EQUIV BIT00, BIT0

.\*BASIC "CPU" TRAP VECTOR ADDRESSES

ERRVEC= 4 ;: TIME OUT AND OTHER ERRORS  
 RESVEC= 10 ;: RESERVED AND ILLEGAL INSTRUCTIONS



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668	000014	TBITVEC=14	:: "T" BIT
669	000014	TRTVEC= 14	:: TRACE TRAP
670	000014	BPTVEC= 14	:: BREAKPOINT TRAP (BPT)
671	000020	IOTVEC= 20	:: I/O OUTPUT TRAP (IOT) **SCOPE**
672	000024	PRRVEC= 24	:: POWER FAIL
673	000030	EMTVEC= 30	:: EMULATOR TRAP (EMT) **ERROR**
674	000034	TRAPVEC=34	:: "TRAP" TRAP
675	000060	TKVEC= 60	:: TTY KEYBOARD VECTOR
676	000064	TPVEC= 64	:: TTY PRINTER VECTOR
677	000240	PIRQVEC=240	:: PROGRAM INTERRUPT REQUEST VECTOR

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;STANDARD INTERRUPT VECTORS
678
679
680
681      000174      000174      .=174
682      000174      000000      DISPREG:0
683      000176      000000      SWREG:0
684      000200      000200      .=200
685      000200      000167      001746      JMP      .START      ;GO TO START OF PROGRAM
686
687
688
689      001100      001100      .=1100
690      001100      000000      .WORD 0
691      001102      177570      LIGHTS:177570
692
693
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705
706      001104      000000      RETURN: 0
707      001106      000000      NEXT: 0      ;ADDRESS OF NEXT TEST TO BE EXECUTED
708      001110      000000      LOCK: 0      ;ADDRESS FOR LOCK ON CURRENT DATA
709      001112      000000      PASCNT: 0      ;ADDRESS CONTAINING PASS COUNT
710      001114      000000      ERRCNT: 0      ;ERROR COUNT
711      001116      000000      SAVSP: 0      ;STACK POINTER STORAGE
712
713
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717
;PROGRAM VARIABLES
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```

718 ;PROGRAM CONVERSATIONAL PARAMETERS
719 001146 377 SYNCNO: .BYTE 377 ;# OF SYNC CHARS REQ'D FOR SYNC'ZATION
720 001147 377 SEXMIT: .BYTE 377 ;SEC XMIT JUMPER "IN"
721 001150 377 SEREC: .BYTE 377 ;SEC REC JUMPER "IN"
722 001151 377 OPTCLR: .BYTE 377 ;OPTIONAL JUMPER CLR "IN"
723 001152 000 MULTD: .BYTE 0 ;NO MULTIPLE DEVICE FLAG
724 001153 377 JMRBY: .BYTE 377 ;EXTERNAL MODEM BYPASS JUMPER "IN"
725 .EVEN
726
727 ;PROGRAM MULTIPLE DEVICE PARAMETERS
728 001154 000000 BASEADD: 0 ;PROG CONTROLLED 1ST DEVICE ADDR
729 001156 000000 KEEPADD: 0 ;SAVED 1ST DEVICE ADDR
730 001160 000000 LASTADD: 0 ;LAST DEVICE RXCSR ADDR
731 001162 000000 BASEIV: 0 ;PROG CONTROLLED IV
732 001164 000000 KEEPIV: 0 ;SAVED INTR VECTOR
733 001166 000000 ACTREG: 0 ;ACTIVE REGISTER, MODIFY THIS
734 ;LOCATION TO DISQUALIFY OR QUALIFY
735 ;DEVICES (1= RUN, 0= DON'T RUN)
736 001170 000000 ROTADD: 0 ;ROTATING POINTER FOR ACTREG..POINTS
737 ;TO DEVICE PRESENTLY UNDER TEST WHEN RUNNING MULTIPLE DEVICES
738
739 ;PROGRAM CONTROL FLAGS
740
741 001172 000 INIFLG: .BYTE 0 ;PROGRAM INITIALIZATION FLAG
742 001173 000 STFLG: .BYTE 0 ;TEST START FLAG
743 001174 000 LOKFLG: .BYTE 0 ;LOCK ON CURRENT TEST FLAG
744 001176 .EVEN
745 001400 .=1400
746
747

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749
750
751 ;INSTRUCTION DEFINITIONS
752
753 005746 PUSH1SP=5746 ; DECREMENT PROCESSOR STACK 1 WORD =TST -(SP)
754 005726 POP1SP=5726 ; INCREMENT PROCESSOR STACK 1 WORD =TST (SP)+
755 010046 PUSHRO=10046 ; SAVE RO ON STACK =MOV RO, -(SP)
756 012600 POPRO=12600 ; RESTORE RO FROM STACK =MOV (SP)+, RO
757 024646 PUSH2SP=24646 ; DECREMENT STACK TWICE =CMP -(SP), -(SP)
758 022626 POP2SP=22626 ; INCREMENT STACK TWICE =CMP (SP)+, (SP)+
759 ;REGISTER DEFINITIONS
760 ;RXCSR BIT DEFINITIONS
761 100000 DSC=BIT15 ; DATA SET CHANGE
762 040000 RING=BIT14 ; RING
763 020000 CTS=BIT13 ; CLR TO SEND
764 010000 CARDET=BIT12 ; CARRIER DETECT
765 004000 RECACT=BIT11 ; REC ACTIVE
766 002000 SRD=BIT10 ; SEC REC DATA
767 001000 DSR=BIT9 ; DATA SET RDY
768 000400 STPSYN=BIT8 ; STRIP SYNC
769 000200 RXDONE=BIT7 ; REC DONE
770 000100 RINTEN=BIT6 ; REC INTR ENABLE
771 000040 DSINTE=BIT5 ; DSC INTR ENABLE
772 000020 SYNSCH=BIT4 ; SYNC SEARCH
773 000010 STD=BIT3 ; SEC XMIT DATA
774 000004 RTS=BIT2 ; REQ TO SEND
775 000002 DTR=BIT1 ; DATA TERM RDY
776 000001 VOID=BIT0
777 ;RXDBUF BIT DEFINITIONS
778 100000 RXERR=BIT15 ; REC ERROR
779 040000 OVRUN=BIT14 ; OVERRUN
780 020000 FRMERR=BIT13 ; FRAME ERROR
781 010000 PARER=BIT12 ; PARITY ERROR
782 ;PARCSR BIT DEFINITIONS
783 001000 PAREN=BIT9 ; PARITY ENABLE
784 000400 EVPAR=BIT8 ; EVEN PARITY SENSE
785 ;PARCSR WRD DEFINITIONS
786 030000 SYNINT=30000 ; SYNC EXTERNAL MODE
787 020000 SYNEXT=20000 ; SYNC INTERNAL MODE
788 000000 ISYM00=0 ; ISOC MODE
789 000000 FIVE=0 ; WORD LENGTH 5 BITS
790 002000 SIX=2000 ; WORD LENGTH 6 BITS
791 004000 SEVEN=4000 ; WORD LENGTH 7 BITS
792 006000 EIGHT=6000 ; WORD LENGTH 8 BITS
793 000000 NOPAR=0 ; NO PARITY
794 001000 ODDPAR=1000 ; ODD PARITY
795 001400 EVEPAR=1400 ; EVEN PARITY
796 ;TXCSR BIT DEFINITIONS
797 100000 DNA=BIT15 ; DATA NOT AVAILABLE
798 040000 MTDATA=BIT14 ; MAINT DATA
799 020000 CLK=BIT13 ; CLK
800 002000 BITW=BIT10 ; BIT WINDOW
801 000400 MRESET=BIT8 ; MASTER RESET
802 000200 TXDONE=BIT7 ; XMIT DONE
803 000100 TXINTE=BIT6 ; XMIT INTR ENABLE

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804	000040	DNAINTE=BITS	;DNA INTR ENAB
805	000020	SENC=BIT4	;SEND
806	000010	HDXEN=BIT3	;HDX/FDX
807	000001	BREAK=BIT0	;BREAK
808		;TXCSR WRD DEFINITIONS	
809	000000	USER=0	;USER MODE
810	004000	MINT=4000	;MAINT INT MODE
811	010000	MEXT=10000	;MAINT EXT MODE
812	014000	SYSTST=14000	;SYSTEM TEST MODE

813  
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815  
816  
817  
818  
819 001400  
820 001400  
821 001400 000000  
822 001402 000  
823 001403 000  
824 001404 000000  
825 001406 000000  
826 001410 000000  
827 001412 000000  
828 001414 000  
829 001415 001  
830 001416 000000  
831 001420 000000  
832 001422 000000  
833 001424 000000  
834 001426 000000  
835 001430 000000  
836 001432 000000  
837 001434 000  
838 001435 000  
839 001436 000000  
840 001440 177570  
841 001442 177570  
842 001444 177560  
843 001446 177562  
844 001450 177564  
845 001452 177566  
846 001454 000  
847 001455 002  
848 001456 012  
849 001457 000  
850 001460 000000  
851  
852 001462 000000  
853 001464 000000  
854 001466 000000  
855 001470 000000  
856 001472 000000  
857 001474 000000  
858 001476 000000  
859 001500 000000  
860 001502 000000  
861 001504 000000  
862 001506 000000  
863 001510 000000  
864 001512 000000  
865 001514 000000  
866 001516 177607 000377  
867 001522 077  
868 001523 015

.SBTTL COMMON TAGS

\*\*\*\*\*  
\*THIS TABLE CONTAINS VARIOUS COMMON STORAGE LOCATIONS  
\*USED IN THE PROGRAM.

SCMTAG: =.

STSTNM: .WORD 0  
SERFLG: .BYTE 0  
SICNT: .WORD 0  
SLPADR: .WORD 0  
SLPERR: .WORD 0  
SERTTL: .WORD 0  
SITEMB: .BYTE 0  
SERMAX: .BYTE 1  
SERRPC: .WORD 0  
SGDADR: .WORD 0  
SBDADR: .WORD 0  
SGDAT: .WORD 0  
SBDAT: .WORD 0  
SAUTOB: .BYTE 0  
SINTAG: .BYTE 0  
SWR: .WORD DSWR  
DISPLAY: .WORD DDISP  
STKS: 177560  
STKB: 177562  
STPS: 177564  
STPB: 177566  
\$NULL: .BYTE 0  
\$FILLS: .BYTE 2  
\$FILLC: .BYTE 12  
STPFLG: .BYTE 0  
SREGAD: .WORD 0  
SREG0: .WORD 0  
SREG1: .WORD 0  
SREG2: .WORD 0  
SREG3: .WORD 0  
SREG4: .WORD 0  
SREG5: .WORD 0  
STMP0: .WORD 0  
STMP1: .WORD 0  
STMP2: .WORD 0  
STMP3: .WORD 0  
STMP4: .WORD 0  
STMP5: .WORD 0  
STIMES: 0  
\$ESCAPE: 0  
\$BELL: .ASCIZ <207><377><377>  
\$QUES: .ASCII /?  
\$CRLF: .ASCII <15>

:: START OF COMMON TAGS

:: CONTAINS THE TEST NUMBER  
:: CONTAINS ERROR FLAG  
:: CONTAINS SUBTEST ITERATION COUNT  
:: CONTAINS SCOPE LOOP ADDRESS  
:: CONTAINS SCOPE RETURN FOR ERRORS  
:: CONTAINS TOTAL ERRORS DETECTED  
:: CONTAINS ITEM CONTROL BYTE  
:: CONTAINS MAX. ERRORS PER TEST  
:: CONTAINS PC OF LAST ERROR INSTRUCTION  
:: CONTAINS ADDRESS OF 'GOOD' DATA  
:: CONTAINS ADDRESS OF 'BAD' DATA  
:: CONTAINS 'GOOD' DATA  
:: CONTAINS 'BAD' DATA  
:: RESERVED--NOT TO BE USED  
  
:: AUTOMATIC MODE INDICATOR  
:: INTERRUPT MODE INDICATOR  
  
:: ADDRESS OF SWITCH REGISTER  
:: ADDRESS OF DISPLAY REGISTER  
:: TTY KBD STATUS  
:: TTY KBD BUFFER  
:: TTY PRINTER STATUS REG. ADDRESS  
:: TTY PRINTER BUFFER REG. ADDRESS  
:: CONTAINS NULL CHARACTER FOR FILLS  
:: CONTAINS # OF FILLER CHARACTERS REQUIRED  
:: INSERT FILL CHARS. AFTER A "LINE FEED"  
:: "TERMINAL AVAILABLE" FLAG (BIT<07>=0=YES)  
:: CONTAINS THE ADDRESS FROM  
:: WHICH (SREG0) WAS OBTAINED  
:: CONTAINS ((SREGAD)+0)  
:: CONTAINS ((SREGAD)+2)  
:: CONTAINS ((SREGAD)+4)  
:: CONTAINS ((SREGAD)+6)  
:: CONTAINS ((SREGAD)+10)  
:: CONTAINS ((SREGAD)+12)  
:: USER DEFINED  
:: USER DEFINED  
:: USER DEFINED  
:: USER DEFINED  
:: USER DEFINED  
:: USER DEFINED  
:: MAX. NUMBER OF ITERATIONS  
:: ESCAPE ON ERROR ADDRESS  
:: CODE FOR BELL  
:: QUESTION MARK  
:: CARRIAGE RETURN

869 001524 000012  
870  
871  
872  
873  
874  
875 001526  
876 001526 000000  
877 001530 000000  
878 001532 000000  
879 001534 000000  
880 001536 000000  
881 001540 000000  
882 001542 000000  
883 001544 000000  
884 001546  
885 001546 000  
886 001547 000  
887 001550 000000  
888 001552 000000  
889 001554 000000  
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896 001556 000  
897 001557 000  
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902 001560 000000  
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904 001562 000  
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906 001564 000000  
907 001566 000  
908 001567 000  
909 001570 000000  
910 001572 000  
911 001573 000  
912 001574 000000  
913 001576 000000  
914 001600 000000  
915 001602 000000  
916 001604 000000  
917 001606 000000  
918 001610 000000  
919 001612 000000  
920 001614 000000  
921 001616 000000  
922 001620 000000  
923 001622 000000  
924 001624 000000

SLF: .ASCIZ <12> ;:LINE FEED  
:\*\*\*\*\*  
:SBTTL APT MAILBOX-ETABLE  
:\*\*\*\*\*  
:EVEN  
\$MAIL: ;:APT MAILBOX  
\$MSGTY: .WORD AMSGTY ;:MESSAGE TYPE CODE  
\$FATAL: .WORD AFATAL ;:FATAL ERROR NUMBER  
\$TESTN: .WORD ATESTN ;:TEST NUMBER  
\$PASS: .WORD APASS ;:PASS COUNT  
\$DEVCT: .WORD ADEVCT ;:DEVICE COUNT  
\$UNIT: .WORD AUNIT ;:I/O UNIT NUMBER  
\$MSGAD: .WORD AMSGAD ;:MESSAGE ADDRESS  
\$MSGLG: .WORD AMSGLG ;:MESSAGE LENGTH  
\$ETABLE: ;:APT ENVIRONMENT TABLE  
\$ENV: .BYTE AENV ;:ENVIRONMENT BYTE  
\$ENVN: .BYTE AENVN ;:ENVIRONMENT MODE BITS  
\$SWREG: .WORD ASWREG ;:APT SWITCH REGISTER  
\$USWR: .WORD AUSWR ;:USER SWITCHES  
\$CPUOP: .WORD ACPUOP ;:CPU TYPE, OPTIONS  
BITS 15-11=CPU TYPE  
11/04=01, 11/05=02, 11/20=03, 11/40=04, 11/45=05  
11/70=06, PDQ=07, Q=10  
BIT 10=REAL TIME CLOCK  
BIT 9=FLOATING POINT PROCESSOR  
BIT 8=MEMORY MANAGEMENT  
\$MAMS1: .BYTE AMAMS1 ;:HIGH ADDRESS, M.S. BYTE  
\$MTYP1: .BYTE AMTYP1 ;:MEM. TYPE, BLK#1  
MEM. TYPE BYTE -- (HIGH BYTE)  
900 NSEC CORE=001  
300 NSEC BIPOLAR=002  
500 NSEC MOS=003  
\$MADR1: .WORD AMADR1 ;:HIGH ADDRESS, BLK#1  
MEM. LAST ADDR. #3 BYTES, THIS WORD AND LOW OF "TYPE" ABOVE  
\$MAMS2: .BYTE AMAMS2 ;:HIGH ADDRESS, M.S. BYTE  
\$MTYP2: .BYTE AMTYP2 ;:MEM. TYPE, BLK#2  
\$MADR2: .WORD AMADR2 ;:MEM. LAST ADDRESS, BLK#2  
\$MAMS3: .BYTE AMAMS3 ;:HIGH ADDRESS, M.S. BYTE  
\$MTYP3: .BYTE AMTYP3 ;:MEM. TYPE, BLK#3  
\$MADR3: .WORD AMADR3 ;:MEM. LAST ADDRESS, BLK#3  
\$MAMS4: .BYTE AMAMS4 ;:HIGH ADDRESS, M.S. BYTE  
\$MTYP4: .BYTE AMTYP4 ;:MEM. TYPE, BLK#4  
\$MADR4: .WORD AMADR4 ;:MEM. LAST ADDRESS, BLK#4  
\$VECT1: .WORD AVECT1 ;:INTERRUPT VECTOR#1, BUS PRIORITY#1  
\$VECT2: .WORD AVECT2 ;:INTERRUPT VECTOR#2, BUS PRIORITY#2  
\$BASE: .WORD ABASE ;:BASE ADDRESS OF EQUIPMENT UNDER TEST  
\$DEVN: .WORD ADEVN ;:DEVICE MAP  
\$CDW1: .WORD ACDW1 ;:CONTROLLER DESCRIPTION WORD#1  
\$CDW2: .WORD ACDW2 ;:CONTROLLER DESCRIPTION WORD#2  
\$DDW0: .WORD ADDW0 ;:DEVICE DESCRIPTOR WORD#0  
\$DDW1: .WORD ADDW1 ;:DEVICE DESCRIPTOR WORD#1  
\$DDW2: .WORD ADDW2 ;:DEVICE DESCRIPTOR WORD#2  
\$DDW3: .WORD ADDW3 ;:DEVICE DESCRIPTOR WORD#3  
\$DDW4: .WORD ADDW4 ;:DEVICE DESCRIPTOR WORD#4  
\$DDW5: .WORD ADDW5 ;:DEVICE DESCRIPTOR WORD#5



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000400  
000200  
000100

; INSTRUCTION DEFINITIONS

PUSH1SP=5746 ; DECREMENT PROCESSOR STACK 1 WORD =TST -(SP)  
 POP1SP=5726 ; INCREMENT PROCESSOR STACK 1 WORD =TST (SP)+  
 PUSHRO=10046 ; SAVE RO ON STACK =MOV RO, -(SP)  
 POPRO=12600 ; RESTORE RO FROM STACK =MOV (SP)+, RO  
 PUSH2SP=24646 ; DECREMENT STACK TWICE =CMP -(SP), -(SP)  
 POP2SP=22626 ; INCREMENT STACK TWICE =CMP (SP)+, (SP)+

; REGISTER DEFINITIONS

; RXCSR BIT DEFINITIONS  
 DSC=BIT15 ; DATA SET CHANGE  
 RING=BIT14 ; RING  
 CTS=BIT13 ; CLR TO SEND  
 CARDET=BIT12 ; CARRIER DETECT  
 REACT=BIT11 ; REC ACTIVE  
 SRD=BIT10 ; SEC REC DATA  
 DSR=BIT9 ; DATA SET RDY  
 STPSYN=BIT8 ; STRIP SYNC  
 RXDONE=BIT7 ; REC DONE  
 RINTEN=BIT6 ; REC INTR ENABLE  
 DSINTE=BIT5 ; DSC INTR ENABLE  
 SYNCH=BIT4 ; SYNC SEARCH  
 STD=BIT3 ; SEC XMIT DATA  
 RTS=BIT2 ; REQ TO SEND  
 DTR=BIT1 ; DATA TERM RDY  
 VOID=BIT0

; RXDBUF BIT DEFINITIONS

RXERR=BIT15 ; REC ERROR  
 OVRUN=BIT14 ; OVERRUN  
 FRM=BIT13 ; FRAME ERROR  
 PARERR=BIT12 ; PARITY ERROR

; PARCSR BIT DEFINITIONS

PAREN=BIT9 ; PARITY ENABLE  
 EVPAR=BIT8 ; EVEN PARITY SENSE

; PARCSR WRD DEFINITIONS

SYNINT=30000 ; SYNC EXTERNAL MODE  
 SYNEXT=20000 ; SYNC INTERNAL MODE  
 ISYMOD=0 ; ISOC MODE  
 FIVE=0 ; WORD LENGTH 5 BITS  
 SIX=2000 ; WORD LENGTH 6 BITS  
 SEVEN=4000 ; WORD LENGTH 7 BITS  
 EIGHT=6000 ; WORD LENGTH 8 BITS  
 NOPAR=0 ; NO PARITY  
 ODDPAR=1000 ; ODD PARITY  
 EVEPAR=1400 ; EVEN PARITY

; TXCSR BIT DEFINITIONS

DNA=BIT15 ; DATA NOT AVAILABLE  
 MTDATA=BIT14 ; MAINT DATA  
 CLK=BIT13 ; CLK  
 BITW=BIT10 ; BIT WINDOW  
 MRESET=BIT8 ; MASTER RESET  
 TXDONE=BIT7 ; XMIT DONE  
 TXINTE=BIT6 ; XMIT INTR ENABLE



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997	000040	DNAINTE=BIT5	;DNA INTR ENAB
998	000020	SEND=BIT4	;SEND
999	000010	HDXEN=BIT3	;HDX/FDX
1000	000001	BREAK=BIT0	;BREAK
1001		;TXCSR WRD DEFINITIONS	
1002	000000	USER=0	;USER MODE
1003	004000	MINT=4000	;MAINT INT MODE
1004	010000	MEXT=10000	;MAINT EXT MODE
1005	014000	SYSTST=14000	;SYSTEM TEST MODE

.SBTTL ERROR POINTER TABLE

;\*THIS TABLE CONTAINS THE INFORMATION FOR EACH ERROR THAT CAN OCCUR.  
;\*THE INFORMATION IS OBTAINED BY USING THE INDEX NUMBER FOUND IN  
;\*LOCATION SITEMB. THIS NUMBER INDICATES WHICH ITEM IN THE TABLE IS PERTINENT.  
;\*NOTE1: IF SITEMB IS 0 THE ONLY PERTINENT DATA IS (SERRPC).  
;\*NOTE2: EACH ITEM IN THE TABLE CONTAINS 4 POINTERS EXPLAINED AS FOLLOWS:

;\* EM ;; POINTS TO THE ERROR MESSAGE  
;\* DH ;; POINTS TO THE DATA HEADER  
;\* DT ;; POINTS TO THE DATA  
;\* DF ;; POINTS TO THE DATA FORMAT

SERRTB:

;ERROR TABLE

EM1 ;ERROR 1 REGISTER ERROR  
DH1  
DT1  
DF1  
EM2 ;ERROR 2 RECEIVER ERROR  
DH1  
DT1  
DF1  
EM3 ;ERROR 3 TRANSMITTER ERROR  
DH1  
DT1  
DF1  
EM4 ;ERROR 4 BIT ERROR (GENERAL)  
0  
DT4  
DF1

;DEFAULT DU ADDRESSES

RXCSR: 160010  
HRXCSR: 160011  
RXTXCF: 160012  
HRCLCF: 160013  
PPCSR: 160012  
HPANSR: 160013  
TXCSR: 160014  
HTXCSR: 160015  
TXDBUF: 160016  
HTXDBUF: 160017

;DEFAULT DU VECTORS

DURIV: 770 ;REC INTR VECTOR  
DURIS: 772 ;REC INTR STATUS  
DUTIV: 774 ;XMIT INTR VECTOR  
DUTIS: 776 ;XMIT INTR STATUS

;ERROR MESSAGES

EM4: .ASCIZ / ERROR PC /  
EM1: .ASCIZ / COMPARISON ERROR ON REGISTERS/

1006  
1007  
1008  
1009  
1010  
1011  
1012  
1013  
1014  
1015  
1016  
1017  
1018  
1019  
1020 001652  
1021  
1022 001652 001762  
1023 001654 002067  
1024 001656 002116  
1025 001660 002132  
1026 001662 002022  
1027 001664 002067  
1028 001666 002116  
1029 001670 002132  
1030 001672 002043  
1031 001674 002067  
1032 001676 002116  
1033 001700 002132  
1034 001702 001746  
1035 001704 000000  
1036 001706 002126  
1037 001710 002132  
1038  
1039  
1040 001712 160010  
1041 001714 160011  
1042 001716 160012  
1043 001720 160013  
1044 001722 160012  
1045 001724 160013  
1046 001726 160014  
1047 001730 160015  
1048 001732 160016  
1049 001734 160017  
1050  
1051 001736 000770  
1052 001740 000772  
1053 001742 000774  
1054 001744 000776  
1055  
1056 001746 020040 051105 047522  
1057 001754 020122 041520 000040  
1058 001762 020040 047503 050115  
1059 001770 051101 051511 047117  
1060 001776 042440 051122 051117  
1061 002004 047440 020116 042522

# M02

DZDU0-A MACY11 27(1006) 03-FEB-77 07:44 PAGE 27  
 DZDU0A.M11 27-JAN-77 09:46 ERROR POINTER TABLE

1062	002012	044507	052123	051105	
1063	000020	000123			
1064	000032	020040	042522	042503	EM2: .ASCIZ / RECEIVER ERROR/
1065	000030	053111	051105	042440	
1066	000036	051122	051117	000	
1067	000043	040	052040	040522	EM3: .ASCIZ / TRANSMITTER ERROR/
1068	002050	051516	044515	052124	
1069	002056	051105	042440	051122	
1070	002064	051117	000		
1071					;DATA HEADERS FOR ERROR MESSAGES
1072	002067	105	051122	041520	DH1: .ASCIZ /ERRPC WANTED ACTUAL/
1073	002074	020040	040527	052116	
1074	002102	042105	020040	041501	
1075	002110	052524	046101	000	
1076		002116			.EVEN
1077					;DATA TABLES FOR ERROR MESSAGES
1078	002116	001416	001130	001132	DT1: .WORD \$ERRPC,HLD0,HLD1,0
1079	002124	000000			
1080					
1081	002126	001416	000000		DT4: .WORD \$ERRPC,0
1082					
1083	002132	000	000	000	DF1: .BYTE 0,0,0,0
1084	002135	000			
1085					.EVEN
1086					.SBTTL ACT11 HOOKS
1087					
1088					::*****
1089					;HOOKS REQUIRED BY ACT11
1090		002136			\$SVPC= ;SAVE PC
1091		000046			=46
1092	000046	012632			\$ENDAD ;;1)SET LOC.46 TO ADDRESS OF \$ENDAD IN .SEOP
1093		000052			=52
1094	000052	000000			.WORD 0 ;;2)SET LOC.52 TO ZERO
1095		002136			=\$SVPC ;; RESTORE PC
1096					.SBTTL APT PARAMETER BLOCK
1097					
1098					::*****
1099					;SET LOCATIONS 24 AND 44 AS REQUIRED FOR APT
1100					::*****
1101		002136			.\$X= ;SAVE CUR ENT LOCATION
1102		000024			=24 ;SET POWER FAIL TO POINT TO START OF PROGRAM
1103	000024	000200			200 ;FOR APT START UP
1104		000044			=44 ;POINT TO APT INDIRECT ADDRESS PNTR.
1105	000044	002136			\$APTHDR ;POINT TO APT HEADER BLOCK
1106		002136			=\$X ;RESET LOCATION COUNTER
1107					::*****
1108					;SETUP APT PARAMETER BLOCK AS DEFINED IN THE APT-POP11 DIAGNOSTIC
1109					;INTERFACE SPEC.
1110					
1111	002136				\$APTHD:
1112	002136	000000			\$HIBTS: .WORD 0 ;; TWO HIGH BITS OF 18 BIT MAILBOX ADDR.
1113	002140	001526			\$MADR: .WORD \$MAIL ;; ADDRESS OF APT MAILBOX (BITS 0-15)
1114	002142	000010			\$LSTM: .WORD 10 ;; RUN TIME OF LONGEST TEST
1115	002144	000010			\$PSTM: .WORD 10 ;; RUN TIME IN SECS. OF 1ST PASS ON 1 UNIT (QUICK VERIFY)
1116	002146	000000			\$UNITH: .WORD ;; ADDITIONAL RUN TIME (SECS) OF A PASS FOR EACH ADDITIONAL UNIT
1117	002150	000052			.WORD \$ETEND-\$MAIL/2 ;;LENGTH MAILBOX-ETABLE(WORDS)

```

1118
1119
1120          ;PROGRAM INITIALIZATION
1121          ;LOCK OUT INTERRUPTS
1122          ;SET UP PROCESSOR STACK
1123          ;SET UP POWER FAIL VECTOR
1124          ;CLEAR PROGRAM CONTROL FLAGS AND COUNTS
1125          ;TYPE TITLE MESSAGE
1126
1127 002152 .START:
1128          ;SBTTL INITIALIZE THE COMMON TAGS
1129          ;:CLEAR THE COMMON TAGS (%CMTAG) AREA
1130          MOV    %CMTAG,R6          ;;FIRST LOCATION TO BE CLEARED
1131          CLR    (R6)+              ;;CLEAR MEMORY LOCATION
1132          CMP    %SWR,R6          ;;DONE?
1133          BNE    -6                  ;;LOOP BACK IF NO
1134          MOV    %STACK,SP         ;;SETUP THE STACK POINTER
1135          ;:INITIALIZE A FEW VECTORS
1136          MOV    %SCOPE,%IOTVEC    ;;IOT VECTOR FOR SCOPE ROUTINE
1137          MOV    %340,%IOTVEC+2    ;;LEVEL 7
1138          MOV    %ERROR,%EMTVEC    ;;EMT VECTOR FOR ERROR ROUTINE
1139          MOV    %340,%EMTVEC+2    ;;LEVEL 7
1140          MOV    %TRAP,%TRAPVEC    ;;TRAP VECTOR FOR TRAP CALLS
1141          MOV    %340,%TRAPVEC+2   ;;LEVEL 7
1142          MOV    %PWRDN,%PWRVEC    ;;POWER FAILURE VECTOR
1143          MOV    %340,%PWRVEC+2   ;;LEVEL 7
1144          CLR    %TIMES            ;;INITIALIZE NUMBER OF ITERATIONS
1145          CLR    %ESCAPE          ;;CLEAR THE ESCAPE ON ERROR ADDRESS
1146          MOV    %1,%SEMAX        ;;ALLOW ONE ERROR PER TEST
1147          MOV    %0,%SLPADR       ;;INITIALIZE THE LOOP ADDRESS FOR SCOPE
1148          MOV    %0,%SLPERR       ;;SETUP THE ERROR LOOP ADDRESS
1149          ;:SIZE FOR A HARDWARE SWITCH REGISTER, IF NOT FOUND OR IT IS
1150          ;:EQUAL TO -1, SETUP FOR A SOFTWARE SWITCH REGISTER.
1151          MOV    %ERRVEC-(SP)     ;;SAVE ERROR VECTOR
1152          MOV    %64%,%ERRVEC     ;;SET UP ERROR VECTOR
1153          MOV    %DSWR,%SWR       ;;SETUP FOR A HARDWARE SWICH REGISTER
1154          MOV    %DISP,%DISPLAY   ;;AND A HARDWARE DISPLAY REGISTER
1155          CMP    %-1,%SWR        ;;TRY TO REFERENCE HARDWARE SWR
1156          BNE    %6%             ;;BRANCH IF NO TIMEOUT TRAP OCCURRED
1157          BR     %6%             ;;AND THE HARDWARE SWR IS NOT = -1
1158          BR     %6%             ;;BRANCH IF NO TIMEOUT
1159          MOV    %65%,(SP)       ;;SET UP FOR TRAP RETURN
1160          RTI
1161          MOV    %SWREG,%SWR     ;;POINT TO SOFTWARE SWR
1162          MOV    %DISPREG,%DISPLAY
1163          MOV    (SP)+,%ERRVEC   ;;RESTORE ERROR VECTOR
1164
1165          CLR    %PASS           ;;CLEAR PASS COUNT
1166          BITB  %APTSIZE,%ENVH    ;;TEST USER SIZE UNDER APT
1167          BEQ  %67%             ;;YES, USE NON-APT SWITCH
1168          MOV    %SSWREG,%SWR   ;;NO, USE APT SWITCH REGISTER
1169
1170          MOV    %STACK,SP       ;;SET STACK
1171          MTPS  %340             ;;LOCK INTERRUPTS
1172          MOV    %PFAIL,%24      ;;SET UP POWER FAIL VECTOR.
1173          CLRB  %STFLG          ;;CLEAR START FLAG

```

```

1174 002436 005067 176450 CLR PASCNT ;CLEAR PASS COUNT
1175 002442 105067 176735 CLR CLRB ;CLEAR ERROR FLAG
1176 002446 005067 176740 CLR SERTTL ;CLEAR ERROR COUNT
1177 002452 005067 176740 CLR SERRPC ;CLEAR LAST ERROR POINTER
1178 002456 012767 000001 176716 MOV #1,STSTM ;SET UP FOR TEST 1
1179 002464 012767 002152 176412 MOV #.START,RETURN ;SET UP FOR POWER FAIL BEFORE
1180 ;TESTING STARTS
1181 002472 013746 000006 MOV #6,-(SP)
1182 002476 013746 000004 MOV #4,-(SP)
1183 002502 012737 002516 000004 MOV #15,#4
1184 002510 005777 176724 TST #SWR
1185 002514 000407 BR #5
1186 002516 012767 000176 176714 15: MOV #SWREG,SWR
1187 002524 012767 000174 176710 MOV #DISPREG,DISPLAY
1188 002532 022626 CMP (SP)+,(SP)+
1189 002534 012637 000004 25: MOV (SP)+,#4
1190 002540 012637 000006 MOV (SP)+,#6
1191 002544 022767 000176 176666 CMP #SWREG,SWR
1192 002552 001007 BNE #5
1193 002554 005737 000042 TST #42 ;CHECK FOR CHAIN
1194 002560 001402 BEQ #33
1195 002562 000167 000522 JMP .BEGIN
1196 002566 004767 010146 33: JSR PC,CNTLU
1197 002572 105767 176374 35: TSTB INIFLG ;HAS INITIALIZATION BEEN PERFORMED
1198 002576 001004 BNE ONCE
1199 002580 104401 015114 TYPE #TITLE ;TYPE TITLE MESSAGE
1200 002584 105167 176362 COMB INIFLG ;IF NOT SET FLAG AND DO
1201 002590 105767 176732 ONCE: TSTB #ENV ;APT CONTROL?
1202 002594 001410 BEQ #11 ;BR IF NO
1203 002596 032767 000001 176726 BIT #1,SUSR ;EXTERNAL JUMPER ON?
1204 002600 001002 BNE #12 ;NO
1205 002604 105067 176321 CLR CLRB ;CLEAR FLAG
1206 002608 000167 000452 125: JMP .BEGIN ;GO DO IT
1207 002612 032777 000001 176574 115: BIT #SW00,#SWR ;RESELECT VECTOR & CONTROL REG?
1208 002616 001002 BNE #15
1209 002620 000167 000436 JMP .BEGIN
1210 002624 012700 000300 15: MOV #300,R0 ;RESTORE VECTOR AREA TO TRAPCATCHER
1211 002628 012701 000302 MOV #302,R1 ;START AT LOCATION 300
1212 002632 012702 000004 MOV #4,R2
1213 002636 010110 25: MOV R1,(R0)
1214 002640 005011 CLR (R1)
1215 002644 060200 ADD R2,R0
1216 002648 060201 ADD R2,R1
1217 002652 022701 001000 CMP #1000,R1 ;END AT LOCATION 776
1218 002656 002771 BLT #25
1219 002660 104406 INSTR ;OUTPUT MESSAGE & GET INPUT STRING
1220 002664 015162 MREGAD ;MESSAGE
1221 002668 104410 PARAM ;CONVERT STRING
1222 002672 160000 160000 ;LOW LIMIT
1223 002676 167776 167776 ;HIGH LIMIT
1224 002680 017074 DUBASE ;STORE AT THIS LOCATION
1225 002684 001 .BYTE 1 ;MASK
1226 002688 001 .BYTE 1 ;HOW MANY TIMES + 2
1227 002692 016767 014146 176226 MOV DUBASE,KEEPA0 ;SAVE
1228 002696 004767 014006 JSR PC,DUA00R
1229 002700 016767 176216 176212 MOV KEEPA0,BASEADD ;RESTORE FOR ROTATION
    
```

1230	002742	104406				INSTR	: OUTPUT MESSAGE & GET INPUT STRING
1231	002744	015147				MVCTO	: MESSAGE
1232	002746	104410				PARAM	: CONVERT STRING
1233	002750	000300				300	: LOW LIMIT
1234	002752	000776				776	: HIGH LIMIT
1235	002754	001736				DURIV	: STORE AT THIS LOCATION
1236	002756	001			.BYTE	1	: MASK
1237	002757	004			.BYTE	4	: HOW MANY TIMES + 2
1238	002760	016767	176752	176176		MOV	DURIV,KEEPIV :SAVE
1239	002766	016767	176744	176166		MOV	DURIV,BASEIV :SET UP FOR ROTATION
1240	002774	104406				INSTR	: OUTPUT MESSAGE & GET INPUT STRING
1241	002776	015212				MULT	: MESSAGE
1242	003000	104414				SETFLG	: SET FLAG BASED UPON INPUT STRING
1243	003002	001152				MULT	: THIS FLAG
1244	003004	105767	176142			TSTB	MULTO :ARE THERE MULTIPLE DEVICES : ON THE SYSTEM ?
1245							: YES,ASK NEXT QUESTION
1246	003010	100406				BMI	BBB
1247	003012	005067	176150			CLR	ACTREG
1248	003016	005067	176146			CLR	ROTADD
1249	003022	000167	000140			JMP	OUTMUL ;JUMP AROUND NEXT QUESTION
1250	003026				BBB:		
1251	003026	104406				INSTR	: OUTPUT MESSAGE & GET INPUT STRING
1252	003030	015241				MULT	: MESSAGE
1253	003032	104410				PARAM	: CONVERT STRING
1254	003034	160000				160000	: LOW LIMIT
1255	003036	167776				167776	: HIGH LIMIT
1256	003040	001160				LASTADD	: STORE AT THIS LOCATION
1257	003042	001			.BYTE	1	: MASK
1258	003043	001			.BYTE	1	: HOW MANY TIMES + 2
1259							: THE FOLLOWING ROUTINE SETS UP ACTREG FOR THE FIRST TIME
1260	003044	012767	000001	176116	1S:	MOV	#1,ROTADD :SET UP POINTER
1261	003052	005067	176110			CLR	ACTREG :CLR ACTIVE REGISTER
1262	003056	056767	176106	176102	2S:	BIS	ROTADD,ACTREG ;MAKE THIS DEVICE ACTIVE
1263	003064	000241				CLC	
1264	003066	006167	176076			ROL	ROTADD :SET UP POINTER
1265	003072	103421				BCS	3S :ARE YOU OUT OF RANGE ?
1266	003074	062767	000010	176052		ADD	#10,BASEADD :SET UP BASE ADDRESS
1267	003102	026767	176052	176044		CMP	LASTADD,BASEADD :IS THIS THE LAST DEVICE ?
1268	003110	101362				BHI	2S :NO DO IT AGAIN
1269	003112	056767	176052	176046		BIS	ROTADD,ACTREG :THIS ASSUMES THAT THERE ARE AT : LEAST TWO DEVICES WHEN YOU ANSWER YES TO : MULTIPLE DEVICE QUESTION
1270							
1271							
1272	003120	012767	000001	176042	4S:	MOV	#1,ROTADD :SET UP FOR LATER USE IN END OF PASS ROUTINE
1273	003126	016767	176024	176020		MOV	KEEPADD,BASEADD :DITTO
1274	003134	000414				BR	OUTMUL :CONTINUE QUESTIONS
1275	003136	016767	176014	176010	3S:	MOV	KEEPADD,BASEADD :RESTORE
1276	003144	104406				INSTR	: OUTPUT MESSAGE & GET INPUT STRING
1277	003146	015335				MULT	: MESSAGE
1278	003150	104410				PARAM	: CONVERT STRING
1279	003152	160000				160000	: LOW LIMIT
1280	003154	167776				167776	: HIGH LIMIT
1281	003156	001160				LASTADD	: STORE AT THIS LOCATION
1282	003160	001			.BYTE	1	: MASK
1283	003161	001			.BYTE	1	: HOW MANY TIMES + 2
1284	003162	000167	177656		1S:	JMP	: DO IT AGAIN
1285	003166	012767	000340	013542	OUTMUL:	MOV	#340,DUPRT



```

1286 003174 004767 013466 JSR PC,DLEV ;COMPARE THE FIRST CHARACTER IN THE TELETYPE INPUT
1287 ;BUFFER TO THE CHARACTERS "1" AND "2".
1288 ;IF THE CHARACTER IS "1" CLEAR THE FLAG
1289 ;IF THE CHARACTER IS "2" SET THE FLAG
1290
1291 003200 AAA:
1292 003200 104406 INSTR ;OUTPUT MESSAGE & GET INPUT STRING
1293 003202 015553 MSYNC ;MESSAGE
1294 003204 122767 000061 012702 3$: CMPB #'1,INBUF ;IS IT "1" ?
1295 003212 001003 BNE 1$
1296 003214 105067 175726 CLRB SYNCNO ;000
1297 003220 000412 BR 4$
1298 003222 122767 000062 012664 1$: CMPB #'2,INBUF ;IS IT "2" ?
1299 003230 001004 BNE 2$
1300 003232 112767 177777 175706 MOVB #-1,SYNCNO ;377
1301 003240 000402 BR 4$
1302 003242 104407 2$: INSTR ;RETRY
1303 003244 000757 BR 3$
1304 003246 000240 4$: NOP
1305 003250 104406 INSTR ;OUTPUT MESSAGE & GET INPUT STRING
1306 003252 015621 MWIRE6 ;MESSAGE
1307 003254 104414 SETFLG ;SET FLAG BASED UPON INPUT STRING
1308 003256 001147 SEXMIT ;THIS FLAG
1309 003260 104406 INSTR ;OUTPUT MESSAGE & GET INPUT STRING
1310 003262 015672 MWIRE5 ;MESSAGE
1311 003264 104414 SETFLG ;SET FLAG BASED UPON INPUT STRING
1312 003266 001150 SEREC ;THIS FLAG
1313 003270 104406 INSTR ;OUTPUT MESSAGE & GET INPUT STRING
1314 003272 015742 MWIRE4 ;MESSAGE
1315 003274 104414 SETFLG ;SET FLAG BASED UPON INPUT STRING
1316 003276 001151 OPTCLR ;THIS FLAG
1317 003300 104406 INSTR ;OUTPUT MESSAGE & GET INPUT STRING
1318 003302 016021 MEXTJ ;MESSAGE
1319 003304 104414 SETFLG ;SET FLAG BASED UPON INPUT STRING
1320 003306 001153 JMRBY ;THIS FLAG
1321
1322 ;TEST START AND RESTART
1323
1324 003310 012706 001100 .BEGIN: MOV #STACK,SP ;SET UP STACK
1325 003314 106427 000340 MTPS #340 ;LOCK OUT INTERRUPTS
1326 003320 032777 000002 176112 BIT #SW01,ASMR ;IF SW01=1, GET STARTING PC
1327 003326 001406 BEQ 3$
1328 003330 104406 INSTR ;OUTPUT MESSAGE & GET INPUT STRING
1329 003332 015505 MTSTPC ;MESSAGE
1330 003334 104410 PARAM ;CONVERT STRING
1331 003336 003362 TST1 ;LOW LIMIT
1332 ;HIGH LIMIT
1333 ;STORE AT THIS LOCATION
1334 003340 001 .BYTE 1 ;MASK
1335 003341 001 .BYTE 1 ;HOW MANY TIMES + 2
1336 003342 000403 BR 4$
1337 003344 012767 003362 175532 3$: MOV #TST1,RETURN ;START AT TEST 1
1338 003352 104401 015501 4$: TYPE R ;TYPE R
1339 003356 000177 175522 JMP @RETURN ;START TESTING
1340
1341

```

INITIALIZE THE COMMON TAGS

1342				
1343				
1344				
1345	003362	000004		
1346	003364	012737	017334	000004
1347	003372	016737	174742	000006
1348	003400	105277	176306	
1349	003404	000401		
1350	003406	104004		
1351	003410	105277	176300	
1352	003414	000401		
1353	003416	104004		
1354	003420	012737	000006	000004
1355	003426	012737	000000	000006
1356				
1357	003434	012767	003777	175456
1358				
1359				
1360				
1361	003442	000004		
1362	003444	012737	017334	000004
1363	003452	016737	174662	000006
1364	003460	105277	176232	
1365	003464	000401		
1366	003466	104004		
1367	003470	105277	176224	
1368	003474	000401		
1369	003476	104004		
1370	003500	012737	000006	000004
1371	003506	012737	000000	000006
1372				
1373				
1374				
1375				
1376	003514	000004		
1377	003516	012737	017334	000004
1378	003524	016737	174610	000006
1379	003532	105277	176164	
1380	003536	000401		
1381	003540	104004		
1382	003542	105277	176156	
1383	003546	000401		
1384	003550	104004		
1385	003552	012737	000006	000004
1386	003560	012737	000000	000006
1387				
1388				
1389				
1390				
1391	003566	000004		
1392	003570	012737	017334	000004
1393	003576	016737	174536	000006
1394	003604	105277	176116	
1395	003610	000401		
1396	003612	104004		
1397	003614	105277	176110	

```

;; THIS TEST PROVES EXISTANCE OF DEVICE REGISTERS
*****
↑ST1: SCOPE
MOV #TRPREG, @#4 ; SETUP TRAPCATCHER
MOV PR7, @#6 ;
INCB @RXCSR ; TEST THIS REG
BR .+4 ; IF OK JMP AROUND ERROR
ERROR 4 ; CHECK DEVICE REG ADDRESSES
INCB @HRXCSR ; TEST UPPER BYTE THIS REGISTER
BR .+4 ; IF OK JMP AROUND ERROR
ERROR 4 ; CHECK DEVICE REG ADDRESSES
MOV #6, @#4 ; RESTORE TRAPCATCHER
MOV #0, @#6 ;
MOV #3777, HOLD ; SET LONGER DELAY FOR TEST.
;; THIS TEST PROVES EXISTANCE OF DEVICE REGISTERS
*****
↑ST2: SCOPE
MOV #TRPREG, @#4 ; SETUP TRAPCATCHER
MOV PR7, @#6 ;
INCB @RXDBUF ; TEST THIS REG
BR .+4 ; IF OK JMP AROUND ERROR
ERROR 4 ; CHECK DEVICE REG ADDRESSES
INCB @HRXDBUF ; TEST UPPER BYTE THIS REGISTER
BR .+4 ; IF OK JMP AROUND ERROR
ERROR 4 ; CHECK DEVICE REG ADDRESSES
MOV #6, @#4 ; RESTORE TRAPCATCHER
MOV #0, @#6 ;
;; THIS TEST PROVES EXISTANCE OF DEVICE REGISTERS
*****
↑ST3: SCOPE
MOV #TRPREG, @#4 ; SETUP TRAPCATCHER
MOV PR7, @#6 ;
INCB @PARCSR ; TEST THIS REG
BR .+4 ; IF OK JMP AROUND ERROR
ERROR 4 ; CHECK DEVICE REG ADDRESSES
INCB @HPARCSR ; TEST UPPER BYTE THIS REGISTER
BR .+4 ; IF OK JMP AROUND ERROR
ERROR 4 ; CHECK DEVICE REG ADDRESSES
MOV #6, @#4 ; RESTORE TRAPCATCHER
MOV #0, @#6 ;
;; THIS TEST PROVES EXISTANCE OF DEVICE REGISTERS
*****
↑ST4: SCOPE
MOV #TRPREG, @#4 ; SETUP TRAPCATCHER
MOV PR7, @#6 ;
INCB @TXCSR ; TEST THIS REG
BR .+4 ; IF OK JMP AROUND ERROR
ERROR 4 ; CHECK DEVICE REG ADDRESSES
INCB @HTXCSR ; TEST UPPER BYTE THIS REGISTER

```

```

1398 003620 000401 BR .+4 ;IF OK JMP AROUND ERROR
1399 003622 104004 ERROR 4 ;CHECK DEVICE REG ADDRESSES
1400 003624 012737 000006 000004 MOV #6,2#4 ;RESTORE TRAPCATCHER
1401 003632 012737 000000 000006 MOV #0,2#6 ;
1402
1403 ;;THIS TEST PROVES EXISTANCE OF DEVICE REGISTERS
1404
1405 *****
1406 003640 000004 †ST5: SCOPE
1407 003642 012737 017334 000004 MOV #TRPREG,2#4 ;SETUP TRAPCATCHER
1408 003650 016737 174464 000006 MOV PR7,2#6 ;
1409 003656 105277 176050 INCB @TXDBUF ;TEST THIS REG
1410 003662 000401 BR .+4 ;IF OK JMP AROUND ERROR
1411 003664 104004 ERROR 4 ;CHECK DEVICE REG ADDRESSES
1412 003666 105277 176042 INCB @HTXDBUF ;TEST UPPER BYTE THIS REGISTER
1413 003672 000001 BR .+4 ;IF OK JMP AROUND ERROR
1414 003674 104004 ERROR 4 ;CHECK DEVICE REG ADDRESSES
1415 003676 012737 000006 000004 MOV #6,2#4 ;RESTORE TRAPCATCHER
1416 003704 012737 000000 000006 MOV #0,2#6 ;
1417
1418 ;;BUS DRIVER TEST
1419
1420 *****
1421 003712 000004 †ST6: SCOPE
1422 003714 022777 000000 176010 CMP #0,@TXDBUF
1423 003722 001401 BEQ .+4
1424 003724 104004 ERROR 4 ;READING TXDBUF SHOULD BE ALL ZERO'S
1425 ;;THIS TEST PERFORMS MASTER RESET TESTING &
1426 ;;TESTING OF READ/WRITE BIT DTR
1427
1428 *****
1429 003726 000004 †ST7: SCOPE
1430 003730 052777 000002 175754 BIS #DTR,@RXCSR ;SET THIS BIT
1431 003736 032777 000002 175746 BIT #DTR,@RXCSR ;TEST THIS BIT
1432 003744 001001 BNE .+4 ;BR IF "1"
1433 003746 104004 ERROR 4 ;THIS BIT SHOULD BE SET
1434 003750 042777 000002 175734 BIC #DTR,@RXCSR ;CLR THIS BIT
1435 003756 032777 000002 175726 BIT #DTR,@RXCSR ;TEST THIS BIT
1436 003764 001401 BEQ .+4 ;BR IF "0"
1437 003766 104004 ERROR 4 ;THIS BIT SHOULD BE CLR
1438 ;NOW SET THIS BIT
1439 003770 052777 000002 175714 BIS #DTR,@RXCSR
1440 003776 052777 000400 175722 BIS #MRESET,@TXCSR ;MASTER RESET
1441 ;;CHECK EXISTANCE OF OPTIONAL CLEAR JUMPER
1442
1443 †STB OPTCLR ;TEST FLAG
1444 004010 100006 BPL 1$ ;OPTIONAL CLR JUMPER IS NOT IN
1445 004012 032777 000002 175672 BIT #DTR,@RXCSR ;TEST THIS BIT
1446 004020 001401 BEQ .+4 ;BR IF "0"
1447 004022 104004 ERROR 4 ;CHECK OUT MASTER RESET LOGIC
1448 004024 000405 BR 2$ ;JMP AROUND
1449 004026 032777 000002 175656 1$: BIT #DTR,@RXCSR ;TEST THIS BIT
1450 004034 001001 BNE .+4 ;BR IF "1"
1451 004036 104004 ERROR 4 ;CHECK OUT OPTIONAL CLR JUMPER
1452 004040 000240 2$: NOP
1453

```

```

1454                                     ;; THIS TEST PERFORMS MASTER RESET TESTING &
1455                                     ;; TESTING OF READ/WRITE BIT RTS
1456                                     ;;
1457                                     ;; *****
1458 004042 000004          †ST10: SCOPE
1459 004044 052777 000004 175640  BIS      #RTS, @RXCSR      ; SET THIS BIT
1460 004052 032777 000004 175632  BIT      #RTS, @RXCSR      ; TEST THIS BIT
1461 004060 001001          BNE      .+4          ; BR IF "-1"
1462 004062 104004          ERROR    4              ; THIS BIT SHOULD BE SET
1463 004064 042777 000004 175620  BIC      #RTS, @RXCSR      ; CLR THIS BIT
1464 004072 032777 000004 175612  BIT      #RTS, @RXCSR      ; TEST THIS BIT
1465 004100 001401          BEQ      .+4          ; BR IF "0"
1466 004102 104004          ERROR    4              ; THIS BIT SHOULD BE CLR
1467                                     : NOW SET THIS BIT
1468 004104 052777 000004 175600  BIS      #RTS, @RXCSR
1469 004112 052777 000400 175606  BIS      #MRESET, @TXCSR   ; MASTER RESET
1470                                     ;; CHECK EXISTANCE OF OPTIONAL CLEAR JUMPER
1471                                     ;;
1472 004120 105767 175025          †STB      OPTCLR      ; TEST FLAG
1473 004124 100006          BPL      1$          ; OPTIONAL CLR JUMPER IS NOT IN
1474 004126 032777 000004 175556  BIT      #RTS, @RXCSR      ; TEST THIS BIT
1475 004134 001401          BEQ      .+4          ; BR IF "0"
1476 004136 104004          ERROR    4              ; CHECK OUT MASTER RESET LOGIC
1477 004140 000405          BR       2$          ; JMP AROUND
1478 004142 032777 000004 175542 1$: BIT      #RTS, @RXCSR      ; TEST THIS BIT
1479 004150 001001          BNE      .+4          ; BR IF "-1"
1480 004152 104004          ERROR    4              ; CHECK OUT OPTIONAL CLR JUMPER
1481 004154 000240          2$: NOP
1482
1483                                     ; WAIT FOR CABLE DELAYS
1484                                     ; *****
1485                                     ; MODIFY "HOLD:" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
1486                                     ; *****
1487 004156 016702 174736          MOV      HOLD, R2 ; SET DELAY TIME
1488 004162 005302          DEC      R2
1489 004164 001376          BNE      -2          ; WAIT THIS TIME
1490                                     ; OK NOW FALL THRU AND CONTINUE TESTING.....
1491                                     ; EXIT STAGE LEFT.... CHINING!
1492                                     ;; THIS TEST PERFORMS MASTER RESET TESTING &
1493                                     ;; TESTING OF READ/WRITE BIT STD
1494                                     ;;
1495                                     ;; *****
1496 004166 000004          †ST11: SCOPE
1497 004170 052777 000010 175514  BIS      #STD, @RXCSR      ; SET THIS BIT
1498 004176 032777 000010 175506  BIT      #STD, @RXCSR      ; TEST THIS BIT
1499 004204 001001          BNE      .+4          ; BR IF "-1"
1500 004206 104004          ERROR    4              ; THIS BIT SHOULD BE SET
1501 004210 042777 000010 175474  BIC      #STD, @RXCSR      ; CLR THIS BIT
1502 004216 032777 000010 175466  BIT      #STD, @RXCSR      ; TEST THIS BIT
1503 004224 001401          BEQ      .+4          ; BR IF "0"
1504 004226 104004          ERROR    4              ; THIS BIT SHOULD BE CLR
1505                                     : NOW SET THIS BIT
1506 004230 052777 000010 175454  BIS      #STD, @RXCSR
1507 004236 052777 000400 175462  BIS      #MRESET, @TXCSR   ; MASTER RESET
1508                                     ;; CHECK EXISTANCE OF OPTIONAL CLEAR JUMPER
1509                                     ;;

```

```

1510 004244 105767 174701 TSTB OPTCLR ;TEST FLAG
1511 004250 100006 BPL 1$ ;OPTIONAL CLR JUMPER IS NOT IN
1512 004252 032777 000010 175432 BIT #STD,@RXCSR ;TEST THIS BIT
1513 004260 001401 BEQ .+4 ;BR IF "0"
1514 004262 104004 ERROR 4 ;CHECK OUT MASTER RESET LOGIC
1515 004264 000405 BR 2$ ;JMP AROUND
1516 004266 032777 000010 175416 1$: BIT #STD,@RXCSR ;TEST THIS BIT
1517 004274 001001 BNE .+4 ;BR IF "-1"
1518 004276 104004 ERROR 4 ;CHECK OUT OPTIONAL CLR JUMPER
1519 004300 000240 2$: NOP

```

;; THIS TEST PERFORMS MASTER RESET TESTING &  
;; TESTING OF READ/WRITE BIT SYNCSCH

\*\*\*\*\*

```

1525 004302 000004 †ST12: SCOPE
1526 004304 052777 000020 175400 BIS #SYNSCH,@RXCSR ;SET THIS BIT
1527 004312 032777 000020 175372 BIT #SYNSCH,@RXCSR ;TEST THIS BIT
1528 004320 001001 BNE .+4 ;BR IF "-1"
1529 004322 104004 ERROR 4 ;THIS BIT SHOULD BE SET
1530 004324 042777 000020 175360 BIC #SYNSCH,@RXCSR ;CLR THIS BIT
1531 004332 032777 000020 175352 BIT #SYNSCH,@RXCSR ;TEST THIS BIT
1532 004340 001401 BEQ .+4 ;BR IF "0"
1533 004342 104004 ERROR 4 ;THIS BIT SHOULD BE CLR
1534 :NOW SET THIS BIT
1535 004344 052777 000020 175340 BIS #SYNSCH,@RXCSR
1536 004352 052777 000400 175346 BIS #MRESET,@TXCSR ;MASTER RESET
1537 004360 032777 000020 175324 BIT #SYNSCH,@RXCSR ;TEST THIS BIT
1538 004366 001401 BEQ .+4 ;BR IF "0"
1539 004370 104004 ERROR 4 ;CHECK OUT MASTER RESET LOGIC

```

;; THIS TEST PERFORMS MASTER RESET TESTING &  
;; TESTING OF READ/WRITE BIT DSINTE

\*\*\*\*\*

```

1545 004372 000004 †ST13: SCOPE
1546 004374 052777 000040 175310 BIS #DSINTE,@RXCSR ;SET THIS BIT
1547 004402 032777 000040 175302 BIT #DSINTE,@RXCSR ;TEST THIS BIT
1548 004410 001001 BNE .+4 ;BR IF "-1"
1549 004412 104004 ERROR 4 ;THIS BIT SHOULD BE SET
1550 004414 042777 000040 175270 BIC #DSINTE,@RXCSR ;CLR THIS BIT
1551 004422 032777 000040 175262 BIT #DSINTE,@RXCSR ;TEST THIS BIT
1552 004430 001401 BEQ .+4 ;BR IF "0"
1553 004432 104004 ERROR 4 ;THIS BIT SHOULD BE CLR
1554 :NOW SET THIS BIT
1555 004434 052777 000040 175250 BIS #DSINTE,@RXCSR
1556 004442 052777 000400 175256 BIS #MRESET,@TXCSR ;MASTER RESET
1557 004450 032777 000040 175234 BIT #DSINTE,@RXCSR ;TEST THIS BIT
1558 004456 001401 BEQ .+4 ;BR IF "0"
1559 004460 104004 ERROR 4 ;CHECK OUT MASTER RESET LOGIC

```

;; THIS TEST PERFORMS MASTER RESET TESTING &  
;; TESTING OF READ/WRITE BIT RINTEN

\*\*\*\*\*

```

1565 004462 000004 †ST14: SCOPE

```

INITIALIZE THE COMMON TAGS

```

1566 004464 052777 000100 175220
1567 004472 032777 000100 175212
1568 004500 001001
1569 004502 104004
1570 004504 042777 000100 175200
1571 004512 032777 000100 175172
1572 004520 001401
1573 004522 104004
1574
1575 004524 052777 000100 175160
1576 004532 052777 000400 175166
1577 004540 032777 000100 175144
1578 004546 001401
1579 004550 104004
1580
1581
1582
1583
1584
1585 004552 000004
1586 004554 052777 000400 175130
1587 004562 032777 000400 175122
1588 004570 001001
1589 004572 104004
1590 004574 042777 000400 175110
1591 004602 032777 000400 175102
1592 004610 001401
1593 004612 104004
1594
1595 004614 052777 000400 175070
1596 004622 052777 000400 175076
1597 004630 032777 000400 175054
1598 004636 001401
1599 004640 104004
1600
1601
1602
1603
1604
1605 004642 000004
1606 004644 052777 000001 175054
1607 004652 032777 000001 175046
1608 004660 001001
1609 004662 104004
1610 004664 042777 000001 175034
1611 004672 032777 000001 175026
1612 004700 001401
1613 004702 104004
1614
1615 004704 052777 000001 175014
1616 004712 052777 000400 175006
1617 004720 032777 000001 175000
1618 004726 001401
1619 004730 104004
1620
1621

```

```

BIS #RINTEN,@RXCSR ;SET THIS BIT
BIT #RINTEN,@RXCSR ;TEST THIS BIT
BNE +4 ;BR IF "-1"
ERROR 4 ;THIS BIT SHOULD BE SET
BIC #RINTEN,@RXCSR ;CLR THIS BIT
BIT #RINTEN,@RXCSR ;TEST THIS BIT
BEQ +4 ;BR IF "0"
ERROR 4 ;THIS BIT SHOULD BE CLR
;NOW SET THIS BIT
BIS #RINTEN,@RXCSR
BIS #RINTEN,@RXCSR ;MASTER RESET
BIT #RINTEN,@RXCSR ;TEST THIS BIT
BEQ +4 ;BR IF "0"
ERROR 4 ;CHECK OUT MASTER RESET LOGIC

;; THIS TEST PERFORMS MASTER RESET TESTING &
;; TESTING OF READ/WRITE BIT STPSYN
*****
†ST15: SCOPE
BIS #STPSYN,@RXCSR ;SET THIS BIT
BIT #STPSYN,@RXCSR ;TEST THIS BIT
BNE +4 ;BR IF "-1"
ERROR 4 ;THIS BIT SHOULD BE SET
BIC #STPSYN,@RXCSR ;CLR THIS BIT
BIT #STPSYN,@RXCSR ;TEST THIS BIT
BEQ +4 ;BR IF "0"
ERROR 4 ;THIS BIT SHOULD BE CLR
;NOW SET THIS BIT
BIS #STPSYN,@RXCSR
BIS #MRESET,@TXCSR ;MASTER RESET
BIT #STPSYN,@RXCSR ;TEST THIS BIT
BEQ +4 ;BR IF "0"
ERROR 4 ;CHECK OUT MASTER RESET LOGIC

;; THIS TEST PERFORMS MASTER RESET TESTING &
;; TESTING OF READ/WRITE BIT BREAK
*****
†ST16: SCOPE
BIS #BREAK,@TXCSR ;SET THIS BIT
BIT #BREAK,@TXCSR ;TEST THIS BIT
BNE +4 ;BR IF "-1"
ERROR 4 ;THIS BIT SHOULD BE SET
BIC #BREAK,@TXCSR ;CLR THIS BIT
BIT #BREAK,@TXCSR ;TEST THIS BIT
BEQ +4 ;BR IF "0"
ERROR 4 ;THIS BIT SHOULD BE CLR
;NOW SET THIS BIT
BIS #BREAK,@TXCSR
BIS #RSET,@TXCSR ;MASTER RESET
BIT #BREAK,@TXCSR ;TEST THIS BIT
BEQ +4 ;BR IF "0"
ERROR 4 ;CHECK OUT MASTER RESET LOGIC

;; THIS TEST PERFORMS MASTER RESET TESTING &

```



```

1622
1623
1624
1625 004732 000004
1626 004734 052777 000010 174764
1627 004742 032777 000010 174756
1628 004750 001001
1629 004752 104004
1630 004754 042777 000010 174744
1631 004762 032777 000010 174736
1632 004770 001401
1633 004772 104004
1634
1635 004774 052777 000010 174724
1636 005002 052777 000400 174716
1637 005010 032777 000010 174710
1638 005016 001401
1639 005020 104004
1640
1641
1642
1643
1644
1645 005022 000004
1646 005024 052777 000020 174674
1647 005032 032777 000020 174666
1648 005040 001001
1649 005042 104004
1650 005044 042777 000020 174654
1651 005052 032777 000020 174646
1652 005060 001401
1653 005062 104004
1654
1655 005064 052777 000020 174634
1656 005072 052777 000400 174626
1657 005100 032777 000020 174620
1658 005106 001401
1659 005110 104004
1660
1661
1662
1663
1664
1665 005112 000004
1666 005114 052777 000040 174604
1667 005122 032777 000040 174576
1668 005130 001001
1669 005132 104004
1670 005134 042777 000040 174564
1671 005142 032777 000040 174556
1672 005150 001401
1673 005152 104004
1674
1675 005154 052777 000040 174544
1676 005162 052777 000400 174536
1677 005170 032777 000040 174530

```

```

:: TESTING OF READ/WRITE BIT HDXEN
:: *****
tst17: SCOPE
BIS #HDXEN,@TXCSR ;SET THIS BIT
BIT #HDXEN,@TXCSR ;TEST THIS BIT
BNE .+4 ;BR IF "-1"
ERROR 4 ;THIS BIT SHOULD BE SET
BIC #HDXEN,@TXCSR ;CLR THIS BIT
BIT #HDXEN,@TXCSR ;TEST THIS BIT
BEQ .+4 ;BR IF "0"
ERROR 4 ;THIS BIT SHOULD BE CLR
;NOW SET THIS BIT
BIS #HDXEN,@TXCSR
BIS #MRESET,@TXCSR ;MASTER RESET
BIT #HDXEN,@TXCSR ;TEST THIS BIT
BEQ .+4 ;BR IF "0"
ERROR 4 ;CHECK OUT MASTER RESET LOGIC

:: THIS TEST PERFORMS MASTER RESET TESTING &
:: TESTING OF READ/WRITE BIT SEND
:: *****
tst20: SCOPE
BIS #SEND,@TXCSR ;SET THIS BIT
BIT #SEND,@TXCSR ;TEST THIS BIT
BNE .+4 ;BR IF "-1"
ERROR 4 ;THIS BIT SHOULD BE SET
BIC #SEND,@TXCSR ;CLR THIS BIT
BIT #SEND,@TXCSR ;TEST THIS BIT
BEQ .+4 ;BR IF "0"
ERROR 4 ;THIS BIT SHOULD BE CLR
;NOW SET THIS BIT
BIS #SEND,@TXCSR
BIS #MSET,@TXCSR ;MASTER RESET
BIT #SEND,@TXCSR ;TEST THIS BIT
BEQ .+4 ;BR IF "0"
ERROR 4 ;CHECK OUT MASTER RESET LOGIC

:: THIS TEST PERFORMS MASTER RESET TESTING &
:: TESTING OF READ/WRITE BIT DMANTE
:: *****
tst21: SCOPE
BIS #DMANTE,@TXCSR ;SET THIS BIT
BIT #DMANTE,@TXCSR ;TEST THIS BIT
BNE .+4 ;BR IF "-1"
ERROR 4 ;THIS BIT SHOULD BE SET
BIC #DMANTE,@TXCSR ;CLR THIS BIT
BIT #DMANTE,@TXCSR ;TEST THIS BIT
BEQ .+4 ;BR IF "0"
ERROR 4 ;THIS BIT SHOULD BE CLR
;NOW SET THIS BIT
BIS #DMANTE,@TXCSR
BIS #MSET,@TXCSR ;MASTER RESET
BIT #DMANTE,@TXCSR ;TEST THIS BIT

```

```

1678 005176 001401      BEQ      +4      ;BR IF "0"
1679 005200 104004      ERROR    4      ;CHECK OUT MASTER RESET LOGIC
1680
1681      ;: THIS TEST PERFORMS MASTER RESET TESTING &
1682      ;: TESTING OF READ/WRITE BIT TXINTE
1683      ;:
1684      ;: *****
1685      ;: †ST22: SCOPE
1686      ;: BIS      @TXINTE,@TXCSR ;SET THIS BIT
1687      ;: BIT      @TXINTE,@TXCSR ;TEST THIS BIT
1688      ;: BNE      +4      ;BR IF "-1"
1689      ;: ERROR    4      ;THIS BIT SHOULD BE SET
1690      ;: BIC      @TXINTE,@TXCSR ;CLR THIS BIT
1691      ;: BIT      @TXINTE,@TXCSR ;TEST THIS BIT
1692      ;: BEQ      +4      ;BR IF "0"
1693      ;: ERROR    4      ;THIS BIT SHOULD BE CLR
1694      ;: NOW SET THIS BIT
1695      ;: BIS      @TXINTE,@TXCSR
1696      ;: BIS      @MRESSET,@TXCSR ;MASTER RESET
1697      ;: BIT      @TXINTE,@TXCSR ;TEST THIS BIT
1698      ;: BEQ      +4      ;BR IF "0"
1699      ;: ERROR    4      ;CHECK OUT MASTER RESET LOGIC
1700
1701      ;: TEST MAINT MODE BIT 0
1702      ;:
1703      ;: THIS TEST PERFORMS MASTER RESET TESTING &
1704      ;: TESTING OF READ/WRITE BIT BIT11
1705      ;:
1706      ;: *****
1707      ;: †ST23: SCOPE
1708      ;: BIS      @BIT11,@TXCSR ;SET THIS BIT
1709      ;: BIT      @BIT11,@TXCSR ;TEST THIS BIT
1710      ;: BNE      +4      ;BR IF "-1"
1711      ;: ERROR    4      ;THIS BIT SHOULD BE SET
1712      ;: BIC      @BIT11,@TXCSR ;CLR THIS BIT
1713      ;: BIT      @BIT11,@TXCSR ;TEST THIS BIT
1714      ;: BEQ      +4      ;BR IF "0"
1715      ;: ERROR    4      ;THIS BIT SHOULD BE CLR
1716      ;: NOW SET THIS BIT
1717      ;: BIS      @BIT11,@TXCSR
1718      ;: BIS      @MRESSET,@TXCSR ;MASTER RESET
1719      ;: BIT      @BIT11,@TXCSR ;TEST THIS BIT
1720      ;: BEQ      +4      ;BR IF "0"
1721      ;: ERROR    4      ;CHECK OUT MASTER RESET LOGIC
1722
1723      ;: TEST MAINT MODE BIT 1
1724      ;:
1725      ;: THIS TEST PERFORMS MASTER RESET TESTING &
1726      ;: TESTING OF READ/WRITE BIT BIT12
1727      ;:
1728      ;: *****
1729      ;: †ST24: SCOPE
1730      ;: BIS      @BIT12,@TXCSR ;SET THIS BIT
1731      ;: BIT      @BIT12,@TXCSR ;TEST THIS BIT
1732      ;: BNE      +4      ;BR IF "-1"
1733      ;: ERROR    4      ;THIS BIT SHOULD BE SET

```

```

1734 005404 042777 010000 174314 BIC #BIT12,@TXCSR ;CLR THIS BIT
1735 01 3412 032777 010000 174306 BIT #BIT12,@TXCSR ;TEST THIS BIT
1736 01 420 001401 BEQ .+4 ;BR IF "0"
1737 005422 104004 ERROR 4 ;THIS BIT SHOULD BE CLR
1738 ;NOW SET THIS BIT
1739 005424 052777 010000 174274 BIS #BIT12,@TXCSR
1740 01 3432 052777 000400 174266 BIS #MRESET,@TXCSR ;MASTER RESET
1741 0 440 032777 010000 174260 BIT #BIT12,@TXCSR ;TEST THIS BIT
1742 0 446 001401 BEQ .+4 ;BR IF "0"
1743 005450 104004 ERROR 4 ;CHECK OUT MASTER RESET LOGIC
1744
1745 ;: THIS TEST PERFORMS MASTER RESET TESTING &
1746 ;: TESTING OF READ/WRITE BIT CLK
1747
1748 ;: *****
1749 005452 000004 †ST25: SCOPE
1750 01 3454 052777 020000 174244 BIS #CLK,@TXCSR ;SET THIS BIT
1751 005462 032777 020000 174236 BIT #CLK,@TXCSR ;TEST THIS BIT
1752 005470 001001 BNE .+4 ;BR IF "-1"
1753 005472 104004 ERROR 4 ;THIS BIT SHOULD BE SET
1754 005474 042777 020000 174224 BIC #CLK,@TXCSR ;CLR THIS BIT
1755 01 502 032777 020000 174216 BIT #CLK,@TXCSR ;TEST THIS BIT
1756 01 510 001401 BEQ .+4 ;BR IF "0"
1757 005512 104004 ERROR 4 ;THIS BIT SHOULD BE CLR
1758 ;NOW SET THIS BIT
1759 005514 052777 020000 174204 BIS #CLK,@TXCSR
1760 005522 052777 000400 174176 BIS #MRESET,@TXCSR ;MASTER RESET
1761 005530 032777 020000 174170 BIT #CLK,@TXCSR ;TEST THIS BIT
1762 01 536 001401 BEQ .+4 ;BR IF "0"
1763 005540 104004 ERROR 4 ;CHECK OUT MASTER RESET LOGIC
1764
1765 ;: THIS TEST PERFORMS MASTER RESET TESTING &
1766 ;: TESTING OF READ/WRITE BIT MTDATA
1767
1768 ;: *****
1769 005542 000004 †ST26: SCOPE
1770 005544 052777 040000 174154 BIS #MTDATA,@TXCSR ;SET THIS BIT
1771 005552 032777 040000 174146 BIT #MTDATA,@TXCSR ;TEST THIS BIT
1772 01 60 001001 BNE .+4 ;BR IF "-1"
1773 01 62 104004 ERROR 4 ;THIS BIT SHOULD BE SET
1774 0 74 042777 040000 174134 BIC #MTDATA,@TXCSR ;CLR THIS BIT
1775 0 72 032777 040000 174126 BIT #MTDATA,@TXCSR ;TEST THIS BIT
1776 0 80 001401 BEQ .+4 ;BR IF "0"
1777 005602 104004 ERROR 4 ;THIS BIT SHOULD BE CLR
1778 ;NOW SET THIS BIT
1779 005604 052777 040000 174114 BIS #MTDATA,@TXCSR
1780 01 612 052777 000400 174106 BIS #MRESET,@TXCSR ;MASTER RESET
1781 0 70 032777 040000 174100 BIT #MTDATA,@TXCSR ;TEST THIS BIT
1782 0 86 001401 BEQ .+4 ;BR IF "0"
1783 005630 104004 ERROR 4 ;CHECK OUT MASTER RESET LOGIC
1784
1785 ;: THIS TEST VERIFYS THAT INIT (RESET) CLEARS BITS IN THE
1786 ;: RXCSR & TXCSR
1787
1788 ;: *****
1789 005632 000004 †ST27: SCOPE

```

```

1790 005634 012777 177777 174050 MOV #177777,@RXCSR ;SET ALL POSSIBLE BITS
1791 005634 012777 177777 174056 MOV #177777,@TXCSR ;DITTO
1792 000005 RESET
1793 106427 000340 MTPS #340 ;RESTORE NON INTERRUPT STATUS
1794 017701 174030 MOV @RXCSR,R1 ;SAVE
1795 017702 174040 MOV @TXCSR,R2 ;SAVE
1796 105767 173257 TSTB OPTCLR ;IS THE OPTIONAL CLR JUMPER ON ?
1797 100402 BMI IS ;YES
1798 042701 000016 BIC #16,R1 ;CLR THE NON RESETABLE BITS
1799 042701 073000 18: BIC #073000,R1 ;CLR ALL NON-CLEARABLE BITS
1800 005704 005701 TST R1 ;ARE THEY ALL 0 ?
1801 005706 001401 BEQ .+4
1802 005710 104004 ERROR 4 ;ALL SPECIFIED BITS SHOULD BE CLEAR
1803 005712 042702 002200 BIC #002200,R2 ;CLEAR ALL NON-CLEARABLE BITS
1804 005716 005702 TST R2 ;ARE THEY ALL 0 ?
1805 005720 001401 BEQ .+4
1806 005722 104004 ERROR 4 ;ALL SPECIFIED BITS SHOULD BE CLEAR
1807 ;WAIT FOR CABLE DELAYS
1808 ;*****
1809 ;MODIFY "HOLD:" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
1810 ;*****
1811 005724 016702 173170 MOV HOLD,R2 ;SET DELAY TIME
1812 005730 005302 DEC R2
1813 005732 001376 BNE .-2 ;WAIT THIS TIME
1814 ;OK NOW FALL THRU AND CONTINUE TESTING.....
1815 ;EXIT STAGE LEFT....CHINNING!
1816
1817 ;: THIS TEST PERFORMS MASTER RESET TESTING &
1818 ;: TESTING OF WRITE ONLY BIT MRESET
1819 ;:
1820 ;: *****
1821 005734 000004 1821: SCOPE
1822 005736 052777 000400 173762 BIS #MRESET,@TXCSR ;TRY TO SET THIS BIT
1823 005744 032777 000400 173754 BIT #MRESET,@TXCSR ;TEST THIS BIT
1824 005752 001401 BEQ .+4 ;BR IF "0"
1825 005754 104004 ERROR 4 ;THIS BIT SHOULD NOT BE SET
1826 005756 052777 000400 173742 BIS #MRESET,@TXCSR ;MASTER RESET
1827 005764 032777 000400 173734 BIT #MRESET,@TXCSR ;TEST THIS BIT
1828 005772 001401 BEQ .+4 ;BR IF "0"
1829 005774 104004 ERROR 4 ;THIS BIT SHOULD NOT BE SET
1830 ;CHECK MASTER RESET LOGIC
1831
1832 ;: THIS TEST VERIFYS THAT THE RXCSR & TXCSR CAN BE BYTE ADDRESSED (DATOB)
1833 ;:
1834 ;: *****
1835 005776 000004 1835: SCOPE
1836 006000 052777 000400 173720 BIS #MRESET,@TXCSR ;MASTER RESET
1837 006006 105767 173137 TSTB OPTCLR ;IS THE OPTIONAL CLR JUMPER ON ?
1838 006012 100405 BMI IS ;YES
1839 006014 012777 000000 173670 MOV #0,@RXCSR ;CLR OUT NON RESETABLE BITS
1840 006022 005777 173664 TST @RXCSR ;CLR OUT DSC BY READING RXCSR
1841 006026 152777 000001 173660 18: BISB #BIT0,@RXCSR ;SET STRIP SYNC UPPER BYTE
1842 006034 017701 173652 MOV @RXCSR,R1 ;SAVE RXCSR
1843 006040 022701 000400 CMP #400,R1 ;TEST RXCSR
1844 006044 001401 BEQ .+4
1845 006046 104004 ERROR 4 ;ONLY STRIP SYNC SHOULD BE SET

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N03

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1846 006050 105077 173636 CLR8 @RXCSR ;CLR LOWER BYTE
1847 006054 017701 173632 MOV @RXCSR,R1 ;SAVE RXCSR
1848 006060 022701 000400 CMP #400,R1 ;TEST RXCSR
1849 006064 001401 BEQ .+4
1850 006066 104004 ERROR 4 ;ONLY STRIP SYNC SHOULD BE SET
1851 006070 052777 000400 173630 BIS #MRESET,@TXCSR ;MASTER RESET
1852 006076 152777 000040 173624 BISH @BITS,@TXCSR ;SET MAINT CLK UPPER BYTE
1853 006104 017701 173616 MOV @TXCSR,R1 ;SAVE TXCSR
1854 006110 042701 002000 BIC @BITW,R1 ;CLR BIT WINDOW (DEPENDENT
;ON H315 CONNECTOR EXISTANCE)
1855 CMP #20200,R1 ;TEST TXCSR
1856 006114 022701 020200 BEQ .+4
1857 006120 001401 ERROR 4 ;ONLY MAINT CLK BIT & TXDONE SHOULD BE SET
1858 006122 104004 CLR8 @TXCSR ;CLR LOWER BYTE
1859 006124 105077 173576 MOV @TXCSR,R1 ;SAVE TXCSR
1860 006130 017701 173572 BIC @BITW,R1 ;CLR BIT WINDOW (DITTO)
1861 006134 042701 002000 CMP #20200,R1 ;TEST TXCSR
1862 006140 022701 020200 BEQ .+4
1863 006144 001401 ERROR 4 ;ONLY MAINT CLK BIT & TXDONE SHOULD BE SET
1864 006146 104004 ;: THIS TEST PERFORMS MASTER RESET TESTING &
;: TESTING OF READ ONLY BIT BITW
;: MAINT INTERNAL
;: *****
1869 ;: *****
1870 006150 000004 †ST32: SCOPE
1871 006152 012777 044001 173546 MOV #MINT!MCDATA!BREAK,@TXCSR ;SET MAINT INT.,BREAK,
;: &MCDATA
1872 BIT @BITW,@TXCSR ;TEST BITW
1873 006160 032777 002000 173540 BNE .+4
1874 006166 001001 ERROR 4 ;BIT WINDOW SHOULD BE SET
1875 006170 104004 BIC @MCDATA,@TXCSR
1876 006172 042777 040000 173526 MOV @01132,R2
1877 006200 013702 001132 15: DEC R2
1878 006204 005302 BNE 15
1879 006206 001376 BIT @BITW,@TXCSR
1880 006210 032777 002000 173510 BEQ .+4
1881 006216 001401 ERROR 4 ;BIT SHOULD BE CLR
1882 006220 104004 ;: NOW SET THE MCDATA
1883 BIS @MCDATA,@TXCSR
1884 006222 052777 040000 173476 BIS #MRESET,@TXCSR ;MASTER RESET
1885 006230 052777 000400 173470 BIS #MINT!BREAK,@TXCSR
1886 006236 052777 004001 173462 MOV @01132,R2
1887 006244 013702 001132 25: DEC R2
1888 006250 005302 BNE 25
1889 006252 001376 BIT @BITW,@TXCSR
1890 006254 032777 002000 173444 BEQ .+4
1891 006262 001401 ERROR 4 ;BITW SHOULD BE CLR BY MASTER RESET
1892 006264 104004 ;: THIS TEST PERFORMS MASTER RESET TESTING &
;: TESTING OF READ ONLY BIT BITW
;: MAINT EXTERNAL
;: *****
1897 ;: *****
1898 006266 000004 †ST33: SCOPE
1899 ;: TEST TO SEE IF EXTERNAL MODEM BYPASS CONNECTOR
1900 ;: IS ON (H315)...IF "NO" JUMP AROUND TEST
1901 006270 105767 172657 †STB JMBY

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1902 006274 100036          BPL      15      ;IT IS NOT ON
1903 006276 012777 050001 173422  MOV      @NEXT!MTDATA!BREAK,@TXCSR ;SET MAINT EXT.,BREAK,
1904                                ;&MTDATA
1905 006304 032777 002000 173414  BIT      @BITW,@TXCSR ;TEST BITW
1906 006312 001001          BNE      .+4
1907 006314 104004          ERROR     4      ;BIT WINDOW SHOULD BE SET
1908 006316 042777 040000 173402  BIC      @MTDATA,@TXCSR
1909 006324 032777 002000 173374  BIT      @BITW,@TXCSR
1910 006332 001401          BEQ      .+4
1911 006334 104004          ERROR     4      ;BIT SHOULD BE CLR
1912                                ;NOW SET THE MTDATA
1913 006336 052777 040000 173362  BIS      @MTDATA,@TXCSR
1914 006344 052777 000400 173354  BIS      @MRESET,@TXCSR ;MASTER RESET
1915 006352 052777 010001 173346  BIS      @NEXT!BREAK,@TXCSR
1916 006360 032777 002000 173340  BIT      @BITW,@TXCSR
1917 006366 001401          BEQ      .+4
1918 006370 104004          ERROR     4      ;BITW SHOULD BE CLR BY MASTER RESET
1919 006372
1920
1921
1922                                ;: THIS TEST PERFORMS MASTER RESET TESTING &
1923                                ;: TESTING OF READ ONLY BIT RXDONE
1924                                ;:
1925                                ;: *****
1926 006372 000004          †ST34: SCOPE
1927 006374 052777 000400 173324  BIS      @MRESET,@TXCSR ;MASTER RESET
1928 006402 032777 000200 173302  BIT      @RXDONE,@RXCSR ;TEST THIS BIT
1929 006410 001401          BEQ      .+4 ;BR IF "0"
1930 006412 104004          ERROR     4      ;CHECK MASTER RESET LOGIC
1931                                ;: OR SHORT ON THIS BIT
1932
1933                                ;: THIS TEST PERFORMS MASTER RESET TESTING &
1934                                ;: TESTING OF READ ONLY BIT RECACT
1935                                ;:
1936                                ;: *****
1937 006414 000004          †ST35: SCOPE
1938 006416 052777 000400 173302  BIS      @MRESET,@TXCSR ;MASTER RESET
1939 006424 032777 004000 173260  BIT      @RECACT,@RXCSR ;TEST THIS BIT
1940 006432 001401          BEQ      .+4 ;BR IF "0"
1941 006434 104004          ERROR     4      ;CHECK MASTER RESET LOGIC
1942                                ;: OR SHORT ON THIS BIT
1943
1944                                ;: THIS TEST PERFORMS MASTER RESET TESTING &
1945                                ;: TESTING OF READ ONLY BIT DSC
1946                                ;:
1947                                ;: *****
1948 006436 000004          †ST36: SCOPE
1949 006440 052777 000400 173260  BIS      @MRESET,@TXCSR ;MASTER RESET
1950 006446 032777 100300 173236  BIT      @DSC,@RXCSR ;TEST THIS BIT
1951 006454 001401          BEQ      .+4 ;BR IF "0"
1952 006456 104004          ERROR     4      ;CHECK MASTER RESET LOGIC
1953                                ;: OR SHORT ON THIS BIT
1954
1955                                ;: THIS TEST PERFORMS MASTER RESET TESTING &
1956                                ;: TESTING OF READ ONLY BIT TXDONE
1957                                ;:

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1958
1959 006460 000004
1960 006462 052777 000400 173236
1961 006470 032777 000200 173230
1962 006476 001001
1963 006500 104004
1964
1965
1966
1967
1968
1969 006502 000004
1970 006504 052777 000400 173214
1971 006512 032777 100000 173206
1972 006520 001401
1973 006522 104004
1974
1975
1976
1977
1978
1979
1980 006524 000004
1981 006526 052777 000400 173172
1982 006534 016703 173156
1983 006540 012700 000377
1984 006544 017701 173146
1985 006550 120001
1986 006552 001401
1987 006554 104002
1988
1989
1990
1991
1992 006556 000004
1993 006560 052777 000400 173140
1994 006566 032777 010000 173122
1995 006574 001401
1996 006576 104004
1997
1998
1999
2000
2001
2002
2003 006600 000004
2004 006602 052777 000400 173116
2005 006610 032777 020000 173100
2006 006616 001401
2007 006620 104004
2008
2009
2010
2011
2012
2013

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*****
†ST37: SCOPE
      BIS      #MRESET,@TXCSR ;MASTER RESET
      BIT      #TXDONE,@TXCSR ;TEST THIS BIT
      BNE      +4              ;BR IF "1"
      ERROR    4              ;CHECK MASTER RESET LOGIC
                               ;OR SHORT ON THIS BIT
      ;; THIS TEST PERFORMS MASTER RESET TESTING &
      ;; TESTING OF READ ONLY BIT DWA
*****
†ST40: SCOPE
      BIS      #MRESET,@TXCSR ;MASTER RESET
      BIT      #DWA,@TXCSR   ;TEST THIS BIT
      BEQ      +4              ;BR IF "0"
      ERROR    4              ;CHECK MASTER RESET LOGIC
                               ;OR SHORT ON THIS BIT
      ;; THIS TEST PERFORMS MASTER RESET TESTING &
      ;; TESTING OF READ ONLY WORD RECEIVE DATA
*****
†ST41: SCOPE
      BIS      #MRESET,@TXCSR ;MASTER RESET
      MOV      R0,R3          ;FOR ERROR MESSAGE
      MOV      #377,R0       ;EXPECTED
      MOV      @R0,R1        ;ACTUAL
      CMPB    R0,R1
      BEQ      +4              ;BR IF "U"
      ERROR    2              ;REC DATA SHOULD BE ALL 1'S
      ;; THIS TEST PERFORMS MASTER RESET TESTING &
      ;; TESTING OF READ ONLY BIT PARER
*****
†ST42: SCOPE
      BIS      #MRESET,@TXCSR ;MASTER RESET
      BIT      #PARER,@RXDBUF ;TEST THIS BIT
      BEQ      +4              ;BR IF "0"
      ERROR    4              ;CHECK MASTER RESET LOGIC
                               ;OR SHORT ON THIS BIT
      ;; THIS TEST PERFORMS MASTER RESET TESTING &
      ;; TESTING OF READ ONLY BIT FMERR
*****
†ST43: SCOPE
      BIS      #MRESET,@TXCSR ;MASTER RESET
      BIT      #FMERR,@RXDBUF ;TEST THIS BIT
      BEQ      +4              ;BR IF "0"
      ERROR    4              ;CHECK MASTER RESET LOGIC
                               ;OR SHORT ON THIS BIT
      ;; THIS TEST PERFORMS MASTER RESET TESTING &
      ;; TESTING OF READ ONLY BIT OVRUN
*****

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2014	006622	000004		
2015	006624	052777	000400	173074
2016	006632	032777	040000	173056
2017	006640	001401		
2018	006642	104004		
2019				
2020				
2021				
2022				
2023				
2024				
2025	006644	000004		
2026	006646	052777	000400	173052
2027	006654	032777	100000	173034
2028	006662	001401		
2029	006664	104004		
2030				
2031				
2032				
2033				
2034				
2035	006666	000004		
2036	006670	012777	177777	173014
2037	006676	052777	000400	173022
2038	006704	016703	173002	
2039	006710	017701	172776	
2040	006714	105767	172231	
2041	006720	100010		
2042	006722	042701	173000	
2043				
2044	006726	012700	000000	
2045	006732	020001		
2046	006734	001401		
2047	006736	104001		
2048	006740	000407		
2049	006742	042701	173000	
2050				
2051	006746	012700	000016	
2052	006752	020001		
2053	006754	001401		
2054	006756	104001		
2055				
2056				
2057	006760			
2058				
2059				
2060				
2061				
2062	006760	016702	172134	
2063	006764	005302		
2064	006766	001376		
2065				
2066				
2067				
2068				
2069				

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TST44: SCOPE
        BIS      #MRESET, @TXCSR ; MASTER RESET
        BIT      #OVRUN, @RXDBUF ; TEST THIS BIT
        BEQ      +4 ; BR IF "0"
        ERROR    4 ; CHECK MASTER RESET LOGIC
                ; OR SHORT ON THIS BIT

        ;; THIS TEST PERFORMS MASTER RESET TESTING &
        ;; TESTING OF READ ONLY BIT RXERR

        *****
TST45: SCOPE
        BIS      #MRESET, @TXCSR ; MASTER RESET
        BIT      #RXERR, @RXDBUF ; TEST THIS BIT
        BEQ      +4 ; BR IF "0"
        ERROR    4 ; CHECK MASTER RESET LOGIC
                ; OR SHORT ON THIS BIT

        ;; THIS TEST VERIFYS THAT THE DEVICE REGISTER RXCSR
        ;; IS CLEARED BY MASTER RESET

        *****
TST46: SCOPE
        MOV      #177777, @RXCSR ; SET ALL POSSIBLE BITS
        BIS      #MRESET, @TXCSR ; MASTER RESET
        MOV      RXCSR, R3 ; FOR ERROR MESSAGE
        MOV      @RXCSR, R1 ; SAVE ACTUAL
        TSTB    OPTCLR ; TEST THE OPT CLR JUMPER FLAG
        BPL     1$ ; NO, ITS NOT IN
        BIC     #173000, R1 ; CLR NON-MASTER RESETTABLE
                ; BITS(SINCE THESE ARE DEPENDENT ON H315 CONNECTORS EXISTANCE)
        MOV     R0, R0 ; EXPECTED
        CMP     R0, R1 ; EXPECTED VS ACTUAL
        BEQ     +4
        ERROR    1 ; ALL MASTER RESETABLE BITS SHOULD BE CLR
        BR     2$ ; JUMP AROUND
1$: BIC     #173000, R1 ; CLR NON-MASTER RESETTABLE
        ; BITS(SINCE THESE ARE DEPENDENT ON H315 CONNECTORS EXISTANCE)
        MOV     #16, R0 ; EXPECTED
        CMP     R0, R1 ; EXPECTED VS ACTUAL
        BEQ     +4
        ERROR    1 ; ONLY STD, RTS, DTR BITS SHOULD BE SET
                ; NOTE THAT STD IS READ =1 INDEPENDENT OF
                ; SEC XMIT #6 STRAP

2$: ; WAIT FOR CABLE DELAYS
        *****
        ; MODIFY "HOLD:" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
        *****
        MOV     HOLD, R2 ; SET DELAY TIME
        DEC     R2
        BNE     -2 ; WAIT THIS TIME
        ; OK NOW FALL THRU AND CONTINUE TESTING.....
        ; EXIT STAGE LEFT....CHINING!

        ;; THIS TEST VERIFYS THAT THE DEVICE REGISTER TXCSR

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2070                                     ;: IS CLEARED BY MASTER RESET
2071                                     ;:
2072                                     ;: *****
2073 006770 000004                               †ST47: SCOPE
2074 006772 012777 177777 172726             MOV     #177777, @TXCSR ; SET ALL POSSIBLE BITS
2075 007000 052777 000400 172720             BIS     @MRESET, @TXCSR ; MASTER RESET
2076 007006 016703 172714                     MOV     TXCSR, R3 ; FOR ERROR MESSAGE
2077 007012 017701 172710                     MOV     @TXCSR, R1 ; SAVE ACTUAL
2078 007016 012700 000200                     MOV     #200, R0 ; EXPECTED
2079 007022 020001                               CMP     R0, R1 ; EXPECTED VS ACTUAL
2080 007024 001401                               BEQ     ;+4
2081 007026 104001                               ERROR   1 ; ONLY TXDONE SHOULD BE SET
2082
2083                                     ;: THIS TEST VERIFYS THAT THE DEVICE REGISTER RXDBUF
2084                                     ;: IS CLEARED BY MASTER RESET
2085                                     ;:
2086                                     ;: *****
2087 007030 000004                               †ST50: SCOPE
2088 007032 052777 000400 172666             BIS     @MRESET, @TXCSR ; MASTER RESET
2089 007040 016703 172652                     MOV     RXDIF, R3 ; FOR ERROR MESSAGE
2090 007044 017701 172646                     MOV     @RXLJUF, R1 ; SAVE
2091 007050 012700 000377                     MOV     #377, R0 ; EXPECTED
2092 007054 020001                               CMP     R0, R1 ; EXPECTED VS ACTUAL
2093 007056 001401                               BEQ     ;+4
2094 007060 104002                               ERROR   2 ; ONLY REC DATA BITS SHOULD BE SET
2095                                     ;: THIS TEST VERIFYS BITS RING, CTS, CARDET, SRD, DSR
2096                                     ;: ALSO DSC IS GENERATED WHEN ANY OF THESE BITS ARE SET
2097                                     ;: OR CLEARED. .... IT ALSO CHECKS THE MODEM BYPASS
2098                                     ;: JUMPER AND THAT THESE BITS CAN BE READ
2099                                     ;: NOTE: THE MODEM BYPASS JUMPER MUST BE ON (H315)
2100
2101                                     ;: *****
2102 007062 000004                               †ST51: SCOPE
2103 007064 005077 172622 172630             CLR     @RXCSR ; TO GET RID OF STD RTS, DTR IF OPTCLR JUMPER #4 IS NOT ON
2104 007070 052777 000400                     BIS     @MRESET, @TXCSR ; MASTER RESET
2105                                     ;: TEST THAT A "YES" ANSWER WAS GIVEN TO QUESTION IN
2106                                     ;: THE MONITOR OR BY DEFAULT
2107                                     ;: THIS TEST WILL BE BYPASSED IF THE EXTERNAL BYPASS
2108                                     ;: JUMPER IS NOT INSTALLED
2109 007076 105767 172051                               †STB   JMRBY
2110 007102 100402                               BMI     ;+6 ; THE ANSWER WAS YES.....
2111                                     ;: PERFORM THIS TEST
2112 007104 000167 000652                               JMP     OUT1 ; JUMP AROUND THIS TEST IF THE ANSWER
2113                                     ;: WAS NO
2114 007110 016703 172576                               MOV     RXCSR, R3 ; SET UP FOR ERROR MESSAGE
2115 007114 017701 172572                               MOV     @RXCSR, R1 ; ACTUAL
2116 007120 005000                               CLR     R0 ; EXPECTED
2117 007122 005701                               TST     R1 ; IS IT = 0 ?
2118 007124 001401                               BEQ     ;+4
2119 007126 104001                               ERROR   1 ; RXCSR SHOULD BE CLR
2120 007130 052777 000002 172554             BIS     @OTR, @RXCSR ; SET DTR
2121                                     ;: WAIT FOR CABLE DELAYS
2122                                     ;: *****
2123                                     ;: MODIFY "HOLD:" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
2124                                     ;: *****
2125 007136 016702 171756                               MOV     HOLD, R2 ; SET DELAY TIME
    
```

2126	007142	005302			DEC	R2	
2127	007144	001376			BNE	.-2	;WAIT THIS TIME
2128							;OK NOW FALL THRU AND CONTINUE TESTING.....
2129							;EXIT STAGE LEFT....CHINNING!
2130	007146	017701	172540		MOV	2RXCSR,R1	;ACTUAL
2131	007152	012700	130002		MOV	#130002,R0	;DSC,CTS,CARDET,DTR
2132	007156	020001			CMP	R0,R1	;EXPECTED VS ACTUAL
2133	007160	001401			BEQ	:+4	
2134	007162	104001			ERROR	1	;CHECK BYPASS CONNECTOR
2135	007164	017701	172522		MOV	2RXCSR,R1	;ACTUAL
2136	007170	012700	030002		MOV	#30002,R0	;CTS,CARDET,DTR
2137	007174	020001			CMP	R0,R1	;EXPECTED VS ACTUAL
2138	007176	001401			BEQ	:+4	
2139	007200	104001			ERROR	1	;PREVIOUS READING OF RXCSR SHOULD ;HAVE CLEARED DSC
2140							
2141	007202	052777	000004	172502	BIS	#RTS,2RXCSR	
2142							;WAIT FOR CABLE DELAYS
2143							*****
2144							;MODIFY "HOLD:" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
2145							*****
2146	007210	016702	171704		MOV	HOLD,R2	;SET DELAY TIME
2147	007214	005302			DEC	R2	
2148	007216	001376			BNE	.-2	;WAIT THIS TIME
2149							;OK NOW FALL THRU AND CONTINUE TESTING.....
2150							;EXIT STAGE LEFT....CHINNING!
2151	007220	017701	172466		MOV	2RXCSR,R1	
2152	007224	012700	170006		MOV	#170006,R0	;DSC,RING,CTS,CARDET,RTS,DTR
2153	007230	020001			CMP	R0,R1	;EXPECTED VS ACTUAL
2154	007232	001401			BEQ	:+4	
2155	007234	104001			ERROR	1	;CHECK BYPASS CONNECTOR
2156	007236	017701	172450		MOV	2RXCSR,R1	
2157	007242	012700	070006		MOV	#70006,R0	;RING,CTS,CARDET,RTS,DTR
2158	007246	020001			CMP	R0,R1	;EXPECTED VS ACTUAL
2159	007250	001401			BEQ	:+4	
2160	007252	104001			ERROR	1	;PREVIOUS READING OF RXCSR SHOULD ;HAVE CLEARED DSC
2161							
2162	007254	105767	171667		TSTB	SEXMIT	;IS SEC XMIT JUMPER IN ?
2163	007260	100112			BPL	OUT2	;NO
2164	007262	105767	171662		TSTB	SEREC	;IS SEC REC JUMPER IN ?
2165	007266	100163			BPL	OUT3	;NO
2166	007270	052777	000010	172414	BIS	#STD,2RXCSR	
2167							;WAIT FOR CABLE DELAYS
2168							*****
2169							;MODIFY "HOLD:" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
2170							*****
2171	007276	016702	171616		MOV	HOLD,R2	;SET DELAY TIME
2172	007302	005302			DEC	R2	
2173	007304	001376			BNE	.-2	;WAIT THIS TIME
2174							;OK NOW FALL THRU AND CONTINUE TESTING.....
2175							;EXIT STAGE LEFT....CHINNING!
2176	007306	017701	172400		MOV	2RXCSR,R1	
2177	007312	012700	173016		MOV	#173016,R0	;DSC,RING,CTS,CARDET,SRD,DSR
2178							;STD,RTS,DTR
2179	007316	020001			CMP	R0,R1	;EXPECTED VS ACTUAL
2180	007320	001401			BEQ	:+4	
2181	007322	104001			ERROR	1	;CHECK BYPASS CONNECTOR

MASK1:

2182	007324	017701	172362		MOV	2RXCSR,R1	
2183	007330	012700	073016		MASK2: MOV	273016,R0	;RING,CTS,CARDET,SRD,DSR,STD
2184							;RTS,DTR
2185	007334	020001			CMP	R0,R1	;EXPECTED VS ACTUAL
2186	007336	001401			BEQ	.+4	
2187	007340	104001			ERROR	1	;PREVIOUS READING OF RXCSR SHOULD
2188							HAVE CLEARED DSC
2189	007342	042777	000002	172342	BIC	2DTR,2RXCSR	
2190							;WAIT FOR CABLE DELAYS
2191							*****
2192							;MODIFY "HOLD:" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
2193							*****
2194	007350	016702	171544		MOV	HOLD,R2	;SET DELAY TIME
2195	007354	005302			DEC	R2	
2196	007356	001376			BNE	.-2	;WAIT THIS TIME
2197							;OK NOW FALL THRU AND CONTINUE TESTING.....
2198							;EXIT STAGE LEFT....CHINNING!
2199	007360	017701	172326		MOV	2RXCSR,R1	
2200	007364	012700	143014		MOV	2143014,R0	;DSC,RING,SRD,DSR,STD,RTS
2201	007370	020001			CMP	R0,R1	;EXPECTED VS ACTUAL
2202	007372	001401			BEQ	.+4	
2203	007374	104001			ERROR	1	;DSC SHOULD BE SET
2204	007376	042777	000004	172306	BIC	2RTS,2RXCSR	
2205							;WAIT FOR CABLE DELAYS
2206							*****
2207							;MODIFY "HOLD:" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
2208							*****
2209	007404	016702	171510		MOV	HOLD,R2	;SET DELAY TIME
2210	007410	005302			DEC	R2	
2211	007412	001376			BNE	.-2	;WAIT THIS TIME
2212							;OK NOW FALL THRU AND CONTINUE TESTING.....
2213							;EXIT STAGE LEFT....CHINNING!
2214	007414	017701	172272		MOV	2RXCSR,R1	
2215	007420	012700	103010		MASK3: MOV	2103010,R0	;DSC,SRD,DSR,STD
2216	007424	020001			CMP	R0,R1	;EXPECTED VS ACTUAL
2217	007426	001401			BEQ	.+4	
2218	007430	104001			ERROR	1	;DSC SHOULD BE SET
2219	007432	042777	000010	172252	BIC	2STD,2RXCSR	
2220							;WAIT FOR CABLE DELAYS
2221							*****
2222							;MODIFY "HOLD:" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
2223							*****
2224	007440	016702	171454		MOV	HOLD,R2	;SET DELAY TIME
2225	007444	005302			DEC	R2	
2226	007446	001376			BNE	.-2	;WAIT THIS TIME
2227							;OK NOW FALL THRU AND CONTINUE TESTING.....
2228							;EXIT STAGE LEFT....CHINNING!
2229	007450	017701	172236		MOV	2RXCSR,R1	
2230	007454	012700	100000		MOV	2100000,R0	;DSC
2231	007460	020001			CMP	R0,R1	;EXPECTED VS ACTUAL
2232	007462	001401			BEQ	.+4	
2233	007464	104001			ERROR	1	;DSC SHOULD BE SET
2234	007466	017701	172220		MOV	2RXCSR,R1	
2235	007472	005000			CLR	R0	;NONE
2236	007474	005701			TST	R1	
2237	007476	001401			BEQ	.+4	

```

2238 007500 104001          ERROR 1          ;DSC SHOULD BE CLEARED FROM PREVIOUS
2239                                     ;READING OF RXCSR
2240 007502 000167 000254    JMP      OUT1      ;JUMP AROUND
2241                                     ;THE FOLLOWING ROUTINE HANDLES THE SITUATION WHERE SEC XMIT
2242                                     ;AND SEC REC JUMPERS ARE NOT ON
2243 007506 052777 000010 172176 OUT2:  BIS      #STD,ARXCSR
2244                                     ;WAIT FOR CABLE DELAYS
2245                                     ;*****
2246                                     ;MODIFY "HOLD:" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
2247                                     ;*****
2248 007514 016702 171400    MOV      HOLD,R2  ;SET DELAY TIME
2249 007517 005302          DEC      R2
2250 007522 001376          BNE     .-2       ;WAIT THIS TIME
2251                                     ;OK NOW FALL THRU AND CONTINUE TESTING.....
2252                                     ;EXIT STAGE LEFT....CHINNING!
2253 007524 017701 172162    MOV      ARXCSR,R1 ;ACTUAL
2254 007530 012700 070016    MOV      #70016,R0 ;EXPECTED: RING ,CTS,CARDET,STD,RTS,DTR
2255 007534 020001          CMP     R0,R1    ;EXPECTED VS ACTUAL
2256 007536 001401          BEQ     .+4
2257 007540 104001          ERROR 1          ;CHECK SEC XMIT & SEC REC JUMPERS
2258 007542 042777 000004 172142 BIC      #RTS,ARXCSR
2259                                     ;WAIT FOR CABLE DELAYS
2260                                     ;*****
2261                                     ;MODIFY "HOLD:" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
2262                                     ;*****
2263 007550 016702 171344    MOV      HOLD,R2  ;SET DELAY TIME
2264 007554 005302          DEC      R2
2265 007556 001376          BNE     .-2       ;WAIT THIS TIME
2266                                     ;OK NOW FALL THRU AND CONTINUE TESTING.....
2267                                     ;EXIT STAGE LEFT....CHINNING!
2268 007560 017701 172126    MOV      ARXCSR,R1 ;ACTUAL
2269 007564 012700 130012    MOV      #130012,R0 ;DSC,CTS,CARDET,DTR,STD
2270                                     ;NOTE THAT DSC STILL ASSERTS EVEN THO THE SEC XMIT JUMPER # 6 IS NOT ON
2271 007570 020001          CMP     R0,R1    ;EXPECTED VS ACTUAL
2272 007572 001401          BEQ     .+4
2273 007574 104001          ERROR 1          ;CHECK BYPASS CONNECTOR
2274 007576 042777 000002 172106 BIC      #DTR,ARXCSR
2275                                     ;WAIT FOR CABLE DELAYS
2276                                     ;*****
2277                                     ;MODIFY "HOLD:" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
2278                                     ;*****
2279 007604 016702 171310    MOV      HOLD,R2  ;SET DELAY TIME
2280 007610 005302          DEC      R2
2281 007612 001376          BNE     .-2       ;WAIT THIS TIME
2282                                     ;OK NOW FALL THRU AND CONTINUE TESTING.....
2283                                     ;EXIT STAGE LEFT....CHINNING!
2284 007614 017701 172072    MOV      ARXCSR,R1 ;ACTUAL
2285 007620 012700 100010    MOV      #100010,R0 ;DSC,STD
2286 007624 020001          CMP     R0,R1    ;EXPECTED VS ACTUAL
2287 007626 001401          BEQ     .+4
2288 007630 104001          ERROR 1          ;ONLY DSC & STD SHOULD BE SET
2289 007632 000167 000124    JMP      OUT1      ;JUMP AROUND
2290 007636 052777 000010 172046 OUT3:  BIS      #STD,ARXCSR
2291                                     ;WAIT FOR CABLE DELAYS
2292                                     ;*****
2293                                     ;MODIFY "HOLD:" ACCORDINGLY FOR FASTER OR SLOWER MACHINE

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2295 007644 016702 171250
2296 007650 005302
2297 007652 001376
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2300 007654 017701 172032
2301 007660 012700 171016
2302 007664 020001
2303 007666 001401
2304 007670 104001
2305 007672 042777 000004 172012
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2310 007700 016702 171214
2311 007704 005302
2312 007706 001376
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2315 007710 017701 171776
2316 007714 012700 131012
2317 007720 020001
2318 007722 001401
2319 007724 104001
2320 007726 042777 000002 171756
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2326 007740 005302
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2330 007744 017701 171742
2331 007750 012700 101010
2332 007754 020001
2333 007756 001401
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2342 007762 000004
2343 007764 052777 000400 171734
2344 007772 012777 020000 171722
2345 010000 052777 000400 171720
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2348 010006 012777 064001 171712
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*****
MOV HOLD,R2 ;SET DELAY TIME
DEC R2
BNE -2 ;WAIT THIS TIME
;OK NOW FALL THRU AND CONTINUE TESTING.....
;EXIT STAGE LEFT....CHINNING!
MOV @RXCSR,R1 ;ACTUAL
MOV @171016,R0 ;EXPECTED: DSC,RING,CTS,CARDET,DSR,STD,RTS,DTR
CMP R0,R1 ;EXPECTED VS ACTUAL
BEQ +4
ERROR i ;CHECK SEC REC JUMPER
BIC @ATS,@RXCSR
;WAIT FOR CABLE DELAYS
*****
;MODIFY "HOLD:" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
*****
MOV HOLD,R2 ;SET DELAY TIME
DEC R2
BNE -2 ;WAIT THIS TIME
;OK NOW FALL THRU AND CONTINUE TESTING.....
;EXIT STAGE LEFT....CHINNING!
MOV @RXCSR,R1 ;ACTUAL
MOV @131012,R0 ;EXPECTED: DSC,CTS,CARDET,DSR,STD,DTR
CMP R0,R1 ;EXPECTED VS ACTUAL
BEQ +4
ERROR i ;CHECK H315 CONNECTOR
BIC @DTR,@RXCSR
;WAIT FOR CABLE DELAYS
*****
;MODIFY "HOLD:" ACCORDINGLY FOR FASTER OR SLOWER MACHINF
*****
MOV HOLD,R2 ;SET DELAY TIME
DEC R2
BNE -2 ;WAIT THIS TIME
;OK NOW FALL THRU AND CONTINUE TESTING.....
;EXIT STAGE LEFT....CHINNING!
MOV @RXCSR,R1 ;ACTUAL
MOV @101010,R0 ;EXPECTED: DSC,DSR,STD
CMP R0,R1 ;EXPECTED VS ACTUAL
BEQ +4
ERROR i ;CHECK H315 CONNECTOR

```

OUT1:

```

; THIS TEST VERIFYS THAT REACT (REC ACTIVE) ASSERTS
; IMMED. WHEN SYNC EXTERNAL MODE IS SELECTED
; AND SYNC SEARCH IS SET

```

```

*****
TEST2: SCOPE
BIS #MRESET,@TXCSR ;MASTER RESET
MOV #SYNEXT,@PARCSR ;SET THE MODE
BIS #MRESET,@TXCSR ;MASTER RESET
;SET MAINT DATA,CLK,BREAK,&MAINTENANCE MODE
MOV #MTDATA!CLK!MINT!BREAK,@TXCSR

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```

;SET MODE # OF BITS, PARITY SENSE & LOAD SYNC REG
MOV #SYNEXT:EIGHT:NOPT:26,@PARCSR
BIT #REACT,@RXCSR
BEQ .+4
ERROR 4 ;REACT SHOULD NOT BE SET
BIS #SYNSCH,@RXCSR ;SET SYNC SEARCH
BIT #REACT,@RXCSR
BNE .+4
ERROR 4 ;REACT DID NOT ASSERT
BIC #SYNSCH,@RXCSR ;DROP SEARCH SYNC
BIT #REACT,@RXCSR ;IS IT =0?
BEQ .+4
ERROR 4 ;REACT SHOULD BE 0

```

```

:: THIS TEST VERIFYS THAT REACT (REC ACTIVE) ASSERTS
:: IMMED. WHEN ISOCRONOUS MODE IS SELECTED
:: AND SYNC SEARCH IS SET

```

```

*****
†ST53: SCOPE
BIS #MRESET,@TXCSR ;MASTER RESET
MOV #ISYMOD,@PARCSR ;SET THE MODE
BIS #MRESET,@TXCSR ;MASTER RESET

```

```

;SET MAINT DATA, CLK, BREAK, & MAINTENANCE MODE
MOV #MNTDATA:CLK:MINT:BREAK,@TXCSR

```

```

;SET MODE # OF BITS, PARITY SENSE & LOAD SYNC REG
MOV #ISYMOD:EIGHT:NOPT:26,@PARCSR
BIT #REACT,@RXCSR
BEQ .+4
ERROR 4 ;REACT SHOULD NOT BE SET
BIS #SYNSCH,@RXCSR ;SET SYNC SEARCH
BIT #REACT,@RXCSR
BNE .+4
ERROR 4 ;REACT DID NOT ASSERT
BIC #SYNSCH,@RXCSR ;DROP SEARCH SYNC
BIT #REACT,@RXCSR ;IS IT =0?
BEQ .+4
ERROR 4 ;REACT SHOULD BE 0

```

```

:: VERIFY THE MATCH DETECT & DATA RDY FLAGS BY PUMPING
:: IN TWO * SYNC CHARS THRU MAINT DATA BIT
:: MATCH THE REACT BIT
:: ON THE THIRD * CHARACTER IT SHOULD SET RXDONE
:: * DEPENDENT ON MONITOR.
:: IF ONE SYNC STRAP IS SELECTED THEN IT WILL ONLY
:: TAKE ONE SYNC CHARACTER FOR RXDONE TO ASSERT
:: ON THE SECOND CHARACTER
:: ALSO CHECK THIS CHARACTER IN RXDBUF
:: AND CHECK OPERATION OF SYNSCH
MODE: SYNC INTERNAL
LENGTH:FIVE

```

```

*****
†ST54: SCOPE

```

```

010206 000004

```



# K04

DZDU0-A MACY11 27(1006) 03-FEB-77 07:44 PAGE 51  
 DZDU0A.M11 27-JAN-77 09:46 INITIALIZE THE COMMON TAGS

```

010210 052777 000400 171510      BIS      #MRESET,@TXCSR ;MASTER RESET
010216 012777 030000 171476      MOV      #SYNINT,@PARCSR ;SET THE MODE
010224 052777 000400 171474      BIS      #MRESET,@TXCSR ;MASTER RESET

;SET MAINT DATA,CLK,BREAK,&MAINTENANCE MODE
010232 012777 064001 171466      MOV      @MNTDATA!CLK!MINT!BREAK,@TXCSR

;SET MODE , # OF BITS,PARITY SENSE,&LOAD SYNC REG
010240 012777 030026 171454      MOV      #SYNINT!FIVE!NOPAR!26,@PARCSR
010246 016703 171444      MOV      RxD!UP,R3 ;SET UP FOR ERROR MESSAGE
010252 052777 000020 171432      BIS      #SYNSCH,@RXCSR ;SET SYNC SEARCH
;POKE CLK TO GET RECEIVER INTO SYNCROIZATION....
010260 042777 020000 171440      BIC      @CLK,@TXCSR ;POKE CLK DOWN
010266 052777 020000 171432      BIS      @CLK,@TXCSR ;POKE CLK UP
;POKE CLK TO GET LOGIC INTO SYNCRONIZATION
010274 042777 020000 171424      BIC      @CLK,@TXCSR ;POKE CLK DOWN
010282 052777 020000 171416      BIS      @CLK,@TXCSR ;POKE CLK UP
010310 012767 000012 170606      MOV      #2,COUNT
010316 012767 000015 170576      1S:    MOV      #5,SHIFT ;# OF SHIFTS
010324 012767 000026 171146      MOV      #26,STMP1 ;SYNC CHARACTER
010332 004767 006540      JSR      PC,RPOKE
010336 005367 170562      DEC      COUNT
010342 001403      BEQ      #25
;TEST SYNCNO TO SEE HOW MANY SYNC CHARS WERE SELECTED
010344 105767 170576      TSTB    SYNCNO
010350 100762      BMI     1S ;TWO SYNC CHARS
010352 105777 171334      2S:    TSTB    @RXCSR ;CHECK REC DONE BIT
010354 100001      BPL     .+4
010356 105767 171322      ERROR  4 ;RXDONE SHOULD NOT BE ASSERTED
010358 032777 004000 171322      BIT     #REACT,@RXCSR
010360 001001      BNE     .+4
010362 104004      ERROR  4 ;REACT SHOULD BE ASSERTED
010364 012767 000005 170520      MOV     #5,SHIFT
010366 012767 000021 171070      MOV     #21,STMP1 ;ANY CHARACTER
010368 004767 006462      JSR     PC,RPOKE
010370 105777 171272      TSTB    @RXCSR ;CHECK RXDONE
010372 100401      BMI     .+4
010374 104004      ERROR  4 ;RXDONE SHOULD BE ASSERTED
010376 032777 004000 171260      BIT     #REACT,@RXCSR
010378 001001      BNE     .+4
010380 105767 171246      ERROR  4 ;REACT SHOULD STILL BE ASSERTED
010382 042777 000020 171246      BIC     #SYNSCH,@RXCSR ;CLR SYNC SEARCH
010384 012777 004000 171240      BIT     #REACT,@RXCSR ;IT SHOULD DROP IMMEDIATELY
010386 01401      BEQ     .+4
010388 104004      ERROR  4 ;REACT SHOULD BE CLR
010390 105777 171230      TSTB    @RXCSR ;RXDONE
010392 100401      BMI     .+4
010394 104004      ERROR  4 ;RXDONE SHOULD STILL BE ASSERTED
010396 012700 000021      MOV     #21,R0 ;EXPECTED DATA
010398 017701 171220      MOV     @RXDBUF,R1 ;ACTUAL DATA
010400 020001      CMP     R0,R1 ;COMPARE EXP VS ACT
010402 001401      BEQ     .+4
010404 104002      ERROR  2 ;DATA CHARS SHOULD COMPARE
010406 105777 171202      TSTB    @RXCSR ;CHECK RXDONE
010408 100001      BPL     .+4
010410 104004      ERROR  4 ;RXDONE SHOULD BE CLR FROM
  
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010514 000004  
010516 052777 000400 171202  
010524 012777 030000 171170  
010532 052777 000400 171166  
  
010540 012777 064001 171160  
  
010546 012777 032026 171146  
010554 016703 171136  
010560 052777 000020 171124  
  
010566 042777 020000 171132  
010574 052777 020000 171124  
  
010602 042777 020000 171116  
010610 052777 070000 171110  
010616 012767 010000 170300  
010624 012767 010000 170270  
010632 012767 010000 170640  
010640 004767 010000 170254  
010644 010000 170254  
010650 001403  
  
010652 105767 170270  
010660 103762  
010670 105777 171026  
010680 107001  
010690 104004  
010700 032777 004000 171014  
010710 001001  
010720 104004  
010730 012767 000006 170212  
010740 012767 000021 170562  
010750 004767 006154  
010760 105777 170764  
010770 100401  
010780 104004  
010790 032777 004000 170752

;PREVIOUS READING OF RXDBUF  
;: VERIFY THE MATCH DETECT & DATA RDY FLAGS BY PUMPING  
;: IN TWO \* SYNC CHARS THRU MAINT DATA BIT  
;: WATCH THE REACT BIT  
;: ON THE THIRD \* CHARACTER IT SHOULD SET RXDONE  
;: \* DEPENDENT ON MONITOR.  
;: IF ONE SYNC STRAP IS SELECTED THEN IT WILL ONLY  
;: TAKE ONE SYNC CHARACTER FOR RXDONE TO ASSERT  
;: ON THE SECOND CHARACTER  
;: ALSO CHECK THIS CHARACTER IN RXDBUF  
;: AND CHECK OPERATION OF SYNCH  
;: MODE: SYNC INTERNAL  
;: LENGTH: SIX  
;: \*\*\*\*\*  
TSTSS: SCOPE  
BIS #MRESET,@TXCSR ;MASTER RESET  
MOV #SYNINT,@SR ;SET THE MODE  
BIS #MRESET,@TXCSR ;MASTER RESET  
  
;SET MAINT DATA, CLK, BREAK, & MAINTENANCE MODE  
MOV #MNTDATA!CLK!MINT!BREAK,@TXCSR  
  
;SET MODE # OF BITS, PARITY SENSE & LOAD SYNC REG  
MOV #SYNINT!SIX!NUPR!26,@PARCSR  
MOV RXDBUF,R3 ;SET UP FOR ERROR MESSAGE  
BIS #SYNCH,@TXCSR ;SET SYNC SEARCH  
;POKE CLK TO GET RECEIVER INTO SYNCHRONIZATION....  
BIC #CLK,@TXCSR ;POKE CLK DOWN  
BIS #CLK,@TXCSR ;POKE CLK UP  
;POKE CLK TO GET LOGIC INTO SYNCHRONIZATION  
BIC #CLK,@TXCSR ;POKE CLK DOWN  
BIS #CLK,@TXCSR ;POKE CLK UP  
18: MOV #2,COUNT  
MOV #6,SHIFT ;# OF SHIFTS  
MOV #26,\$TMP1 ;SYNC CHARACTER  
JSR PC,\$POKE  
DEC COUNT  
BEQ 25  
;TEST SYNCNO TO SEE HOW MANY SYNC CHARS WERE SELECTED  
TSTB SYNCNO  
BMI 15 ;TWO SYNC CHARS  
25: TSTB @RXCSR ;CHECK REC DONE BIT  
BPL .+4  
ERROR 4 ;RXDONE SHOULD NOT BE ASSERTED  
BIT #REACT,@RXCSR  
BNE .+4  
ERROR 4 ;REACT SHOULD BE ASSERTED  
MOV #6,SHIFT  
MOV #21,\$TMP1 ;ANY CHARACTER  
JSR PC,\$POKE  
TSTB @RXCSR ;CHECK RXDONE  
BMI .+4  
ERROR 4 ;RXDONE SHOULD BE ASSERTED  
BIT #REACT,@RXCSR

```

2518 010740 001001
2519 010742 104004
2520 010744 042777 000020 170740
2521 010752 032777 004000 170732
2522 010760 001401
2523 010762 104004
2524 010764 105777 170722
2525 010770 100401
2526 010772 104004
2527 010774 012700 000021
2528 011000 017701 170712
2529 011004 020001
2530 011006 001401
2531 011010 104002
2532 011012 105777 170674
2533 011016 100001
2534 011020 104004
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2551 011022 000004
2552 011024 052777 000400 170674
2553 011032 012777 030000 170662
2554 011040 052777 000400 170660
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2557 011046 012777 064001 170652
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2560 011054 012777 034026 170640
2561 011062 016703 170630
2562 011066 052777 000020 170616
2563
2564 011074 042777 020000 170624
2565 011102 052777 020000 170616
2566
2567 011110 042777 020000 170610
2568 011116 052777 017000 170602
2569 011124 012767 000002 167772
2570 011132 012767 000007 167762
2571 011140 012767 000026 170332
2572 011146 004767 005724
2573 011152 005367 167746

```

```

BNE .+4
ERROR 4 ;RECACT SHOULD STILL BE ASSERTED
BIC #SYNSCH,@RXCSR ;CLR SYNC SEARCH
BIT #RECACT,@RXCSR ;IT SHOULD DROP IMMEDIATELY
BEQ .+4
ERROR 4 ;RECACT SHOULD BE CLR
TSTB @RXCSR ;RXDONE
BMI .+4
ERROR 4 ;RXDONE SHOULD STILL BE ASSERTED
MOV #21,R0 ;EXPECTED DATA
MOV @RXDBUF,R1 ;ACTUAL DATA
CMP R0,R1 ;COMPARE EXP VS ACT
BEQ .+4
ERROR 2 ;DATA CHARS SHOULD COMPARE
TSTB @RXCSR ;CHECK RXDONE
BPL .+4
ERROR 4 ;RXDONE SHOULD BE CLR FROM
;PREVIOUS READING OF RXDBUF

```

```

;: VERIFY THE MATCH DETECT & DATA RDY FLAGS BY PUMPING
;: IN TWO * SYNC CHARS THRU MAINT DATA BIT
;: WATCH THE RECACT BIT
;: ON THE THIRD * CHARACTER IT SHOULD SET RXDONE
;: * DEPENDENT ON MONITOR.....
;: IF ONE SYNC STRAP IS SELECTED THEN IT WILL ONLY
;: TAKE ONE SYNC CHARACTER FOR RXDONE TO ASSERT
;: ON THE SECOND CHARACTER
;: ALSO CHECK THIS CHARACTER IN RXDBUF
;: AND CHECK OPERATION OF SYNSCH
;: MODE: SYNC INTERNAL
;: LENGTH: SEVEN

```

```

;: *****
;: STS6: SCOPE
;: BIS #MRESET,@TXCSR ;MASTER RESET
;: MOV #SYNINT,@PARCSR ;SET THE MODE
;: BIS #MRESET,@TXCSR ;MASTER RESET
;: SET MAINT DATA, CLK, BREAK, & MAINTENANCE MODE
;: MOV #MTDATA!CLK!MINT!LEAK,@TXCSR
;: SET MODE, # OF BITS, PARITY SENSE, & LOAD SYNC REG
;: MOV #SYNINT!SEVEN!NOPAR!26,@PARCSR
;: MOV R0,R3 ;SET UP FOR ERROR MESSAGE
;: BIS #SYNSCH,@RXCSR ;SET SYNC SEARCH
;: POKE CLK TO GET RECEIVER INTO SYNCRIZATION....
;: BIC #CLK,@TXCSR ;POKE CLK DOWN
;: BIS #CLK,@TXCSR ;POKE CLK UP
;: POKE CLK TO GET LOGIC INTO SYNCRIZATION
;: BIC #CLK,@TXCSR ;POKE CLK DOWN
;: BIS #CLK,@TXCSR ;POKE CLK UP
;: MOV #2,COUNT
;: 1S: MOV #7,SHIFT ;# OF SHIFTS
;: MOV #26,$IMP1 ;SYNC CHARACTER
;: JSR PC,RPOKE
;: DEC COUNT

```

INITIALIZE THE COMMON TAGS

```

2574 011156 001403      BEQ      25
2575      :TEST SYNCNO TO SEE HOW MANY SYNC CHARS WERE SELECTED
2576 011160 105767 167762  TSTB     SYNCNO
2577 011164 100762      BMI      15      ;TWO SYNC CHARS
2578 011166 105777 170520 25: TSTB     @RXCSR ;CHECK REC DONE BIT
2579 011172 100001      BPL      +4
2580 011174 104004      ERROR    4      ;RXDONE SHOULD NOT BE ASSERTED
2581 011176 032777 004000 170506  BIT      @REACT,@RXCSR
2582 011204 001001      BNE      +4
2583 011206 104004      ERROR    4      ;REACT SHOULD BE ASSERTED
2584 011210 012767 000007 167704  MOV      #7,SHIFT
2585 011216 012767 000021 170254  MOV      #21,STMP1 ;ANY CHARACTER
2586 011224 004767 005646      JSR      PC,RPOKE
2587 011230 105777 170456      TSTB     @RXCSR ;CHECK RXDONE
2588 011234 100401      BMI      +4
2589 011236 104004      ERROR    4      ;RXDONE SHOULD BE ASSERTED
2590 011240 032777 004000 170444  BIT      @REACT,@RXCSR
2591 011246 001001      BNE      +4
2592 011250 104004      ERROR    4      ;REACT SHOULD STILL BE ASSERTED
2593 011252 042777 000020 170432  BIC      @SYNSCH,@RXCSR ;CLR SYNC SEARCH
2594 011260 032777 004000 170424  BIT      @REACT,@RXCSR ;IT SHOULD DROP IMMEDIATELY
2595 011266 001401      BEQ      +4
2596 011270 104004      ERROR    4      ;REACT SHOULD BE CLR
2597 011272 105777 170414      TSTB     @RXCSR ;RXDONE
2598 011276 100401      BMI      +4
2599 011300 104004      ERROR    4      ;RXDONE SHOULD STILL BE ASSERTED
2600 011302 012700 000021      MOV      #21,R0 ;EXPECTED DATA
2601 011306 017701 170404      MOV      @RXDBUF,R1 ;ACTUAL DATA
2602 011312 020001      CMP      R0,R1 ;COMPARE EXP VS ACT
2603 011314 001401      BEQ      +4
2604 011316 104002      ERROR    2      ;DATA CHARS SHOULD COMPARE
2605 011320 105777 170366      TSTB     @RXCSR ;CHECK RXDONE
2606 011324 100001      BPL      +4
2607 011326 104004      ERROR    4      ;RXDONE SHOULD BE CLR FROM
                ;PREVIOUS READING OF RXDBUF
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2610      :; VERIFY THE MATCH DETECT & DATA RDY FLAGS BY PUMPING
2611      :; IN TWO * SYNC CHARS THRU MAINT DATA BIT
2612      :; WATCH THE REACT BIT
2613      :; ON THE THIRD * CHARACTER IT SHOULD SET RXDONE
2614      :; * : DEPENDENT ON MONITOR.
2615      :; IF ONE SYNC STRAP IS SELECTED THEN IT WILL ONLY
2616      :; TAKE ONE SYNC CHARACTER FOR RXDONE TO ASSERT
2617      :; ON THE SECOND CHARACTER
2618      :; ALSO CHECK THIS CHARACTER IN RXDBUF
2619      :; AND CHECK OPERATION OF SYNSCH
2620      :; MODE: SYNC INTERNAL
2621      :; LENGTH:EIGHT
2622
2623      :*****
2624 011330 000004      TST57: SCOPE
2625 011332 052777 000400 170366  BIS      @MRESET,@TXCSR ;MASTER RESET
2626 011340 012777 030000 170354  MOV      #SYNINT,@PARCSR ;SET THE MODE
2627 011346 052777 000400 170352  BIS      @MRESET,@TXCSR ;MASTER RESET
2628
2629      ;SET MAINT DATA,CLK,BREAK,&MAINTENANCE MODE

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2630 011354 012777 064001 170344      MOV      #MTDATA!CLK!MINT!BREAK,@TXCSR
2631
2632                                     ;SET MODE # OF BITS PARITY SENSE & LOAD SYNC REG
2633 011362 012777 036026 170332      MOV      #SYNINT!EIGHT!NOPAR!26,@PARCSR
2634 011370 016703 170322      MOV      RXDBUF,R3      ;SET UP FOR ERROR MESSAGE
2635 011374 052777 000020 170310      BIS      #SYNSCH,@RXCSR  ;SET SYNC SEARCH
2636                                     ;POKE CLK TO GET RECEIVER INTO SYNCRIZATION....
2637 011402 042777 020000 170316      BIC      #CLK,@TXCSR    ;POKE CLK DOWN
2638 011410 052777 020000 170310      BIS      #CLK,@TXCSR    ;POKE CLK UP
2639                                     ;POKE CLK TO GET LOGIC INTO SYNCRONIZATION
2640 011416 042777 020000 170302      BIC      #CLK,@TXCSR    ;POKE CLK DOWN
2641 011424 052777 020000 170274      BIS      #CLK,@TXCSR    ;POKE CLK UP
2642 011432 012767 000002 167464      MOV      #2,COUNT
2643 011440 012767 000010 167454      15:     MOV      #8,SHIFT      ;# OF SHIFTS
2644 011446 012767 000026 170024      MOV      #26,$TMP1      ;SYNC CHARACTER
2645 011454 004767 005416      JSR      PC,@POKE
2646 011460 005367 167440      DEC      COUNT
2647 011464 001403      BEQ      25
2648                                     ;TEST SYNCNO TO SEE HOW MANY SYNC CHARS WERE SELECTED
2649 011466 105767 167454      TSTB     SYNCNO
2650 011472 100762      BMI      15      ;TWO SYNC CHARS
2651 011474 105777 170212      25:     TSTB     @RXCSR      ;CHECK REC DONE BIT
2652 011500 100001      BPL      .+4
2653 011502 104004      ERROR    4      ;RXDONE SHOULD NOT BE ASSERTED
2654 011504 032777 004000 170200      BIT      @REACT,@RXCSR
2655 011512 001001      BNE      .+4
2656 011514 104004      ERROR    4      ;REACT SHOULD BE ASSERTED
2657 011516 012767 000010 167376      MOV      #8,SHIFT
2658 011524 012767 000021 167746      MOV      #21,$TMP1      ;ANY CHARACTER
2659 011532 004767 005340      JSR      PC,@POKE
2660 011536 105777 170150      TSTB     @RXCSR      ;CHECK RXDONE
2661 011542 100401      BMI      .+4
2662 011544 104004      ERROR    4      ;RXDONE SHOULD BE ASSERTED
2663 011546 032777 004000 170136      BIT      @REACT,@RXCSR
2664 011554 001001      BNE      .+4
2665 011556 104004      ERROR    4      ;REACT SHOULD STILL BE ASSERTED
2666 011560 042777 000020 170124      BIC      #SYNSCH,@RXCSR ;CLR SYNC SEARCH
2667 011566 032777 004000 170116      BIT      @REACT,@RXCSR ;IT SHOULD DROP IMMEDIATELY
2668 011574 001401      BEQ      .+4
2669 011576 104004      ERROR    4      ;REACT SHOULD BE CLR
2670 011600 105777 170106      TSTB     @RXCSR      ;RXDONE
2671 011604 100401      BMI      .+4
2672 011606 104004      ERROR    4      ;RXDONE SHOULD STILL BE ASSERTED
2673 011610 012700 000021      MOV      #21,R0      ;EXPECTED DATA
2674 011614 017701 170076      MOV      @RXDBUF,R1    ;ACTUAL DATA
2675 011620 020001      CMP      R0,R1      ;COMPARE EXP VS ACT
2676 011622 001401      BEQ      .+4
2677 011624 104002      ERROR    2      ;DATA CHARS SHOULD COMPARE
2678 011626 105777 170060      TSTB     @RXCSR      ;CHECK RXDONE
2679 011632 100001      BPL      .+4
2680 011634 104004      ERROR    4      ;RXDONE SHOULD BE CLR FROM
2681                                     ;PREVIOUS READING OF RXDBUF

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;; THIS TEST VERIFYS WORD LENGTH SELECT OF THE
;; RECEIVER SECTION. IT USES THE ERROR FLAGS
;; TO DETERMINE THAT IT WAS SELECTED CORRECTLY

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INITIALIZE THE COMMON TAGS

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011636 000004
011640 052777 000400 170060
011646 012777 000000 170046
011654 052777 000400 170044

011662 012777 064001 170036

011670 012777 000000 170024
011676 052777 000020 170006

011704 042777 020000 170014
011712 052777 020000 170006

011720 042777 020000 170000
011726 052777 020000 167772
011734 016703 167756
011740 012700 000025
011744 012767 000007 167150
011752 012767 000152 167520
011760 004767 005112
011764 105777 167722
011770 100401
011772 104004
011774 017701 167716
012000 020001
012002 001401
012004 104002

012006 012767 000007 167106
012014 012767 000152 167456
012022 004767 005050

012026 012767 000007 167066
012034 012767 000152 167436
012042 004767 005030
012046 012700 140025

012052 017701 167640
012056 020001
012060 001401
012062 104002
  
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```

; (OVRUN, RXERR)
; MODE: ISYMOD
; LENGTH: FIVE
; CHAR: 25
;*****
TST60: SCOPE
BIS #MRESET, @TXCSR ; MASTER RESET
MOV #ISYMOD, @PARCSR ; SET THE MODE
BIS #MRESET, @TXCSR ; MASTER RESET

; SET MAINT DATA, CLK BREAK, & MAINTENANCE MODE
MOV #MNTDATA!CLK!MINT!BREAK, @TXCSR

; SET MODE, # OF BITS, PARITY SENSE, & LOAD SYNC REG
MOV #ISYMOD!FIVE!NOPAR!D, @PARCSR
BIS #SYNSCH, @RXCSR ; SET SYNC SEARCH
; POKE CLK TO GET RECEIVER INTO SYNCRIZATION....
BIC #CLK, @TXCSR ; POKE CLK DOWN
BIS #CLK, @TXCSR ; POKE CLK UP
; POKE CLK TO GET LOGIC INTO SYNCRIZATION
BIC #CLK, @TXCSR ; POKE CLK DOWN
BIS #CLK, @TXCSR ; POKE CLK UP
MOV #25, R0 ; EXPECTED
MOV #7, R1 ; # OF SHIFTS
MOV #152, R2 ; DATA CHAR
JSR PC, RPOKE ; SHIFT IN THIS CHAR
TSTB @RXCSR ; RXDONE
BMI .+4
ERROR 4 ; RXDONE SHOULD BE SET
MOV @RXDBUF, R1 ; ACTUAL
CMP R0, R1 ; COMPARE EXPECTED VS. ACTUAL
BEQ .+4
ERROR 2 ; RECEIVED DATA DID NOT MATCH
; EXPECTED DATA - CHECK MAINT DATA
; OR RECEIVER LOGIC
MOV #7, R1 ; # OF SHIFTS
MOV #152, R2 ; DATA CHAR
JSR PC, RPOKE ; SHIFT IN THIS CHAR
; NOW SHIFT IN A SECOND CHARACTER WITHOUT READING RXDBUF
MOV #7, R1 ; # OF SHIFTS
MOV #152, R2 ; DATA CHAR
JSR PC, RPOKE ; SHIFT IN THIS CHAR
MOV #140000!25, R0 ; EXPECTED DATA PLUS
; RXERR & OVRUN
MOV @RXDBUF, R1 ; ACTUAL
CMP R0, R1 ; COMPARE EXP VS. ACT
BEQ .+4
ERROR 2 ; SPECIFICALLY LOOK AT RXERR &
; OVRUN BITS...THEY BOTH SHOULD BE SET

; THIS TEST VERIFYS WORD LENGTH SELECT OF THE
; RECEIVER SECTION, IT USES THE ERROR FLAGS
; TO DETERMINE THAT IT WAS SELECTED CORRECTLY
; (OVRUN, RXERR)
  
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INITIALIZE THE COMMON TAGS

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012064 000004  
012066 052777 000400 167632  
012074 012777 000000 167620  
012102 052777 000400 167616  
  
012110 012777 064001 167610  
  
012116 012777 000000 167576  
012124 052777 000020 167560  
  
012132 042777 020000 167566  
012140 052777 020000 167560  
  
012146 042777 020000 167552  
012154 052777 020000 167544  
012162 016703 167530  
012166 012700 000012  
012172 012757 000007 166722  
012200 012767 000124 167272  
012206 004767 004664  
012212 105777 167474  
012216 100401  
012220 104004  
012222 017701 167470  
012226 020001  
012230 001401  
012232 104002  
  
012234 012767 000007 166660  
012242 012767 000124 167230  
012250 004767 004622  
  
012254 012767 000007 166640  
012262 012767 000124 167210  
012270 004767 004602  
012274 012700 140012  
  
012300 017701 167412  
012304 020001  
012306 001401  
012310 104002

```

:MODE: ISYMOD
:LENGTH: FIVE
:CHAR: 12
:*****
↑ST61: SCOPE
BIS @MRESET,@TXCSR ; MASTER RESET
MOV @ISYMOD,@PARCSR ; SET THE MODE
BIS @MRESET,@TXCSR ; MASTER RESET

;SET MAINT DATA,CLK PEAK, & MAINTENANCE MODE
MOV @MNTDATA!CLK!MINT!PEAK,@TXCSR

;SET MODE # OF BITS,PARITY SENSE & LOAD SYNC REG
MOV @ISYMOD!FIVE!NUM!A!0,@PARCSR
BIS @SYNCH!0!CSR ; SET SYNC SEARCH
;POKE CLK TO GET RECEIVER INTO SYNCRIZATION....
BIC @CLK,@TXCSR ; POKE CLK DOWN
BIS @CLK,@TXCSR ; POKE CLK UP
;POKE CLK TO GET LOGIC INTO SYNCRONIZATION
BIC @CLK,@TXCSR ; POKE CLK DOWN
BIS @CLK,@TXCSR ; POKE CLK UP
MOV @RXERR,R3 ; SET UP FOR ERROR MESSAGE
MOV @12,R0 ; EXPECTED
MOV @7,SHIFT ; # OF SHIFTS
MOV @124,$TMP1 ; DATA CHAR
JSR PC,RPOKE ; SHIFT IN THIS CHAR
TSTB @RXCSR ; RXDONE
BMI +4
ERROR 4 ; RXDONE SHOULD BE SET
MOV @RXDBUF,R1 ; ACTUAL
CMP R0,R1 ; COMPARE EXPECTED VS. ACTUAL
BEQ +4
ERROR 2 ; RECEIVED DATA DID NOT MATCH
; EXPECTED DATA - CHECK MAINT DATA
; OR RECEIVER LOGIC
MOV @7,SHIFT ; # OF SHIFTS
MOV @124,$TMP1 ; DATA CHAR
JSR PC,RPOKE ; SHIFT IN THIS CHAR
;NOW SHIFT IN A SECOND CHARACTER WITHOUT READING RXDBUF
MOV @7,SHIFT ; # OF SHIFTS
MOV @124,$TMP1 ; DATA CHAR
JSR PC,RPOKE ; SHIFT IN THIS CHAR
MOV @140000!12,R0 ; EXPECTED DATA PLUS
;RXERR & OVRUN
MOV @RXDBUF,R1 ; ACTUAL
CMP R0,R1 ; COMPARE EXP VS. ACT
BEQ +4
ERROR 2 ; SPECIFICALLY LOOK AT RXERR &
; OVRUN BITS...THEY BOTH SHOULD BE SET

;END OF PASS
;TYPE NAME OF TEST
;UPDATE PASS COUNT
```

```

2798 ;CHECK FOR EXIT TO ACT-11
2799 ;RESTART TEST
2800
2801 012312 000004 .EOP: SCOPE
2802 012314 004767 000344 JSR PC,CKSWR
2803 012320 104401 TYPE ;TYPE NAME OF TEST
2804 012322 015454 MEPASS
2805 012324 104413 012556 CONVRT ,OUTCRY
2806 012330 104401 015273 TYPE ,DEVICE
2807 012334 105767 166612 TSTB MULTD ;ARE YOU RUNNING MULTIPLE DEVICES ?
2808 012340 001511 BEQ CCC ;NO JUMP AROUND
2809 012342 005767 166620 TST ACTREG ;ARE ANY DEVICES ACTIVE ?
2810 012346 001007 BNE RUNIT ;YES
2811 012350 104401 015305 TYPE MCON ;NO
2812 012354 016700 166606 MCV ACTREG,RO ;DISPLAY ACTREG
2813 012360 000000 HALT ;SELECT SOMETHING TO RUN @ ACTREG:
2814 ;SELECT SWITCHES & HIT CONTINUE (PUT SW00 =1)
2815 012362 000167 167564 JMP .START ;START OVER AGAIN..... YOU DESELECTED EVERYTHING
2816 012366 062767 000010 166560 RUNIT: ADD #10,BASEADD ;NEXT BLOCK (ADDRESSES)
2817 012374 062767 000010 166560 ZERO: MOO #10,BASEIV ;NEXT BLOCK (VECTORS)
2818 012402 01241 CLC
2819 012404 06167 166560 ROL ROTADD ;UP DATE ROTATING POINTER
2820 012410 103410 BCS ZS ;IS IT THE LAST DEVICE
2821 ;TO BE TESTED IN THIS PASS ?
2822 012412 036767 166552 166546 BIT ROTADD,ACTREG ;TEST THIS DEVICE FOR ACTIVE STATUS
2823 012420 001762 BEQ RUNIT ;IF NOT ACTIVE, TRY NEXT ADDRESS
2824 012422 004767 000034 JSR PC,REPLAY ;CALCULATE NEW PARAMETERS
2825 012426 000167 000210 JMP RESTART ;YES IT WAS ACTIVE, TEST THIS DEVICE
2826 012432 012767 000001 166530 ZS: MOV #1,ROTADD ;OK! NOW SET UP ROTATING
2827 ;POINTER FOR NEXT MULTIPLE PASS
2828 012440 016767 166512 166506 MOV KEEPADD,BASEADD ;RESTORE BASE ADDRESS
2829 012446 016767 166512 166506 MOV KEEPIV,BASEIV ;RESTORE BASE INTERRUPT VECTORS
2830 012454 004767 000002 JSR PC,REPLAY ;CALC NEW PARAMETERS
2831 012460 000441 BR CCC ;JUMP AROUND REPLAY
2832 012462 016767 166466 004404 REPLAY: MOV BASEADD,UBASE ;SET UP FOR NEW ADDRESSES
2833 012470 004767 004246 JSR PC,DURADR ;CREATE NEW ADDRESSES
2834 012474 016767 166462 167234 MOV BASEIV,DURIV ;CREATE DURIV
2835 012502 062767 000002 166452 ADD #2,BASEIV
2836 012510 06767 166446 167222 MOV BASEIV,DURIS ;CREATE DURIS
2837 012516 062767 000002 166436 ADD #2,BASEIV
2838 012524 016767 166432 167210 MOV BASEIV,DUTIV ;CREATE DUTIV
2839 012532 062767 000002 166422 ADD #2,BASEIV
2840 012540 016767 166416 167176 MOV BASEIV,DUTIS ;CREATE DUTIS
2841 012546 016767 167164 166406 MOV DURIV,BASEIV ;RESTORE
2842 012554 000207 RTS PC
2843
2844 012556 000001 OUTCRY: 1
2845 012560 006 002 .BYTE 6,2
2846 012562 001712 RXCSR
2847
2848 012564 CCC:
2849 012564 005067 166612 CLR $STNM ;CLEAR TEST NUMBER
2850 012570 005067 166622 CLR $ERRPC ;CLEAR LAST ERROR PC
2851 012574 005067 166603 CLR $ERFLG ;CLEAR ERROR FLAG
2852 012600 005267 166306 INC PASCNT ;UPDATE PASS COUNT
2853 012604 016767 166302 166270 MOV PASCNT,LIGHTS ;DISPLAY PASS COUNT
    
```



```

2854 012612 016767 166274 166714      MOV      PASCNT,SPASS      ;PASS COUNT TO APT
2855 012620 013701 000042              MOV      #42,R1          ;CHECK FOR ACT-11 OR DDP
2856 012624 001406                      BEQ      RESTART        ;IF NO CONTINUE TESTING
2857 012626 000005                      RESET
2858 012630 000005                      RESET
2859 012632 004711      SENDAD:  JSR      PC,(R1)
2860 012634 000240                      NOP
2861 012636 000240                      NOP
2862 012640 000240                      NOP
2863 012642 106427 000340      RESTRT: MTPS     #340    ;PREVENT INTERRUPTS (PRIO: 7)
2864 012646 004767 000012      JSR      PC,CKSWR
2865 012652 012767 003364 166526      MOV      #TST1+2,SLPADR ;SET LAST ADDRESS POINTER
2866 012660 000167 170476      JMP      TST1
2868                      ;CHECK SWITCH REGISTER ROUTINE.
2869                      ;CHECKS TO ALLOW FOR <↑G> TO ALLOW
2870                      ;THE CHANGING OF LOCATION 176
2871
2872 012664 005737 000042      CKSWR:  TST      #42
2873 012670 001040                      BNE     OUT
2874 012672 022767 000176 166540      CMP      #SWREG,SWR    ;SOFTWARE SWR PRESENT?
2875 012700 001034                      BNE     OUT            ;NO--LEAVE
2876 012702 105777 166536      TSTB    #STKS         ;CHECK TTY READY
2877 012706 100031                      BPL     OUT            ;NO--LEAVE
2878 012710 017767 166532 000422      MOV      #STKB,MSG     ;GET CHARACTER
2879 012716 042767 177600 000414      BIC      #177600,MSG   ;STRIP JUNK
2880 012724 122767 000007 000406      CMPB    #7,MSG        ;IS IT <↑G> ?
2881 012732 001017                      BNE     OUT            ;NO
2882 012734 104401 016061      TYPE    MCNTG
2883 012740 005137 013000      CNTLU:  COM      #RDSW
2884 012744 104401 016071      TYPE    ,MMSWR
2885 012750 104413      CONVRT
2886 012752 013002      SWREGL
2887 012754 104406 016102      INSTR,MMNEW
2888 012760 104410      PARAM
2889 012762 000000      0
2890 012764 177777      177777
2891 012766 000176      SWREG
2892 012770 000000 001      .BYTE 0,1
2893 012772 005037 013000      OUT:    CLR      #RDSW
2894 012776 000007      RTS     PC
2895 013000 000000      RDSW:  .WORD 0
2896 013002 000001      SWREGL: 1
2897 013004 000006 002      .BYTE 6,2
2898 013006 000176      SWREG
2899
2900 013010 000005      S
2901
2902                      ;CHECK FOR FREEZE ON CURRENT DATA
2903
2904 013012 004767 177646      .SCOPI: JSR      PC,CKSWR
2905 013016 032777 001000 166414      BIT      #SW09,#SWR
2906 013024 001402                      BEQ      IS
2907 013026 016716 166056      MOV      LOCK,(SP)
2908 013032 000002      IS:    RTI
2909                      .SBTTL TYPE ROUTINE
  
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*****
*ROUTINE TO TYPE ASCIZ MESSAGE, MESSAGE MUST TERMINATE WITH A 0 BYTE.
*THE ROUTINE WILL INSERT A NUMBER OF NULL CHARACTERS AFTER A LINE FEED.
*NOTE1:    $NULL CONTAINS THE CHARACTER TO BE USED AS THE FILLER CHARACTER.
*NOTE2:    $FILLC CONTAINS THE NUMBER OF FILLER CHARACTERS REQUIRED.
*NOTE3:    $FILLC CONTAINS THE CHARACTER TO FILL AFTER.
*
*CALL:
*1) USING A TRAP INSTRUCTION
*      TYPE      ,MESADR      ;;MESADR IS FIRST ADDRESS OF AN ASCIZ STRING
*OR
*      TYPE
*      MESADR
*
013034 105767 166417 $TYPE: TSTB $TPFLG      ;; IS THERE A TERMINAL?
013040 107002      EPL      1$      ;; BR IF YES
013042 000000      HALT      ;; HALT HERE IF NO TERMINAL
013044 000430      BR      3$      ;; LEAVE
013046 010046      IS:  MOV      RO, -(SP)      ;; SAVE RO
013048 017600 000002  MOV      22(SP), RO      ;; GET ADDRESS OF ASCIZ STRING
013054 122767 000001 166464  CMPB   $APTENV, SENV      ;; RUNNING IN APT MODE
013062 001011      BNE      61$      ;; NO GO CHECK FOR APT CONSOLE
013064 132767 000100 166455  BITB   $APTPOOL, SENVM      ;; SPOOL MESSAGE TO APT
013072 001405      BEQ      62$      ;; NO GO CHECK FOR CONSOLE
013074 010067 000004  MOV      RO, 61$      ;; SETUP MESSAGE ADDR SS FOR APT
013100 004767 000006  JSR      PC, $ATY3      ;; SPOOL MESSAGE TO APT
013104 000000      61$: .WORD      0      ;; MESSAGE ADDRESS
013106 132767 000040 166433 62$: BITB   $APTCSUP, SENVM      ;; APT CONSOLE SUPPRESSED
013114 001003      BNE      60$      ;; YES, SKIP TYPE OUT
013116 112046      2$:  MOVB   (RO)+, -(SP)      ;; PUSH CHARACTER TO BE TYPED ONTO STACK
013120 001005      BNE      4$      ;; BR IF IT ISN'T THE TERMINATOR
013122 005726      TST      (SP)+      ;; IF TERMINATOR POP IT OFF THE STACK
013124 012600      60$: MOV      (SP)+, RO      ;; RESTORE RO
013126 062716 000002 3$:  ADD      #2, (SP)      ;; ADJUST RETURN PC
013132 000002      RTI      ;; RETURN
013134 122716 000011 4$:  CMPB   $HT, (SP)      ;; BRANCH IF (HT)
013140 001430      BEQ      8$      ;; BRANCH IF NOT (CRLF)
013142 122716 000200  CMPB   $CRLF, (SP)
013146 001006      BNE      5$      ;; POP (CR)<(LF) EQUIV
013150 005726      TST      (SP)+      ;; TYPE A CR AND LF
013152 104401      TYPE      ;;
013154 001523      $CRLF      ;;
013156 105067 000130  CLRB   $CHARCNT      ;; CLEAR CHARACTER COUNT
013162 000755      BR      2$      ;; GET NEXT CHARACTER
013164 004767 000056 5$:  JSR      PC, $TYPEC      ;; GO TYPE THIS CHARACTER
013170 126726 166262 6$:  CMPB   $FILLC, (SP)+      ;; IS IT TIME FOR FILLER CHARS.?
013174 001350      BNE      2$      ;; IF NO GO GET NEXT CHAR.
013176 016746 166252  MOV      $NULL, -(SP)      ;; GET # OF FILLER CHARS. NEEDED
                                ;; AND THE NULL CHAR.
013202 105366 000001 7$:  DECB   1(SP)      ;; DOES A NULL NEED TO BE TYPED?
013206 002770      BLT      6$      ;; BR IF NO--GO POP THE NULL OFF OF STACK
013210 004767 000032  JSR      PC, $TYPEC      ;; GO TYPE A NULL
013214 105367 000072  DECB   $CHARCNT      ;; DO NOT COUNT AS A COUNT
013220 000770      BR      7$      ;; LOOP

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013222 112716 000040  
 013223 004767 000014  
 013224 132767 000007 000052  
 013225 001372  
 013226 005726  
 013227 000724  
 013228 105777 166176  
 013229 100375  
 013230 116677 000002 166170  
 013231 122766 000015 000002  
 013232 001003  
 013233 105067 000014  
 013234 000406  
 013235 122766 000012 000002  
 013236 001402  
 013237 105227  
 013238 000000  
 013239 000207

;HORIZONTAL TAB PROCESSOR

```

85:   MOVB   #' (SP)           ; REPLACE TAB WITH SPACE
95:   JSR    PC,$TYPEC         ; TYPE A SPACE
      BITB   #',$SCHARCNT     ; BRANCH IF NOT AT
      BNE   '95              ; TAB STOP
      TST   (SP)+            ; POP SPACE OFF STACK
      BR    2$              ; GET NEXT CHARACTER
$TYPEC: TSTB  2$STPS          ; WAIT UNTIL PRINTER IS READY
      BPL   $TYPEC
      MOVB  2(SP),2$STPB     ; LOAD CHAR TO BE TYPED INTO DATA REG.
      CMPB  #'CR,2(SP)       ; IS CHARACTER A CARRIAGE RETURN?
      BNE   '1$              ; BRANCH IF NO
      CLRB  $SCHARCNT        ; YES--CLEAR CHARACTER COUNT
      BR    $TYPEX           ; EXIT
1$:   CMPB  #'LF,2(SP)       ; IS CHARACTER A LINE FEED?
      BEQ   $TYPEX           ; BRANCH IF YES
      INCB  (PC)+            ; COUNT THE CHARACTER
      $SCHARCNT: .WORD 0     ; CHARACTER COUNT STORAGE
$TYPEX: RTS    PC
    
```

;ASCII STRING INPUT ROUTINE

```

.INSTR: MOV   2(SP),.MSG      ; PICK UP MESSAGE
      ADD   #2,(SP)          ; JUMP AROUND MESSAGE FOR RTI
      TSTB  $ENV             ; APT CONTROL
      BNE   INSTR2          ; YES NO TYPE
.INST1: TYPE
      .MSG: 0
      MOV   #INBUF,R4        ; GET STARTING LOC OF INBUF
      MOV   #7,R3            ; MAX # OF CHARS
1$:   TSTB  2$TKS ; TTY FLAG
      BPL   '1$
      MOVB  2$TKB(R4)         ; TAKE CHAR
      BICB  #200,(R4)        ; STRIP
      CMPB  (R4),#25         ; IS IT <1G>
      BEQ   .INST1
      CMPB  (R4)+,#15        ; CHECK FOR CR
      BEQ   INSTR2
2$:   TSTB  2$TPS ; TEST FLAG
      BPL   2$
      MOVB  2$TKB,2$TPB     ; ECHO CHARACTER
      DEC   R3               ; DID YOU TYPE TOO MANY CHARS ?
      BNE   '1$
.INSTE: TYPE
      MOVB  ;?
      BR    .INST1 ; RETRY
INSTR2: RTI
    
```

;CONVERT ASCII STRING TO OCTAL

```

.PARAM: MOV   (SP),R5 ; PUT CONTENTS OF SP INTO R5
      MOV   (R5)+,LOLIM    ; PUT LOW LIMIT INTO LOLIM
      MOV   (R5)+,HILIM    ; PUT HIGH LIMIT INTO HILIM
    
```

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 DZDUQA.M11 27-JAN-77 09:46 TYPE ROUTINE

```

3022 013446 012567 000156      MOV      (RS)+,DEVADR      ;PUT STORE LOC INTO DEVADR
3023 013452 112567 000154      MOVB    (RS)+,LOBITS     ;PUT MASK INTO LOBITS
3024 013456 112567 000151      MOVB    (RS)+,ADRCNT    ;PUT COUNT INTO ADRCNT
3025 013462 010516                MOV      RS,(SP) ;RESTORE RETURN ADDR ON STACK FOR RTI
3026 013464 005005                PARAM1: CLR      RS
3027 013466 012704 016114      MOV      #INBUF,R4
3028 013472 122714 000015      CMPB    #15,(R4) ;CR ?
3029 013476 001420                BEQ     PARERR ;YOU TYPED CR TOO SOON !
3030 013500 121427 000060      1$:    CMPB    (R4),#60 ;LOW LIMIT ASCII 0
3031 013504 002415                BLT     PARERR
3032 013506 121427 000067      CMPB    (R4),#67 ;HIGH LIMIT ASCII 7
3033 013512 003012                BGT     PARERR
3034 013514 142714 000060      BICB    #60,(R4) ;CONVERT TO OCTAL
3035 013520 152405                BISB    (R4)+,RS ;STORE AWAY ITS AN OK CHAR
3036 013522 122714 000015      CMPB    #15,(R4) ;CR ?
3037 013526 001414                BEQ     LIMITS ;NOW CHECK FOR HIGH & LOW LIMIT CONDS
3038 013530 006305                ASL     RS ;ALLOCATE ROOM FOR NEXT CHAR
3039 013532 006305                ASL     RS
3040 013534 006305                ASL     RS
3041 013536 000760                BR      1$
3042 013540 122714 000015      PARERR: CMPB    #15,(R4) ;CR?
3043 013544 001003                BNE     120$
3044 013546 005737 013000      TST     #RDSW ;CK SWR USED
3045 013552 001023                BNE     PARTI
3046 013554 104407                120$:  INSTER  ;RETRY
3047 013556 000742                BR      PARAM1
3048
3049 ;TEST TO SEE IF NUMBER IS WITHIN LIMITS
3050
3051 013560 020567 000042      LIMITS: CMP     RS,HILIM
3052 013564 101365                BHI     PARERR ;THE # IS TOO HIGH
3053 013566 020567 000032      CMP     RS,LOLIM
3054 013572 103762                BLO     PARERR ;THE # IS TOO LOW
3055 013574 136705 000032      BITB   LOBITS,RS ;TEST BY MASKINGTHE #
3056 013600 001357                BNE     PARERR
3057
3058 ;STORE NUMBER AT SPECIFIED ADDRESS
3059
3060 013602 016704 000022      1$:    MOV     DEVADR,R4 ;GET STARTING ADDR OF
3061 013606 010524                MOV     RS,(R4)+ ;STORE AT THIS ADDR
3062 013610 062705 000002      ADD     #2,RS
3063 013614 105367 000013      DECB   ADRCNT ;HOW MANY TIMES + 2 ?
3064 013620 001372                BNE     1$
3065 013622 000002                PARTI: RTI
3066 013624 000000                LOLIM: 0
3067 013626 000000                HILIM: 0
3068 013630 000000                DEVADR: 0
3069 013632 000000                LOBITS: 0
3070                ADRCNT=LOBITS+1
3071
3072 ;SAVE PC OF TEST THAT FAILED AND RO-R5
3073
3074 013634 016667 000004 165264 .SAV05: MOV     4(SP),SAVPC
3075
3076 ;SAVE RO-R5
3077
    
```

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3078 013642 010567 165626
3079 013646 010467 165620
3080 013652 010367 165612
3081 013656 010267 165604
3082 013662 010167 165576
3083 013666 010067 165570
3084 013672 000002
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3088 013674 016700 165562
3089 013700 016701 165560
3090 013704 016702 165556
3091 013710 016703 165554
3092 013714 016704 165552
3093 013720 016705 165550
3094 013724 000002
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3098 013726 104401
3099 013730 015405
3100 013732 017601 000000
3101 013736 062716 000002
3102 013742 012167 000130
3103 013746 112167 000126
3104 013752 112167 000123
3105 013756 013167 000120
3106
3107 013762 016704 000114
3108 013766 116705 000106
3109 013772 012700 016156
3110 013776 010403
3111 014000 042703 177770
3112 014004 062703 000260
3113 014010 110320
3114 014012 006204
3115 014014 01204
3116 014016 01204
3117 014020 005305
3118 014022 001365
3119 014024 012703 016220
3120 014030 114023
3121 014032 105367 000042
3122 014036 001374
3123 014040 105767 000035
3124 014044 001405
3125 014046 112723 000240
3126 014052 105367 000023
3127 014056 001373
3128 014060 105013
3129 014062 104401
3130 014064 016220
3131 014066 005367 000004
3132 014072 001325
3133 014074 000002
  
```

```

SV05:  MOV    R5, $REG5
      MOV    R4, $REG4
      MOV    R3, $REG3
      MOV    R2, $REG2
      MOV    R1, $REG1
      MOV    R0, $REG0
      RTI

      ;RESTORE R0-R5

.RES05: MOV    $REG0, R0
      MOV    $REG1, R1
      MOV    $REG2, R2
      MOV    $REG3, R3
      MOV    $REG4, R4
      MOV    $REG5, R5
      RTI

      ;CONVERT OCTAL NUMBER TO ASCII AND OUTPUT TO TELEPRINTER

.CONVR: TYPE
      MCRLF  ;CR LF
      MOV    2(SP), R1 ;PICK UP DATA POINTER
      ADD    2(SP), R1 ;SET UP SP FOR RTI
      MOV    (R1)+, WROCNT ;PICK UP # OF WORDS FROM TABLE
      1$:   MOVB (R1)+, CHRCNT ;PICK UP # OF CHARS FROM TABLE
      MOVB (R1)+, SPACNT ;PICK UP # OF SPACES FROM TABLE
      MOV    2(R1)+, BINWRD ;PICK UP ADDRESS OF MSG
      ;FROM TABLE
      2$:   MOV    BINWRD, R4 ;SAVE
      MOVB  CHRCNT, R5 ;SAVE
      MOV    8TEMP, R0 ;STARTING ADDRESS OF TEMP BLOCK
      3$:   MOV    R4, R3 ;SAVE
      BIC    8177770, R3 ;CLR OUT UPPER BITS .. SAVE CHAR
      ADD    8260, R3 ;CONVERT TO ASCII
      MOVB  R3, (R0)+ ;STORE AWAY
      ASR    R4 ;SHIFT FOR NEXT #
      ASR    R4 ;DITTO
      ASR    R4 ;DITTO
      DEC    R5 ;DEC CHAR COUNT
      BNE   3$ ;DO IT AGAIN ?
      MOV    8MDATA, R3 ;STARTING ADDRESS OF MDATA BLOCK
      4$:   MOVB -(R3), (R3)+ ;REVERSE THE ORDER OF NUMBERS
      DECB  CHRCNT ;DEC CHAR COUNT
      BNE   4$ ;DO IT AGAIN ?
      TSTB  SPACNT ;HOW MANY SPACES ?
      BEQ   6$ ;TYPE # IF BR =0
      5$:   MOVB  8240, (R3)+ ;"SPACE" IN ASCII
      DECB  SPACNT ;DEC # OF SPACE COUNT
      BNE   5$ ;DO IT AGAIN ?
      6$:   CLPB  (R3) ;INSERT "0" FOR TTY OUTPUT ROUTINE
      TYPE  MDATA ;THIS MESSAGE
      DEC   WROCNT ;# OF MANY #'S ?
      BNE   1$ ;DO THIS ROUTINE AGAIN IF NOT EQUAL TO 0
      RTI  ;RETURN TO PROGRAM
  
```

```

3134 014076 000000 WRDCNT: 0
3135 014100 000000 CHRCNT: 0
3136 014101 014101 SPACNT=CHRCNT+1
3137 014102 000000 BINWRD: 0
3138
3139 ;COMPARE THE FIRST CHARACTER IN THE TELETYPE INPUT
3140 ;BUFFER TO THE CHARACTERS "N" AND "Y".
3141 ;IF THE CHARACTER IS "N" CLEAR THE FLAG
3142 ;IF THE CHARACTER IS "Y" SET THE FLAG
3143
3144 014104 017605 000000 .SETFLG:MOV @ (SP),R5
3145 014110 122767 000116 001776 CMPB @'N,INBUF ;IS IT "N" ?
3146 014116 001002 BNE 15
3147 014120 105015 CLRB (R5) ;000
3148 014122 000406 BR 25
3149 014124 122767 000131 001762 15: CMPB @'Y,INBUF ;IS IT "Y" ?
3150 014132 001005 BNE 35
3151 014134 112715 177777 MOVB @-1,(R5) ;377
3152 014140 062716 000002 25: ADD @2,(SP)
3153 014144 000002 RTI
3154 014146 104407 35: INSTER ;RETRY
3155 014150 000755 BR .SETFLG
3156 .SBTTL ERROR HANDLER ROUTINE
3157
3158 ;*****
3159 ;THIS ROUTINE WILL INCREMENT THE ERROR FLAG AND THE ERROR COUNT,
3160 ;SAVE THE ERROR ITEM NUMBER AND THE ADDRESS OF THE ERROR CALL
3161 ;AND GO TO SAVIT ON FAILURE
3162 ;THE SWITCH OPTIONS PROVIDED BY THIS ROUTINE ARE:
3163 ;SW15=1 HALT ON ERROR
3164 ;SW13=1 INHIBIT ERROR TYPEOUTS
3165 ;SW10=1 BELL ON ERROR
3166 ;SW09=1 LOOP ON ERROR
3167 ;CALL
3168 ;* ERROR N ;;ERROR=EMT AND N=ERROR ITEM NUMBER
3169
3170 014152 $ERROR:
3171 014152 105267 165225 75: INCB $ERFLG ;SET THE ERROR FLAG
3172 014156 001775 BEQ 75 ;DON'T LET THE FLAG GO TO ZERO
3173 014160 016777 165216 165254 MOV $STNM,@DISPLAY ;DISPLAY TEST NUMBER AND ERROR FLAG
3174 014166 032777 002000 165244 BIT @BIT10,@SWR ;CALL ON ERROR?
3175 014174 001402 BEQ 15 ;NO - SKIP
3176 014176 104401 001516 TYPE $BELL ;RING BELL
3177 014178 005267 165204 15: INC $CNTL ;COUNT THE NUMBER OF ERRORS
3178 014180 011667 165176 MOV (SP),@R7PC ;GET ADDRESS OF ERROR INSTRUCTION
3179 014212 162767 000002 165176 SUB @2,@R7PC
3180 014214 117767 165166 MOVB @R7PC,$ITEMB ;STRIP AND SAVE THE ERROR ITEM CODE
3181 014216 032777 000000 165204 BIT @BIT13,@SWR ;SKIP TYPEOUT IF SET
3182 014218 001004 BNE 205 ;SKIP TYPEOUTS
3183 014236 004767 000072 JSR PC,SAVIT ;GO TO USER ERROR ROUTINE
3184 014242 104401 001523 TYPE ,SCLF
3185 014246 205:
3186 014246 122767 000001 165272 CMPB @APTENV,$ENV ;RUNNING IN APT MODE
3187 014254 001007 BNE 25 ;NO, SKIP APT ERROR REPORT
3188 014256 116767 165132 000004 MOVB $ITEMB,215 ;SET ITEM NUMBER AS ERROR NUMBER
3189 014264 004767 000016 JSR PC,$ATY4 ;REPORT FATAL ERROR TO APT
    
```

ERROR HANDLER ROUTINE

```

3190 014270 000 21$: .BYTE 0
3191 014271 000 .BYTE 0
3192 014272 000777 22$: BR 22$
3193 014274 005777 165140 2$: TST 2$SWR
3194 014300 100001 BPL 3$
3195 014372 000000 HALT
3196 014374 022777 001000 165126 3$: BIT 2$BIT09,2$SWR
3197 014312 001402 BEQ 4$
3198 014314 016716 165070 MOV 2$LPERR,(SP)
3199 014370 005767 165170 4$: TST 2$ESCAPE
3200 014374 001402 BEQ 5$
3201 014326 016716 165162 MOV 2$ESCAPE,(SP)
3202 014332 5$:
3203 014332 000002 RTI ;:RETURN
3204 014334 010067 164570 SAVIT: MOV R0,HLD0
3205 014340 010167 164566 MOV R1,HLD1
3206 014344 010267 164564 MOV R2,HLD2
3207 014350 010367 164562 MOV R3,HLD3
3208 014354 010467 164560 MOV R4,HLD4
3209 014360 010567 164556 MOV R5,HLD5
3210 014364 016767 165012 164552 MOV 2$STNM,HLD6

```

.SBTTL ERROR MESSAGE TYPEOUT ROUTINE

```

;*****
;THIS ROUTINE USES THE "ITEM CONTROL BYTE" (*ITEMB) TO DETERMINE WHICH
;ERROR IS TO BE REPORTED. IT THEN OBTAINS, FROM THE "ERROR TABLE" (SERRTB),
;AND REPORTS THE APPROPRIATE INFORMATION CONCERNING THE ERROR.

```

```

3219 014372 SERRTYP:
3220 014372 104401 001523 TYPE 2$SCLF ;:"CARRIAGE RETURN" & "LINE FEED"
3221 014376 010046 MOV R0,-(SP) ;:SAVE R0
3222 014470 005000 CLR R0 ;:PICKUP THE ITEM INDEX
3223 014472 153701 001414 BISB 2*$ITEMB,R0
3224 014406 001004 BNE 1$ ;:IF ITEM NUMBER IS ZERO, JUST
3225 014410 016746 165002 MOV 2$ERRPC,-(SP) ;:TYPE THE PC OF THE ERROR
3226 014414 104402 ;:SAVE 2$ERRPC FOR TYPEOUT
3227 014416 012067 000004 ;:ERROR ADDRESS
3228 014418 012067 000004 ;:GO TYPE--OCTAL ASCII(ALL DIGITS)
3229 014420 012067 000004 ;:GET OUT
3230 014422 012067 000004 ;:ADJUST THE INDEX SO THAT IT WILL
3231 014424 012067 000004 ;:WORK FOR THE ERROR TABLE
3232 014426 012067 000004 ;:
3233 014428 012067 000004 ;:
3234 014430 012067 001652 ADD 2$SERRTB,R0 ;:FORM TABLE POINTER
3235 014432 012067 000004 MOV (R0)+,2$ ;:PICKUP "ERROR MESSAGE" POINTER
3236 014434 001404 BEQ 3$ ;:SKIP TYPEOUT IF NO POINTER
3237 014436 104401 TYPE ;:TYPE THE "ERROR MESSAGE"
3238 014438 000000 ;:"ERROR MESSAGE" POINTER GOES HERE
3239 014440 104401 001523 2$: .WORD 0 ;:"CARRIAGE RETURN" & "LINE FEED"
3240 014442 012067 000004 3$: MOV (R0)+,4$ ;:PICKUP "DATA HEADER" POINTER
3241 014444 001404 BEQ 5$ ;:SKIP TYPEOUT IF 0
3242 014446 104401 TYPE ;:TYPE THE "DATA HEADER"
3243 014448 000000 ;:"DATA HEADER" POINTER GOES HERE
3244 014450 104401 001523 4$: .WORD 0 ;:"CARRIAGE RETURN" & "LINE FEED"
3245 014452 011000 5$: MOV (R0),R0 ;:PICKUP "DATA TABLE" POINTER

```

ERROR MESSAGE TYPEOUT ROUTINE

```

3246 014472 001004
3247 014474 012000
3248 014476 104401 001523
3249 014478 000207
3250 01447A
3251 01447C
3252 01447E 013046
3253 014480 104402
3254 014510 005710
3255 014512 001770
3256 014514 104401 014522
3257 014520 000771
3258 014522 020040 000
3259 014526
3260
3261
3262
3263
3264
3265
3266
3267
3268
3269
3270
3271
3272
3273
3274
3275
3276
3277
3278
3279
3280
3281
3282
3283
3284 014526 017646 000000
3285 014532 116667 000001 000211
3286 014540 112667 000207
3287 014544 062716 000002
3288 014550 000406
3289 014552 112767 000001 000171
3290 014560 112767 000006 000165
3291 014566 112767 000005 000154
3292 014574 010346
3293 014576 010446
3294 014600 010546
3295 014602 116704 000145
3296 014606 005404
3297 014610 062704 000006
3298 014614 110467 000132
3299 014620 116704 000125
3300 014624 016605 000012
3301 014630 005003

```

```

6S: BNE 7S ; GO TYPE THE DATA
MOV (SP)+,R0 ; RESTORE R0
TYPE SCRLF ; "CARRIAGE RETURN" & "LINE FEED"
RTS PC ; RETURN

7S: MOV 2(R0)+,-(SP) ; SAVE 2(R0)+ FOR TYPEOUT
TYPOC ; GO TYPE--OCTAL ASCII (ALL DIGITS)
TST (R0) ; IS THERE ANOTHER NUMBER?
BEQ 6S ; BR IF NO
TYPE 6S ; TYPE TWO(2) SPACES
BR 7S ; LOOP

8S: .ASCIZ / / ; TWO(2) SPACES
.EVEN
.SBTL BINARY TO OCTAL (ASCII) AND TYPE

;*****
;THIS ROUTINE IS USED TO CHANGE A 16-BIT BINARY NUMBER TO A 6-DIGIT
;OCTAL (ASCII) NUMBER AND TYPE IT.
;STYPOS---ENTER HERE TO SETUP SUPPRESS ZEROS AND NUMBER OF DIGITS TO TYPE
;CALL:
; MOV NUM,-(SP) ; NUMBER TO BE TYPED
; TYPOS ; CALL FOR TYPEOUT
; .BYTE N ; N=1 TO 6 FOR NUMBER OF DIGITS TO TYPE
; .BYTE M ; M=1 OR 0
; ; 1=TYPE LEADING ZEROS
; ; 0=SUPPRESS LEADING ZEROS

;STYPO---ENTER HERE TO TYPE OUT WITH THE SAME PARAMETERS AS THE LAST
;STYPOS OR STYPOC
;CALL:
; MOV NUM,-(SP) ; NUMBER TO BE TYPED
; TYPO ; CALL FOR TYPEOUT

;STYPOC---ENTER HERE FOR TYPEOUT OF A 16 BIT NUMBER
;CALL:
; MOV NUM,-(SP) ; NUMBER TO BE TYPED
; TYPOC ; CALL FOR TYPEOUT

STYPOS: MOV 2(SP),-(SP) ; PICKUP THE MODE
MOV 1(SP),SOFILL ; LOAD ZERO FILL SWITCH
MOV 2(SP),SOMODE+1 ; NUMBER OF DIGITS TO TYPE
ADD 2,SP ; ADJUST RETURN ADDRESS
BR STYPO

STYPOC: MOV 1,SOFILL ; SET THE ZERO FILL SWITCH
MOV 6,SOMODE+1 ; SET FOR SIX(6) DIGITS
STYPO: MOV 5,SOCNT ; SET THE ITERATION COUNT
MOV R3,-(SP) ; SAVE R3
MOV R4,-(SP) ; SAVE R4
MOV R5,-(SP) ; SAVE R5
MOV 5,SOMODE+1,R4 ; GET THE NUMBER OF DIGITS TO TYPE
NEG R4 ; SUBTRACT IT FOR MAX. ALLOWED
ADD 6,R4 ; SAVE IT FOR USE
MOV 5,SOFILL,R4 ; GET THE ZERO FILL SWITCH
MOV 12(SP),R5 ; PICKUP THE INPUT NUMBER
CLR R3 ; CLEAR THE OUTPUT WORD

```



# N05

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BINARY TO OCTAL (ASCII) AND TYPE

3302	014632	006105		15:	ROL R5	; ROTATE MSB INTO "C"
3303	014634	000404			BR 35	; GO DO MSB
3304	014636	006105		25:	ROL R5	; FORM THIS DIGIT
3305	014640	006105			ROL R5	
3306	014642	006105			ROL R5	
3307	014644	010503			MOV R5,R3	
3308	014646	006103		35:	ROL R3	; GET LSB OF THIS DIGIT
3309	014650	105367	000076		DECB \$OMODE	; TYPE THIS DIGIT?
3310	014654	100016			BPL 75	; BR IF NO
3311	014656	042703	177770		BIC #177770,R3	; GET RID OF JUNK
3312	014662	001002			BNE 45	; TEST FOR 0
3313	014664	005704			TST R4	; SUPPRESS THIS 0?
3314	014666	001403			BEQ 55	; BR IF YES
3315	014670	005204		45:	INC R4	; DON'T SUPPRESS ANYMORE 0'S
3316	014672	0703	000060		BIS #'0,R3	; MAKE THIS DIGIT ASCII
3317	014676	052703	000040	55:	BIS #' R3	; MAKE ASCII IF NOT ALREADY
3318	014702	110367	000040		MOVB R3,85	; SAVE FOR TYPING
3319	014706	104401	014746		TYPE 85	; GO TYPE THIS DIGIT
3320	014712	100367	000032	75:	DECB \$OCNT	; COUNT BY 1
3321	014716	0747			BGT 25	; BR IF MORE TO DO
3322	014720	07402			BLT 65	; BR IF DONE
3323	014722	07204			INC R4	; INSURE LAST DIGIT ISN'T A BLANK
3324	014724	07744			BR 25	; GO DO THE LAST DIGIT
3325	014726	012605		65:	MOV (SP)+,R5	; RESTORE R5
3326	014730	012604			MOV (SP)+,R4	; RESTORE R4
3327	014732	012603			MOV (SP)+,R3	; RESTORE R3
3328	014734	016666	000002 000004		MOV 2(SP),4(SP)	; SET THE STACK FOR RETURNING
3329	014742	012616			MOV (SP)+,(SP)	
3330	014744	000002			RTI	; RETURN
3331	014746	000		85:	.BYTE 0	; STORAGE FOR ASCII DIGIT
3332	014747	000			.BYTE 0	; TERMINATOR FOR TYPE ROUTINE
3333	014750	000		\$OCNT:	.BYTE 0	; OCTAL DIGIT COUNTER
3334	014751	000		\$OFILL:	.BYTE 0	; ZERO FILL SWITCH
3335	014752	000000		\$OMODE:	.WORD 0	; NUMBER OF DIGITS TO TYPE
3336						; ENTER HERE ON POWER FAILURE
3337						
3338						
3339	014754			SPWRON:		
3340	014754	010046		.PFAIL:	MOV R0,-(SP)	; SAVE R0-R5 ON PROCESSOR STACK
3341	014756	010146			MOV R1,-(SP)	
3342	014760	010246			MOV R2,-(SP)	
3343	014762	010346			MOV R3,-(SP)	
3344	014764	010446			MOV R4,-(SP)	
3345	014766	010546			MOV R5,-(SP)	
3346	014770	016746	163030		MOV 24,-(SP)	
3347	014774	010667	164116		MOV SP,SAVSP	; SAVE STACK POINTER
3348	015000	012767	015012 163016		MOV #RESTART,24	; SET UP FOR POWER UP TRAP
3349	015006	000000			HALT	; HALT ON POWER DOWN NORMAL
3350	015010	000777			BR .	
3351						
3352						; PROCESSOR WILL TRAP HERE WHEN POWER IS RESTORED
3353						
3354	015012	016706	164100	RESTAR:	MOV SAVSP,SP	; RESTORE STACK POINTER
3355	015016	012605			MOV (SP)+,R5	; RESTORE R0-R5
3356	015020	012604			MOV (SP)+,R4	
3357	015022	012603			MOV (SP)+,R3	

3358	015021	012602				MOV	(SP)+,R2
3359	015021	012601				MOV	(SP)+,R1
3360	015021	012600				MOV	(SP)+,R0
3361	015021	012607	014754	162764		MOV	#PFAIL,24 ;SET UP FOR POWER FAILURE
3362	015021	106427	000340			MTPS	#340
3363	015021	012706	001100			MOV	#STACK,SP
3364	015021	012706	001102			CLR	TEMP
3365	015021	012706	001076			INC	TEMP
3366	015021	001375				BNE	.-4
3367	015021	104413				CONVRT	
3368	015021	015106				PFTAB	
3369	015021	104401				TYPE	
3370	015021	015410				MPFAIL	
3371	015021	015410	164305			CLR	SERFLG
3372	015021	015410	164314			CLR	SERRPC
3373	015106	015177	163776			JMP	RETURN
3374	015106	000001				PFTAB:	1
3375	015110	000006	002			.BYTE	6,2
3376	015112	000007				RETURN	
3377	015114	000015	042012	053125		MTITLE:	.ASCIZ <15><12><12>/DUV11 DZDUQ-A TAPE A /<15><12>
3378	015122	000046	042040	042132			
3379	015130	000052	040455	052040			
3380	015136	000101	020105	020101			
3381	015144	000501	000				
3382	015147	000501	053012	041505		MVECTO:	.ASCIZ <15><12>/VEC ADD-/
3383	015154	000440	042104	000055			
3384	015162	000501	051461	020124		MREGAD:	.ASCIZ <15><12>/1ST DEV: REC CSR ADD-/
3385	015170	000440	035126	051040			
3386	015176	000440	041440	051123			
3387	015204	000440	042104	000055			
3388	015212	000501	052114	052114		MULT:	.ASCIZ <15><12>/MULT DEV ? (Y OR N)-/
3389	015220	000440	052105	037440			
3390	015228	000440	020131	051117			
3391	015234	000440	026451	000			
3392	015241	000501	046012	051501		MLASTD:	.ASCIZ <15><12>/LAST DEV: REC CSR ADDR-/
3393	015246	000501	042504	035126			
3394	015254	000501	041505	041440			
3395	015262	000501	040440	042104			
3396	015270	000522	000				
3397	015273	000751	042504	044526		DEVICE:	.ASCIZ /=DEVICE /
3398	015300	000440	020040	000			
3399	015308	000501	051412	046105		MCOV:	.ASCIZ <15><12>/SELECT TO RUN DACTREG/
3400	015312	000501	020124	047524			
3401	015318	000501	047124	040040			
3402	015324	000501	051124	043505			
3403	015330	000					
3404	015336	000501	047412	043126		MRANGE:	.ASCIZ <15><12>/OVFLO:RETYPE LAST DEV RXCSR ADDS-/
3405	015342	000475	051072	052105			
3406	015348	000501	020105	040514			
3407	015354	000521	042040	053105			
3408	015364	000501	041530	051123			
3409	015372	000440	042104	026523			
3410	015408	000					
3411	015401	00040	037440	000		MM:	.ASCIZ / ?/
3412	015405	000501	000012			MCRLF:	.ASCIZ <15><12>
3413	015410	000431	044501	026114		MPFAIL:	.ASCIZ /PFAIL, RESTART AT TEST IN PROGRESS/



3470 016102 020040 047040 053505  
3471 016110 020075 000040  
3472  
3473  
3474  
3475  
3476 016114 000000  
3477 016156 000000  
3478 016156 000000  
3479 016220 000000  
3480 016220 000000  
3481 016262 000000  
3482  
3483  
3484  
3485  
3486  
3487  
3488  
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3490  
3491  
3492  
3493  
3494  
3495  
3496 016262  
3497  
3498  
3499  
3500 016262  
3501 016262 004767 174376  
3502 016266 005067 163124  
3503 016272 022716 003364  
3504 016276 001413  
3505  
3506 016300 000406  
3507 016302 105777 163136  
3508 016306 100123  
3509 016310 017766 163132 177776  
3510 016316 032777 040000 163114  
3511 016324 001114  
3512  
3513 016326 000416  
3514  
3515 016330 013746 000004  
3516 016334 012737 016354 000004  
3517 016342 005737 177060  
3518 016346 012637 000004  
3519 016352 000463  
3520 016354 012626  
3521 016356 012637 000004  
3522 016362 000423  
3523 016364  
3524 016364 032777 000400 163046  
3525 016372 001404

```
MMNEW: .ASCIZ / NEW= /  
.EVEN  
;BUFFERS FOR INPUT-OUTPUT  
INBUF: 0  
.=.+40  
TEMP: 0  
.=.+40  
MDATA: 0  
.=.+40  
.SBTTL SCOPE HANDLER ROUTINE  
:*****  
:THIS ROUTINE CONTROLS THE LOOPING OF SUBTESTS. IT WILL INCREMENT  
:AND LOAD THE TEST NUMBER($TSTNM) INTO THE DISPLAY REG.(DISPLAY<7:C>)  
:AND LOAD THE ERROR FLAG ($ERRFLG) INTO DISPLAY<15:08>  
:THE SWITCH OPTIONS PROVIDED BY THIS ROUTINE ARE:  
:SW14=1 LOOP ON TEST  
:SW11=1 INHIBIT ITERATIONS  
:SW09=1 LOOP ON ERROR  
:S 08=1 LOOP ON TEST IN SWR<7:0>  
:CALL SCOPE ;;SCOPE=IOT  
$SCOPE:  
;SCOPE LOOP AND INTERATION HANDLER  
.SCOPE:  
JSR PC,CKSWR  
CLR $ERRPC ;CLEAR LAST ERROR PC  
CMP #TST1+2,(SP) ;IS SCOPE AT BEGINING OF TEST 1?  
BEQ $XTSTR ;YES NO LOOP.  
TTST: BR 1$ ;GO TO 1$ (IF LOCK SW02=1)  
TSTB #STKS ;KEYBOARD DONE?  
BPL $OVER ;BR IF NO  
MOV #STKB,-2(SP) ;CLEAR DONE BIT  
1$: BIT #BIT14,$SWR ;LOOP ON PRESENT TEST?  
BNE $OVER ;YES IF SW14=1  
:#####START OF CODE FOR THE XOR TESTER#####  
$XTSTR: BR 6$ ;IF RUNNING ON THE "XOR" TESTER CHANGE  
;THIS INSTRUCTION TO A "NOP" (NOP=240)  
MOV #ERRVEC,-(SP) ;SAVE THE CONTENTS OF THE ERROR VECTOR  
MOV #SS,$ERRVEC ;SET FOR TIMEOUT  
TST #177060 ;TIME OUT ON XOR?  
MOV (SP)+,$ERRVEC ;RESTORE THE ERROR VECTOR  
BR $SVLAD ;GO TO THE NEXT TEST  
5$: CMP (SP)+,(SP)+ ;CLEAR THE STACK AFTER A TIME OUT  
MOV (SP)+,$ERRVEC ;RESTORE THE ERROR VECTOR  
BR 7$ ;LOOP ON THE PRESENT TEST  
6$;#####END OF CODE FOR THE XOR TESTER#####  
BIT #BIT08,$SWR ;LOOP ON SPEC. TEST?  
BEQ 2$ ;BR IF NO
```

```

3526 016374 127767 163040 163000      CMPB 2SWR,$STSTM      ;; ON THE RIGHT TEST?  SWR<7:0>
3527 016402 001465                BEQ  $OVER           ;; BR IF YES
3528 016404 105767 162773          2S:  T  'B          SERFLG           ;; HAS AN ERROR OCCURRED?
3529 016410 001421                BEJ  3S              ;; BR IF NO
3530 016412 126767 162777 162763    CMPB SERMAX,SERFLG   ;; MAX. ERRORS FOR THIS TEST OCCURRED?
3531 016420 101015                BHI  3S              ;; BR IF NO
3532 016422 032777 001000 163010    BIT  #BIT09,2SWR     ;; LOOP ON ERROR?
3533 016430 001404                BEQ  4S              ;; BR IF NO
3534 016432 016767 162752 162746    7S:  MOV  $LPERR,$LPADR ;; SET LOOP ADDRESS TO LAST SCOPE
3535 016440 000446                BR   $OVER           ;;
3536 016442 105067 162735          4S:  CLRB SERFLG      ;; ZERO THE ERROR FLAG
3537 016446 005067 163040          CLR  $TIMES          ;; CLEAR THE NUMBER OF ITERATIONS TO MAKE
3538 016452 000415                BR   1S              ;; ESCAPE TO THE NEXT TEST
3539 016454 032777 004000 162756    3S:  BIT  #BIT11,2SWR   ;; INHIBIT ITERATIONS?
3540 016462 001011                BNE  1S              ;; BR IF YES
3541 016464 005767 163044          TST  $PASS           ;; IF FIRST PASS OF PROGRAM
3542 016470 001406                BEQ  1S              ;; INHIBIT ITERATIONS
3543 016472 002267 162706          INC  $ICNT           ;; INCREMENT ITERATION COUNT
3544 016476 026767 163010 162700    CMP  $TIMES,$ICNT    ;; CHECK THE NUMBER OF ITERATIONS MADE
3545 016504 002024                BGE  $OVER           ;; BR IF MORE ITERATION REQUIRED
3546 016506 012767 000001 162670    1S:  MOV  #1,$ICNT     ;; REINITIALIZE THE ITERATION COUNTER
3547 016514 016767 000056 162770    MOV  $SMXCNT,$TIMES ;; SET NUMBER OF ITERATIONS TO DO
3548 016522 105267 162654          $SVLAD: INCB $STSTM   ;; COUNT TEST NUMBERS
3549 016526 116767 162650 162776    MOVB $STSTM,$STSTM  ;; SET TEST NUMBER IN APT MAILBOX
3550 016534 011667 162646          MOV  (SP),$LPADR    ;; SAVE SCOPE LOOP ADDRESS
3551 016540 011667 162644          MOV  (SP),$LPERR    ;; SAVE ERROR LOOP ADDRESS
3552 016544 005067 162744          CLR  $ESCAPE        ;; CLEAR THE ESCAPE FROM ERROR ADDRESS
3553 016550 112767 000001 162637    MOVB #1,$SERMAX     ;; ONLY ALLOW ONE(1) ERROR ON NEXT TEST
3554 016556 016777 162620 162656    $OVER: MOV  $STSTM,$DISPLAY ;; DISPLAY TEST NUMBER
3555 016564 016716 162616          MOV  $LPADR,(SP)    ;; FUDGE RETURN ADDRESS
3556 016570 000002          4S:  RTI
3557 016572 001407          BRW: 1407
3558 016574 000432          BRX: 432
3559 016576 000005          $SMXCNT: 5          ;; MAX. NUMBER OF ITERATIONS
3560          .SBTTL TRAP DECODER
3561
3562          ;; *****
3563          ;; THIS ROUTINE WILL PICKUP THE LOWER BYTE OF THE "TRAP" INSTRUCTION
3564          ;; AND USE IT TO INDEX THROUGH THE TRAP TABLE FOR THE STARTING ADDRESS
3565          ;; OF THE DESIRED ROUTINE. THEN USING THE ADDRESS OBTAINED IT WILL
3566          ;; GO TO THAT ROUTINE.
3567
3568 016600 010046          $TRAP: MOV  RO,-(SP)   ;; SAVE RO
3569 016602 016600 000002    MOV  2(SP),RO      ;; GET TRAP ADDRESS
3570 016606 005740          TST  -(RO)         ;; BACKUP BY 2
3571 016610 111000          MOVB (RO),RO      ;; GET RIGHT BYTE OF TRAP
3572 016612 006300          ASL  RO            ;; POSITION FOR INDEXING
3573 016614 016000 016634    MOV  $TRPAD(RO),RO ;; INDEX TO TABLE
3574 016620 000200          RTS  RO            ;; GO TO ROUTINE
3575
3576
3577          ;; THIS IS USE TO HANDLE THE "GETPRI" MACRO
3578
3579 016622 011646          $TRAP2: MOV  (SP),-(SP) ;; MOVE THE PC DOWN
3580 016624 016666 000004 000002    MOV  4(SP),2(SP)   ;; MOVE THE PSW DOWN
3581 016632 000002          RTI               ;; RESTORE THE PSW

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016642 014526  
016644 014566  
  
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016650 013316  
016652 013424  
016654 013434  
016656 013634  
016660 013674  
016662 013726  
016664 014104  
  
016666 006367 000044  
016672 006367 000040  
016676 006367 000034  
016702 006367 000030  
016706 006367 000024  
016712 016767 000020 000020  
016720 162767 000001 000012  
016726 042767 000037 000004  
  
016742 016767 000126 162742  
016750 005267 000120  
016754 016767 000114 162732  
016762 006367 000106  
016766 016767 000102 162722  
016774 016767 000074 162720  
017002 006367 000066  
017006 016767 000062 162704  
017014 016767 000054 162702  
017018 006367 000046  
017034 005267 000034 162672  
017040 016767 000030 162662  
017046 005267 000022  
017052 016767 000016 162652

```
.SBTTL TRAP TABLE
; *THIS TABLE CONTAINS THE STARTING ADDRESSES OF THE ROUTINES CALLED
; *BY THE "TRAP" INSTRUCTION.
;
; ROUTINE
; -----
$TRPAD: .WORD $TRAP2
        $TYPE  :: CALL=TYPE      TRAP+1(104401)  TTY TYPEOUT ROUTINE
        $TYPOC  :: CALL=TYPOC    TRAP+2(104402)  TYPE OCTAL NUMBER (WITH LEADING ZEROS)
        $TYPOS  :: CALL=TYPOS    TRAP+3(104403)  TYPE OCTAL NUMBER (NO LEADING ZEROS)
        $TYPON  :: CALL=TYPON    TRAP+4(104404)  TYPE OCTAL NUMBER (AS PER LAST CALL)
;
        .SCOP1  :: CALL=SCOP1    TRAP+5(104405)
        .INSTR  :: CALL=INSTR    TRAP+6(104406)
        .INSTER :: CALL=INSTER   TRAP+7(104407)
        .PARAM  :: CALL=PARAM    TRAP+10(104410)
        .SAVOS  :: CALL=SAVOS    TRAP+11(104411)
        .RESOS  :: CALL=RESOS    TRAP+12(104412)
        .CONVRT :: CALL=CONVRT   TRAP+13(104413)
        .SETFLG :: CALL=SETFLG   TRAP+14(104414)
; *****
; UTILITIES
; *****
; THIS UTILITY CALCULATES PRIORITY LEVEL
DULEV: ASL     DUPRT     ; SHIFT LEFT
        ASL     DUPRT
        ASL     DUPRT
        ASL     DUPRT
        ASL     DUPRT
        MOV     DUPRT, LESS1 ; MOVE THIS TO LESS1
        SUB     #1, LESS1   ; CREATE LESS1
        BIC     #37, LESS1  ; CLEAR TNZVC
        RTS
        PC
DUPRT: PRS
LESS1: PR4 ; LEVEL TO ALLOW INTERRUPTS
; NEW DU ADDRESSES
DUADDR: MOV     DU     E, RXCSR ; XXX0
        INC     DU
        MOV     DU     E, HRXCSR ; XXX1
        INC     DU
        MOV     DU     E, RXDBUF ; XXX2
        MOV     DU     E, PARCSR ; XXX2
        INC     DU
        MOV     DU     E, HRXDBUF ; XXX3
        MOV     DU     E, HPARCSR ; XXX3
        INC     DU
        MOV     DUBASE, TXCSR ; XXX4
        INC     DUBASE
        MOV     DU     E, HTXCSR ; XXX5
        INC     DU
        MOV     DUBASE, TXDBUF ; XXX6
```

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3638 017060 005267 000010      INC      DUBASE
3639 017064 016767 000004 162642    MOV      DUBASE,HTXDBUF ;XXX7
3640 017072 000207                RTS      PC
3641 017074 000000                DUBASE: 0
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; THIS UTILITY POKES THE MAINT DATA BASED UPON THE
; INFORMATION CONTAINED IN STMP1 AND IT IS
; SHIFTED IN BY THE CONTENTS OF SHIFT
RPOKE: BIC      @MTDATA,@TXCSR
        CLR      STMP2
        ROR      STMP1 ;FORCE CARRY
        ROR      STMP2 ;PICK UP CARRY IN BIT 15
        ASR      STMP2 ;SHIFT INTO BIT 14
        BIC      @BIT15,STMP2 ;CLR BIT 15
        BIS      STMP2,@TXCSR ;POKE MAINT DATA
        BIC      @CLK,@TXCSR ;POKE CLK
        BIS      @CLK,@TXCSR ;
        DEC      SHIFT
        BNE      RPOKE
        RTS      PC

; THIS ROUTINE CALCULATES ODD PARITY FOR AN 8 BIT CHAR
0008:  MOV      STMP1,STMP2 ;SAVE TEMP1
        CLR      STMP3
        MOV      @B.,(PC)+
45:    0
15:    ROR      STMP2
        ADC      STMP3
        DEC      45
        BNE      15
        ROR      STMP3
        BCS      25
        BIS      @BIT8,STMP1 ;SET ODD PARITY
        BR       35
25:    BIC      @BIT8,STMP1 ;CLR EVEN PARITY
        ;STMP1 NOW HAS ODD PARITY CHARACTER
35:    RTS      PC

; THIS ROUTINE CALCULATES EVEN PARITY FOR AN 8 BIT CHARACTER
EVEN8: MOV      STMP1,STMP2 ;SAVE TEMP1
        CLR      STMP3
        MOV      @B.,(PC)+
45:    0
15:    ROR      STMP2
        ADC      STMP3
        DEC      45
        BNE      15
        ROR      STMP3
        BCC      25
        BIS      @BIT8,STMP1 ;SET EVEN PARITY
        BR       35
25:    BIC      @BIT8,STMP1 ;CLR ODD PARITY
        ;STMP1 NOW HAS EVEN PARITY CHARACTER
35:    RTS      PC

TRPREG: ADD      @2,(SP) ;ALLOW IT TO "CRUNCH" INTO ERROR BACK
        ;IN MAIN PART OF THE PROGRAM

```

H06

DZDUQ-A MACY11 27(1006) 03-FEB-77 07:44 PAGE 74  
DZDUQA.M11 27-JAN-77 09:46 TRAP TABLE

3694 017340 000002 RTI  
3695 000001 .END

























		3530	3537	3538	3539	3551	3554	3559						
SSUREG	001550	887#	1168											
STK=	000000	3492	3493	3526										
STESTN	001532	878#	3549#											
STINES	001512	864#	1144#	3537#	3544	3547#	3559							
STKB	001446	843#	2878	3001	3009	3509								
STKS	001444	842#	2876	2999	3507									
STMP0	001476	858#												
STMP1	001500	859#	2425#	2439#	2498#	2512#	2571#	2585#	2644#	2658#	2712#	2724#	2728#	2767#
		2779#	2783#	3648#	3660	3670#	3672#	3677	3687#	3689#				
STMP2	001502	860#	3647#	3649#	3650#	3651#	3652	3660#	3664#	3677#	3681#			
STMP3	001504	861#	3661#	3665#	3668#	3678#	3682#	3685#						
STMP4	001506	862#												
STMP5	001510	863#												
STN =	000062	534#	1344	1346#	1360	1362#	1375	1377#	1390	1392#	1405	1407#	1420	1422#
		1428	1430#	1457	1459#	1495	1497#	1524	1526#	1544	1546#	1564	1566#	1584
		1556#	1604	1606#	1624	1626#	1644	1646#	1664	1666#	1684	1686#	1706	1708#
		1728	1730#	1748	1750#	1768	1770#	1788	1790#	1820	1822#	1834	1836#	1869
		1871#	1897	1899#	1925	1927#	1936	1938#	1947	1949#	1958	1960#	1968	1970#
		1979	1981#	1991	1993#	2002	2004#	2013	2015#	2024	2026#	2034	2036#	2072
		2074#	2076	2088#	2101	2103#	2341	2343#	2368	2370#	2404	2406#	2477	2479#
		2550	2552#	2623	2625#	2691	2693#	2746	2748#					
STPB	001452	845#	2977#	2998	3009#									
STPFLG	001457	849#	2976	2978										
STPS	001450	844#	2975	2988	3007									
STRAP	016600	1140	3568#											
STRAP2	016622	3579#	3570											
STRP =	000015	3583#	3592#	3593#	3594#	3595#	3597	3598#	3599#	3600#	3601#	3602#	3603#	3604#
		3605#												
STRPAD	016634	3573	3590#											
STSTM	002142	1114#												
STSTM	001402	822#	1178#	2849#	3173	3204	3210	3487	3526	3548#	3549	3554	3560	
STY =	##### U	3595												
STY =	##### U	3595												
STYPE	013034	534	2926#	3583	3591									
STYPEC	013246	2956	2963	2970	2975#	2976								
STYPEX	013314	2931	2933	2986#										
STYPOC	014552	3279#	3592											
STYPON	014566	3278	3291#	3594										
STYPOS	014576	3274#	3593											
SUNIT	001540	881#												
SUNITM	002146	1116#												
SLUR	001552	888#	1203											
SVECT1	001576	913#												
SVECT2	001600	914#												
SXTSTR	016326	3504	3513#											
SOFILL	014751	3285#	3289#	3299	3334#									
S4OCAT =	##### U	3183	3510											
	017342	534#	568#	681#	684#	689#	744#	745#	819#	870	1076#	1090	1091#	1093#
		1095#	1101	1102#	1104#	1106#	1133	1147	1148	1349	1352	1365	1368	1380
		1383	1395	1398	1410	1413	1423	1432	1436	1446	1450	1461	1465	1475
		1479	1489	1499	1503	1513	1517	1528	1532	1538	1548	1552	1558	1568
		1572	1578	1588	1592	1598	1608	1612	1618	1628	1632	1638	1648	1652
		1658	1668	1672	1678	1678	1692	1698	1710	1714	1720	1732	1736	1742
		1752	1756	1762	1772	1776	1782	1801	1805	1813	1824	1828	1844	1849
		1857	1863	1874	1881	1891	1906	1910	1917	1929	1940	1951	1962	1972







CROSS REFERENCE TABLE -- MACRO NAMES

SSNEWT	678	1344	1360	1375	1390	1405	1420	1428	1457	1495	1524	1544	1564	1584	1604
	1624	1644	1664	1684	1706	1728	1748	1768	1788	1820	1834	1869	1897	1925	1936
	1947	1958	1968	1979	1991	2002	2013	2024	2034	2072	2086	2101	2341	2368	2404
	2477	2550	2623	2691	2746										
SSSET	3583	3592	3593	3594	3597	3598	3599	3600	3601	3602	3603	3604			
SETH	1165														
XIP	678														
EQAT	333	568													
XC	333														
SETUP	333	1118													
XTI	333	1086													
PTB	333	871													
PTH	333	1096													
PYTY	333	534													
SCATC	333														
SCHTA	333	813													
SP	333														
SO	333	3156													
BERRT	333	3212													
SPONE	333														
SCOP	333	3482													
STRAP	333	3560													
STYPE	333	3509													
STYPO	333	3259													

. ABS. 017342 000

ERRORS DETECTED: 0  
DEFAULT GLOBALS GENERATED: 0

DZDUQA, DZDUQA.SEG/SOL/CRF+DZDUQ1/EQ:RUNA, DZDUQ2, DZDUQA  
RUN-TIME: 19 14 1 SECONDS  
RUN-TIME RATIO: 108/35=3.0  
CORE USED: 31K (62 PAGES)