Appendix TS

Technical Specifications for Physical/Electrical Interfaces

Physical/Electrical Characteristics of Hierarchical Digital Interfaces (ITU–T Recommendation G.703)

1544kbit/s Interface

Bit rate	1544kbit/s	
Tolerance	±50ppm	
Pair(s) in each direction of transmission	symmetric	
Test load impedance	100 Ω resistive	
Code	AMI o B8ZS	
Pulse shape	within the mask of Fig. TS–1	
Signal level(1)	*Power at 772kHz:*	+12dBm to +19dBm
	Power at 1544kHz:	At least 25dB below the power at 772kHz

For the characteristics of maximum jitter at output port, of maximum tolerable input jitter and for Jitter transfer function refer to section "Control of Jitter in Hierarchical Digital Interfaces"

NOTE (1) ***The Signal level is the power level measured in a 3kHz bandwidth at the point where the signal arrives at the distribution frame for an all 1s pattern transmitted***

Tab. TS–1 *1544kbit/s Interface Characteristics*

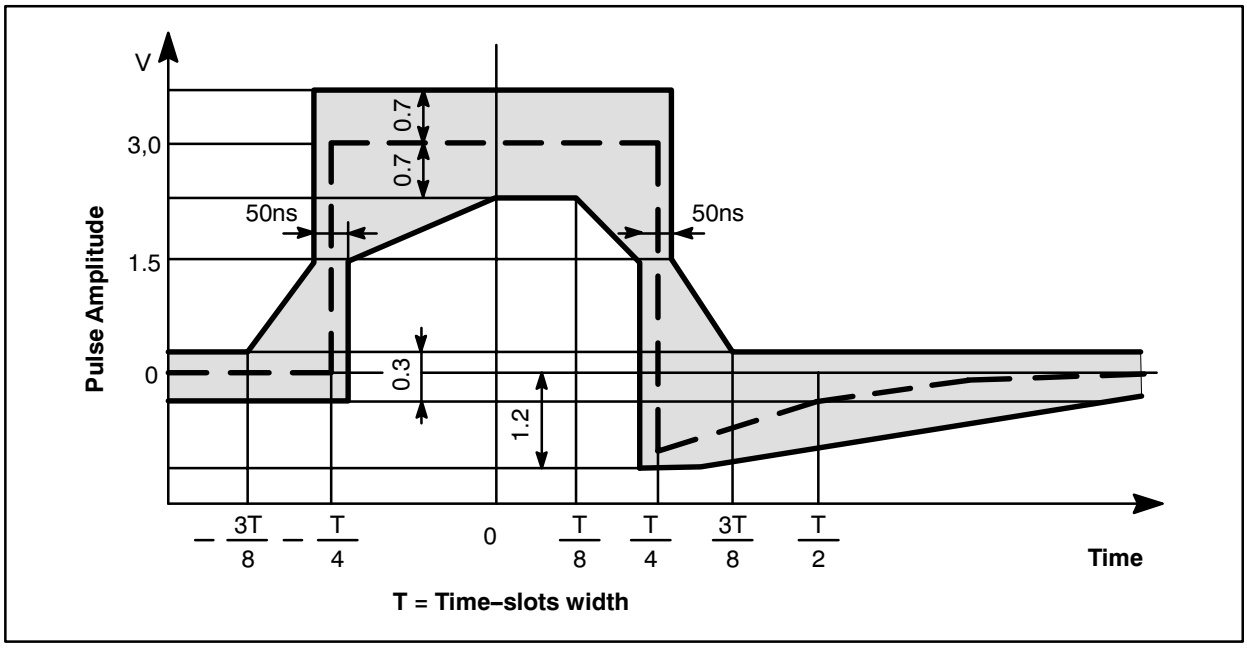


Fig. TS–1 *Pulse mask at 1544kbit/s Interface*

2048kbit/s Interface

Bit rate	2048kbit/s
Tolerance	±50ppm
Pair(s) in each direction	coaxial or symmetric
Test load impedance	75Ω (coax) or 120Ω (symmetric) resistive
Code	HDB3
Pulse shape	within the mask of Fig. TS–2
Nominal peak voltage of a mark (pulse)	2.37V
Peak voltage of a space (no pulse)	0 ± 0.237V
Nominal pulse width	244 ns
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05
Return loss	>12 dB in 51 to 102kHz bandwidth >18 dB in 102 to 2048kHz bandwidth >14 dB in 2048 to 3042kHz bandwidth

For the characteristics of maximum jitter at output port, of maximum tolerable input jitter and for Jitter transfer function refer to section "Control of Jitter in Hierarchical Digital Interfaces"

Tab. TS–2 *2048kbit/s Interface Characteristics*

The digital signal presented at the input port shall be as defined in Tab. TS–2 but modified by the characteristics of the interconnecting pair. The attenuation of this pair shall be assumed to follow a $\sqrt{f}$ law and the loss at the frequency of 1024kHz shall be in the range 0 to 6dB.

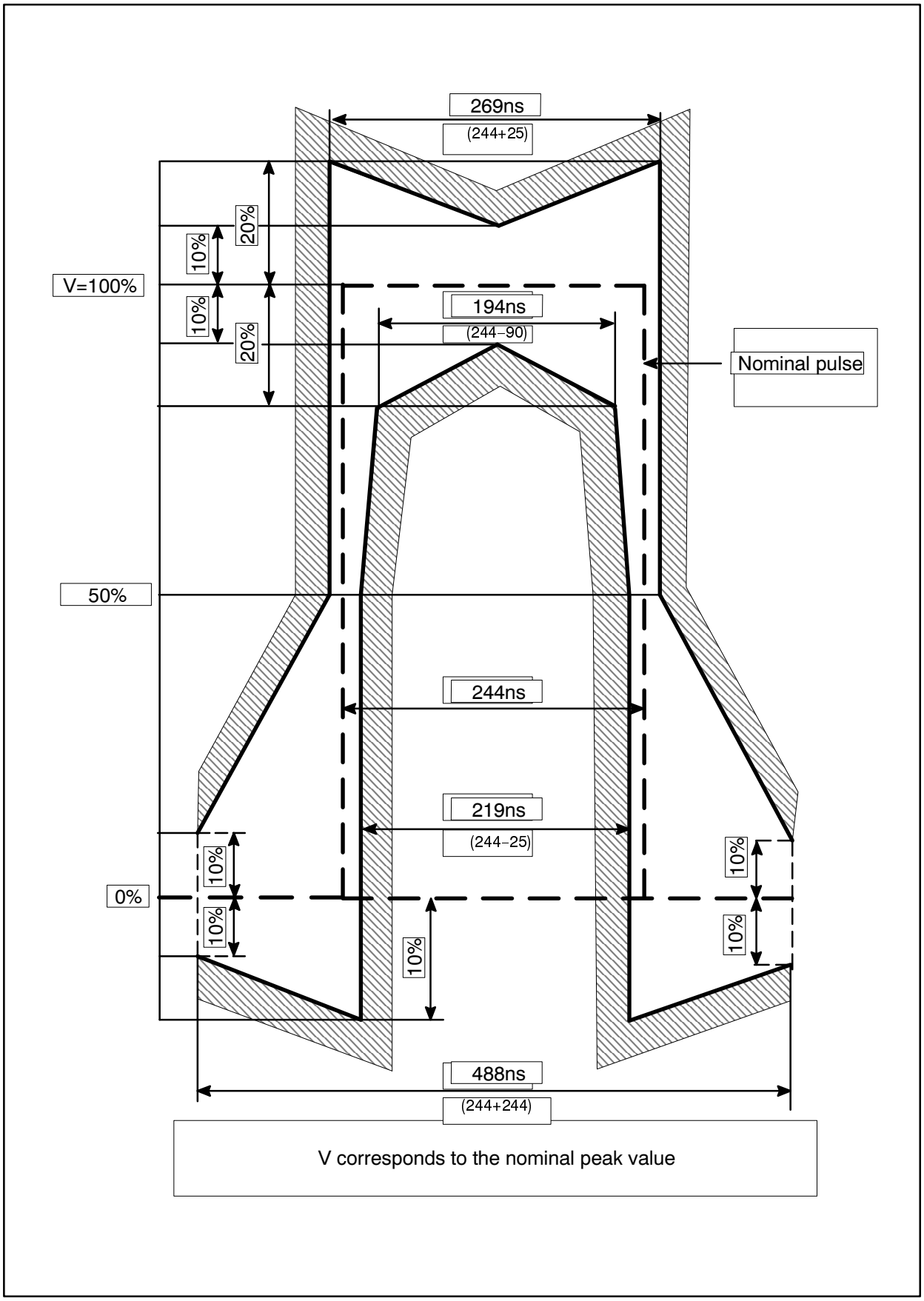


Fig. TS–2 *Pulse mask at 2048kbit/s Interface*

34368kbit/s Interface

Bit rate	34368kbit/s
Tolerance	±20ppm
Pair(s) in each direction	coaxial
Test load impedance	75Ω resistive
Code	HDB3
Pulse shape	within the mask of Fig. TS–3
Nominal peak voltage of a mark (pulse)	1.0V
Peak voltage of a space (no pulse)	0 ± 0.1V
Nominal pulse width	14.55ns
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05
Return loss	>12 dB in 860 to 1720kHz bandwidth >18 dB in 1720 to 34368kHz bandwidth >14 dB in 34368 to 51550kHz

For the characteristics of maximum jitter at output port, of maximum tolerable input jitter and for Jitter transfer function refer to section "Control of Jitter in Hierarchical Digital Interfaces"

Tab. TS–3 *34368kbit/s Interface Characteristics*

The digital signal presented at the input port shall be as defined in Tab. TS–3 but modified by the characteristics of the interconnecting pair. The attenuation of this pair shall be assumed to follow a $\sqrt{f}$ law and the loss at the frequency of 17184kHz shall be in the range 0 to 12dB.

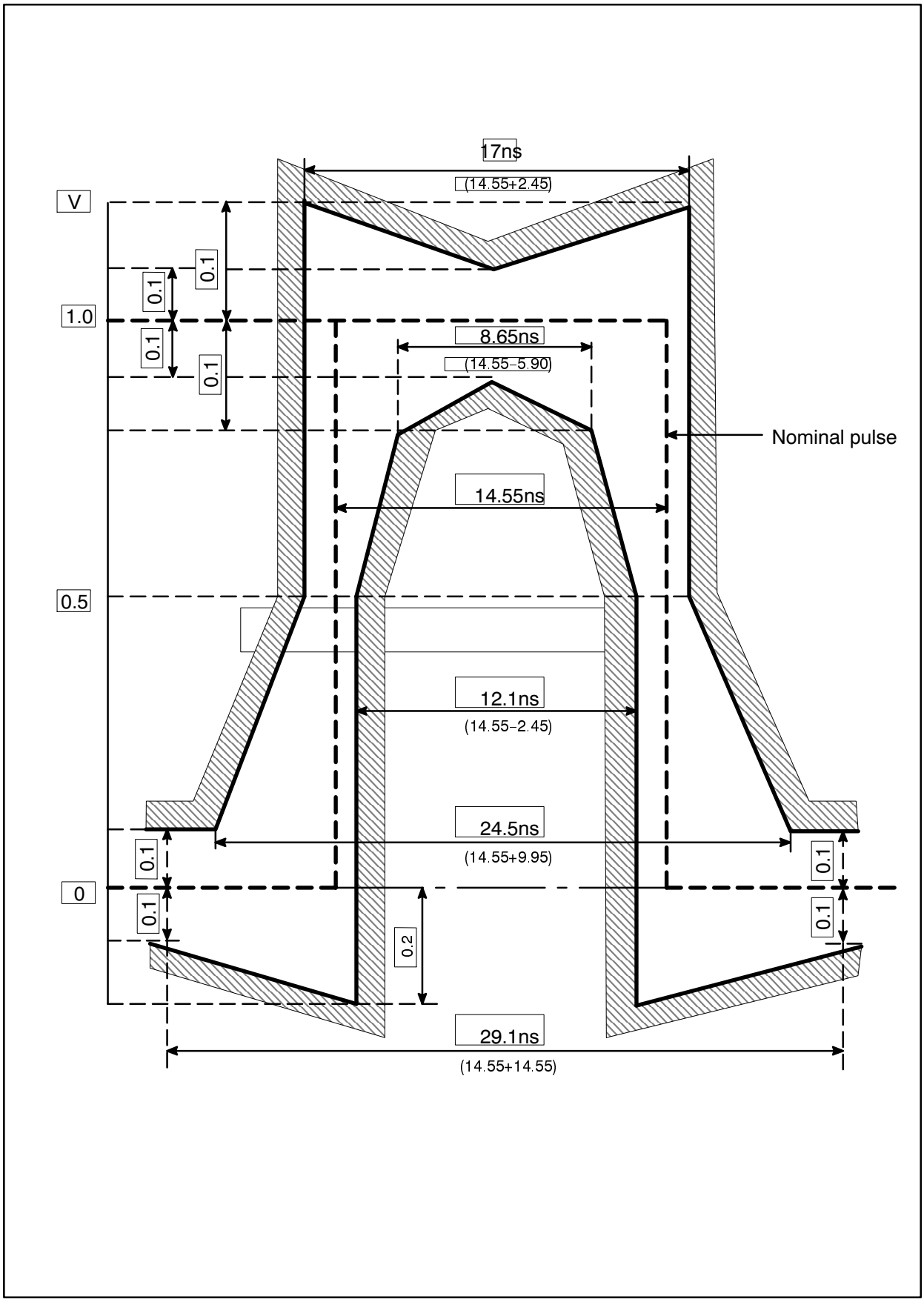


Fig. TS–3 *Pulse mask at 34368kbit/s Interface*

44736kbit/s Interface

Bit rate	44736kbit/s
Tolerance	±20ppm
Pair(s) in each Tx direction	coaxial
Test load impedance	75 Ω resistive
Code	B3ZS
Pulse shape	within the mask of Fig. TS–4
Signal level(1)	*Power at 22638kHz :* –1.8dBm to +5.7dBm
	Power at 44736kHz : At least 25dB below power at 22638kHz

For the characteristics of maximum jitter at output port, of maximum tolerable input jitter and for Jitter transfer function refer to section "Control of Jitter in Hierarchical Digital Interfaces"

NOTE (1) ***The Signal level is the power level measured in a 3kHz bandwidth at the point where the signal arrives at the distribution frame for an all 1s pattern transmitted***

Tab. TS–4 *44736kbit/s Interface Characteristics*

	T	Curve Value
Lower curve	$T \leq -0.36$	0
	$-0.36 \leq T \leq 0.28$	$0.5\,[1 + \sin\frac{\pi}{2}(1 + \frac{T}{0.18})]$
	$0.28 \leq T$	$0.11\,e^{-3.42\,(T-0.3)}$
Upper curve	$T \leq -0.65$	0
	$-0.65 \leq T \leq 0$	$1.05[1 - e^{-4.6\,(T+0.65)}]$
	$0 \leq T \leq 0.36$	$0.5\,[1 + \sin\frac{\pi}{2}(1 + \frac{T}{0.34})]$
	$0.36 \leq T$	$0.05 + 0.407e^{-1.84\,(T-0.36)}$

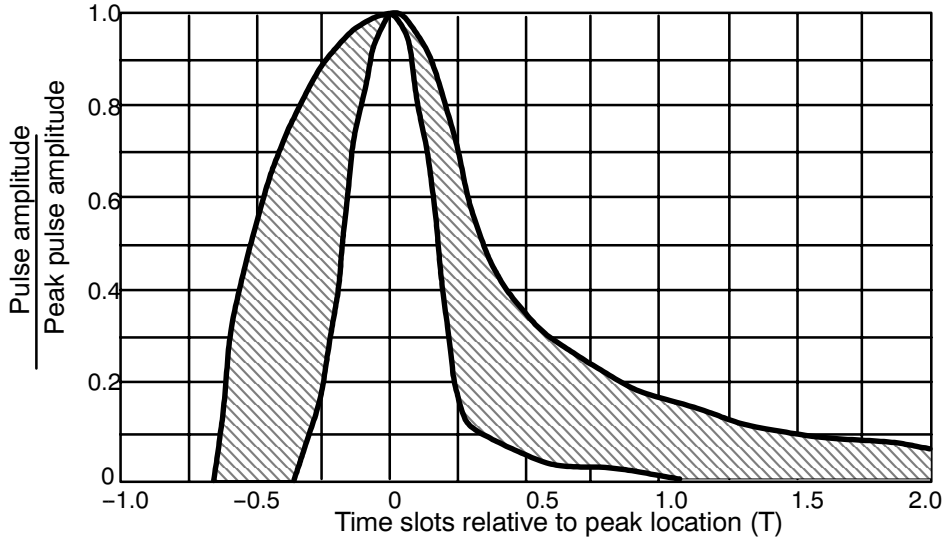


Fig. TS–4 *Pulse mask at 44736kbit/s interface*

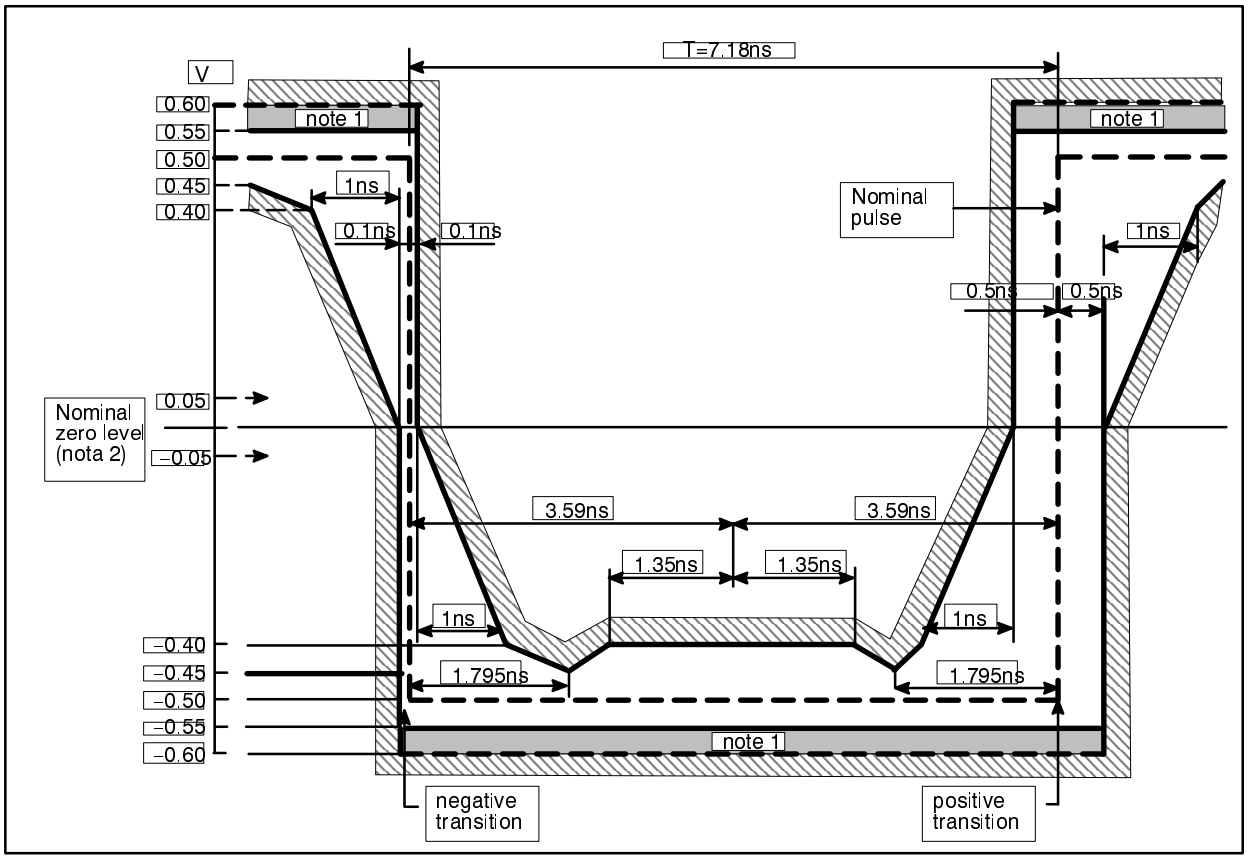
139264kbit/s Interface

Bit rate	139264kbit/s
Tolerance	±15ppm
Pair(s) for each direction	coaxial
Test load impedance	75Ω resistive
Code	CMI
Pulse shape	within the mask of Fig. TS–5 and Fig. TS–6
Peak–to–peak voltage	1 ± 0.1V
Rise time between 10% and 90% amplitudes of the measured steady state amplitude	3.2ns
Transition timing tolerance (referred to the mean value of the 50% amplitude points of negative transition)	Negative transitions : + 0.1ns Positive transitions at unit interval boundaries : +0.5ns Positive transitions at mid–interval : +0.35ns
Return loss	>15 dB in 7 to 210MHz bandwidth

For the characteristics of maximum jitter at output port, of maximum tolerable input jitter and for Jitter transfer function refer to section "Control of Jitter in Hierarchical Digital Interfaces"

Tab. TS–5 *139264kbit/s Interface Characteristics*

The digital signal presented at the input port shall be as defined in Tab. TS–5 but modified by the characteristics of the interconnecting pair. The attenuation of this pair shall be assumed to follow a $\sqrt{f}$ law and the loss at the frequency of 70MHz shall be in the range 0 to 12dB.



Note 1

The maximum steady state amplitude should not exceed the 0.55V limit. Overshoots and other transients are permitted to fall into dotted area, bounded by the amplitude levels 0.55V and 0.6V, provided that they not do not exceed the steady state level by more than 0.05V.

Note 2

For all measurements using these mask, the signal should be AC coupled, using a capacitor of not less than 0.01μf, to the input of the oscilloscope used for measurements. The nominal zero level for both mask should be aligned with the oscilloscope trace with no input signal. With the signal than applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05V of the nominal zero level of the mask.

Note 3

Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding and succeeding pulses. For actual verification, if a timing signal associated with the source of the interface signal is available, its use as a timing reference for an oscilloscope is preferred. Otherwise, compliance with the relevant mask may be tested by means of all–0s and all–1s signals,respectively.

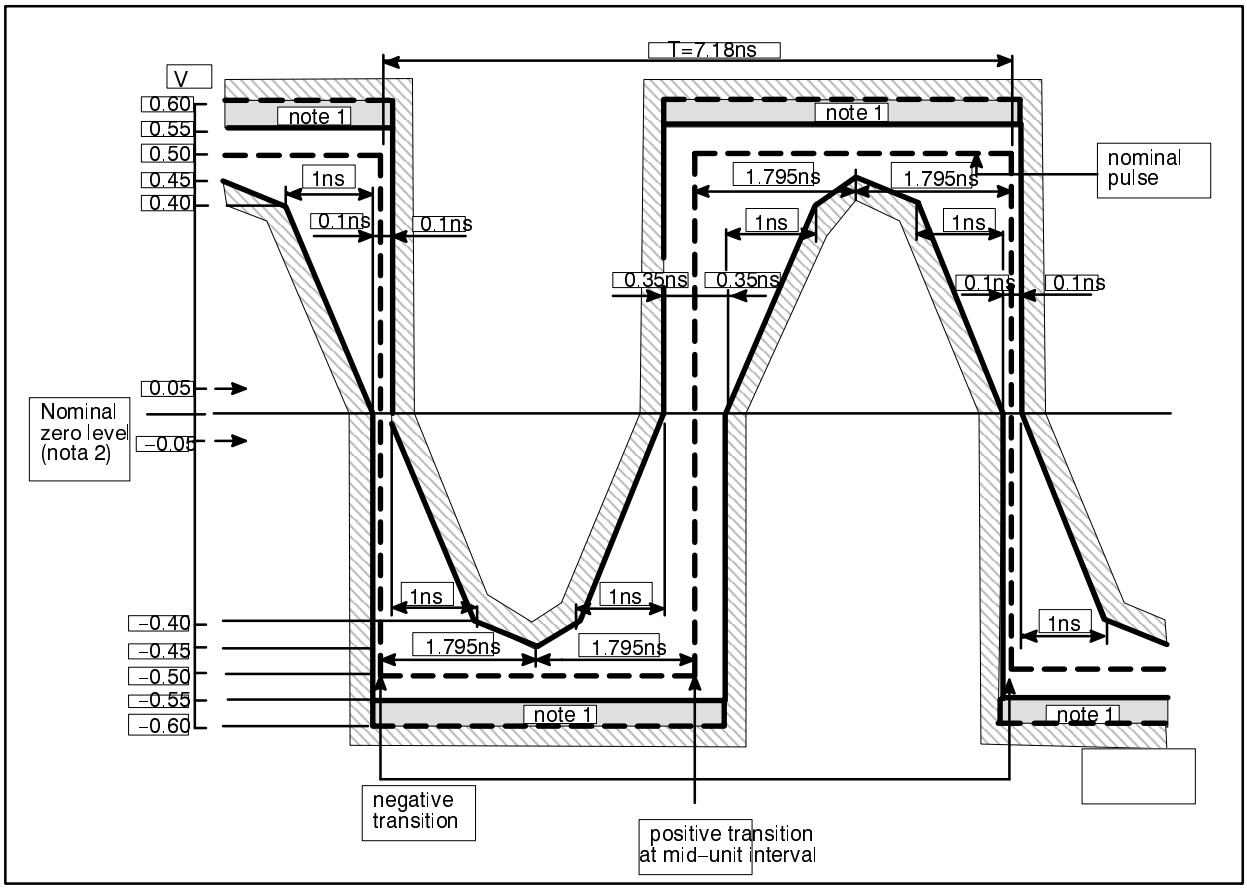
Note 4

For the purpose of these mask, the rise time and decay time should be measured between –0.4V and 0.4V, and should not exceed 2ns.

Note 5

The inverse pulse will have the same characteristics, nothing that the timing tolerance at the zero level of the negative and positive transition are ±0.1ns and ±0.5ns respectively.

Fig. TS–5 *Pulse mask (binary ”1”) at 139262kbit/s Interface*



Note 1

The maximum steady state amplitude should not exceed the 0.55V limit. Overshoots and other transients are permitted to fall into dotted area, bounded by the amplitude levels 0.55V and 0.6V, provided that they not do not exceed the steady state level by more than 0.05V.

Note 2

For all measurements using these mask, the signal should be AC coupled, using a capacitor of not less than 0.01μf, to the input of the oscilloscope used for measurements. The nominal zero level for both mask should be aligned with the oscilloscope trace with no input signal. With the signal than applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05V of the nominal zero level of the mask.

Note 3

Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding and succeeding pulses. For actual verification, if a timing signal associated with the source of the interface signal is available, its use as a timing reference for an oscilloscope is preferred. Otherwise, compliance with the relevant mask may be tested by means of all–0s and all–1s signals,respectively.

Note 4

For the purpose of these mask, the rise time and decay time should be measured between –0.4V and 0.4V, and should not exceed 2ns.

Fig. TS–6 *Pulse mask (binary ”0”) at 139262kbit/s Interface*

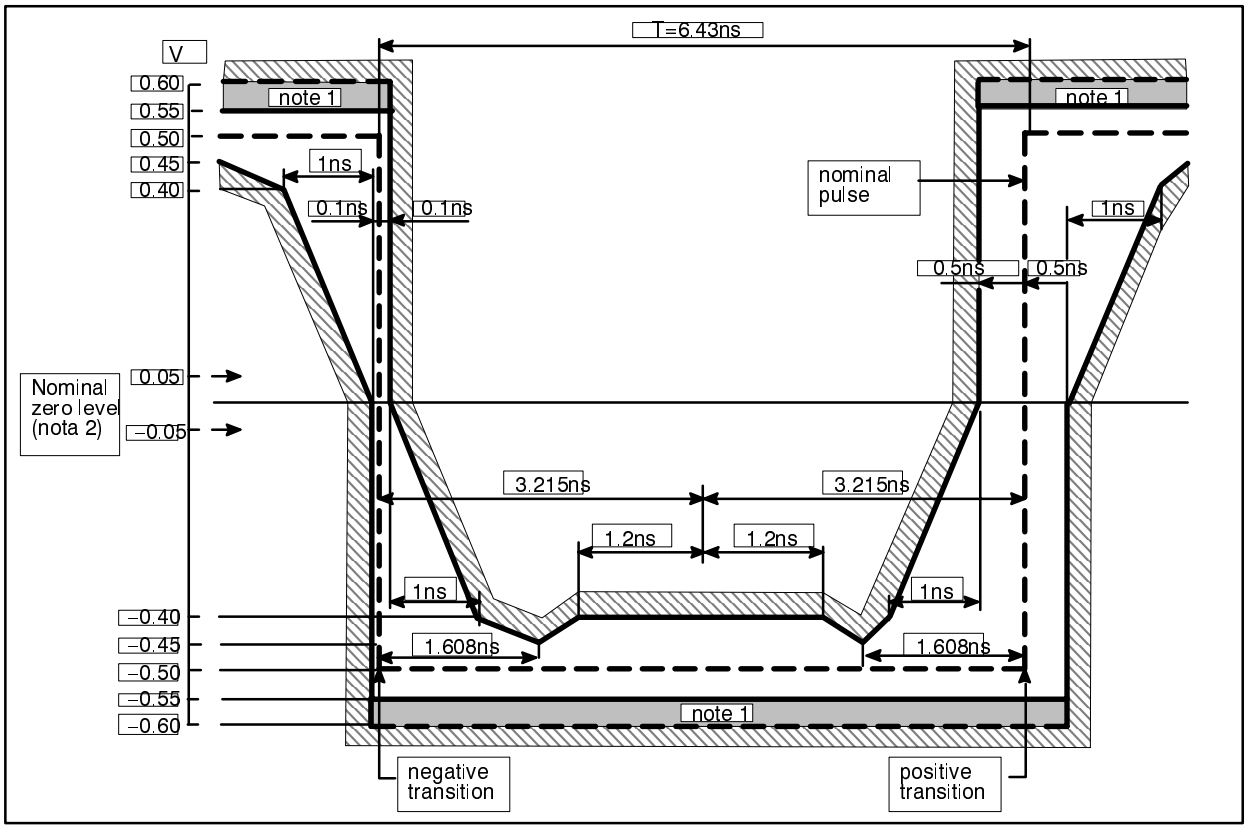
155520kbit/s Interface

Bit rate	155520kbit/s
Tolerance	±20ppm
Pair(s) for each direction	coaxial
Test load impedance	75Ω resistive
Code	CMI
Pulse shape	within the mask of Fig. TS–7 and Fig. TS–8
Peak–to–peak voltage	1 ± 0.1V
Rise time between 10% and 90% amplitudes of the measured steady state amplitude	3.2ns
Transition timing tolerance (referred to the mean value of the 50% amplitude points of negative transition)	Negative transitions : + 0.1ns Positive transitions at unit interval boundaries : +0.5ns Positive transitions at mid–interval : +0.35ns
Return loss	>15 dB in 8 to 240MHz bandwidth

For the characteristics of maximum jitter at output port, of maximum tolerable input jitter and for Jitter transfer function refer to section "Control of Jitter in Hierarchical Digital Interfaces"

Tab. TS–6 *155520kbit/s Interface Characteristics*

The digital signal presented at the input port shall be as defined in Tab. TS–6 but modified by the characteristics of the interconnecting pair. The attenuation of this pair shall be assumed to follow a $\sqrt{f}$ law and the loss at the frequency of 78MHz shall be in the range 0 to 12.7dB.



Note 1

The maximum steady state amplitude should not exceed the 0.55V limit. Overshoots and other transients are permitted to fall into dotted area, bounded by the amplitude levels 0.55V and 0.6V, provided that they not do not exceed the steady state level by more than 0.05V.

Note 2

For all measurements using these mask, the signal should be AC coupled, using a capacitor of not less than 0.01μf, to the input of the oscilloscope used for measurements. The nominal zero level for both mask should be aligned with the oscilloscope trace with no input signal. With the signal than applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05V of the nominal zero level of the mask.

Note 3

Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding and succeeding pulses. For actual verification, if a timing signal associated with the source of the interface signal is available, its use as a timing reference for an oscilloscope is preferred. Otherwise, compliance with the relevant mask may be tested by means of all–0s and all–1s signals,respectively.

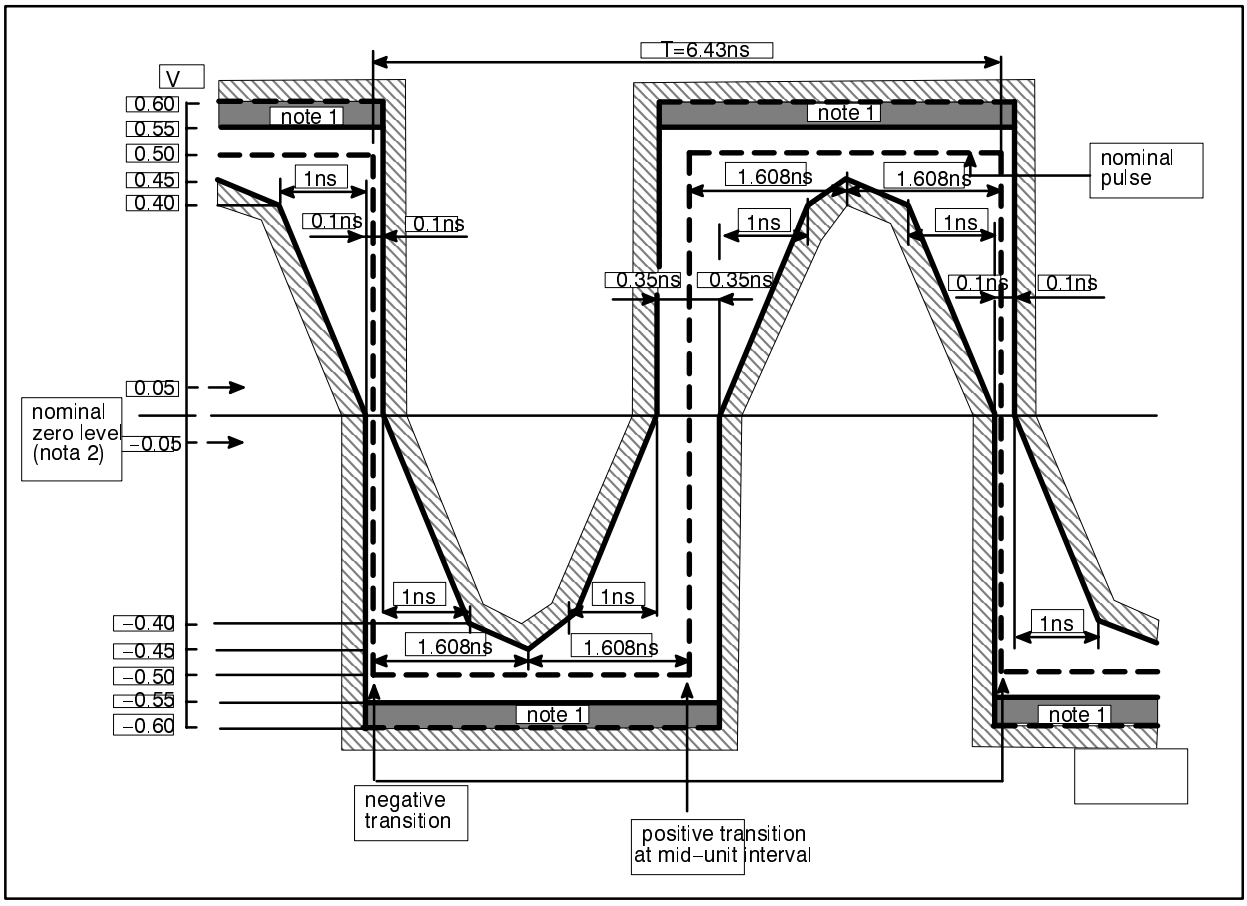
Note 4

For the purpose of these mask, the rise time and decay time should be measured between –0.4V and 0.4V, and should not exceed 2ns.

Note 5

The inverse pulse will have the same characteristics, nothing that the timing tolerance at the zero level of the negative and positive transition are ±0.1ns and ±0.5ns respectively.

Fig. TS–7 *Pulse mask (binary ”1”) at 155520kbit/s Interface*



Note 1

The maximum steady state amplitude should not exceed the 0.55V limit. Overshoots and other transients are permitted to fall into dotted area, bounded by the amplitude levels 0.55V and 0.6V, provided that they not do not exceed the steady state level by more than 0.05V.

Note 2

For all measurements using these mask, the signal should be AC coupled, using a capacitor of not less than 0.01μf, to the input of the oscilloscope used for measurements. The nominal zero level for both mask should be aligned with the oscilloscope trace with no input signal. With the signal than applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05V of the nominal zero level of the mask.

Note 3

Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding and succeeding pulses. For actual verification, if a timing signal associated with the source of the interface signal is available, its use as a timing reference for an oscilloscope is preferred. Otherwise, compliance with the relevant mask may be tested by means of all–0s and all–1s signals,respectively.

Note 4

For the purpose of these mask, the rise time and decay time should be measured between –0.4V and 0.4V, and should not exceed 2ns.

Fig. TS–8 *Pulse mask (binary ”0”) at 155520kbit/s Interface*

2048kHz Synchronization interface

Output port

Bit rate	2048kbit/s
Tolerance	±4.3 ppm
Type of pair	coaxial
Test load impedance	75Ω resistive
Pulse shape	within the mask of Fig. TS–9
Maximum peak voltage	1.5 V
Minimum peak voltage	0.75 V
Maximum jitter at an output port	0.05 UI peak–to–peak measured within the frequency range 20Hz to 100kHz

Tab. TS–7 *2048 Synchronization interface (output port) characteristics*

Input port

The signal presented at the input port should be as defined above but modified by the characteristics of the interconnecting pair.

The attenuation of this pair shall be assumed to follow a $\sqrt{f}$ law and the loss at frequency of 2048kHz should be in the range 0 to 6db (minimum value).

The input port shall be able to tolerate a digital signal with these electrical characteristics but modulated by Jitter. The Jitter value is under study.

The return loss at 2048kHz should be ≥ 15dB.

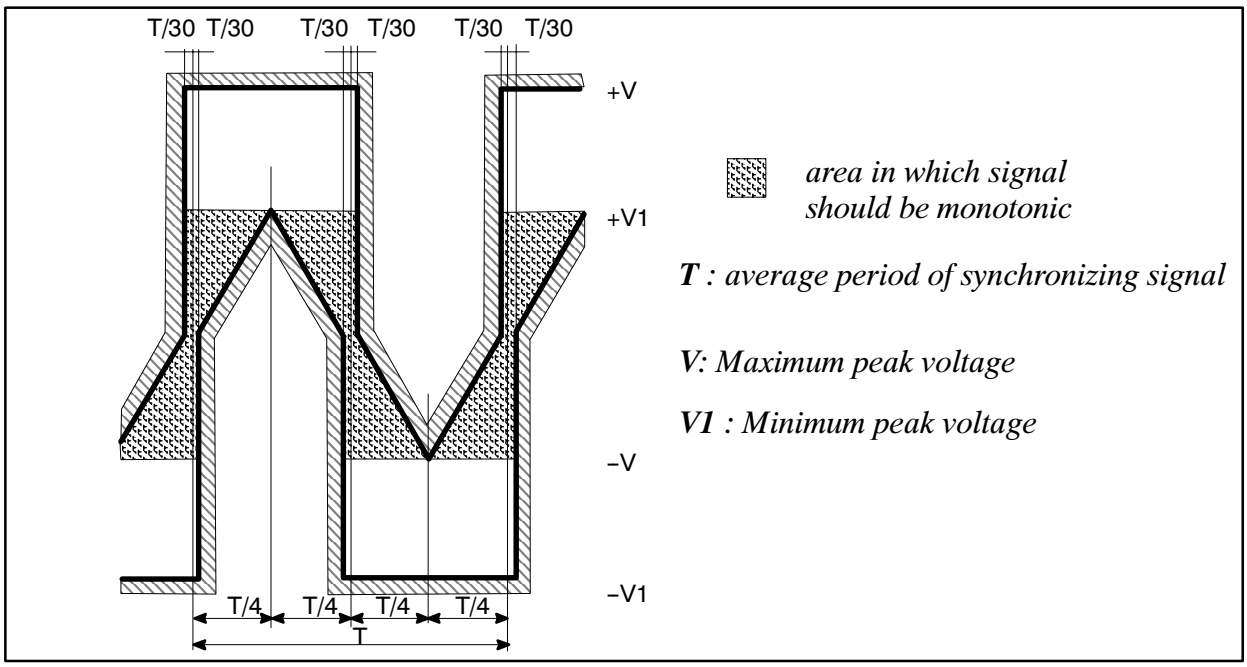


Fig. TS–9 *Pulse Shape of the 2048kHz Synchronization Interface*

Control of Jitter in Hierarchical Digital Interface (ITU–T Recommendation G.823, G.824, G.783)

Input Jitter Tolerance

Parameter value	Peak–to–peak amplitude			Frequency					Pseudo–random test signal
Digit rate kbit/s	A_0 (μs)	A_1 (UI)	A_2 (ui)	f_0 (HZ)	f_1 (HZ)	f_2 (HZ)	f_3 (kHz)	f_4 (kHz)	Pseudo–random test signal
1544	18 NO TAG	5	0.1	1.2×10^{-5}	10	120	6	40	$2^{20} - 1$
2048	18	1.5	0.2	1.2×10^{-5}	20	93	18	100	$2^{15} - 1$
34368	18	1.5	0.15	*	100	1000	10	800	$2^{23} - 1$
44736	18	5	0.1	1.2×10^{-5}	10	600	30	400	$2^{20} - 1$
139264	*	1.5	0.075	*	200	500	10	3500	$2^{23} - 1$
155520	*	1.5	0.15	*	*	6500	65	*	$2^{23} - 1$

NOTE (*) value under ITU–T study

NOTE (1) The value for A_0 (18μs) represents a relative phase deviation between the incoming signal and the internal local signal derived from the reference clock

Tab. TS–8 *Parameter values for input jitter tolerance*

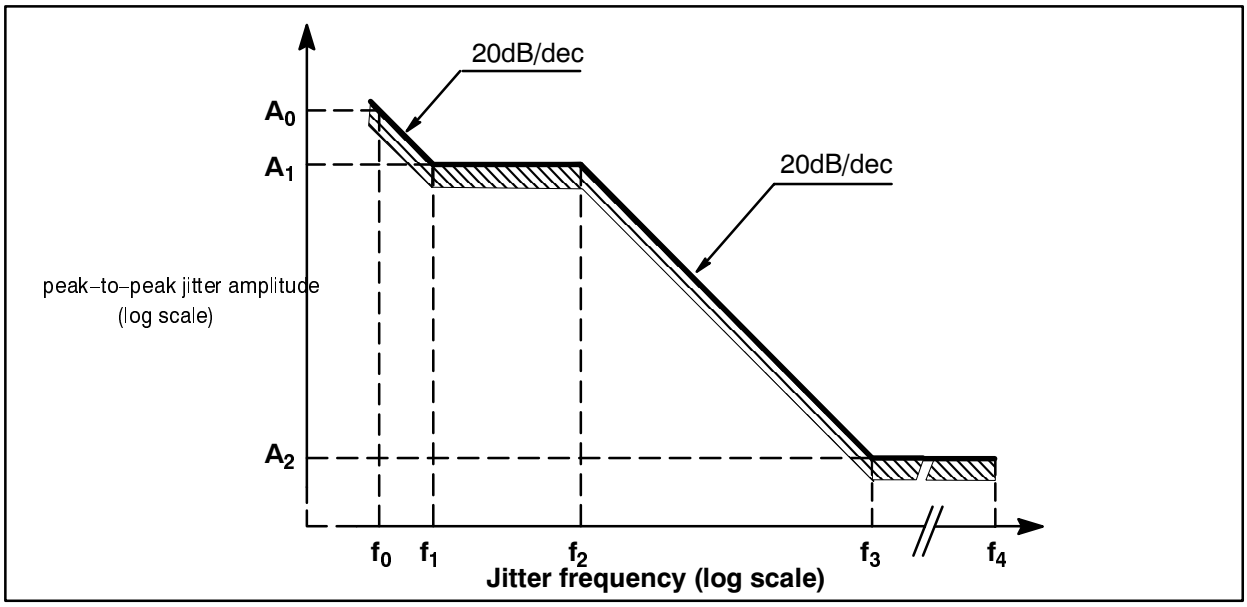


Fig. TS–10 *Lower limit of maximum tolerable input jitter*

Jitter transfer function

2048kbit/s Hierarchy

Parameter value / Digit rate kbit/s	Jitter gain		Frequency			
	x (dB)	–y (dB)	f_0(1) (HZ)	f_5 (HZ)	f_6 (kHZ)	f_7 (kHz)
2048	0.5	–19.5	–	40	0.4	100
34368	0.5	–19.5	–	300	3	800
139264	0.5	–19.5	–	900	90	3500
155520	*	*	–	*	*	*

* = *values under ITU–T study.*

NOTE (1) ***The value for f_0 should be lower than 20Hz and as low as possible but inside the measurement equipment limits***

Tab. TS–9 *Parameter Value for Jitter transfer function (2048kbit/s hierarchy)*

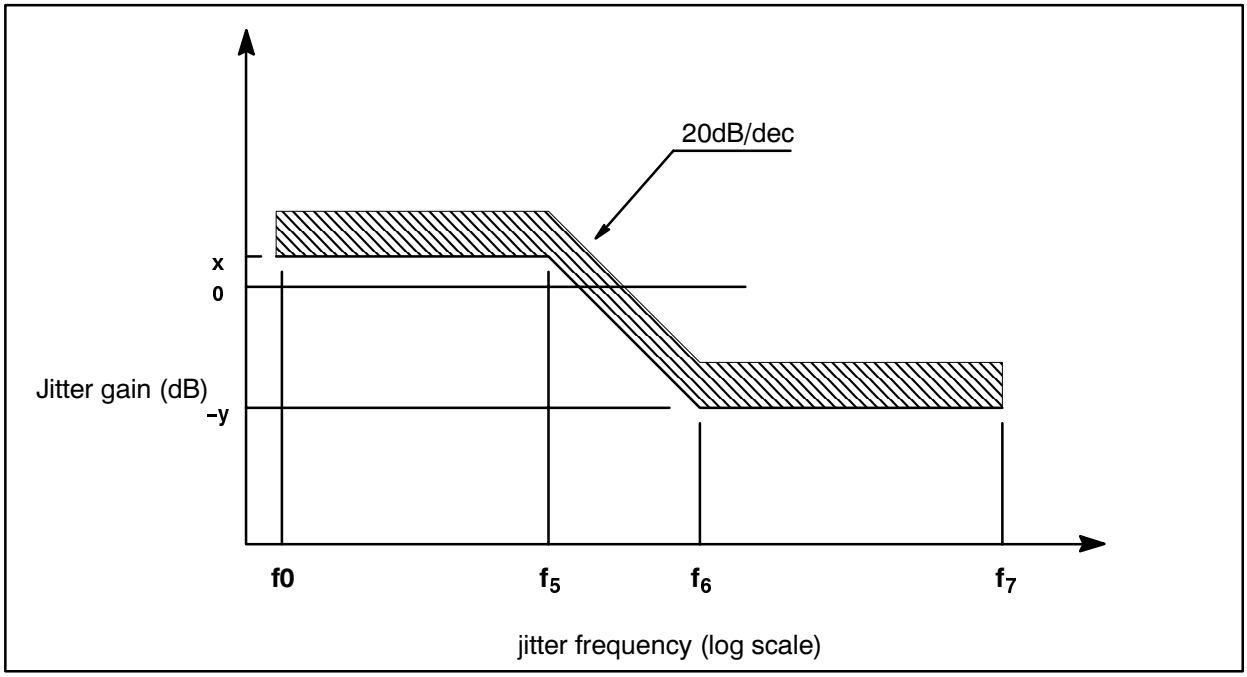


Fig. TS–11 *Upper limits for Jitter transfer function (2048kbit/s hierarchy)*

1544kbit/s Hierarchy

Parameter value / Digit rate kbit/s	Jitter Gain		Frequency			
	x (dB)	–y (dB)	f_0 (HZ)	f_5 (HZ)	f_6 (kHZ)	f_7 (kHz)
1544	0.5	*	–	35	0.25	15
44736	0.1	*	–	1000	15	*

NOTE (*) ***values under ITU–T study***

NOTE (1) ***The value for f_0 should be lower than 20Hz and as low as possible but inside the measurement equipment limits***

Tab. TS–10 *Parameter value for Jitter transfer function (1544kbit/s Hierarchy)*

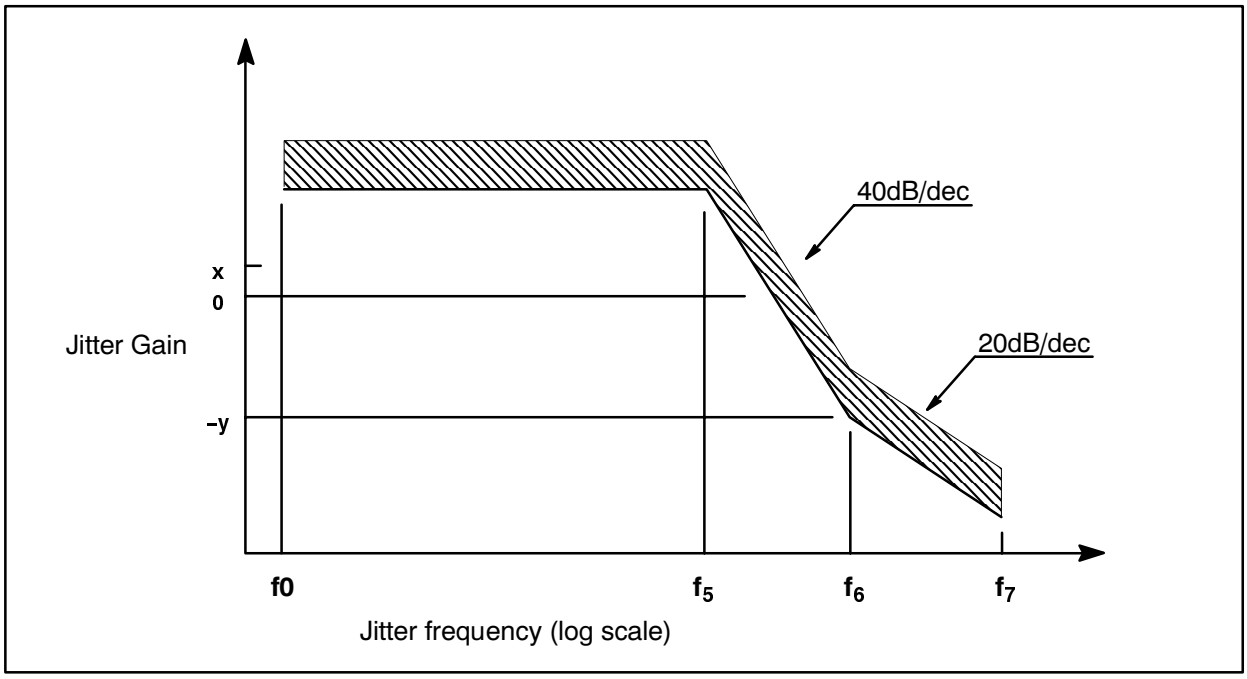


Fig. TS–12 *Upper limit for the Jitter transfer function (1544kbit/s Hierarchy)*

IMPORTANT *The values of Tab. TS–9 and Tab. TS–10 are referred to the plesiochronous signal multiplexing therefore they have to be considered as minimum requirement. More stringent requirements for Jitter transfer function which includes attenuation of the jitter arising from decoded pointer adjustments are under ITU–T study.*

Maximum Output Jitter

In the synchronous multiplexer the jitter tolerance on output signals are the same as jitter tolerance in plesiochronous multiplexer (see Tab. TS–11 and Fig. TS–13).

Has also to be taken into account the jitter generated by synchronous multiplexer due to the mapping of plesiochronous tributaries into synchronous containers and to the pointer adjustments.

The global effect of these two jitters is defined as ”combined” jitter and it must be included in the tolerance value as shown in Tab. TS–12, in the hypothesis of absence of input jitter.

Maximum jitter on output signal

Parameter value / Digit rate kbit/s	Network limits		Measurement filter bandwidth (lower cut–off frequency f_1 or f_3 and upper cut–off frequency f_4)		
	B_1 (UI pp)	B_2 (UI pp)	f_1 (HZ)	f_3 (kHZ)	f_4 (kHz)
1544	5.0	0.1	10	8	100
2048	1.5	0.2	20	18 (700Hz)	100
34368	1.5	0.15	100	10	800
44736	5.0	0.1	10	30	400
139264	1.5	0.075	200	10	3500
155520	1.5	0.15	500	65	1300

Tab. TS–11 *Maximum Jitter on output signal*

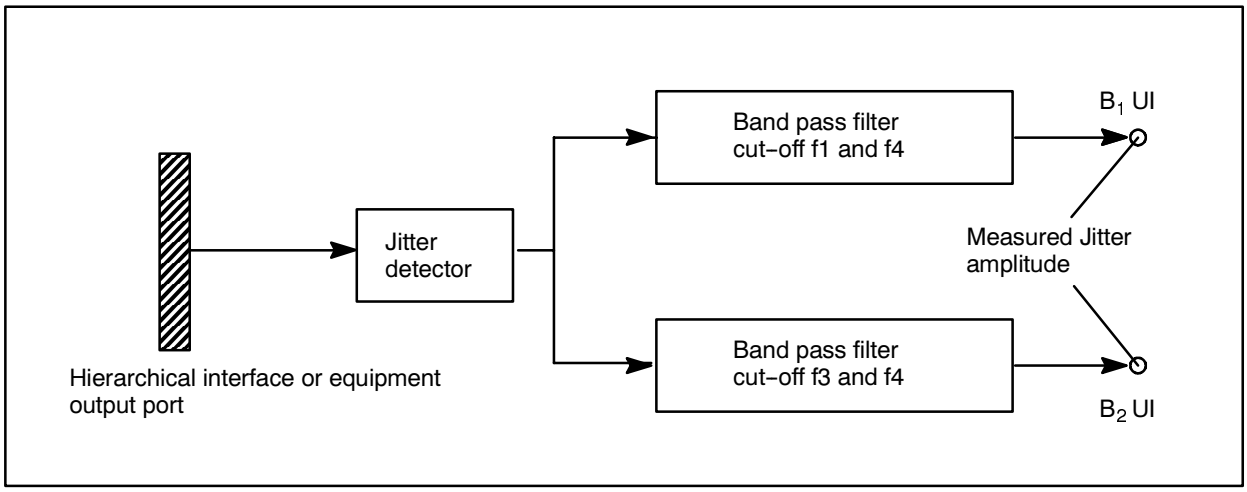


Fig. TS–13 *Measurement arrangements for output jitter from a hierarchical interface or an equipment output port*

"Combined" Jitter generated by the equipment

Parameter value / Digit rate kbit/s	Maximum pk–pk jitter (mapping)		Maximum pk–pk jitter ("combined")		Measurement filter bandwidth (lower cut–off frequency f_1 or f_3 and upper cut–off frequency f_4)		
	B_1 (UI pp)	B_2 (UI pp)	B_1 (UI pp)	B_2 (UI pp)	f_1 (HZ)	f_3 (kHZ)	f_4 (kHz)
1544	note (1)	note (1)	1.5	note (1)	10	note (1)	40
2048	note (1)	0.075	0.4	0.075	20	18 (700Hz)	100
34368	note (1)	0.075 note (3)	0.4 00.75 note (2)	0.075 note (3)	100	10	800
44736	note (1)	note (1)	1.5	note (1)	note (1)	note (1)	400
139264	note (1)	note (4)	note (5)	note (4)	200	10	3500

NOTE (1) ***Values under ITU–T study.***

NOTE (2) ***The 0.4 UI limit corresponds to a single pointer adjustments of one polarity followed by another single pointer adjustment of the opposite polarity, and the 0.75 UI limit corresponds to a double pointer adjustment of one polarity followed by another double pointer adjustments of the opposite polarity. It is assumed that pointer adjustments of opposite polarities are well spread in time.***

NOTE (3) ***This limits corresponds to a double pointer adjustments of one polarity followed by another double pointer pointer adjustments of the opposite polarity. It is assumed that pointer adjustments of opposite polarities are well spread in time.***

NOTE (4) ***A value of 0.075 UI has been proposed (Note 3 applies)***

NOTE (5) ***Values of 0.4 UI and 0.75 UI has been proposed (Note 2 applies)***

Tab. TS–12 *"Combined" Jitter generated by the equipment*

——————— *The measurements arrangements for "combined" Jitter are the same as used for maximum output Jitter (see Fig. TS–13)*

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