Appendix AV
V Interface Signals

The paragraphs that follow describe series 100 signals used in the V.11, V.28, V.35, V.36 interfaces.

The table below lists interface signals (CCITT Circuits) and their functions.

CCITT CIRCUIT	DESCRIPTION
102	Electric ground
103	Transmit data
104	Receive data
105	Transmit request
106	Clear to send
107	DCE ready
108	DTE ready
109	Data received indicator
114	Transmit bit timing (from DCE)
115	Receive bit timing
140	Remote Loop2b request
141	Loop3c request
142	Test indication

Circuit 107

When this circuit is in active state (ON), the channel is perfectly operational, and can therefore dialog with the User.

The circuit goes to ON state when:

- *there are no stable alarms present;*
- *circuit 108 is in active state ON.*

Circuit 107 must be in active state ON and circuit 108 must be in active state NO in order to accept all signals received from other interface circuits as valid, excluding circuit 141.

Circuit 107 goes to idle state OFF when circuit 108 goes to OFF state. As a result, the state D=1 S=OFF is sent on the line and circuit 107 goes from ON state to OFF state within 8 envelopes.

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Circuit 107 must be in OFF state, even if circuit 108 is in ON state, in the following conditions:

- *loop2b from remote or CDN;*
- *Network Out–of–service condition (D=0 S=OFF) received by network interface for longer than 3s +/–0.5 s;*
- *FAT–X.50 alarm present for more than 3s +/– 0.5 s;*
- *selftest;*
- *during automatic acquisition of the bit rate used by the interface.*

Circuit 108

When this circuit is in active state ON, the device used by the Subscriber is perfectly operational, and can therefore dialog with the interface.

Circuit 105

The state of this circuit is associated to the condition of the status bit (ST) transmitted on the line.
When the circuit is in ON state, the status bit (ST) transmitted over the line goes to logic ”1”.
When the circuit is in OFF state, the status bit (ST) transmitted over the line goes to logic ”0”.

Circuit 106

This circuit is used to respond to the state of circuit 105. This state is deemed valid if it is stable for 1s +/–0.25ms.
When circuit 105 goes from OFF to ON state, circuit 106 goes from OFF to ON state in a period of less than 10 envelopes. During the transition, the character D=1 S=ON is sent on line.
When circuit 105 goes from ON to OFF state, circuit 106 goes from ON to OFF state in a period of less than 8 envelopes.

Circuit 109

The state of this circuit is associated to the logic level of the receive status bit (SR). A variation in level of bit SR is transferred to circuit 109 only if the variation is confirmed as illustrated in the following table:

SR (t–1)	SR (t)	109 (t)
0	0	OFF
0	1	109 (t–1)
1	1	ON
1	0	109 (t–1)

The transition from ON to OFF, in addition to the above mentioned criteria, is also determined by the presence of the FAT–X.50 alarm.
When circuit 109 is in OFF condition, circuit 104 is forced to logic ”1”.

Circuit 141

When this circuit is put in ON state for at least 8 +/–2ms, the port is set to loop 3c and circuit 142 is set to ON state.

Circuit 140

When this circuit is set to ON state for at least 8 +/–2ms, the loop 2b activation signal is sent to the remote DCE.

Circuit 142

When this circuit is in ON state, it indicates that the port is in loop conditions.

Circuit 103

The data transmitted from the port is received by this circuit.

Circuit 104

The data transmitted by subscribers or by the network is delivered to this circuit.

Circuit 114

The clock signal required for correct timing of data transmitted to circuit 103 is sent to this circuit.

Circuit 115

The clock signal required for correct timing of data received from circuit 104 is sent to this circuit.

Correspondence of V.11 signals with CCITT circuits

The table below indicates the relationship between V.11 Interface signals and CCITT circuits:

CCITT CIRCUIT	V.11 INTERFACE
103	T
104	R
105	C
109	I
115	S

Circuit used by the V.11, V.28, V.35, V.36 interfaces

Nella seguente tabella sono indicati i circuiti utilizzati dalle varie interfacce.

The table below indicates the circuits used by the various interfaces.

CIRCUIT	V.11	V.28	V.35	V.36
102	NO	YES	YES	YES
103	YES	YES	YES	YES
104	YES	YES	YES	YES
105	YES	YES	YES	YES
106	NO	YES	YES	YES
107	NO	YES	YES	YES
108	NO	YES	NO	NO
109	YES	YES	YES	YES
114	NO	YES	YES	YES
115	YES	YES	YES	YES
140	NO	YES	YES	YES
141	NO	YES	YES	YES
142	NO	YES	YES	YES

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