Appendix PF
Performance Monitoring

General

Performance monitoring refers to the monitoring of transmission quality (error performance) on SDH trails i.e. regenerator sections, multiplex sections and paths, PDH paths according to the user defined schedules and thresholds.

Performance Management (PM) refers to capability of controlling the PM process by means of the generations of performance data, reporting of the performance data and the reporting of threshold crossing.

The definitions of PM related events and parameters are based upon the error performance measurement of blocks.

Definition and Measurement of the Block

Regenerator section

For Regenerator Section the used error detection code is BIP–8, therefore the number of blocks per second is 8000 for each STM–N.

STM–N	bits/block	blocks/s	Error detection code
STM–1	19 440	8000	BIP–8
STM–4	77 760	8000	BIP–8
STM–16	311 040	8000	BIP–8

Tab. PF–1 *Performance in the Regenerator section*

Multiplex section

Each BIP–1x24xN of MS in the STM–N (N≥1), pertains to 24xN different blocks. For the generic Multiplex Section in the STM–N, 24xN blocks are present (1).

STM–N	bits/block	blocks/s	Error detection code
STM–1	801	8000x1x24	BIP–1
STM–4	801	8000x4x24	BIP–1
STM–16	801	8000x16x24	BIP–1

Tab. PF–2 *Performance in the Multiplex section*

NOTE (1) ***A previous definition was based on NxBIP–24 error detection codes and Nx8000 blocks/s, therefore the number of bits/block was 19224 instead of 801.***

SDH path

The definitions of block size for SDH digital paths are as follow:

VC–N	bits/block	blocks/s	Error detection code
VC–4	18 792	8000	BIP–8
VC–4–4C	75 168	8000	BIP–8
VC–3	6120	8000	BIP–8
VC–2	3424	2000	BIP–2
VC–2–mc	3424	mx2000	mxBIP–2
VC–12	1120	2000	BIP–2
VC–11	832	2000	BIP–2

Tab. PF–3 *Block size for the SDH digital path*

PDH path

The definitions of block size for PDH digital paths are as follow:

Bit rate	Block size
1544kbit/s	4632 bits
2048kbit/s	2048 bits
6312kbit/s	3156 bits
44736kbit/s	4760 bits

Tab. PF–4 *Block size for the PDH digital path*

SDH Performance Parameters

The SDH multiplexing structure as defined in the ITU–T rec. G.707, provides a number of overhead Bytes to be used for in–service monitoring of System and Path Performance.

The monitored entities are :

- **RS** *(Regenerator Section)*
  A Regenerator Section is the part of the line system between two Regenerator Section Termination (RST).
  One byte (B1) in the RSOH is allocated for regenerator section error monitoring.
- **MS Near end** *(Multiplex Section, Near end)*
  A Multiplex Section is the part of line system between two Multiplex Section Termination (MST).
  Three bytes (B2) in the MSOH are allocated for multiplex section error monitoring function.
- **MS Far end** (*Multiplex Section, Far end)*
  One byte (M1) in the SOH is allocated to convey back the status of the remote MST.
- **VC–4/VC–3 Near end** *(Virtual Container at 140 or 45/34Mbit/s, Near End*)
  VC–4/VC–3 is the higher order (HO) container into the STM–1 frame.
  One byte (B3) is allocated in each VC–3 or VC–4 POH for a path error monitoring function.
- **VC–4/VC–3 Far end** *(Virtual Container at 140 or 45/34Mbit/s, Far End)*
  One byte (G1) is allocated in each VC–3/VC–4 POH to convey back to the VC–3/VC–4 path generator the path terminating status and performance.
- **VC–1/VC–2 Near end** (V*irtual Container at 1.5, 2 or 6Mbit/s, Near End)*
  VC–1/VC–2 is the lower order (LO) container into the STM–1 frame.
  The first two bits of the lower order POH byte (V5) are allocated for a path error monitoring function.
- **VC–1/VC–2 Far end** *(Virtual Container at 1.5, 2 or 6Mbit/s, Far End)*
  The bit 3 of the lower order POH byte (V5) is allocated to convey back to the VC–1/VC–2 path generator the path terminating performance.
- **AU Rx** *(Administrative Unit)*
- **TU** *(Tributary Unit selected)*

Monitored entity	Events
RS Near End	ES,BBE,UAS,SES,OFS,CSES
MS Near End	ES,BBE,UAS,SES,PSC,PSD,CSES
MS Far End	ES, BBE, UAS, SES, CSES
VC3 / VC4 Far End	ES,BBE,SES,CSES
VC3 / VC4 Near End	ES,BBE,UAS,SES,CSES
VC12 Far End	ES,BBE,SES,CSES
VC12 Near End	ES,BBE,UAS,SES,CSES
AU4 Rx	AU PJE
Selected TU	ES,BBE,UAS,SES,CSES

Tab. PF-5 *The computable events for the different monitored entities*

PDH Performance Parameters

According to ITU G.826 on the PDH streams, the monitored entities are:

- ***PDH Near End*** *(2Mbit/s, 34Mbit/s, 45Mbit/s, 140Mbit/s and VideoCodec PDH signals)*
- ***PDH Far End*** *(2Mbit/s, 34Mbit/s, 45Mbit/s, 140Mbit/s and VideoCodec PDH signals)*

Monitored entity	Events
PDH Near End	ES, BBE, SES, UAS, CSES
PDH Far End	ES, BBE, SES, CSES

Tab. PF-6 *The computable events for the different monitored entities*

Event Description

According to G.826 Recommendation, the monitored events are:

- **Errored Block** *(*EB)*: a block in which one or more bits are in error.*
- **Errored Second** *(*ES)*: a one second period with one or more errored blocks.*
- **Severely Errored Second** *(*SES)*: a one second period which contains more than 30% errored blocks*
- ***BBE** Background Block Error: an errored block not occurring as part of a SES.*

To have a SES in a SDH path, the number of BIP violations must exceed a fixed threshold, which is defined for each VC path in ITU–T Recc. G.826.

In a SDH path, in addition to the events listed before, there are also the following monitored events:

- **Administrative Unit Pointer Justification Event** *(*AU PJE*): indication of an occurred pointer justification on AU3/AU4*
- **Out of Frame Second** *(OFS): loss of alignment of SDH frame*
- ***UAS** Unavailable Second: indication of an excessive number of errors so that statistics become unavailable. It is caused by a sequence of consecutive SES (SUE – Start of Unavailability Event) and finish with a sequence of consecutive free error seconds (TUE – Termination of Unavailability Event).*
- **Protection Switching Count** *(PSC): counter of protection switches in the measurement period*
- **Protection Switching Duration** *(PSD): indication of the duration of occurred protection switches*
- **Consecutive SES** *(CSES): counts configurable in the range of 2 to 9 SES*

the causes of a UAS in an SDH psth are:

- *Higher order path AIS*
- *Lower order path AIS*
- *Loss of TU pointer*
- *Loss of AU pointer*
- *Higher order path RDI*
- *Lower order path RDI*

Performance Data Recording

Performance parameters are accumulated in designated registers. There are two types of registers:

- ***24–hour register**:*
  it accumulates performance events over fixed 24 hour periods
- ***15–minute register**:*
  it accumulates performance events over fixed 15 minute periods

There are two 24–hour registers, the *current* and the *recent*. The current 24–hour register is reset to zero at the end of each 24–hour period, after the data have been printed and transferred to the recent 24–hour register.

The 15–minute registers form a stack of at least 16 registers.
At the end of a 15–minute period, the content of the current register is transferred to the first of the recent registers. When all the 15–minute registers are full, the content of the earliest register is deleted.

When the current 15–minute register is empty, no data is transferred into the first recent 15–minute register.