Appendix MN

Synchronous Digital Multiplexing Operation Principle

Signal of the Synchronous Digital Hierarchy

Signal processing in the equipments of the Synchronous Digital Hierarchy is in accordance with CCITT Recommendations G.707 to G.709, G.781 to G.784 and G.957 and G.958.

The SDH is a hierarchically organized set of digital transport structures which have been standardized for the transmission of payloads in transmission networks.

Electrical and Optical Signals

Multiplexing and processing of signals in the devices is performed electrically. All interfaces in the devices are therefore electrical.

External interfaces for STM–1 signals (TRIB) have been provided for electrical signals. They are CMI–coded in accordance with CCITT G.703.

The interface signals (STM–4 on MSH31 or STM–16 on MSH50–MSH53) on the LINE side are optical.

Signal Frame Structure

Fig. MN–1 shows the framework structure of an STM–1 signal. This shows that a frame consists of 9 rows each containing 270bytes. Each byte consists of 8bits.

The frame frequency (8kHz) has been chosen so that 1byte of the frame corresponds to the transmission capacity of a 64kbit/s channel.

The first 9bytes of each row of a frame (with the exception of row 4) contain a section overhead. The first 9 bytes of row 4 contain the AU pointer (payload address).

The field shown in Fig. MN–1 consisting of 261 x 9bytes for payload transmission (STM payload) is known as the virtual container (VC) and consists of the actual payload, known as the container (C), and a preceding additional overhead, known as the path overhead (POH), for path–related information.

The virtual container is not located rigidly in the frame but can move around freely in the payload section. The pointer indicates the position of the first byte of the VC (this is always the first byte of the POH). This allows a VC received in the

multiplexer to be matched to a prespecified frame phase of the STM–1 signal. Since CCITT envisages increments of 3bytes for the start address of the VC in the pointer, but the phase of the signals arriving at the multiplexer can vary at will, an additional phase alignment procedure must be performed with a 3byte justification process.

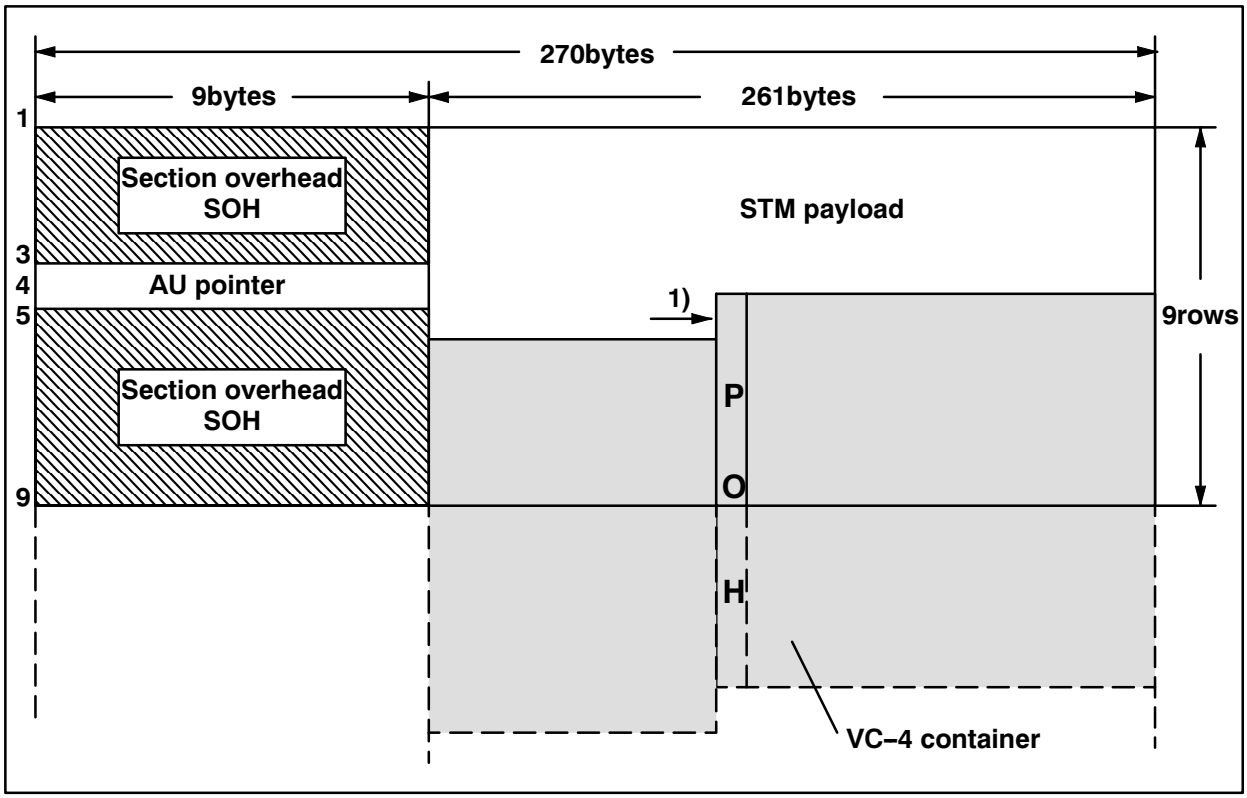


Fig. MN–1 *Frame Structure of an STM–1 Signal*

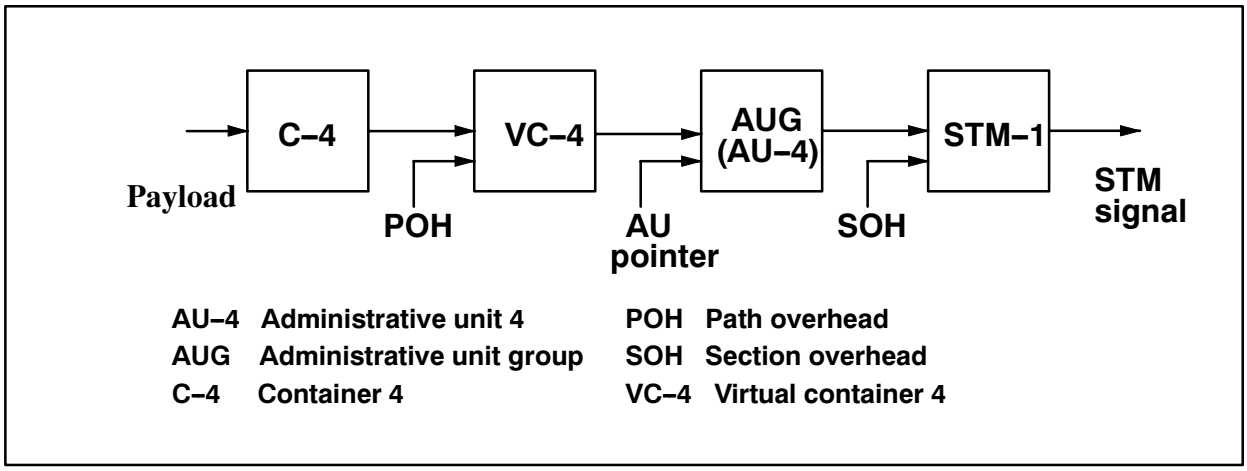


Fig. MN–2 *Explanation of Terms*

Multiplexing

Multiplex signal STM–N is composed of N AUG signals of the type used in STM–1 (AU–4) and a block of 8 x N x 9 SOH bytes (Fig. MN–3). It is formed by bytewise interleaving of the N AUG signals. This produces a signal of N–times the bit rate (N = 4 on STM–4, N = 16 on STM–16) with unchanged frame period (125 µs). In this multiplex signal, the first byte belongs to the first STM–1 signal, the second byte to the second signal etc. With STM–4, the fifth byte then belongs once again to the first STM–1 signal, the sixth byte to the second signal and so on. With STM–16, the seventeenth byte then belongs again to the first STM–1 signal, the eighteenth byte to the second signal and so on.

IMPORTANT *When multiplexing N STM–1 signals, only the VC–4 component of the STM–1 signal is adopted unchanged in the STM–N signal. The SOH bytes of the STM–N signal are restructured as per Fig. MN–5 and the pointers set to the required new value*

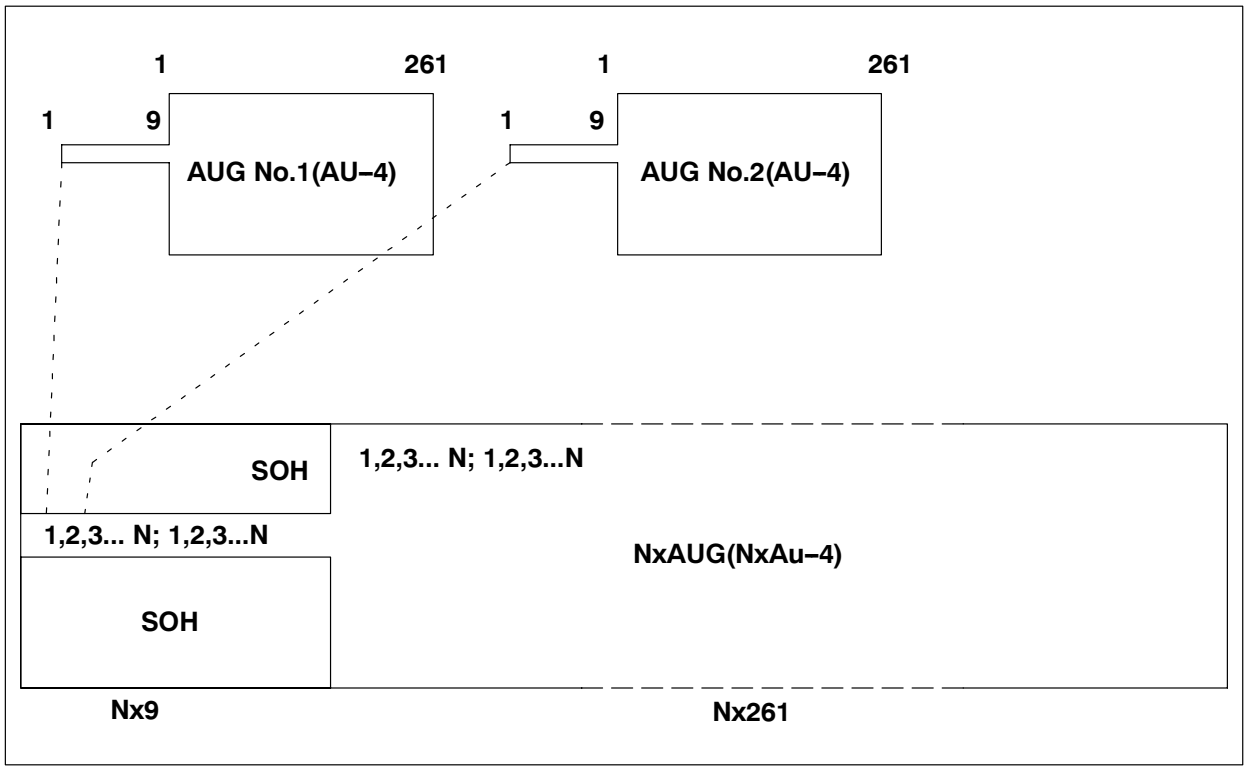


Fig. MN–3 *Multiplexing of N Administrative Unit Group (AUG) to form an STM–N Signal*

Section Overhead (SOH)

Fig. MN–4 shows the structure of the section overhead component of an STM–1 signal.

The overhead bytes are used for additional information, for frame alignment, and for monitoring, maintenance and control functions.

The overhead bytes in the first three rows of a frame can be accessed in all regenerators and line multiplexers (regenerator section overhead RSOH) and the

overhead bytes in rows 5 to 9 in the line multiplexers only (multiplex section overhead MSOH). The bytes of frame row 4 essentially contain the pointer data and three free bytes for phase alignment (justification).

Unlike ail other frame components, the overhead section of frame row 1 is not scrambled before transmission since it contains, among other things, the frame alignment signal (comprising A1 and A2 bytes). The C1 byte following the A bytes is of no significance for STM–1 signals. It is used with STM–4 and STM–16 to identify the STM–1 signals in the STM–N signal. Byte B1 is used for error monitoring of the entire STM–N signal during operation using a parity check (for the relevant regenerator section). Byte E1 is employed as an orderwire. Byte F1 is available to the operator as a data channel.

Bytes D1 to D3 together form a 192kbit/s transmission channel (DCC_R) for the network management.

The multiplex section overhead contains the B2 bytes for monitoring a multiplex section by means of a parity check (separately for each STM–1 contained in the STM–N signal), the K bytes for controlling and checking line protection switching and bytes D4 to D12 which together form a 576kbit/s transmission channel (DCC_M) for the network management.

The Z bytes are reserved for functions not yet defined by CCITT.

Byte E2 is defined for the orderwire between line multiplexers.

The shaded bytes are reserved for national purposes.

The non–designated bytes are available for auxiliary channels. However, CCITT reserves the right to standardize their usage at a later date.

As already mentioned with the multiplexing principle (Fig. MN–3), the overhead for higher hierarchy levels (STM–N) consists of N * 9bytes per row.

By way of illustration, Fig. MN–5 shows the arrangement of overhead bytes for an STM–4 signal.

For STM–16 the overhead section is a further four times larger, i.e. 4 x 4 * 3 A1 bytes etc.

As stated earlier, the overhead is restructured during multiplexing. Since the B1 , D, E, F and K bytes are used only once per STM–N signal, the structure of the overhead for the higher hierarchy levels does not correspond to the N–times interleaved structure of the STM–1 overhead.

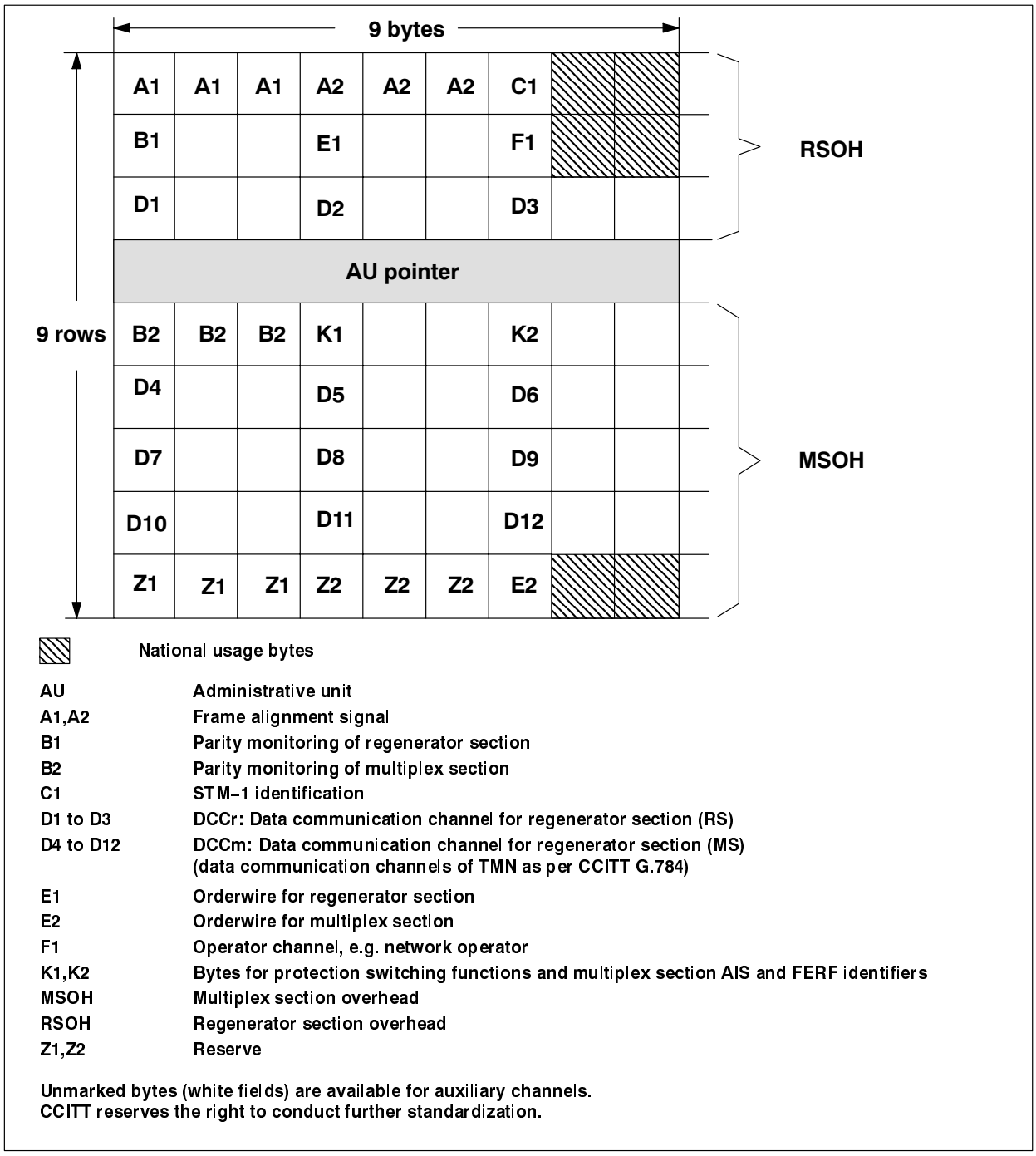


Fig. MN–4 *Use of the Overhead Bytes in the STM–1 Frame as per CCITT Recommendation G.708*

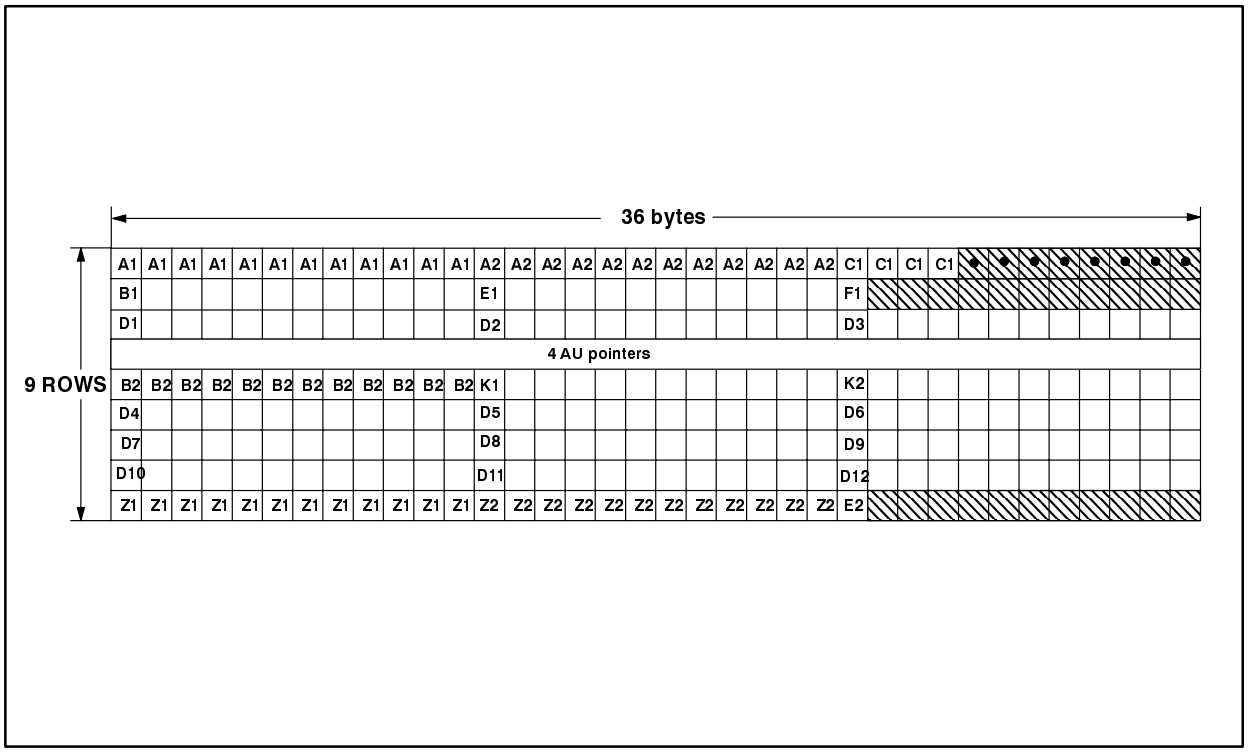


Fig. MN–5 *Arrangement of the Overhead Bytes in an STM–4 Signal*

Pointer

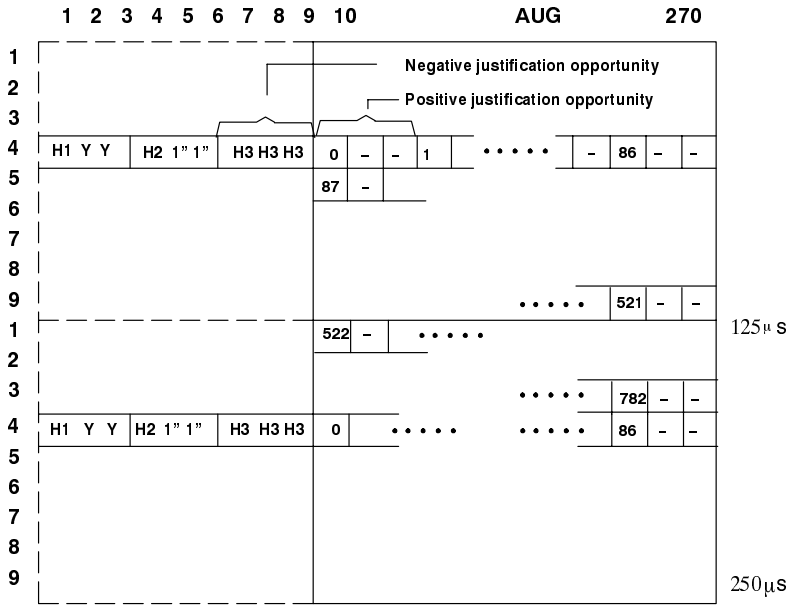
Preliminary note: CCITT provides various pointers for different signal types and combinations. The AU–4 pointer which is of significance for MSH31 and MSH50–MSH53 is discussed below.

The AU–4 pointer allows flexible and dynamic arrangement of the virtual container (VC–4) within the STM–N frame, i.e. a phase fluctuation between the STM–N frame and VC is permissible.

Fig. MN–6 shows the byte structure of the pointer. The H3 bytes allow the payload to be transmitted with negative justification. H1 and H2 contain the pointer information as shown in Fig. MN–7.

The first four bits of byte H1 (new data flag) are used to indicate an arbitrary phase reversal between overhead and VC. Such a reversal can occur, for example, when a new payload starts (new connection).

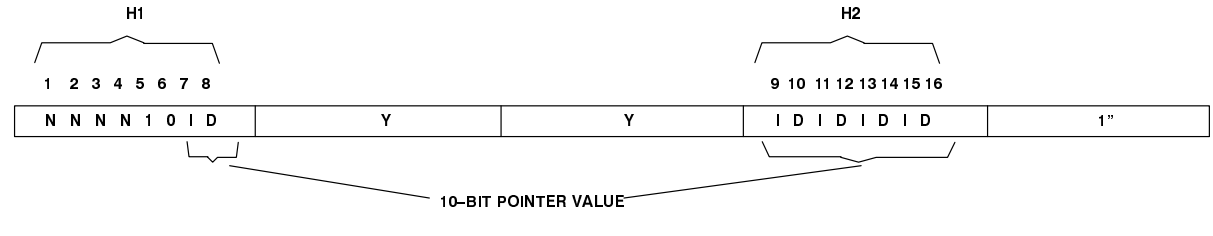
Together with H2, the last 2bits of H1 form a 10–bit word for the address of the VC start in the payload section. This address is a binary number with a value from 0 to 782 (decimal). It shows the phase shift between pointer and first VC byte in increments of three bytes.



As clarification:
A VC–4 container contains 9x261 bytes (Fig. MN–1) this corresponding to 3x783 bytes (Fig. MN–6). During justification, 3 further bytes (H3) are available (negative justification) or 3 bytes are not used (positive justification).

1" Byte with "1" in all bit positions
Y 10011011

Fig. MN–6 *Bytes Structure of the AU–4 Pointer*



I Inverted in order to initiate positive justification
D Inverted in order to initiate negative justification
N Marking bit for new payload

Marking for new payload:
–Switched on 1001
–Switched off 0110

Pointer value (bits 7 to 16)
–Normal range AU–4: 0 to 782 decimal

Fig. MN–7 *Bytes of the Pointer*

Justification Method

If a frequency difference occurs between the STM frame and VC, the value of the pointer, i.e. of the address, is incremented or decremented as required and is accompanied by positive or negative justification.

If the frequency of the VC is too low with respect to the STM frame, the VC start in the frame must slip back periodically in time, the positive justification opportunity contains no information and the pointer value must be incremented each time by 1 . This operation is indicated by inversion of the I bits in the pointer word. The following pointers contain the new value.

If the VC frequency is too high, the negative justification opportunity must be employed and the pointer value decremented by 1. This is indicated by inversion of the D bits in the pointer word.

Payload – Path Overhead

As already mentioned (Fig. MN–2), the payload is accommodated in the virtual container. From the various VC types envisaged by CCITT the virtual container VC–4 is used only. It consists of the VC–4 path overhead which contains path–specific information (address, error monitoring etc. of a payload link) and container C4 (Fig. MN–8)

The VC–4 path overhead is each accommodated in the first bytes of all 9 rows of the VC–4 (Fig. MN–9). These 9 bytes have the following tasks:

J 1	Path trace
B3	Parity byte for error rate monitoring of the VC–4 path
C2	Indication: Path equipped/not equipped/unused
G 1	Path status reports to the transmitter
F2	Operator communication
H4	Indication of several continuous frames (for special payloads)
Z3 to Z5	Bytes reserved for future applications.

Container C–4 contains the payload to be transmitted. This can be a plesiochronous source signal (e.g. 140Mbit/s) or a signal of the Synchronous Digital Hierarchy.

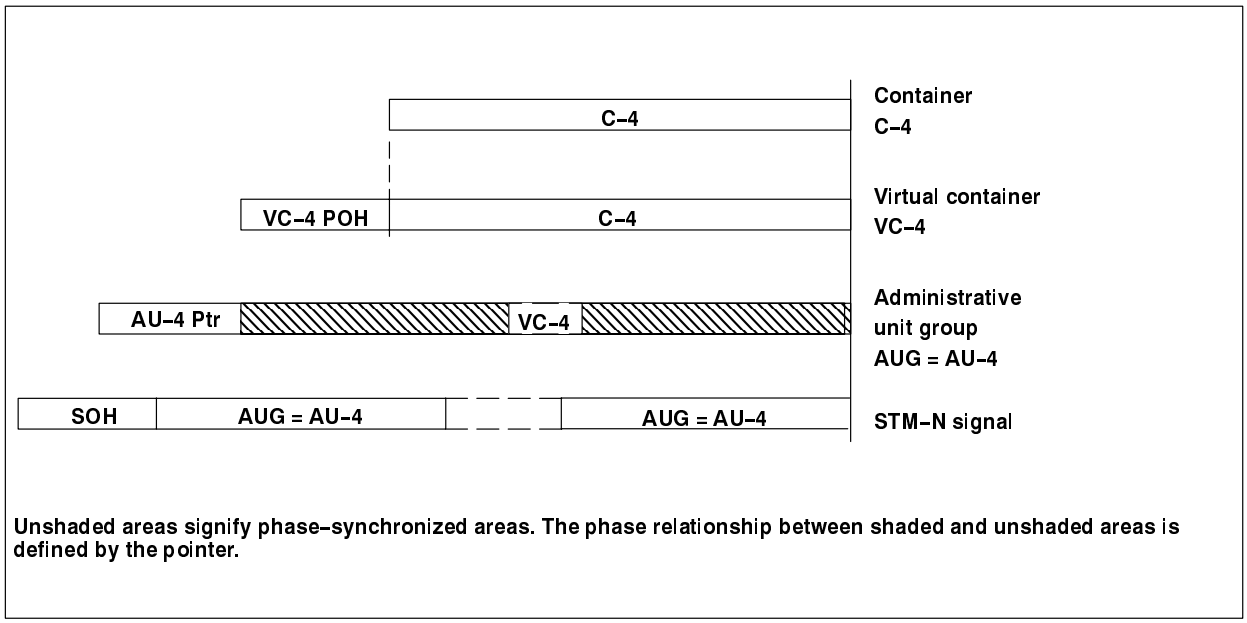


Fig. MN–8 *Structure and Composition of an STM–N Signal*

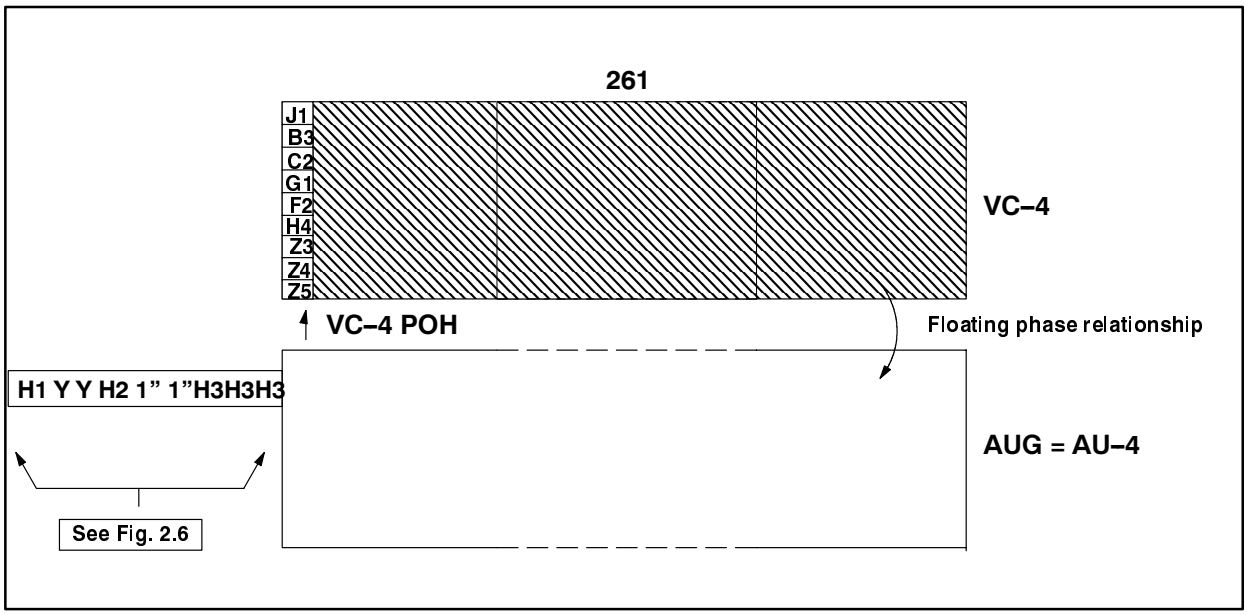


Fig. MN–9 *Payload and Path Overhead in Virtual Container VC–4 combined with the AU–4 Pointer to the AUG*

Plesiochronous Signals

The Synchronous Digital Hierarchy also allows transmission of plesiochronous signals. For this purpose, a further justification process is required for inserting plesiochronous signals into the container (C) (mapping).

Mapping

A plesiochronous 139.264Kbit/s signal can be accommodated into a C–4 container.

Fig. MN–10 shows the arrangement: each of the 9 rows of the C–4 container is subdivided into 20 blocks of 13bytes each. 12bytes of these are used for transmission of the 140Mbits/s signal (information bits). A 13th byte is employed in various ways as shown in Fig. MN–11 (bytes W, X, Y and Z).

Overhead bits O are reserved for future overhead communication purposes.

Justification

The five justification control bits C in each row provide information on the associated justification opportunity bit S: CCCCC = 00000 indicates that the S bit is an information bit, while CCCCC = 11111 indicates that the S bit is a justification bit.

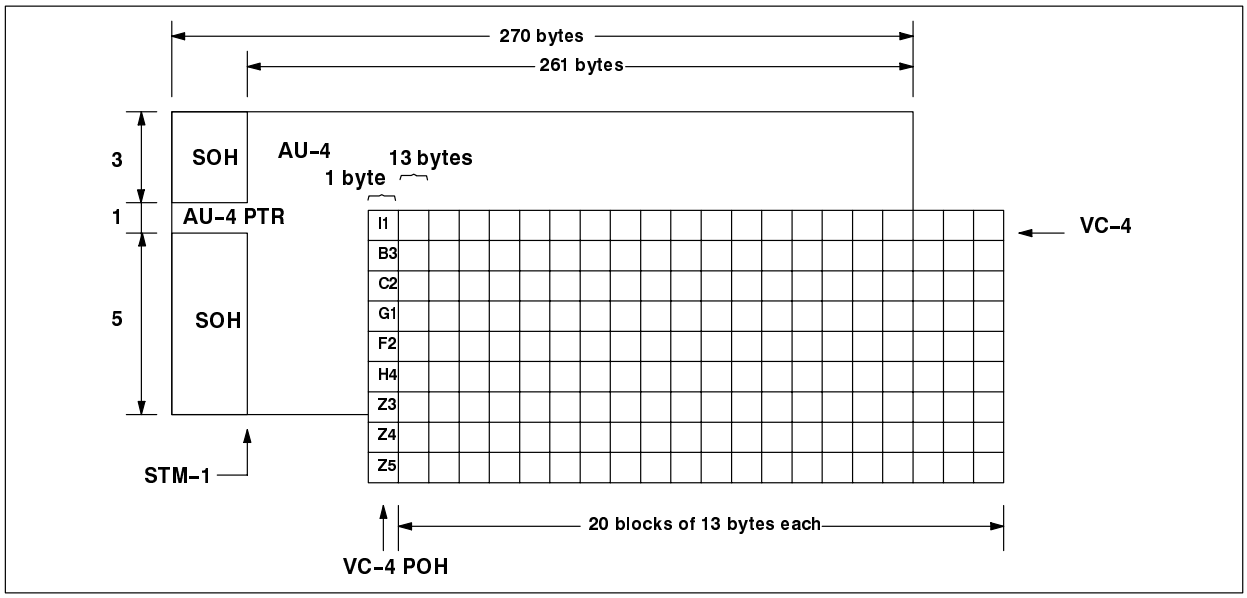


Fig. MN–10 *Insertion of a Plesiochronous 139264kbit/s Signal into an STM–1 Signal*

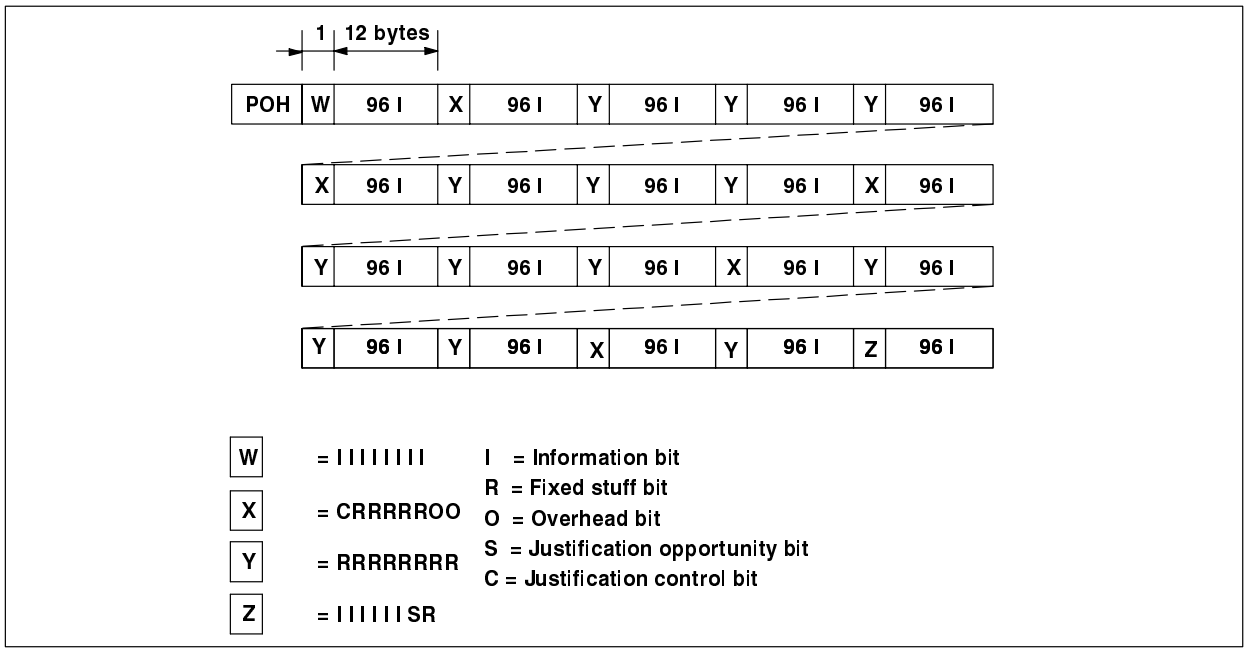


Fig. MN–11 *A Row from the 9–Row Structure*

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