Appendix SH
SDH Principles

General

The Synchronous Digital Hierarchy is a communication protocol based on hierarchic levels and designed for high speed digital data links operating on optical fibre transmission bearers.

The protocol has been developed in view of the need for eliminating the limits set by the asynchronous hierarchy so as to meet the growing demands for improved flexibility and efficiency in line utilization.

Initially the principal object was to develop a synchronous network with optical interfaces, designed and developed by different manufacturers, but all mutually compatible.

Subsequently other aspects were also taken into consideration and a synchronous system was defined which offered the following advantages compared with former methods:

- *simplified multiplexing/demultiplexing techniques;*
- *direct extraction/insertion of lower speed tributaries without having to multiplex/demultiplex the entire frame;*
- *exchange operations, administrative and maintenance capability.*

Synchronous Transport Module of Level 1

The STM frame is the basic unit of information of the Synchronous Digital Hierarchy and is defined as the first level where the bit rate is 155.520kbit/s.

End–user information (Tributary Streams) is assembled within the frame into blocks (Containers) and groups of blocks (Hierarchical Structures) according to well defined procedures.

During the first two basic multiplexing operations, the plesiochronous and/or synchronous tributary streams are assembled coherently according to their bit rate (1.5–2–6–34–45–140Mbit/s) first into Containers (C–n, n= 1 to 4) and then into virtual containers (VC–n, n=1 to 4) by adding to them each time specific groups of bits (bytes).

Bytes added to form Containers consist of justification and stuff bits.

Bytes added to form Virtual Containers provide virtual container path information (e.g. performance monitoring,alarm status indications) between point of insertion of the tributary stream and its point of extraction.

An additional group of bytes (TU Pointer) is added to each basic Virtual Container; this group occupies a specific position within the frame and locates the start of the Container with which it forms a Tributary Unit (TU).

Tributary Units are multiplexed into a Tributary Unit Group (TUG) by single–byte interleaving.

Two different types of Tributary Unit Group can be formed depending on the transmission speed of the TUs included in the TUG: high–speed 34 or 45Mbit/s (TUG3) and low–speed 6Mbit/s (TUG2).

Low–speed TUGs can be further multiplexed into Tributary Unit Group of higher transmission speed.

Tributary Unit Groups are multiplexed into a higher level Virtual Container (VC–n, n=3,4) to which groups of bytes are added to provide virtual container path information between the point of assembly of the VC–n and its point of disassembly.

An additional group of bytes (AU Pointer) is added to each VC–n; this group occupies a specific position within the frame and locates the start of the Higher Order Virtual Container with which it forms an Administrative Unit (AU).

Depending on the transmission speed (45 or 140Mbit/s), three or one AUs can be assembled into an Administrative Unit Group (AUG); a group of bytes defined Section overhead (SOH) carrying section information (e.g. section data communication, error monitoring, APS signalling) is added to the AUG to form the Synchronous Transport Module Level 1 (STM–1).

The structure of the STM–1 frame is illustrated in Fig. SH–1 in case of 140Mbit/s; the parameters of the STM–1 frame are listed in Fig. SH–1.

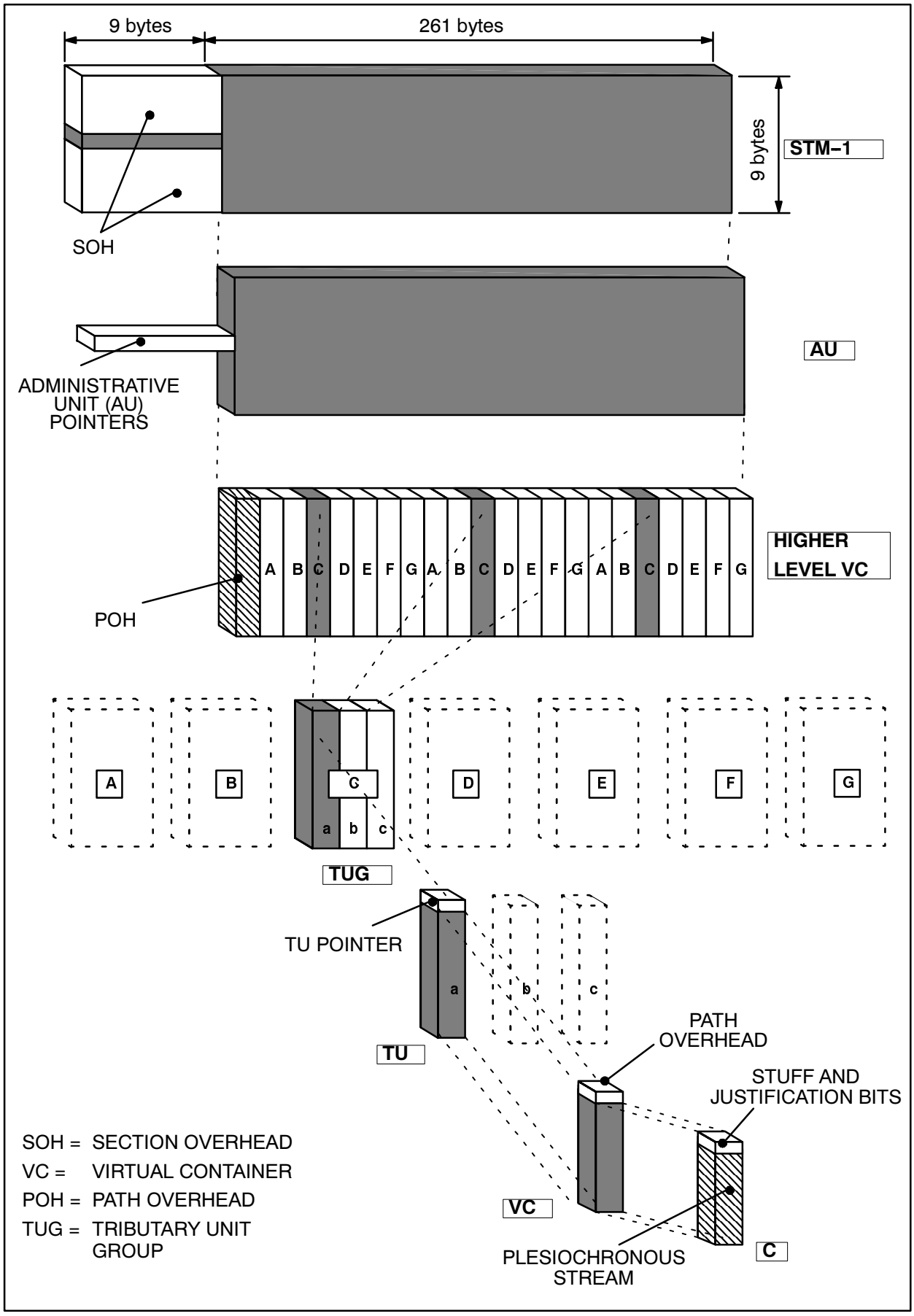


Fig. SH–1 *Structure of STM–1 frame*

Parameters of STM–1 Frame

The Synchronous STM–1 frame (Fig. SH–1) is characterized by the following parameters:

Structure	9 rows of 270 columns (bytes)
Frame width	2430 bytes 19440 bits
Type of frame	125µs
Transmission speed	155.520Mbit/s
Byte–order of transmission	row after row from left to right
Bits–order of transmission	The most significant bit of each byte is sent first and the least significant last
Section Overhead (SOH)	Rows 1 to 3 and 5 to 9 of columns 1 to 9
Payload	all rows of columns 10 to 270

Tab. SH–1 *STM–1 Frame Parameters*

The STM–1 payload consists of different combinations of lower hierarchical order containers.

Containers

The container (Fig. SH–2) is the basic payload unit of the Synchronous Digital Hierarchy.

Containers (C) carry end–user information and have different capacities which make them compatible with the various bit rates of the plesiochronous system.

Containers are designated with the letter ”C” followed by one numeral; depending on the value of these numerals, they are grouped into levels as listed in Fig. SH–2.

	Container	Stream
Level 1	**C11**	1.5Mbit/s
	C12	2Mbit/s
Level 2	**C2**	6Mbit/s
Level 3	**C3**	34Mbit/s or 45Mbit/s
Level 4	**C4**	140Mbit/s

Tab. SH–2 *Type of Containers*

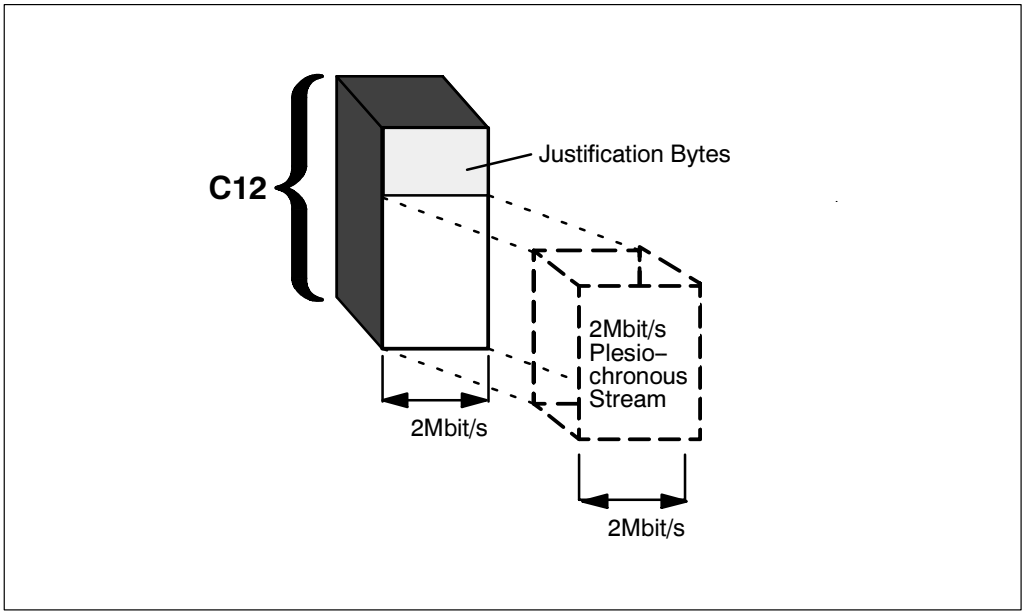


Fig. SH–2 *C–12 Container*

Virtual Containers

A Virtual container (Fig. SH–3) comprises a single Container plus control information appropriate to the level of the Container and designated Path Overhead (POH).

The Path Overhead is provided for communication between the point of assembly of virtual container and its point of disassembly.

Among the functions included in this overhead are path performance monitoring, signals for maintenance purposes and alarm status indications.

The POH consists of one byte if added to a level 1 or 2 payload (1.5, 2, and 6Mbit/s streams) and of nine bytes if added to a level 3 or 4 payload (34, 45 or 140Mbit/s streams).

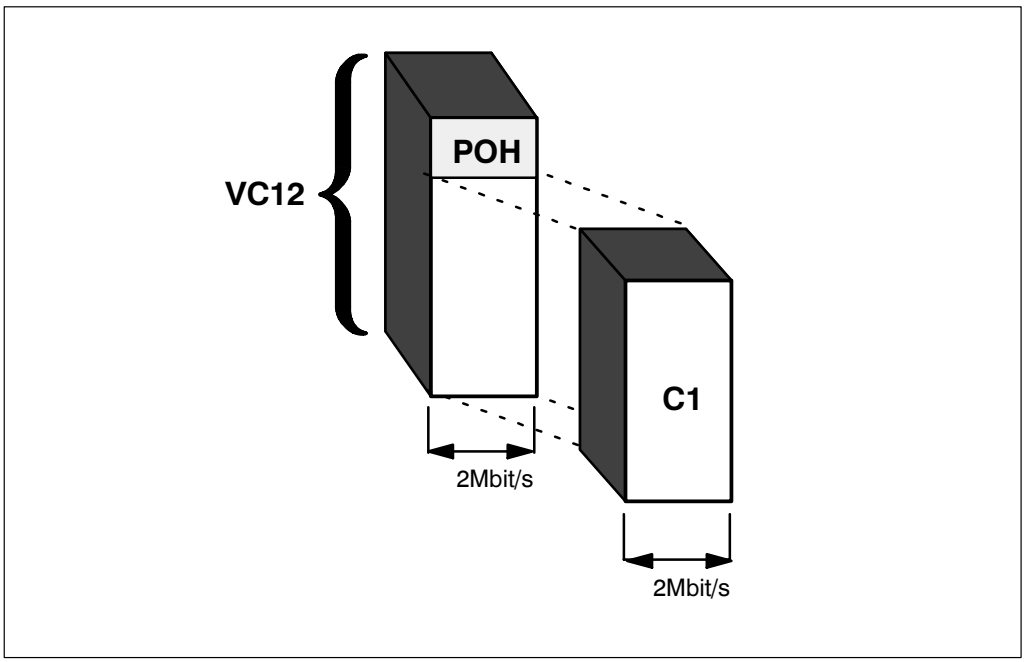
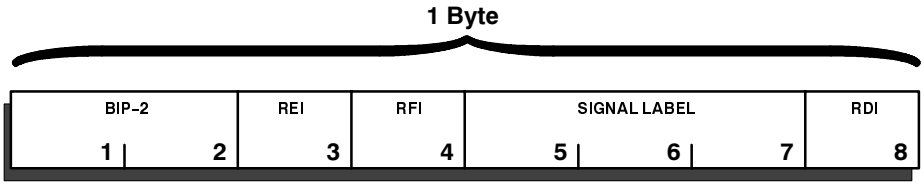


Fig. SH–3 *VC–12 Virtual Container*

The contents of the two types of path overhead are shown in Fig. SH–4 & Fig. SH–5.



REI CODING	
0	no errors
1	one or two errors

RFI CODING	
0	no failure
1	remote failure indication

RDI CODING	
0	error check correct
1	error check wrong

SIGNAL LABEL CODING	
0 0 0	unequipped
0 0 1	equipped non–specific payload
0 1 0	asynchronous
0 1 1	bit synchronous
1 0 0	byte synchronous
1 0 1	reserved
1 1 0	O.181 test signal (TSS4)
1 1 1	VC–AIS

BIP –2 = BIT INTERLEAVED PARITY (ERROR CHECKING)
REI (FORMER FEBE) = REMOTE ERROR INDICATION
RFI = REMOTE FAILURE INDICATION
RDI (FORMER FERF) = REMOTE DEFECT INDICATION

Fig. SH–4 *Path overhead, Levels 1 & 2*

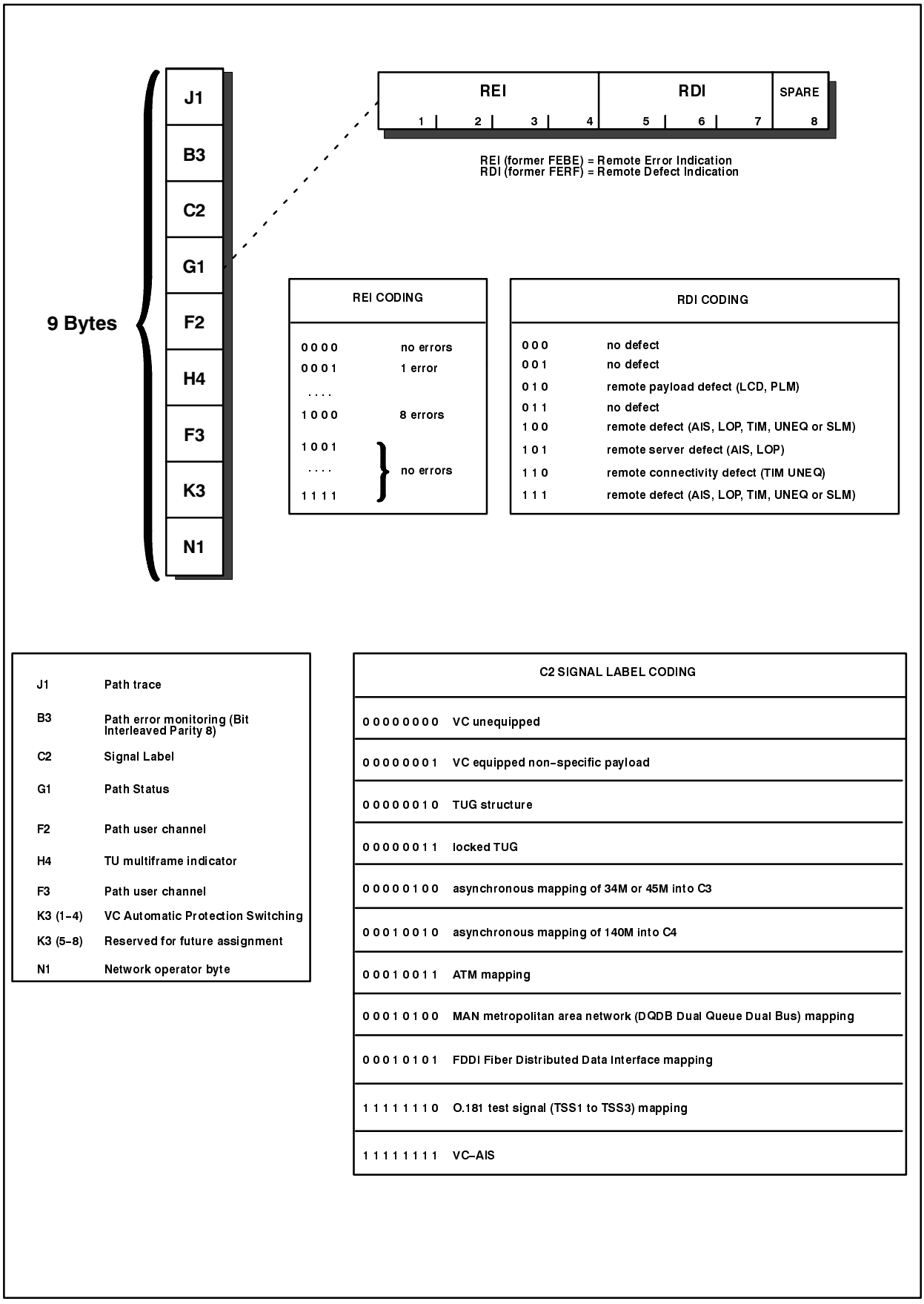


Fig. SH–5 *Path overhead, Levels 3 & 4*

Mapping of tributaries into VCs

Plesiochronous tributaries of level 1 and 2 are mapped into VCs using the floating multiplexing mode in which four consecutive 125μs frames are organized into a 500μs multiframe.

Synchronous tributaries are mapped into VCs using the locked multiplexing mode which overssees insertion of the container into a 125μs frame according to a fixed scheme.

The formats for mapping the various streams into Virtual Containers are shown in Fig. SH–6 to Fig. SH–17.

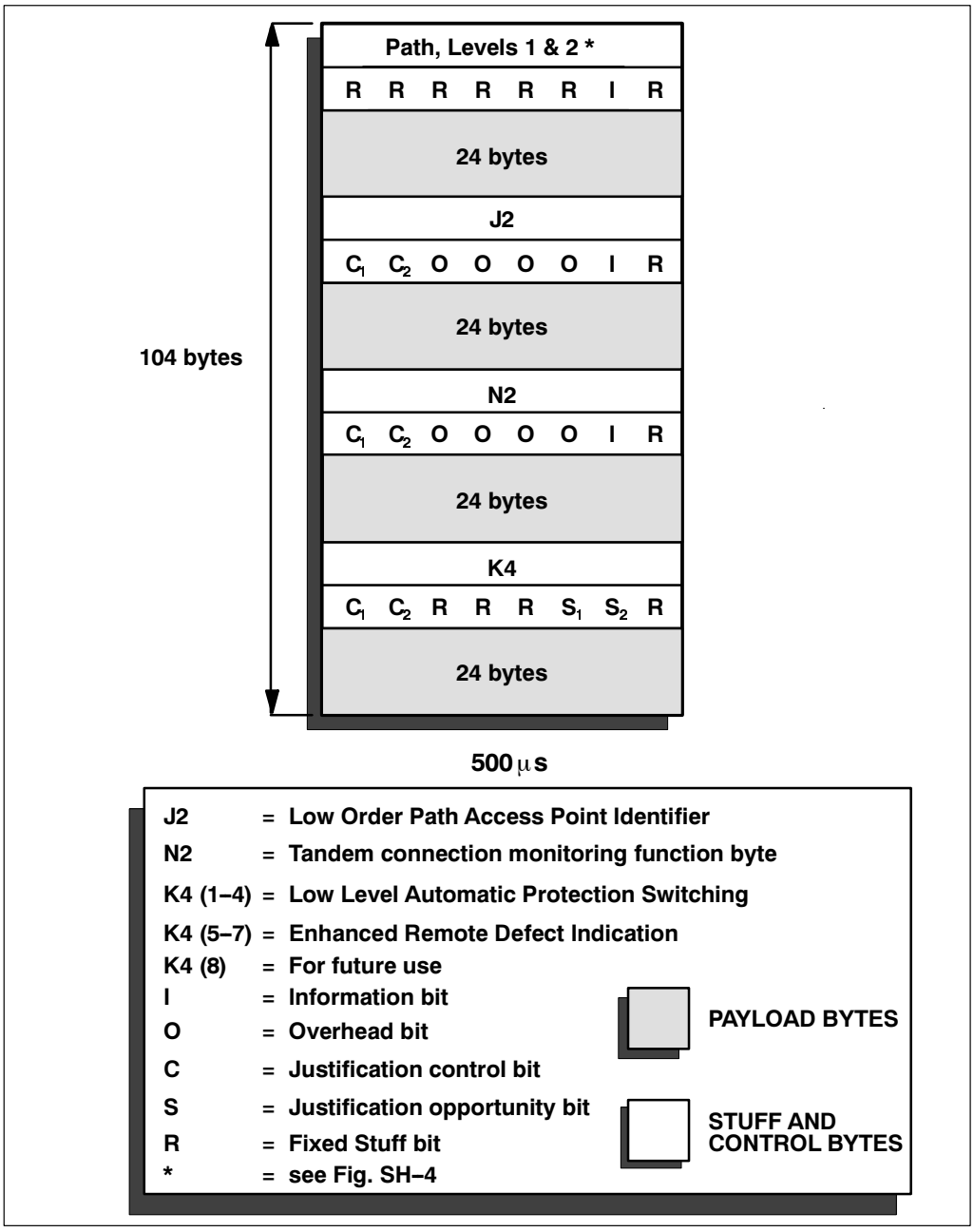


Fig. SH–6 *Asynchronous mapping of 1544kbit/s Tributary into a VC–11*

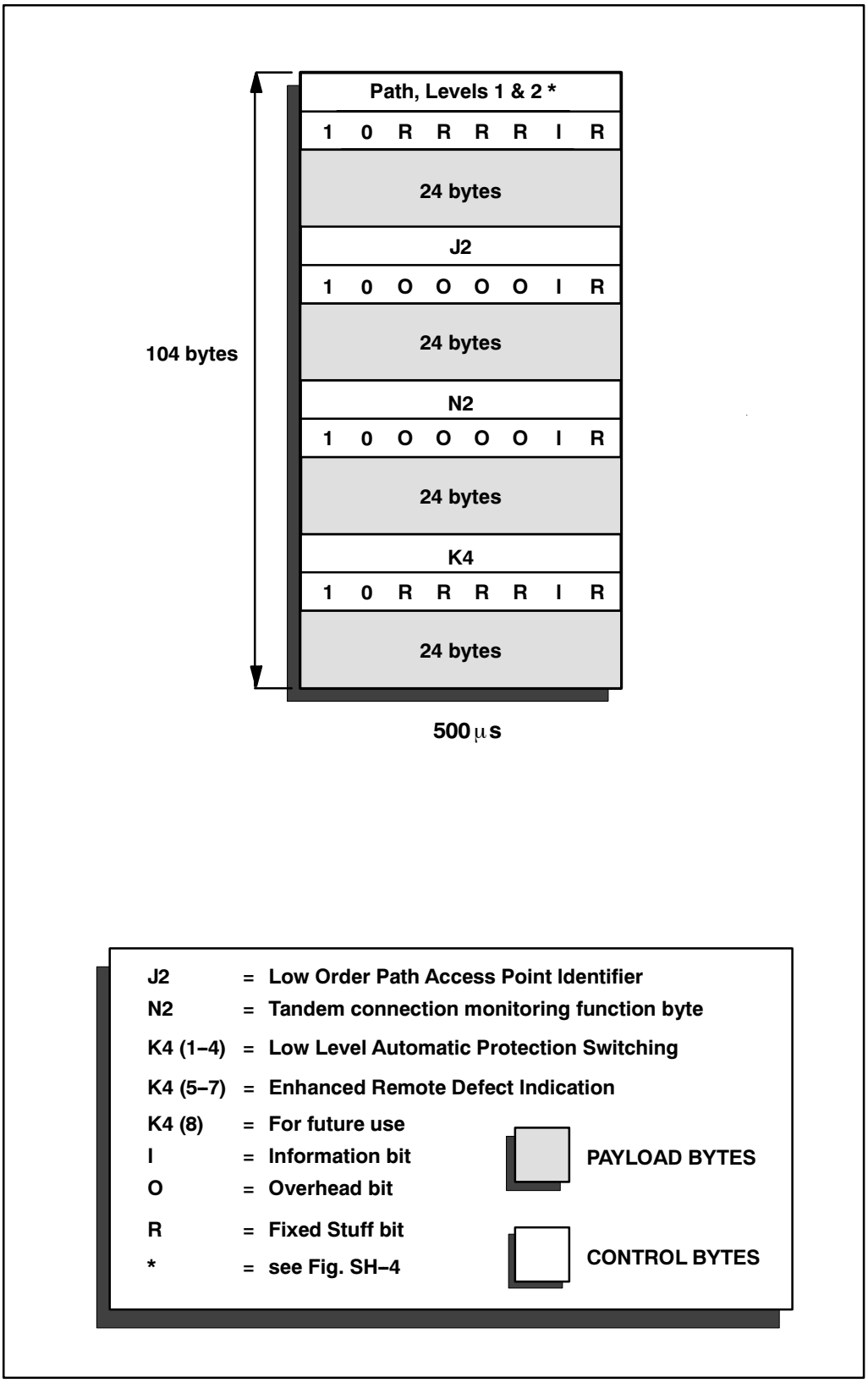


Fig. SH–7 *Mapping of synchronous 1544kbit/s Tributary into a VC–11*

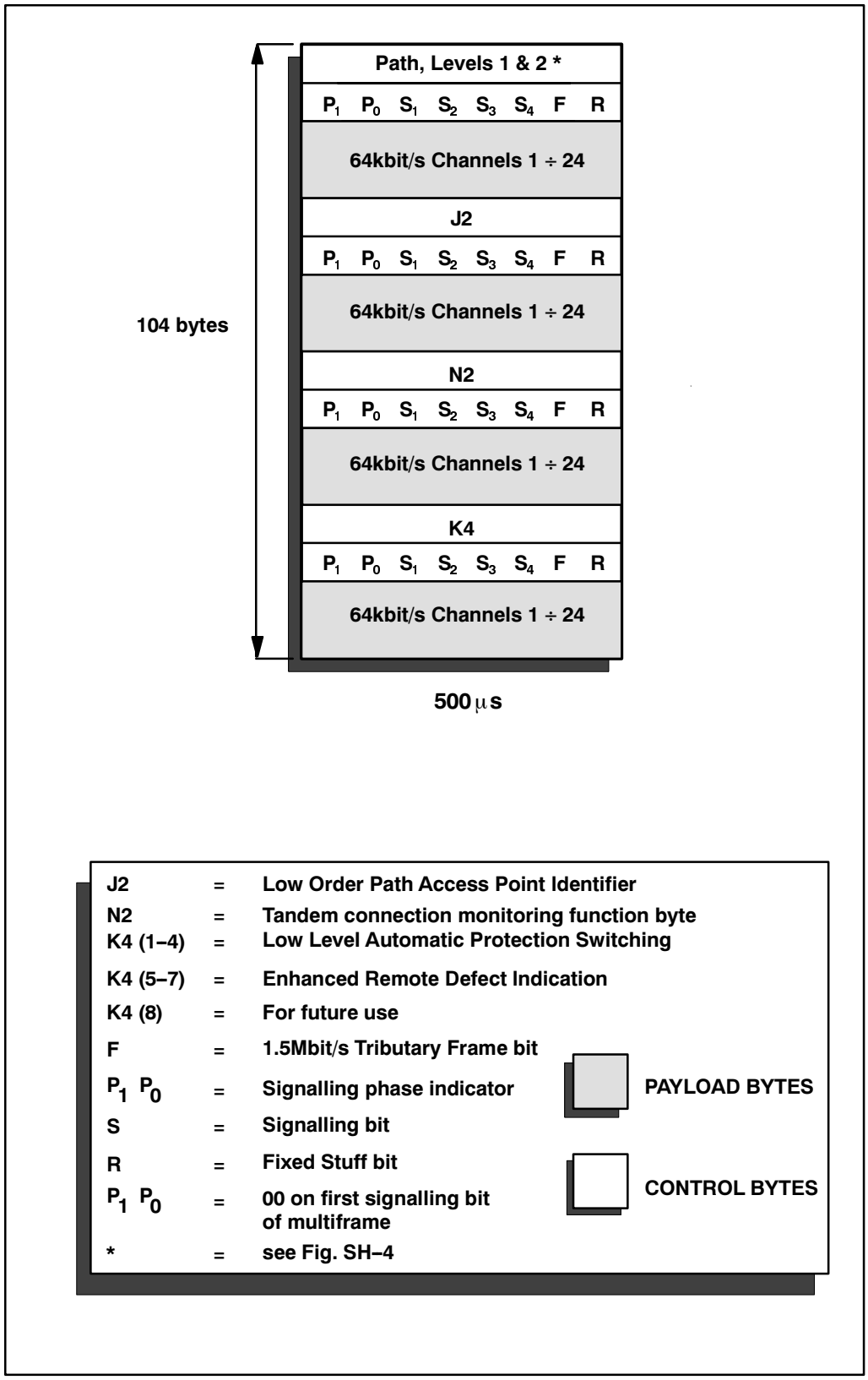


Fig. SH–8 *Mapping of synchronous 1544kbit/s Tributary (24 telephone channels system) into a VC–11*

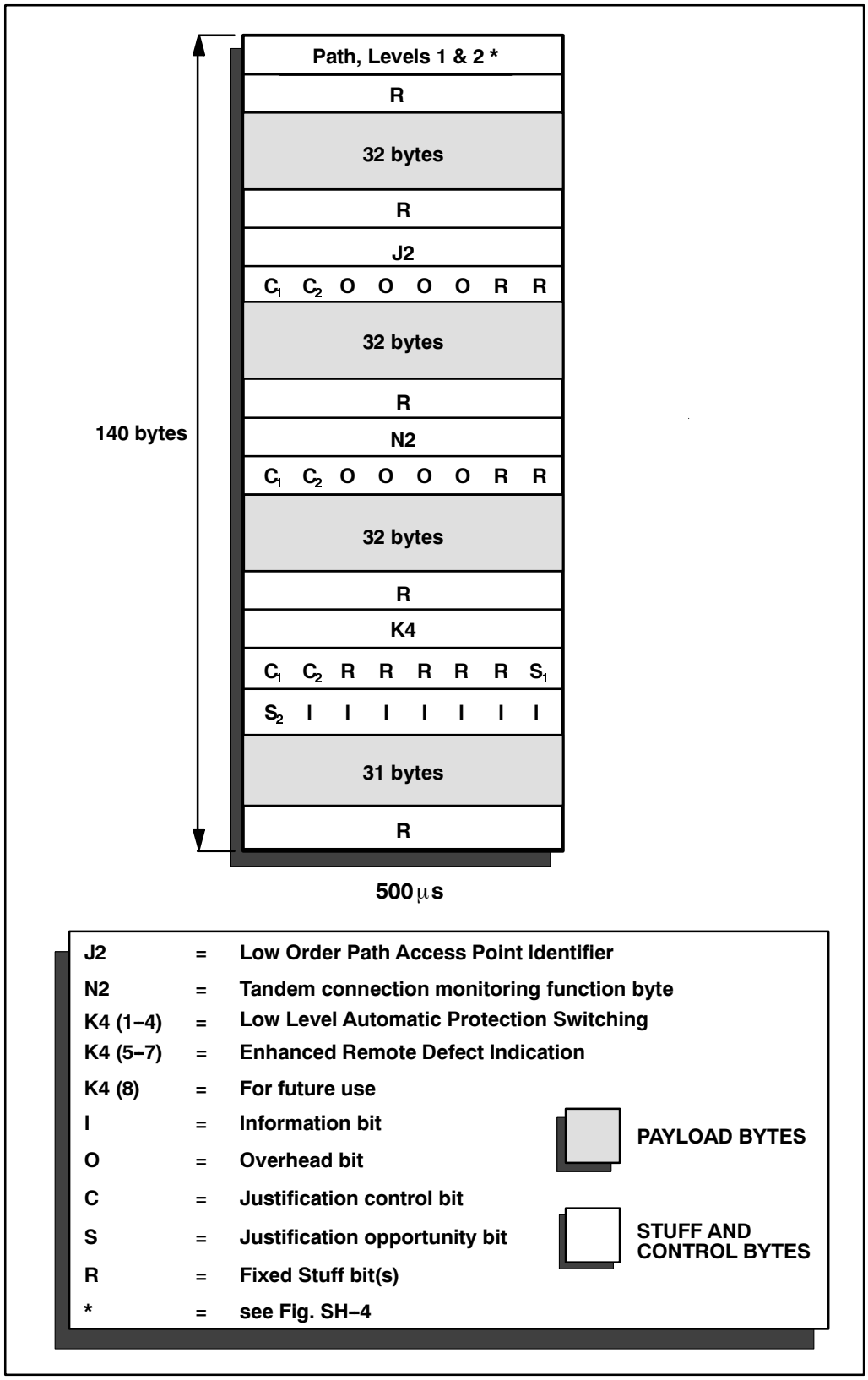


Fig. SH–9 *Asynchronous mapping of 2048kbit/s Tributary into a VC–12*

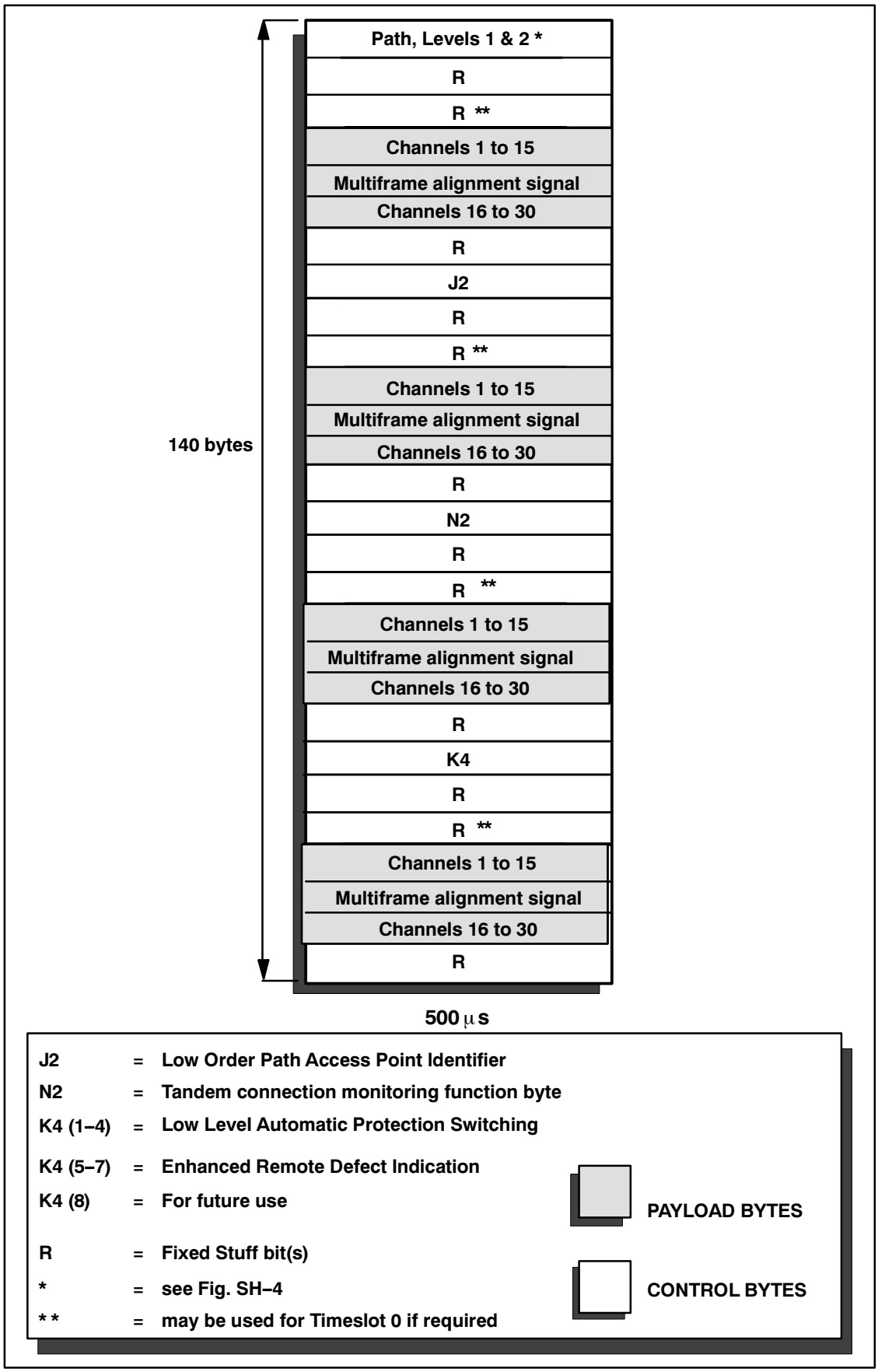


Fig. SH–10 *Synchronous mapping of 2048kbit/s Tributary (30 channels with channel associated signalling) into a VC–12*

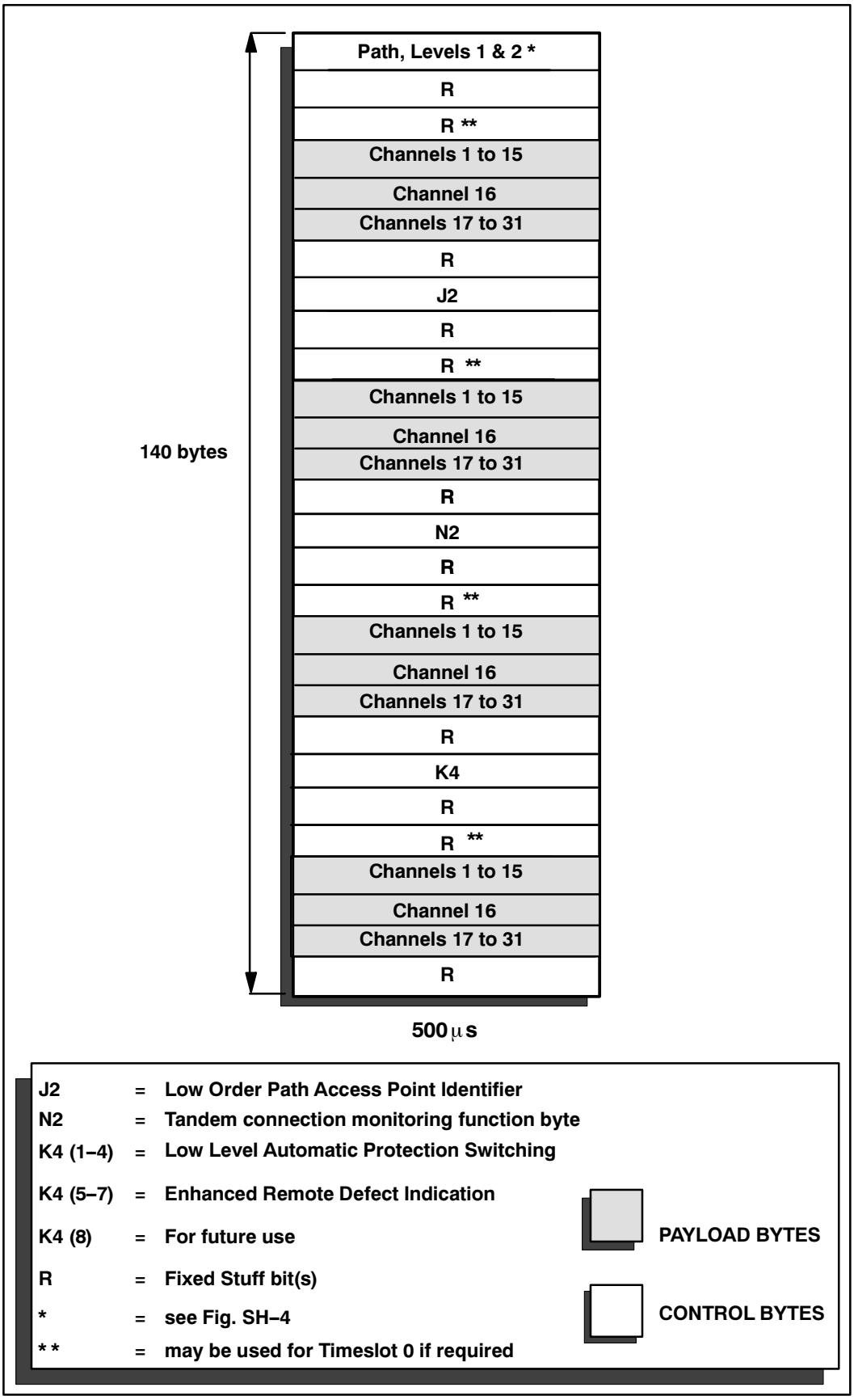


Fig. SH–11 *Synchronous mapping of 2048kbit/s Tributary (31 channels with common signalling channel) into a VC–12*

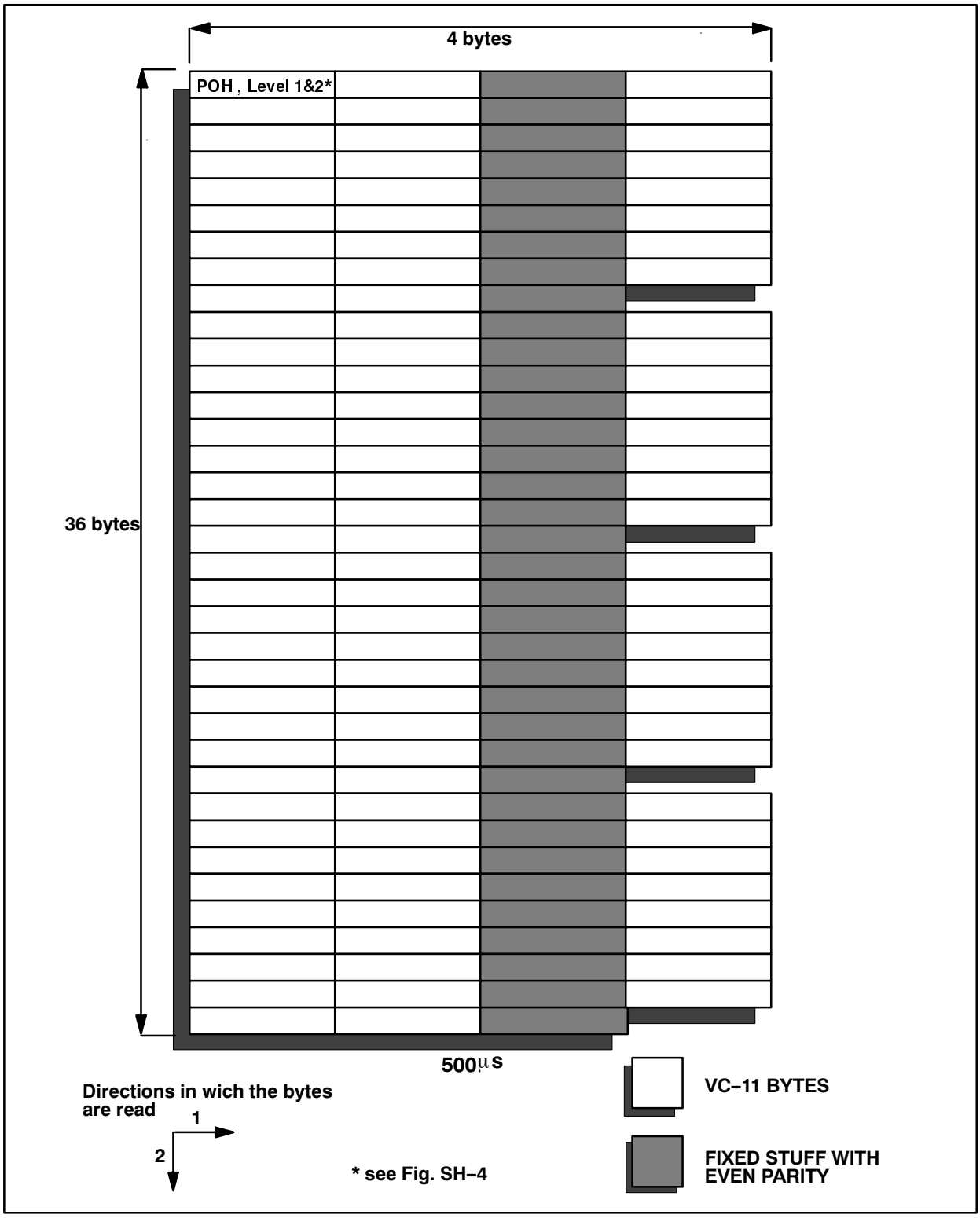


Fig. SH–12 *Conversion of VC–11 to VC–12 for transport by TU–12*

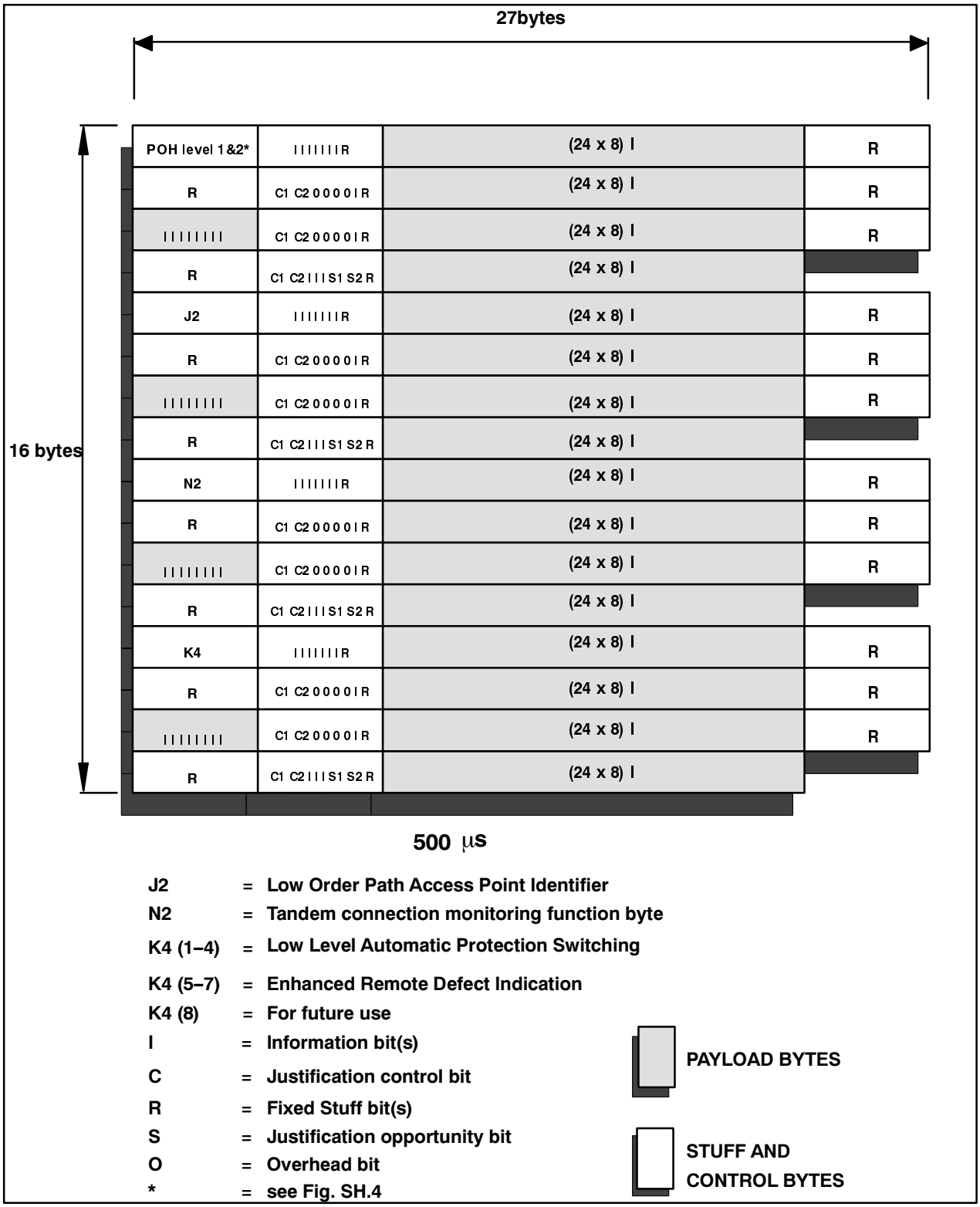


Fig. SH–13 *Asynchronous mapping of 6312kbit/s tributary into a VC–2*

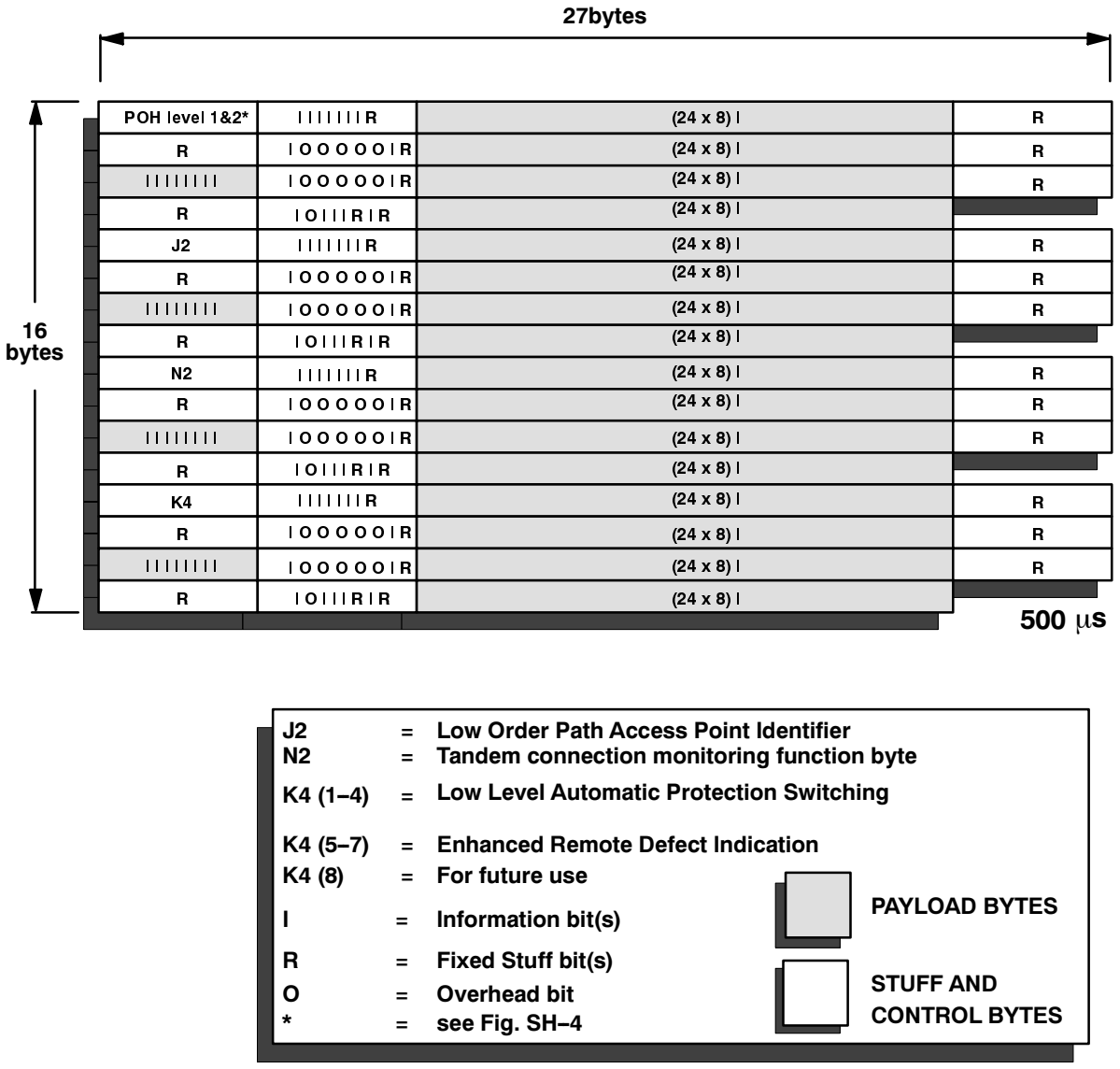


Fig. SH–14 *Synchronous mapping of 6312kbit/s tributary into a VC–2*

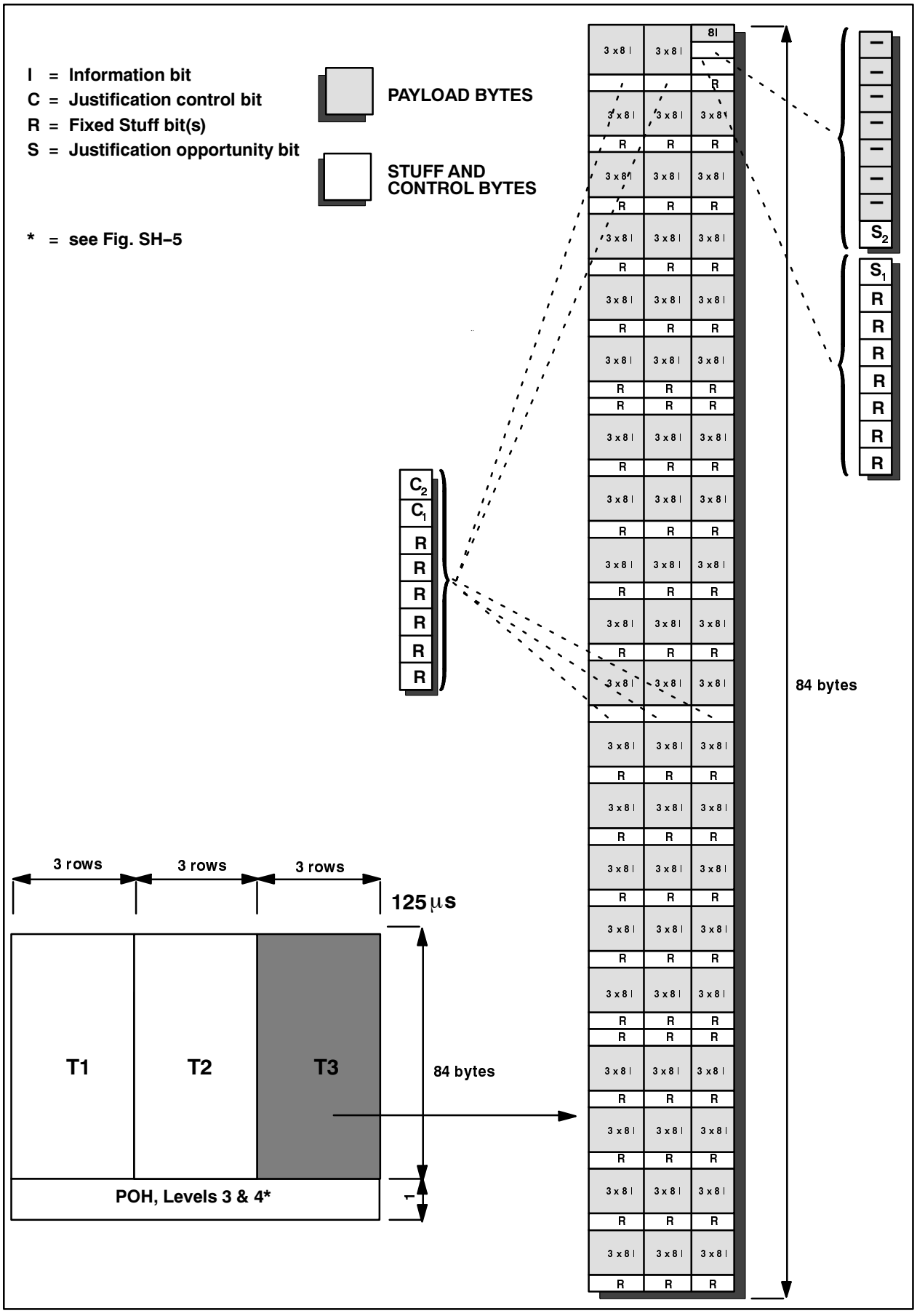


Fig. SH–15 *Asynchronous mapping of 34368kbit/s Tributary into a VC–3*

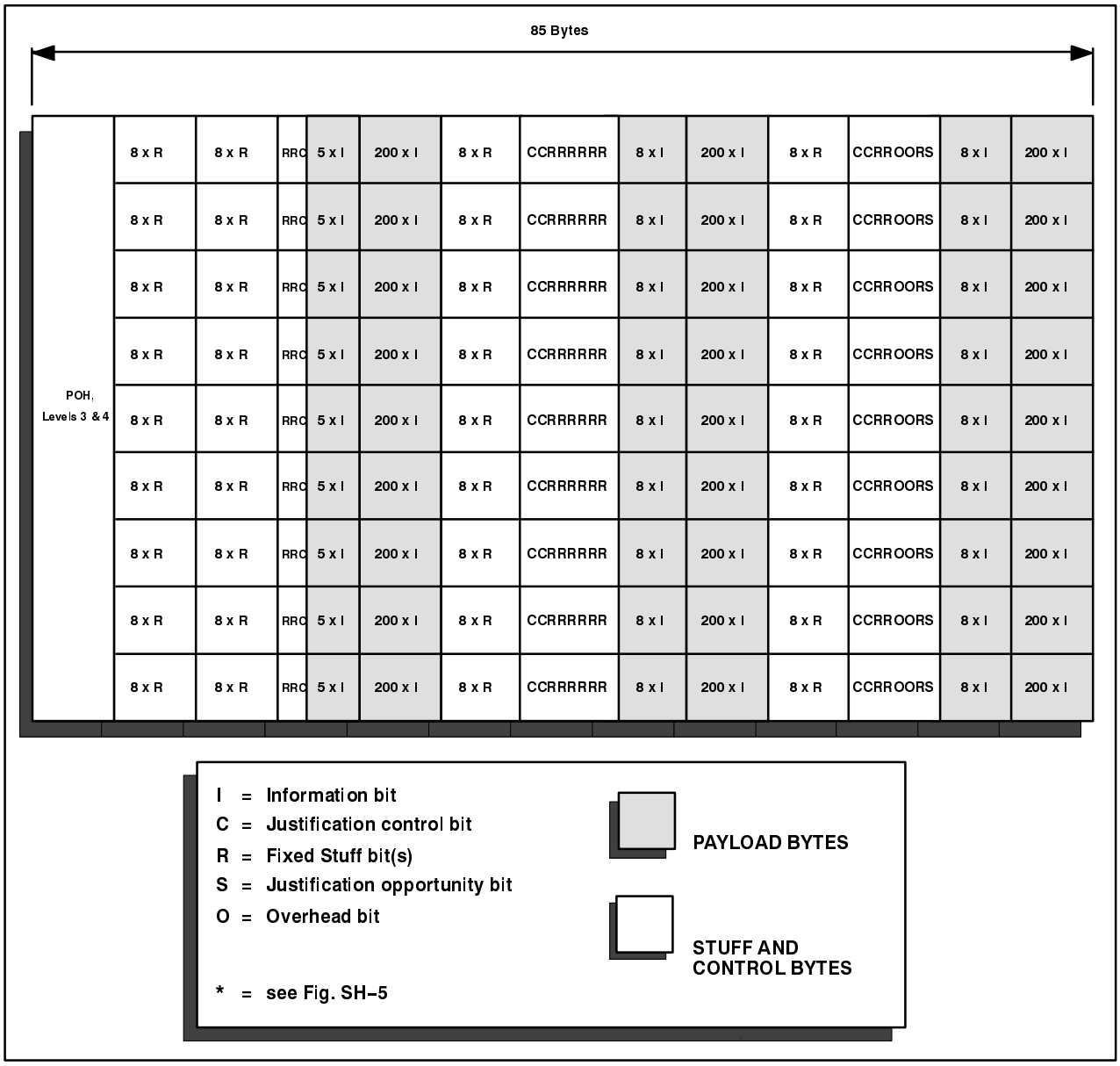


Fig. SH–16 *Asynchronous mapping of 44736kbit/s tributary into a VC–3*

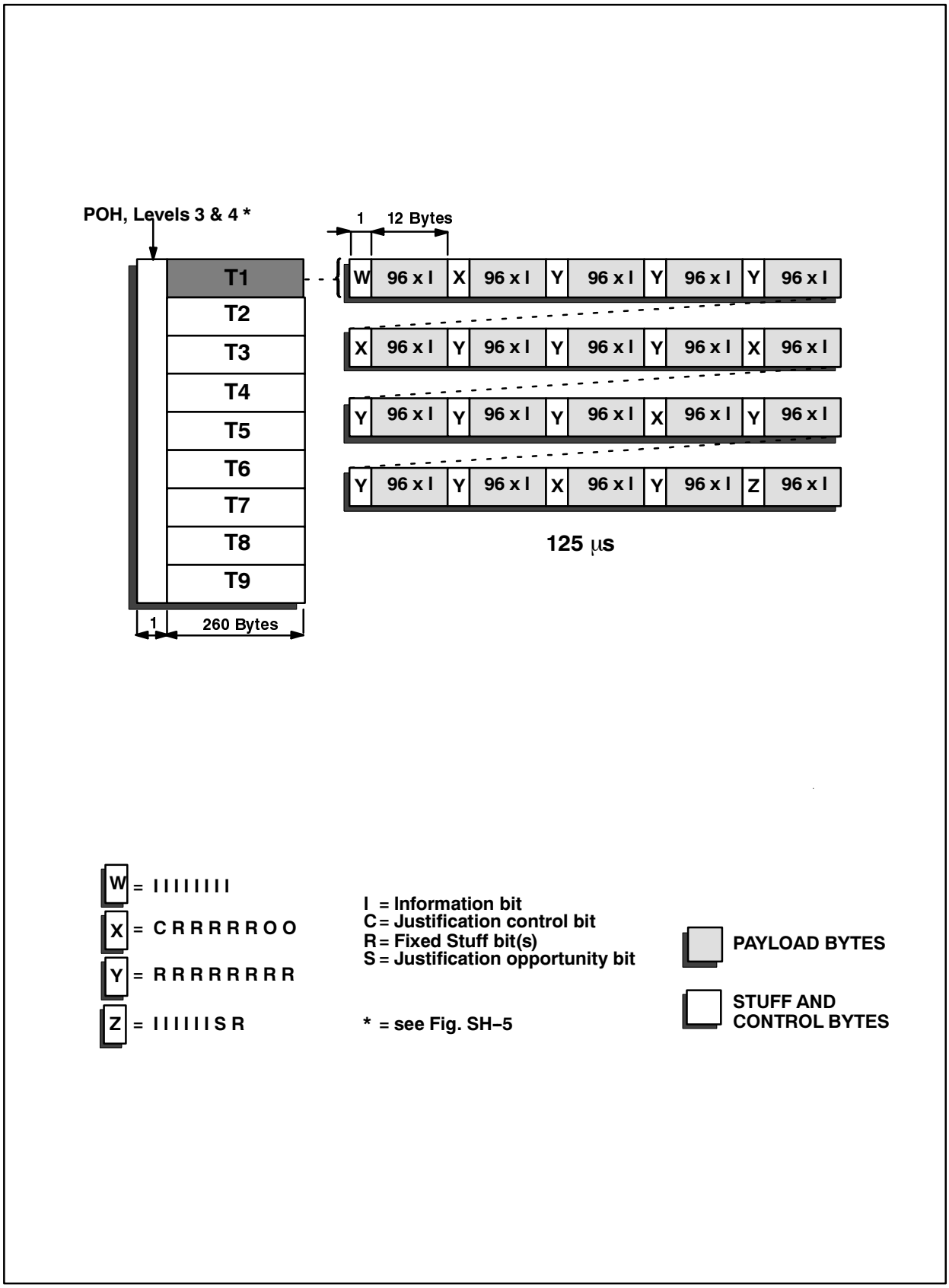


Fig. SH–17 *Asynchronous mapping of 139264kbit/s Tributary into VC–4*

Tributary Units

A Tributary Unit (TU) consists of a Virtual Container (VC) plus a Tributary Unit Pointer (Fig. SH–18).

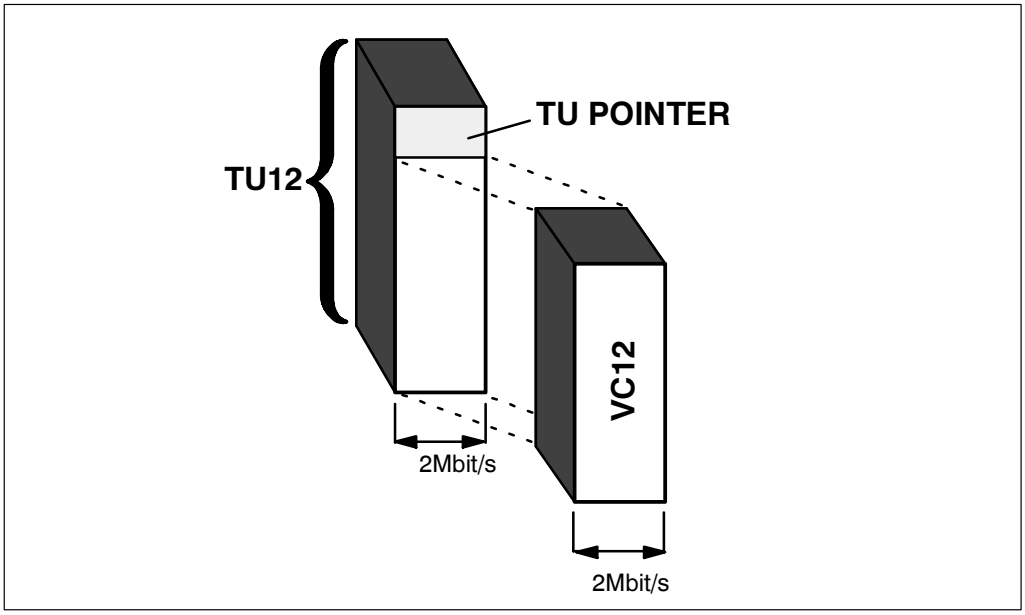
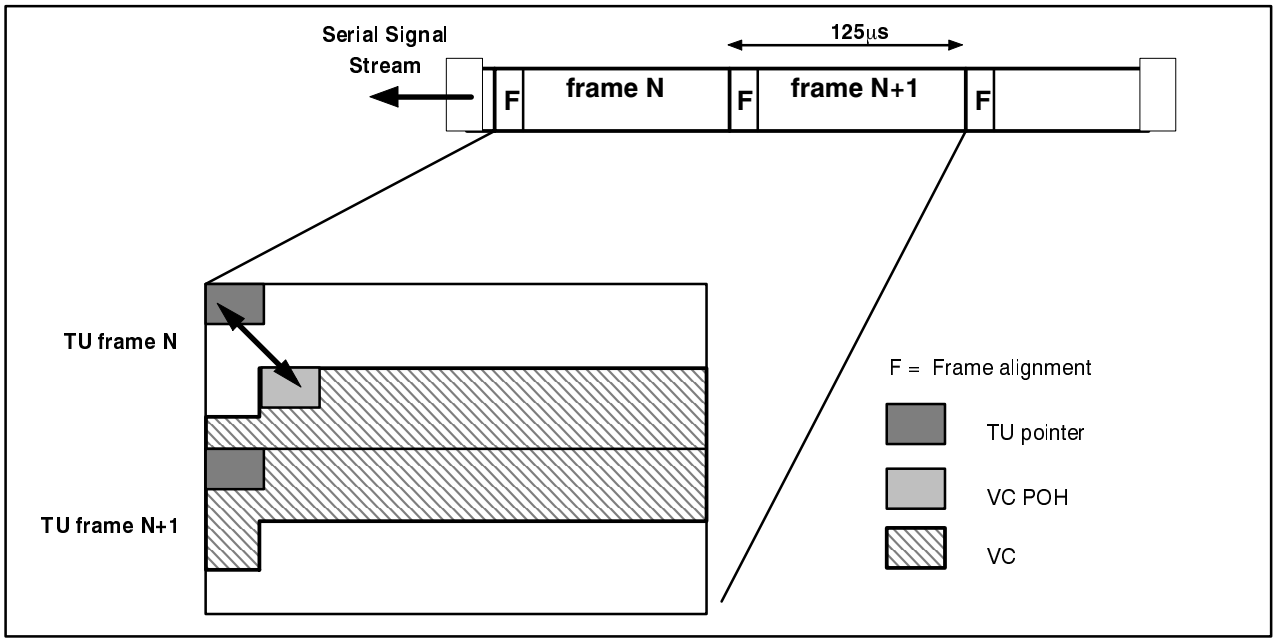


Fig. SH–18 *2Mbit/s Tributary units (TU–12)*

A Tributary Unit Pointer consists of a string of information that provides for flexible dynamic alignment of the Virtual Container within the TU frame.



Dynamic alignment means that the VC is allowed to float within the TU frame.

The string indicates the offset (in bytes) between the Pointer and the first byte of the associated Virtual Container as well as the type of TU and the eventual change of pointer value if the change is due. In the case of Virtual Container of levels 1 and 2, a pointer is only used with floating mapping (500µs multiframe).

The positions and contents of TU Pointers are shown in Fig. SH–19, Fig. SH–20 and Fig. SH–21.

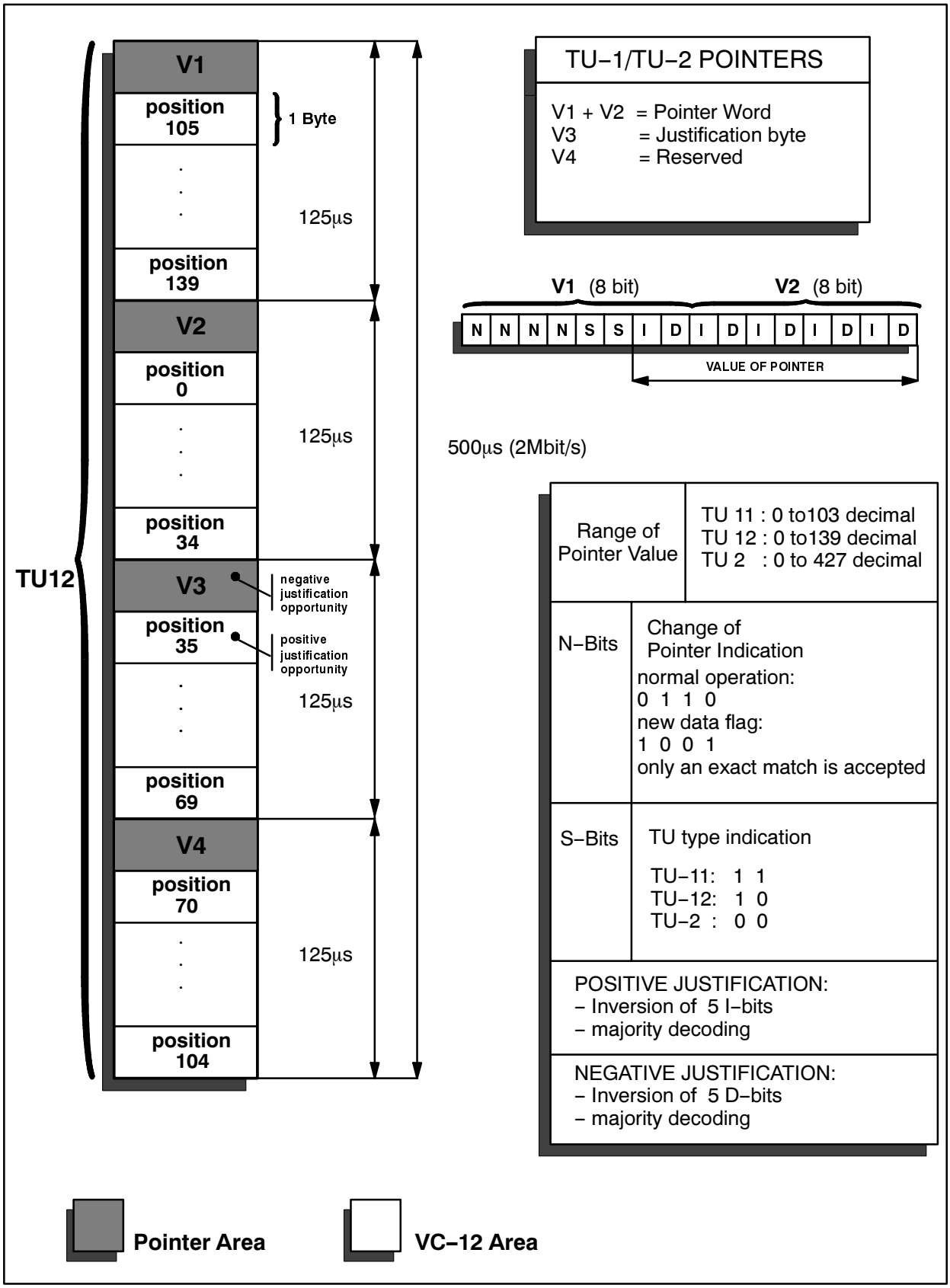


Fig. SH–19 *TU–1, TU–2 pointers layout*

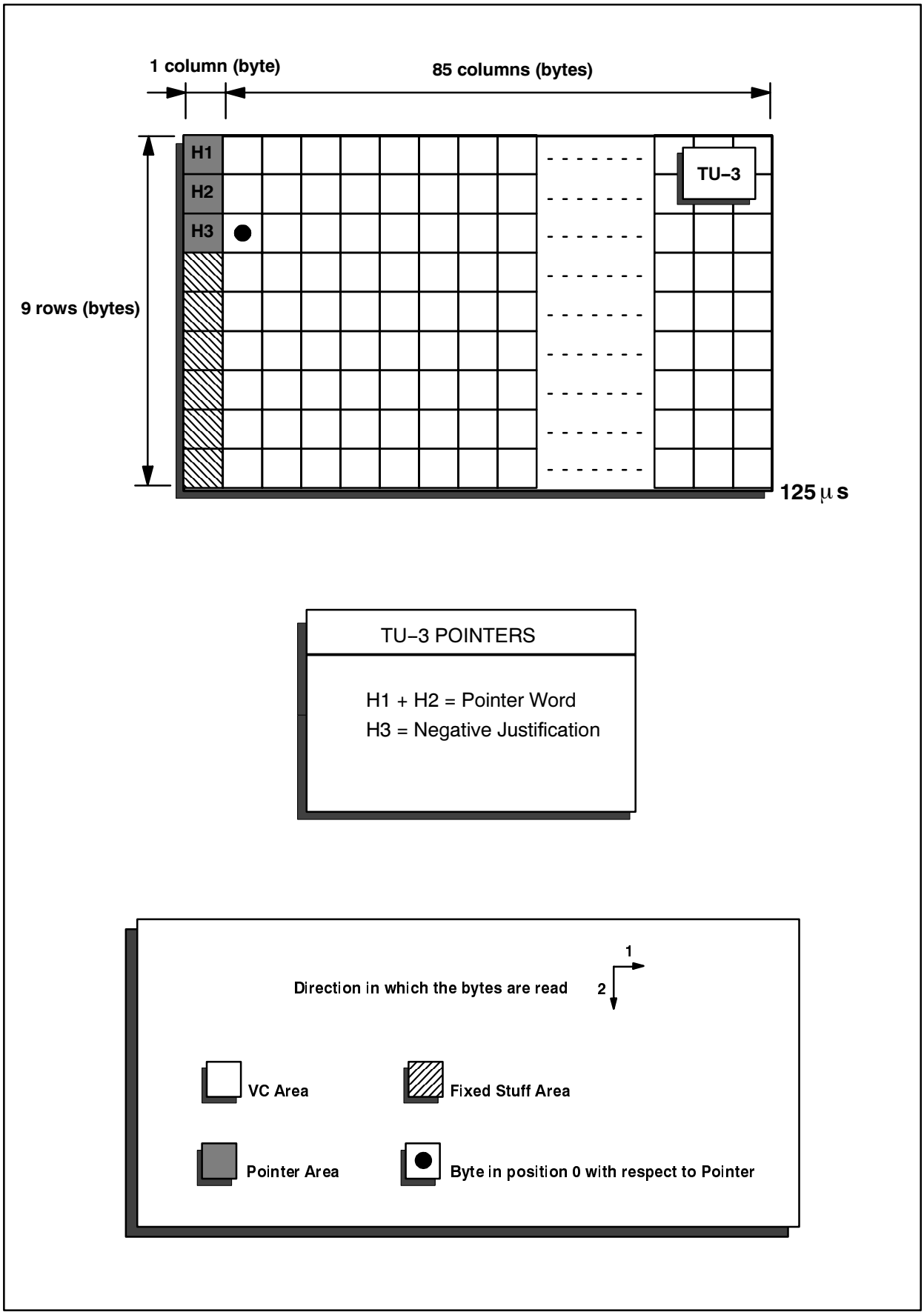


Fig. SH–20 *TU–3 Pointer Layout*

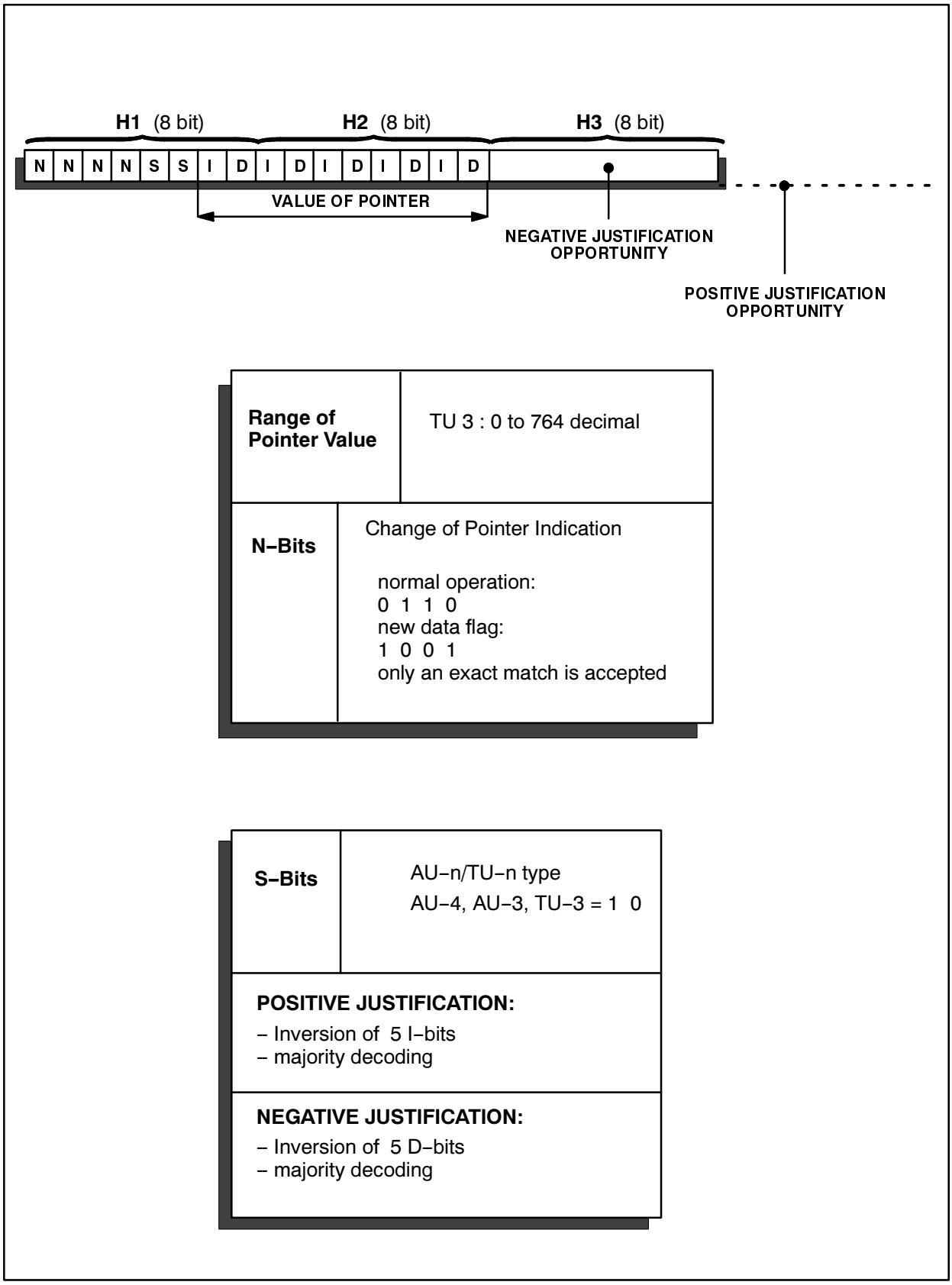


Fig. SH–21 *TU–3 Pointer Word*

Tributary Unit Group (TUG)

Tributary units can be multiplexed into a Tributary Unit Group (TUG) of a higher order or of the same order as the assembled TUs.

High–speed 45Mbit/s and low speed 6Mbit/s TUGs can be formed. Low speed 6Mbit/s TUGs can be multiplexed into TUGs of higher order.

The TUG multiplexing structure and multiplexing methods are shown in detail in the next Section, ”Multiplexing structures”.

Higher Level Virtual Containers (45 and 140Mbit/s)

Tributary Units Groups are further multiplexed into a 45Mbit/s or a 140Mbit/s Higher Level Virtual Container.

These Virtual Containers are to all effects identical to the higher order virtual container comprising a single 45Mbit/s (C–3) or a 140Mbit/s (C–4) tributary streams.

The multiplexing structure of higher order virtual containers and the corresponding multiplexing methods are shown in detail in the next Section, ”Multiplexing Structure”.

Administrative Unit (AU)

An Administrative Unit (AU) consists of a Higher Order Virtual Container plus an Administrative Unit Pointer. (Fig. SH-22)

The available mapping formats are for transporting either a single VC-4 (140Mbit/s) in one AU-4 or three VC-3 (34 or 45Mbit/s) in three AU-3.

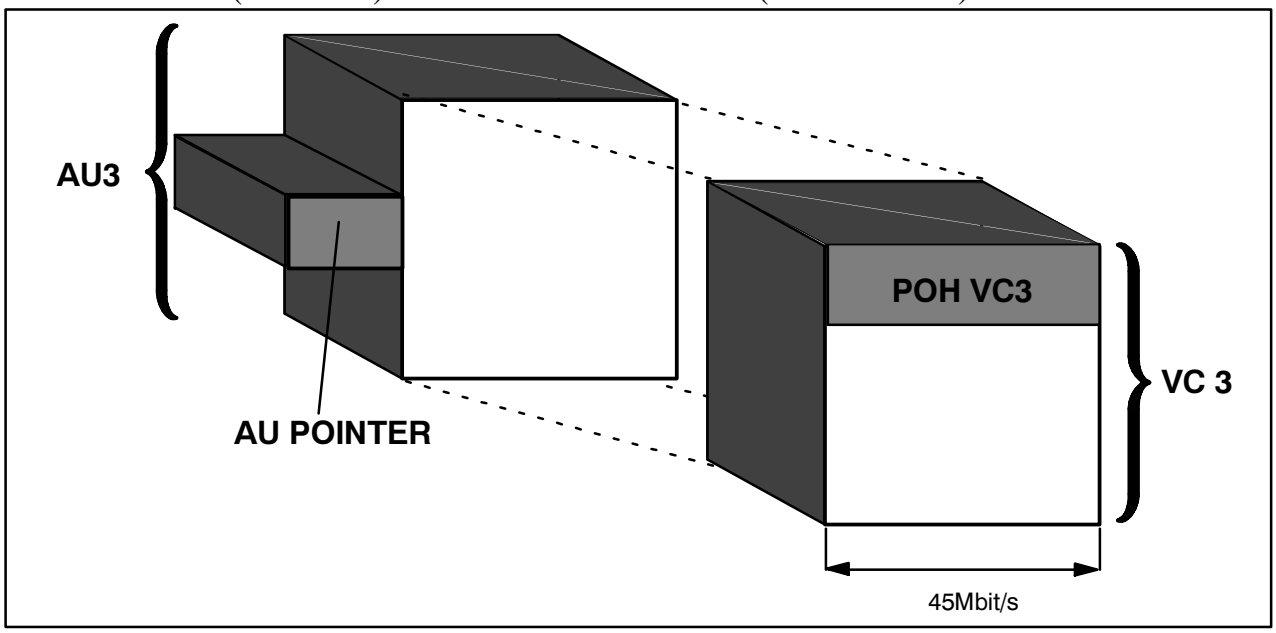
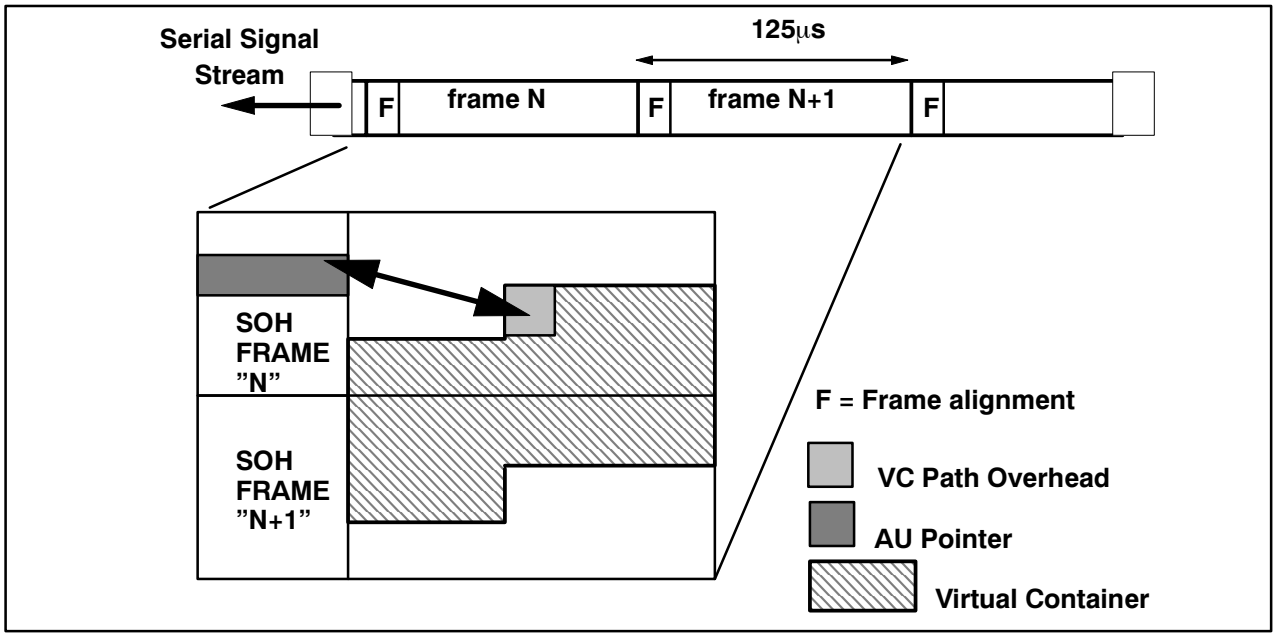


Fig. SH-22 *45Mbit/s Administrative Unit (AU-3)*

The AU pointer consists of an information string that indicates the offset (in bytes) between the pointer and the start of the VCs assembled in the Administrative Unit.



The positions and contents of AU pointers are illustrated in Fig. SH-23 and Fig. SH-24.

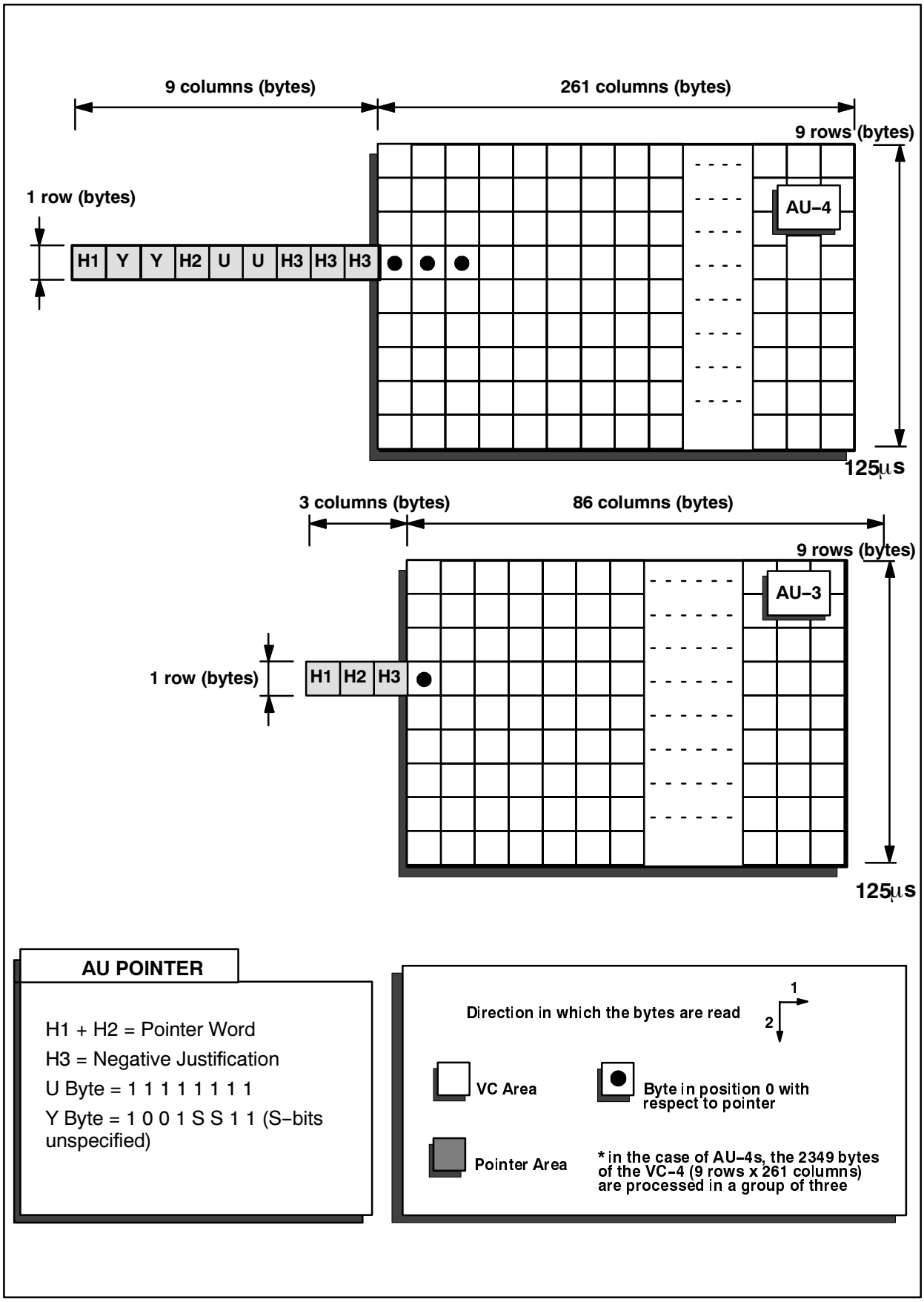
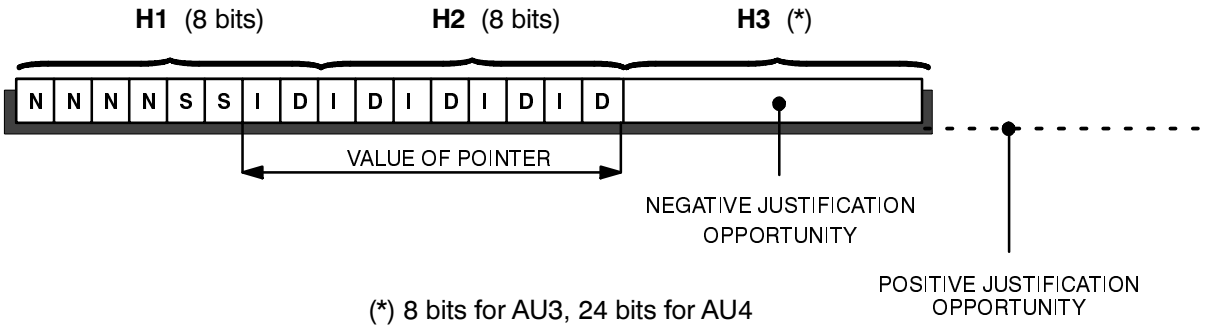


Fig. SH–23 *AU–3, AU–4 Pointer Layout*



Range of Pointer Value	AU 3 : 0 to 782 decimal AU 4 : 0 to 782 decimal
N–Bits	Change of Pointer Indication normal operation: 0 1 1 0 new data flag: 1 0 0 1 only an exact match is accepted

S–Bits	AU type indication AU–4, AU–3: 1 0
POSITIVE JUSTIFICATION: – Inversion of 5 I–bits – Majority decoding	
NEGATIVE JUSTIFICATION: – Inversion of 5 D–bits – Majority decoding	

Fig. SH–24 *AU pointer Word*

Administrative Unit Group (AUG)

Administrative Units are multiplexed into an Administrative Unit Group (AUG).

Either one AU–4 or three AU–3 can be multiplexed into AUGs.

The multiplexing methods are shown in detail in the next Section, ”Multiplexing methods”.

155Mbit/s Synchronous Frame (STM–1)

Control information, called Section Overhead (SOH), is added to the assembled AUs so as to create the 155Mbit/s Synchronous Frame (STM–1) (Fig. SH–25).

The SOH consists of a 72–bytes string which carries information on STM–1 framing, section performance, error monitoring and protection switching control. In addition the SOH provides section data communication, orderwire channels for voice communication and bytes reserved for national use.

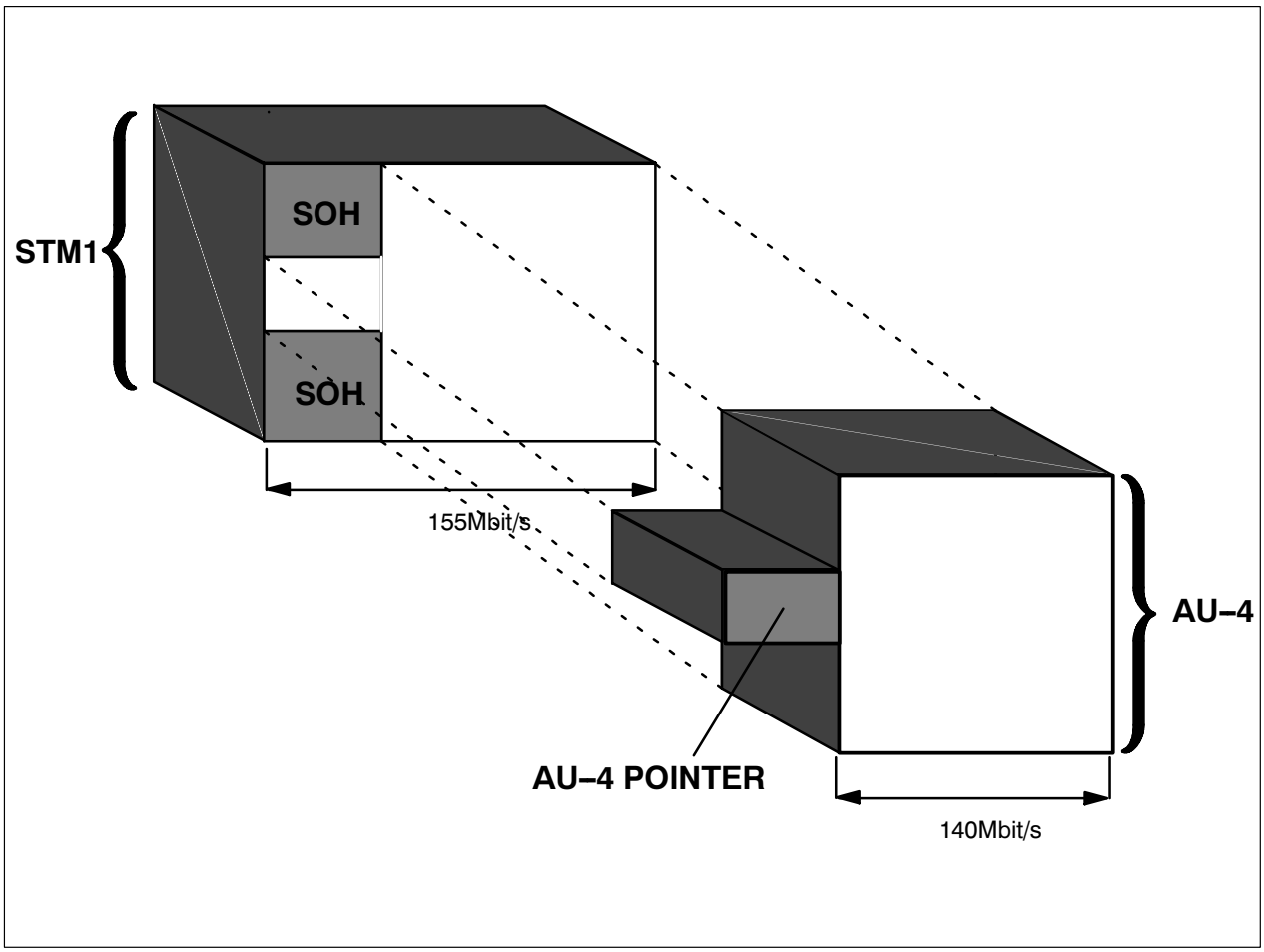


Fig. SH–25 *Synchronous 155Mbit/s Frame (STM–1)*

The SOH content is shown in detail in Fig. SH–26 on the next page.

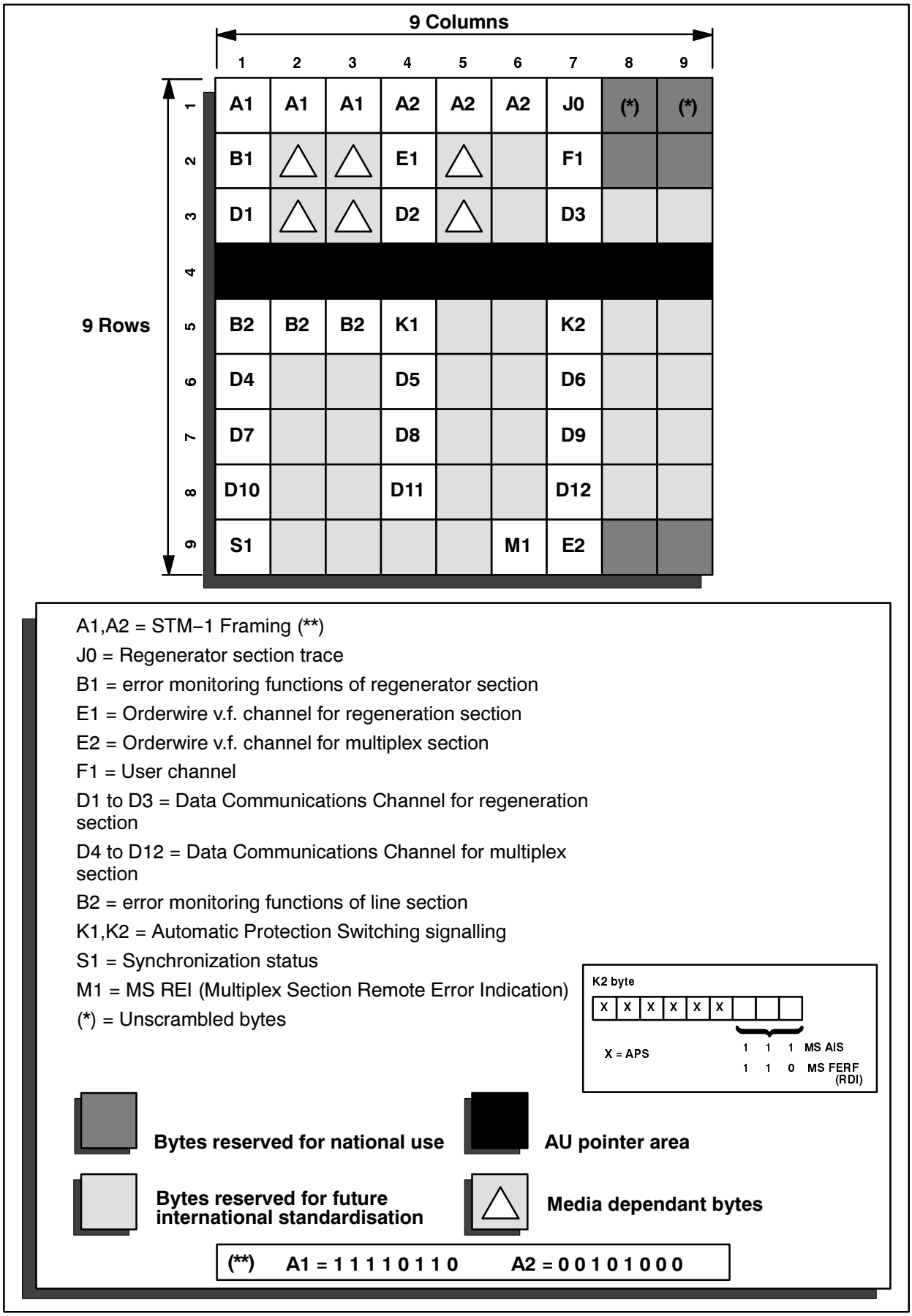
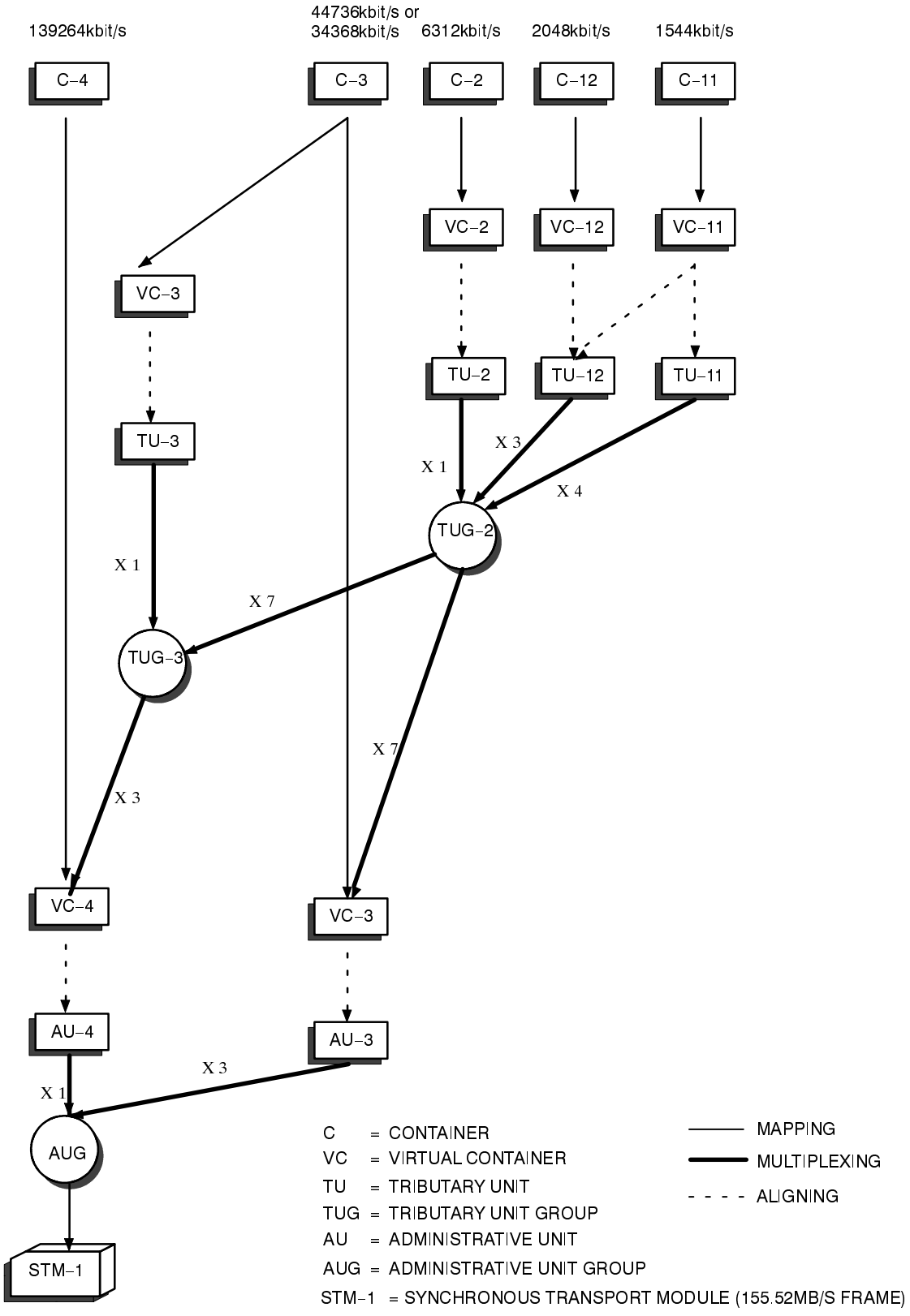


Fig. SH–26 *Location of SOH Bytes in STM–1 frame*

Multiplexing Structure



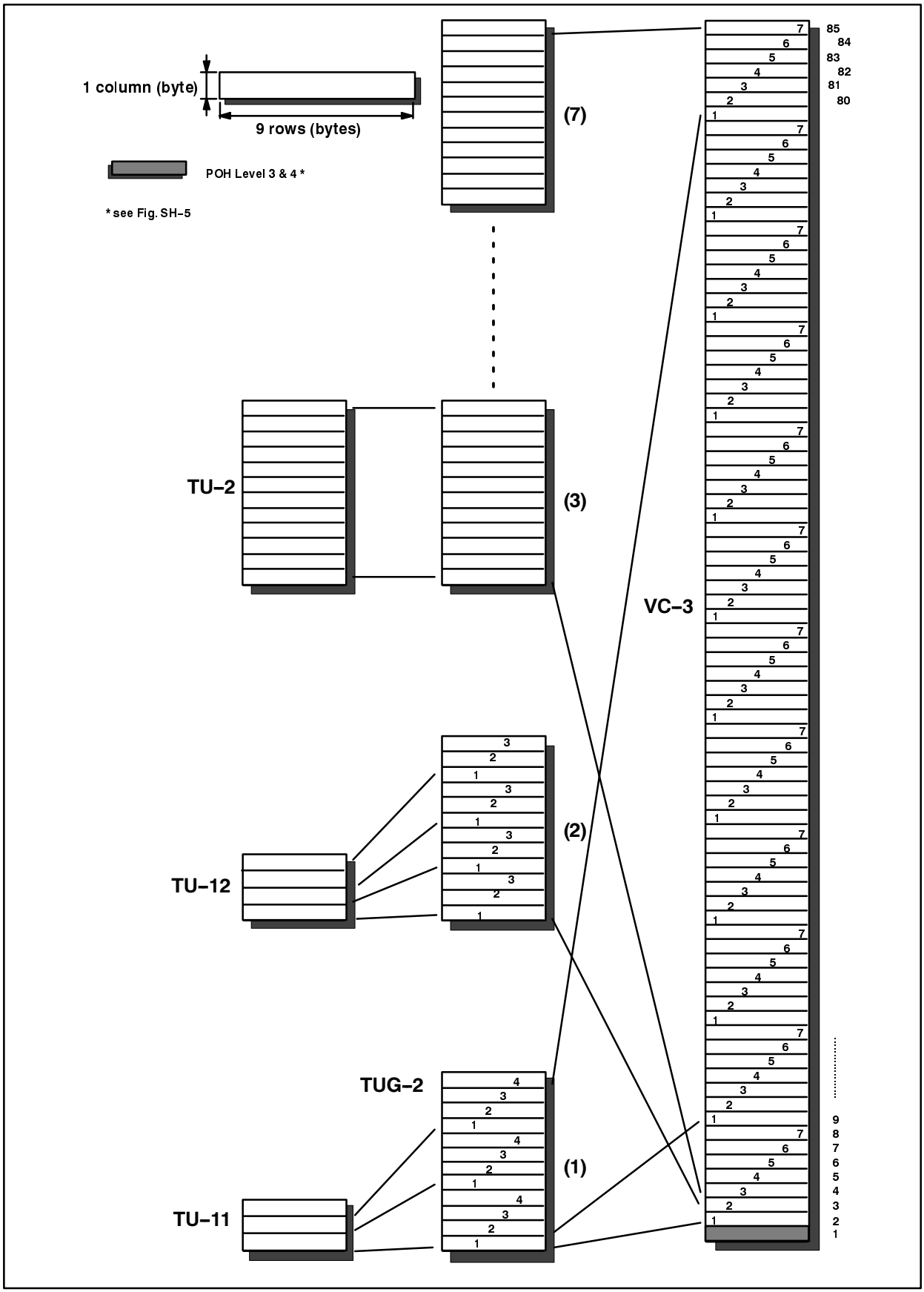


Fig. SH-27 *Multiplexing of 7 TUG-2 into VC-3*

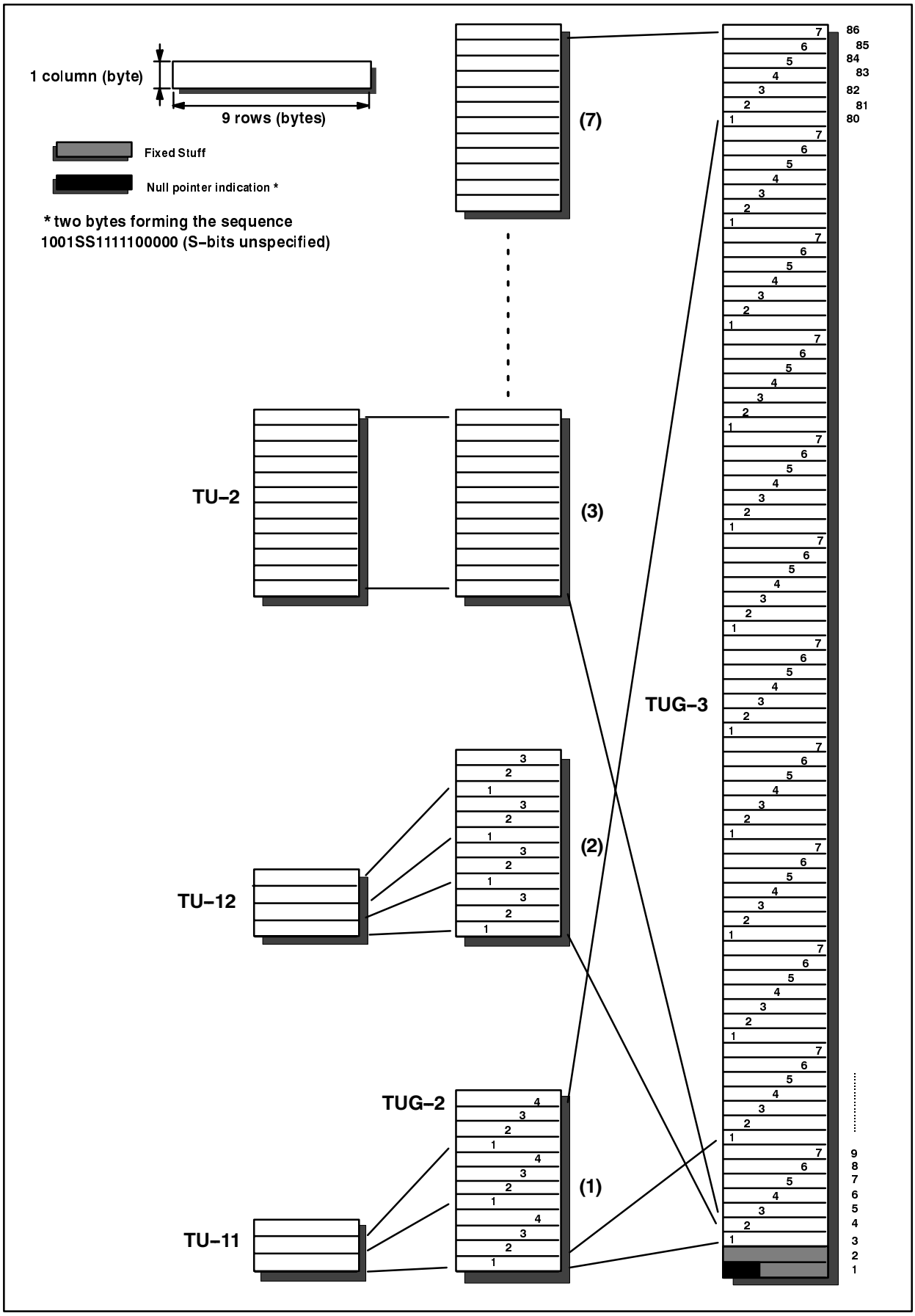


Fig. SH–28 *Multiplexing of 7 TUG–2 into TUG–3*

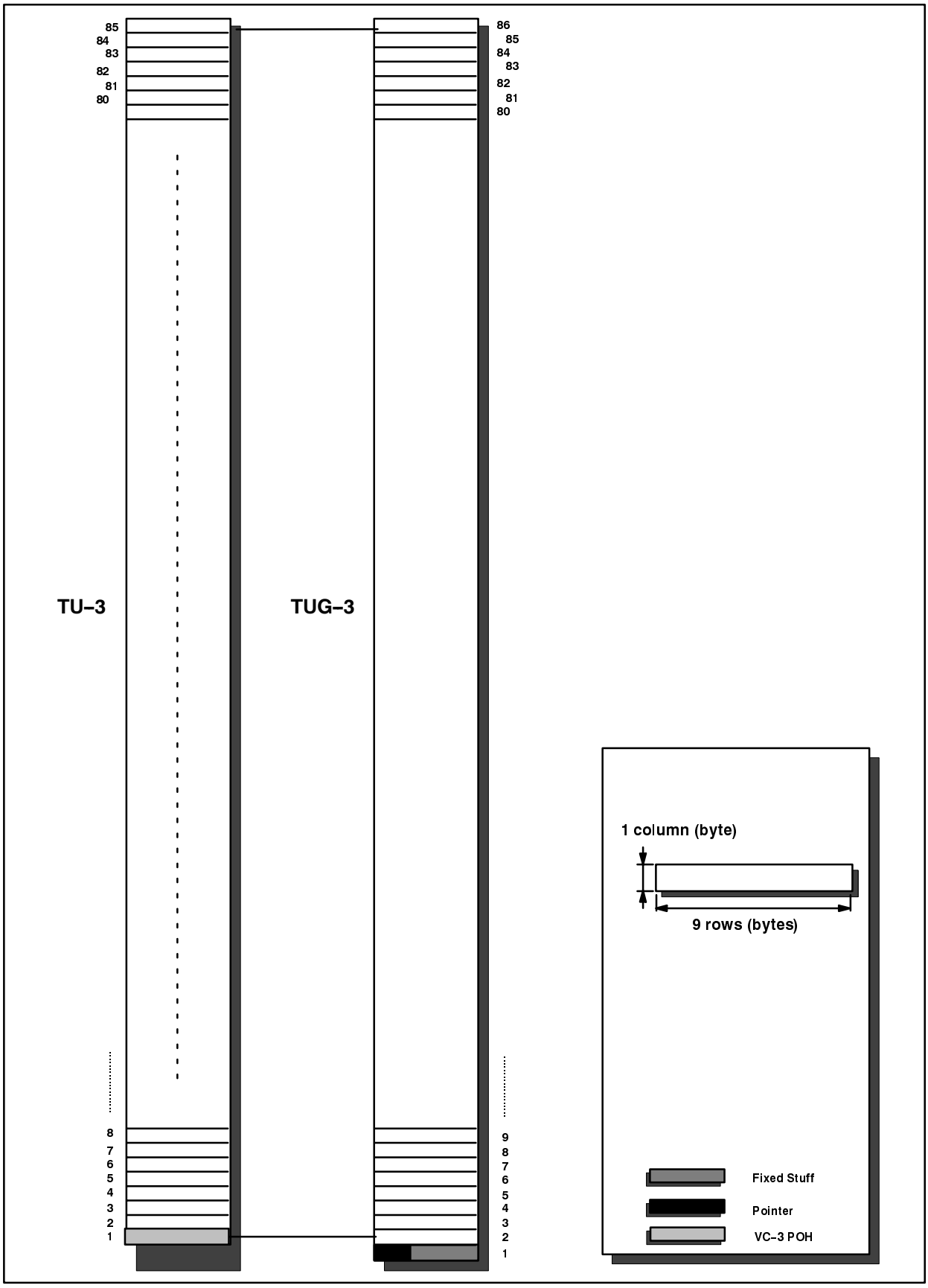


Fig. SH–29 *Multiplexing of TU–3 into TUG–3*

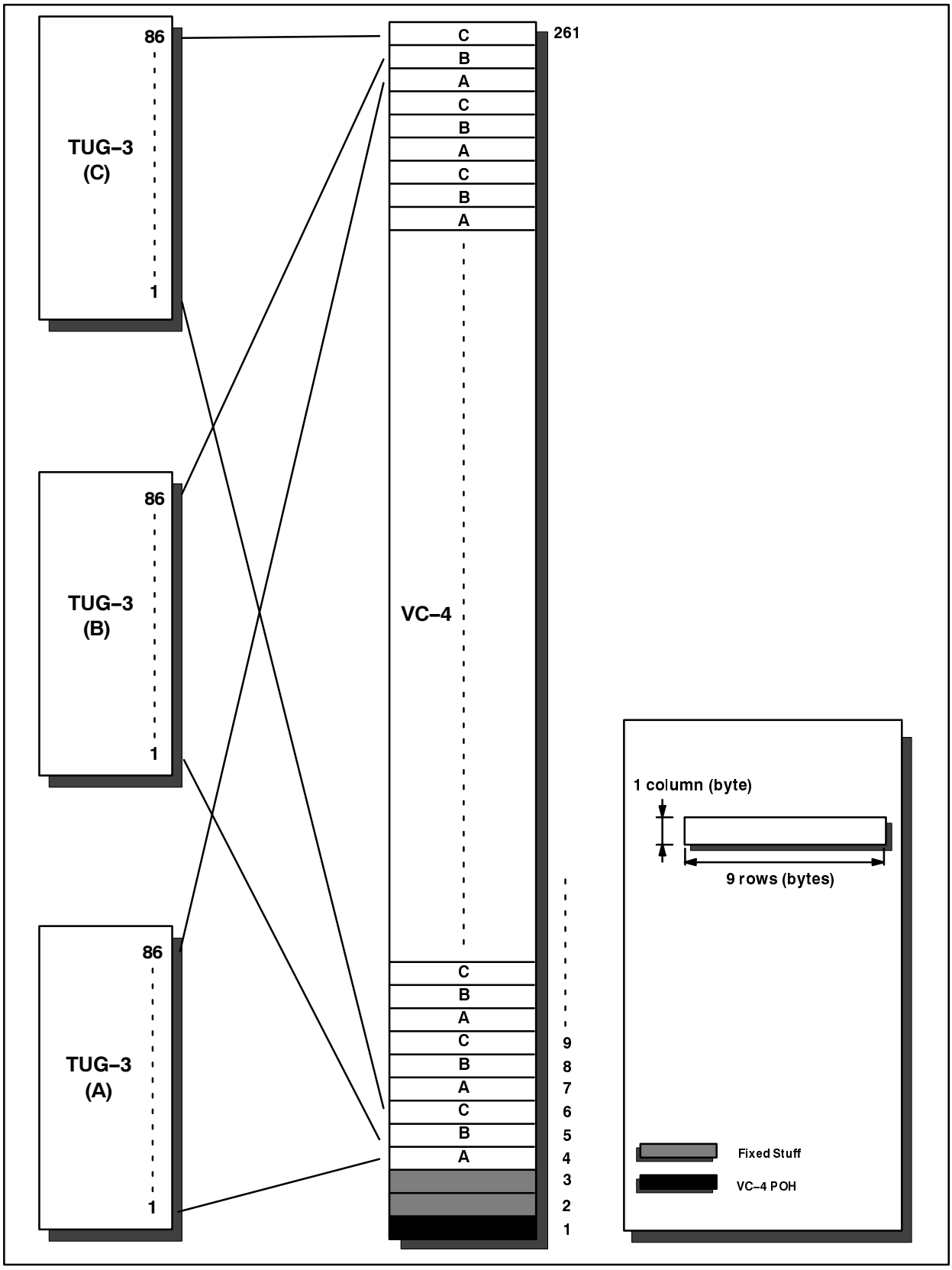


Fig. SH–30 *Multiplexing of 3 TUG–3 into VC–4*

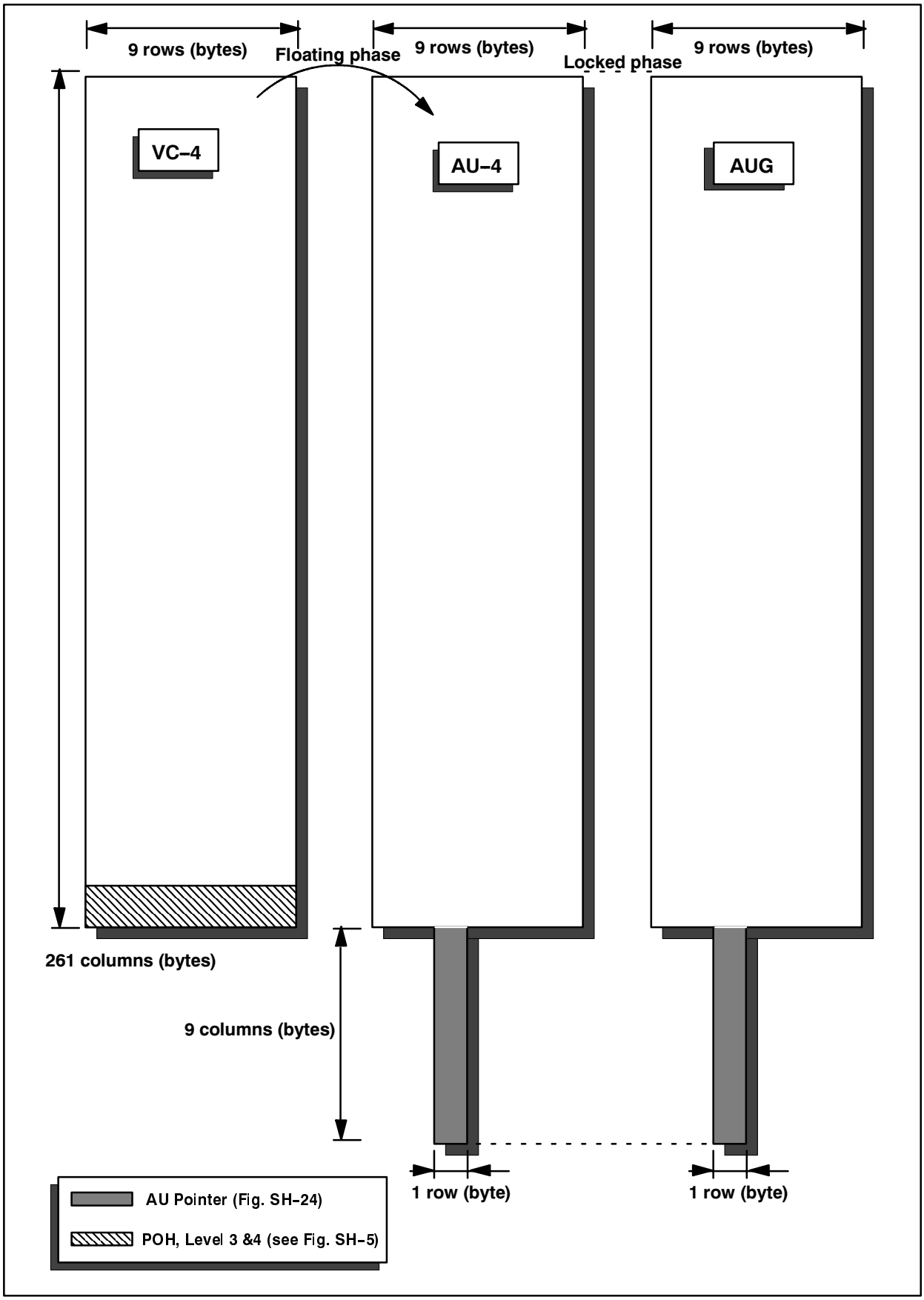


Fig. SH–31 *Multiplexing of AU4 into AUG*

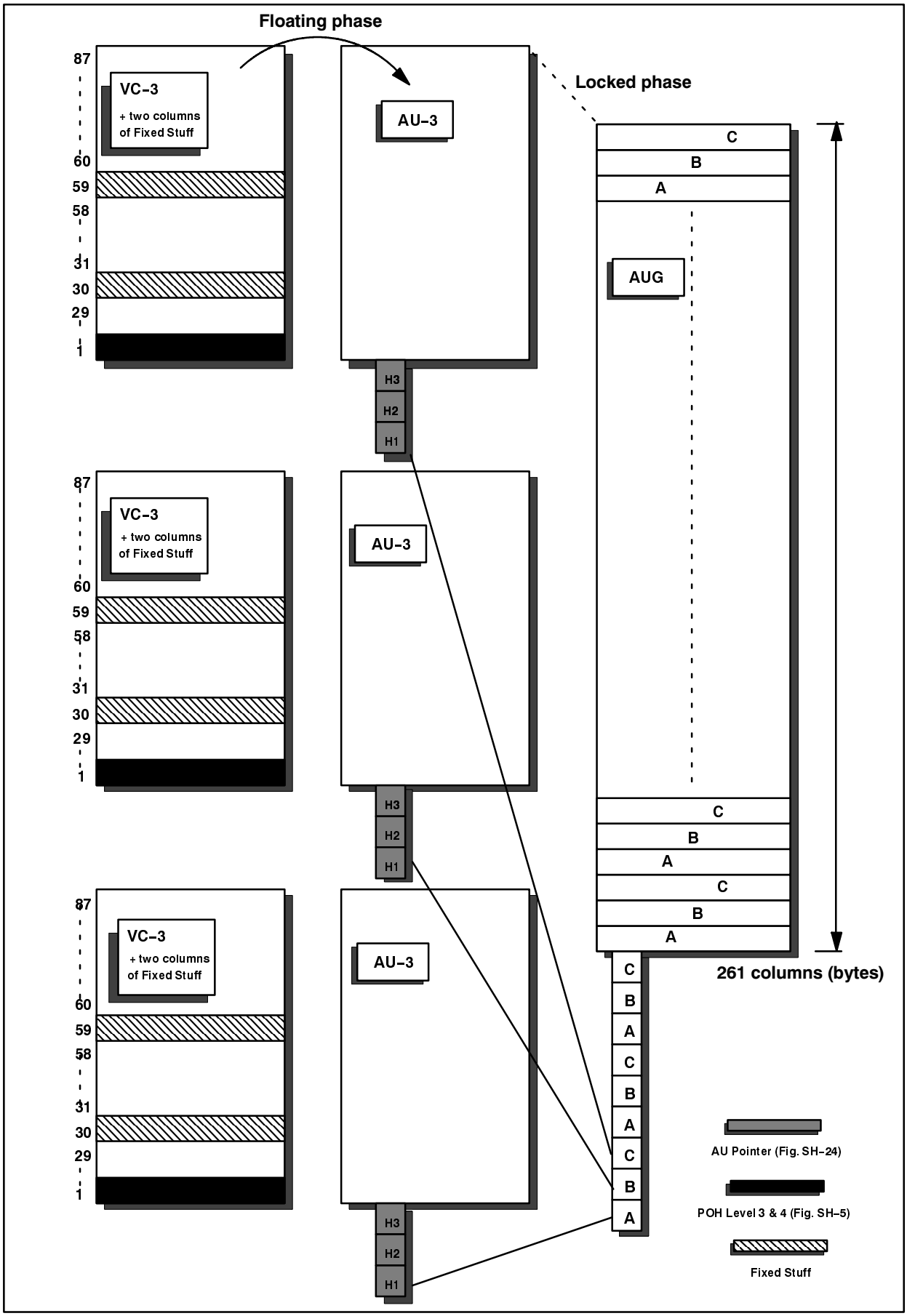


Fig. SH-32 *Multiplexing of 3 AU3 into AUG*

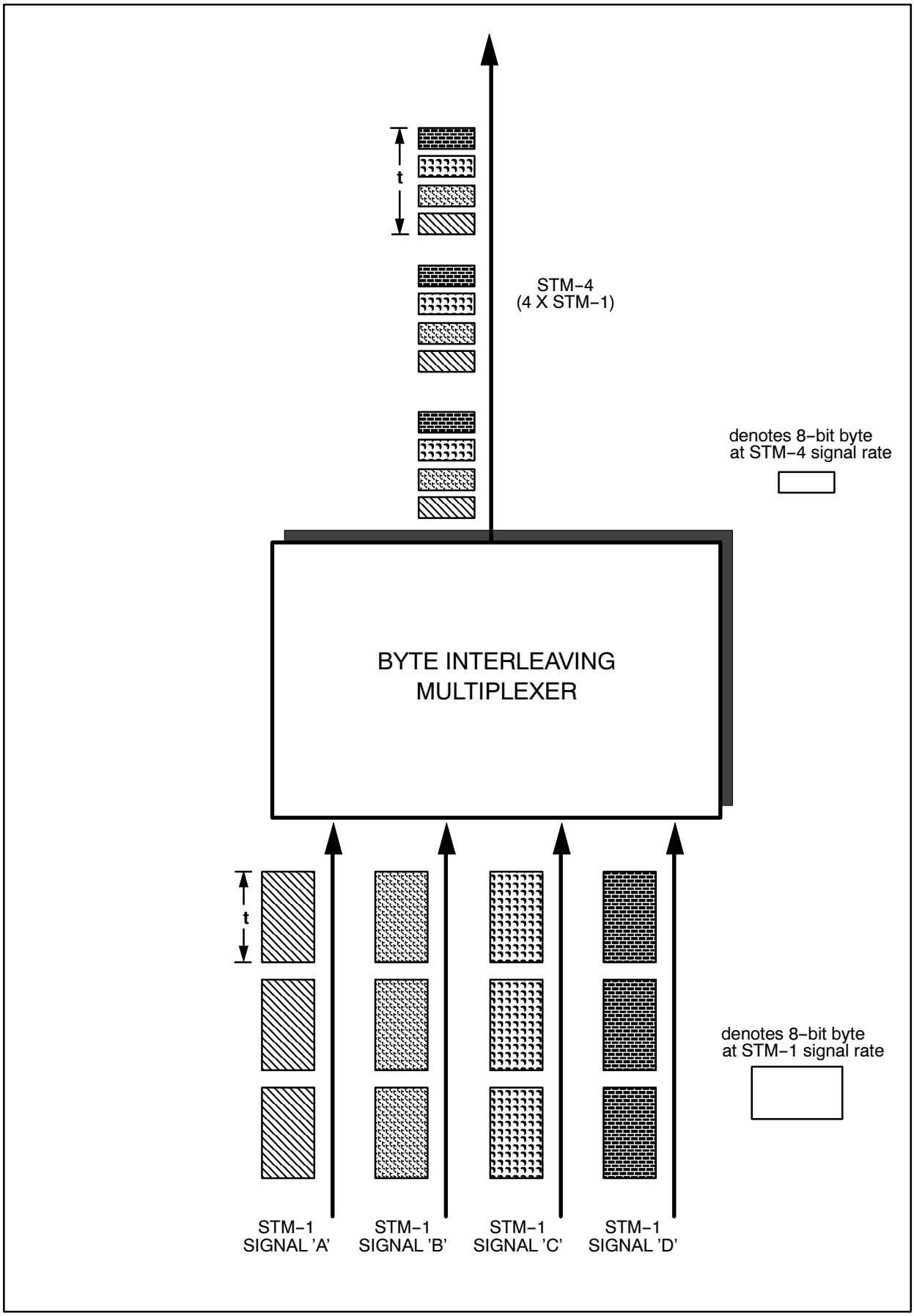


Fig. SH–33 *Synchronous byte–interleaved multiplexing*

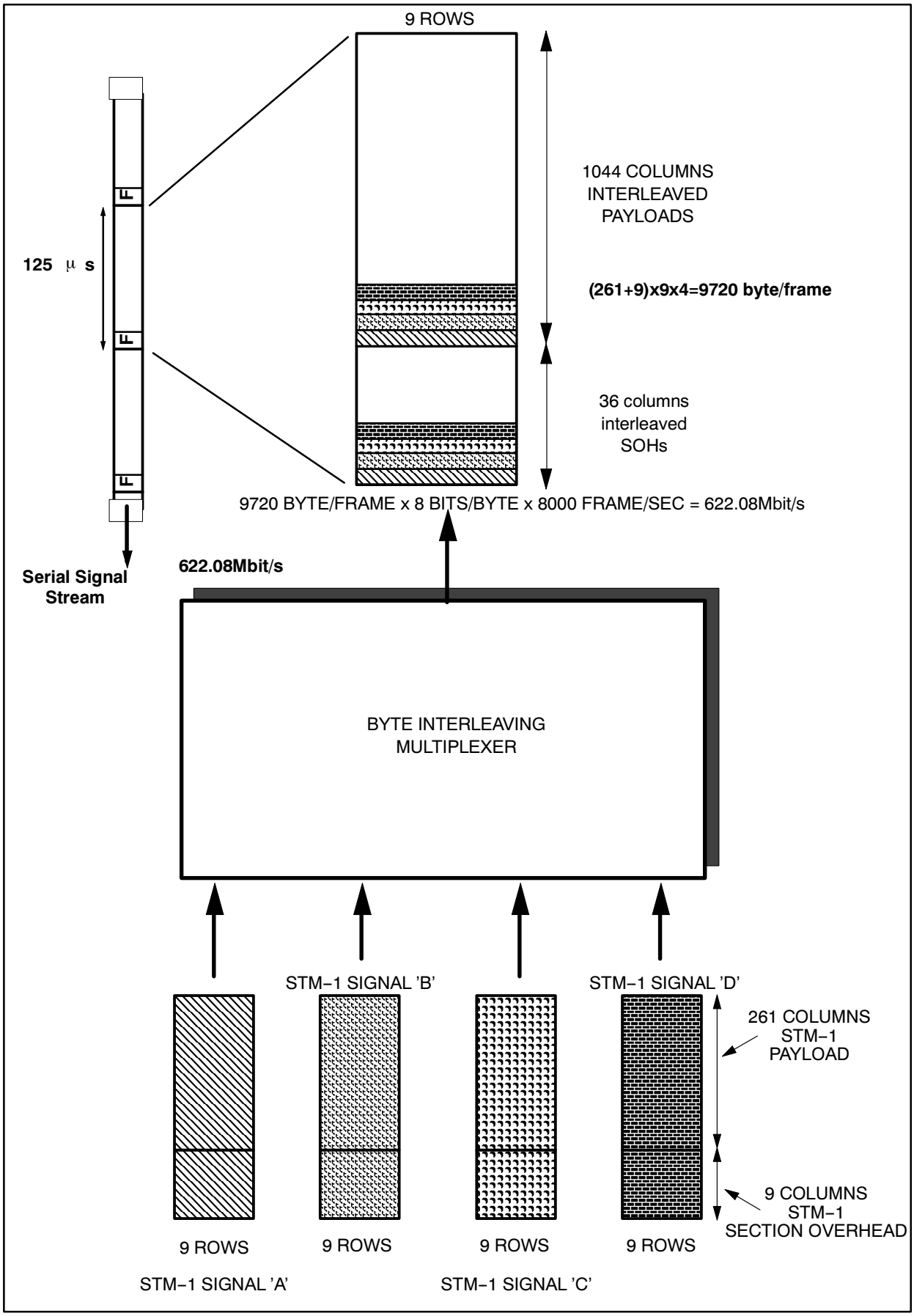


Fig. SH–34 *SDH STM–4 frame structure*

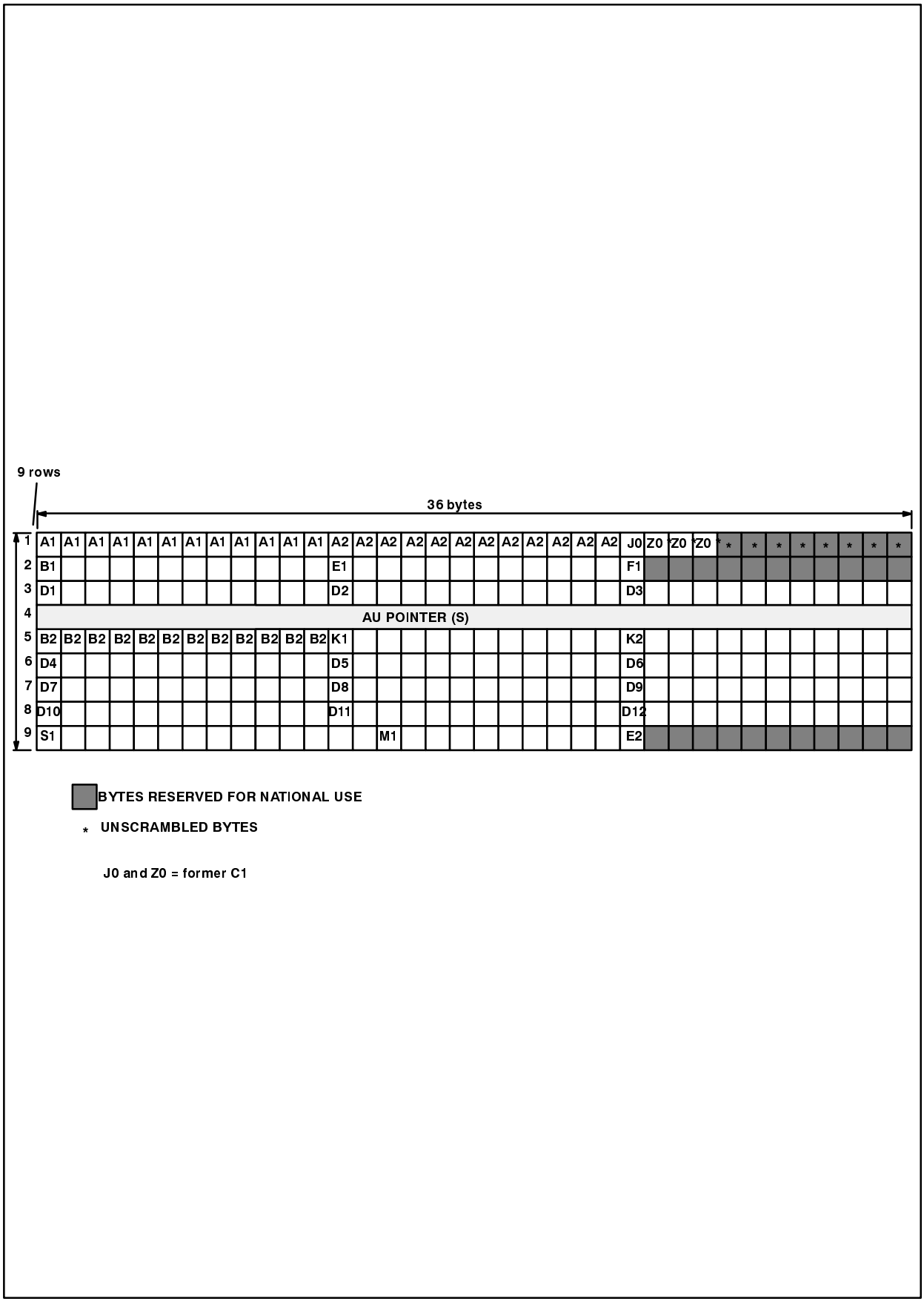


Fig. SH-35 *STM-4 Section Overhead layout*

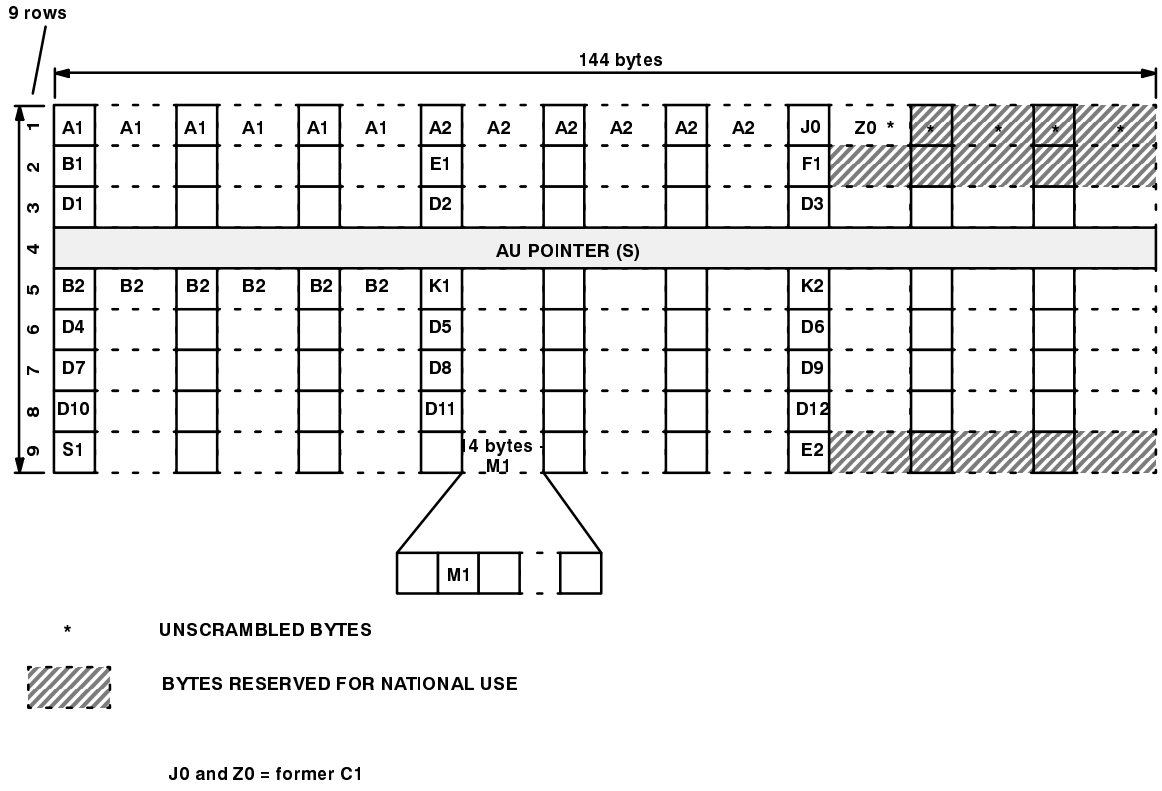


Fig. SH-36 *STM-16 Section Overhead layout*

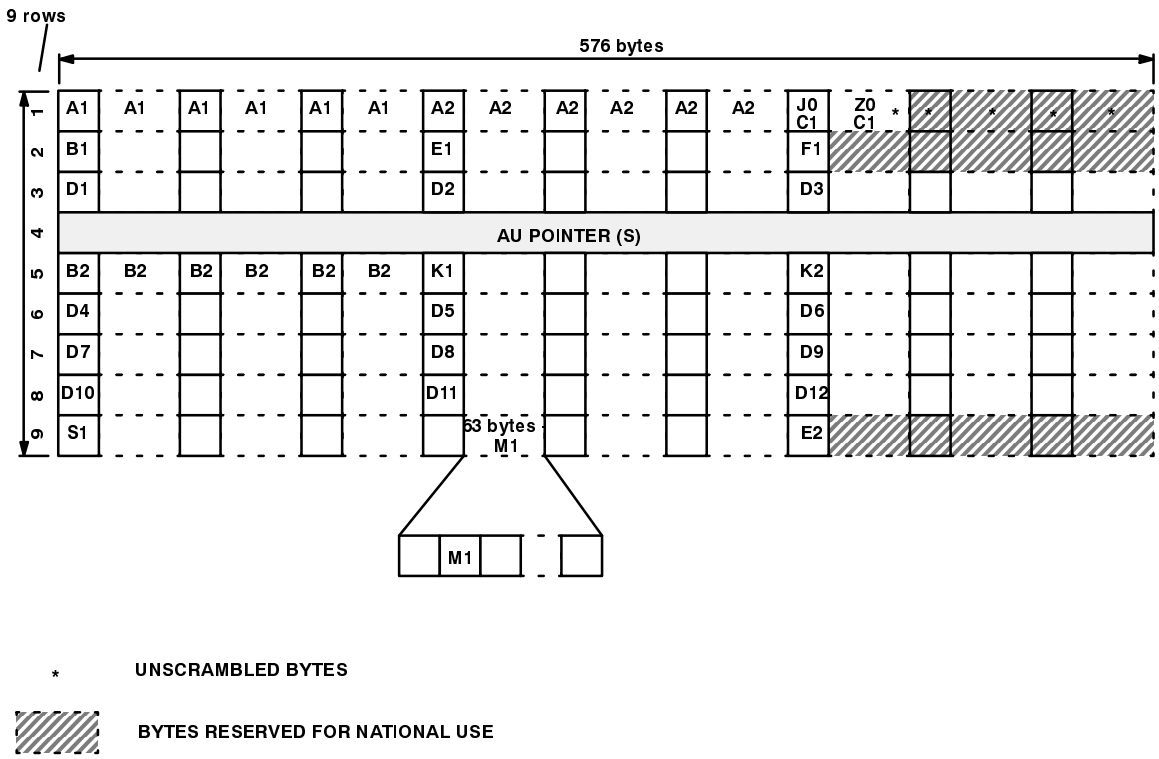


Fig. SH-37 *STM-64 Section Overhead layout*

SDH Equipment Block Diagram

With reference to ITU–T Recc. G.781, G.782, G.783 and G.784 the following describe the simplified flow of signals through a generic SDH equipment.

In Fig. SH–38 the block diagram of an SDH equipment is given.

Signal Flow: Multiplexing (G.703 input – STM–N output)

PDH signal is received by PPI block, which provides a G.703 interface and is mapped into an appropriate SDH container, by LPA block (also eventual re–justification takes place).

LPT block terminates the lower order path by generating and adding the VC POH to the relevant container. The flexible interconnection of the VC–1/2/3s is performed by LPC block.

In the case of an unused connection at the output of LPC block, LUG block generates a lower order VC with an undefined payload and a valid POH, including a signal label set to the value *unequipped*.

The HPA block performs the adaption of a lower order VC (VC–1/2/3) to an higher order one (VC–3/4) by adding the TU pointer, which indicates the phase of the first byte of VC–1/2/3 POH relative to the first byte of VC–3/4 POH, and assembling the complete VC–3/4. Then the HPT block terminates a higher order path, by generating and adding the appropriate VC POH to the relevant container.

The flexible interconnection of the VC–3/4s is performed by HPC block. If no valid higher order VC is available at the output of HPC block the HUG function generates a higher order VC with undefined payload and valid POH, including a signal label set to the value *unequipped.*

The AU–3/4 pointer is added by MSA block in order to indicate the phase of the VC–3/4 POH relative to the STM–N SOH. It is also up to this group to byte–multiplex the AU Groups (AUGs) and construct the complete STM–N frame.

For protection purposes the signal can be branched to another line system by MSP block.

The SOH is generated and added to the frame by MST and RST blocks. MST is responsible for rows from 5 to 9 and RST for rows from 1 to 3. RST block is also responsible for the STM–N signal scrambling.

SPI block converts the internal logic level STM–N signal into an STM–N interface signal (either optical or electrical).

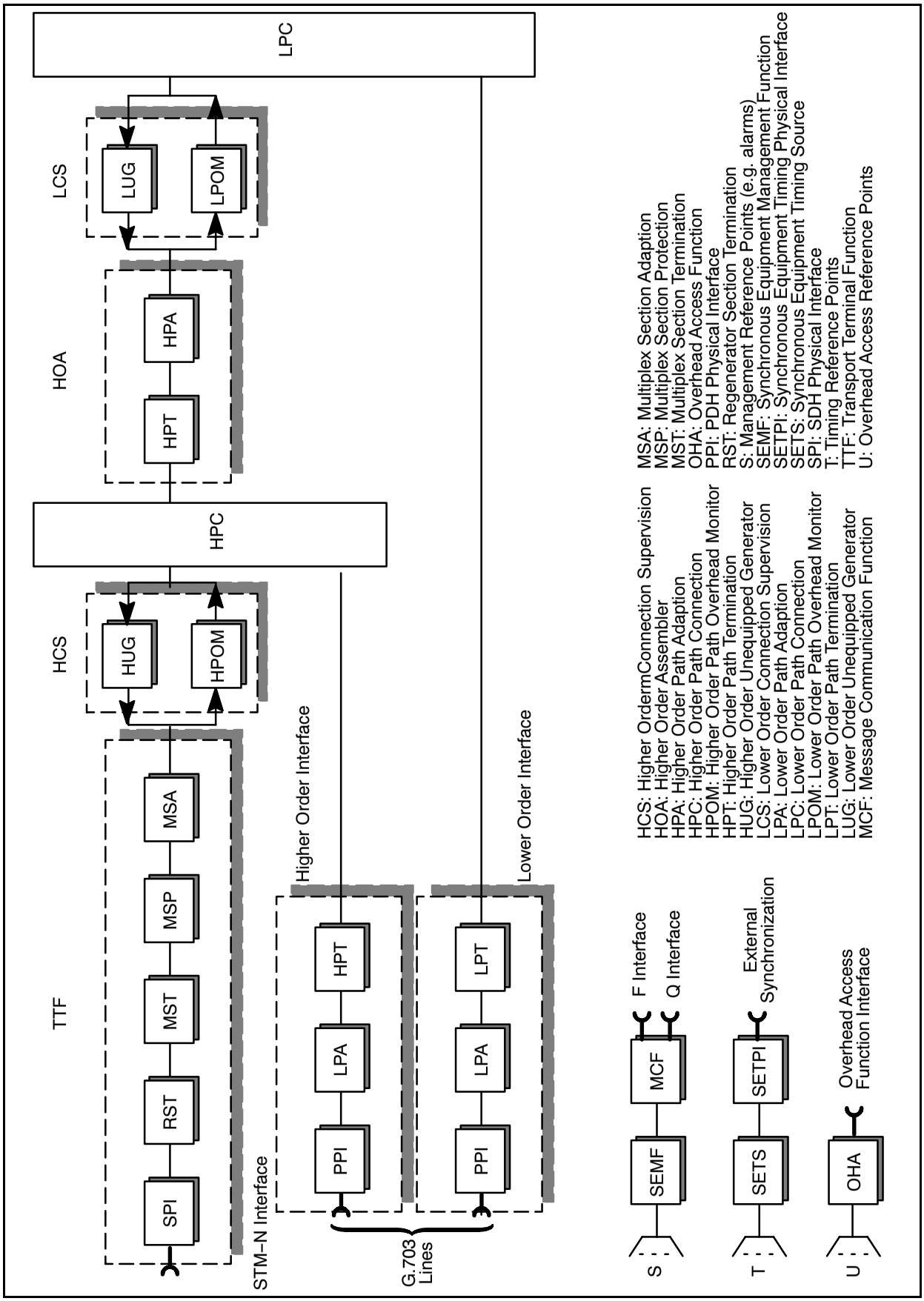


Fig. SH–38 *Block diagram of a generic SDH equipment*

Signal Flow: Demultiplexing (STM–N input – G.703 output)

The STM–N signal is received by SPI block, which converts the interface signal into an internal logic level. This block also recovers the clock from the line signal.

The RST block identifies the frame alignment word, descrambles the signal and processes rows from 1 to 3 of SOH. MST block processes rows from 4 to 9 of SOH.

MSP block is able to detect from which line (working one or protection one) the signal must be extracted. The processing of AU–3/4 pointer is made by MSA block, in order to detect the phase of VC–3/4 POH relative to STM–SOH. The VC–3/4 POH is monitored by HPOM block, without modifying it.

As in multiplexing the HPC block allows the flexible interconnection of the VC–3/4s whilst the HPT block extracts the VC–3/4 POH.

The HPA processes the TU pointer in order to detect the phase of the first byte of VC–1/2/3 POH relative to the first byte of VC–3/4 POH.

The VC–1/2/3 POH is monitored by LPOM block.

As in multiplexing the LPC block allows the flexible interconnection of the VC–1/2/3s.

The VC–1/2/3 POH is removed and read by LPT block. The LPA block must be provided with a buffer store and smoothing circuit to attenuate the clock jitter caused by the multiplex process, pointer moves and bit stuffing.

PPI block extracts the payload of the SDH container and converts it from the internal logic level to a G.703 signal.

Management Access

Performance data, implementation of specific alarms and other messages related to management functions, collected on different blocks, are converted into messages ready to be sent over the DCCs and a Q interface. This conversion is performed on SEMF block.

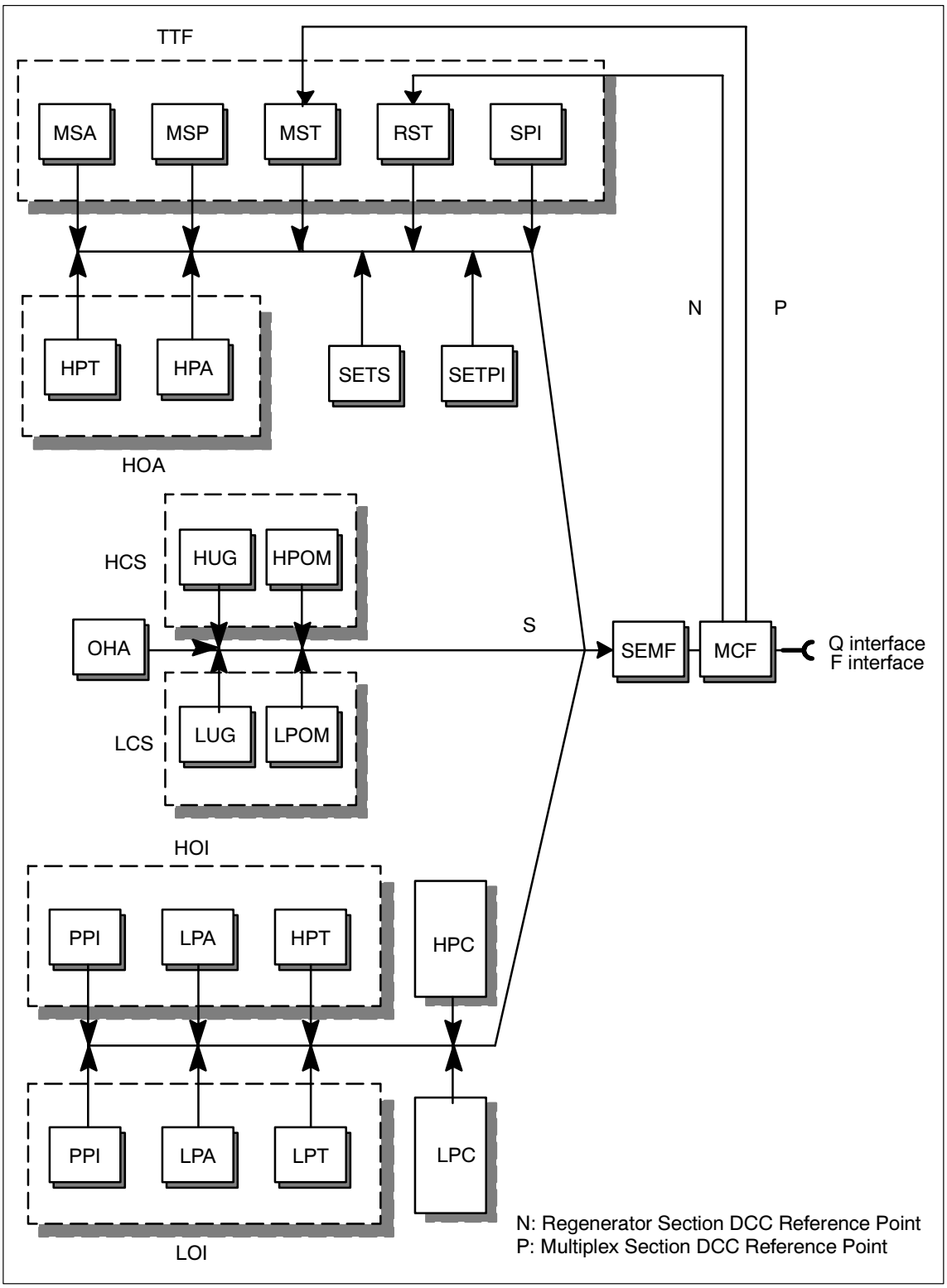


Fig. SH–39 *Management Access Block Diagram*

The MCF block sends the management messages on the Q interface (also F interface if a Local Controller is available) or on the DCCs.

Overhead Management

The OHA block gives access to the overhead bytes extracted from the STM–N frame. In Fig. SH–40 OHA block is shown with all the blocks from which overhead bytes are extracted.

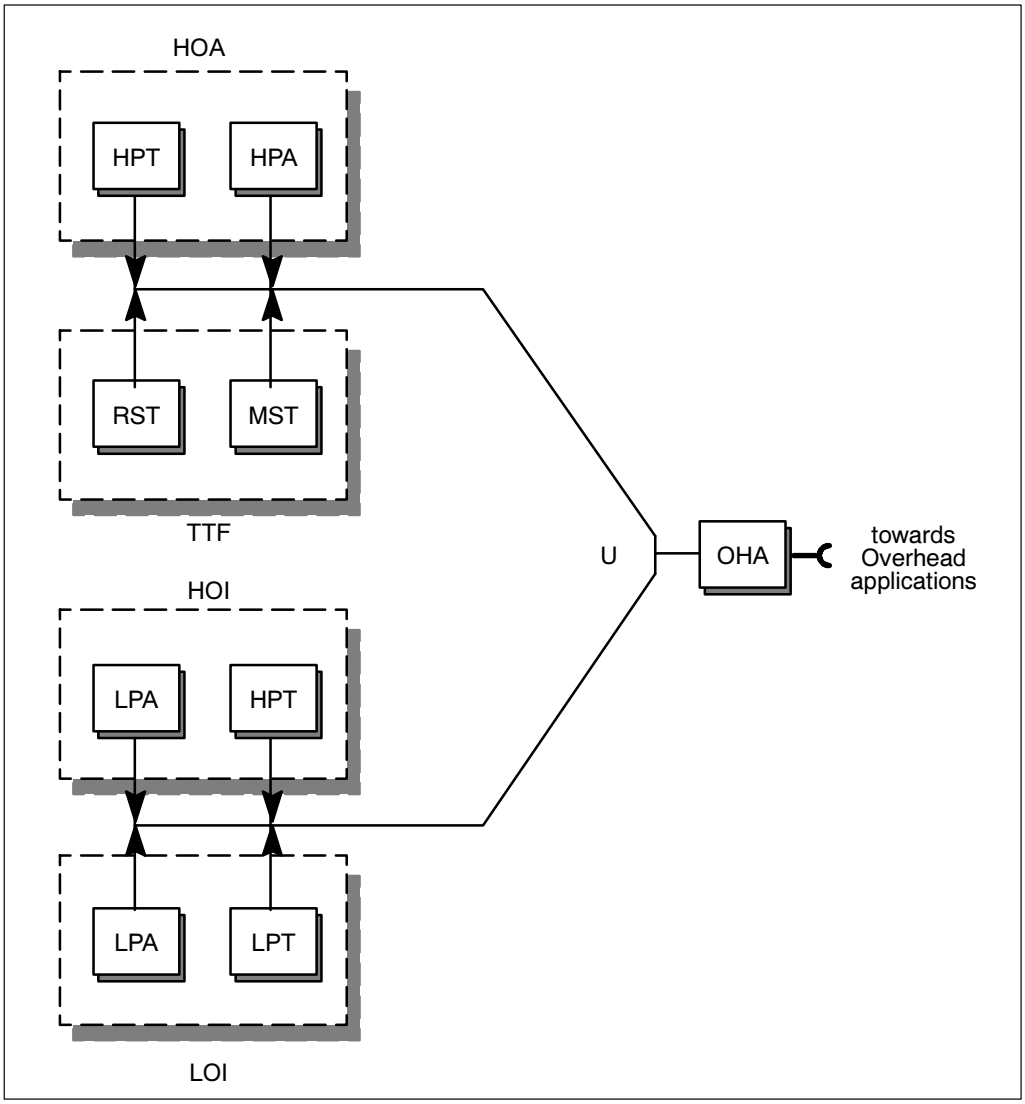


Fig. SH–40 *Overhead Bytes Access*

Timing

The SETS block provides timing reference to the relevant component parts of an SDH equipment. This timing reference is represented by the SDH network clock.

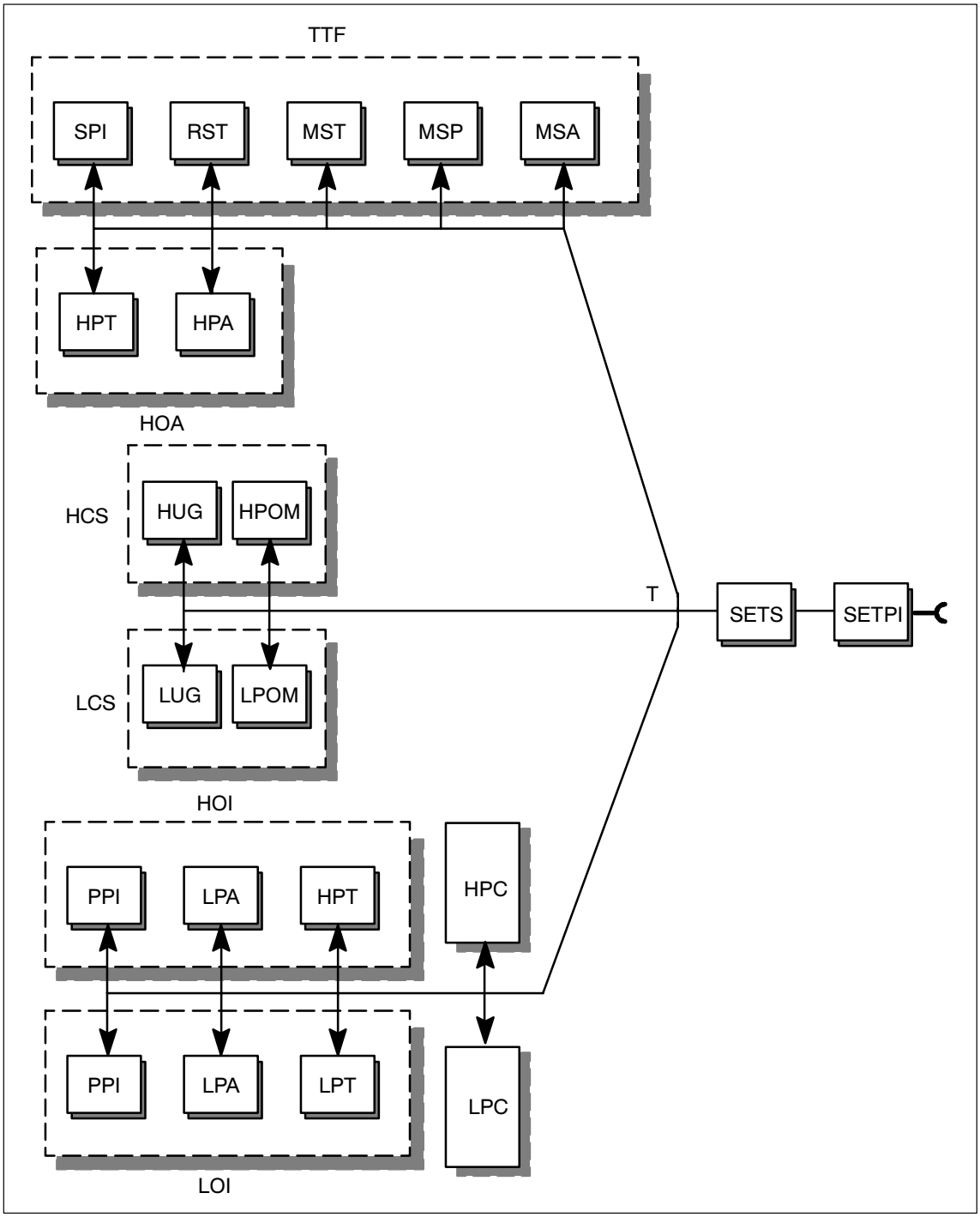


Fig. SH–41 *Management Access Block Diagram*

The SETPI block provides the interface between an external synchronization signal and the SETS block. It is also up to this block to provide an synchronization output signal for use by external equipment.