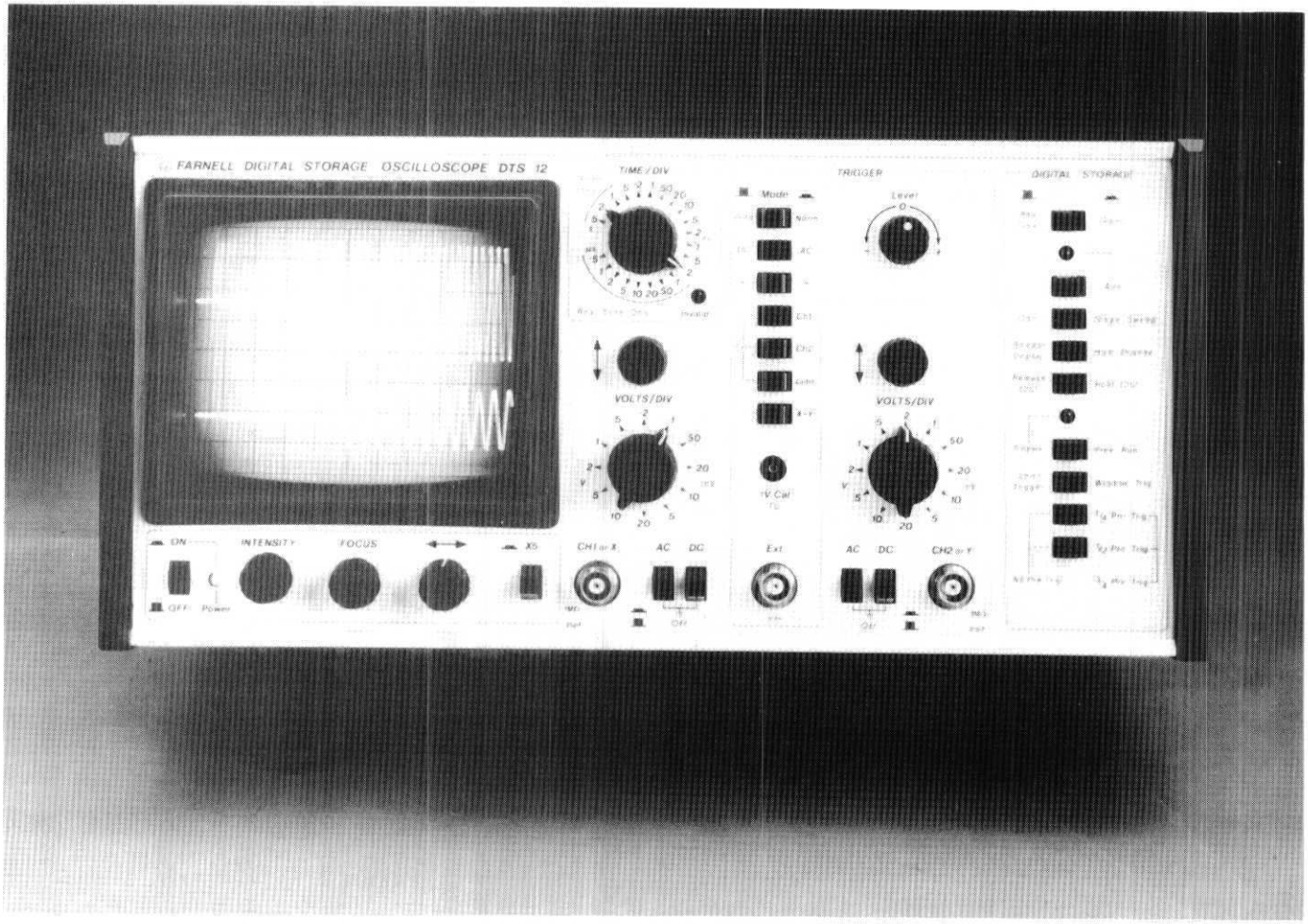
SCHEDULE OF EQUIPMENT

The instrument has been carefully packed to prevent damage in transit. When removing the unit from the packing box, be sure that all parts and accessories are removed from the packing material.

The complete equipment comprises:-

1 off DTS12 or DTS12P or DTS12T as ordered.
1 off mains lead
1 off instruction book

Note:- In the event of damage in transit or shortage in delivery, separate notices in writing should be given to both the carriers and Farnell Instruments Ltd., within three days of receipt of the goods, followed by a complete claim within five days. All goods which are the subject of any claim for damage in transit or missing items should be preserved intact as delivered, for a period of seven days after making the claim, pending inspection instructions from Farnell Instruments Ltd., or an agent of this Company.



The Farnell DTS12 Digital Storage Oscilloscope

INTRODUCTION

The Farnell DTS12 Digital Storage Oscilloscope is in fact two oscilloscopes in one - a real time 12MHz dual trace oscilloscope and a DSO with a maximum sample rate of 500kHz, or 250kHz in dual channel operation. The DTS12 has been designed with simplicity of use in mind, it's easily understood controls make the change from normal oscilloscope to DSO as simple as possible. The dual trace display is available in chopped or alternate modes in normal operation, the most appropriate mode being selected automatically by the timebase switch. A times five expansion facility in the horizontal axis is provided in both modes of operation so that more detailed examination of waveforms may be made.

Triggering is positive in action and works in the same manner for either mode of operation, but with the added benefits of a window trigger for detecting transients of unforseen polarity and a single sweep facility for use in digital storage mode.

Also provided in storage mode is the ability to see the waveform occurring immediately prior to the trigger event. This is possible as a result of a 'free wheeling' store which is being continuously updated, whether or not a trigger is present. By selection of one of the Pre-trigger modes offered, a proportion of what is already in this store is 'frozen' once a trigger is received and the ensuing input is written only into the remainder of the memory.

The DTS12 is compact and simple to operate. It incorporates many excellent features which should make your acquisition an invaluable addition to your laboratory.

SPECIFICATION

Real-time operation

Vertical deflection

Two identical input channels

BANDWIDTH	D.C. coupled: D.C.-12MHz (-3dB @ 4 div deflection) A.C. coupled: 2Hz-12MHz (-3dB @ 4 div deflection)
RISE TIME	<29ns at 4 div deflection
SENSITIVITY	5mV/div to 10V/div in 11 calibrated ranges (1-2-5 sequence).
ACCURACY	±3%
INPUT IMPEDANCE	1M ohms & 30pF nominal in parallel.
COUPLING	A.C. or D.C. with provision for grounding the input to the attenuator or turning the channel off.
MAX INPUT VOLTAGE	400V D.C. + A.C. peak

Display modes

SINGLE TRACE	Channel 1 or Channel 2 only. OFF position for unused channel on AC-DC-GND switches. Chopped or alternate. Automatically selected by timebase switch. Nominal chop frequency 100kHz. Alternate above 1ms/div.
X-Y	Channel 1 is used to provide X-deflection with same calibrated sensitivity as for Y operation, D.C. or A.C. coupled. Bandwidth is D.C. to 800kHz. Phase difference between X and Y channels is 10° max. at 100kHz. (Note - not available in storage mode).

Horizontal deflection

MODE	Either internal timebase or with CH1 providing X deflection in X-Y mode selected on timebase switch.
TIMEBASE:	
SWEEP SPEEDS	0.5us/div in 19 calibrated ranges (1-2-5 sequences). Use of x 5 expansion extends fastest sweep to 100ns/div.
EXPANSION	X5 magnifier operated by push switch near X-shift control. Affects timebase only-inoperative in X-Y mode.

ACCURACY	±3% all speeds, except 0.5us/div @ ±5% ±5% on all speeds in x 5 expanded mode.
Triggering	
SOURCE	Channel 1, Channel 2, External, or Line
NORMAL MODE	Sweep triggering only when signal is present.
AUTO MODE	Sweep free runs in absence of suitable signal, with signal triggering the same as Normal mode.
SLOPE	Triggering from positive or negative going signals may be selected by +/- switch.
COUPLING	A.C. or D.C.
LEVEL	Variable trigger level control with adjustment over full 8cm equivalent deflection.
SENSITIVITY	Internal <0.5 div 40Hz to 2MHz (from D.C. when D.C. selected) <2 div 8Hz to 40Hz & 2MHz to 15MHz External <1V 40Hz to 0.1MHz <5V 8Hz to 40Hzs & 0.1MHz to 15MHz.

EXTERNAL	Separate front-panel input, impedance >100k ohms in parallel with 30pF.
LINE	Provides triggering from mains supply frequency (e.g. 50Hz).
CALIBRATOR	Front panel socket (2mm) provides 1V ±2% pk-pk square wave at a nominal 1kHz. This may be used for probe compensation or to check Y amplifier gain.
Z MODULATION/BLANKING	Rear panel 4mm socket. An input pulse of +5V blanks the trace. This facility is A.C. coupled.
TRACE ROTATE	Adjustment by rear panel screwdriver operated control.
ASTIGMATISM	Adjustment by rear panel operated control.

General

C.R.T.	5 in. diagonal rectangular faced tube with integral graticule 8 x 10 div with 5 sub-divisions along central axes. Mono-accelerator working at 2kV. Medium persistence P31 phosphor.
POWER SUPPLY	100, 120, 220, 240V a.c. inputs ±10% by voltage selector plate. 50-60Hz. Power consumption 65VA (DTS12). 69VA (DTS12T). Stabilised against power line variation ±10%.
FUSE RATINGS	190-260V. 500mA anti-surge. 95-130V inputs. 1A anti-surge.
TEMPERATURE	Ambient temperature operating range 0 to 45°C. Specification valid for operation in range 15 to 35°C.
OPTIONS (TO ORDER)	Probe kit with X1, GND, X10 positions, full spec. on request. Rack mounting kit. Soft carrying case for protection in transit.
ACCESSORIES (SUPPLIED)	Handbook
DIMENSIONS	340mm wide 170mm high 340mm deep 8.5kg.

DSO SECTION

DISPLAY MODES	CH1 only, CH2 only. CH1 and CH2 dual trace. Hold CH2 and update CH1 for comparison (In dual trace mode, channels are scanned alternately).
REFRESHED	Depending on the triggered/free run switch setting, the display is continuously updated, displaying the input waveform via the digital store.
SINGLE	Freezes store at the end of a triggered sweep.
HOLD DISPLAY	When depressed, freezes the information in full store after completing its sweep. In dual channel mode, it freezes both channels.
HOLD CH2	When depressed, freezes the alternate samples in dual channel mode. Locks CH2 information into store for update on CH1 for comparison.
TRIGGERED	Displays the input waveform triggered at a certain level, selected by the trigger controls.
FREE RUN	The store is continuously updated at a rate selected by the timebase switch.

PRE-TRIGGER	Displays historic information prior to the trigger pulse. Selectable for $^1/_4$, $^1/_2$ and $^3/_4$ of full store.
LINEAR INTERPOLATOR	A linear interpolator (dot joiner) circuit ensures that the display is a smooth continuous waveform.
STORE SIZE	1024 x 8 bits
VERTICAL RESOLUTION	256 steps over 8 divisions. Approximately 30 steps/cm.
HORIZONTAL RESOLUTION	Single trace, 1024 samples for a complete scan (approx. 100 samples/cm. With X5 expansion 20 samples/cm). Dual trace 512 samples for a complete scan, (50 samples/cm. With X5 expansion 10 samples/cm). In dual trace mode the input channels are sampled alternately but the resultant stored waveforms are displayed on sequential scans.
MAXIMUM SAMPLE RATE	0.5MHz sample/sec. (2us/sample) at 0.2ms per cm timebase setting. Maximum event speed 100kHz (single trace). 50kHz (dual trace)
WRITING SPEED	Selected from 0.2ms/div to 5s/div in 1-2-5 sequence.
READOUT SPEED	Constant speed of one full scan every 2ms

TRIGGER FACILITIES IN STORAGE MODE

SOURCE	CH1, CH2 or external
NORMAL MODE	Sweep triggering only when signal is present.
SLOPE	Triggering from positive or negative going signals may be selected by Positive/Negative switch.
COUPLING	D.C. or A.C.
LEVEL	Variable trigger level control with adjustment over full 8 divisions equivalent deflection.
SENSITIVITY	Internal A.C. and D.C. <0.5 div (above 40Hz A.C.) External A.C. only 1V p-p above 40Hz.
LINE	Triggers on mains power supply frequency. Trigger position varied by means of Level control and the Slope pos/neg switch.
WINDOW TRIGGER	Triggers when signal deviates by more than 1 div (±20%) above or below the trigger level setting.

NOTE: ADDITIONAL INFORMATION FOR THE DTS12P (X-Y PLOTTER OUTPUT) AND DTS12T (IEEE488 AND BBC MODEL B INTERFACE) IS CONTAINED IN SECTIONS 9 AND 10 RESPECTIVELY.

INSTALLATION

The voltage to which the unit is set prior to despatch is printed on the rear of the unit. Check that this voltage corresponds to the available a.c. supply.

To alter the mains input setting (to 100, 120 or 220V from 240V for example) remove the power cord connector from the rear panel socket and slide the perspex window, covering the mains fuse, to one side. This will reveal the present voltage setting. The selector plate may be removed and reinserted in alternative positions to match the available a.c. supply.

The three core mains lead must be connected as follows:-

Brown	-	Mains live
Blue	-	Mains neutral
Green/yellow	-	Earth (ground)

Always check the value of the mains fuse if the mains tapping has been altered - see specification.

DETAILED DESCRIPTION OF CONTROLS

a. **ON/OFF**

This push button when depressed permits the instrument to be powered up indicated by illumination of the adjacent green led.

b. **Intensity**

This varies the brightness of the trace. **NOTE:** Excessive intensity can shorten the life of the tube.

c. **Focus**

This varies the fineness of the trace. **NOTE:** It is normal for the trace to defocus at excessive intensity.

d. **Astigmatism (rear panel)**

This control is best adjusted in conjunction with the focus control while viewing a sinewave to give best fineness of trace in both the X and Y directions.

e. **Trace rotate (rear panel)**

This control aligns the horizontal trace with the graticule lines. When viewing the timebase line with the input to a channel grounded, the timebase line should be shifted by the channel Y shift control to screen centre, and adjusted to be parallel with the horizontal graticule lines,

by the trace rotate control.

f. **(X-shift)**

Rotation of the X-shift control moves the spot or trace left or right in the X direction. Operation of the control has sufficient effect to deflect trace off the screen completely so if the trace is lost, operation of this control may be necessary to recover the display. The X shift control has equal effect on both Y channel displays.

g. **X5**

The X5 multiplier is operated by depressing the X5 push button. This effectively increases the length of the timebase scan by five times, with only 10 div. of the scan being viewable at any one instant, operation of the X shift allowing the rest of the trace to be examined. The X5 multiplier is not operative in the X-Y mode.

h. **Input mode selector buttons - identical operation on each channel.**

These provide four separate possibilities according to which buttons are depressed.

AC - The input to the channel is capacitively coupled, blocking d.c. up to 400V and giving a bottom end frequency response down to 2Hz.

DC - The input is directly coupled to the amplifier allowing d.c. levels to be displayed as well as a.c. signals.

GND (both buttons in) - The input to the amplifier of the channel concerned is disconnected from the input socket and is connected to signal

ground. The input signal is not shorted to ground but left open-circuit. OFF (both buttons out) - The channel is turned off and only the other channel is displayed. It is still possible however to trigger from a signal input to a channel which is turned off. This facility may be particularly useful where it is desired to measure time delays between infrequently occurring events in different parts of a circuit viewed on each channel. The alternate beam switching may then cause the second event to be missed, but using CH1 as reference to trigger the timebase while turned off will ensure that the second event coupled to CH2 will not be missed. It is an invalid mode to have both CH1 and CH2 switched off.

i. **Y channel attenuator switches**

These switches adjust the input sensitivity of the Y channels. If a square wave of amplitude 1V pk-pk is coupled directly to channel 1 input with d.c. selected and the attenuator switch set to 1V/div. then the waveform displayed will be 1 div high. If the attenuator is set at 0.2V/div. then the displayed waveforms will be 5 div high. By using the range switch position in combination with the internal graticule, which has minor divisions marked on the X and Y axes every 0.2 div., the peak to peak voltage of any waveform can be determined. For example: a waveform measuring 4.8 div. in amplitude with the attenuator set to the 0.5V/div. range has peak to peak voltage of 2.4V

j. **Y-shift**

These controls move the trace for the respective channel in a vertical (Y) direction. It is possible to move the trace right off the screen in

either direction. This can be used to observe a.c. components on top of larger d.c. offsets whilst still d.c. coupled. The Y shift on channel 1 is rendered inoperative in the X-Y mode. The X shift can be used as normal.

k. **Time/div switch**

This switch allows selection of a choice of 19 different sweep speeds from 0.5us/div. to 5s/div (without the X5 expansion). This allows the time between events to be measured along the X axis of the internal graticule in the same way voltage was determined on the Y scale (see i above). The three slowest speeds 1s/div to 5s/div. are not available for use in real-time mode. If these positions are selected inadvertently, the red invalid lamp will light indicating erroneous operation, however no damage results from such selection. The frequency of repetitive waveforms can be measured in one of two ways. 1) If the distance between two identical portions of successive waveforms is measured, e.g. from one positive peak to the next, as say 2.5 div on the 50us/div. range, the length represents 2.5 x 50 = 125us, the reciprocal of which gives a frequency of 8kHz. 2) A simpler, but more approximate method is to set the timebase range to one of the decimals of unity e.g. 1, 1ms/div. etc and simply count the number of complete waveforms displayed across the screen, divide by ten and multiply by the reciprocal of the timebase range.

1. Trigger mode switches (all active in storage mode except X-Y/and Auto)

These switches control the various ways in which the timebase can be triggered. The legends printed in red indicate the function selected with the button out, and those in black the function with the button in.

(i) Auto/Norm

In the 'Norm' (in) position a timebase sweep will only be initiated if there is a signal present to trigger it, and only then if the correct input has been selected and the level control adjusted correctly (see m). In 'Auto' if a suitable trigger is not received within approx. 0.1s from the end of the last sweep then a sweep is automatically initiated. If no trigger signal is present then the displayed signal will not lock. So long as a suitable signal is applied which triggers the timebase, then sweeps will be triggered as in the 'Norm' mode. The only exception here is with infrequently repetitive signals of less than approx. 10 per second, in this case it is essential to use 'Norm' mode to obtain a locked display

(ii) DC/AC

For most input signals 'AC' (in) should be selected. This a.c. couples the signal to the trigger circuit. With the button out the signal is d.c. coupled to the trigger circuit. The action of this is for triggering to take place at a particular vertical level on the screen, adjustable by the trigger level control. A trace will be triggered whenever the signal level from the selected trigger source, including the effect of the Y

position controls, crosses the trigger level set in the direction given by the setting of the +/- switch.

(iii) '+/-'

With 'AC' and '+' (button out) selected, sweeps will be triggered by positive going (rising) edges. By selected 'AC' mode and '-' (button in) negative going edges trigger the sweep. In DC mode the action is similar - see paragraph above for description.

(iv) CH1

When 'CH1' trigger button is depressed the signal applied to channel 1 is routed to the trigger circuit - even if its Y channel is 'off'.

(v) CH2

When 'CH2' trigger button is depressed the signal applied to channel 2 is routed to the trigger circuit - even if its Y channel is 'off'.

(vi) Line

Depressing this button allows the trace(s) to be triggered from the mains power supply frequency waveform, to which the trigger circuit is coupled in this position via the mains transformer.

(vii) Ext

Selected when both 'CH1', 'CH2' and Line buttons are out together. This then routes a signal applied to the 'Ext. Trigger' socket to the trigger circuit.

X-Y

In the X-Y position the timebase is disabled and the output from the channel 1 Y amplifier is switched through to the X amplifier, maintaining the same deflection sensitivity in terms of volts per div., but at a reduced bandwidth. The CH2 Y amplifier is automatically switched through to the Y amplifier. In this way the oscilloscope may be used to generate X-Y displays.

NOTE: The CH1 Y shift control becomes inoperative in X-Y mode, and the X shift control should be used as normal.

m. **Trigger level**

This control is used in conjunction with the mode switches, particularly the '+/-' switch and it determines the point on the waveform from which a sweep is initiated. Adjustment of this control will move the point from which the waveform starts up or down the rising or falling edge (dependent upon selection of +/-). For waveforms which do not occupy the full height of the screen it is possible to adjust the trigger point beyond the amplitude of the waveform either positively or negatively, in which case synchronism will be lost. Readjustment of the control should enable lock to be restored. Note: As there is no signal delay line in this

oscilloscope, a delay between the signal initiating the trigger and the observed start of the trace causes an apparent shift in the trigger point at the fastest timebase speeds. This delay is approximately 160ns.

n. **1V Cal.**

This socket provides a square wave output at a frequency of approximately 1kHz and an amplitude of 1V pk-pk from a source resistance of approximately 2k ohms. The purpose of this output is to aid the correct adjustment of the high frequency compensation in dividing type oscilloscope probes.

DESCRIPTION OF STORAGE CONTROLS

1. Real Time/Store

When 'Real Time' operation is selected, the oscilloscope behaves as a normal oscilloscope without storage facilities, and the other buttons in the right hand column are rendered inoperative. When store is selected, the screen displays the contents of the storage memory, and the way in which this memory content is updated depends upon the settings of the other buttons in this column.

2. Arm & Arm Light

This button is used when 'Single Sweep' operation is selected to set the trigger circuit such that the next time a valid sweep is initiated and the memory contents are updated. When the trigger circuit has been armed the Arm lamp lights, and when the write sweep is completed, it is extinguished.

3. Cont/Single Sweep

When a continuous mode is selected, the write sweep is initiated again every time a valid trigger is received after the completion of the previous write sweep. If 'Free Run' is selected, a new sweep is initiated after the completion of each previous one. 'Single Sweep' mode permits only one sweep to take place after the timebase circuit has been armed by the Arm button. Further sweeps can only be initiated by further operation of the Arm button.

4. **Release Display/Hold Display**

When 'Hold Display' is selected, the current write sweep will be completed if one was already initiated, and then the display will be 'frozen'. No further writing to memory can take place. Releasing this button again allows the display to be updated in the ways described.

5. **Release CH2/Hold CH2**

This button operates in the same way as the one above, except that only CH2 is 'frozen'. CH1 may still be updated allowing comparisons to be made between incoming waveforms on CH1 and a waveform stored. When doing comparisons, care should be taken to note that if the timebase position or CH2 attenuator setting is altered, this will have no effect on the stored display which may lead to false comparisons being made. Note also that this control has no effect when CH2 single channel operation is selected. To hold the display in this situation, the 'Hold Display' button should be used.

6. **Trigger/Free Run**

When 'Trigger' is selected, updating of the memory is only initiated if a valid triggering signal is detected at the trigger source selected CH1, CH2, Ext. or Line (50Hz). Pressing 'Free Run' causes new sweeps to be initiated at the termination of each previous sweep, and the memory is continuously updated. 'Free Run' is over-ridden by the 'Single Sweep' and by 'Hold Display' controls - both these disabling 'Free Run' operation.

7. **Level Trigger/Window Trig**

'Level Trigger' operation uses precisely the same method of triggering as that described for normal oscilloscope operation, i.e. the slope of the signal causing a trigger is selected by the +/- button, and the level at which triggering occurs is set by the 'Trigger Level' control. Window trigger is an alternative trigger circuit only available when in Storage mode. It is intended for use in capturing and storing waveforms with unexpected transients, and this will be normally used in 'Single Sweep' mode. It is an a.c. coupled circuit only and is independent of the setting of the Level control. Transients which would cause a deflection of either + or - one major division from the quiescent value will cause a trigger.

8. **$^1/_4$ Pre Trig**

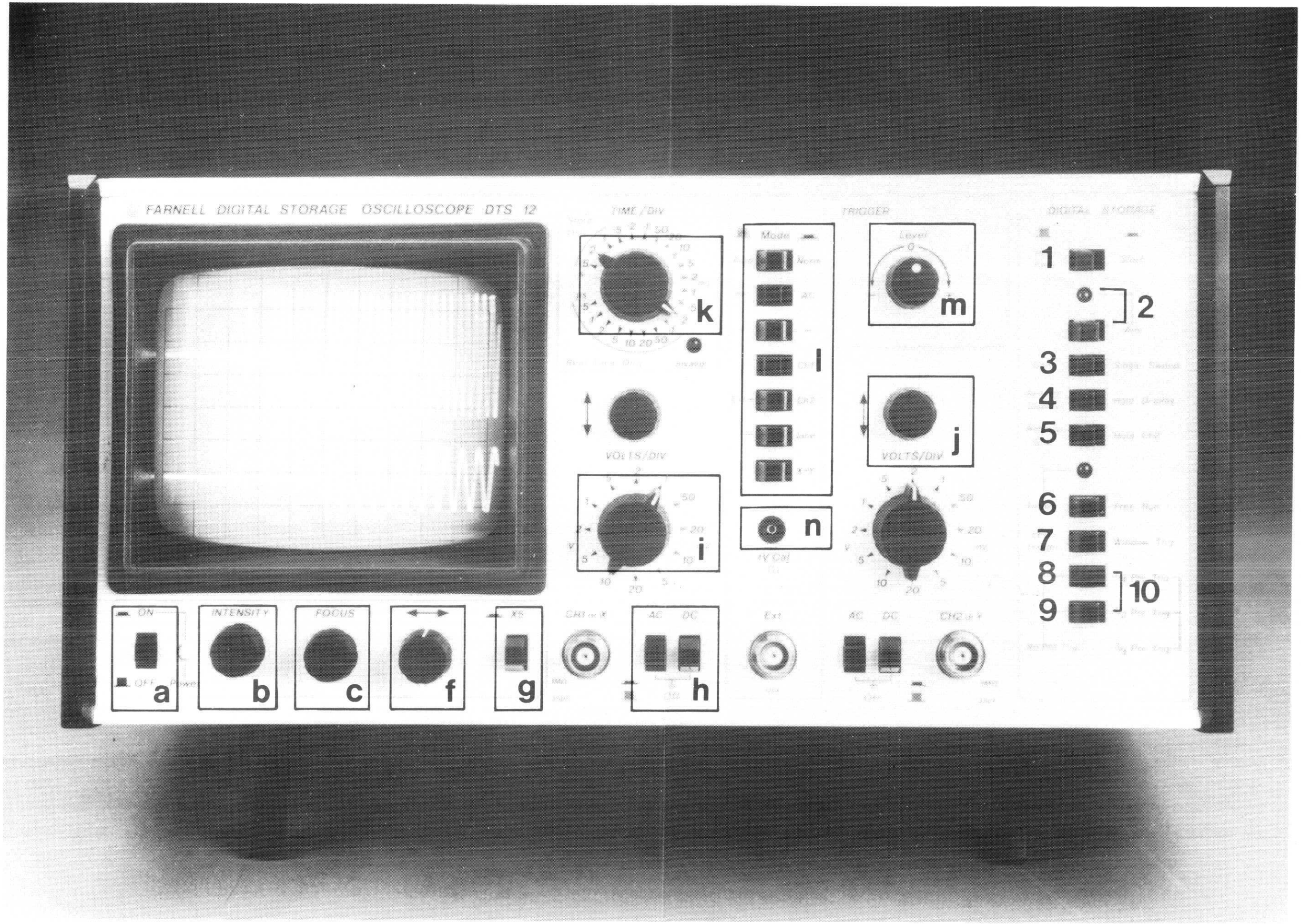
This causes the signal causing the triggering of the sweep to be displayed from $^1/_4$ the way along the trace (from the left hand edge) to the completion of the sweep. This means that signals displayed before the points are a record of the waveform applied to the input prior to the event causing the trigger.

9. **$^1/_2$ Pre Trig**

This button behaves exactly as the one above, except that the event causing the trigger appears half way along the trace(s).

10. $^{3}/_{4}$ Pre Trig

Obtained by depressing both $^{1}/_{4}$ and $^{1}/_{2}$ Pre Trig buttons simultaneously. This has the same action as $^{1}/_{4}$ Pre Trig, except that the triggering event is displayed $^{3}/_{4}$ of the way along the trace and the first $7^{1}/_{2}$ major divisions of the trace display signals occurring before the trigger.


FARNELL DIGITAL STORAGE OSCILLOSCOPE DTS 12
TIME/DIV
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i
TRIGGER
Mode
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ON
OFF
a
INTENSITY
b
FOCUS
c
f
X5
g
CH1 or X
AC DC
h
Ext
AC DC
CH2 or Y

OPERATING INSTRUCTIONS

The Farnell DTS12 is simple to operate in either REAL TIME or STORAGE MODE.

REAL TIME OPERATION

Locate the 'Real Time/Store' button in the top right hand corner of the front panel and ensure that it is not pressed in. Once this is done it does not matter whether any other buttons in the DIGITAL STORAGE section are in or out -they are inoperative.

First use

Connect the instrument to the a.c. supply and switch on the unit by depressing 'Power On' button. The adjacent green LED mains indicator should light. Set the controls as follows:-

REAL TIME/STORE	to real-time (out)
TIME/DIV	to 0.2ms
TRIGGER LEVEL	to mid travel
TRIGGER MODE	Auto-Norm button to Auto (out)
	AC-DC button to AC (in)
	'+' '-' button to + (out)
	CH1 button depressed
	CH2 button out
	Line button out
X SHIFT	set to mid travel
Y SHIFT	both set to mid travel

VOLTS/DIV	both Y attenuators set to 0.2V
AC-DC	input selector switches both set to DC

After allowing a brief warm up period (less than 1 minute) two traces should be visible on the screen. If not, further adjustment of the X-shift and Y-shift controls, with a possible increase in intensity should reveal the traces. Adjust the intensity control for a suitable viewing level. Note: Excessive intensity can shorten the life of the tube. Adjust the focus control to give a sharp trace. Using either a probe or a suitable input lead coupled to CH1 connect to the 1V cal. output and check that the square wave is displayed. Rotate the trigger level control until the display locks (the square wave is stationary).

STORAGE MODE - First time operation

To observe how easy is the transition to storage mode - try this sequence:

a) In real time mode connect a signal of about 1kHz (the Cal. output will do) to the input of CH2. Leave CH1 on but with no input. Select CH2 triggering, timebase 0.5ms/div, AC trigger, and obtain a steady display of this signal in the lower half of the screen. Position the CH1 trace (horizontal line) in the upper half.

b) Look at the buttons enclosed by the DIGITAL STORAGE area of the front panel. A useful adage at this point is: 'if in doubt, buttons out!'. Make sure all the buttons are out. Press in the 'Store' button. The display will remain almost as before except the signals are being stored before being displayed.

The store is being continually updated by the inputs. You can see this by adjusting the CH1 Y shift control. Notice the trace moves as in real time operation. Temporarily remove the input to CH2 and note that the display

'freezes' and the 'Trigger' light extinguishes. Movement of CH1 Y shift control no longer alters the trace position. The original signal has been stored.

c) **Hold display**

Reconnect input to CH2. Once again the display is being updated and you can confirm this with CH1 Y shift as before. Now press 'Hold Display' and note that once again the display is frozen. What actually happens is that when this button is pressed in, the write timebase completes that scan and the memory is then prevented from receiving further updating. This can be checked by trying the same procedure as above but at a much slower timebase setting.

d. **Hold CH2**

Finally try releasing the display but pressing 'Hold CH2'. This time it will be noticed that the CH2 trace is frozen but CH1 can still be seen being updated. This is possible because CH1 trace is still being triggered by CH2, as the 'Trigger' light shows. If the input to CH2 is removed, once more the light goes out and even CH1 is frozen.

e. **Free run**

Pressing 'Free Run' now will show that CH1 is being updated. Return to Trigger, select CH1 as source and connect input to CH1 and note how this information can be compared with the CH2 trace already held in store.

f. Single sweeps

Return input and trigger source to CH2. Release CH2 and check display is triggered and remove CH2 input temporarily. Select 'Single Sweep' and depress the 'Arm' button. The Arm lamp should light. Reconnect input and observe Trigger lamp lights and sweep is triggered. Both lamps extinguish at the end of the sweep and no further sweeps are triggered.

g. Pre-trigger

Retaining 'Single Sweep' mode, remove input signal, select '$^1/_2$ Pre Trig' press 'Arm', and briskly reconnect the input. Note that most or all of the first half of the trace is blank. The signal which actually triggered the sweep is now at the mid point of the trace. Note that if a positive level and slope have been selected for triggering and at the instant of reconnection the input signal was negative, then this will appear before the half way mark (prior to the triggering point). This demonstrates that signals occurring prior to the trigger are stored and displayed.

Finally, try pressing 'Hold CH2' after a display has been stored as above. Change trigger source to CH1, select '$^3/_4$ Pre Trig' (both lower buttons in together), press 'Arm' and connect the signal to CH1. Now the CH1 trace should trigger giving a display whose trigger point is $^3/_4$ of the way along the trace.

ANOMALIES AND PRECAUTIONS WHEN USING DIGITAL STORAGE

1. Aliasing

This phenomenon manifests itself when a signal - say a sine wave, is presented to the oscilloscope of a much higher frequency than would be appropriate for display at the timebase speed set. The resulting display may be a perfect sine wave, but at a spacing on the screen suggesting a much lower frequency than that of the actual input. This occurs because of the sampling nature of a digital storage oscilloscope. The Nyquist criteria demands two samples in the period of the fastest sine wave to be stored, in practice a minimum of 5 samples is necessary. If the input signal is faster than this, aliasing may occur. There is no automatic system for avoiding the problem on the DTS12 but, if you suspect aliasing is occurring, try a faster timebase speed or check the appearance of the input on Real Time operation. Input frequencies should be less than 20 divided by the time per div setting of the timebase switch.

2. Dual Channel/Single Channel Operation

Horizontal resolution can be doubled by using only one channel. The unused channel is turned off as in Real Time mode by releasing both input coupling selector switches (AC - DC). When operating CH2 alone, note that the Hold CH2 facility is inoperative and the 'Hold Display' button must be used to retain a stored waveform. This is intentional because it is not possible to store a waveform on CH2 operating on its own, and then retain this when switching back to dual channel operation. This is because in single channel operation, the whole memory is used for that

channel, whereas when both channels are used, the odd memory locations are used for CH1 information and CH2 in the even locations. Therefore any waveform stored when in single channel operation becomes meaningless if dual operation is selected and vice-versa.

3. X-Y Operation

X-Y operation is not available in Storage mode, and attempts to obtain this mode by depressing the X-Y switch can result in an anomalous display.

4. Y-Shift Controls

The Y shift controls have no further effect on a trace once stored. While it may seem desirable at times to be able to move a stored waveform up and down the screen, perhaps for better comparison with the waveform stored from the other channel, it is not possible. This is because the display screen in storage mode is displaying the entire memory within the 'window' that the screen represents - like looking at a photograph through a frame which just fits it. To move the traces after storage would involve changing the information in the memory, which is beyond the capabililty of an instrument of this category.

CIRCUIT DESCRIPTION

a) Real Time Section

CAUTION. Personnel attempting maintenance or servicing this oscilloscope should take care to avoid contact with the high voltages that are present within the unit at many points, particularly, but not only, in the vicinity of the cathode ray tube. NOTE. The insulating washers used in the mounting of power transistors on the rear of the heatsink flange (inside) are of Beryllia which can be highly toxic if consumed or if dust from a crushed or broken washer is inhaled. Take great care when servicing to avoid losing these washers or, in the event of disposal, ensure that they are treated as toxic waste.

General description and location of parts

The circuit is divided into a number of separate functional parts for the purpose of this description. The physical location of these parts is as follows.

The input signals to Y channels are taken to separate attenuators mounted on the front panel rotary switches. The FET stage following the passive attenuator and the succeeding impedance transforming transistors and pre-amplifiers are mounted on small circuit boards beneath the attenuator switches each of which is completely housed in a screening box. Access to these can only be gained easily by withdrawing the module, which the two input attenuators comprise, out through the front panel after first removing the front panel legend escutcheon. See Recalibration section.

The input Y amplifiers are both on the main, horizontally mounted circuit board to the right of the vertically mounted 'trigger' board. The main Y amplifier is

at the rear of the main circuit board behind the CRT. The trigger circuitry together with the selector switches and timebase generator are all to be found on the vertically mounted board, with the exception of the timebase timing resistors which are on a small board on the back of the timebase switch.
The timebase ramp is fed to the main X amplifier which is located on the horizontal circuit board to the right of the CRT. The blanking information is also fed to the blanking amplifier mounted centrally at the rear of the large circuit board. The low voltage power supply is fully stabilised by integrated circuit regulators mounted on the rear heatsink flange under the mains transformer. The EHT tripler and regulator components are mounted underneath the CRT.

Y attenuators and input amplifiers

The input stages for CH1 and CH2 are identical. The input attenuator consists of four passive sections switched in various combinations to obtain the desired attenuation. A preamplifier using a matched dual FET follows the attenuator. One of the FETs forms a source follower, with the other used as a constant current tail to keep the gain close to unity and maintain good d.c. temperature stability. The d.c. balance is trimmed by adjusting this current using P1.
The output of the FET stage is fed via an emitter follower, TR3, to give a low impedance drive to the amplifying stage formed with TR4 as a common emitter feeding TR5 as a common base stage. The gain of this configuration is determined by R20 and series combination of R23 and P2.
Calibration is adjusted by means of P2. The output from this stage is fed via screened cable to the input of the trigger and beam switching stages on the main board.

Y beam switching and output

Further Y amplification and variable gain are obtained with the differential amplifier stages TR150, 153 and 154 (CH1) and TR250, 253, 254 (CH2). TR256 and 257 are constant current tails for CH2 stage. TR150 and 250 amplify and separate the signal from the trigger circuits.

Beam switching is achieved by TR151 and 152 (CH1) and TR251, 252, 259 and 260 (CH2). TR259 and 260 are in operation when CH2 'Invert' is selected.

TR258 is used to form a constant current source to provide the same biasing into the main Y amplifier when in the CH1 + CH2 mode as when in the normal mode. The selected signal (or both simultaneously if CH1 and CH2 is selected) is fed to the Y output stage which also operates as a feedback amplifier with the input to TR302 being a virtual earth point. TR304 and 305 act as a constant current tail for differential amplifier TR302 and 303, which in turn feeds high voltage transistors TR306 and 307 in common base connection. The output of these each goes to an emitter follower, TR308 and 309, providing a low impedance drive to the Y plates, and feedback resistors R301 and R325. Z301 prevents the emitter followers from saturating, likewise TR307 by diodes D301 and 304.

X amplifier and output

TR507 and TR508 combine to form the X driver amplifier. Feedback via R522 to the virtual earth point at the base of TR508 allows the gain to be varied for the X5 expansion facility, and for calibrating X-Y gain by varying the input resistance to this stage. Switching to X5 expansion parallels R514 with R520and P506 calibrates the X5 gain. The X-Y input is fed through R513 and P505, the latter is used to calibrate X gain in the X-Y mode.

The X-plate driver amplifier is a conventional differential amplifier with TR503 and 504 as constant current tails. TR501 and TR505 form the differential pair driving TR502 and TR506 acting as high voltage plate drivers. The X plate output is also used to derive a focus correction waveform by way of the circuitry including D501 to 504 and TR509 and this is applied to a special electrode in the tube.

Blanking and Z Mod

The logic signal corresponding to 'flyback + holdoff' is used to turn on TR705 which feeds the high voltage transistor TR706, the output of which is coupled to the grid of the cathode ray tube via C720.

Power supply

There are 5 d.c. supply rails. The $\pm$12V rails are derived from the same transformer secondary and are stabilised using integrated circuit regulators IC701, 702. The variable current for the twist coil is provided from this part of the circuit by TR706.

The +5V d.c. supply is stabilised using an integrated circuit regulator mounted on the back panel. The raw supply for this rail comes from a separate secondary on the mains transformer. The 275V d.c. supply comes from a separate transformer winding, rectified by a bridge rectifier D706 to 709, and smoothed with section C703 and 704 with R728 and R729.

The -1850V d.c. tube supply is derived from a tripler fed from another winding on the transformer which is then stabilised by transistors TR702 to 704, TR702 acting as a series regulator. P703 allows the regulator to adjust the supply to give 1850V at the tube cathode.

Trigger circuit

The trigger circuit may drive its source from either input channel trigger take-off amplifiers, or from the external input socket or from a secondary of the mains transformer when 'Line' is selected. The appropriate source is selected by using the lower two push buttons of the mode selector switches, while unused inputs are decoupled to ground by capacitors to stop spurious triggering. The selected source is coupled via the DC/AC switch to the long tail pair TR2 & 3 which gives in phase and inverted outputs. The desired output is selected by the '+/-' slope push switch and is passed direct to TR4.

The amplifier TR3 also has a variable bias provided by the trigger level control and passes the amplified and level adjusted signal to comparator IC601. This comparator has positive feedback applied by R629 and R630 giving some hysteresis and a Schmitt trigger effect.

The trigger pulses from the output are passed to the trigger logic circuit via a NOR gate acting as a buffer, in IC603. These triggers clock a D-type flip-flop in IC602 where the D input is held at 0. When clocked the Q output becomes 0 and hence Q becomes 1 which initiates a sweep. The CLR and PRE inputs to this D-type when low (active) override the clock. The CLR input is held low for X-Y mode operation to ensure the flyback blanking circuit is disabled.

Triggers from the D-type Q output are also fed to an inverter in IC609 which shorts C613 to ground. In the absence of trigger pulses the voltage on C613 rises slowly fed by R642. When this voltage reaches logical '1' a CMOS buffer in IC604 inverts this signal to feed the sweep deciding logic NOR gate in IC603, which in turn allows the timebase to free run. In 'normal' mode a switch shorts C615 permanently to logic '0'. The above conditions control the output of the deciding logic (Pin 1 IC603) which goes low to allow the timebase to sweep and

high for flyback and hold-off. The logical expression for pin 1 to be low and hence allow a sweep is, in terms of pin numbers '2 OR (6 AND 5)', the equivalent of which in function terms is 'trigger present' or (free run and not flying back plus settling delay).

When the timebase sweeps, comparator IC607 is used to detect both end-of-sweep and end-of-flyback. Its output is normally high, going low at end of sweep, returning high at completion of flyback. The latch formed by half of IC608 together with an inverter in IC609 and the NAND gate in IC604 form a monostable circuit which is timed by R70 and C622 with the addition of C623 at slow timebase speeds. This monostable is triggered by the negative going output of comparator IC607 at the end of sweep. Its timed low going output is connected to the pin 10 PRE input of IC602 which inhibits triggers during the flyback and subsequent settling period.

The monostable high going output feeds through NOR gates in IC603 setting pin 1 high which turns TR13 on to short out the timing capacitors C620 and C621, causing flyback. Termination of the monostable timing period will cause a further sweep when in the AUTO mode in the absence of triggers.

Timebase

A constant current source charging a capacitor is used to generate the timebase ramp. To achieve the different ranges only two timing capacitors are used, the intervening ranges are effected by altering the charging current by resistor selection. IC605 generates a constant voltage across the selected charging resistor. A constant current of approximately 1mA produced by TR5 and 6 and associated circuitry results in a constant voltage drop across R689. By the action of negative feedback the same voltage appears across the charging resistor selected thus attaining a constant charging current into either C620 or

C621. IC606 is used to buffer the ramp before applying it to the X preamplifier and the comparator. IC607 which defines the ramp limits at approximately 0V and 5V.

Channel switch and cal. oscillator

Two buffers in CMOS IC604 and one in IC609 are used with R631, R632 and C610 to form an astable multivibrator running approx 1kHz. The lightly loaded open collector output of IC609 buffer approximates closely to the supply rails and offers sufficient stability for a calibrator. The actual output voltage is trimmed to 1V pk-pk by the potential divider R635 and P606.
A similar oscillator formed by a buffer and a NOR gate in IC604 with C616, R126 and R651 is used as the chopper oscillator, running at approx 200kHz. The output of this oscillator is used to clock a D-type flip-flop connected in a toggling mode. The outputs from this D-type are used to drive the beam switch circuit. This flip-flop can be jammed into one mode or the other by the use of the preset or clear inputs which can be enabled by the channel select switches or by the X-Y position on the timebase switch. Selection of any of these disables the chopper oscillator via D604 or gates in IC608 and IC609.
At higher timebase speeds, the chopper oscillator is disabled by applying a '0' to pin 6 of IC604 and a '1' to pin 7. This then allows the flyback logic signal from pin 10 of IC603 to be used to clock the beam switch D-type toggle which in turn provides alternate beam switching.

b) DSO SECTION

In storage mode, outputs from each Y channel are taken from the Y preamplifier outputs which follow the channel attenuator. When operating in dual channel

mode these Y signals are time multiplexed - much as in Chop mode - to the input of an analogue to digital converter, which converts samples from each channel alternately to an 8-bit digital number representing the instantaneous voltage of each sample. The rate at which the samples are taken is dependent upon the setting of the timebase switch, but it is always arranged such that there will be 1000 samples for a full sweep of the screen. If one channel only is selected then there will be 1000 samples of this channel. If both channels are selected then 500 samples will be taken of each channel. An 8 bit number can define 256 different levels, so the Y direction can display signals to a resolution of one part in 256 spread across the 8 divisions of the screen. Input signals which would be displayed above the top or below the bottom of the screen are digitised as though they were at the top or the bottom, i.e. the effect of the digitising is to clip large signals to the limits of the tube height - although this is transparent to the user because the clipping cannot be seen. From this it should be noted that the Y shift controls act on the input signal prior to digitising, and once in store, the Y shift controls cannot be used to move the displayed traces.

Display & Display Memory

In storage mode the screen displays the contents of the display memory - a 1K x 8 bit RAM (two chips IC28,30) in the format described (i.e. 256 levels in Y direction by 1000 samples in X direction), whether or not a signal has been recorded into it. Displaying this memory is achieved by reading successive locations and using a digital to analogue converter to reproduce an analogue signal which is taken to the scope Y amplifier. A timebase sweep is applied to the X-amplifier synchronised to start at the first address read from the memory. Reading the memory is quite independent of the digitised samples being written

into it. The whole memory is read every 2ms, but displayed in one of two ways. In single channel operation every memory location is read and displayed in one sweep lasting 2ms. During the sweep, all the even locations are read first, then all the odd ones. In dual channel mode, all the odd numbered memory locations are read in one sweep - displaying CH1 signal, and then the even numbered locations are read in the following sweep (each sweep lasting 1ms). Summarising: CH1 and CH2 samples are written **into** memory alternately (CH1 to odd locations) whereas they are read **out** of memory sequentially - first of all CH1, then all CH2's samples.

Delay Memory

To cater for the provision of seeing events occuring before the trigger the DTS has also a separate delay memory (IC29, 31) which is also a 8 bit x 1K RAM (two chips). Output from the A-D converter is never written directly into the Display memory but always into the Delay memory. This happens continuously irrespective of trigger state - because one never knows when a trigger is likely to occur! The delay memory is a circulating store, the best analogy for which is that of the circular overhead conveyor for a paint-shop heat-treatment plant. The sequence here is that stoved painted parts are removed from a hook for shipment to the metalwork store. A freshly painted part can then be placed on the vacated hook. The number of parts which will be removed for shipment to the store before this part comes round depends upon the number of hooks round the conveyor. The main Display memory is the metalwork store in the analogy, and the hooks on the conveyor the Delay memory. Clearly the conveyor must be clocked round at the speed at which freshly painted parts become available. The Delay memory address counter (IC32, $^1/_2$ IC26) is clocked at the A to D digitising rate. The size of the Delay memory (the number of hooks) can be varied

by the amount of pretrigger selected - from 2 samples (Note not zero!) in No Pretrig., 256 samples in $^1/_4$ Pre Trig, 512 samples in $^1/_2$ Pre Trig and 768 samples in $^3/_4$ Pre Trig.

System Cycle

The timing of all events is referred to a 500kHz square wave hereinafter called the system cycle. This is generated on the timebase board by division of the 5MHz crystal oscillator by IC15 and IC13 and buffered on the logic board by part of IC9. The system cycle, when high, selects the value of the 'read' counter on to the address lines of the display memory, and when low selects the 'write' counter. When the system cycle goes high, the 'read' address counter is incremented and the display memory is set in Read mode, while the delay memory is inactive. The contents of location addressed by the 'read' counter is fed to and stored in IC13 on the Analogue board - an 8 bit latch.
When the system cycle goes low, there exists a possible 'write' mode. At slow timebase speeds many system cycle low states will pass in which nothing happens, but at the fastest time base speed there is a 'write' sequence every system cycle low. When activity is set to occur, as decided by a positive transition of the 'write' time base clock, the sequence is as follows:

a) 'Write' address counter and delay address counter are both incremented.

b) Both D types in IC16 on the Timebase board are preset ready for next falling edge of system cycle.

c) The contents of the delay memory at the location currently addressed by the delay address counter is output on to the data bus and written into the display memory at the location addressed by the current value of the 'write' address counter. After this operation, chip select is removed

from the display memory. The delay memory is then activated into 'write' mode, at the same time as the 8 bit latch IC11 on the Analogue board is enabled which holds the latest result of an A/D conversion from IC10. This data transfers to the delay memory.

LOGIC BOARD

Write Address Counter

The write counter comprises IC22 and one flip flop in IC26. The way in which the write address counter is clocked differs depending upon whether dual or single channel operation is selected.

Note: It is worth interposing an explanation of some of the logic gate groupings used in connection with this function. There are 3 groupings of gates which all perform the logical function of a single pole double throw switch, and in each the position is determined by whether Single or Dual operation is selected.

These are tabulated as follows:-

Output from	Input selected from Dual	Input selected from Single	Gates involved in SPDT group
IC1 p8	IC16 p5	IC33 p6	IC4 p1,2,3;IC1 p8,9, 10
(Note o/p inverted)	(Write t.b. - 2)	(Lo=CH1 only, Hi=CH2 only)	IC2 p1,2,3;IC11 P10,11

IC4 p11 (Read address l.s.b.)	IC33 p6 (Lo=CH1, Hi=CH2)	IC23 p10 (Lo, 1st 512 counts)	IC4 p4,5,6;IC4 p8,9,10 IC4 p11,12,13;IC11 p10,11
IC6 p6 (Read counter reset)	IC23 p11 (Goes lo after 512 counts)	IC23 p10 (Goes lo after 1024 counts)	IC6 p1,2,3;IC6 p4,5,6; IC4 p4,5,6;IC11 p10,11

Dual Mode

The write time base (w.t.b.) clock input drives a divide-by-two toggle in IC16(i). The output of this toggle is selected as described above as the Data input for D-type IC16(ii). This D-type is also clocked by the write time base so its outputs Q and $\overline{Q}$ also toggle at half the w.t.b. frequency. These outputs are used to multiplex the Y input channels to the analogue to digital converter (ADC). The Q output is also selected to act as clock for both the write address counter and delay address counter and is itself the l.s.b. (least significant bit) of the addresses. This results in the data from the ADC, which is a result of the previous conversion (CH1 information) being written into the odd locations.

Single Channel Mode

If one of the two Y channels is switched off, a different mode of storage is enabled. The D-type toggle IC16(i) provides the write counter clock and l.s.b. display. The Data input to IC16(ii) is set at Hi for CH1 and Lo for CH2, and this level appears at the output throughout a write cycle, as the w.t.b. is still connected to the clock. In this mode the data is stored in the display memory by first filling all the even address locations, then all the odd addresses. In other words, the l.s.b. of the address is connected to the m.s.b. (most significant bit) of the address counter and, furthermore, all the other address bits must be removed one bit lower on the counter output. This is achieved by the selectors IC18, 21 and 25, which switch the address lines between the counter outputs appropriately.

Read Address Counter

The read address counter comprises IC19 and IC23 and is always clocked at 500kHz by the system cycle. In dual channel operation the contents of the memory are displayed in two sweeps, one displaying all the odd memory locations (CH1), the next all the even ones. This is facilitated by the count of 512 causing a monostable on the timebase board (IC19) to be triggered, which resets the read counter and toggles D-type IC33(i), the output of which is selected in dual mode to be the l.s.b. of the read address. In single channel operation all the memory locations are read in one sweep; all the even locations first; followed by the odd locations. This is achieved by the action of one of the dual/single selector gate groups previously mentioned, which disconnects the read address l.s.b. from toggle IC33(i) and connects it to the 210 output of the read counter which is low for the first 512 counts and high for the next 512.

Read/Write Address Selection

The choice between read address or possible write address selection is controlled by the system cycle which controls the address multiplex ICs IC17, IC20 and IC24, the inputs to which come from the read address counter and the appropriate selections already made by selectors IC18, IC21, IC25 from the write address counter.

Triggering, Free Run and Hold

Valid triggers are available from the oscilloscope's normal trigger circuit, or from the window trigger circuit which simply looks for transient deviations on the trigger input exceeding + or - 1cm of equivalent Y deflection from the quiescent position. This window detector (IC11 and diodes D2, D3) is on the trigger board. Whichever is selected, a rising edge is a valid trigger. This signal is gated by IC1(i) to prevent triggers going further when Hold Display is selected. From this IC, triggers pass to the clock of IC14(ii), the sweep control D-type. The Data input to this flip-flop is high if continuous mode is selected, or in Single Sweep where the Arm button has been depressed setting the Q of D-type IC14(i) to 1. When the Q output of the sweep control D-type IC14(ii) is clocked high by a trigger, this opens the gate IC1(ii) allowing the write timebase to clock the write counter. Note that the delay address counter is clocked continuously irrespective of trigger state, but after a write count has been commenced data from the delay memory will no longer go to waste, but be passed to the display memory.

When the write counter reaches the end of its count, this triggers monostable IC27(i) which resets the sweep control D-type IC14(ii) and the Arm D-type IC14(i).
The D-types in IC12 simply serve to de-bounce the action of the mechanical switches used for ARM and Single Sweep.

Hold CH2

The action of this function is to prevent CH2 information being overwritten by a new sweep. If the button is pressed during a sweep, then that sweep is completed. As it is only logical to implement this function when both channels are operative, gate IC8(iii) prevents the switch output being applied when one channel is off. If Hold CH2 is depressed during a sweep then this immediately removes the Clear signal from the Hold CH2 flip-flop IC33(ii), but not until the end of the sweep does the presence of a high on the Q output of the sweep control D-type cause the flip-flop to be preset; in which situation it will remain until the Hold CH2 button is released. Once the Q o/p of IC33(ii) has gone high, this is gated by IC2 (iv) and IC10 (i) and then NANDED (in IC8iv) with the complement of l.s.b. of the write counter, which goes high for even addresses (corresponding to CH2 information). Note, IC2 (iv) is only active when the 'P' or 'T' option is incorporated into the scope. The output of this gate removes the enable signal for the write address selectors setting address zero into which all further CH2 information is written. This location is never read because the read counter resets to 2 rather than zero at the end of a sweep.

Delay Counter

The delay counter IC32 and IC26(ii) has its count length controlled by the

action of the switches and gates in IC7 and IC8(ii). When No Pre Trig is selected, this causes a Clear signal to be fed through IC7(iv) and IC7(iii) so no clocking takes place. However, as the write clock also acts as the l.s.b. of the delay memory address, there is an effective 1 bit count. When $^1/_4$ Pre Trig is selected this causes IC7 p34 to go high, and when the count passes 256 this causes IC7 p6 to go high, and the NAND in IC8 causes the counter to be cleared and start counting again. When $^1/_2$ Pre Trig is selected, this leaves IC7 p6 high, but waits until the count passes 512 before IC7 p3 becomes high - causing the counter to be cleared as above. When $^3/_4$ Pre Trig is selected IC7 p3 and IC7 p6 only become high together after 768 counts which again clears the counter as before.

Analogue Board

The heart of the system is the analogue to digital converter (ADC), most of the circuit for which is on one chip, IC10. This converter is a successive approximation type of converter, which requires nine clock cycles to complete a conversion. The chip is clocked by the 5MHz crystal oscillator signal from the trigger board. During the successive approximation process the analogue signal presented to the chip must remain constant. This is done by use of sample and hold gates, one for each channel using IC17 + IC6 and IC18 + IC19. The output from the appropriate sample and hold gate is selected by analogue switches in IC20. When an A/D conversion is complete, the digital data is entered and stored in 8-bit latch IC11. The way in which this data is stored into memory is discussed elsewhere. Data to be displayed is held in latch IC13 which feeds digital to analogue converter IC14. The sample and hold circuit IC9 and IC12 together with integrator IC7 form a linear interpolator between successive data points so that a smooth display appears on the screen.

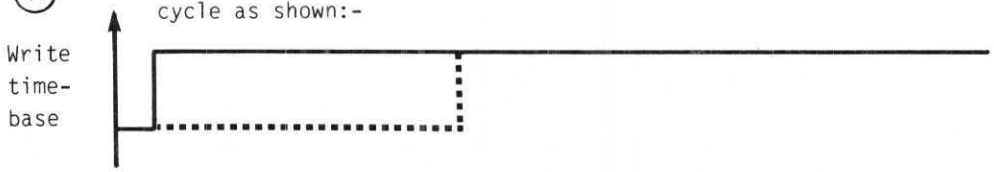
Trigger and Timebase Board

The circuit description of the trigger and timebase for the Real Time operation of the 'scope is given in an earlier section. The same trigger circuit is also used when the 'scope is used in storage mode. The write time base is derived from the 5MHz crystal oscillator on this board which is also used as the clock source for the A/D converter. The oscillator comprises TR15, TR16 and IC21(i). Transistor TR14 is used to disable the oscillator in Real Time operation. IC13, 14 and 15 are dual -10 counters, each divided into -5 and -2 sections. Three signals, at 1MHz, 0.5MHz and 0.2MHz are taken from appropriate divisions by IC13 and IC15 to one wafer of the timebase switch. For each valid position of the write timebase, one of these signals is selected and then taken directly as the write timebase clock (except for the 1MHz), or divided down by 10, 100, 1000, or 10,000 as selected by the second timebase switch wafer, the divisions being done by combinations of the divider IC's mentioned. The timing of the various functions of the storage and display play process are determined by the monostable circuits IC17-20 on this board. Their initiation is either by the selected write timebase clock or, for reading, by the 0.5MHz system cycle. This action is best described graphically - see Figs 1 to 4.

DTS12 Storage Scope

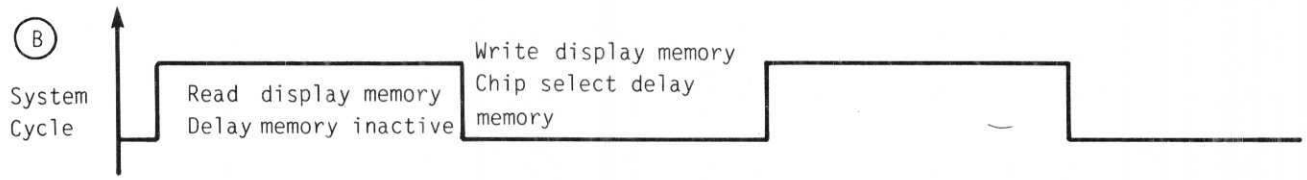
FIG 1. WRITE - SEQUENCE (DISPLAY MEMORY)

Ⓐ A 'write' sequence is initiated by a combination of the write time base & the system cycle as shown:-



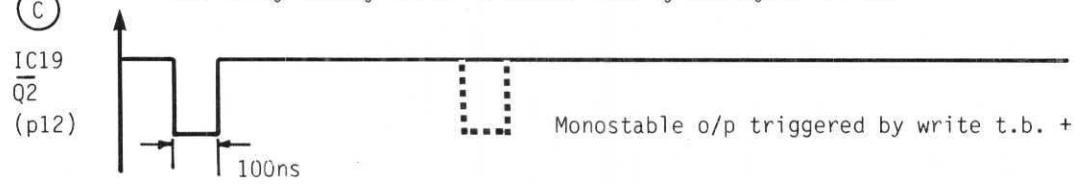
Note: rising edge of write t.b.may be coincident with + or - edge of system cycle

Ⓑ

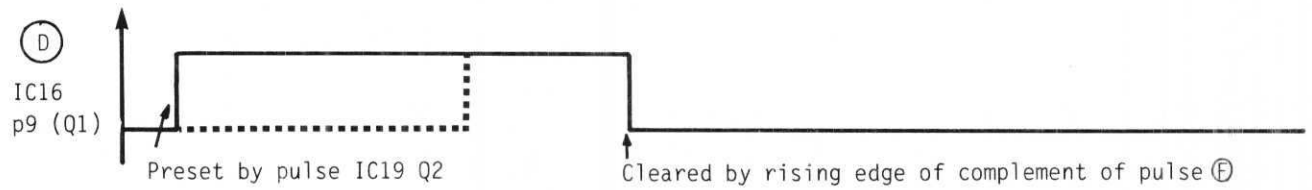


The system cycle sets display memory in 'read' when high & possible write when low, also the delay memory $\overline{CS}$ is selected when system cycle is low.

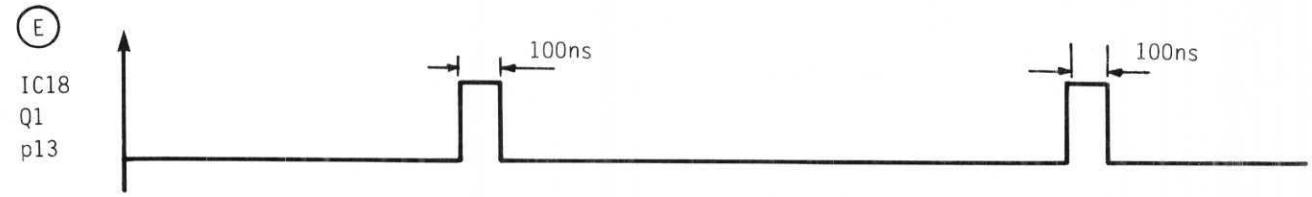
Ⓒ



Ⓓ

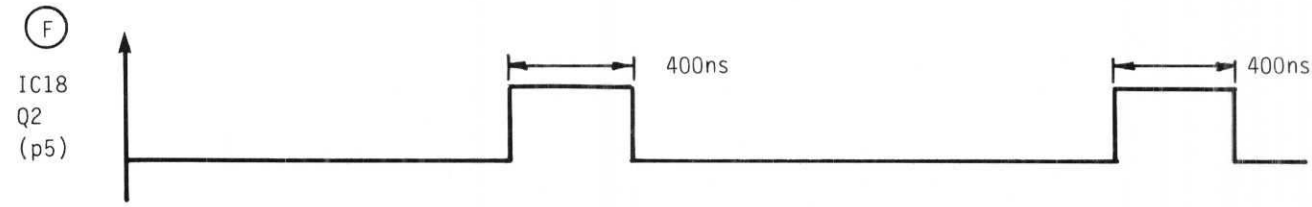


Ⓔ



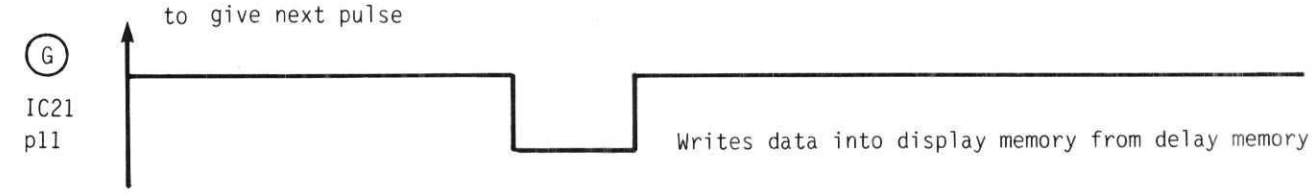
Delay pulse to give start of next pulse (below), triggered by system cycle -ve edge

Ⓕ



This pulse triggered by falling edge of previous pulse. This pulse is 'NANDED' with Ⓓ to give next pulse

Ⓖ



DISPLAY MEMORY CHIP-SELECT IN 'WRITE' MODE

FIG 2. WRITE - SEQUENCE (DELAY MEMORY)

A 'write' sequence is initiated by a combination of the write time base and the system cycle as shown.

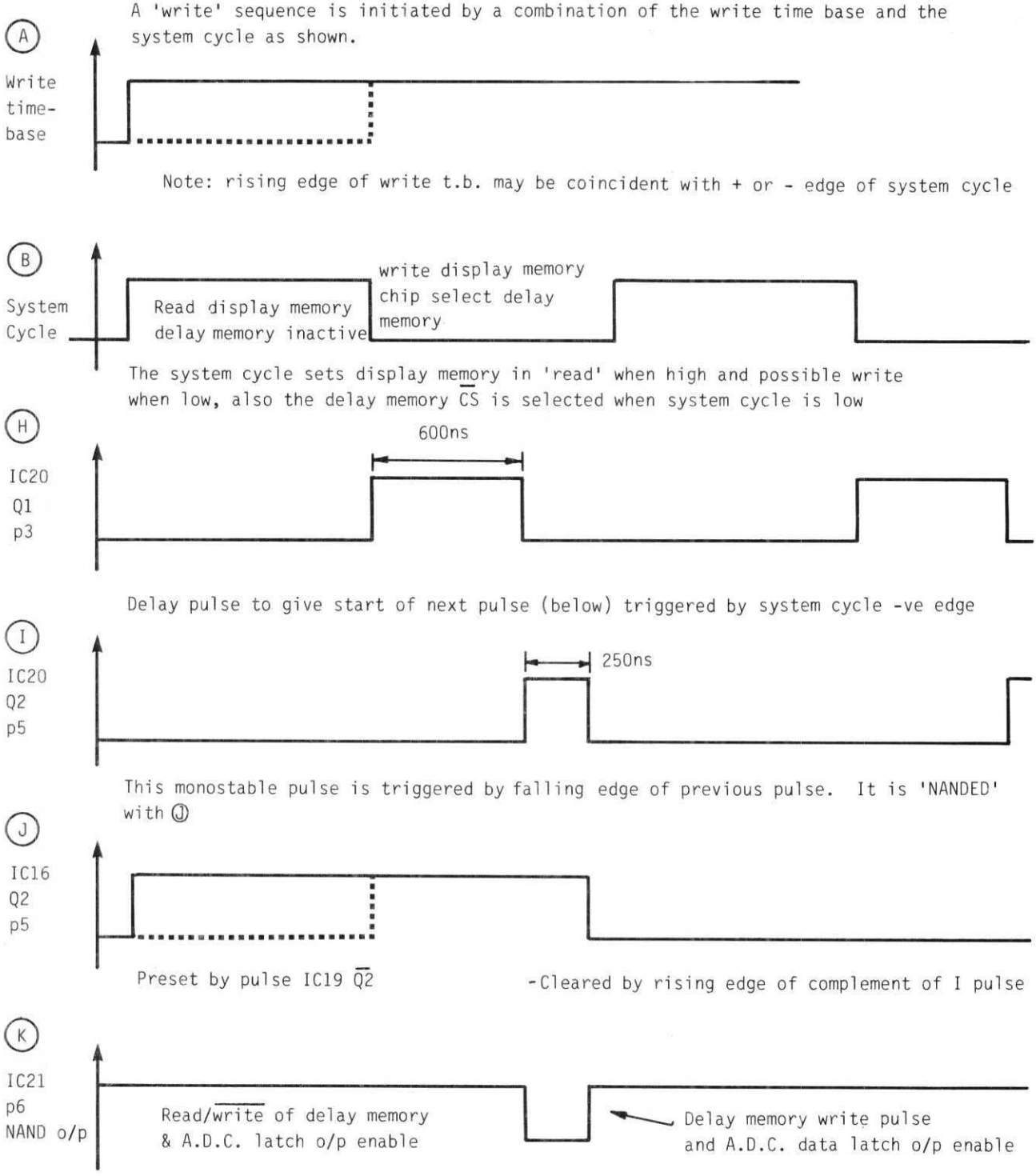
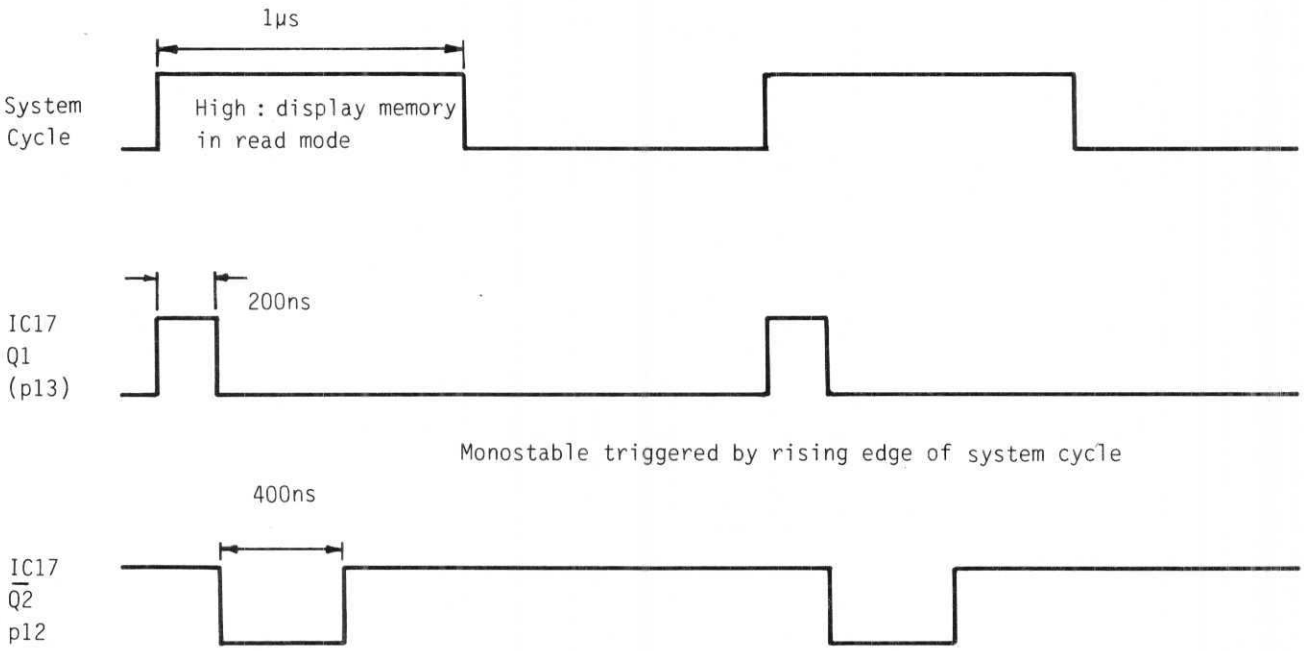


FIG 3. READ SEQUENCE

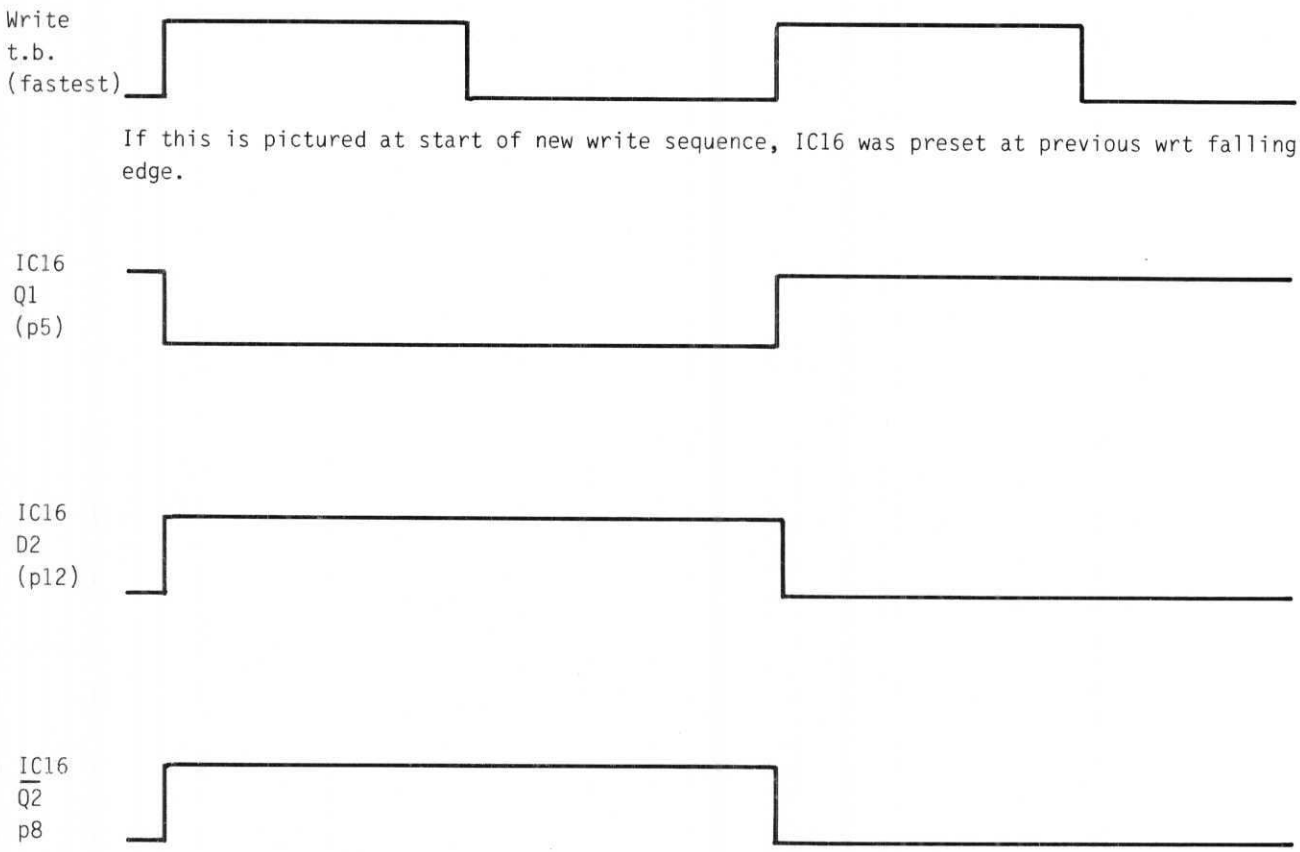
DTS12 Storage Scope



This is the same waveform as $\overline{CS}$ display memory in read mode. Also enables the 8 bit data latch which feeds the digital to analogue converter.

This waveform after another inversion goes to $\overline{\text{chip}}$ $\overline{\text{select}}$ of display memory in read mode.

FIG 4. WRITE CLOCKING DUAL MODE



If this is pictured at start of new write sequence, IC16 was preset at previous wrt falling edge.

This is used as write clock,
write address l.s.b.& also Ch2 enable (Ch1 enable is complement of this).

RE-CALIBRATION

Access

To gain access to the internal circuitry the top cover may be removed by unscrewing the two screws on each side near the base of the unit, and then withdrawing the cover rearwards and slightly upwards.

The underside of the main circuit board can be reached by removing the base plate. Adjustment of the compensating capacitor of the Y channel input attenuators can be done from the underside of the unit having removed the base plate. If necessary the covers to the screened boxes may be prised off for easier access. However should it be necessary to replace any components on the circuit boards or switches, then the attenuator assembly must be withdrawn through the front panel. This is effected by first slackening the screws affixing the two plastic side cheeks, pulling the cheeks off frontwards and thus releasing the top and bottom trims. The knobs must then be removed. The escutcheon carrying the front panel legends can then be lifted off. The attenuator module is then removed by unscrewing the four countersunk screws in the corners and withdrawing the assembly through the panel. It will be necessary to unsolder the wires to the board before complete withdrawal is possible.

CAUTION There are high voltages present within the unit at many points, particularly, but not only, in the vicinity of the cathode ray tube.

NOTE The insulating washers used in the mounting of the power transistors on the heatsink flange at the rear are of Beryllia which can be highly toxic if consumed, or if dust from a crushed or broken washer is inhaled. Take great care when servicing to avoid losing these washers or in the event of disposal treat them as toxic waste.

CALIBRATION

There follows a calibration procedure which will also help in identifying any faults which may have developed. The references to a 'scope are not to the unit under test, but to a service 'scope of bandwidth greater than 35MHz to help in the calibration.

Equipment required

Oscilloscope with a minimum bandwidth of 35MHz
Digital voltmeter and suitable high voltage probe
(Farnell DM141 or Data Precision)
Oscilloscope calibrator (Pulsetech)
Levelled signal generator (Tektronix 191)
Pulse generator (Farnell PG101/2)

Procedure

Switch on and allow the oscilloscope to warm up for at least ten minutes then check the following:-

+12V between chassis and IC701 O/P	Limits 11.6V to 12.8V
-12V between chassis and IC702 O/P	Limits -11.8V to -12.9V
+275V between C704 on rear heat sink (red) and chassis (a)	Limits 270V to 285V
-6V between Z601 cathode on Trigger board and chassis (a)	Limits -5.9V to -8V
+5V between pins 72 and 73	Limits 4.75V to 5.25V
+18V between IC701 I/P and pin 73 - unregulated.	Mean d.c. limits +17V to +23V

Ripple <4V pk to pk.

Flyback blanking

Connect 'scope to junctions of D720 and R734.

Check for negative going pulse at timebase frequency.

Limits: Most negative level: +12V ±1.5V, positive level: +39V ±6V.

Y-plate mean d.c. adjustment

Switch off CH2, Ground CH1.

Set front panel Y shift control (CH1) to centre of its movement. Connect probes from a dual trace scope to Pins 1 and 2 (o/p to 'Y' plates). Adjust P1 on attenuator boards (CH1) to obtain same voltage on both probes. Adjust P301 to obtain 150V on both probes. Switch off CH1. Ground CH2. Set CH2 front panel 'Y' shift to centre of its movement. Adjust P1 on attenuator (CH2) to obtain same volts on both probes.

'X' plate d.c. level

Depress both CH1 select buttons. Depress both CH2 select buttons. Depress X-Y switch to X-Y. Connect a dual trace oscilloscope probes to pins 36 and 37. Use X-shift pot on the front panel to obtain same voltage on each probe. Use P503 to adjust voltage on probes to 145V.

Trace rotate and geometry(when CRT has been replaced)

Connect signal source to channel 1 (1V pk to pk approx 20kHz) and depress both CH2 input switches. Set trigger to Auto. Switch on and adjust Y2 shift to position trace on centre line. Adjust 'trace rotate' to obtain horizontal line.

-18V between IC702 I/P and pin 73. Mean d.c. limits -17V to -23V

Ripple <4V pk to pk

275V supply - across C704 - ripple <5V pk to pk

E.H.T. adjustment

Connect the high voltage probe and digital multimeter to pin 43. Switch on and adjust P703 to obtain -1850V as accurately as possible.

Chopper oscillator

Set timebase to 1ms/div

Connect 'scope probe to IC604 pin 5.

Check oscillation frequency - Limits 200kHz to 280kHz.

Check positive peak >3.2V

Check negative peak <0.5V.

Beam switch flip-flop

Ensure that channel select switches are in the 'on' position (d.c. or a.c.)

Set timebase switch to 50us/div.

Connect 'scope to IC602 pin 5.

Check for a square wave at half the timebase ramp frequency

Check amplitude is between <0.2V and >4.5V

Connect 'scope to IC602 pin 6.

Check for a square wave at half the timebase ramp frequency

Check amplitude is between <0.2V and 4.5V

Switch off and reverse the trace rotate leads to the coil if a horizontal line is impossible to obtain. Position the trace to the top graticule line and adjust P502 to obtain as straight a line as possible. Check for straightness by moving the trace from top to bottom of screen. Switch CH1 on with the attenuator on the 0.2V/div and normal trigger, CH2. A vertical line will be displayed on the screen. Position vertical line at the extreme left and then right hand graticule lines and check that excessive distortion is not present. Slightly readjust P502 to obtain the best compromise for horizontal and vertical linearity. Check correctness of operation of channel input switches. Remove signal source.

Y axis ripple rejection

Set the trigger to Auto, CH1 to 0.2V/div.

Set the timebase to 2ms/div.

Depress both CH1 select buttons.

Switch off CH2 (both input select buttons out)

Adjust P302 for minimum hum on the trace (minimum vertical ripple)

Attenuators

Set channel 1 attenuator to 5mV/div.

Apply a 20mV signal to channel 1 from the calibrator and check display for a good square wave.

Change attenuator to 10mV/div, apply 40mV signal and adjust C9 on the attenuator for best square wave.

Change attenuator to 20mV/div.

Apply 80mV signal and adjust C12 for best square wave.

Change attenuator to 50mV/div.

Apply 200mV signal and adjust C6 for best square wave.

Change attenuator to 100mV/div.

Apply 400mV signal and check for good square wave.

Change attenuator to 200mV/div.

Apply 800mV signal and check for good square wave.

Change attenuator to 500mV/div.

Apply 2V signal and adjust C2 for best square wave.

Check on all the other attenuator positions for good square wave.

Reset attenuator to 5mV/div.

Connect calibrator through 10.1 probe to channel 1.

Apply a 200mV signal and adjust probe compensator for a good square wave.

Change attenuator to 10mV/div.

Apply a 400mV signal and adjust C8 for best square wave.

Change attenuator to 20mV/div.

Apply an 800mV signal and adjust C11 for best square wave.

Change attenuator to 50mV/div.

Apply a 2V signal and adjust C5 for best square wave.

Change attenuator to 100mV/div.

Apply a 4V signal and check for good square wave.

Change attenuator to 200mV/div.

Apply a 8V signal and check for good square wave.

Change attenuator to 500mV/div.

Apply a 40V signal and adjust C1 for best square wave

Switch to a.c. and check that the square wave does not change significantly.

Repeat above steps for channel 2 using channel 2 adjusters.

'Y' Attenuator gain and d.c. balance settng

Ground channel 1.

Switch off channel 2.

Adjust 'Y' shift control to centre of its movement.

Adjust P1 to centre the trace, if necessary.

Switch channel 1 to d.c., switch attenuator to 5mV/div and apply 20mV signal to channel 1 input.

Adjust P2 to give a display of 4 divisions accurately.

Switch off channel 1.

Ground channel 2.

Repeat for channel 2 from step 3 using channel 2 attenuator adjusters.

Cal. waveform setting

Set CH1 to 20mV/div. Connect probe set on X10 to 1V cal. position on the front panel and check square wave. Adjust P2 on trigger boards to obtain 1V as accurately as possible. Check that the frequency is 1kHz ±200Hz. If necessary S.O.T. R32.

Sweep length and fast speed cal.

Set timebase switch to 50us/div. Trigger to CH1, CH1 on, CH2 off. Set attenuator to 500mV (CH1). Set bench scope to 100us/div. and connect the probe to the top of R125 on the trigger board. Adjust P4 to obtain sweep of 550us as accurately as possible. Remove probe.

With timebase still at 50us/div. and attenuator at 500mV/div. apply signal from calibrator to give markers at 50us repetition rate. Adjust P504 to obtain alignment of markers with tube scale.

Slow speed cal.

Set timebase switch to 5ms/div. Set calibrator to give markers of 5ms repetition rate. Adjust P3 (P4) to align markers to tube scale. Pull X5 switch and adjust P506 to obtain X5. Set timebase to 0.5us. Set calibrator to give markers of 0.5us repetition rate. Pull X5 switch. Reduce mains by 10% and adjust P503 so that display just does not break up. Re-set mains and depress X5 switch to X1. Re-check calibration at 50us and 5ms and then at all timebase positions.

D.C. trigger

Set front panel trigger level control to centre of movement. Apply a 1kHz sine wave of 20mV pk-pk to Ch1 set to 5mV/div with Ch2 off. Set timebase to 0.2ms/div. Adjust P7 on trigger board so that start point of sine wave is at the same d.c. level for either selection of trigger polarity (+ or -). Adjust P1 so that this point is centre screen. Check that the same is true if Ch2 is used instead of Ch1.

X-Y operation

Switch both channels on. Set attenuators to 200mV/div. Apply a sine wave of 1V. pk to pk at 1kHz to both channels. Switch to X-Y position and adjust P505 to obtain line at 45°C as accurately as possible.

Bandwidth

IMPORTANT Do not attempt to adjust C305 with scope switched on except with an insulated trim tool. This is a high voltage point.
Set CH1 attenuator to 5mV/div. Apply a sine wave from a constant amplitude signal generator. Amplitude set to give 4 large divisions, frequency set at 140kHz. Switch generator to 13MHz. Adjust C305 (trimmer) so that display on scope has an amplitude of 2 large and 4 small divisions (i.e. -3dB from original 4 large divisions at 140kHz). Repeat for all positions on CH1 and CH2. They should be no worse than -3dB at 12MHz.

Pulse response

Set Ch1 attenuator to 5mV/div. Set timebase to 0.5us. Apply a 1MHz pulse 0.6us width. Set amplitude to give 5 large divisions on each range. Check overshoot and general pulse response on each range from 5mV to 2V on both channels.

Z modulation

Connect a square wave pulse of frequency 1kHz to the Z modulation input on rear panel. Amplitude of pulse min. 0V max. +5.0V. Switch to Auto trigger. Select channel 1. Timebase to 1ms/div. Check display is blanked at input signal frequency.

Ext. trigger

Select Ext. trigger (both CH1 and CH2 trigger mode buttons out). Select norm. Connect output of signal generator to ext. trigger input socket. Check

triggering at 50kHz - triggers with 1V min pk to pk input. Check triggering at 12MHz - triggers with 5V min pk to pk input.

CALIBRATION - DSO section

Procedure

First ensure that the calibration procedure for the Real-Time operation has been completed. With the covers still removed, and observing usual safety precautions, power up the unit. In Real Time mode set traces to mid screen, ensure all trigger mode switches are out except AC Trigger on CH1 source. Set timebase ('t.b.' hereafter) switch to 0.2ms/div, ensure all storage mode switches are out, and then select Store mode.

Mention made in this procedure to monitoring test points with a 'scope refer to the use of another oscilloscope (such as a Farnell DTV12-14), and not the DTS12 under test unless specifically stated.

1. Check +5V present at IC1 pin 16, and -5V at the negative end of C36 on the analogue board.

2. Use oscilloscope to check 5MHz signal present at TP17 on t.b. board.

3. Monitor with 'scope t.b. switch terminal TBB3-6 (TBB3-2 earlier units). Check for square wave at 0.5MHz. As t.b. switch is rotated anticlockwise, check frequency reduces in 1, 2, 5 fashion, down to 5s/div position.

4. Monitor the waveform on pin 1 on the main board. A t.b. ramp should be displayed. Check with CH1 on, CH2 off, and adjust P2 on t.b. board to give 4.5V pk-pk approx. Turn on CH2, check repetition frequency of ramp doubles

and adjust P3 to give 4.5V pk-pk approx.

5. Monitor the voltage on pin 13, IC10, analogue board and adjust P6 to give 0.5V ±2mV with respect to the earth plane on the board.

6. Apply a 1kHz sine wave signal (hereafter 'test' signal) to CH1, with CH2 off, adjusting amplitude and position to display an 8 div pk-pk waveform positioned and triggered mid-screen in Real-time operation. Switch to Store.

   Check with 'scope that test signal appears at IC2 pin 6 on Analogue board. Monitor test signal waveform at IC20 pin 8 and adjust P1 and P11 to give 0.5V p-p biassed at -0.25V with respect to 0V.

7. Repeat 6) but feeding test signal into CH2 input with CH1 off, checking IC3 p6, and then IC20 pin 8, adjusting for level and bias with P2 and P12 on the Analogue board.

8. Select Real-time operation and set CH1 trace to mid screen with input grounded and CH2 off. Select Store mode and Free-run Trigger. Monitor rearmost end of R51 with DVM and use P3 to obtain 0V ±20mV. Adjust P7 to centre the trace on the DTS12 screen.

9. **Stored data display set-up**

   Select AC input mode on CH1, feeding in the 1kHz test signal, and return to triggered mode - check green 'Trigger' LED lights. On Analogue board, set P5 fully clockwise, and increase input signal amplitude until displayed waveform just limits at top and bottom. Using P3 and P5 set this display so

that the waveform clips evenly top and bottom and just above top and below bottom screen graticule.

10. **Amplitude calibration**

Switch Ch1 input to A.C. Apply a signal from the oscilloscope calibrator to CH1, to give 4 divisions deflection on Real-time, use 'Y' shift to position trace centrally on the screen. Select Store mode and use P11 on the Analogue board to give a display of 4 divisions high. Use P1 to position trace centrally as in the Real-time mode.

11. Repeat 10) for CH2, with CH1 off, using P12 and P2 for adjustment.

12. **Crosstalk**

Ground the input to both channels. Select Free-run Trigger in Store mode. Set CH1 trace to mid screen, and using the Y-shift on CH2, check for movement of CH1 trace as CH2 trace is moved up and down. Minimise this crosstalk with P14.

13. Set CH2 trace mid-screen and move CH1 trace up and down. Minimise crosstalk with P13.

14. **Timebase calibration**

Use an oscilloscope, calibrator or other accurate time mark source as input for CH1 with CH2 off, and set a triggered display in Store mode with the t.b. set to 0.2ms/div. Adjust P2 on t.b. board to align time marks with

graticule. Turn both channels on, and adjust P3 to align time marks with graticule.

15. 'Invalid' LED

Check operation of the Invalid LED by switching TB switch to invalid positions in real-time and storage operation.

16. **Single sweep and pre-trigger**

Select Store mode, t.b. to 0.2ms/div., Single Sweep and with no input connected, depress Arm. Check Arm LED lights. Apply test signal to CH1, with CH1 on. This should trigger a single trace (if not, see Trigger setting up), the Trigger LED should light momentarily and the Arm LED extinguish at the end of the sweep. Disconnect test signal.

Set t.b. to 2ms/div, select $^1/_4$ Pre Trig, re-Arm and reconnect signal. Check that resulting stored trace shows no signal for first $^1/_4$ screen.

Perform similar checks for $^1/_2$ and $^3/_4$ Pre Trig

17. **Display holds**

Select 0.2ms/div on t.b., continuous operation in Store mode and connect the test signal to CH2, with controls suitably set to trigger trace. (Check in Real-time if necessary). When trace is observed, press 'Hold CH2', remove signal, and apply this to CH1. Trigger from CH1. Check that CH1 is being updated (vary Y shift) whilst CH2 is held. Press Hold Display and check

that both channels are now held, and remove input signal as final confirmation.

18. Window trigger

Connect test signal to CH1, and adjust amplitude to give 2 divisions deflection about mid-screen (check on Level Trigger). Select Window Trigger, and gradually increase and reduce input amplitude and confirm that traces are triggered when amplitude exceeds +1 or -1 division approx, and that trace is frozen for smaller amplitudes.

MAINTENANCE

Guarantee

The equipment supplied by Farnell Instruments Ltd., is guaranteed against defective material and faulty manufacture for a period of twelve months from the date of despatch. In the case of material or components employed in the equipment but not manufactured by us, we allow the customer the period of any guarantee extended to us.

The equipment has been carefully inspected and submitted to comprehensive tests at the factory prior to despatch. If, within the guarantee period, any defect is discovered in the equipment in respect of material or workmanship and reasonably within our control, we undertake to make good the defect at our own expense subject to our standard conditions of sale. In exceptional circumstances and at the discretion of the Service Manager, a charge for labour and carriage costs incurred may be made.

Our responsibility is in all cases limited to the cost of making good the defect in the equipment itself. The guarantee does not extend to third parties, nor does it apply to defects caused by abnormal conditions of working, accident, misuse, neglect or wear and tear.

In the event of difficulty, or apparent circuit malfunction, it is advisable to telephone (or telex) the Service Department or your local Sales Engineer or Agent (if overseas) for advice before attempting repairs.

For repairs it is recommended that the complete unit be returned to:-

The Service Department,

Farnell Instruments Ltd.,

Osborn House, Sandbeck Way,

Wetherby, West Yorkshire LS22 4DH. Tel: 0937 61961 Telex 557294

Please ensure adequate care is taken with packing and arrange insurance cover against transit damage or loss. If repairs are to be attempted by the customer these should be undertaken only by personnel conversant with this type of equipment.

ANALOGUE BOARD (A.Bd)

SK1

		L.Bd PL1
1	DOT TRIG	21
2	CH1 ENABLE	22
3	$\overline{\text{STORE}}$/REAL TIME	23
4	DAC LATCH ENABLE	24
5	ADC LATCH I/P ENABLE	25
6	DATA BIT 4	26
7	DATA BIT 3	27
8	DATA BIT 5	28
9	DATA BIT 2	29
10	DATA BIT 6	30
11	DATA BIT 1	31
12	DATA BIT 7	32
13	DATA BIT 0	33
14	ADC LATCH O/P ENABLE	34
15	START CONVERT	35
16	CH2 ENABLE	36
17	N.C.	37
18	SAMPLE TRIG	38
19	OV	39
20	N.C.	40

SK2

1	+12V
2	OV (A)
3	OV (A)
4	-12V
5	OV (D)
6	+5V

PINS

TP1	CH1 I/P	M.Bd PIN 27
TP2	OV	M.Bd PIN 61
TP3	CH2 I/P	M.Bd PIN 66
TP4	OV	M.Bd PIN 63
TP5	5MHz CLOCK	T.Bd PIN 17
TP6	OV	T.Bd PIN 18
TP7	Y O/P	M.Bd PIN 88
TP8	OV	M.Bd PIN 87

LOGIC BOARD (L.Bd)

PL1

1	OSC ENABLE	T.Bd SK1 PIN 20
2	POWER ON RESET	19
3	CS DISPLAY MEMORY	18
4	SYSTEM CYCLE RAW	17
5	R/$\overline{\text{W}}$ DELAY MEMORY	16
6	LINK TO PIN 21	15
7	SYSTEM CYCLE BUFFER	14
8	MSB DETECT	13
9	WRITE TIMEBASE	12
10	READ COUNT LOAD	11
11	LINK TO PIN 25	10
12	NORMAL TIMEBASE	9
13	[illegible]	8
14	CHOPPER DISABLE	7
15	WINDOW TRIGGER	6
16	$\overline{\text{SINGLE}}$/DUAL	5
17	NORMAL DISPLAY OFF = LO	4
18	$\overline{\text{CH2 OFF}}$	3
19	$\overline{\text{CH1 OFF}}$	2
20	STORE TIMEBASE	1
21	LINK TO PIN 6	A.Bd SK1 PIN 1
22	CH1 ENABLE	2
23	$\overline{\text{STORE}}$/REAL TIME	3
24	DAC LATCH I/P ENABLE	4
25	LINK TO PIN 11	5
26	DATA BIT 4	6
27	DATA BIT 3	7
28	DATA BIT 5	8
29	DATA BIT 2	9
30	DATA BIT 6	10
31	DATA BIT 1	11
32	DATA BIT 7	12
33	DATA BIT 0	13
34	READ/$\overline{\text{WRITE}}$ DELAY MEMORY	14
35	START CONVERT	15
36	CH2 ENABLE	16
37	N.C.	17
38	WRITE TIMEBASE	18
39	OV	19
40	N.C.	20

SK1

1	TRIG LEVEL	T.Bd TP 21
2	OV	T.Bd TP 22
3	NO CON.	M.Bd PIN 59
4	RAMP TO X-AMP	M.Bd PIN 31

SK2

1	OV
2	+5V

TP1	ARM LED A
TP2	ARM LED K
TP3	TRIG LED K
TP4	TRIG LED A

SK3 Bt. 4 on

1. Wr. Ctr CLEAR I/P
2. $\overline{\text{HOLD}}$ DISPLAY
3. NORMAL Wr. Ctr. CLR.
4. WRITE ADDRESS LAB.
5. WRITE Ctr 2^{10} O/P
6. WRITE Ctr Clk I/P
7. WRITE Ctr Clk DRIVE
8. MODE CONTROL SGL/DUAL
9. $\overline{\text{PLOT}}$ ACTIVE
10. $\overline{\text{CS}}$ DISP MEM
11. +5V
12. OV

TRIGGER BOARD (T.Bd)

SK1

1	STORE TIMEBASE	L.Bd PL1 PIN 20
2	$\overline{\text{CH1}}$ OFF	19
3	$\overline{\text{CH2}}$ OFF	18
4	NORMAL DISP. OFF = LO	17
5	$\overline{\text{SINGLE}}$/DUAL	16
6	WINDOW TRIG	15
7	CHOPPER DISABLE	14
8	OV	13
9	NORMAL TIMEBASE	12
10	DATA LATCH	11
11	READ COUNT LOAD	10
12	WRITE TIMEBASE	9
13	M.S.B. DETECT	8
14	BUFFER SYSTEM CYCLE	7
15	DOT JOIN TRIG	6
16	R/$\overline{\text{W}}$ DELAY MEMORY	5
17	SYSTEM CYCLE	4
18	CS DISPLAY MEMORY	3
19	POWER ON RESET	2
20	STORE ENABLE	1

PL1

1	X-Y MODE X O/P	M.Bd A1
2	N.C.	A2
3	CH2 TRIG I/P	A3
4	+12V	A4
5	N.C.	A5
6	N.C.	A6
7	N.C.	A7
8	N.C.	A8
9	CH2 ENABLE	A9
10	CH1 ENABLE	A10
11	N.C.	A11
12	CHOPPER BLANK	A12

PL2

1	N.C.	M.Bd B1
2	N.C.	B2
3	N.C.	B3
4	-12V	B4
5	OV (A)	B5
6	OV (A)	B6

PINS

TP1	EXT TRIG I/P	F/P
TP2	OV	F/P
TP3	CH1 TRIG I/P	M.Bd PIN 50
TP6	50Hz	M.Bd PIN 68
TP10	CAL SK	F/P
TP15	+5V	
TP16	OV (D)	
TP17	5MHz CLOCK	A. Bd TP5
TP18	OV	A. Bd TP6

SK2

1	$\overline{\text{Ch1 off}}$	Ch1 AC-DC SW
2	$\overline{\text{Ch2 off}}$	Ch2 AC-DC SW
3	[illegible]	ATT Bd PIN 13
4	TRIGGER O/P	[illegible]

SK3

1	N.C.
2	[illegible] — TRIG LEVEL POT
3	[illegible] — TRIG LEVEL POT
4	WIPER — TRIG LEVEL POT

TRACED	ISS	DATE	MOD No	ISS	DATE	MOD No
	A	20.4.83	—			
CHECKED	B	12.1.84	—			
DRAWN LDG						

NOTE:- M.Bd. MAIN BOARD. ATT. Bd. ATTENUATOR BOARD. F/P FRONT PANEL.

USED ON	FACTORY NO	SERIAL NO FROM	SERIAL NO TO
DTS12	965	51	

NOTE: CAPACITOR VALUES GIVEN IN µF, RESISTOR VALUES IN Ω UNLESS OTHERWISE STATED

FARNELL INSTRUMENTS LTD. WETHERBY, YORKS.

TITLE: DTS12 CONNECTION LIST

DRAWING No: 2ZV0965204

SHEET 1 OF 1 SHEETS

ANALOGUE BOARD(A.BD)

SK1		L.BD PL1
1	DOT TRIG	21
2	CH1 ENABLE	22
3	STORE/REAL TIME	23
4	DAC LATCH ENABLE	24
5	ADC LATCH I/P ENABLE	25
6	DATA BIT 4	26
7	DATA BIT 3	27
8	DATA BIT 5	28
9	DATA BIT 2	29
10	DATA BIT 6	30
11	DATA BIT 1	31
12	DATA BIT 7	32
13	DATA BIT 0	33
14	ADC LATCH O/P ENABLE	34
15	START CONVERT	35
16	CH2 ENABLE	36
17	N.C.	37
18	SAMPLE TRIG	38
19	0V	39
20	N.C.	40

SK2	
1	+12V
2	0V(A)
3	0V(A)
4	-12V
5	0V(D)
6	+5V

PINS		
TP1	CH1 I/P	M.BD PIN 27
TP2	0V	M.BD PIN 61
TP3	CH2 I/P	M.BD PIN 66
TP4	0V	M.BD PIN 63
TP5	5MHz CLOCK	T. BD PIN 17
TP6	0V	T. BD PIN 18
TP7	Y O/P	M.BD PIN 88
TP8	0V	M.BD PIN 87

TRIGGER BOARD (T.BD)

SK1		L.BD PL1 PIN
1	N.C.	20
2	CH1 OFF	19
3	CH2 OFF	18
4	NORMAL DISP. OFF = LO	17
5	SINGLE/DUAL	16
6	WINDOW TRIG	15
7	CHOPPER DISABLE	14
8	0V	13
9	N.C.	12
10	DATA LATCH	11
11	READ COUNT LOAD	10
12	WRITE TIMEBASE	9
13	M.S.B. DETECT	8
14	BUFFER SYSTEM CYCLE	7
15	DOT JOIN TRIG	6
16	R/W DELAY MEMORY	5
17	SYSTEM CYCLE	4
18	CS DISPLAY MEMORY	3
19	POWER ON RESET	2
20	STORE ENABLE	1

SK2		
1	CH1 OFF	CH1 AC-DC SW
2	CH2 OFF	CH2 AC-DC SW
3	CH1 POS'N POT DISABLE	ATT BD PIN 13
4	TRIGGER O/P	L.BD SK1 PIN 1

SK3		
1	N.C.	
2	CCW	TRIG LEVEL POT
3	CW	
4	WIPER	

PL1		
1	X-Y MODE X O/P	M.BD A1
2	RAMP TO MAIN BOARD	A2
3	CH2 TRIG I/P	A3
4	+12V	A4
5	N.C.	A5
6	N.C.	A6
7	N.C.	A7
8	N.C.	A8
9	CH2 ENABLE	A9
10	CH1 ENABLE	A10
11	N.C.	A11
12	CHOPPER BLANK	A12

PL2		
1	N.C.	M.BD B1
2	N.C.	B2
3	N.C.	B3
4	-12V	B4
5	0V(A)	B5
6	0V(A)	B6

PINS		
TP1	EXT TRIG I/P	F/P
TP2	0V	F/P
TP3	CH1 TRIG I/P	M.BD PIN 50
TP6	50 HZ	M.BD PIN 68
TP10	CAL SK	F/P
TP15	+5V	
TP16	0V(D)	
TP17	5MHZ CLOCK	A.BD TP5
TP18	0V	A.BD TP6

LOGIC BOARD (L.BD)

SK1		
1	TRIG LEVEL	T.BD TP 21
2	0V	T.BD TP 22
3	NO CON.	M.BD PIN 59
4	N.C.	

SK2	
1	0V
2	+5V

PINS	
TP1	ARM LED A
TP2	ARM LED K
TP3	TRIG LED K
TP4	TRIG LED A

LOGIC BOARD(L.BD) AND I/O BOARD (I/O BD)

PL1		
1	OSC ENABLE	T.BD SK1 PIN 20
2	POWER ON RESET	19
3	CS DISPLAY MEMORY	18
4	SYSTEM CYCLE RAW	17
5	R/W DELAY MEMORY	16
6	LINK TO PIN 21	15
7	SYSTEM CYCLE BUFFER	14
8	MSB DETECT	13
9	WRITE TIMEBASE	12
10	READ COUNT LOAD	11
11	LINK TO PIN 25	10
12	N.C.	9
13	LOGIC 0V	8
14	CHOPPER DISABLE	7
15	WINDOW TRIGGER	6
16	SINGLE/DUAL	5
17	NORMAL DISPLAY OFF = LO	4
18	CH2 OFF	3
19	CH1 OFF	2
20	N.C.	1
21	LINK TO PIN 6	A.BD SK1 PIN 1
22	CH1 ENABLE	2
23	STORE/REAL TIME	3
24	DAC LATCH I/P ENABLE	4
25	LINK TO PIN 11	5
26	DATA BIT 4	6
27	DATA BIT 3	7
28	DATA BIT 5	8
29	DATA BIT 2	9
30	DATA BIT 6	10
31	DATA BIT 1	11
32	DATA BIT 7	12
33	DATA BIT 0	13
34	READ/WRITE DELAY MEMORY	14
35	START CONVERT	15
36	CH2 ENABLE	16
37	N.C.	17
38	WRITE TIMEBASE	18
39	0V	19
40	CS DISP. M. DRIVE	20
41	HOLD	
42	HOLD DRIVE	
43	R/W DISP. M. DRIVE	
44	SWEEP ACTIVE	
45	N.C.	
46	ADDRESS SELECT	
47	WRITE CLEAR DRIVE	
48	WRITE CLEAR	
49	ADDRESS LSB	
50	HOLD CH2	

I/O BOARD (I/O BD)

SK1 (IEEE)	
1	DIO1
2	DIO5
3	DIO2
4	DIO6
5	DIO3
6	DIO7
7	DIO4
8	DIO8
9	EOI
10	REN
11	DAV
12	OVD
13	NRFD
14	OVD
15	NDAC
16	0V
17	IFC
18	OVD
19	SRQ
20	OVD
21	ATN
22	OVD
23	N.C.
24	OVD

SK2 (BBC μC)	
1	N.C.
2	ABF
3	N.C.
4	ASTB
5	ST5
6	PA0
7	N.C.
8	PA1
9	N.C.
10	PA2
11	N.C.
12	PA3
13	N.C.
14	PA4
15	N.C.
16	PA5
17	N.C.
18	PA6
19	N.C.
20	PA7

SK3	
1	+5V
2	OVD
3	-12V
4	CURSOR OUT
5	OVA
6	+12V

SK4	
1	X OUTPUT
2	Y OUTPUT
3	OVA
4	PEN LIFT

TRACED	ISS	DATE	MOD No	ISS	DATE	MOD No
	A	26/3/85				
CHECKED						
DRAWN JC.						

USED ON: DTS 12T F10030

NOTE:
CAPACITOR VALUES GIVEN IN μF
RESISTOR VALUES IN Ω
UNLESS OTHERWISE STATED

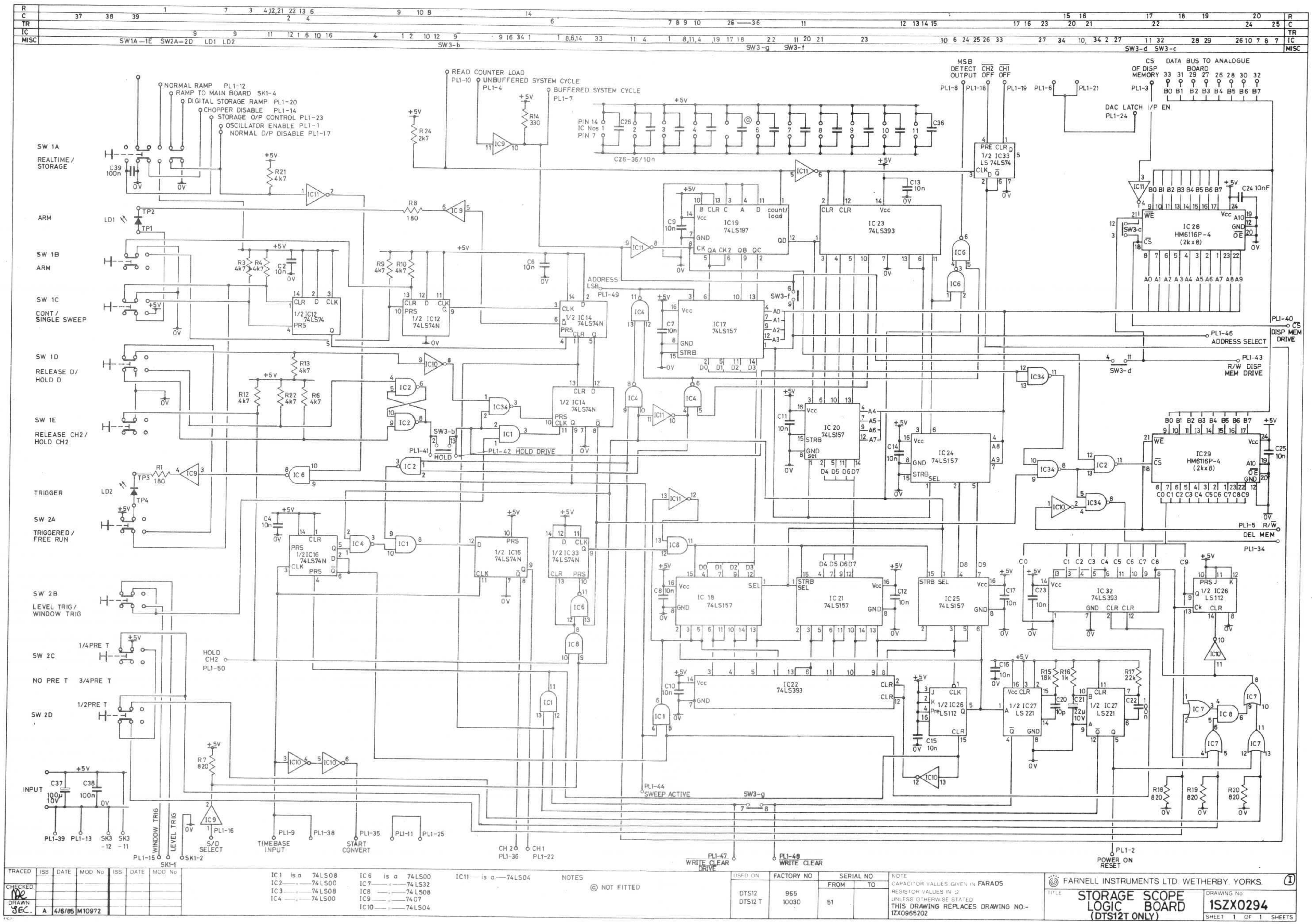
FARNELL INSTRUMENTS LTD. WETHERBY, YORKS.

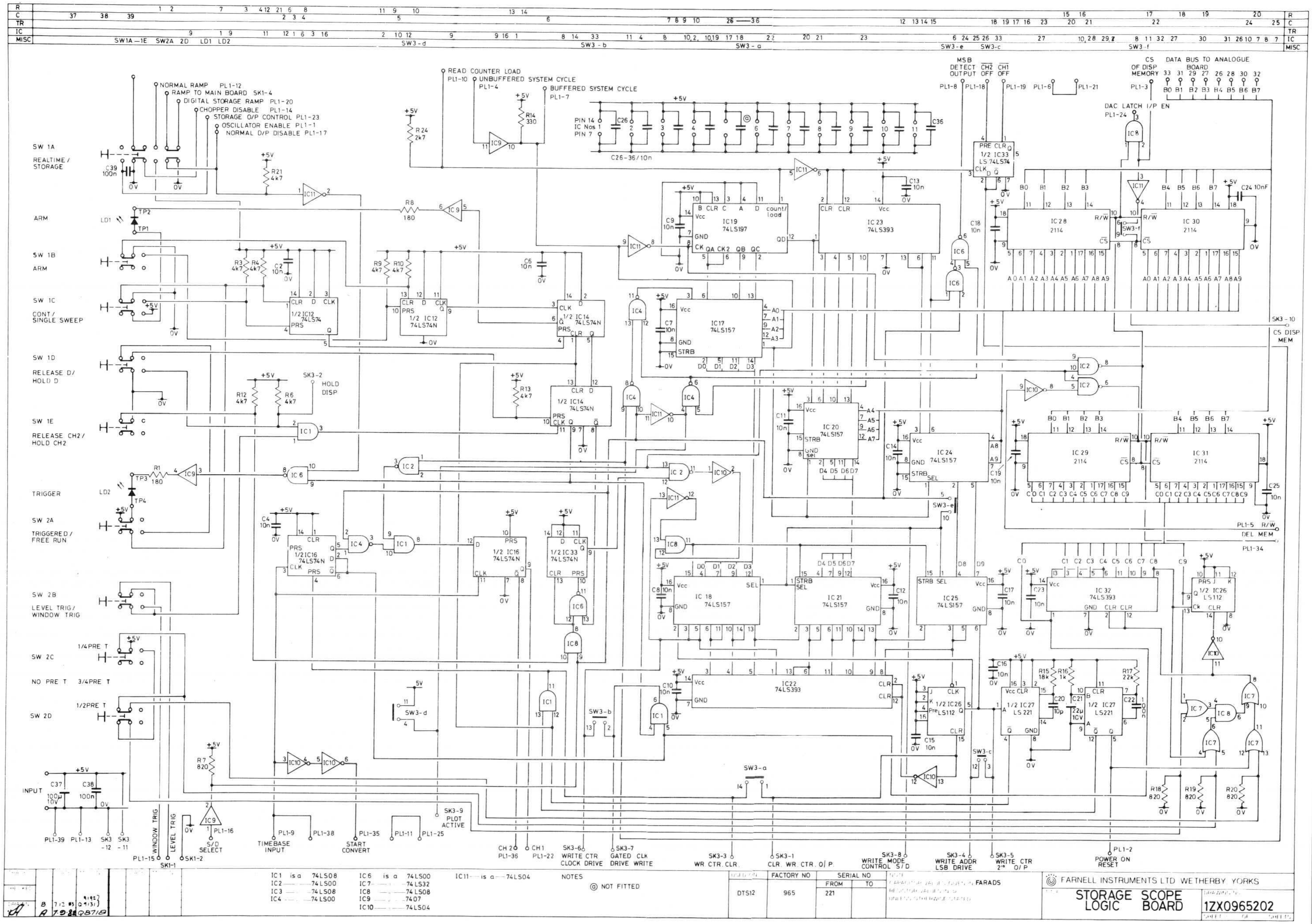
TITLE: DTS 12T CONNECTION LIST

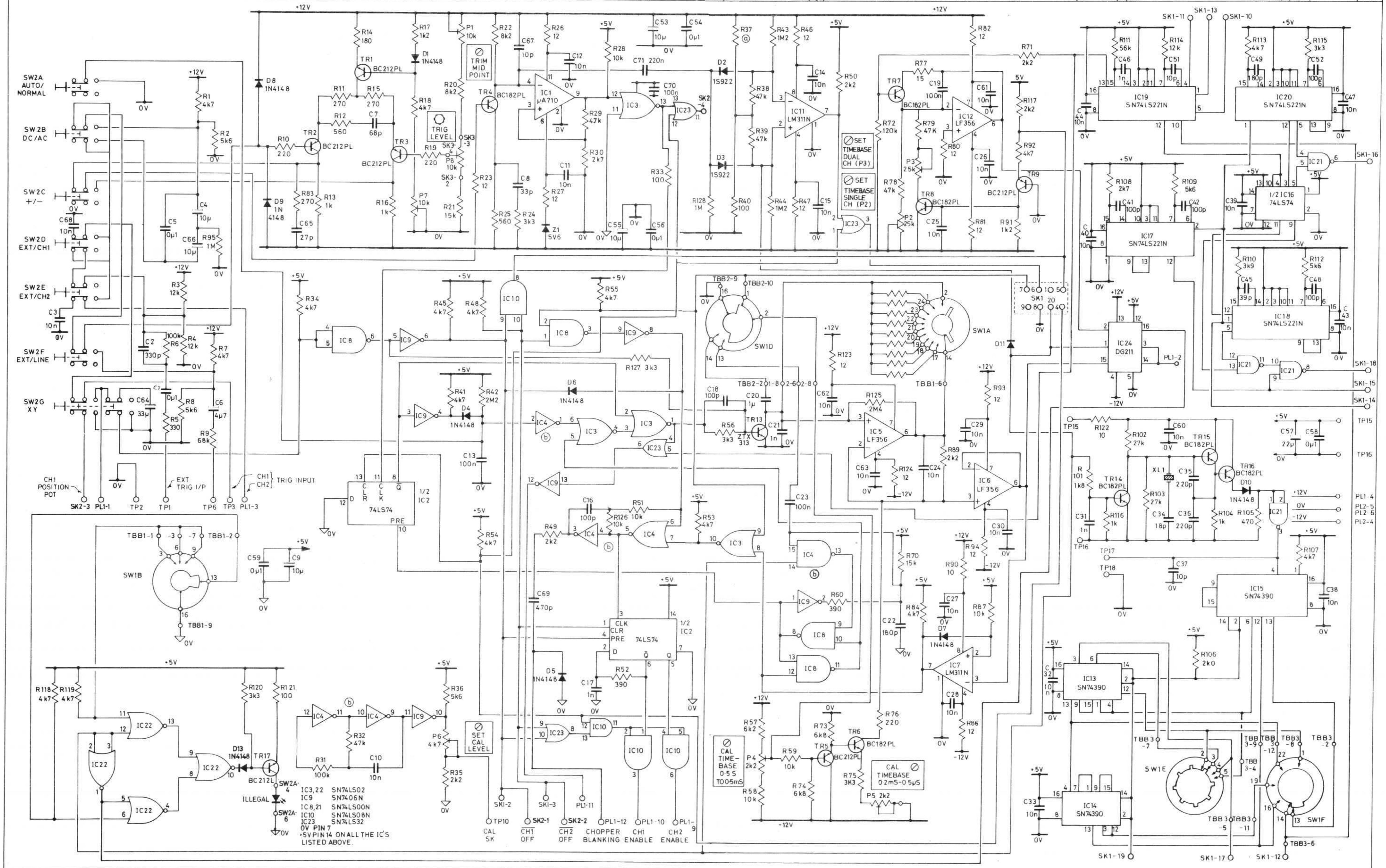
DRAWING No: 2ZV10030200

SHEET 1 OF 1 SHEETS

A4RQUE 5893/83


SW 1A
REALTIME / STORAGE
ARM
SW 1B
ARM
SW 1C
CONT / SINGLE SWEEP
SW 1D
RELEASE D / HOLD D
SW 1E
RELEASE CH2 / HOLD CH2
TRIGGER
SW 2A
TRIGGERED / FREE RUN
SW 2B
LEVEL TRIG / WINDOW TRIG
SW 2C
NO PRE T 3/4PRE T
SW 2D
INPUT
NORMAL RAMP PL1-12
RAMP TO MAIN BOARD SK1-4
DIGITAL STORAGE RAMP PL1-20
CHOPPER DISABLE PL1-14
STORAGE O/P CONTROL PL1-23
OSCILLATOR ENABLE PL1-1
NORMAL D/P DISABLE PL1-17
READ COUNTER LOAD PL1-10
UNBUFFERED SYSTEM CYCLE PL1-4
BUFFERED SYSTEM CYCLE PL1-7
C26-36/10n
MSB DETECT OUTPUT
CH2 OFF
CH1 OFF
CS OF DISP MEMORY
DATA BUS TO ANALOGUE BOARD
DAC LATCH I/P EN PL1-24
ADDRESS LSB PL1-49
ADDRESS SELECT PL1-46
CS DISP MEM DRIVE PL1-40
R/W DISP MEM DRIVE PL1-43
HOLD PL1-41
PL1-42 HOLD DRIVE
HOLD CH2 PL1-50
R/W PL1-5
DEL MEM PL1-34
SWEEP ACTIVE PL1-44
WRITE CLEAR DRIVE PL1-47
WRITE CLEAR PL1-48
POWER ON RESET PL1-2
TIMEBASE INPUT
START CONVERT
S/D SELECT
WINDOW TRIG
LEVEL TRIG
CH 2 PL1-36
CH 1 PL1-22
IC1 is a 74LS08
IC2 — 74LS00
IC3 — 74LS08
IC4 — 74LS00
IC6 is a 74LS00
IC7 — 74LS32
IC8 — 74LS08
IC9 — 7407
IC10 — 74LS04
IC11 — is a — 74LS04
NOTES
@ NOT FITTED
TRACED
CHECKED
DRAWN
A 4/6/85 M10972
USED ON
DTS12
DTS12 T
FACTORY NO
965
10030
SERIAL NO
FROM
TO
51
NOTE
CAPACITOR VALUES GIVEN IN FARADS
RESISTOR VALUES IN Ω
UNLESS OTHERWISE STATED
THIS DRAWING REPLACES DRAWING NO:-
1ZX0965202
FARNELL INSTRUMENTS LTD. WETHERBY, YORKS.
TITLE
STORAGE SCOPE LOGIC BOARD
(DTS12T ONLY)
DRAWING No
1SZX0294
SHEET 1 OF 1 SHEETS


SW 1A REALTIME / STORAGE
NORMAL RAMP PL1-12
RAMP TO MAIN BOARD SK1-4
DIGITAL STORAGE RAMP PL1-20
CHOPPER DISABLE PL1-14
STORAGE O/P CONTROL PL1-23
OSCILLATOR ENABLE PL1-1
NORMAL O/P DISABLE PL1-17
ARM
SW 1B ARM
SW 1C CONT / SINGLE SWEEP
SW 1D RELEASE D/ HOLD D
SW 1E RELEASE CH2/ HOLD CH2
TRIGGER
SW 2A TRIGGERED / FREE RUN
SW 2B LEVEL TRIG/ WINDOW TRIG
SW 2C
NO PRE T
SW 2D
INPUT
READ COUNTER LOAD PL1-10
UNBUFFERED SYSTEM CYCLE PL1-4
BUFFERED SYSTEM CYCLE PL1-7
PIN 14 IC Nos 1 PIN 7
C26-36/10n
MSB DETECT OUTPUT
CS OF DISP MEMORY
DATA BUS TO ANALOGUE BOARD
DAC LATCH I/P EN PL1-24
SK3-10 CS DISP MEM
PL1-5 R/W
DEL MEM PL1-34
HOLD DISP SK3-2
PLOT ACTIVE SK3-9
TIMEBASE INPUT PL1-9
START CONVERT PL1-35
S/D SELECT PL1-16
WINDOW TRIG
LEVEL TRIG
CH 2 PL1-36
CH1 PL1-22
SK3-6 WRITE CTR CLOCK DRIVE
SK3-7 GATED CLK DRIVE WRITE
SK3-3 WR CTR CLR
SK3-1 CLR WR CTR O/P
SK3-8 WRITE MODE CONTROL S/D
SK3-4 WRITE ADDR LSB DRIVE
SK3-5 WRITE CTR 2^n O/P
PL1-2 POWER ON RESET
IC1 is a 74LS08
IC2 74LS00
IC3 74LS08
IC4 74LS00
IC6 is a 74LS00
IC7 74LS32
IC8 74LS08
IC9 7407
IC10 74LS04
IC11 is a 74LS04
NOTES
◎ NOT FITTED
FACTORY NO 965
SERIAL NO FROM 221 TO
DTS12
FARADS
FARNELL INSTRUMENTS LTD WETHERBY YORKS
STORAGE SCOPE LOGIC BOARD
1ZX0965202



R	118,119	6,8,4,3,1,2,95,7	10,83,34,13,	11,12,	14	15	16	17,18,19,45,41,20,21,42,23,22,24, 25	26 27	29,30,28,55,	127	33	128	37,40,38,39,43,44 46,47	50,123 125, 72 78,77,79	80, 82,81 93 117,92,71,91	122,111,108	114 109	110 113	112 115

R	5	9	120 121	31 32	36,35 48 54	49	126	52 51	53	56 57 58	59 74 73	76 75 124 70,84	89 90,86 94,87	101 116 102	103 106	104 105	107

C	3 68	64,2,1,5 66,4 6	59	65,9	7 10	13	67 8 69 12 11 16 17 71	55,53,70 56 54	18	20 21	14 23 15,62,60 63	22	19 24,25 28,27,29,26,61 30	33,40,44,32,31,	46,41	34,51,60,42,37,35,36	39,45,49	57,58,52,48,47,43,38

TR	17	2	1	3 12	4	13	5	6	7	8	9	14	15 16

MISC	IC22	D8, D9, D13	IC4, 8, 2	IC9, 4 D1 P7, 6	D4 P1, 8	IC10, 4, 8, 3, 1 Z1 D5 D6	IC23 IC3, 10,	D2, 3	IC3	P4	IC11, 4, 8, 9	P5 IC5	P2, 3 IC12	D7 IC7	IC6	D11	IC13, 14	IC17, 19, 24	D10 IC15, 18, 16, 20, 21

TRACED	ISS	DATE	MOD No	ISS	DATE	MOD No
	A	6/6/85	M10972			
CHECKED						
DRAWN JEC.						

NOTES
ⓐ NOT FITTED.
ⓑ +5V PIN 16, 0V PIN 8 MC14572

	FACTORY NO	SERIAL NO	
		FROM	TO
DTS12	965		
DTS12T	10030	51	

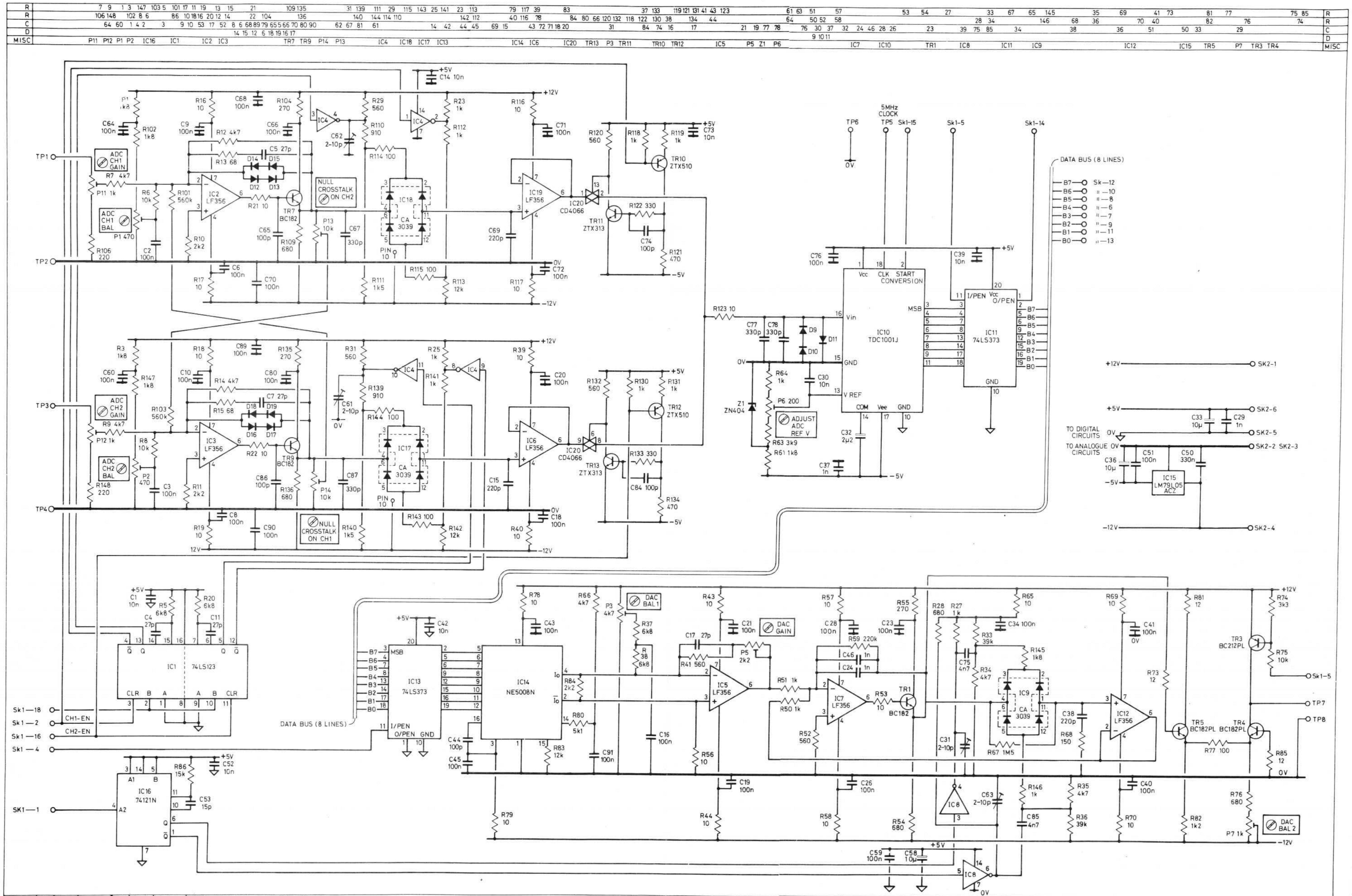
FARADS

THIS DRAWING REPLACES DRAWING NO:- 1ZX0965201

FARNELL INSTRUMENTS LTD WETHERBY YORKS

TRIGGER CIRCUIT DTS-12 1SZX0295

SHEET 1 OF 1 SHEETS



TRACED	ISS	DATE	MOD No	ISS	DATE	MOD No	NOTE
CHECKED	A	2-12-82					IC20, PIN7 TO -5V, PIN14 TO +5V
DRAWN SA							

USED ON	FACTORY NO	SERIAL NO FROM	SERIAL NO TO
DTS12	965	51	170

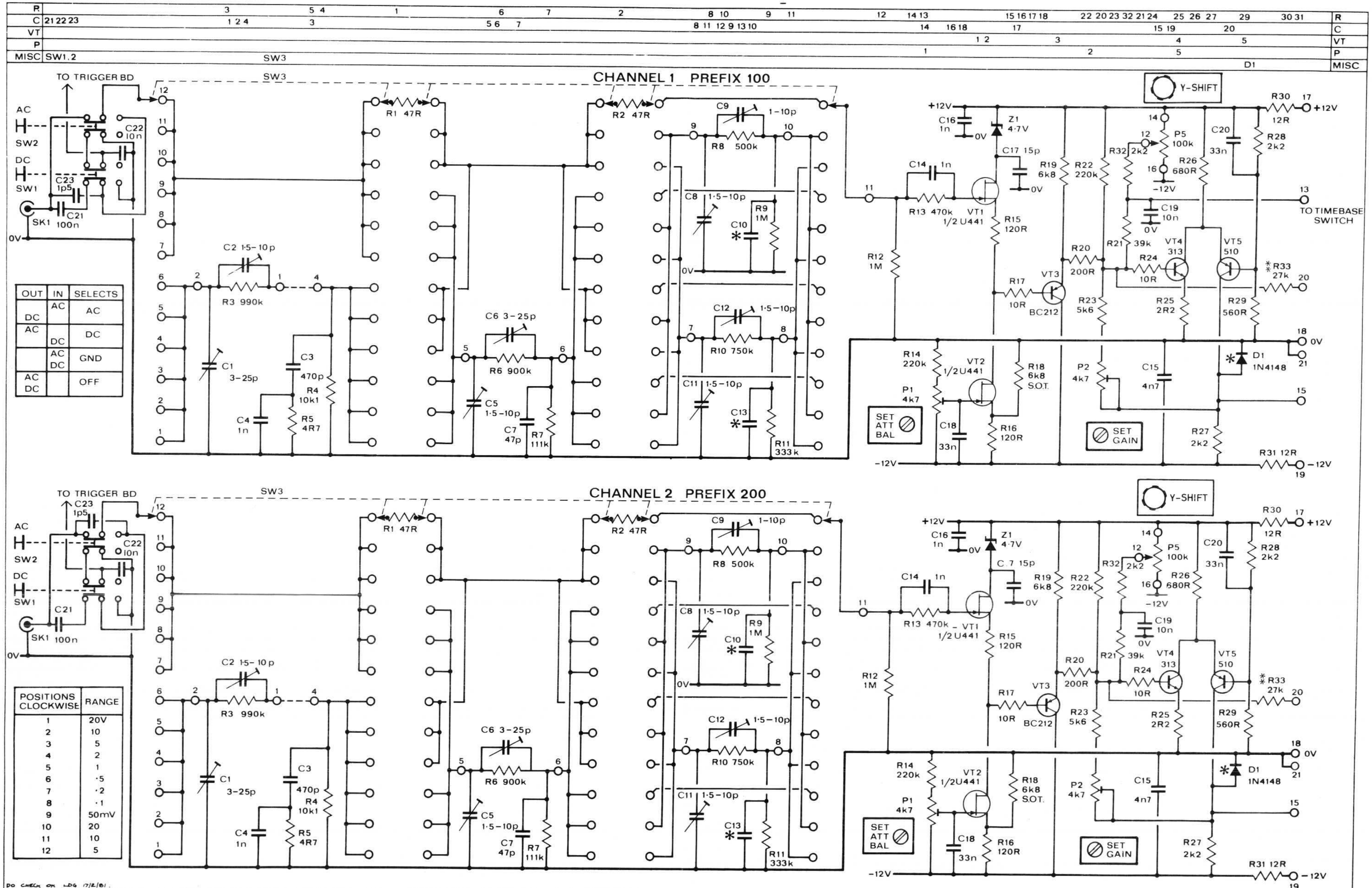
NOTE
CAPACITOR VALUES GIVEN IN FARAD
RESISTOR VALUES IN Ω
UNLESS OTHERWISE STATED
DIODES ARE 1N4148

FARNELL INSTRUMENTS LTD. WETHERBY, YORKS.

TITLE
ANALOGUE BOARD CIRCUIT DIAGRAM

DRAWING No
12X0965203

SHEET OF SHEETS



OUT	IN	SELECTS
DC	AC	AC
AC	DC	DC
	AC DC	GND
AC DC		OFF

POSITIONS CLOCKWISE	RANGE
1	20V
2	10
3	5
4	2
5	1
6	·5
7	·2
8	·1
9	50mV
10	20
11	10
12	5

DO CHECK ON LDG 17/2/81.

TRACED	ISS	DATE	MOD No	ISS	DATE	MOD No
	A	15·5·81	6668, 7040 7178.			
CHECKED Pa. L.	B	11·11·81	Q7200			
	C	20.6.82	7040 7781 7782			
DRAWN SH	D	21·2·83	Q8385			
	E	7·12·83	Q8989			

✱ NOT FITTED

SW3 SHOWN IN THE MOST CLOCKWISE POSITION (5mV).

⁑ ONLY FITTED ON DT12C

USED ON	FACTORY NO	SERIAL NO. FROM	TO
DT12/5	858	1401	
DTV12-14	859	100	
DTC12	966	51	
DTS12	976	51	

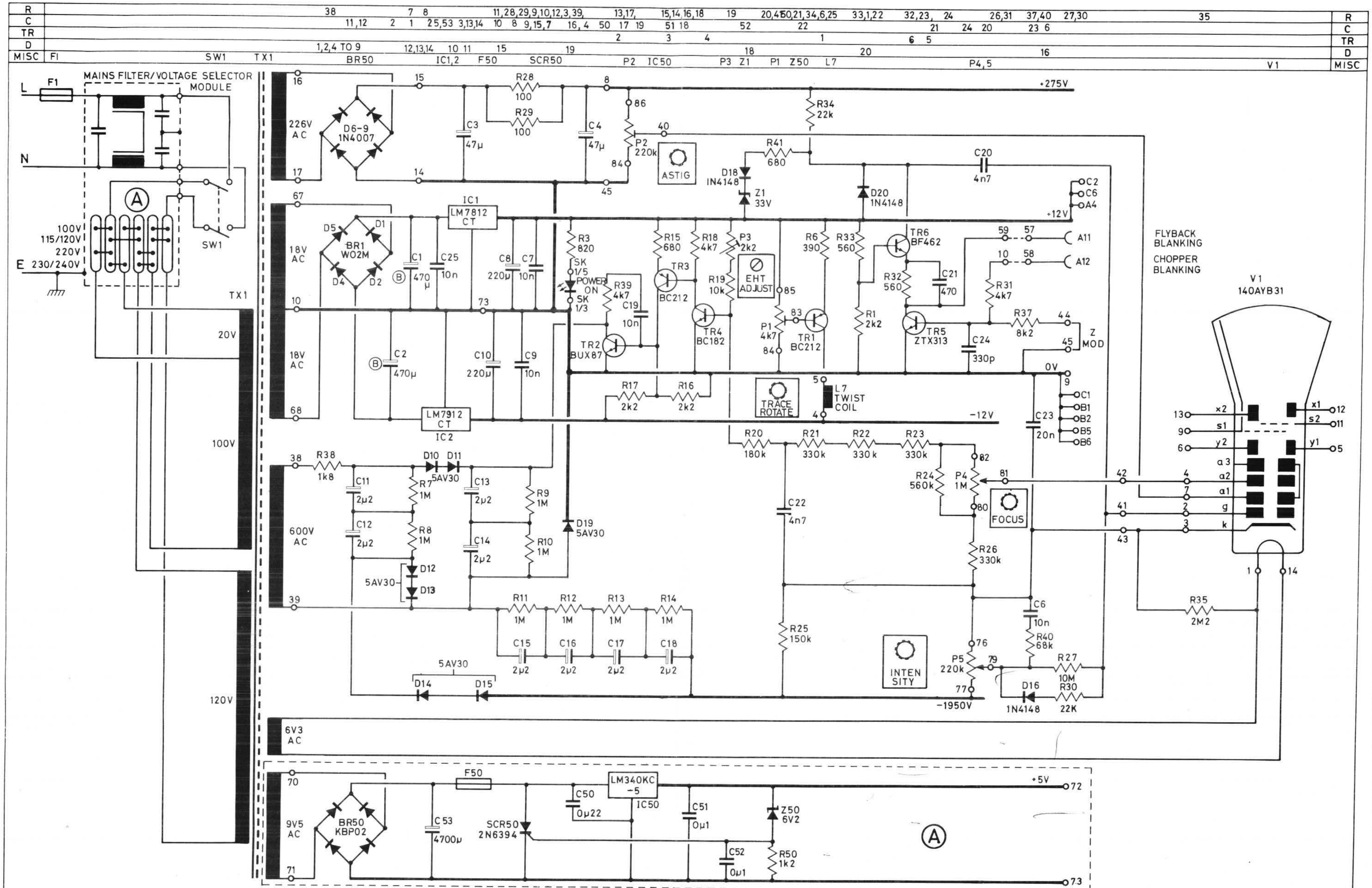
NOTE
CAPACITOR VALUES GIVEN IN FARADS
RESISTOR VALUES IN Ω
UNLESS OTHERWISE STATED

FARNELL INSTRUMENTS LTD. WETHERBY, YORKS.

TITLE ATTENUATORS & Y-AMPS. CIRCUIT DIAGRAM

DRAWING No 2SZX0144

SHEET 1 OF 1 SHEETS



TRACED	ISS	DATE	MOD No	ISS	DATE	MOD No
CHECKED	C	6.1.84	CR0734			
DRAWN	B	20.12.83	9478			
P.G.F.	A	11.1.83	~			

ALL COMPONENTS PREFIX 700

NOTE
(A) ONLY FITTED ON DTS12
(B) C1, C2 ARE 1000μ ON DTS12

USED ON	FACTORY NO	SERIAL NO FROM	SERIAL NO TO
DTS12	965	51	
DT12-5	858	1901	
DTV12-14	859	946	
DTC12	966	656	

NOTE
CAPACITOR VALUES GIVEN IN F
RESISTOR VALUES IN Ω
UNLESS OTHERWISE STATED

FARNELL INSTRUMENTS LTD. WETHERBY, YORKS.

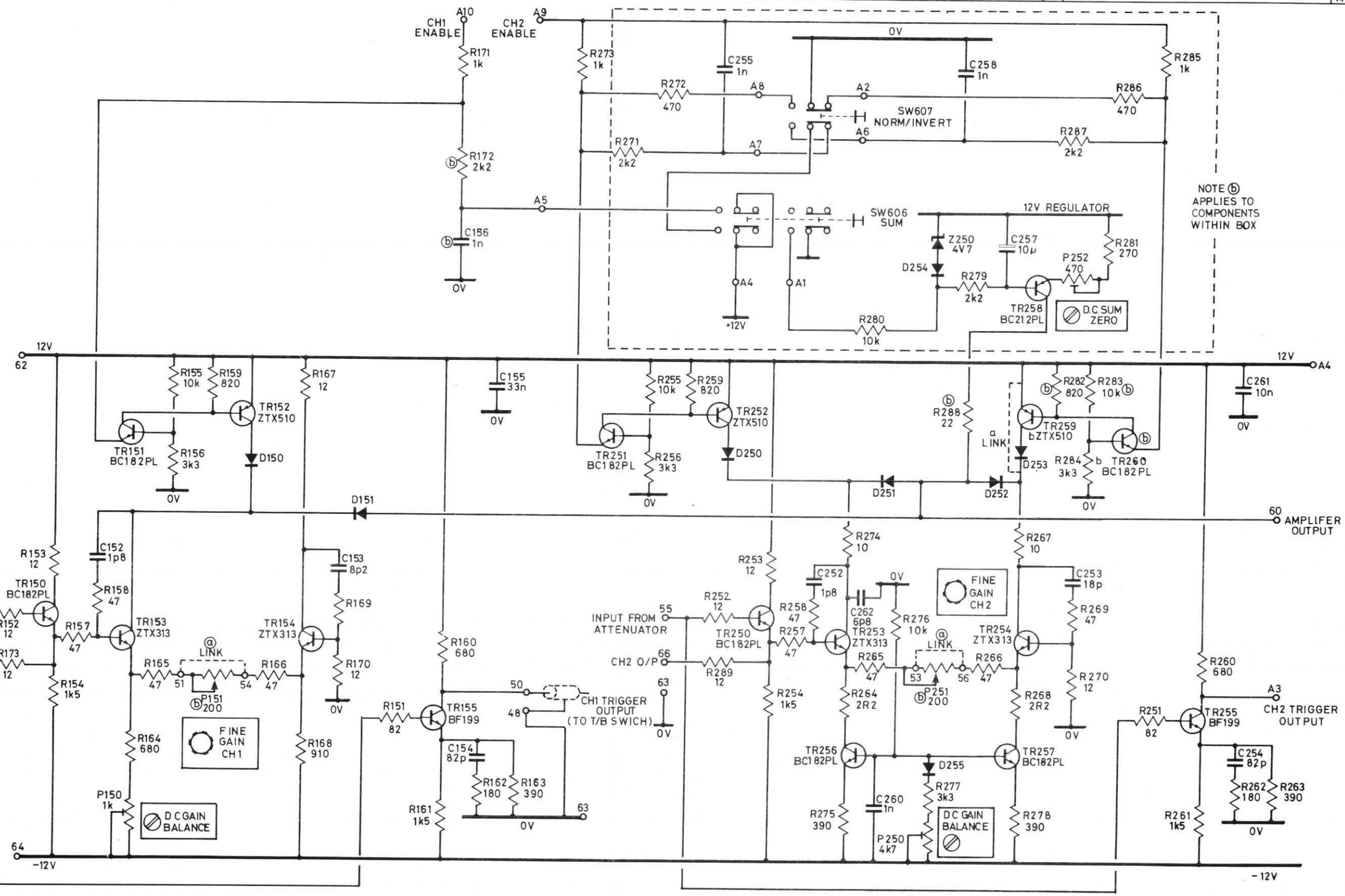
TITLE
SCOPE POWER SUPPLY

DRAWING No
2/SZX/0205

SHEET OF SHEETS

GAF 3956 78

R	152 153 154 156 155 159 167 169 151 161 160 162 163 272 271 272 252 253 258 275 264 265 277 279 266 268 278 269 270 284 285 260 261 262 263	R
R	173 157 158 164 165 166 168 170 172 171 256 255 259 289 254 257 274 280 276 288 267 282 284 281 251	R
C	152 153 156 154 155 255 252 260 258 257 253 261 254	C
TR	150 151 153 152 154 155 251 252 250 253 256 257 254 268 259 258 260 255	TR
MISC	P150 P151 D150 D151 D250 SW607 D251 SW606 Z250 D254 P250 D255,252,253 P252	MISC



TRACED	ISS	DATE	MOD No.	ISS	DATE	MOD No.
	A	17·1·83				
CHECKED	B	23.12.83	9727			
	B	6.1.84	CR0734			
DRAWN P.G.F.						

NOTES
ⓐ FITTED ON DT12/5 AND DTS12
ⓑ NOT FITTED ON DT12/5 AND DTS12

USED ON:	FACTORY NO	SERIAL NO FROM	SERIAL NO TO
DT12-5	858	1901	
DTV12-14	859	946	
DTC12	966	656	
DTS12	965	51	

NOTE:
CAPACITOR VALUES GIVEN IN µF
RESISTOR VALUES IN Ω
UNLESS OTHERWISE STATED
DIODES ARE 1N4148 UNLESS OTHERWISE STATED
03 INDICATES SOLDER PIN NUMBER.

FARNELL INSTRUMENTS LTD. WETHERBY, YORKS.

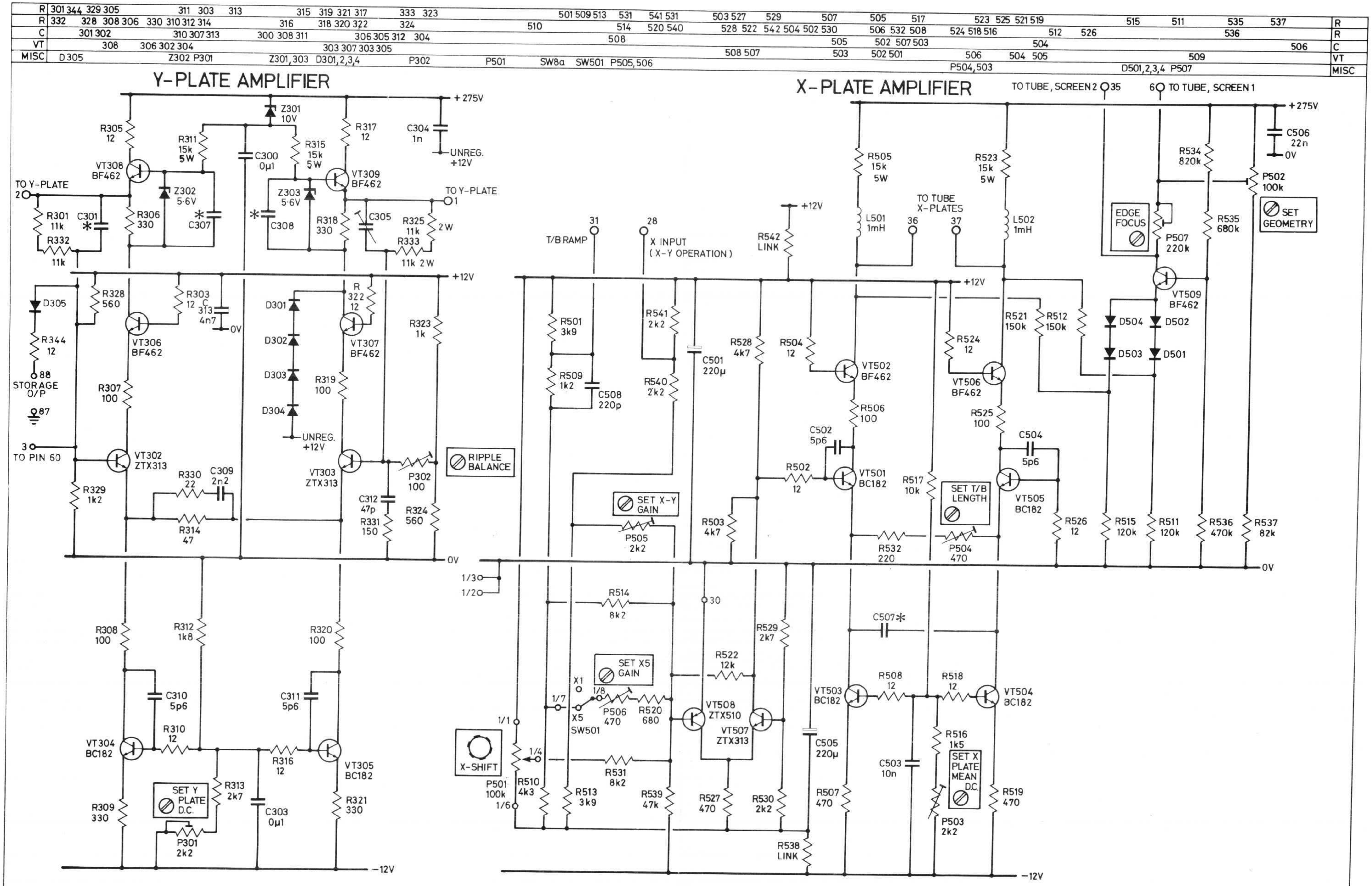
TITLE: Y AMPLIFIERS WITH FINE ADJUSTMENT CCT.DIA.

DRAWING No. 2/SZX/0206

SHEET OF SHEETS

FICD.

GAF 3956/78



TRACED	ISS	DATE	MOD No	ISS	DATE	MOD No
CHECKED	A	17·1·83	7555 7782			
DRAWN P.G.F.	B	7·12·83	8744 8836			

ALL DIODES ARE 1N4148.

*NOT FITTED.

USED ON	FACTORY NO	SERIAL NO FROM	TO
DT12-5	858	1901	
DTV12-14	859	946	
DTC12	966	656	
DTS12	965	51	

NOTE:
CAPACITOR VALUES GIVEN IN FARADS
RESISTOR VALUES IN Ω
UNLESS OTHERWISE STATED
03 INDICATES SOLDER PIN NUMBER
1/3 INDICATES SKT1 PIN 3

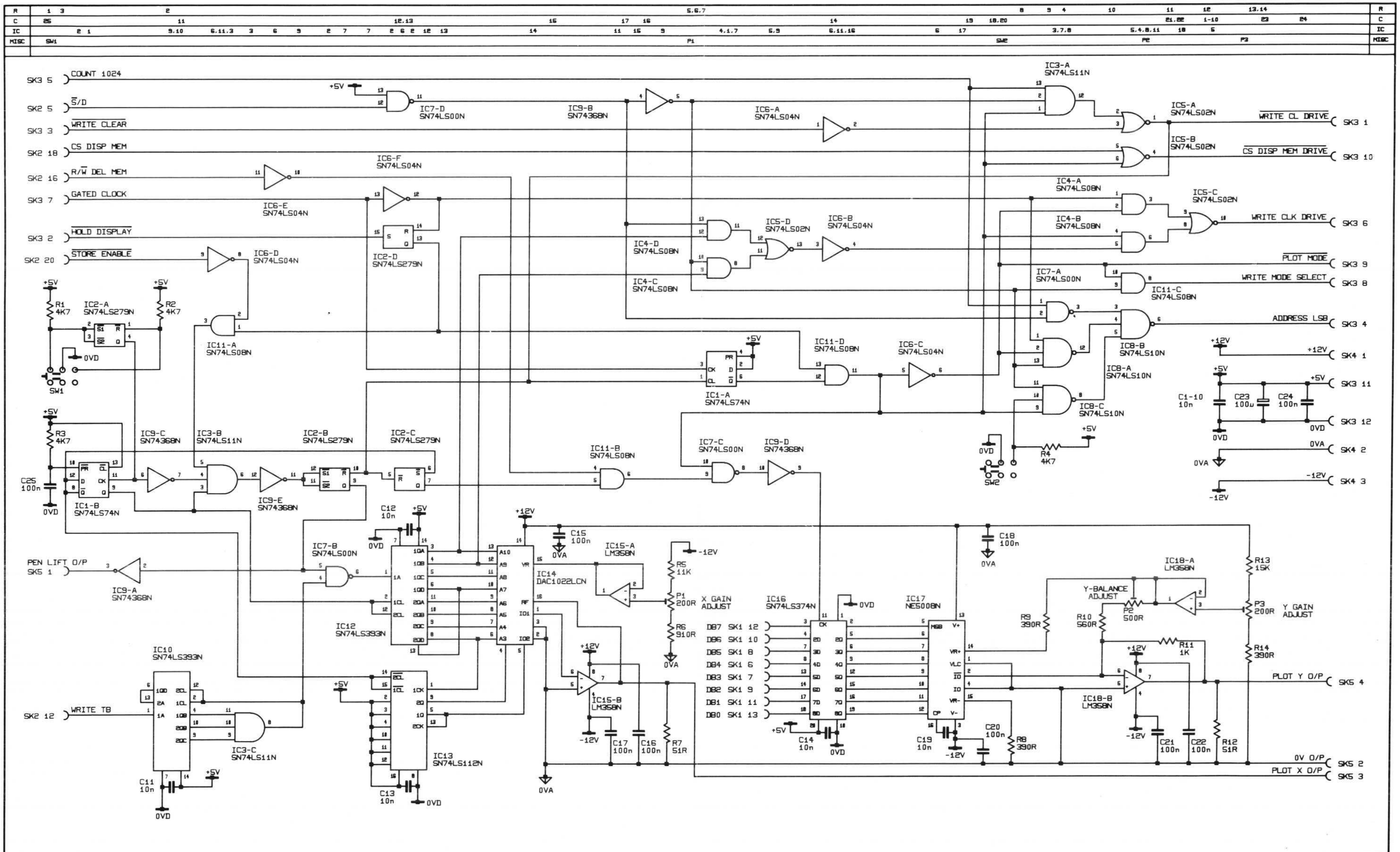
FARNELL INSTRUMENTS LTD. WETHERBY, YORKS.

TITLE

X&Y PLATE AMPS. CIRCUIT DIAGRAM

DRAWING No **2/SZX/0207**

SHEET 1 OF 1 SHEETS



IC	1	2	3	4	5	6	7	8	9	11
+5V	14	16	14	14	14	14	14	14	16	14
0V	7	8	7	7	7	7	7	7	8	7

ISSUE	A
DATE	3/11/83
MOD. NO.	-
CHECKED	[signature]
NAME	L.D.G

USED ON: DTS 12P F990

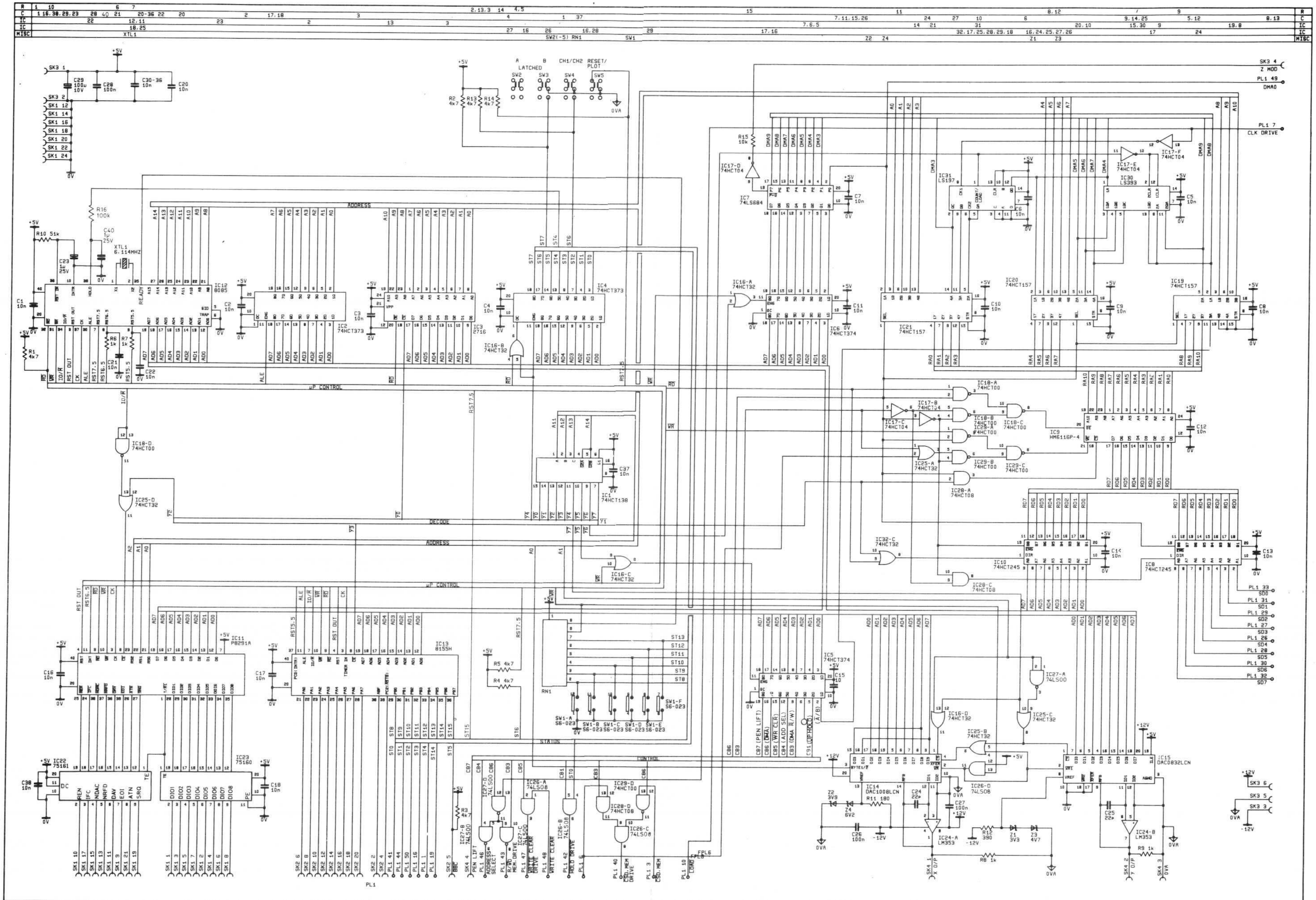
NOTES:
ALL CAPACITOR VALUES IN F.
ALL RESISTOR VALUES IN OHMS.
C1-10 ARE DECOUPLING CAPACITORS FOR IC1-9 AND IC11
UNLESS OTHERWISE STATED.

FARNELL INSTRUMENTS LTD., SANDBECK WAY, WETHERBY, YORKS. LS22 4DH

TITLE: X-Y PLOTTER OUTPUT BOARD CIRCUIT DIAGRAM

DRAWING NO. CZX0990200

SHEET 1 OF 1 SHEETS.



ISSUE	PA	A	B
DATE	11/8/84	18.3.85	20/11/85
MOD. NO.		-	
CHECKED		PB2	
DRAWN	P.G.F	JAE	

USED ON: DTS12T F10030

NOTES: ALL CAPACITOR VALUES IN F. ALL RESISTOR VALUES IN OHMS. UNLESS OTHERWISE STATED.

FARNELL INSTRUMENTS LTD., SANDBECK WAY, WETHERBY, YORKS. LS22 4DH

TITLE: COMPUTER INTERFACE DIA

DRAWING NO. CZX10030201

SHEET 1 OF 1 SHEETS.

F A R N E L L I N S T R U M E N T S L T D

DATE : 1/10/86 — P A R T S L I S T

MAIN UNIT ITEM NUMBER : 15DTS12P — DESCRIPTION : GEN/X *DTS12P * 990

IMPORTANT EXPLANATION - PLEASE READ BEFORE ORDERING PARTS.
DUE TO LIMITATIONS IN THE NUMBER OF CHARACTER SPACES AVAILABLE THE INFORMATION IN THE CIRCUIT REFERENCE FIELD HAS BEEN ABBREVIATED AND THE FOLLOWING NOTES ARE PROVIDED AS A GUIDE TO IT'S INTERPRETATION:

1. WHERE A COMPONENT IS USED MORE THAN ONCE ON AN ASSEMBLY THE ALPHABETIC PORTION OF THE CIRCUIT REFERENCE FOR ITS SECOND AND SUBSEQUENT LOCATIONS HAS BEEN OMITTED; EG. THE CIRCUIT REFERENCE INFORMATION FOR A COMPONENT LOCATED AT R1 AND R6 WILL APPEAR AS R1 6
2. THE CIRCUIT REFERENCE NUMBERS ARE PRESENTED IN ASCENDING DECADE BLOCKS DELIMITED BY COLONS: SECOND AND SUBSEQUENT NUMBERS WITHIN A DECADE BLOCK REPRESENT ONLY THE UNIT VALUE OF THE LOCATION (THE TENS AND HUNDREDS VALUES BEING IMPLIED); EG. FOR A COMPONENT LOCATED AT R54,R57,R59,R82,R87,R102,R110, AND R112 THE CIRCUIT REFERENCE ENTRY WILL BE R54 7 9:82 7:102:10 2
3. WHERE COMPONENTS ARE USED IN A SERIES OF NEIGHBOURING CIRCUIT REFERENCE LOCATIONS THE CIRCUIT REFERENCE NUMBERS ARE REPRESENTED AS INCLUSIVE BLOCKS USING A HYPHEN; EG. A COMPONENT LOCATED AT R16,R19,R21,R24,R25,R26,R31,R37,R38,R39,R40,R44 AND R46 WILL BE REPRESENTED AS R16 9:21 4-6:31 37-40 4 6 (AN EXCEPTION TO THE RULES OCCURS WHEN A SERIES CROSSES A DECADE BLOCK IN WHICH CASE THE TENS VALUE IS INSERTED.
4. COMMENTS ARE PRECEDED BY A SEMICOLON.

WHEN ORDERING REPLACEMENT PARTS PLEASE BE SURE TO QUOTE THE PART NUMBER PROVIDED.

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
25DTS12P		END ITEM: FIN/A *DTS12P
35DTS12		CASING: CAS/C *DTS12
4NDTSCP		ASSEMBLY: SUB/D *CHASSIS DTS12P
4NDTSFPP		ASSEMBLY: SUB/B *F/PANEL DTS12P
4SDTATN		ASSEMBLY: SUB/B *DUAL ATTN
4SDTSS1		ASSEMBLY: SUB/A *CH1 ATTN SW
5SDTATN1		CCT BOARD: CPS/I *CH1 ATTN DTS12
RC12R2025	2R2 5% MUL CR25	R25
RC14R7025	4R7 5% MUL CR25	R5
RC6470K25	470KR 5% MUL CR25	R13
RM210R025	10R 1% MUL MR25	R17:24
RM212R025	12R 1% MUL MR25	R30 1
RM3120R25	120R 1% MUL MR25	R15 6
RM3560R25	560R 1% MUL MR25	R29
RM3680R25	680R 1% MUL MR25	R26
RM42K2025	2K2R 1% MUL MRS25	R27 8:32
RM45K6025	5K6R 1% MUL MR25	R18:23
RM46K8025	6K8R 1% MUL MR25	R19
RM510K1H8	10K1R 1% 100PPM H8	R4
RM539K025	39KR 1% MUL MR25	R21
RM6111KH8	111KR 1% 100PPM H8	R7
RM6220K25	220KR 1% MUL MR25	R14:22
RM6333KH8	333KR 1% 100PPM H8	R11
RM6500KH8	500KR 1% 100PPM H8	R8
RM6750KH8	750KR 1% 100PPM H8	R10
RM6900KH4	900KR 1% 100PPM H4	R6
RM6990KH4	990KR 1% 100PPM H4	R3 FITTED ON BACK OF CB
RM71M00H8	1MOR 1% 100PPM H8	R9:12
RM3200R25	200R 1% MUL MR25	R20
CC247P0N642	47PF 100V 683-34479	C7
CC41K00831H	1K0PF ERI 831/HIK	C4:14
CC510K0861	10KPF ERI 861T/25	C19:22
CC215P0N642	15PF 100V 683-10159	C17
CV210P	10PF 109-2991-010 BLU	C2 5 8:11 2
CC11P50861	1P5F ERI 861/P100	C23 FITTED ON BACK OF CB
CV2325P	3-25PF 109-2991 GRN	C1 6 9
CF0U100NMKS3	0.1UF 100V WIM MKS3	C16
CF44K70NFKS2	4K7PF 100V WIM FKS2	C15
PC44K7010V	POT 4K7R PIH PT10V	P1 2
VF441	TRANS U441 FET *STATIC	VT1-2
VT212PL	TRANSISTOR BC212PL	VT3
VTX313	TRANSISTOR ZTX313	VT4
VTX510	TRANSISTOR ZTX510	VT5
CAOMIT	CAPACITORS OMITTED	C10 3
DAOMIT	DIODES OMITTED	D1

F A R N E L L I N S T R U M E N T S L T D

DATE : 1/10/86 P A R T S L I S T

MAIN UNIT ITEM NUMBER : 15DTS12P DESCRIPTION : GEN/X *DTS12P * 990

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
BC0684	2SZ/B *DT125 ATT *	PREFIX 100
DZ14V700W5	ZPD4.7 ITT	Z1
SB0057	4ST/A *INPUT DTS12	SW1-2
CF0U100T352	0.1UF 400V 368-50104	C21 FITTED ON BACK OF CB
RM527K025	27KR 1% MUL MR25	R33
TP15080	CB PIN MR15080 TUC	C/S X20 T/S X1
DGJPAD100	DIODE JPAD/100 SIL	D2
CF3470PNFKP2	470PF 100V 5% FKP2	C3
CF522K0NFKS3	22KPF 100V WIM FKS3	C18:20
RM247R025	47R 1% MUL MR25	R1 2
SW0036	3ST/B *WAFER SCOPE	SW3
4SDTSS2		ASSEMBLY: SUB/A *CH2 ATTN SW
5SDTATN2		CCT BOARD: CPS/I *CH2 ATTN DTS12
RC12R2025	2R2 5% MUL CR25	R25
RC6470K25	470KR 5% MUL CR25	R13
RM210R025	10R 1% MUL MR25	R17:24
RM212R025	12R 1% MUL MR25	R30 1
RM3120R25	120R 1% MUL MR25	R15 6
RM3560R25	560R 1% MUL MR25	R29
RM3680R25	680R 1% MUL MR25	R26
RM42K2025	2K2R 1% MUL MRS25	R27 8:32
RM45K6025	5K6R 1% MUL MR25	R18:23
RM46K8025	6K8R 1% MUL MR25	R19
RM510K1H8	10K1R 1% 100PPM H8	R4
RM539K025	39KR 1% MUL MR25	R21
RM6111KH8	111KR 1% 100PPM H8	R7
RM6220K25	220KR 1% MUL MR25	R14:22
RM6333KH8	333KR 1% 100PPM H8	R11
RM6500KH8	500KR 1% 100PPM H8	R8
RM6750KH8	750KR 1% 100PPM H8	R10
RM6900KH4	900KR 1% 100PPM H4	R6
RM6990KH4	990KR 1% 100PPM H4	R3 FITTED ON BACK OF CB
RM71M00H8	1M0R 1% 100PPM H8	R9:12
RM3200R25	200R 1% MUL MR25	R20
RC14R7025	4R7 5% MUL CR25	R5
CC247P0N642	47PF 100V 633-34479	C7
CC41K00831H	1K0PF ERI 831/H1K	C4:14
CC510K0861	10KPF ERI 861T/25	C19:22
CV210P	10PF 109-2991-010 BLU	C2 5 8:11 2
CV2325P	3-25PF 109-2991 GRN	C1 6 9
CF0U100NMKS3	0.1UF 100V WIM MKS3	C16
CF44K70NFKS2	4K7PF 100V WIM FKS2	C15
CC215P0N642	15PF 100V 633-10159	C17
CC11P50861	1P5F ERI 361/P100	C23 FITTED ON BACK OF CB
CAOMIT	CAPACITORS OMITTED	C10 3
PC44K7010V	POT 4K7R PIH PT10V	P1 2
VF441	TRANS U441 FET *STATIC	VT1-2
VT212PL	TRANSISTOR BC212PL	VT3
VTX313	TRANSISTOR ZTX313	VT4
VTX510	TRANSISTOR ZTX510	VT5
DAOMIT	DIODES OMITTED	D1
MP075BLKVX	PVC SLV VX.75 BLK PER	C23
BC0684	2SZ/B *DT125 ATT *	PREFIX 200
DZ14V700W5	ZPD4.7 ITT	Z1
SB0057	4ST/A *INPUT DTS12	SW2
CF0U100T352	0.1UF 400V 368-50104	C21 FITTED ON BACK OF CB
RM527K025	27KR 1% MUL MR25	R33
TP15080	CB PIN MR15080 TUC	C/S X21
DGJPAD100	DIODE JPAD/100 SIL	D2
CF3470PNFKP2	470PF 100V 5% FKP2	C3
CF522K0NFKS3	22KPF 100V WIM FKS3	C18:20
RM247R025	47R 1% MUL MR25	R1 2
SW0036	3ST/B *WAFER SCOPE	SW3
4NDTSTB		ASSEMBLY: SUB/B *TIME BASE DTS12
BC098	C /B *DTS SW/TB *S12B	FREE ISS TO SUPPLIER
SW0051C	3ST/A *SW LESS CB N-OR	SWITCH LESS CB
SB0084	3ST/A *TIMES 5 DTS12	SW501
5NDTSA		CCT BOARD: CPS/E *ANLG DTS IP AMP
BC097	C /D *DTS12 ANA *P32B	3
RM210R025	10R 1% MUL MR25	R16-19:21 2:39:40:116 7:23
RM268R025	68R 1% MUL MR25	R13 5
RM3220R25	220R 1% MUL MR25	R106

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MAIN UNIT ITEM NUMBER : 15DTS12P DESCRIPTION : GEN/X *DTS12P * 990

FARNELL PART NUMBER	DESCRIPTION	*---------- CIRCUIT REFERENCE ----------*
RM3330R25	330R 1% MUL MRS25	R122:33
RM3470R25	470R 1% MUL MR25	R121:34
RM3560R25	560R 1% MUL MR25	R29:31:120:32
RM3680R25	680R 1% MUL MR25	R109:36
RM41K0025	1K0R 1% MUL MR25	R23 5:112 8 9:30 1:41
RM41K5025	1K5R 1% MUL MR25	R111:40
RM41K8025	1K8R 1% MUL MR25	R1 3:102:47
RM42K2025	2K2R 1% MUL MRS25	R10
RM44K7025	4K7R 1% MUL MR25	R7 9:12 4
RM510K025	10KR 1% MUL MR25	R6 8
CC227P0N642	27PF 100V 683-34279	C5 7
CC3100PN642	100PF 100V 683-34101	C65:74:34 6
CC3330PN642	330PF 100V 683-58331	C67:87
CF510K0N2MIN	10KPF 100V WIM FKS2MIN	C73
CF44K70NFKS2	4K7PF 100V WIM FKS2	C70
CF0U100NMKS3	0.1UF 100V WIM MKS3	C2 3 6 8-10 8:20:60 6 8:71 2:88-90
DG4148	DIODE 1N4148	D12-19
VT182PL	TRANSISTOR BC182PL	TR7 9
VTX313	TRANSISTOR ZTX313	TR11 3
VTX510	TRANSISTOR ZTX510	TR10 2
VA356TC	IC UAF356TC/LF356N	IC2 3 6:19
VA3039	INT CCT CA3039 RCA	IC17 8
VD4066CN	IC CD4066CN *STATIC	IC20
PC3470R10V	POT 470R PIH PT10V	P1 2
PC41K0010V	POT 1K0R PIH PT10V	P11 2
PC510K010V	10KR PIH PT10V	P13 4
5NDTSAL		CCT BOARD: CPS/E *ANLOG LOGIC DTS
RM210R025	10R 1% MUL MR25	R43 4:53 56-58:65 9:70 8 9
RM212R025	12R 1% MUL MR25	R73:81 5
RM3220R25	220R 1% MUL MR25	R148
RM3560R25	560R 1% MUL MR25	R41:52
RM3680R25	680R 1% MUL MR25	R28:54:76
RM41K0025	1K0R 1% MUL MR25	R27:50 1:64:146
RM41K2025	1K2R 1% MUL MR25	R82
RM41K8025	1K8R 1% MUL MR25	R61:145
RM42K2025	2K2R 1% MUL MRS25	R11:84
RM43K3025	3K3R 1% MUL MR25	R74
RM43K9025	3K9R 1% MUL MR25	R63
RM44K7025	4K7R 1% MUL MR25	R34 5:66
RM46K8025	6K8R 1% MUL MR25	R5:20:37 8
RM510K025	10KR 1% MUL MR25	R75
RM515K025	15KR 1% MUL MR25	R86
RM539K025	39KR 1% MUL MR25	R33 6
RM6220K25	220KR 1% MUL MR25	R59
RM6560K30	560KR 2% MUL MR30	R101 3
RC71M5025	1M5R 5% MUL CR25	R67
RM3150R25	150R 1% MUL MR25	R68
RM3100R25	100R 1% MUL MR25	R77
RM3270R25	270R 1% MUL MR25	R55
RM45K1025	5K1R 1% MUL MR25	R80
RM512K025	12KR 1% MUL MR25	R83
CC215P0N642	15PF 100V 683-10159	C53
CC227P0N642	27PF 100V 683-34279	C4:11 7
CC3100PN642	100PF 100V 683-34101	C44
CC3330PN642	330PF 100V 683-58331	C77 8
CE12U20KD	2U2F 50V DUB K	C32
CE210U0GM	100F 25V MUL 030	C33 6:58
CF510K0N2MIN	10KPF 100V WIM FKS2MIN	C1:14:30 9:42:52
CF44K70NFKS2	4K7PF 100V WIM FKS2	C75 P05 C35 P08
CF41K00NFKS2	1K0PF 100V WIM FKS2	C24 9:37:46
CF0U330NMKS	0.33UF 100V WIM MKS4	C50
CF0U100NMKS3	0.1UF 100V WIM MKS3	C16 9:21 3 6 8:34:40 1 3 5:51 9:64:76:91
CV2210P803	V/CAP 2/10PF 80311109	C61-63
DG4148	DIODE 1N4143	D9-11
DZ12V500W3	ZN404 FER	Z1
PC41K0010V	POT 1K0R PIH PT10V	P7
PC42K2010V	POT 2K2R PIH PT10V	P5
PC44K7010V	POT 4K7R PIH PT10V	P3
PM3200R63P	200R SPL 63P	P6
VA1001J	IC TDC1001J8C *STATIC	IC10
VA356TC	IC UAF356TC/LF356N	IC5 7:12
VA3039	INT CCT CA3039 RCA	IC9

F A R N E L L I N S T R U M E N T S L T D

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MAIN UNIT ITEM NUMBER : 15DTS12P DESCRIPTION : GEN/X *DTS12P * 990

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
VA5008N	IC NE5008N *STATIC	IC14
VA79L05ACZ	INT CCT LM79L05ACZ	IC15
VD74LS123N	INT CCT SN74LS123N	IC1
VD74LS373N	INT CCT SN74LS373N	IC11
VD7406N	INT CCT SN7406N	IC4 8
VD74121N	INT CCT SN74121N TEX	IC16
VT212PL	TRANSISTOR BC212PL	TR3
VT182PL	TRANSISTOR BC182PL	TR1 4 5
CAOMIT	CAPACITORS OMITTED	C31
VP1A	TRANSITOR PAD TW1A	Z1
TP15080	CB PIN MR15080 TUC	C/S X8
VD74LS374N	INT CCT DM74LS374N	IC13
CF3220PNFKP2	220PF 100V 5% FKP2	C38
RM3910R25	910R 1% MUL MR25	R110:39
RM3100R25	100R 1% MUL MR25	R114 5:43 4
RM3270R25	270R 1% MUL MR25	R104:35
RM512K025	12KR 1% MUL MR25	R113:42
TBM3906PR	6W 2420-09-75-1061	SK2
TIH2520NR1L	20W HEAD M52-1220-460	SK1
CF3220PNFKP2	220PF 100V 5% FKP2	C15:69
5NDTSTG		CCT BOARD: CPS/L *TRIGGER DTS12
BC095	C /D *DTS12 TRGR*P323	B
RM210R025	10R 1% MUL MR25	R122
RM212R025	12R 1% MUL MR25	R23 6 7:46 7:80-82 6:90 3 4:123 4
RM215R025	15R 1% MUL MR25	R77:129
RM3100R25	100R 1% MUL MR25	R33:40:121
RM3180R25	180R 1% MUL MR25	R14
RM3220R25	220R 1% MUL MR25	R10 9:76
RM3270R25	270R 1% MUL MR25	R11 5:83
RM3330R25	330R 1% MUL MRS25	R5
RM3390R25	390R 1% MUL MR25	R52:60
RM3470R25	470R 1% MUL MR25	R105
RM3560R25	560R 1% MUL MR25	R12:24
RM41K0025	1K0R 1% MUL MR25	R13 6:54:104:16
RM41K2025	1K2R 1% MUL MR25	R17
RM41K8025	1K8R 1% MUL MR25	R101
RM42K0025	2K0R 1% MUL MR25	R106
RM42K2025	2K2R 1% MUL MRS25	R35:49:50:71:89:91:117
RM42K7025	2K7R 1% MUL MR25	R30:108
RM43K3025	3K3R 1% MUL MR25	R25:56:115:20 7
RM43K9025	3K9R 1% MUL MR25	R75:110
RM44K7025	4K7R 1% MUL MR25	R1 7:18:34:41 5 8:53 5:84:92:107:13 8 9
RM45K6025	5K6R 1% MUL MR25	R2 8:36:109:12
RM46K8025	6K8R 1% MUL MR25	R73 4
RM48K2025	8K2R 1% MUL MR25	R20 2
RM510K025	10KR 1% MUL MR25	R23:51 8 9:87:126
RM512K025	12KR 1% MUL MR25	R3 4:114
RM515K025	15KR 1% MUL MR25	R21:70
RM527K025	27KR 1% MUL MR25	R102 3
RM547K025	47KR 1% MUL MR25	R29:32 8 9:78 9
RM556K025	56KR 1% MUL MR25	R111
RM568K025	68KR 1% MUL MR25	R9
RM6100K25	100KR 1% MUL MR25	R6:31
RM6120K25	120KR 1% MUL MR25	R72
RC71M2025	1M2R 5% MUL CR25	R43 4
RC72M2025	2M2R 10% MUL CR25	R42
RM72M40H2	2M4R 1% 100PPM H2	R125
CC210PON642	10PF 100V 683-10109	C37:51
CC218PON642	18PF 100V 683-10189	C34
CC233PON642	33PF 100V 683-34339	C8
CC239PON642	39PF 100V 683-34399	C45
CC268PON642	68PF 100V 683-34689	C7
CC3100PN642	100PF 100V 683-34101	C16 8:41 2 8:52
CC3330PN642	330PF 100V 683-58331	C2
CC3220PN683	220PF 100V 683-58221	C35 6
CF0U100R352	0.1UF 250V 368-40104	C1:13
CF0U100NMKS3	0.1UF 100V WIM MKS3	C5:19:23:54 6 8 9:70
CF11U00PRNR	1UF 160V 5% RNR ICW	C20
CF41K00NFKS2	1K0PF 100V WIM FKS2	C31:46
CF510K0N2MIN	10KPF 100V WIM FKS2MIN	C3:10-12 4 5:24-30 2 3 8 9:40 3 4 7:50:60-63 8
CE210U0GM	10UF 25V MUL 030	C4 9:53 5:66
CE222U0DM	22UF 10V MUL 030	C57

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MAIN UNIT ITEM NUMBER : 15DTS12P DESCRIPTION : GEN/X *DTS12P * 990

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
VT182PL	TRANSISTOR BC182PL	TR4 6-8:14-16
VT212PL	TRANSISTOR BC212PL	TR1-3 5 9:17
DG4148	DIODE 1N4148	D1 4-13
DG922	DIODE 1S922	D2 3
VA311N	INT CCT LM311N 8PIN	IC7:11
VA356TC	IC UAF356TC/LF356N	IC5 6:12
VA710CN	INT CCT LM710CN 14PDIL	IC1
VD14572P	IC MC14572UBCP *STATIC	IC4
VD74LS00N	INT CCT SN74LS00N	IC8:21
VD74LS02N	INT CCT SN74LS02N TEX	IC3:22
VD74LS08N	INT CCT SN74LS08N	IC10
VD74LS221N	IC SN74LS221N NAT	IC17-20
VD7406N	INT CCT SN7406N	IC9
VD74LS74N	INT CCT SN74LS74N	IC2:16
VD74390N	INT CCT SN74390N	IC13-15
VX5M00	5MHZ HC18U	XL1 MC1 X1/L
VS8P	IC SKT 703-1308-010410	V
VS14L	IC SKT 703-1314-010410	V
VS16L	IC SKT 703-1316-010410	V
PC42K2010LH	2K2R PIH PT10LH	P4 5
PC44K7010LH	4K7R PIH PT10LH	P6
PC510K010LH	10KR PIH PT10LH	P1 7
PC522K010LH	22KR PIH PT10LH	P2 3
RC71M0025	1MOR 5% MUL CR25	R95:128
CC227P0N642	27PF 100V 683-34279	C65
DZ15V600W5	ZPD5.6 ITT	Z1
CC3180PN683	180PF 100V 683-58181	C22:49
SB0054	3ST/A *DTS12 TRIG 7W	SW2A-2G
TP7401	CB PIN 12W 1-163740-1	FIT T/S
TP7404	CB PIN 6W 163740-4 AMP	FIT T/S
CE14U70LM	4U7F 63V 015-90044	C6
CC3470PN630	470PF 100V 630-18471	C69
RA0MIT	RESISTORS OMITTED	R37
RM46K2025	6K2R 1% MUL MR25	R57
CC41K00N630	1K0PF 100 630-19102	C17
CE233U0FES	33UF 16V SMVB ECC	C64
MC1	CERAMIC BEAD SDP1 MET	XL1
TP15080	CB PIN MR15030 TUC	C/S X9
CF0U220NMKS4	0.22UF 100V MKS4	C71
VD74LS32N	INT CCT SN74LS32N	IC23
TBM2504PR	4W 7478-22-05-3041	SK2
TBM2512PT	12W 4094 22 05 2125	TBB1 2 3
TBM2504PS	4W 6410 22-27 2041	SK3
TIH252ONT1L	20W M52-1220-260	SK1
VTX313	TRANSISTOR ZTX313	TR13
CF41K00NFKP2	1K0PF 100V 5% FKP2	C21
CASOT	CAP SELECT ON TEST	C67
5NDTSL		CCT BOARD: CPS/F *LOGIC DTS12
BC096	C /D *DTS12 LOG *P32B	B
RM3180R25	180R 1% MUL MR25	R1 8
RM3820R25	820R 1% MUL MR25	R7:18-20
RM41K0025	1K0R 1% MUL MR25	R16
RM44K7025	4K7R 1% MUL MR25	R3 4 6 9:10 2 3:21
RM518K025	18KR 1% MUL MR25	R15
RM522K025	22KR 1% MUL MR25	R17
CC210P0N642	10PF 100V 683-10109	C20
CE222U0DM	22UF 10V MUL 030	C21
CE3100UDM	100UF 10V MUL 030	C37
CF0U100NMKS3	0.1UF 100V WIM MKS3	C22:38 9
CF510K0N2MIN	10KPF 100V WIM FKS2MIN	C2 4 6-19:23-29:31-36
SB0052	3ST/A *DTS12 LOGIC 4W	SW2
SB0053	3ST/A *DTS12 LOGIC 5W	SW1
LD134R	LED RED T1 3/4 MV5753	LED1
VD472114AP1	IC TMM314A PL-1*STATIC	IC28-31
VD7407N	INT CCT SN7407N	IC9
VD74LS00N	INT CCT SN74LS00N	IC2 4 6
VD74LS04N	INT CCT SN74LS04N	IC10 1
VD74LS08N	INT CCT SN74LS08N	IC1 8
VD74LS32N	INT CCT SN74LS32N	IC7
VD74LS74N	INT CCT SN74LS74N	IC12 4 6:33
VD74LS112N	INT CCT SN74LS112N	IC26
VD74LS157N	INT CCT SN74LS157N	IC17 8:20 1 4 5

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FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
VD74LS197N	INT CCT SN74LS197N	IC19
VD74LS221N	IC SN74LS221N NAT	IC27
VD74LS393N	INT CCT SN74LS393N	IC22 3:32
VS14L	IC SKT 703-1314-010410	V
VS16L	IC SKT 703-1316-010410	V
VS18L	IC SKT 703-1318-010410	V
RM42K7025	2K7R 1% MUL MR25	R24
LD134G	LED GRN T1 3/4 MV64530	LED2
TBM3902PR	2W 2420-09-75-1021	SK2
TBM2504PR	4W 7478-22-05-3041	SK1
RM3330R25	330R 1% MUL MRS25	R14
TP15080	CB PIN MR15080 TUC	C/S X4
TL675191T	14W PROG HEADER	SW3
TBM2512PT	12W 4094 22 05 2125	SK3
CC510K0861	10KPF ERI 861T/25	C
RC3100R16	100R 5% MUL CR16	R
5NDTS12XY		CCT BOARD: CPS/B *X-Y PLOTTER CB
BC215	/A *X-Y DTS12P*P32B	B
RM2510025	51R 1% MUL MR25	R7:12
RM3390R25	390R 1% MUL MR25	R8 9:14
RM3560R25	560R 1% MUL MR25	R10
RM3910R25	910R 1% MUL MR25	R6
RM41K0025	1K0R 1% MUL MR25	R11
RM44K7025	4K7R 1% MUL MR25	R1-4
RM511K025	11KR 1% MUL MR25	R5
RM515K025	15KR 1% MUL MR25	R13
CE3100UDM	100UF 10V MUL 030	C23
CF0U100NMKS3	0.1UF 100V WIM MKS3	C15-18:20-22 4 5
CF510K0N2MIN	10KPF 100V WIM FKS2MIN	C1-14 9
PM3200R63X	200R SPL 63X	RV1 3
PM3500R63X	500R SPL 63X	RV2
VD74LS00N	INT CCT SN74LS00N	IC7
VD74LS02N	INT CCT SN74LS02N TEX	IC5
VD74LS04N	INT CCT SN74LS04N	IC6
VD74LS08N	INT CCT SN74LS08N	IC4:11
VD74LS10N	INT CCT SN74LS10N TEX	IC8
VD74LS11N	INT CCT SN74LS11N	IC3
VD74LS74N	INT CCT SN74LS74N	IC1
VD74LS112N	INT CCT SN74LS112N	IC13
VD74LS393N	INT CCT SN74LS393N	IC10 2
VD74LS374N	INT CCT DM74LS374N	IC16
VA358N	INT CCT LM358N	IC15 8
VA5008N	IC NE5008N *STATIC	IC17
VD74LS279	INT CCT 74LS279 NAT	IC2
VD74368AN	INT CCT 74368 NAT	IC9
VD1022LCN	INT CCT DAC1022LCN NAT	IC14
TIH2520NT1L	20W M52-1220-260	SK1 2
TBM2512PS	12W 6401 22-27 2121	SK3
TBM2503PS	3W 6410-22-27-2031	SK4
TBM2504PS	4W 6410 22-27 2041	SK5
SB0061	3ST/A *P/B SW DTS12P	SW1 2
RC72M2025	2M2R 10% MUL CR25	R735
PC0858308	4ZP/A *POT 100KR ?C	P105:205
PC0858310	4ZP/A *POT 10KR ?C	P608
PM44K7016N	4K7R TYPE 16PE LIN	P701
PM6100K12P	100KR LIN 12PE	P501
PM6220K16	220KR 16PE LIN 6MM SPI	P702
PM6220K16N4	220KR 16PE LIN 4MM SPI	P705
LD134R	LED RED T1 3/4 MV5753	LED717
LD134K	LED T1 3/4 MTG KIT	LED717
LD134G	LED GRN T1 3/4 MV64530	LED717
DS6394	SELEC DS6394 RCA ONLY	SCR750
VA40147	INT CCT. TY40147 MOT	SCR750
VA7912CT	INT CCT LM7912CT	IC702
VALM7812CT	INT CCT LM7812CT	IC701
PM71M0016	1M0R 16PE LIN 4MM SPI	P704
4NDTSCR		ASSEMBLY: SUB/C *CTR ASM
5NDTSM		CCT BOARD: CPS/D *DTS12 MAIN
5SDTMS		CCT BOARD: CPS/B *SCOPE STD
5SDTMCH1		CCT BOARD: CBP/B *CH1 COMPS
RM212R025	12R 1% MUL MR25	R152 3:70 3 P09:R167 P23
RM247R025	47R 1% MUL MR25	R157 8:65 6 9

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FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
RM282R025	82R 1% MUL MR25	R151
RM3180R25	180R 1% MUL MR25	R162
RM3390R25	390R 1% MUL MR25	R163
RM3910R25	910R 1% MUL MR25	R168
RM3680R25	680R 1% MUL MR25	R160 4
RM3820R25	820R 1% MUL MR25	R159
RM41K0025	1K0R 1% MUL MR25	R171
RM41K5025	1K5R 1% MUL MR25	R154:61
RM43K3025	3K3R 1% MUL MR25	R156
RM510K025	10KR 1% MUL MR25	R155
CC282P0N642	82PF 100V 683-34829	C154
CC11P80N642	1P8F 100V 683-09188	C152
CC41K00861	1K0PF ERI 861/AX	C156
CC18P20N642	8P2F 100V 683-09828	C153
DG4148	DIODE 1N4148	D150 1
PC41K0010V	POT 1K0R PIH PT10V	P150
VT182PL	TRANSISTOR BC182PL	TR150 1
VTBF199	TRANSISTOR BF199	TR155
VTX313	TRANSISTOR ZTX313	TR153 4
VTX510	TRANSISTOR ZTX510	TR152
5SDTMCH2		CCT BOARD: CBP/C *CH2 COMPS
RC12R2025	2R2 5% MUL CR25	R264 8
RM210R025	10R 1% MUL MR25	R267:74
RM212R025	12R 1% MUL MR25	R252 3:70:89
RM247R025	47R 1% MUL MR25	R257 8:65 6 9
RM282R025	82R 1% MUL MR25	R251
RM3180R25	180R 1% MUL MR25	R262
RM3390R25	390R 1% MUL MR25	R263:75 8
RM3680R25	680R 1% MUL MR25	R260
RM3820R25	820R 1% MUL MR25	R259
RM41K0025	1K0R 1% MUL MR25	R273
RM41K5025	1K5R 1% MUL MR25	R254:61
RM43K3025	3K3R 1% MUL MR25	R256:77
RM510K025	10KR 1% MUL MR25	R255:76
CC218P0N642	18PF 100V 683-10189	C253
CC282P0N642	82PF 100V 683-34829	C254
CC41K00861	1K0PF ERI 861/AX	C260
CC11P80N642	1P8F 100V 683-09188	C252
CC16P80N642	6P8F 100V 683-09688	C262
CF510K0N2MIN	10KPF 100V WIM FKS2MIN	C261
DG4148	DIODE 1N4148	D250 1 5
PC44K7010V	POT 4K7R PIH PT10V	P250
VT182PL	TRANSISTOR BC182PL	TR250 1 6 7
VTBF199	TRANSISTOR BF199	TR255
VTX313	TRANSISTOR ZTX313	TR253 4
VTX510	TRANSISTOR ZTX510	TR252
5SDTMX		CCT BOARD: CBP/C *X AMP COMPS
CAOMIT	CAPACITORS OMITTED	C507
RC6470K25	470KR 5% MUL CR25	R536
RC6680K25	680KR 5% MUL CR25	R535
RC6820K25	820KR 5% MUL CR25	R534
RM212R025	12R 1% MUL MR25	R502 4 8:18:24 6
RM3100R25	100R 1% MUL MR25	R506:25
RM3220R25	220R 1% MUL MR25	R532
RM3470R25	470R 1% MUL MR25	R507:19:27
RM3680R25	680R 1% MUL MR25	R520
RM41K2025	1K2R 1% MUL MR25	R509
RM41K5025	1K5R 1% MUL MR25	R516
RM42K2025	2K2R 1% MUL MRS25	R530:40 1
RM42K7025	2K7R 1% MUL MR25	R529
RM44K3025	4K3R 1% MUL MR25	R510
RM44K7025	4K7R 1% MUL MR25	R503:28
RM48K2025	8K2R 1% MUL MR25	R514:31
RM510K025	10KR 1% MUL MR25	R517
RM512K025	12KR 1% MUL MR25	R522
RM515K076	15KR 5% WEL FA36	R505:23
RM547K025	47KR 1% MUL MR25	R539
RM582K025	82KR 1% MUL MR25	R537
RM6120K25	120KR 1% MUL MR25	R511 5
RM6150K25	150KR 1% MUL MR25	R512:21
RM43K9025	3K9R 1% MUL MR25	R501:13
RLINK24	24 SWG TC LINK	R538:42

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MAIN UNIT ITEM NUMBER : 15DTS12P DESCRIPTION : GEN/X *DTS12P * 990

FARNELL PART NUMBER	DESCRIPTION	*---------- CIRCUIT REFERENCE ----------*
CC15P60861	5P6F ERI 861/N470	C502 4
CC3220P831H	220PF ERIE 831/HI-K	C508
CE3220UFM	220UF 16V MUL 031	C501 5
CF522K0T352	22KPF 400V 368-50223	C506
CF510K0N2MIN	10KPF 100V WIM FKS2MIN	C503
DG4148	DIODE 1N4148	D501-4
PC3470R10V	POT 470R PIH PT10V	P504 6
PC42K2010V	POT 2K2R PIH PT10V	P503 5
PC6220K10V	POT 220KR PIH PT10V	P507
PM6100K63P	100KR SPL 63P	P502
VT182PL	TRANSISTOR BC182PL	TR501 3-5
VTBF462	TRANSISTOR BF462	TR502 6 9
VTX313	TRANSISTOR ZTX313	TR507
VTX510	TRANSISTOR ZTX510	TR508
ZC1M10	1000UH 552-5373-49-020	L501 2
MC2	CERAMIC BEAD SDP2 MET	R505:23 X2/L
CC3150PN642	150PF 100V 683-34151	C509
5SDTMY		CCT BOARD: CBP/C *Y AMP COMPS
CAOMIT	CAPACITORS OMITTED	C301 2 6-8
RM212R025	12R 1% MUL MR25	R303 5:10 6 7:22
RM222R025	22R 1% MUL MR25	R330
RM247R025	47R 1% MUL MR25	R314
RM3100R25	100R 1% MUL MR25	R307 8:19:20
RM3330R25	330R 1% MUL MRS25	R306 9:13:21
RM3560R25	560R 1% MUL MR25	R324 8
RM41K0025	1K0R 1% MUL MR25	R323
RM41K2025	1K2R 1% MUL MR25	R329
RM41K6025	1K6R 1% MUL MR25	R312
RM42K7025	2K7R 1% MUL MR25	R313
RM511K084	11KR 5% FA84*RM522K075	R301:25:32 3
RM515K076	15KR 5% WEL FA86	R311 5
CC15P60861	5P6F ERI 861/N470	C310 1
CC41K00861	1K0PF ERI 861/AX	C304
CC247P0N642	47PF 100V 683-34479	C312
CF0U100T352	0.1UF 400V 368-50104	C300 3
CF44K7ONFKS2	4K7PF 100V WIM FKS2	C313
CV210P	10PF 109-2991-010 BLU	C305
CF42K2ONFKS2	2K2PF 100V WIM FKS2MIN	C309
DG4148	DIODE 1N4148	D301-5
PC42K2010V	POT 2K2R PIH PT10V	P301
VT182PL	TRANSISTOR BC182PL	TR304 5
VTX313	TRANSISTOR ZTX313	TR302 3
DZ210V00W5	ZPD10 ITT	Z301
DZ15V60UW5	ZPD5.6 ITT	Z302 3
MC2	CERAMIC BEAD SDP2 MET	R301:25:32 3 X1/L:R311 5 X2/L
RM315UR25	150R 1% MUL MR25	R331
PC3100R10LH	100R PIH PT10LH	P302
5SDTMPS		CCT BOARD: CPS/F *P/SUPPLY COMPS
RC810M025	10MR 10% MUL CR25	R727
RG71M0037	1M0R 5% MUL VR37	R707-14
RM3390R25	390R 1% MUL MR25	R706
RM356UR25	560R 1% MUL MR25	R732 3
RM3680R25	680R 1% MUL MR25	R715:41
RM3820R25	820R 1% MUL MR25	R703
RM42K2025	2K2R 1% MUL MRS25	R701:16 7
RM41K2025	1K2R 1% MUL MR25	R750
RM44K7025	4K7R 1% MUL MR25	R718:31 9
RM48K2025	8K2R 1% MUL MR25	R737
RM510K025	10KR 1% MUL MR25	R719
RM568K025	68KR 1% MUL MR25	R740
RM615UK30	150KR 2% MUL MR30	R725
RM633UK30	330KR 2% MUL MR30	R721-3 6
RM656UK30	560KR 2% MUL MR30	R724
RM41K6030	1K6R 2% MUL MR30	R738
RM522K075	2K2R 5% FA85*RM511K084	R734
RAOMIT	RESISTORS OMITTED	R736
CC347UP031H	47UPF ERI 831/HIK	C721
CC44K70ZRDX	4K7PF 4KV RDX025	C720 2
CC520K0ZHD25	20KPF 2KV HD25K32UN	C723
CE3220UKEK	220UF 50V KMVB ECC	C708:10
CF510K0N2MIN	10KPF 100V WIM FKS2MIN	C709
CC333UPN642	33UPF 100V 683-53331	C724

FARNELL INSTRUMENTS LTD

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MAIN UNIT ITEM NUMBER : 15DTS12P DESCRIPTION : GEN/X *DTS12P * 990

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE	
CE12U20UE	2U2F 450V SMT ECC	C711-18	
DBW02M	BRDG RECT W02M	BR701	
DG4007	DIODE 1N4007	D706-09	
DG4148	DIODE 1N4148	D716 8:20	
PC42K2010V	POT 2K2R PIH PT10V	P703	
PAOMIT	POTENTIOMETERS OMITTED	P701 2 4 5	
VAOMIT	TRANSISTORS/ICS OMITTE	IC701 2:TR706	
VT182PL	TRANSISTOR BC182PL	TR704	
VT212PL	TRANSISTOR BC212PL	TR701 3	
VTBUX87	TRANSISTOR BUX87	TR702	
VTX313	TRANSISTOR ZTX313	TR705	
DZ233V00W5A	BZX79C33 MUL	Z701	
TBM2508PR	8W 7478 22-05 3081	SK1	
RM6180K30	180KR 2% MUL MR30	R720	
CC510K0Y621	0.01UF 1000V RAX621	C719	
RM522K025	22KR 1% MUL MR25	R730	
MC2	CERAMIC BEAD SDP2 MET	R734 X2/L	
MC1	CERAMIC BEAD SDP1 MET	BR701 X1/L	
CF0U100LMKS	0.1UF 63V WIM MKS2MIN	C707	
DG240	DIODE GP0240	D710 1)	FIT ACROSS 2 PITCHES:D719
CF0U220LMKS2	0.22UF 63V WIM MKS2	C725	
CP510K0TMKT1	10KPF 400V 5% MKT1.50	C706	
BC099	C /D *DTS MAIN *S12B	B	
MM5L	BER OXIDE WASHER NW5S	TR502 6	
MB0057	4SV/D *M2.5 BUSH NAT	TR502 6	
YP7130BLK	BLACK 24AWG UL1430	LINK	
RAOMIT	RESISTORS OMITTED	R172:271 2 9:80-88	
CAOMIT	CAPACITORS OMITTED	C155:255-59	
DAOMIT	DIODES OMITTED	D252-254:Z250	
PAOMIT	POTENTIOMETERS OMITTED	P252	
VAOMIT	TRANSISTORS/ICS OMITTE	TR253-60	
RM212R025	12R 1% MUL MR25	R344	
CE41K00GE	1KUF 25V KMVB ECC	C701 2	
CF0U220LMKS2	0.22UF 63V WIM MKS2	C750	
CE44K70FTM	4K7UF 16V TSW TAG MNT	C753	
CF0U100LMKS	0.1UF 63V WIM MKS2MIN	C751 2	
FH5229	FUSEHOLDER 5229	F750	
FF1A0013	FUSE TDC13 1AMP	F750	
DBP02	BRDG RECT KBP02	BR750	
DZ16V200W5	ZPD6.2 ITT	Z750	
DLINK24	24 SWG TC LINK	D253	
VLINK24	24 SWG TC LINK	TR259 E TO C	
YT24	T/C WIRE 24SWG	LINKS X19	
TP15080	CB PIN MR15080 TUC	C/S X38 T/S X25	
ZC0858301	3ZQ/B *CHK DT12/5	L700	
ZR0272	2SR/E *DTS12	TX701	
RM3100R30	100R 2% MUL MR30	R728 9	
CE247U0SSMT	47UF 350V SMT ECC	C703 4	
FT500M11	500MA A/S TDC11	F701	

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MAIN UNIT ITEM NUMBER : 15DTS12B DESCRIPTION : GEN/T *DTS12B * 989

IMPORTANT EXPLANATION - PLEASE READ BEFORE ORDERING PARTS.
DUE TO LIMITATIONS IN THE NUMBER OF CHARACTER SPACES AVAILABLE THE INFORMATION IN THE CIRCUIT REFERENCE FIELD HAS BEEN ABBREVIATED AND THE FOLLOWING NOTES ARE PROVIDED AS A GUIDE TO IT'S INTEPPRETATION:

1. WHERE A COMPONENT IS USED MORE THAN ONCE ON AN ASSEMBLY THE ALPHABETIC PORTION OF THE CIRCUIT REFERENCE FOR ITS SECOND AND SUBSEQUENT LOCATIONS HAS BEEN OMITTED; EG. THE CIRCUIT REFERENCE INFORMATION FOR A COMPONENT LOCATED AT R1 AND R6 WILL APPEAR AS R1 6
2. THE CIRCUIT REFERENCE NUMBERS ARE PRESENTED IN ASCENDING DECADE BLOCKS DELIMITED BY COLONS: SECOND AND SUBSEQUENT NUMBERS WITHIN A DECADE BLOCK REPRESENT ONLY THE UNIT VALUE OF THE LOCATION (THE TENS AND HUNDREDS VALUES BEING IMPLIED); EG. FOR A COMPONENT LOCATED AT R54,R57,R59,R82,R87,R102,R110, AND R112 THE CIRCUIT REFERENCE ENTRY WILL BE R54 7 9:82 7:102:10 2
3. WHERE COMPONENTS ARE USED IN A SERIES OF NEIGHBOURING CIRCUIT REFERENCE LOCATIONS THE CIRCUIT REFERENCE NUMBERS ARE REPRESENTED AS INCLUSIVE BLOCKS USING A HYPHEN; EG. A COMPONENT LOCATED AT R16,R19,R21,R24,R25,R26,R31,R37,R38,R39,R40,R44 AND R46 WILL BE REPRESENTED AS R16 9:21 4-6:31 37-40 4 6 (AN EXCEPTION TO THE RULES OCCURS WHEN A SERIES CROSSES A DECADE BLOCK IN WHICH CASE THE TENS VALUE IS INSERTED.
4. COMMENTS ARE PRECEDED BY A SEMICOLON.

WHEN ORDERING REPLACEMENT PARTS PLEASE BE SURE TO QUOTE THE PART NUMBER PROVIDED.

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
25DTS12B		END ITEM: FIN/A *DTS12B
35DTS12		CASING: CAS/C *DTS12
4NDTSCB		ASSEMBLY: SUB/C *CHASSIS DTS12B
4NDTSF		ASSEMBLY: SUB/C *F/PANEL DTS12
4SDTATN		ASSEMBLY: SUB/B *DUAL ATTN
4SDTSS1		ASSEMBLY: SUB/A *CH1 ATTN SW
5SDTATN1		CCT BOARD: CPS/I *CH1 ATTN DTS12
RC12R2025	2R2 5% MUL CR25	R25
RC14R7025	4R7 5% MUL CR25	R5
RC6470K25	470KR 5% MUL CR25	R13
RM210R025	10R 1% MUL MR25	R17:24
RM212R025	12R 1% MUL MR25	R30 1
RM3120R25	120R 1% MUL MR25	R15 6
RM3560R25	560R 1% MUL MR25	R29
RM3680R25	680R 1% MUL MR25	R26
RM42K2025	2K2R 1% MUL MRS25	R27 8:32
RM45K6025	5K6R 1% MUL MR25	R18:23
RM46K8025	6K8R 1% MUL MR25	R19
RM510K1H8	10K1R 1% 100PPM H8	R4
RM539K025	39KR 1% MUL MR25	R21
RM6111KH8	111KR 1% 100PPM H8	R7
RM6220K25	220KR 1% MUL MR25	R14:22
RM6333KH8	333KR 1% 100PPM H8	R11
RM6500KH8	500KF 1% 100PPM H8	R8
RM6750KH8	750K 1% 100PPM H8	R10
RM6900KH4	900KR 1% 100PPM H4	R6
RM6990KH4	990KR 1% 100PPM H4	R3 FITTED ON BACK OF CB
RM71M00H8	1MOR 1% 100PPM H8	R9:12
RM3200R25	200R 1% MUL MR25	R20
CC247P0N642	47PF 100V 683-34479	C7
CC41K00831H	1K0PF ERI 831/HIK	C4:14
CC510K0861	10KPF ERI 861T/25	C19:22
CC215P0N642	15PF 100V 683-10159	C17
CV210P	10PF 109-2991-010 BLU	C2 5 8:11 2
CC11P50661	1P5F ERI 861/P100	C23 FITTED ON BACK OF CB
CV2325P	3-25PF 109-2991 GRN	C1 6 9
CF0U100NMKS3	0.1UF 100V WIM MKS3	C16
CF44K70NFKS2	4K7PF 100V WIM FKS2	C15
PC44K7010V	POT 4K7R PIH PT10V	P1 2
VF441	TRANS U441 FET *STATIC	VT1-2
VT212PL	TRANSISTOR BC212PL	VT3
VTX313	TRANSISTOR ZTX313	VT4
VTX510	TRANSISTOR ZTX510	VT5
CAOMIT	CAPACITORS OMITTED	C10 3

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MAIN UNIT ITEM NUMBER : 15DTS12B DESCRIPTION : GEN/T *DTS12B * 989

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
DAOMIT	DIODES OMITTED	D1
BC0684	2SZ/B *DT125 ATT *	PREFIX 100
DZ14V700W5	ZPD4.7 ITT	Z1
SB0057	4ST/A *INPUT DTS12	SW1-2
CF0U100T352	0.1UF 400V 368-50104	C21 FITTED ON BACK OF CB
RM527K025	27KR 1% MUL MR25	R33
TP15080	CB PIN MR15080 TUC	C/S X20 T/S X1
DGJPAD100	DIODE JPAD/100 SIL	D2
CF3470PNFKP2	470PF 100V 5% FKP2	C3
CF522K0NFKS3	22KPF 100V WIM FKS3	C18:20
RM247R025	47R 1% MUL MR25	R1 2
SW0036	3ST/B *WAFER SCOPE	SW3
4SDTSS2		ASSEMBLY: SUB/A *CH2 ATTN SW
5SDTATN2		CCT BOARD: CPS/I *CH2 ATTN DTS12
RC12R2025	2R2 5% MUL CR25	R25
RC6470K25	470KR 5% MUL CR25	R13
RM210R025	10R 1% MUL MR25	R17:24
RM212R025	12R 1% MUL MR25	R30 1
RM3120R25	120R 1% MUL MR25	R15 6
RM3560R25	560R 1% MUL MR25	R29
RM3680R25	680R 1% MUL MR25	R26
RM42K2025	2K2R 1% MUL MRS25	R27 8:32
RM45K6025	5K6R 1% MUL MR25	R18:23
RM46K8025	6K8R 1% MUL MR25	R19
RM510K1H8	10K1R 1% 100PPM H8	R4
RM539K025	39KR 1% MUL MR25	R21
RM6111KH8	111KR 1% 100PPM H8	R7
RM6220K25	220KR 1% MUL MR25	R14:22
RM6333KH8	333KR 1% 100PPM H8	R11
RM6500KH8	500KR 1% 100PPM H8	R3
RM6750KH8	750KR 1% 100PPM H8	R10
RM6900KH4	900KR 1% 100PPM H4	R6
RM6990KH4	990KR 1% 100PPM H4	R3 FITTED ON BACK OF CB
RM71M00H8	1MOR 1% 100PPM H8	R9:12
RM3200R25	200R 1% MUL MR25	R20
RC14R7025	4R7 5% MUL CR25	R5
CC247P0N642	47PF 100V 683-34479	C7
CC41K00831H	1KUPF ERI 831/HIK	C4:14
CC510K0861	10KPF ERI 861T/25	C19:22
CV210P	10PF 109-2991-010 BLU	C2 5 8:11 2
CV2325P	3-25PF 109-2991 GRN	C1 6 9
CF0U100NMKS3	0.1UF 100V WIM MKS3	C16
CF44K70NFKS2	4K7PF 100V WIM FKS2	C15
CC215P0N642	15PF 100V 683-10159	C17
CC11P50861	1P5F ERI 861/P100	C23 FITTED ON BACK OF CB
CAOMIT	CAPACITORS OMITTED	C10 3
PC44K7010V	POT 4K7R PIH PT10V	P1 2
VF441	TRANS U441 FET *STATIC	VT1-2
VT212PL	TRANSISTOR BC212PL	VT3
VTX313	TRANSISTOR ZTX313	VT4
VTX510	TRANSISTOR ZTX510	VT5
D4OMIT	DIODES OMITTED	D1
MP075BLKVX	PVC SLV VX.75 BLK PER	C23
BC0684	2SZ/B *DT125 ATT *	PREFIX 200
DZ14V700W5	ZPD4.7 ITT	Z1
SB0057	4ST/A *INPUT DTS12	SW2
CF0U100T352	0.1UF 400V 368-50104	C21 FITTED ON BACK OF CB
RM527K025	27KR 1% MUL MR25	R33
TP15080	CB PIN MR15080 TUC	C/S X21
DGJPAD100	DIODE JPAD/100 SIL	D2
CF3470PNFKP2	470PF 100V 5% FKP2	C3
CF522K0NFKS3	22KPF 100V WIM FKS3	C18:20
RM247R025	47R 1% MUL MR25	R1 2
SW0036	3ST/B *WAFER SCOPE	SW3
4NDTSTB		ASSEMBLY: SUB/B *TIME BASE DTS12
BC098	C /B *DTS SW/TB *S12B	FREE ISS TO SUPPLIER
SW0051C	3ST/A *SW LESS CR N-OR	SWITCH LESS CB
SB0084	3ST/A *TIMES 5 DTS12	SW501
5NDTSA		CCT BOARD: CPS/E *ANLG DTS IP AMP
BC097	C /D *DTS12 ANA *P32B	B
RM210R025	10R 1% MUL MR25	R16-19:21 2:39:40:116 7:23

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MAIN UNIT ITEM NUMBER : 15DTS12B DESCRIPTION : GEN/T *DTS12B * 989

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
RM268R025	68R 1% MUL MR25	R13 5
RM3220R25	220R 1% MUL MR25	R106
RM3330R25	330R 1% MUL MRS25	R122:33
RM3470R25	470R 1% MUL MR25	R121:34
RM3560R25	560R 1% MUL MR25	R29:31:120:32
RM3680R25	680R 1% MUL MR25	R109:36
RM41K0025	1K0R 1% MUL MR25	R23 5:112 8 9:30 1:41
RM41K5025	1K5R 1% MUL MR25	R111:40
RM41K8025	1K8R 1% MUL MR25	R1 3:102:47
RM42K2025	2K2R 1% MUL MRS25	R10
RM44K7025	4K7R 1% MUL MR25	R7 9:12 4
RM510K025	10KR 1% MUL MR25	R6 8
CC227PON642	27PF 100V 683-34279	C5 7
CC3100PN642	100PF 100V 683-34101	C65:74:84 6
CC3330PN642	330PF 100V 683-58331	C67:87
CF510K0N2MIN	10KPF 100V WIM FKS2MIN	C73
CF44K70NFKS2	4K7PF 100V WIM FKS2	C70
CF0U100NMKS3	0.1UF 100V WIM MKS3	C2 3 6 8-10 8:20:60 6 8:71 2:88-90
DG4148	DIODE 1N4148	D12-19
VT182PL	TRANSISTOR BC182PL	TR7 9
VTX313	TRANSISTOR ZTX313	TR11 3
VTX510	TRANSISTOR ZTX510	TR10 2
VA356TC	IC UAF356TC/LF356N	IC2 3 6:19
VA3039	INT CCT CA3039 RCA	IC17 8
VD4066CN	IC CD4066CN *STATIC	IC20
PC3470R10V	POT 470R PIH PT10V	P1 2
PC41K0010V	POT 1K0R PIH PT10V	P11 2
PC510K010V	10KR PIH PT10V	P13 4
SNDTSAL		CCT BOARD: CPS/E *ANLOG LOGIC DTS
RM210R025	10R 1% MUL MR25	R43 4:53 56-58:65 9:70 8 9
RM212R025	12R 1% MUL MR25	R73:31 5
RM3220R25	220R 1% MUL MR25	R148
RM3560R25	560R 1% MUL MR25	R41:52
RM3680R25	680R 1% MUL MR25	R28:54:76
RM41K0025	1K0R 1% MUL MR25	R27:50 1:64:146
RM41K2025	1K2R 1% MUL MR25	R82
RM41K8025	1K8R 1% MUL MR25	R61:145
RM42K2025	2K2R 1% MUL MRS25	R11:34
RM43K3025	3K3R 1% MUL MR25	R74
RM43K9025	3K9R 1% MUL MR25	R63
RM44K7025	4K7R 1% MUL MR25	R34 5:66
RM46K8025	6K8R 1% MUL MR25	R5:20:37 8
RM510K025	10KR 1% MUL MR25	R75
RM515K025	15KR 1% MUL MR25	R86
RM539K025	39KR 1% MUL MR25	R33 6
RM6220K25	220KR 1% MUL MR25	R59
RM6560K30	560KR 2% MUL MR30	R101 3
RC71M5025	1M5R 5% MUL CR25	R67
RM3150R25	150R 1% MUL MR25	R69
RM3100R25	100R 1% MUL MR25	R77
RM3270R25	270R 1% MUL MR25	R55
RM45K1025	5K1R 1% MUL MR25	R80
RM512K025	12KR 1% MUL MR25	R83
CC215PON642	15PF 100V 683-10159	C53
CC227PON642	27PF 100V 683-34279	C4:11 7
CC3100PN642	100PF 100V 683-34101	C44
CC3330PN642	330PF 100V 683-58331	C77 8
CE12U20KD	2U2F 50V DUB K	C32
CE210U0GM	10UF 25V MUL 030	C33 6:58
CF510K0N2MIN	10KPF 100V WIM FKS2MIN	C1:14:30 9:42:52
CF44K70NFKS2	4K7PF 100V WIM FKS2	C75 P05 C85 P08
CF41K00NFKS2	1K0PF 100V WIM FKS2	C24 9:37:46
CF0U330NMKS	0.33UF 100V WIM MKS4	C50
CF0U100NMKS3	0.1UF 100V WIM MKS3	C16 9:21 3 6 8:34:40 1 3 5:51 9:64:76:91
CV2210P808	V/CAP 2/10PF 30811109	C61-63
DG4148	DIODE 1N4148	D9-11
DZ12V500W3	ZN404 FER	Z1
PC41K0010V	POT 1K0R PIH PT10V	P7
PC42K2010V	POT 2K2R PIH PT10V	P5
PC44K7010V	POT 4K7R PIH PT10V	P3
PM3200R63P	200R SPL 63P	P6

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MAIN UNIT ITEM NUMBER : 15DTS12B DESCRIPTION : GEN/T *DTS12B * 989

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
VA1001J	IC TDC1001J8C *STATIC	IC10
VA356TC	IC UAF356TC/LF356N	IC5 7:12
VA3039	INT CCT CA3039 RCA	IC9
VA5008N	IC NE5008N *STATIC	IC14
VA79L05ACZ	INT CCT LM79L05ACZ	IC15
VD74LS123N	INT CCT SN74LS123N	IC1
VD74LS373N	INT CCT SN74LS373N	IC11
VD7406N	INT CCT SN7406N	IC4 3
VD74121N	INT CCT SN74121N TEX	IC16
VT212PL	TRANSISTOR BC212PL	TR3
VT182PL	TRANSISTOR BC182PL	TR1 4 5
CAOMIT	CAPACITORS OMITTED	C31
VP1A	TRANSITOR PAD TW1A	Z1
TP15080	CB PIN MR15080 TUC	C/S X8
VD74LS374N	INT CCT DM74LS374N	IC13
CF3220PNFKP2	220PF 100V 5% FKP2	C38
RM3910R25	910R 1% MUL MR25	R110:39
RM3100R25	100R 1% MUL MR25	R114 5:43 4
RM3270R25	270R 1% MUL MR25	R104:35
RM512K025	12KR 1% MUL MR25	R113:42
TBM3906PR	6W 2420-09-75-1061	SK2
TIH2520NR1L	20W HEAD M52-1220-460	SK1
CF3220PNFKP2	220PF 100V 5% FKP2	C15:69
5NDTSTG		CCT BOARD: CPS/L *TRIGGER DTS12
BC095	C /D *DTS12 TRGR*P32B	B
RM210R025	10R 1% MUL MR25	R122
RM212R025	12R 1% MUL MR25	R23 6 7:46 7:80-82 6:90 3 4:123 4
RM215R025	15R 1% MUL MR25	R77:129
RM3100R25	100R 1% MUL MR25	R33:40:121
RM3180R25	180R 1% MUL MR25	R14
RM3220R25	220R 1% MUL MR25	R10 9:76
RM3270R25	270R 1% MUL MR25	R11 5:83
RM3330R25	330R 1% MUL MRS25	R5
RM3390R25	390R 1% MUL MR25	R52:60
RM3470R25	470R 1% MUL MR25	R105
RM3560R25	560R 1% MUL MR25	R12:24
RM41K0025	1K0R 1% MUL MR25	R13 6:54:104:16
RM41K2025	1K2R 1% MUL MR25	R17
RM41K8025	1K8R 1% MUL MR25	R101
RM42K0025	2K0R 1% MUL MR25	R106
RM42K2025	2K2R 1% MUL MRS25	R35:49:50:71:89:91:117
RM42K7025	2K7R 1% MUL MR25	R30:108
RM43K3025	3K3R 1% MUL MR25	R25:56:115:20 7
RM43K9025	3K9R 1% MUL MR25	R75:110
RM44K7025	4K7R 1% MUL MR25	R1 7:18:34:41 5 8:53 5:84:92:107:13 8 9
RM45K6025	5K6R 1% MUL MR25	R2 8:36:109:12
RM46K8025	6K8R 1% MUL MR25	R73 4
RM48K2025	8K2R 1% MUL MR25	R20 2
RM510K025	10KR 1% MUL MR25	R28:51 8 9:87:126
RM512K025	12KR 1% MUL MR25	R3 4:114
RM515K025	15KR 1% MUL MR25	R21:70
RM527K025	27KR 1% MUL MR25	R102 3
RM547K025	47KR 1% MUL MR25	R29:32 8 9:78 9
RM556K025	56KR 1% MUL MR25	R111
RM568K025	68KR 1% MUL MR25	R9
RM6100K25	100KR 1% MUL MR25	R6:31
RM6120K25	120KR 1% MUL MR25	R72
RC71M2025	1M2R 5% MUL CR25	R43 4
RC72M2025	2M2R 10% MUL CR25	R42
RM72M40H2	2M4R 1% 100PPM H2	R125
CC210PON642	10PF 100V 683-10109	C37:51
CC218PON642	18PF 100V 683-10189	C34
CC233PON642	33PF 100V 683-34339	C8
CC239PON642	39PF 100V 683-34399	C45
CC268PON642	68PF 100V 683-34689	C7
CC3100PN642	100PF 100V 683-34101	C16 8:41 2 8:52

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FARNELL PART NUMBER	DESCRIPTION	*---------- CIRCUIT REFERENCE ----------*
CC330PN642	330PF 100V 683-58331	C2
CC220PN633	22UPF 100V 683-58221	C35 6
CF0U100R352	0.1UF 250V 368-40104	C1:13
CF0U100NMKS3	0.1UF 100V WIM MKS3	C5:19:23:54 6 8 9:70
CF11U00PRNR	1UF 160V 5% RNR ICW	C20
CF41K00NFKS2	1KUPF 100V WIM FKS2	C31:46
CF510K0N2MIN	10KPF 100V WIM FKS2MIN	C3:10-12 4 5:24-30 2 3 8 9:40 3 4 7:50:60-63 8
CE210U0GM	10UF 25V MUL 030	C4 9:53 5:66
CE222U0DM	22UF 10V MUL 030	C57
VT182PL	TRANSISTOR BC182PL	TR4 6-8:14-16
VT212PL	TRANSISTOR BC212PL	TR1-3 5 9:17
DG4148	DIODE 1N4148	D1 4-13
DG922	DIODE 1S922	D2 3
VA311N	INT CCT LM311N 8PIN	IC7:11
VA356TC	IC UAF356TC/LF356N	IC5 6:12
VA710CN	INT CCT LM710CN 14PDIL	IC1
VD14572P	IC MC14572UBCP *STATIC	IC4
VD74LS00N	INT CCT SN74LS00N	IC8:21
VD74LS02N	INT CCT SN74LS02N TEX	IC3:22
VD74LS08N	INT CCT SN74LS08N	IC10
VD74LS221N	IC SN74LS221N NAT	IC17-20
VD7406N	INT CCT SN7406N	IC9
VD74LS74N	INT CCT SN74LS74N	IC2:16
VD74390N	INT CCT SN74390N	IC13-15
VX5M0U	5MHZ HC18U	XL1 MC1 X1/L
VS8P	IC SKT 703-1308-010410	V
VS14L	IC SKT 703-1314-010410	V
VS16L	IC SKT 703-1316-010410	V
PC42K2010LH	2K2R PIH PT10LH	P4 5
PC44K7010LH	4K7R PIH PT10LH	P6
PC510K010LH	10KR PIH PT10LH	P1 7
PC522K010LH	22KR PIH PT10LH	P2 3
RC71M0025	1MOR 5% MUL CR25	R95:128
CC227P0N642	27PF 100V 683-34279	C65
DZ15V600W5	ZPD5.6 ITT	Z1
CC3180PN683	180PF 100V 683-58181	C22:49
SB0054	3ST/A *DTS12 TRIG 7W	SW2A-2G
TP7401	CB PIN 12W 1-163740-1	FIT T/S
TP7404	CB PIN 6W 163740-4 AMP	FIT T/S
CE14U70LM	4U7F 63V 015-90044	C6
CC3470PN630	470PF 100V 630-18471	C69
RAOMIT	RESISTORS OMITTED	R37
RM46K2025	6K2R 1% MUL MR25	R57
CC41K00N630	1KUPF 100 630-19102	C17
CE233U0FES	33UF 16V SMVB ECC	C64
MC1	CERAMIC BEAD SDP1 MET	XL1
TP15080	CB PIN MR1508U TUC	C/S X9
CF0U220NMKS4	0.22UF 100V MKS4	C71
VD74LS32N	INT CCT SN74LS32N	IC23
TBM2504PR	4W 7478-22-05-3041	SK2
TBM2512PT	12W 4094 22 05 2125	TBR1 2 3
TBM2504PS	4W 6410 22-27 2041	SK3
TIH2520NT1L	20W M52-1220-260	SK1
VTX313	TRANSISTOR ZTX313	TR13
CF41K00NFKP2	1KUPF 100V 5% FKP2	C21
CASOT	CAP SELECT ON TEST	C67
SNDTSL		CCT BOARD: CPS/F *LOGIC DTS12
BC096	C /D *DTS12 LOG *P32B	B
RM3180R25	180R 1% MUL MR25	R1 8
RM3820R25	820R 1% MUL MR25	R7:18-20
RM41K0025	1KOR 1% MUL MR25	R16
RM44K7025	4K7R 1% MUL MR25	R3 4 6 9:10 2 3:21
RM518K025	18KR 1% MUL MR25	R15
RM522K025	22KR 1% MUL MR25	R17
CC210P0N642	10PF 100V 683-10109	C20
CE222U0DM	22UF 10V MUL 030	C21
CE3100UDM	100UF 10V MUL 030	C37
CF0U100NMKS3	0.1UF 100V WIM MKS3	C22:38 9
CF510K0N2MIN	10KPF 100V WIM FKS2MIN	C2 4 6-19:23-29:31-36
SB0052	3ST/A *DTS12 LOGIC 4W	SW2
SB0053	3ST/A *DTS12 LOGIC 5W	SW1
LD134R	LED RED T1 3/4 MV5753	LED1

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FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
VD472114AP1	IC TMM314A PL-1*STATIC	IC28-31
VD7407N	INT CCT SN7407N	IC9
VD74LS00N	INT CCT SN74LS00N	IC2 4 6
VD74LS04N	INT CCT SN74LS04N	IC10 1
VD74LS08N	INT CCT SN74LS08N	IC1 8
VD74LS32N	INT CCT SN74LS32N	IC7
VD74LS74N	INT CCT SN74LS74N	IC12 4 6:33
VD74LS112N	INT CCT SN74LS112N	IC26
VD74LS157N	INT CCT SN74LS157N	IC17 8:20 1 4 5
VD74LS197N	INT CCT SN74LS197N	IC19
VD74LS221N	IC SN74LS221N NAT	IC27
VD74LS393N	INT CCT SN74LS393N	IC22 3:32
VS14L	IC SKT 703-1314-010410	V
VS16L	IC SKT 703-1316-010410	V
VS18L	IC SKT 703-1318-010410	V
RM42K7025	2K7R 1% MUL MR25	R24
LD134G	LED GRN T1 3/4 MV64530	LED2
TBM3902PR	2W 2420-09-75-1021	SK2
TBM2504PR	4W 7478-22-05-3041	SK1
RM330R25	330R 1% MUL MRS25	R14
TP15080	CB PIN MR15080 TJC	C/S X4
TL675191T	14W PROG HEADER	SW3
TBM2512PT	12W 4094 22 05 2125	SK3
CC510K0861	10KPF ERI 861T/25	C
RC3100R16	100R 5% MUL CR16	R
5NDTS12B		CCT BOARD: CPS/A *BUS INTERFACE
BC229	C /B *BUS DTS12B*P32B	B
RM44K7025	4K7R 1% MUL MR25	R1-8
CE3100UDM	100UF 10V MUL 030	C16
CF0U100NMKS3	0.1UF 100V WIM MKS3	C17 8
CF510K0N2MIN	10KPF 100V WIM FKS2MIN	C1-15 9
VD74LS86N	IC SN74LS86N TEX	IC1 2
VD74LS27N	IC SN74LS27N TEX	IC3
VD74LS11N	INT CCT SN74LS11N	IC4
VD74LS00N	INT CCT SN74LS00N	IC5
VD74LS08N	INT CCT SN74LS08N	IC6
VD74LS279	INT CCT 74LS279 NAT	IC7
VD74LS74N	INT CCT SN74LS74N	IC8 9
VD74LS04N	INT CCT SN74LS04N	IC10 1
VD74LS368AN	IC SN74LS368AN TEX	IC12
VD74LS374N	INT CCT DM74LS374N	IC13
VD75161AN	INT CCT SN75161AN	IC14
VD75160AN	INT CCT SN75160AN	IC15
TIH2520NT1L	20W M52-1220-260	SK1 2
TBM2512PS	12W 6401 22-27 2121	SK3
TBM2502PS	2W 641-22-27-2021	SK5
SC6	DIL SWITCH SDS6	SW1-5
TIH2526NT3L	26W HEAD M52-226-360	SK4
RC72M2025	2M2R 10% MUL CR25	R735
PM44K7016N	4K7R TYPE 16PE LIN	P701
PM6100K12P	100KR LIN 12PE	P501
PM6220K16	220KR 16PE LIN 6MM SPI	P702
PM6220K16N4	220KR 16PE LIN 4MM SPI	P705
PM71M0016	1MOR 16PE LIN 4MM SPI	P704
PC0858308	4ZP/A *POT 100KR ?C	P105:205
PC0858310	4ZP/A *POT 10KR ?C	P608
LD134G	LED GRN T1 3/4 MV64530	LED717
LD134R	LED RED T1 3/4 MV5753	LED717
LD134K	LED T1 3/4 MTG KIT	LED717
VTBF462	TRANSISTOR BF462	TR306-09:706
VA7912CT	INT CCT LM7912CT	IC702
VA40147	INT CCT. TY40147 MOT	IC750
DS6394	SELEC DS6394 RCA ONLY	SCR750
VALM7812CT	INT CCT LM7812CT	IC701
4NDTSCR		ASSEMBLY: SUB/C *CTR ASM
5NDTSM		CCT BOARD: CPS/D *DTS12 MAIN
5SDTMS		CCT BOARD: CPS/B *SCOPE STD
5SDTMCH1		CCT BOARD: CBP/B *CH1 COMPS
RM212R025	12R 1% MUL MR25	R152 3:70 3 P09:R167 P23
RM247R025	47R 1% MUL MR25	R157 8:65 6 9
RM282R025	82R 1% MUL MR25	R151

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RM3180R25	180R 1% MUL MR25	R162
RM3390R25	390R 1% MUL MR25	R163
RM3910R25	910R 1% MUL MR25	R168
RM3680R25	680R 1% MUL MR25	R160 4
RM3820R25	820R 1% MUL MR25	R159
RM41K0025	1K0R 1% MUL MR25	R171
RM41K5025	1K5R 1% MUL MR25	R154:61
RM43K3025	3K3R 1% MUL MR25	R156
RM510K025	10KR 1% MUL MR25	R155
CC282P0N642	82PF 100V 683-34829	C154
CC11P80N642	1P8F 100V 683-09188	C152
CC41K00861	1K0PF ERI 861/AX	C156
CC18P20N642	8P2F 100V 683-09828	C153
DG4148	DIODE 1N4148	D150 1
PC41K0010V	POT 1K0R PIH PT10V	P150
VT182PL	TRANSISTOR BC182PL	TR150 1
VTBF199	TRANSISTOR BF199	TR155
VTX313	TRANSISTOR ZTX313	TR153 4
VTX510	TRANSISTOR ZTX510	TR152
5SDTMCH2		CCT BOARD: CBP/C *CH2 COMPS
RC12R2025	2R2 5% MUL CR25	R264 8
RM210R025	10R 1% MUL MR25	R267:74
RM212R025	12R 1% MUL MR25	R252 3:70:89
RM247R025	47R 1% MUL MR25	R257 8:65 6 9
RM282R025	82R 1% MUL MR25	R251
RM3180R25	180R 1% MUL MR25	R262
RM3390R25	390R 1% MUL MR25	R263:75 8
RM3680R25	680R 1% MUL MR25	R260
RM3820R25	820R 1% MUL MR25	R259
RM41K0025	1K0R 1% MUL MR25	R273
RM41K5025	1K5R 1% MUL MR25	R254:61
RM43K3025	3K3R 1% MUL MR25	R256:77
RM510K025	10KR 1% MUL MR25	R255:76
CC213P0N642	18PF 100V 683-10189	C253
CC282P0N642	82PF 100V 683-34829	C254
CC41K00861	1K0PF ERI 861/AX	C260
CC11P80N642	1P8F 100V 683-09188	C252
CC16P80N642	6P8F 100V 683-09638	C262
CF510K0N2MIN	10KPF 100V WIM FKS2MIN	C261
DG4148	DIODE 1N4148	D250 1 5
PC44K7010V	POT 4K7R PIH PT10V	P250
VT182PL	TRANSISTOR BC182PL	TR250 1 6 7
VTBF199	TRANSISTOR BF199	TR255
VTX313	TRANSISTOR ZTX313	TR253 4
VTX510	TRANSISTOR ZTX510	TR252
5SDTMX		CCT BOARD: CBP/C *X AMP COMPS
CAOMIT	CAPACITORS OMITTED	C507
RC6470K25	470KR 5% MUL CR25	R536
RC6680K25	680KR 5% MUL CR25	R535
RC6820K25	820KR 5% MUL CR25	R534
RM212R025	12R 1% MUL MR25	R502 4 8:18:24 6
RM3100R25	100R 1% MUL MR25	R506:25
RM3220R25	220R 1% MUL MR25	R532
RM3470R25	470R 1% MUL MR25	R507:19:27
RM3680R25	680R 1% MUL MR25	R520
RM41K2025	1K2R 1% MUL MR25	R509
RM41K5025	1K5R 1% MUL MR25	R516
RM42K2025	2K2R 1% MUL MRS25	R530:40 1
RM42K7025	2K7R 1% MUL MR25	R529
RM44K3025	4K3R 1% MUL MR25	R510
RM44K7025	4K7R 1% MUL MR25	R503:28
RM48K2025	8K2R 1% MUL MR25	R514:31
RM510K025	10KR 1% MUL MR25	R517
RM512K025	12KR 1% MUL MR25	R522
RM515K076	15KR 5% WEL FA86	R505:23
RM547K025	47KR 1% MUL MR25	R539
RM582K025	82KR 1% MUL MR25	R537
RM6120K25	120KR 1% MUL MR25	R511 5
RM6150K25	150KR 1% MUL MR25	R512:21
RM43K9025	3K9R 1% MUL MR25	R501:13
RLINK24	24 SWG TC LINK	R538:42

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FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
CC15P60861	5P6F ERI 861/N470	C502 4
CC3220P831H	220PF ERIE 831/HI-K	C508
CE3220UFM	220UF 16V MUL 031	C501 5
CF522K0T352	22KPF 400V 368-50223	C506
CF510K0N2MIN	10KPF 100V WIM FKS2MIN	C503
DG4148	DIODE 1N4148	D501-4
PC3470R10V	POT 470R PIH PT10V	P504 6
PC42K2010V	POT 2K2R PIH PT10V	P503 5
PC6220K10V	POT 220KR PIH PT10V	P507
PM6100K63P	100KR SPL 63P	P502
VT182PL	TRANSISTOR BC182PL	TR501 3-5
VTBF462	TRANSISTOR BF462	TR502 6 9
VTX313	TRANSISTOR ZTX313	TR507
VTX510	TRANSISTOR ZTX510	TR508
ZC1M10	1000UH 552-5373-49-020	L501 2
MC2	CERAMIC BEAD SDP2 MET	R505:23 X2/L
CC3150PN642	150PF 100V 683-34151	C509
5SDTMY		CCT BOARD: CBP/C *Y AMP COMPS
CAOMIT	CAPACITORS OMITTED	C301 2 6-8
RM212R025	12R 1% MUL MR25	R303 5:10 6 7:22
RM222R025	22R 1% MUL MR25	R330
RM247R025	47R 1% MUL MR25	R314
RM3100R25	100R 1% MUL MR25	R307 8:19:20
RM3330R25	330R 1% MUL MRS25	R306 9:18:21
RM3560R25	560R 1% MUL MR25	R324 8
RM41K0025	1K0R 1% MUL MR25	R323
RM41K2025	1K2R 1% MUL MR25	R329
RM41K8025	1K8R 1% MUL MR25	R312
RM42K7025	2K7R 1% MUL MR25	R313
RM511K084	11KR 5% FA84*RM522K075	R301:25:32 3
RM515K076	15KR 5% WEL FA86	R311 5
CC15P60861	5P6F ERI 861/N470	C310 1
CC41K00861	1K0PF ERI 861/AX	C304
CC247P0N642	47PF 100V 683-34479	C312
CF0U100T352	0.1UF 400V 368-50104	C300 3
CF44K70NFKS2	4K7PF 100V WIM FKS2	C313
CV210P	10PF 109-2991-010 BLU	C305
CF42K20NFKS2	2K2PF 100V WIM FKS2MIN	C309
DG4148	DIODE 1N4148	D301-5
PC42K2010V	POT 2K2R PIH PT10V	P301
VT182PL	TRANSISTOR BC182PL	TR304 5
VTX313	TRANSISTOR ZTX313	TR302 3
DZ210V00W5	ZPD10 ITT	Z301
DZ15V600W5	ZPD5.6 ITT	Z302 3
MC2	CERAMIC BEAD SDP2 MET	R301:25:32 3 X1/L:R311 5 X2/L
RM3150R25	150R 1% MUL MR25	R331
PC3100R10LH	100R PIH PT10LH	P302
5SDTMPS		CCT BOARD: CPS/F *P/SUPPLY COMPS
RC810M025	10MR 10% MUL CR25	R727
RG71M0037	1M0R 5% MUL VR37	R707-14
RM3390R25	390R 1% MUL MR25	R706
RM3560R25	560R 1% MUL MR25	R732 3
RM3680R25	680R 1% MUL MR25	R715:41
RM3820R25	820R 1% MUL MR25	R703
RM42K2025	2K2R 1% MUL MRS25	R701:16 7
RM41K2025	1K2R 1% MUL MR25	R750
RM44K7025	4K7R 1% MUL MR25	R718:31 9
RM48K2025	8K2R 1% MUL MR25	R737
RM510K025	10KR 1% MUL MR25	R719
RM568K025	68KR 1% MUL MR25	R740
RM6150K30	150KR 2% MUL MR30	R725
RM6330K30	330KR 2% MUL MR30	R721-3 6
RM6560K30	560KR 2% MUL MR30	R724
RM41K8030	1K8R 2% MUL MR30	R738
RM522K075	22KR 5% FA85*RM511K084	R734
RAOMIT	RESISTORS OMITTED	R736

FARNELL INSTRUMENTS LTD

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MAIN UNIT ITEM NUMBER : 15DTS12B DESCRIPTION : GEN/T *DTS12B * 989

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE	
CC3470P831H	470PF ERI 831/HIK	C721	
CC44K70ZRDX	4K7PF 4KV RDX625	C720 2	
CC520K0ZHD25	20KPF 2KV HD25K320N	C723	
CE3220UKEK	220UF 50V KMVB ECC	C708:10	
CF510K0N2MIN	10KPF 100V WIM FKS2MIN	C709	
CC3330PN642	330PF 100V 683-58331	C724	
CE12U20UE	2U2F 450V SMT ECC	C711-18	
DBW02M	BRDG RECT W02M	BR701	
DG4007	DIODE 1N4007	D706-09	
DG4148	DIODE 1N4148	D716 8:20	
PC42K2010V	POT 2K2R PIH PT10V	P703	
PA0MIT	POTENTIOMETERS OMITTED	P701 2 4 5	
VA0MIT	TRANSISTORS/ICS OMITTE	IC701 2:TR706	
VT182PL	TRANSISTOR BC182PL	TR704	
VT212PL	TRANSISTOR BC212PL	TR701 3	
VTBUX87	TRANSISTOR BUX87	TR702	
VTX313	TRANSISTOR ZTX313	TR705	
DZ233V00W5A	BZX79C33 MUL	Z701	
TBM2508PR	8W 7478 22-05 3081	SK1	
RM6180K30	180KR 2% MUL MR30	R720	
CC510K0Y621	0.01UF 1000V RAX621	C719	
RM522K025	22KR 1% MUL MR25	R730	
MC2	CERAMIC BEAD SDP2 MET	R734 X2/L	
MC1	CERAMIC BEAD SDP1 MET	BR701 X1/L	
CF0U100LMKS	0.1UF 63V WIM MKS2MIN	C707	
DG240	DIODE GP0240	D710 1)	FIT ACROSS 2 PITCHES:D719
CF0U220LMKS2	0.22UF 63V WIM MKS2	C725	
CP510K0TMKT1	10KPF 400V 5% MKT1.50	C706	
BC099	C /D *DTS MAIN *S123	B	
MM5L	BER OXIDE WASHER NW5S	TR502 6	
M30057	4SV/D *M2.5 BUSH NAT	TR502 6	
YP7130BLK	BLACK 24AWG UL1430	LINK	
RA0MIT	RESISTORS OMITTED	R172:271 2 9:80-88	
CA0MIT	CAPACITORS OMITTED	C155:255-59	
DA0MIT	DIODES OMITTED	D252-254:Z250	
PA0MIT	POTENTIOMETERS OMITTED	P252	
VA0MIT	TRANSISTORS/ICS OMITTE	TR258-60	
RM212R025	12R 1% MUL MR25	R344	
CE41K00GE	1KUF 25V KMVB ECC	C701 2	
CF0U220LMKS2	0.22UF 63V WIM MKS2	C750	
CE44K70FTM	4K7UF 16V TSW TAG MNT	C753	
CF0U100LMKS	0.1UF 63V WIM MKS2MIN	C751 2	
FH5229	FUSEHOLDER 5229	F750	
FF1A0013	FUSE TDC13 1AMP	F750	
DBP02	BRDG RECT KBP02	BR750	
DZ16V200W5	ZPD6.2 ITT	Z750	
DLINK24	24 SWG TC LINK	D253	
VLINK24	24 SWG TC LINK	TR259 E TO C	
YT24	T/C WIRE 24SWG	LINKS X19	
TP15080	CB PIN MR15080 TUC	C/S X38 T/S X25	
ZC0858301	3ZW/B *CHK DT12/5	L700	
ZR0272	2SR/E *DTS12	TX701	
RM3100R30	100R 2% MUL MR30	R728 9	
CE247U0SSMT	47UF 350V SMT ECC	C703 4	
FT500M11	500MA A/S TDC11	F701	

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P A R T S L I S T

MAIN UNIT ITEM NUMBER : 15DTS12 DESCRIPTION : GEN/AK*DTS12 * 965

IMPORTANT EXPLANATION - PLEASE READ BEFORE ORDERING PARTS.
DUE TO LIMITATIONS IN THE NUMBER OF CHARACTER SPACES AVAILABLE THE INFORMATION IN THE CIRCUIT REFERENCE FIELD HAS BEEN ABBREVIATED AND THE FOLLOWING NOTES ARE PROVIDED AS A GUIDE TO IT'S INTERPRETATION:

1. WHERE A COMPONENT IS USED MORE THAN ONCE ON AN ASSEMBLY THE ALPHABETIC PORTION OF THE CIRCUIT REFERENCE FOR ITS SECOND AND SUBSEQUENT LOCATIONS HAS BEEN OMITTED; EG. THE CIRCUIT REFERENCE INFORMATION FOR A COMPONENT LOCATED AT R1 AND R6 WILL APPEAR AS R1 o
2. THE CIRCUIT REFERENCE NUMBERS ARE PRESENTED IN ASCENDING DECADE BLOCKS DELIMITED BY COLONS: SECOND AND SUBSEQUENT NUMBERS WITHIN A DECADE BLOCK REPRESENT ONLY THE UNIT VALUE OF THE LOCATION (THE TENS AND HUNDREDS VALUES BEING IMPLIED); EG. FOR A COMPONENT LOCATED AT R54,R57,R59,R82,R87,R102,R110, AND R112 THE CIRCUIT REFERENCE ENTRY WILL BE R54 7 9:82 7:102:10 2
3. WHERE COMPONENTS ARE USED IN A SERIES OF NEIGHBOURING CIRCUIT REFERENCE LOCATIONS THE CIRCUIT REFERENCE NUMBERS ARE REPRESENTED AS INCLUSIVE BLOCKS USING A HYPHEN; EG. A COMPONENT LOCATED AT R16,R19,R21,R24,R25,R26,R31,R37,R38,R39,R40,R44 AND R46 WILL BE REPRESENTED AS R16 9:21 4-6:31 37-40 4 6 (AN EXCEPTION TO THE RULES OCCURS WHEN A SERIES CROSSES A DECADE BLOCK IN WHICH CASE THE TENS VALUE IS INSERTED.
4. COMMENTS ARE PRECEDED BY A SEMICOLON.

WHEN ORDERING REPLACEMENT PARTS PLEASE BE SURE TO QUOTE THE PART NUMBER PROVIDED.

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
25DTS12		END ITEM: FIN/C *DTS12
4NDTSC		ASSEMBLY: SUB/F *CHASSIS DTS12
4NDTSF		ASSEMBLY: SUB/C *F/PANEL DTS12
4SDTATN		ASSEMBLY: SUB/3 *DUAL ATTN
4SDTSS1		ASSEMBLY: SUB/A *CH1 ATTN SW
5SDTATN1		CCT BOARD: CPS/I *CH1 ATTN DTS12
RC12R2025	2R2 5% MUL CR25	R25
RC14R7025	4R7 5% MUL CR25	R5
RC6470K25	470KR 5% MUL CR25	R13
RM210R025	10R 1% MUL MR25	R17:24
RM212R025	12R 1% MUL MR25	R30 1
RM3120R25	120R 1% MUL MR25	R15 6
RM3560R25	560R 1% MUL MR25	R29
RM3680R25	680R 1% MUL MR25	R26
RM42K2025	2K2R 1% MUL MRS25	R27 8:32
RM45K6025	5K6R 1% MUL MR25	R18:23
RM46K8025	6K8R 1% MUL MR25	R19
RM510K1H8	10K1R 1% 100PPM H8	R4
RM539K025	39KR 1% MUL MR25	R21
RM6111KH8	111KR 1% 100PPM H8	R7
RM6220K25	220KR 1% MUL MR25	R14:22
RM6333KH8	333KR 1% 100PPM H8	R11
RM6500KH8	500KR 1% 100PPM H8	R8
RM6750KH8	750KR 1% 100PPM H8	R10
RM6900KH4	900KR 1% 100PPM H4	R6
RM6990KH4	990KR 1% 100PPM H4	R3 FITTED ON BACK OF CB
RM71M00H8	1MOR 1% 100PPM H8	R9:12
RM3200R25	200R 1% MUL MR25	R20
CC247P0N642	47PF 100V 683-34479	C7
CC41K00831H	1K0PF ERI 831/HIK	C4:14
CC510K0861	10KPF ERI 861T/25	C19:22
CC215P0N642	15PF 100V 683-10159	C17
CV210P	10PF 109-2991-010 BLU	C2 5 8:11 2
CC11P50861	1P5F ERI 861/P100	C23 FITTED ON BACK OF CB
CV2325P	3-25PF 109-2991 GRN	C1 6 9
CF0U100NMKS3	0.1UF 100V WIM MKS3	C16
CF44K70NFKS2	4K7PF 100V WIM FKS2	C15
PC44K7010V	POT 4K7R PIH PT10V	P1 2
VF441	TRANS U441 FET *STATIC	VT1-2
VT212PL	TRANSISTOR BC212PL	VT3
VTX313	TRANSISTOR ZTX313	VT4
VTX510	TRANSISTOR ZTX510	VT5
CAOMIT	CAPACITORS OMITTED	C10 3
DAOMIT	DIODES OMITTED	D1

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MAIN UNIT ITEM NUMBER : 15DTS12 DESCRIPTION : GEN/AK*DTS12 * 965

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
BC0684	2SZ/B *DT125 ATT *	PREFIX 100
DZ14V700W5	ZPD4.7 ITT	Z1
SB0057	4ST/A *INPUT DTS12	SW1-2
CF0U100T352	0.1UF 400V 368-50104	C21 FITTED ON BACK OF CB
RM527K025	27KR 1% MUL MR25	R33
TP15080	CB PIN MR15080 TUC	C/S X20 T/S X1
DGJPAD100	DIODE JPAD/100 SIL	D2
CF3470PNFKP2	470PF 100V 5% FKP2	C3
CF522K0NFKS3	22KPF 100V WIM FKS3	C18:20
RM247R025	47R 1% MUL MR25	R1 2
SW0036	3ST/B *WAFER SCOPE	SW3
4SDTSS2		ASSEMBLY: SUB/A *CH2 ATTN SW
5SDTATN2		CCT BOARD: CPS/I *CH2 ATTN DTS12
RC12R2025	2R2 5% MUL CR25	R25
RC6470K25	470KR 5% MUL CR25	R13
RM210R025	10R 1% MUL MR25	R17:24
RM212R025	12R 1% MUL MR25	R30 1
RM3120R25	120R 1% MUL MR25	R15 6
RM3560R25	560R 1% MUL MR25	R29
RM3680R25	680R 1% MUL MR25	R26
RM42K2025	2K2R 1% MUL MRS25	R27 8:32
RM45K6025	5K6R 1% MUL MR25	R18:23
RM46K8025	6K8R 1% MUL MR25	R19
RM510K1H8	10K1R 1% 100PPM H8	R4
RM539K025	39KR 1% MUL MR25	R21
RM6111KH8	111KR 1% 100PPM H8	R7
RM6220K25	220KR 1% MUL MR25	R14:22
RM6333KH8	333KR 1% 100PPM H8	R11
RM6500KH8	500KR 1% 100PPM H8	R8
RM6750KH8	750KR 1% 100PPM H8	R10
RM6900KH4	900KR 1% 100PPM H4	R6
RM6990KH4	990KR 1% 100PPM H4	R3 FITTED ON BACK OF CB
RM71M00H8	1MOR 1% 100PPM H8	R9:12
RM3200R25	200R 1% MUL MR25	R20
RC14R7025	4R7 5% MUL CR25	R5
CC247P0N642	47PF 100V 683-34479	C7
CC41K00831H	1KUPF ERI 831/HIK	C4:14
CC510K0861	10KPF ERI 861T/25	C19:22
CV210P	10PF 109-2991-010 BLU	C2 5 8:11 2
CV2325P	3-25PF 109-2991 GRN	C1 6 9
CF0U100NMKS3	0.1UF 100V WIM MKS3	C16
CF44K70NFKS2	4K7PF 100V WIM FKS2	C15
CC215P0N642	15PF 100V 683-10159	C17
CC11P50861	1P5F ERI 861/P100	C23 FITTED ON BACK OF CB
CAOMIT	CAPACITORS OMITTED	C10 3
PC44K7010V	POT 4K7R PIH PT10V	P1 2
VF441	TRANS U441 FET *STATIC	VT1-2
VT212PL	TRANSISTOR BC212PL	VT3
VTX313	TRANSISTOR ZTX313	VT4
VTX510	TRANSISTOR ZTX510	VT5
DAOMIT	DIODES OMITTED	D1
MP075BLKVX	PVC SLV VX.75 BLK PER	C23
BC0684	2SZ/B *DT125 ATT *	PREFIX 200
DZ14V700W5	ZPD4.7 ITT	Z1
SB0057	4ST/A *INPUT DTS12	SW2
CF0U100T352	0.1UF 400V 368-50104	C21 FITTED ON BACK OF CB
RM527K025	27KR 1% MUL MR25	R33
TP15080	CB PIN MR15080 TUC	C/S X21
DGJPAD100	DIODE JPAD/100 SIL	D2
CF3470PNFKP2	470PF 100V 5% FKP2	C3
CF522K0NFKS3	22KPF 100V WIM FKS3	C18:20
RM247R025	47R 1% MUL MR25	R1 2
SW0036	3ST/B *WAFER SCOPE	SW3
4NDTSTB		ASSEMBLY: SUB/B *TIME BASE DTS12
BC098	C /B *DTS SW/TB *S123	FREE ISS TO SUPPLIER
SW0051C	3ST/A *SW LESS CB N-OR	SWITCH LESS CB
SB0J34	3ST/A *TIMES 5 DTS12	SW501
5NDTSA		CCT BOARD: CPS/E *ANLG DTS IP AMP
BC097	C /D *DTS12 ANA *P323	B
RM210R025	10R 1% MUL MR25	R16-19:21 2:39:40:116 7:23
RM268R025	68R 1% MUL MR25	R13 5

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MAIN UNIT ITEM NUMBER : 15DTS12 DESCRIPTION : GEN/AK*DTS12 * 965

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
RM3220R25	220R 1% MUL MR25	R106
RM3330R25	330R 1% MUL MRS25	R122:33
RM3470R25	470R 1% MUL MR25	R121:34
RM3560R25	560R 1% MUL MR25	R29:31:120:32
RM3680R25	680R 1% MUL MR25	R109:36
RM41K0025	1K0R 1% MUL MR25	R23 5:112 8 9:30 1:41
RM41K5025	1K5R 1% MUL MR25	R111:40
RM41K8025	1K8R 1% MUL MR25	R1 3:102:47
RM42K2025	2K2R 1% MUL MRS25	R10
RM44K7025	4K7R 1% MUL MR25	R7 9:12 4
RM510K025	10KR 1% MUL MR25	R6 8
CC227P0N642	27PF 100V 683-34279	C5 7
CC3100PN642	100PF 100V 683-34101	C65:74:84 6
CC3330PN642	330PF 100V 683-58331	C67:87
CF510K0N2MIN	10KPF 100V WIM FKS2MIN	C73
CF44K70NFKS2	4K7PF 100V WIM FKS2	C70
CF0U100NMKS3	0.1UF 100V WIM MKS3	C2 3 6 8-10 8:20:60 6 8:71 2:88-90
DG4148	DIODE 1N4148	D12-19
VT182PL	TRANSISTOR BC182PL	TR7 9
VTX313	TRANSISTOR ZTX313	TR11 3
VTX510	TRANSISTOR ZTX510	TR10 2
VA356TC	IC UAF356TC/LF356N	IC2 3 6:19
VA3039	INT CCT CA3039 RCA	IC17 8
VD4066CN	IC CD4066CN *STATIC	IC20
PC3470R10V	POT 470R PIH PT10V	P1 2
PC41K0010V	POT 1K0R PIH PT10V	P11 2
PC510K010V	10KR PIH PT10V	P13 4
5NDTSAL		CCT BOARD: CPS/E *ANLOG LOGIC DTS
RM210R025	10R 1% MUL MR25	R43 4:53 56-58:65 9:70 8 9
RM212R025	12R 1% MUL MR25	R73:81 5
RM3220R25	220R 1% MUL MR25	R148
RM3560R25	560R 1% MUL MR25	R41:52
RM3680R25	680R 1% MUL MR25	R28:54:76
RM41K0025	1K0R 1% MUL MR25	R27:50 1:64:146
RM41K2025	1K2R 1% MUL MR25	R82
RM41K8025	1K8R 1% MUL MR25	R61:145
RM42K2025	2K2R 1% MUL MRS25	R11:84
RM43K3025	3K3R 1% MUL MR25	R74
RM43K9025	3K9R 1% MUL MR25	R63
RM44K7025	4K7R 1% MUL MR25	R34 5:66
RM46K8025	6K8R 1% MUL MR25	R5:20:37 8
RM510K025	10KR 1% MUL MR25	R75
RM515K025	15KR 1% MUL MR25	R86
RM539K025	39KR 1% MUL MR25	R33 6
RM6220K25	220KR 1% MUL MR25	R59
RM6560K30	560KR 2% MUL MR30	R101 3
RC71M5025	1M5R 5% MUL CR25	R67
RM3150R25	150R 1% MUL MR25	R68
RM3100R25	100R 1% MUL MR25	R77
RM3270R25	270R 1% MUL MR25	R55
RM45K1025	5K1R 1% MUL MR25	R80
RM512K025	12KR 1% MUL MR25	R83
CC215P0N642	15PF 100V 683-10159	C53
CC227P0N642	27PF 100V 683-34279	C4:11 7
CC3100PN642	100PF 100V 683-34101	C44
CC3330PN642	330PF 100V 683-58331	C77 3
CE12U20KD	2U2F 50V DUB K	C32
CE210U0GM	10UF 25V MUL 030	C33 6:58
CF510K0N2MIN	10KPF 100V WIM FKS2MIN	C1:14:30 9:42:52
CF44K70NFKS2	4K7PF 100V WIM FKS2	C75 P05 C85 P08
CF41K00NFKS2	1K0PF 100V WIM FKS2	C24 9:37:46
CF0U330NMKS	0.33UF 100V WIM MKS4	C50
CF0U100NMKS3	0.1UF 100V WIM MKS3	C16 9:21 3 6 8:34:40 1 3 5:51 9:64:76:91
CV2210P308	V/CAP 2/10PF 80811109	C61-63
DG4148	DIODE 1N4143	D9-11
DZ12V500W3	ZN404 FER	Z1
PC41K0010V	POT 1K0R PIH PT10V	P7
PC42K2010V	POT 2K2R PIH PT10V	P5
PC44K7010V	POT 4K7R PIH PT10V	P3
PM3200R63P	200R SPL 63P	P6
VA1001J	IC TDC1001J8C *STATIC	IC10

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MAIN UNIT ITEM NUMBER : 15DTS12 DESCRIPTION : GEN/AK*DTS12 * 965

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
VA356TC	IC UAF356TC/LF356N	IC5 7:12
VA3039	INT CCT CA3039 RCA	IC9
VA5008N	IC NE5008N *STATIC	IC14
VA79L05ACZ	INT CCT LM79L05ACZ	IC15
VD74LS123N	INT CCT SN74LS123N	IC1
VD74LS373N	INT CCT SN74LS373N	IC11
VD7406N	INT CCT SN7406N	IC4 3
VD74121N	INT CCT SN74121N TEX	IC16
VT212PL	TRANSISTOR BC212PL	TR3
VT182PL	TRANSISTOR BC182PL	TR1 4 5
CAOMIT	CAPACITORS OMITTED	C31
VP1A	TRANSITOR PAD TW1A	Z1
TP15080	CB PIN MR15030 TUC	C/S X8
VD74LS374N	INT CCT DM74LS374N	IC13
CF3220PNFKP2	220PF 100V 5% FKP2	C33
RM3910R25	910R 1% MUL MR25	R110:39
RM3100R25	100R 1% MUL MR25	R114 5:43 4
RM3270R25	270R 1% MUL MR25	R104:35
RM512K025	12KR 1% MUL MR25	R113:42
TBM3906PR	6W 2420-09-75-1061	SK2
TIH2520NR1L	20W HEAD M52-1220-460	SK1
CF3220PNFKP2	220PF 100V 5% FKP2	C15:69
5NDTSTG		CCT BOARD: CPS/L *TRIGGER DTS12
BC095	C /D *DTS12 TRGR*P32B	B
RM210R025	10R 1% MUL MR25	R122
RM212R025	12R 1% MUL MR25	R23 6 7:46 7:80-82 6:90 3 4:123 4
RM215R025	15R 1% MUL MR25	R77:129
RM3100R25	100R 1% MUL MR25	R33:40:121
RM3180R25	180R 1% MUL MR25	R14
RM3220R25	220R 1% MUL MR25	R10 9:70
RM3270R25	270R 1% MUL MR25	R11 5:83
RM3330R25	330R 1% MUL MRS25	R5
RM3390R25	390R 1% MUL MR25	R52:60
RM3470R25	470R 1% MUL MR25	R105
RM3560R25	560R 1% MUL MR25	R12:24
RM41K0025	1K0R 1% MUL MR25	R13 6:54:104:16
RM41K2025	1K2R 1% MUL MR25	R17
RM41K8025	1K8R 1% MUL MR25	R101
RM42K0025	2K0R 1% MUL MR25	R106
RM42K2025	2K2R 1% MUL MRS25	R35:49:50:71:89:91:117
RM42K7025	2K7R 1% MUL MR25	R30:108
RM43K3025	3K3R 1% MUL MR25	R25:56:115:20 7
RM43K9025	3K9R 1% MUL MR25	R75:110
RM44K7025	4K7R 1% MUL MR25	R1 7:18:34:41 5 8:53 5:64:92:107:13 8 9
RM45K6025	5K6R 1% MUL MR25	R2 8:36:109:12
RM46K8025	6K8R 1% MUL MR25	R73 4
RM48K2025	8K2R 1% MUL MR25	R20 2
RM510K025	10KR 1% MUL MR25	R28:51 8 9:87:126
RM512K025	12KR 1% MUL MR25	R3 4:114
RM515K025	15KR 1% MUL MR25	R21:70
RM527K025	27KR 1% MUL MR25	R102 3
RM547K025	47KR 1% MUL MR25	R29:32 8 9:78 9
RM556K025	56KR 1% MUL MR25	R111
RM568K025	68KR 1% MUL MR25	R9
RM6100K25	100KR 1% MUL MR25	R6:31
RM6120K25	120KR 1% MUL MR25	R72
RC71M2025	1M2R 5% MUL CR25	R43 4
RC72M2025	2M2R 10% MUL CR25	R42
RM72M40H2	2M4R 1% 100PPM H2	R125
CC210PON642	10PF 100V 683-10109	C37:51
CC218PON642	18PF 100V 683-10189	C34
CC233PON642	33PF 100V 683-34339	C8
CC239PON642	39PF 100V 683-34399	C45
CC268PON642	68PF 100V 683-34689	C7
CC3100PN642	100PF 100V 683-34101	C16 8:41 2 8:52
CC3330PN642	330PF 100V 683-58331	C2

F A R N E L L I N S T R U M E N T S L T D

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MAIN UNIT ITEM NUMBER : 15DTS12 DESCRIPTION : GEN/AK*DTS12 * 965

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
CC3220PN683	220PF 100V 683-58221	C35 6
CF0U100R352	0.1UF 250V 366-40104	C1:13
CF0U100NMKS3	0.1UF 100V WIM MKS3	C5:10:23:54 6 8 9:70
CF11U00PRNR	1UF 160V 5% R.R ICW	C20
CF41K00NFKS2	1K0PF 100V WIM FKS2	C31:46
CF510K0N2MIN	10KPF 100V WIM FKS2MIN	C3:10-12 4 5:24-30 2 3 8 9:40 3 4 7:50:60-63 8
CE210U0GM	100UF 25V MUL 030	C4 9:53 5:66
CE222U0DM	22UF 10V MUL 030	C57
VT182PL	TRANSISTOR BC182PL	TR4 6-8:14-16
VT212PL	TRANSISTOR BC212PL	TR1-3 5 9:17
DG4148	DIODE 1N4148	D1 4-13
DG922	DIODE 1S922	D2 3
VA311N	INT CCT LM311N 8PIN	IC7:11
VA356TC	IC UAF356TC/LF356N	IC5 6:12
VA710CN	INT CCT LM710CN 14PDIL	IC1
VD14572P	IC MC14572UBCP *STATIC	IC4
VD74LS00N	INT CCT SN74LS00N	IC3:21
VD74LS02N	INT CCT SN74LS02N TEX	IC3:22
VD74LS08N	INT CCT SN74LS08N	IC10
VD74LS221N	IC SN74LS221N NAT	IC17-20
VD7406N	INT CCT SN7406N	IC9
VD74LS74N	INT CCT SN74LS74N	IC2:16
VD74390N	INT CCT SN74390N	IC13-15
VX5M00	5MHZ HC18U	XL1 MC1 X1/L
VS8P	IC SKT 703-1308-010410	V
VS14L	IC SKT 703-1314-010410	V
VS16L	IC SKT 703-1316-010410	V
PC42K2010LH	2K2R PIH PT10LH	P4 5
PC44K7010LH	4K7R PIH PT10LH	P6
PC510K010LH	10KR PIH PT10LH	P1 7
PC522K010LH	22KR PIH PT10LH	P2 3
RC71M0025	1MOR 5% MUL CR25	R95:128
CC227P0N642	27PF 100V 683-34279	C65
DZ15V600W5	ZPD5.6 ITT	Z1
CC3180PN683	180PF 100V 683-58181	C22:49
SB0054	3ST/A *DTS12 TRIG 7W	SW2A-2G
TP7401	CB PIN 12W 1-163740-1	FIT T/S
TP7404	CB PIN 6W 1o3740-4 AMP	FIT T/S
CE14U70LM	4U7F 63V 015-90044	C6
CC3470PN630	470PF 100V 630-18471	C59
RA0MIT	RESISTORS OMITTED	R37
RM46K2025	6K2R 1% MUL MR25	R57
CC41K00N630	1K0PF 100 630-19102	C17
CE233U0FES	33UF 16V SMVB ECC	C64
MC1	CERAMIC BEAD SDP1 MET	XL1
TP15080	CB PIN MR15080 TUC	C/S X9
CF0U220NMKS4	0.22UF 100V MKS4	C71
VD74LS32N	INT CCT SN74LS32N	IC23
TBM2504PR	4W 7478-22-05-3041	SK2
TBM2512PT	12W 4094 22 05 2125	TB81 2 3
TBM2504PS	4W 6410 22-27 2041	SK3
TIH2520NT1L	20W M52-1220-260	SK1
VTX313	TRANSISTOR ZTX313	TR13
CF41K00NFKP2	1K0PF 100V 5% FKP2	C21
CASOT	CAP SELECT ON TEST	C57
5NDTSL		CCT BOARD: CPS/F *LOGIC DTS12
BC096	C /D *DTS12 LOG *P323	3
RM3180R25	180R 1% MUL MR25	R1 8
RM3820R25	820R 1% MUL MR25	R7:13-20
RM41K0025	1K0R 1% MUL MR25	R16
RM44K7025	4K7R 1% MUL MR25	R3 4 6 9:10 2 3:21
RM518K025	18KR 1% MUL MR25	R15
RM522K025	22KR 1% MUL MR25	R17
CC210P0N642	10PF 100V 683-10109	C20
CE222U0DM	22UF 10V MUL 030	C21
CE310U0DM	100UF 10V MUL 030	C37
CF0U100NMKS3	0.1UF 100V WIM MKS3	C22:38 9
CF510K0N2MIN	10KPF 100V WIM FKS2MIN	C2 4 6-19:23-29:31-36
SB0052	3ST/A *DTS12 LOGIC 4W	SW2
SB0053	3ST/A *DTS12 LOGIC 5W	SW1
LD134R	LED RED T1 3/4 MV5753	LED1
VD472114AP1	IC TMM314A PL-1*STATIC	IC28-31
VD7407N	INT CCT SN7407N	IC9

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MAIN UNIT ITEM NUMBER : 15DTS12 DESCRIPTION : GEN/AK*DTS12 * 965

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
VD74LS00N	INT CCT SN74LS00N	IC2 4 6
VD74LS04N	INT CCT SN74LS04N	IC10 1
VD74LS08N	INT CCT SN74LS08N	IC1 8
VD74LS32N	INT CCT SN74LS32N	IC7
VD74LS74N	INT CCT SN74LS74N	IC12 4 6:33
VD74LS112N	INT CCT SN74LS112N	IC26
VD74LS157N	INT CCT SN74LS157N	IC17 8:20 1 4 5
VD74LS197N	INT CCT SN74LS197N	IC19
VD74LS221N	IC SN74LS221N NAT	IC27
VD74LS393N	INT CCT SN74LS393N	IC22 3:32
VS14L	IC SKT 703-1314-01041D	V
VS16L	IC SKT 703-1316-01041D	V
VS18L	IC SKT 703-1318-01041D	V
RM42K7025	2K7R 1% MUL MR25	R24
LD134G	LED GRN T1 3/4 MV64530	LED2
TBM3902PR	2W 2420-09-75-1021	SK2
TBM2504PR	4W 7478-22-05-3041	SK1
RM3330R25	330R 1% MUL MRS25	R14
TP15080	CB PIN MR15080 TUC	C/S X4
TL675191T	14W PROG HEADER	SW3
TBM2512PT	12W 4094 22 05 2125	SK3
CC510K0861	10KPF ERI 861T/25	C
RC3100R16	100R 5% MUL CR16	R
RC72M2025	2M2R 10% MUL CR25	R735
PM44K7016N	4K7R TYPE 16PE LIN	P701
PM71M0016	1MOR 16PE LIN 4MM SPI	P704
PC0658308	4ZP/A *POT 100KR ?C	P105:205
PC0658310	4ZP/A *POT 10KR ?C	P608
LD134R	LED RED T1 3/4 MV5753	LED717
LD134K	LED T1 3/4 MTG KIT	LED717
VTBF462	TRANSISTOR BF462	TR306-09:706
PM6220K16	220KR 16PE LIN 6MM SPI	P702
VA7912CT	INT CCT LM7912CT	IC702
LD134G	LED GRN T1 3/4 MV64530	LED717
PM6220K16N4	220KR 16PE LIN 4MM SPI	P705
DS6394	SELEC DS6394 RCA ONLY	SCR750
VA40147	INT CCT. TY40147 MOT	IC750
PM6100K12P	100KR LIN 12PE	P501
VALM7812CT	INT CCT LM7812CT	IC701
4NDTSCR		ASSEMBLY: SUB/C *CTR ASM
5NDTSM		CCT BOARD: CPS/D *DTS12 MAIN
5SDTMS		CCT BOARD: CPS/B *SCOPE STD
5SDTMCH1		CCT BOARD: CBP/B *CH1 COMPS
RM212R025	12R 1% MUL MR25	R152 3:70 3 P09:R167 P23
RM247R025	47R 1% MUL MR25	R157 8:65 6 9
RM282R025	82R 1% MUL MR25	R151
RM3180R25	180R 1% MUL MR25	R162
RM3390R25	390R 1% MUL MR25	R163
RM3910R25	910R 1% MUL MR25	R168
RM3680R25	680R 1% MUL MR25	R160 4
RM3820R25	820R 1% MUL MR25	R159
RM41K0025	1KOR 1% MUL MR25	R171
RM41K5025	1K5R 1% MUL MR25	R154:61
RM43K3025	3K3R 1% MUL MR25	R156
RM510K025	10KR 1% MUL MR25	R155
CC282PON642	82PF 100V 633-34829	C154
CC11P80N642	1P8F 100V 633-09138	C152
CC41K00861	1KOPF ERI 861/AX	C156
CC18P20N642	8P2F 100V 633-09828	C153
DG4148	DIODE 1N4148	D150 1
PC41K0010V	POT 1KOR PIH PT10V	P150
VT182PL	TRANSISTOR BC182PL	TR150 1
VTBF199	TRANSISTOR BF199	TR155
VTX313	TRANSISTOR ZTX313	TR153 4
VTX510	TRANSISTOR ZTX510	TR152
5SDTMCH2		CCT BOARD: CBP/C *CH2 COMPS
RC12R2025	2R2 5% MUL CR25	R264 8
RM210R025	10R 1% MUL MR25	R267:74
RM212R025	12R 1% MUL MR25	R252 3:70:89
RM247R025	47R 1% MUL MR25	R257 8:65 6 9
RM282R025	82R 1% MUL MR25	R251
RM318OR25	180R 1% MUL MR25	R262

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MAIN UNIT ITEM NUMBER : 15DTS12 DESCRIPTION : GEN/AK*DTS12 * 965

FARNELL PART NUMBER	DESCRIPTION	*---------- CIRCUIT REFERENCE ----------*
RM390R25	390R 1% MUL MR25	R263:75 8
RM680R25	680R 1% MUL MR25	R260
RM820R25	820R 1% MUL MR25	R259
RM41K0025	1K0R 1% MUL MR25	R273
RM41K5025	1K5R 1% MUL MR25	R254:61
RM43K3025	3K3R 1% MUL MR25	R256:77
RM510K025	10KR 1% MUL MR25	R255:76
CC218P0N642	18PF 100V 683-10189	C253
CC282P0N642	82PF 100V 683-34829	C254
CC41K00861	1K0PF ERI 861/AX	C260
CC11P80N642	1P8F 100V 683-09188	C252
CC1oP80N642	6P8F 100V 683-09688	C262
CF510K0N2MIN	10KPF 100V WIM FKS2MIN	C261
DG4148	DIODE 1N4148	D250 1 5
PC44K7010V	POT 4K7R PIH PT10V	P250
VT182PL	TRANSISTOR BC182PL	TR250 1 6 7
VTBF199	TRANSISTOR BF199	TR255
VTX313	TRANSISTOR ZTX313	TR253 4
VTX510	TRANSISTOR ZTX510	TR252
5SDTMX		CCT BOARD: CBP/C *X AMP COMPS
CAOMIT	CAPACITORS OMITTED	C507
RC6470K25	470KR 5% MUL CR25	R536
RC6680K25	680KR 5% MUL CR25	R535
RC6820K25	820KR 5% MUL CR25	R534
RM212R025	12R 1% MUL MR25	R502 4 8:18:24 6
RM3100R25	100R 1% MUL MR25	R506:25
RM3220R25	220R 1% MUL MR25	R532
RM3470R25	470R 1% MUL MR25	R507:19:27
RM3680R25	680R 1% MUL MR25	R520
RM41K2025	1K2R 1% MUL MR25	R509
RM41K5025	1K5R 1% MUL MR25	R516
RM42K2025	2K2R 1% MUL MRS25	R530:40 1
RM42K7025	2K7R 1% MUL MR25	R529
RM44K3025	4K3R 1% MUL MR25	R510
RM44K7025	4K7R 1% MUL MR25	R503:28
RM48K2025	8K2R 1% MUL MR25	R514:31
RM510K025	10KR 1% MUL MR25	R517
RM512K025	12KR 1% MUL MR25	R522
RM515K076	15KR 5% WEL FA86	R505:23
RM547K025	47KR 1% MUL MR25	R539
RM582K025	82KR 1% MUL MR25	R537
RM6120K25	120KR 1% MUL MR25	R511 5
RM6150K25	150KR 1% MUL MR25	R512:21
RM43K9025	3K9R 1% MUL MR25	R501:13
RLINK24	24 SWG TC LINK	R533:42
CC15P0861	5P6F ERI 861/N470	C502 4
CC3220P831H	220PF ERIE 831/HI-K	C503
CE3220UFM	220UF 16V MUL 031	C501 5
CF522K0T352	22KPF 400V 368-50223	C506
CF510K0N2MIN	10KPF 100V WIM FKS2MIN	C503
DG4148	DIODE 1N4148	D501-4
PC3470R10V	POT 470R PIH PT10V	P504 6
PC42K2010V	POT 2K2R PIH PT10V	P503 5
PC6220K10V	POT 220KR PIH PT10V	P507
PM6100K63P	100KR SPL 63P	P502
VT182PL	TRANSISTOR BC182PL	TR501 3-5
VTBF462	TRANSISTOR BF462	TR502 6 9
VTX313	TRANSISTOR ZTX313	TR507
VTX510	TRANSISTOR ZTX510	TR508
ZC1M10	1000UH 552-5373-49-020	L501 2
MC2	CERAMIC BEAD SDP2 MET	R505:23 X2/L
CC3150PN642	150PF 100V 683-34151	C509
5SDTMY		CCT BOARD: CBP/C *Y AMP COMPS
CAOMIT	CAPACITORS OMITTED	C301 2 6-8
RM212R025	12R 1% MUL MR25	R303 5:10 6 7:22
RM222R025	22R 1% MUL MR25	R330
RM247R025	47R 1% MUL MR25	R314
RM3100R25	100R 1% MUL MR25	R307 8:19:20
RM3330R25	330R 1% MUL MRS25	R306 9:18:21
RM3560R25	560R 1% MUL MR25	R324 8
RM41K0025	1K0R 1% MUL MR25	R323

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FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
RM41K2025	1K2R 1% MUL MR25	R329
RM41K8025	1K8R 1% MUL MR25	R312
RM42K7025	2K7R 1% MUL MR25	R313
RM511K084	11KR 5% FA84*RM522K075	R301:25:32 3
RM515K076	15KR 5% WEL FA86	R311 5
CC15P60861	5P6F ERI 861/N470	C310 1
CC41K00861	1K0PF ERI 861/AX	C304
CC247P0N642	47PF 100V 643-34479	C312
CF0U100T352	0.1UF 400V 368-50104	C300 3
CF44K70NFKS2	4K7PF 100V WIM FKS2	C313
CV210P	10PF 109-2991-010 BLU	C305
CF42K20NFKS2	2K2PF 100V WIM FKS2MIN	C309
DG4148	DIODE 1N4148	D301-5
PC42K2010V	POT 2K2R PIH PT10V	P301
VT182PL	TRANSISTOR BC182PL	TR304 5
VTX313	TRANSISTOR ZTX313	TR302 3
DZ210V00W5	ZPD10 ITT	Z301
DZ15V600W5	ZPD5.6 ITT	Z302 3
MC2	CERAMIC BEAD SDP2 MET	R301:25:32 3 X1/L:R311 5 X2/L
RM3150R25	150R 1% MUL MR25	R331
PC3100P10LH	100R PIH PT10LH	P302
5SDTMPS		CCT BOARD: CPS/F *P/SUPPLY COMPS
RC810M025	10MR 10% MUL CR25	R727
RG71M0037	1MOR 5% MUL VR37	R707-14
RM3390R25	390R 1% MUL MR25	R706
RM3560R25	560R 1% MUL MR25	R732 3
RM3680R25	680R 1% MUL MR25	R715:41
RM3820R25	820R 1% MUL MR25	R703
RM42K2025	2K2R 1% MUL MRS25	R701:16 7
RM41K2025	1K2R 1% MUL MR25	R750
RM44K7025	4K7R 1% MUL MR25	R718:31 9
RM48K2025	8K2R 1% MUL MR25	R737
RM510K025	10KR 1% MUL MR25	R719
RM568K025	68KR 1% MUL MR25	R740
RM6150K30	150KR 2% MUL MR30	R725
RM6330K30	330KR 2% MUL MR30	R721-3 6
RM6560K30	560KR 2% MUL MP30	R724
RM41K8030	1K8R 2% MUL MR30	R738
RM522K075	22KR 5% FA85*RM311K084	R734
RAOMIT	RESISTORS OMITTED	R736
CC347GP831H	470PF ERI 831/HIK	C721
CC44K70ZRDX	4K7PF 4KV RDX625	C720 2
CC520K0ZHD25	20KPF 2KV HD25K32UN	C723
CE3220UKEK	220UF 50V KMVB ECC	C708:10
CF510K0N2MIN	10KPF 100V WIM FKS2MIN	C709
CC3330PN642	330PF 100V 643-59331	C724
CE12U20UE	2U2F 450V SMT ECC	C711-18
DBW02M	BRDG RECT W02M	BR701
DG4007	DIODE 1N4007	D706-09
DG4148	DIODE 1N4148	D716 8:20
PC42K2010V	POT 2K2R PIH PT10V	P703
PAOMIT	POTENTIOMETERS OMITTED	P701 2 4 5
VAOMIT	TRANSISTORS/ICS OMITTE	IC701 2:TR706
VT182PL	TRANSISTOR BC182PL	TR704
VT212PL	TRANSISTOR BC212PL	TR701 3
VTBUX87	TRANSISTOR BUX87	TR702
VTX313	TRANSISTOR ZTX313	TR705
DZ233V00W5A	BZA79C33 MUL	Z701
TBM2508PR	8W 7478 22-05 3081	SK1
RM6180K30	180KR 2% MUL MR30	R720
CC510K0Y621	0.01UF 1000V RAX621	C719
RM522K025	22KR 1% MUL MR25	R730
MC2	CERAMIC BEAD SDP2 MET	R734 X2/L
MC1	CERAMIC BEAD SDP1 MET	BR701 X1/L

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MAIN UNIT ITEM NUMBER : 15DTS12 DESCRIPTION : GEN/AK*DTS12 * 965

FARNELL PART NUMBER	DESCRIPTION	CIRCUIT REFERENCE
CF0U100LMKS	0.1UF 63V WIM MKS2MIN	C707
DG240	DIODE GP0240	D710 1) FIT ACROSS 2 PITCHES:D719
CF0U220LMKS2	0.22UF 63V WIM MKS2	C725
CP510K0TMKT1	10KPF 400V 5% MKT1.50	C706
BC099	C /D *DTS MAIN *S12B	B
MM5L	BER OXIDE WASHER NW5S	TR502 6
MB0057	4SV/D *M2.5 BUSH NAT	TR502 6
YP7130BLK	BLACK 24AWG UL1430	LINK
RA0MIT	RESISTORS OMITTED	R172:271 2 9:80-88
CA0MIT	CAPACITORS OMITTED	C155:255-59
DA0MIT	DIODES OMITTED	D252-254:Z250
PA0MIT	POTENTIOMETERS OMITTED	P252
VA0MIT	TRANSISTORS/ICS OMITTE	TR258-60
RM212R025	12R 1% MUL MR25	R344
CE41K00GE	1KUF 25V KMVB ECC	C701 2
CF0U220LMKS2	0.22UF 63V WIM MKS2	C750
CE44K70FTM	4K7UF 16V TSW TAG MNT	C753
CF0J100LMKS	0.1UF 63V WIM MKS2MIN	C751 2
FH5229	FUSEHOLDER 5229	F750
FF1A0013	FUSE TDC13 1AMP	F750
DBP02	BRDG RECT KBP02	BR750
DZ16V200W5	ZPD6.2 ITT	Z750
DLINK24	24 SWG TC LINK	D253
VLINK24	24 SWG TC LINK	TR259 E TO C
YT24	T/C WIRE 24SWG	LINKS X19
TP15080	CB PIN MR15080 TUC	C/S X33 T/S X25
ZC0858301	3Z6/B *CHK DT12/5	L700
ZR0272	2SR/E *DTS12	TX701
RM3100P30	100R 2% MUL MR30	R728 9
CE247U0SSMT	47UF 35JV SMT ECC	C703 4
FT500M11	500MA A/S TDC11	F701
35DTS12		CASING: CAS/C *DTS12

THE ADDITIONAL FEATURES OF THE DTS12P

The X-Y plotter option for the DTS12 provides analogue X-Y outputs which allow the instrument to interface with an X-Y or Y-T chart recorder to obtain a 'hard copy' of the stored waveform.

There are four outputs associated with this option. These are made available on 4 mm sockets on the instrument's rear panel. These signals are 'Plot-Y', 'Plot-X', "Pen-lift" and OV. The 'Plot-Y' output provides the calibrated amplitude of the stored waveform and the 'Plot-X' output provides a calibrated timebase. The plotting speed of both outputs can be varied using the instrument's main timebase switch. The 'Pen-Lift' output, when used in conjunction with the appropriate recorder input, allows the pen to be lowered and raised automatically at the beginning and end of a sweep.

X-Y PLOTTER OUTPUT SPECIFICATION

Y-Output

AMPLITUDE	100mV per division of screen. Bipolar signal with 0V corresponding to the screen centre.
ACCURACY	± 3% of full scale.
OUTPUT IMPEDANCE	approximately 50 ohms.

X-Output

AMPLITUDE	100mV per division of screen. Positive ramp from 0V.
SWEEP TIMES	1s to 5000s per complete sweep in 1-2-5 steps, selected by the timebase switch, the sweep time in seconds corresponding directly to the time/division settings in milliseconds.
ACCURACY	± 3% of full scale.
OUTPUT IMPEDANCE	approximately 50 ohms.

PEN LIFT - output

DESCRIPTION OF SIGNAL	TTL levels. '1' to lift pen. '0' to lower pen.
DRIVE CAPABILITY	Low level output current = 32mA.

USING THE PLOTTER OPTION

Setting Up Procedure:

1. Connect the DTS12P to an X-Y, or Y-T recorder as shown in Figure 1.

2. Set up the controls of the chart recorder as required noting the following:

   a) The Plot-X output is calibrated such that 0V corresponds to the left hand edge of the screen graticule and +1.0V to the right hand edge. During a plot the signal at this output ramps at a linear rate from 0V to +1.0V.

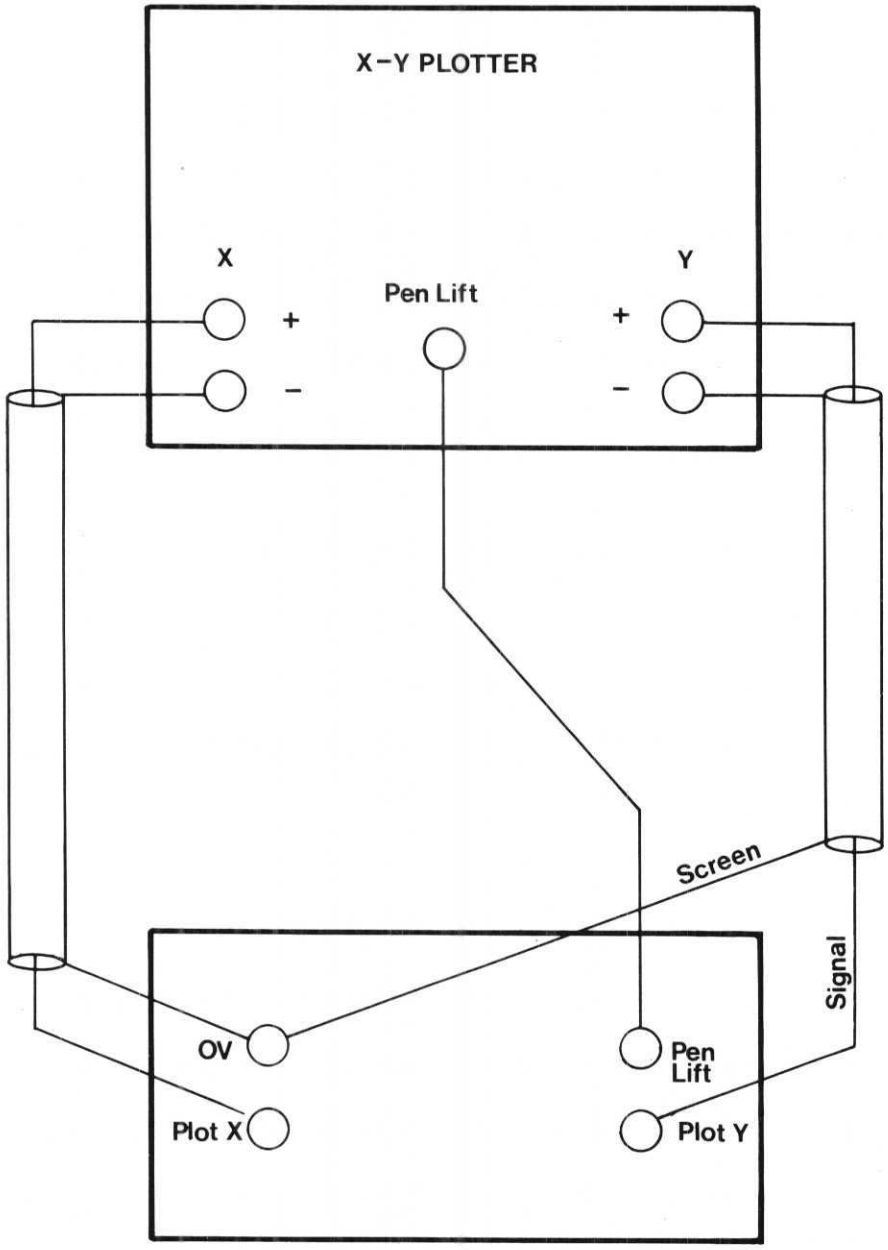
   b) The Plot-Y output is calibrated such that 0V corresponds to the screen centre, +400mV to the top edge of the screen graticule and -400mV to the lower edge. During a plot the signal at the Plot-Y output varies between these limits according to the amplitude of the stored signal.

Obtaining a Plot

1. Store the required signal(s) on the display of the DTS12P using the 'Hold Display' button, making a record of the timebase switch setting if required. Note that it is only possible to plot traces which have already been stored and held. It is not possible to plot out a signal as it is being fed in.
2. Select the required plotting speed using the main oscilloscope timebase switch. The plotting time in seconds corresponds directly to the time/div. setting in milliseconds, eg, if the timebase switch is set at 10ms/div. a plot will take 10 seconds to complete. The plotting time can be varied in this way from 1s to 5000s in 1-2-5 steps.

FIGURE 1

DTS12P - X-Y Plotter Connections



REAR PANEL OF DTS12P

Note If the 'Pen Lift' facility is required, check that the DTS12P output is electrically compatible with the corresponding plotter input.

To ensure that the Plot-Y signal does not exceed the slewing capabilities of the chart recorder, signals containing high dY/dT components will require slower plotting speeds than those that vary slowly. A plotting time of 10 to 20 seconds will yield a good record of most signals and it is unlikely that plotting times outside the range 5 to 200 seconds will ever be needed.

3. Only one of the two possible stored traces may be plotted at a time. Select which one it is desired to plot using the Ch1/Ch2 button located near the Trigger Level control on the front panel. If one channel is turned off and the oscilloscope is in the signal channel mode, this button is inoperative.

4. Initiate a plot by pressing the 'Reset/Plot' button once. At the end of a plot the pen will remain at the last plotted position.

5. To reset the recorder axes to the starting position, press 'Reset/Plot' a second time. Further plots can be initiated in the same way, selecting Ch1/Ch2 as desired.

X-Y PLOTTER BOARD CIRCUIT OPERATION

When the X-Y Plotter option is fitted to a DTS12 the control signals associated with the write address counter and the display memory are derived from the X-Y board. They are selected either from the original control signals obtained from the logic board or from a set of signals generated by the X-Y Plotter board itself. The original signals are enabled and selected until the 'Hold Display' button is pressed. At this point the normal control signals are disabled and the write address counter becomes a second read address counter controlled directly from the X-Y Plotter board. When the 'Reset/Plot' button is pressed, the 'WRITE' half of 'SYSTEM CYCLE' is utilised to read through the display memory at a rate determined by the plotting speed selected. The memory data is latched and converted on the X-Y Plotter board to give the Y-analogue output. The X-output is generated by converting to analogue form the outputs of a digital counter which is clocked from zero to full scale to give an analogue ramp or timebase.

DTS12P - CALIBRATION PROCEDURE - X-Y PLOTTER BOARD

First ensure that the calibration procedure for the real-time operation and the storage section has been completed. With the cover still removed, and observing usual safety precautions, power up the unit in the storage mode with the timebase ('t.b.' hereafter) switch set to 0.5ms/div. Ensure all trigger and storage mode switches are out except 'Free Run'. Select Ch1 d.c. coupled and position the trace as accurately as possible at the screen centre.

1. Press 'Hold Display' and, with a d.v.m., monitor the 'Plot X' output on the rear panel with respect to the OV output. Check that 'Plot X' is at OV.

2. Press the 'Reset/Plot' button (R.P. hereafter) once and check that the voltage at 'Plot X' rises to approximately 1V. Adjust P1 on the X-Y Plotter Board to give 1.000V $\pm$ 10mV.

3. Set the t.b. switch to 2s/div, and press the R.P. button twice. Adjust P3 fully clockwise and, monitoring the Plot Y output with respect to OV, adjust P2 to give OV $\pm$3mV. Set the t.b. switch to 0.5ms/div.

4. Release the display. Position the trace as accurately as possible to +4 divisions deflection and hold the display again.
   Set the t.b. switch to 2s/div.
   Press the R.P. button twice and adjust P3 to give +0.4V $\pm$3mV at the 'Plot Y' output. Set the t.b. switch to 0.5ms/div.

5. Release the display and, using a signal generator, adjust the DTS12P front panel controls as necessary to store and hold two traces on the screen. On Ch1, store a few cycles of a sine wave in the top half of the screen and, on Ch2, store a few cycles of a square wave in the bottom half of the screen. Set the t.b. switch at 10ms/div.

Take another oscilloscope and set the sensitivity of both channels to 0.1V/div. (with X1 probes). Switch the same oscilloscope into the X-Y mode, setting OV in the Y axis to the centre of the screen and OV in the X axis to the left hand side of the screen. With this oscilloscope monitor the 'Plot-X' and 'Plot-Y' outputs on the DTS12P.

Ensure that the Plot Ch1/Ch2 option switch on the DTS12P front panel is in the Ch1 position and press the R.P. button once to reset the outputs and a second time to start the plot. Check that the trace on the screen of the second oscilloscope follows the shape of the trace stored on Ch1 of the DTS12P and is completed in 10 seconds (the plot can be repeated by resetting and starting the plot using the R.P. button).

Reset the outputs at the end of the plot, select 'Plot Ch2' and check the timing and shape of this plot.

THE ADDITIONAL FACILITIES OF THE DTS12T

The I/O board provides the DTS12T with the following additional facilities:

1. A second 1K memory which can be used in an identical fashion to the existing display memory. It is therefore possible to store 2 screens of data and choose which is to be displayed or updated at any one time. This facility is controlled by 2 latched pushbuttons on the front panel, marked 'A' and 'B' respectively. The one that is in the 'in' position is the memory that is being displayed and will be overwritten by any new incoming data.

2. An X-Y or Y-T plotter interface. This facility allows the oscilloscope to be connected to an analogue plotter to obtain a hard copy of the stored waveform. The interface is in the form of four 4 mm connectors on the rear panel of the instrument. The outputs are PLOT X, PLOT Y, OV and PEN LIFT. The interface is controlled by a further 2 pushbuttons on the front panel. The CH1/CH2 button when in the dual channel mode selects which of the displayed traces is to be plotted. The RESET/PLOT button, when pushed once initiates a plot, and when pressed a second time resets the outputs to their start position.

3. A GPIB (IEEE488) interface. The oscilloscope can be configured as a 'talker' or a 'listener', i.e. the screen data can be transferred to the controlling microcomputer or signal data can be sent from the microcomputer to the oscilloscope. In addition, the bus controller can remotely control the oscilloscope's 'hold' facility and position a dot cursor on the screen of the DTS12.

4. An interface to the BBC model B microcomputer. This interface provides similar facilities to the IEEE interface. Software for the BBCuC is available which provides a variety of display, signal processing and storage facilities.

SPECIFICATION

Memory size

Total memory capacity of oscilloscope: 2K bytes divided into two "screens" each of 1K byte

X-Y Output

Y-Output

Amplitude: 1V/div. A unipolar signal with 0V corresponding to the bottom of the screen and +8V to the top. Accuracy: ±3% of full scale. Output impedance: 1kΩ approx.

X-Output

Amplitude: 1V/div. A positive ramp from 0V. Sweep time: 20 seconds or 40 seconds. Accuracy: ±3% of full scale. Output impedance: 1kΩ approx.

Pen Lift Output

Control: TTL high corresponds to 'lift pen'.
TTL low corresponds to 'lower pen'.

Drive capability: high level output current 2.6mA

Outputs

4 mm sockets on rear panel of oscilloscope.

GPIB interface

Bus configuration

Talker and Listener functions available. External device can read from and write to display memory and control the 'hold' function, but not other oscilloscope functions. A 'dot' cursor can be positioned on the oscilloscope screen.

Device address

Factory set to 5. Can be reset to alternative address using internal DIL switches.

Connection

Via standard IEEE bus connector on rear of oscilloscope.

BBCuC interface

Facilities

The same facilities are available as for the GPIB interface. Data transfer rate is greater that 2K-bytes per second.

Connection

Via a 20-way IDC connector mounted on rear of oscilloscope. Connection made to the USER PORT of the BBC microcomputer via a 1m IDC cable supplied with the DTS12T.

THE OPERATION OF THE MEMORY A/B FACILITY

The DTS12T has 2K of signal memory organised to enable the user to store a full screen's worth of information whilst updating the screen with fresh data.

The 2K of signal memory is presented in the form of two 1K blocks named memory A and memory B as defined on the front panel buttons. When button A is pressed in, then A is the 'live' memory, i.e. the memory which is displayed on the oscilloscope screen and will be updated by any new incoming data. If button B is now pressed in, then the displayed signals are stored internally and the contents of memory B, previously unseen, are displayed on the screen since B is now the 'live' memory. If the 'hold' button is pressed in, then the user can toggle freely between the stores without fear of erasing one with new data.

The Input/Output facilities of the DTS12T always operate in conjunction with the 'live' memory. Thus, when sending data to a microcomputer it is the signal data seen on the display that is transferred and, when receiving signal data, the data is stored in the 'live' memory thus overwriting the existing display.

Notes:

1. It is not possible to save just one trace of a dual channel display using this facility, since the 'swop' operation acts upon the full 1K store.

2. It is not possible to view 4 traces simultaneously, only one store can be viewed at any one time.

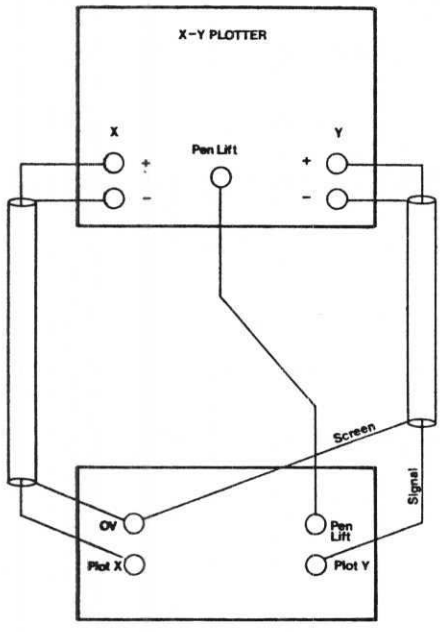
3. The maximum length of a trace in the single channel mode is 1K bytes and in the dual channel mode, 512 bytes.

OPERATION OF THE X-Y PLOTTER OUTPUT

The X-Y plotter output provides analogue X-Y outputs which allow the instrument to interface with an X-Y or Y-T pen recorder to obtain a 'hard copy' of the stored waveform.

There are 4 outputs associated with this interface. These are made available on 4 mm sockets on the instrument's rear panel. These signals are 'Plot Y', 'Plot X', 'Pen Lift' and OV. The plot Y output provides the calibrated amplitude of the displayed waveform and the Plot X output provides a calibrated timebase. The plotting speed of both outputs can be selected to give a plotting time of 20s or 40s according to the position of a DIL switch on the I/O board. The Pen Lift output, when used in conjunction with the appropriate recorder input, allows the pen to be lowered and raised automatically at the beginning and end of a sweep.

X-Y Plotter Connections



REAR PANEL OF DTS12P

N.B. If the Pen Lift facility is required, check that the DTS12T output is electrically compatible with the corresponding plotter input.

Setting up procedure

1. Connect the DTS12T to the recorder as shown in figure 1.

2. Set up the controls of the recorder as required, noting the following;

   a) The Plot X output is calibrated such that 0V corresponds to the left hand edge of the screen graticule and +10V to the right hand edge. During a plot the Plot X output signal ramps in a linear fashion from 0V to 10V.

   b) The Plot Y output is calibrated such that 0V corresponds to the bottom edge of the screen graticule and +8V to the top edge. During a plot the signal at this output varies between these limits according to the amplitude of the stored signal.

3. If a slow plotting speed is required (perhaps for a signal containing very high dv/dt components), then set DIL switch 6 on the I/O board to ON. This sets the plotting time to 40s; with the switch OFF the plotting time is 20s. Access to this switch is obtained by removing the instrument covers and the plate on the rear panel which houses the edge connectors for the logic board and the I/O board.

Obtaining a plot

1. Ensuring that the oscilloscope is in the storage mode, store the required signal on the screen using the 'hold' button.

2. In the dual channel mode, only one of the two traces may be plotted at a time. Select the one it is desired to plot using the 'Plot CH1/CH2' button on the front panel. The state of this button is ignored when the instrument is in the single channel mode.

3. Initiate a plot by pressing the 'Reset/Plot' button once. At the end of the plot the pen will remain in the last plotted position.

4. To reset the recorder axes to the start position, press 'Reset/Plot' a second time. Further plots can be initiated in the same way, selecting CH1/CH2 as desired if in the dual channel mode.

Notes:

1. The Plotter outputs are disabled when either of the buttons 'Store' or 'Hold' are not pressed in and also when a BBCuC is connected to the DTS12T.

2. It is only possible to plot traces which have already been stored, it is not possible to plot a signal as it is being fed in.

THE DIGITAL INTERFACES - GENERAL INFORMATION

The following information is common to both the BBC microcomputer and the GPIB interfaces.

Data format

The signal has an amplitude resolution of 8 bits, thus the data word 00000000 corresponds to a point at the bottom edge of the screen, and 11111111 to a point at the top edge. The words 10000000 or 01111111 (half full scale) will correspond approximately but not necessarily exactly to the vertical centre of the screen defined by the graticule. The data is stored in the oscilloscope and transferred over the interfaces in the form of 8 bit binary bytes. It should be noted that the first 4 locations of the display memory are never addressed by the oscilloscope, so only 1020 bytes of true signal data are available. The cpu in the oscilloscope compensates for this by creating 4 bytes (set to the value of the 5th byte) to give a full 1K.

When transferring signal data over the digital interfaces with the DTS12T in the single channel mode, the 512 bytes of data corresponding to the left half of the trace is transferred first, followed by the 512 bytes corresponding to the right half. The first byte transferred therefore corresponds to the beginning of the trace and the last byte to the end. In the dual channel mode the first 512 bytes transferred represent the channel 2 trace and the next 512 bytes respresent the channel 1 trace. This format must be adhered to when writing display data back to the scope from the microcomputer.

Using the interfaces

To communicate with a microcomputer the oscilloscope must be in the storage mode. If signal data is to be sent from the controller to the instrument screen, the the 'hold' button should be pressed to prevent the transferred data being immediately overwritten by fresh data from the analogue to digital converter.

Software

The software routines in the DTS12T which control the communication with the GPIB and the BBCuC are initiated by interrupts received from the external microcomputer. Since the microcomputer can require the DTS12T to perform one of a number of functions in response to these interrupts it is necessary at the start of a data exchange for the microcomputer to send a control byte to the oscillocope in order that the instrument will know how to respond to the interrupts that will follow.

Software for the BBCuC interface is supplied with the DTS12T and a listing of a program for using the Commodore PET as the GPIB controller with the bus interface is also available. For those wishing to use the GPIB interface with a different controller, a detailed description of the software required to drive the GPIB interface is included in a later section of this manual.

THE GPIB INTERFACE

Specification

Conforming to the IEEE488 standard, the DTS12T GPIB interface can configure the oscilloscope as a talker or a listener. In the listener mode the DTS12T can receive signal data which is displayed on the screen, cursor data which defines the position of a dot cursor on a displayed trace, or instructions to remotely hold or release the display. In the talker mode the DTS12T can send signal data or two bytes which describe the status of the instrument to the bus controller.

The bus address of the DTS12T is factory set to 5 but can be altered by changing the position DIL switches 1 to 5 on the I/O board. Switch 1 corresponds to the least significant digit. Access to these switches is obtained by removing the instrument covers and the plate on the rear panel which houses the edge connectors for the logic board and the I/O board.

Using the interface

The bus interface provides a standard GPIB socket on the oscilloscope's rear panel. This should be connected by a standard GPIB interconnecting cable to the bus controller in the usual way. To communicate to the bus the oscilloscope must be in the storage mode. If signal data is to be sent from the controller to the instrument screen, then the 'hold' button should be pressed to prevent the transferred data being immediately overwritten by fresh data from the analogue to digital converter.

Software

A listing of a program for the Commodore PET to implement all the available bus interface functions is available. For users wishing to use a different controller, there follows a description of the necessary interface software.

The software routines in the DTS12T which control the communication with the GPIB are initiated by interrupts received from the external microcomputer. Since the microcomputer can require the DTS12T to perform one of a number of functions in response to these interrupts it is necessary at the start of a data exchange for the microcomputer to send a control byte to the oscilloscope in order that the instrument will know how to respond to the interrupts that will follow.

The significance of the bits in this control byte are listed below:

bit no	mnemonic	function
0	TXDA	send data byte
1	RXDA	receive data byte
2	RXCR	receive cursor byte
3	RXCL	receive control byte
4	TXS1	send status word 1
5	TXS2	send status word 2
6	HLD	hold display
7	RLS	release display

The data held in the oscilloscope is in the form of 8 bit binary bytes rather than ASCI. The ease with which a controlling device can be programmed to communicate with the DTS12T depends upon the capability of the controller to handle data in this form. Some controllers are only capable of receiving one binary byte per addressing sequence and therefore to extract the 1K display data from the DTS12T will require 1024 addressing sequences. Other controllers allow the user direct access to the I/O registers used for BUS transactions, thus overcoming such limitations of high level bus commands. The Commodore PET falls into this second category.

Listed below are the software sequences required to perform all the DTS12T bus functions.

Program sequences

The usual bus handshake protocol is assumed in all the following transactions.

1. To read 1K of display memory from DTS12T to controller:

    1.1 Address oscilloscope to listen (send listen address with ATN low).
    1.2 Send instruction byte to 'scope with bit 0 (TXDA) set (01 hex).
    1.3 Address 'scope to talk (send talk address with ATN low).
    1.4 Receive byte from 'scope.
    1.5 Repeat 1.4 a further 1023 times.

Notes:

a) If the controller can only handle 1 byte per addressing sequence, then both 1.3 and 1.4 will have to be repeated a further 1023 times.

b) The sequence must be repeated exactly 1024 times in order to leave the 'scope in the correct state.

2. To read status words from 'scope to the controller:

2.1 Address 'scope to listen.

2.2 Send control byte to 'scope with bits 4 & 5 (TSX1 & 2) set (30 hex).

2.3 Address 'scope to talk.

2.4 Receive STATUS WORD 1 from 'scope.

2.5 Receive STATUS WORD 2 from 'scope.

Notes:

a) If the controller can only handle 1 byte per addressing sequence then 2.3 must be repeated between 2.4 and 2.5.

3) To write 1K of display data from the controller to the DTS12T:

3.1 Address 'scope to listen.

3.2 Send control byte to 'scope with bit 1 (RXDA) set (02 hex).

3.3 Address 'scope to listen.

3.4 Send signal data byte to 'scope.

3.5 Repeat 3.4 a further 1023 times.

Notes:

Notes for section 1 apply.

4) To write a cursor byte from the controller to the DTS12T:

4.1 Address the 'scope to listen.

4.2 Send control byte to 'scope with bit 2 (RXCR) set (04 hex).

4.3 Address 'scope to listen.

4.4 Send cursor byte to 'scope.

5. To hold the oscilloscope display:

5.1 Address the 'scope to listen.

5.2 Send control byte to 'scope with bit 6 (HLD) set (40 hex).

Notes:

The front panel controls have priority over the remote hold facility so the display will not remotely hold if the 'free run' button is pressed in.

6. To release the oscilloscope display:

6.1 Address the 'scope to listen.

6.2 Send control byte to 'scope with bit 7 (RLS) set (80 hex).

Notes:

The front panel controls have priority over the remote release facility, so the display will not remotely release if the 'hold' button is pressed in.

The cursor byte

In order to understand the operation of the DTS12T cursor, it is necessary to appreciate how signal data is stored in the main display memory of the oscilloscope. This is as follows:

In the single channel mode the first 512 bytes, corresponding to the left hand half of the trace, are stored in the even locations of the 1K display memory, and the second 512 bytes, corresponding to the right hand half, in the odd locations. In the dual channel mode the 512 bytes corresponding to the channel 2 trace are stored in the even locations and the 512 bytes corresponding to the channel 1 trace, on the odd locations.

The 'dot' cursor is implemented by switching off the beam for a short period during a trace using the oscilloscope's Z-mod. facility. The position of the cursor is determined by comparing (in hardware) an 8 bit value sent from the bus controller with 8 bits of the 10 bit display memory address bus. A Z-modulating pulse is generated when the two values are the same. The cursor can be moved along a trace simply by incrementing or decrementing the value of the cursor byte sent from the controller. The address bits used for this comparison are shown below.

address bit No.	value	cursor bit No.	comment
0	1	0	selects even or odd locations
1	2	-	not used in comparison

2	4	-	not used in comparison
3	8	1	
4	16	2	
5	32	3	
6	64	4	
7	128	5	
8	256	6	
9	512	7	

It can be seen from this table that the cursor has a resolution of 4 points in 1024.

Positioning the cursor

Moving the cursor from the left hand end of the trace to the right end is achieved as follows.

In the single channel mode:

1. Send cursor byte set to &00.
2. Increment cursor byte by 2 and send to 'scope.
3. Repeat 2. up to cursor value of &FE, this covers left half of trace.
4. Send cursor byte set to &01.
5. Repeat 2. up to cursor value of &FF, this covers right half of trace.

In the dual channel mode:

1. Send cursor byte set to &00.
2. Increment byte by 2 and send to 'scope.

3. Repeat 2. up to cursor value of &FE, this covers CH2 trace.

4. Send cursor byte set to &01.

5. Repeat 2. up to cursor value of &FF, this covers CH1 trace.

Moving the cursor in the opposite direction requires the reverse procedures.

THE BBC MICROCOMPUTER INTERFACE

The DTS12T provides an interface to the BBC model B microcomputer (BBCuC) utilising the microcomputer's USER PORT. This interface enables the user to transfer signal data from the oscilloscope to the BBCuC and from the BBCuC back to the oscilloscope screen. It is also possible for the microcomputer to remotely control the oscilloscope's 'hold' facility.

Using the interface

With both instruments turned off, connect the DTS12T to the BBCuC with the cable supplied. This connects, at the oscilloscope end, to a 20 way IDC socket mounted on the rear panel and, at the BBCuC to the USER PORT connector located beneath the keyboard. Turn the BBCuC on first and then the DTS12T. With appropriate software in the microcomputer, the desired data exchanges can now take place between the two instruments. Note that for all DTS12T/BBCuC operations, the oscilloscope must be in the storage mode. To use the program on the free user disc, connect the two instruments as described above, load the disc into the disc drive and, holding SHIFT down, press BREAK once. This loads and runs the program, presenting the user with a 'menu' of operations.

Software

Three software packages are currently available on disc for use with this interface. These are described below:

1. The first is a collection of the machine code routines which control the interface functions. These are useful to those who may wish to

incorporate the routines in their own programs.

2. The second package uses these routines as the basis of a simple display and storage program written in BASIC. This software allows the user to transfer data between the two instruments, save and recall waveforms from disc, remotely control the oscillocope's hold facility, and dump the contents of the screen to a printer. This package is supplied free with the DTS12T.

3. The third software package, consisting of a disc and a ROM which is fitted inside the BBCuC, includes the same functions, but in addition provides the user with powerful signal measurement and processing facilities. These include a sophisticated fast fourier transform program which allows the DTS12T/BBCuC combination to be used as a spectrum analyser.

THE DTS12T-BBCuC INTERFACE

Hardware

The BBCuC interface is implemented using an 8155 peripheral interface adapter in conjunction with the 8085 cpu in the DTS12T. Port A of the 8155 IC is used to transfer data between the I/O board and the BBCuC USER PORT. Two of the 8155 PORT C lines are used in conjunction with the CB1 and CB2 lines of the BBC's 6522 VIA to control the data transfer. A third PORT C line is used to drive the RST 5.5 interrupt on the 8085 uP.

Software

The software routines in the DTS12T which control the communication with the BBCuC are initiated by interrupts received from the microcomputer. Since the BBCuC can require the oscilloscope to perform one of a number of operations in response to these interrupts it is necessary at the start of a data exchange for the BBCuC to send a control word to the oscilloscope in order that the instrument will know how to respond to the interrupts that will follow.

The significance of each bit of this control word is described below.

bit No.	mnemonic	function
0	TXDA	send data byte
1	RXDA	receive data byte
2	RXCR	receive data byte

3	RXCL	receive control word
4	TXS1	send status word 1
5	TXS2	send status word 2
6	HLD	hold display
7	RLS	release display

A typical exchange of data between the DTS12T and the BBCuC would therefore be as follows.

To transfer the contents of the display memory to the BBCuC:

1. On switch on, the 8085 in the DTS12T sets PORT A of the 8155 as an input and sets the RXCL bit in its own control word.

2. The BBCuC sends a new control word to the 8085 with bit 4 (TXS1) set.

3. Because RXCL was initially set, the 8085 accepts the control word and stores it in the correct location. It sees that it's next operation will be to send data, so it sets PORT A of the 8155 to talk.

4. The BBCuC, having set it's user port to receive data, sends a 'ready for data' signal to the 8085.

5. The 8085, seeing that TXS1 is set, sends status word 1 to the BBCuC. It then resets bit 4 (TXS1) of the control word, sets bit 3 (RXCL) again and sets 8155 PORT A to listen, ready to receive the next instruction.

6. The BBCuC now sends a second control word with bit 0 (TXDA) set.

7. The 8085 receives and stores the control word, sets PORT A of the 8155 to talk, initiates a DMA transfer from the display memory to the I/O board memory and initialises it's registers for a 1K transfer.

8. The BBCuC sets the user port to receive data and sends a 'ready for data' signal to the 8155.

9. The 8085 then sends 1K data bytes to the BBCuC under handshake control. When this has been completed, the TXDA bit in the control word is reset, the RXCL bit is set and PORT A of the 8155 is set to listen again.

HARDWARE DESCRIPTION

The I/O board is a double-sided, plated-through-hole printed circuit board which is mounted in the oscilloscope immediately adjacent to the logic board. The four pushbuttons associated with the I/O facilities are board mounted, as are the DIL switches used to set the GPIB address. The connections to the GPIB and the BBCuC connectors on the rear panel are made via board mounted IDC connectors.

The fast data transfer, the memory decoding and other dedicated functions are implemented in 74HCT and 74LS series logic. The signal data is stored in one 2Kx8 static RAM, and the program is contained in one 2Kx8 EPROM. The board uses an INTEL 8085 as its cpu, with an 8155 peripheral interface adapter to provide the interface to the BBCuC, and an 8291 dedicated IEEE488 interface IC for the GPIB interface. CMOS digital to analogue converters, interfaced directly to the microprocessor data bus, drive the X and Y analogue outputs via a dual op-amp. The 8155 IC also contains 256 bytes of RAM which is used as 'scratchpad' memory by the 8085.

Operation

Since the I/O board is an optional facility, it was necessary to leave the basic DTS12 hardware largely unchanged. For this reason, it was not possible to give the microprocessor direct access to the existing display memory. The method used to exchange data between the display memory and the I/O board therefore involves the used of a duplicate display memory located on the I/O board and a

direct memory transfer between the two, controlled by dedicated hardware. The address bus of the duplicate memory can be selected to be either the DMA hardware generated address bus or the microprocessor address bus. In this way the signal data can be read from the display memory to the duplicate memory, then the cpu can send the data to one of the output devices under program control. Similarly, data received from an input port can be transferred to the display memory and so to the oscilloscope screen.

The microprocessor monitors the condition of the oscilloscope through two 'status words'. Status word 1 monitors 7 signals via an 8 bit latch interfaced directly to the uP data bus. Status word 2 monitors 8 signals via one of the I/O ports of the 8155 PIA. In a similar way the 8085 controls the storage operation of the oscilloscope and the DMA transfers via an 8 bit control word sent directly to a third latch. A cursor byte is sent to another latch and this value is compared by a hardware comparator to the read address of the display memory to generate the Z modulating pulse.

One 74HCT138 IC is used to decode all the necessary addresses for the board. The 8 select outputs decode the EPROM, the 2K RAM, the 8291, the 8155, the status latch, the control latch, the cursor latch and the digital to analogue converters. Each of these devices is decoded to occupy one 2K block and the whole 16K block is allowed to 'roll over' once since address line A15 is not used in the decoding.

The control word by which the 8085 controls the storage operation of the oscilloscope and the DMA transfer is described below:

bit No.	mnemonic	function
0	$\overline{A/B}$	selects 1 half of the 2K RAM.
1	$\overline{HOLD}$	a low holds the oscilloscope display.
2	not used	
3	$\overline{DMA\ R/W}$	determines direction of DMA transfer low = scope to I/O board transfer.
4	ADD.SEL	a low holds the logic board address bus in the read state for a DMA transfer.
5	$\overline{WRT.CLR}$	controls the CLEAR line on the logic board write address counters.

6	$\overline{\text{DMA}}$	a low gives control of the 2K RAM to the hardware DMA address counters.
7	PEN LIFT	drives the plotter PEN LIFT output.

The two status words monitored by the 8085 are described below:

STATUS WORD 1

bit no.	mnemonic	function
0	$\overline{\text{HOLD}}$	logic 0 if the oscilloscope's 'hold display' button is pressed in.
1	$\overline{\text{END}}$	logic 0 if the oscilloscope has completed a write sweep.
2	HOLD2	logic 0 if the oscilloscope's 'hold CH2' button is pressed in.

3	$\overline{\text{S/D}}$	logic 0 if the oscilloscope is in the single channel mode, logic 1 if in dual.
4	$\overline{\text{STORE}}$	logic 0 if the 'storage mode' button is pressed in.
5	$\overline{\text{BBC}}$	logic 0 if the BBCuC is connected to the DTS12T and switched on.
6	PLOT $\overline{\text{CH1/CH2}}$	selects which channel is to be plotted by the X-Y interface (not used by the BBCuC).
7	$\overline{\text{A/B}}$	selects which memory is viewed and updated (not used by the BBCuC).

STATUS WORD 2

bit No.	mnemonic	description
0	SW6	

1	SW5	
2	SW4	STATUS OF DIL SWITCHES ON I/O BOARD. Logic 0 corresponds to 'ON'.
3	SW3	
4	SW2	These switches are not required by BBCuC.
5	SW1	
6	$\overline{\text{CH1 OFF}}$	logic 0 if oscilloscope channel 1 is switched off.
7	$\overline{\text{CH2 OFF}}$	logic 0 if oscilloscope channel 2 is switched off.

DESCRIPTION OF SOFTWARE

The software, contained in a 2K EPROM, consists of an initialisation sequence, a relatively short core program, interrupt routines to service the plotter outputs, the GPIB interface and the BBCuC interface.

The initialisation sequence sets the I/O IC's and the system variables to their start conditions. The core program constantly monitors the status of the oscilloscope and alters certain variables according to changes in certain front panel settings. The A/B memory exchange is performed within this core program when a change in state of the B button is recorded.

The plotter output sequence is interrupt driven, using the highest priority RTS7.5 interrupt. This interrupt line is driven by the RESET/PLOT button. On receiving this interrupt the processor checks a flag byte to determine whether a RESET or a PLOT is required then, assuming a PLOT condition, a DMA transfer is initiated from the screen memory to the I/O board memory. When this is complete the processor sends successive bytes of signal data to the Y DAC whilst sending an incrementing 10 bit digital count to the X DAC. The position of DIL switch No. 6 determines the length of delay between successive points and thus the plotting speed. In the dual channel mode the status of the PLOT CH1/CH2 button determines which trace is plotted. All other processor operations, including other interrupts, are disabled during a plot sequence. The processor will only initiate a plot if the oscilloscope is in the storage mode with the 'hold' button pressed in. The plotter facility is disabled altogether when the oscilloscope is connected to a BBCuC.