

# 1-Ω DUAL SPDT ANALOG SWITCH

## 5-V/3.3-V 2-CHANNEL 2:1 MULTIPLEXER/DEMULTIPLEXER

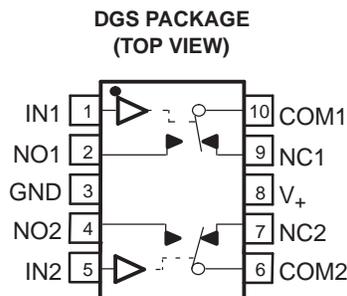
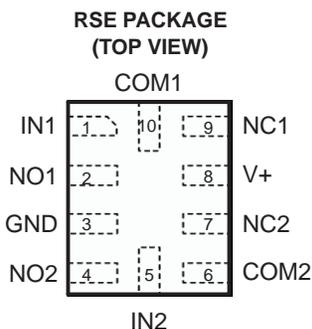
Check for Samples: [TS5A23159](#)

### FEATURES

- Isolation in Power-Down Mode,  $V_{+} = 0$
- Specified Break-Before-Make Switching
- Low ON-State Resistance ( $1\ \Omega$ )
- Control Inputs Are 5.5-V Tolerant
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

### APPLICATIONS

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communication Circuits
- Modems
- Hard Drives
- Computer Peripherals
- Wireless Terminals and Peripherals



### DESCRIPTION/ORDERING INFORMATION

The TS5A23159 is a dual single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers low ON-state resistance and excellent ON-state resistance matching with the break-before-make feature, to prevent signal distortion during the transferring of a signal from one channel to another. The device has an excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

**Table 1. ORDERING INFORMATION<sup>(1)</sup>**

$T_A$	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(3)</sup>
–40°C to 85°C	VSSOP – DGS (MSOP)	Tape and reel	TS5A23159DGSR	JE_
	QFN – RSE	Tape and reel	TS5A23159RSER	JE_

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(3) DGS/RSE: The actual top-side marking has one additional character that designates the assembly/test site.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**Table 2. SUMMARY OF CHARACTERISTICS<sup>(1)</sup>**

Configuration	Dual 2:1 Multiplexer/Demultiplexer (2 × SPDT)
Number of channels	2
ON-state resistance ( $r_{on}$ )	1.1 $\Omega$
ON-state resistance match ( $\Delta r_{on}$ )	0.1 $\Omega$
ON-state resistance flatness ( $r_{on(Flat)}$ )	0.15 $\Omega$
Turn-on/turn-off time ( $t_{ON}/t_{OFF}$ )	20 ns/15 ns
Break-before-make time ( $t_{BBM}$ )	12 ns
Charge injection ( $Q_C$ )	-7 pC
Bandwidth (BW)	100 MHz
OFF isolation ( $O_{ISO}$ )	-65 dB at 1 MHz
Crosstalk ( $X_{TALK}$ )	-66 dB at 1 MHz
Total harmonic distortion (THD)	0.01%
Leakage current ( $I_{NO(OFF)}/I_{NC(OFF)}$ )	$\pm 20$ nA
Power-supply current ( $I_+$ )	50 nA
Package options	10-pin VSSOP and QFN

(1)  $V_+ = 5$  V,  $T_A = 25^\circ\text{C}$ **Table 3. FUNCTION TABLE**

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

**Absolute Minimum and Maximum Ratings<sup>(1) (2)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_+$	Supply voltage range <sup>(3)</sup>	-0.5	6.5	V
$V_{NC}$ $V_{NO}$ $V_{COM}$	Analog voltage range <sup>(3) (4) (5)</sup>	-0.5	$V_+ + 0.5$	V
$I_K$	Analog port diode current	$V_{NC}, V_{NO}, V_{COM} < 0$		mA
$I_{NC}$ $I_{NO}$ $I_{COM}$	On-state switch current	-200	200	mA
	On-state peak switch current <sup>(6)</sup>	-400	400	
$V_I$	Digital input voltage range <sup>(3) (4)</sup>	-0.5	6.5	V
$I_{IK}$	Digital input clamp current	$V_I < 0$		mA
$I_+$	Continuous current through $V_+$		100	mA
$I_{GND}$	Continuous current through GND	-100	100	mA
$\theta_{JA}$	Package thermal impedance <sup>(7)</sup>	DGS package		165
		RSE package		TBD
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.
- (6) Pulse at 1-ms duration < 10% duty cycle
- (7) The package thermal impedance is calculated in accordance with JESD 51-7.

## Electrical Characteristics for 5-V Supply<sup>(1)</sup>

$V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	$V_{COM}, V_{NO}, V_{NC}$				0		$V_+$	V
Peak ON resistance	$r_{peak}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -100\text{ mA}$ , Switch ON, See <a href="#">Figure 14</a>	25°C Full	4.5 V		0.8	1.1 1.5	$\Omega$
ON-state resistance	$r_{on}$	$V_{NO} \text{ or } V_{NC} = 2.5\text{ V}$ , $I_{COM} = -100\text{ mA}$ , Switch ON, See <a href="#">Figure 14</a>	25°C Full	4.5 V		0.7	0.9 1.1	$\Omega$
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} \text{ or } V_{NC} = 2.5\text{ V}$ , $I_{COM} = -100\text{ mA}$ , Switch ON, See <a href="#">Figure 14</a>	25°C Full	4.5 V		0.05	0.1 0.1	$\Omega$
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -100\text{ mA}$ , $V_{NO} \text{ or } V_{NC} = 1\text{ V}, 1.5\text{ V}, 2.5\text{ V}$ , $I_{COM} = -100\text{ mA}$ , Switch ON, See <a href="#">Figure 14</a>	25°C Full	4.5 V		0.15 0.1	0.25 0.25	$\Omega$
NC, NO OFF leakage current	$I_{NO(OFF)}, I_{NC(OFF)}$	$V_{NC} \text{ or } V_{NO} = 1\text{ V}$ , $V_{COM} = 1\text{ V to }4.5\text{ V}$ , or $V_{NC} \text{ or } V_{NO} = 4.5\text{ V}$ , $V_{COM} = 1\text{ V to }4.5\text{ V}$ , Switch OFF, See <a href="#">Figure 15</a>	25°C	5.5 V	-20	2	20	nA
			Full		-100		100	
NC, NO ON leakage current	$I_{NO(ON)}, I_{NC(ON)}$	$V_{NC} \text{ or } V_{NO} = 1\text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NC} \text{ or } V_{NO} = 4.5\text{ V}$ , $V_{COM} = \text{Open}$ , Switch ON, See <a href="#">Figure 16</a>	25°C	5.5 V	-20	2	20	nA
			Full		-100		100	
COM OFF leakage current	$I_{COM(PWROFF)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } 5.5\text{ V}$ , $V_{COM} = 5.5\text{ V to } 0$ , Switch OFF, See <a href="#">Figure 15</a>	25°C	0 V	-1	0.1	1	$\mu\text{A}$
			Full		-20		20	
COM ON leakage current	$I_{COM(ON)}$	$V_{NC} \text{ or } V_{NO} = \text{Open}$ , $V_{COM} = 1\text{ V}$ , or $V_{NC} \text{ or } V_{NO} = \text{Open}$ , $V_{COM} = 4.5\text{ V}$ , Switch ON, See <a href="#">Figure 16</a>	25°C	5.5 V	-20	2	20	nA
			Full		-100		100	
<b>Digital Control Inputs (IN1, IN2)<sup>(2)</sup></b>								
Input logic high	$V_{IH}$		Full		2.4		5.5	V
Input logic low	$V_{IL}$		Full		0		0.8	V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or } 0$	25°C	5.5 V	-2		2	nA
			Full		-100		100	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at  $V_+$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**Electrical Characteristics for 5-V Supply<sup>(1)</sup> (continued)**
 $V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>								
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , See <a href="#">Figure 18</a>	25°C	5 V	1	8	13	ns
			Full	4.5 V to 5.5 V	1		16.5	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , See <a href="#">Figure 18</a>	25°C	5 V	1	5	8	ns
			Full	4.5 V to 5.5 V	1		8	
Break-before-make time	$t_{BBM}$	$V_{NC} = V_{NO} = V_+$ , $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , See <a href="#">Figure 19</a>	25°C	5 V	1	5.5	13	ns
			Full	4.5 V to 5.5 V	1		14	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ , $C_L = 1\text{ nF}$ , See <a href="#">Figure 23</a>	25°C	5 V		-7		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$ , $C_{NO(OFF)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch OFF, See <a href="#">Figure 17</a>	25°C	5 V		18		pF
NC, NO ON capacitance	$C_{NC(ON)}$ , $C_{NO(ON)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch ON, See <a href="#">Figure 17</a>	25°C	5 V		55		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See <a href="#">Figure 17</a>	25°C	5 V		54.5		pF
Digital input capacitance	$C_I$	$V_I = V_+$ or GND, See <a href="#">Figure 17</a>	25°C	5 V		2		pF
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON, See <a href="#">Figure 20</a>	25°C	5 V		100		MHz
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ , Switch OFF, See <a href="#">Figure 21</a>	25°C	5 V		-64		dB
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ , Switch ON, See <a href="#">Figure 22</a>	25°C	5 V		-64		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ , $f = 20\text{ Hz to }20\text{ kHz}$ , See <a href="#">Figure 24</a>	25°C	5 V		0.004		%
<b>Supply</b>								
Positive supply current	$I_+$	$V_I = V_+$ or GND, Switch ON or OFF	25°C	5.5 V		10	50	nA
			Full				750	

### Electrical Characteristics for 3.3-V Supply<sup>(1)</sup>

V<sub>+</sub> = 3 V to 3.6 V, T<sub>A</sub> = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T <sub>A</sub>	V <sub>+</sub>	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	V <sub>COM</sub> , V <sub>NO</sub> , V <sub>NC</sub>				0		V <sub>+</sub>	V
Peak ON resistance	r <sub>peak</sub>	0 ≤ (V <sub>NO</sub> or V <sub>NC</sub> ) ≤ V <sub>+</sub> , I <sub>COM</sub> = –100 mA, Switch ON, See Figure 14	25°C Full	3 V		1.3	1.6 2	Ω
ON-state resistance	r <sub>on</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 2 V, I <sub>COM</sub> = –100 mA, Switch ON, See Figure 14	25°C Full	3 V		1.2	1.5 1.7	Ω
ON-state resistance match between channels	Δr <sub>on</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 2 V, 0.8 V, I <sub>COM</sub> = –100 mA, Switch ON, See Figure 14	25°C Full	3 V		0.1	0.15 0.2	Ω
ON-state resistance flatness	r <sub>on(flat)</sub>	0 ≤ (V <sub>NO</sub> or V <sub>NC</sub> ) ≤ V <sub>+</sub> , I <sub>COM</sub> = –100 mA, Switch ON, See Figure 14	25°C Full	3 V		0.15		Ω
NC, NO OFF leakage current	I <sub>NO(OFF)</sub> , I <sub>NC(OFF)</sub>	V <sub>NC</sub> or V <sub>NO</sub> = 1 V, V <sub>COM</sub> = 1 V to 3 V, or V <sub>NC</sub> or V <sub>NO</sub> = 3 V, V <sub>COM</sub> = 1 V to 3 V, Switch OFF, See Figure 15	25°C	3.6 V	–20	2	20	nA
			Full		–50		50	
NC, NO ON leakage current	I <sub>NO(ON)</sub> , I <sub>NC(ON)</sub>	V <sub>NC</sub> or V <sub>NO</sub> = 1 V, V <sub>COM</sub> = Open, or V <sub>NC</sub> or V <sub>NO</sub> = 3 V, V <sub>COM</sub> = Open, Switch ON, See Figure 16	25°C	3.6 V	–10	2	10	nA
			Full		–20		20	
COM OFF leakage current	I <sub>COM(PWROFF)</sub>	V <sub>NC</sub> or V <sub>NO</sub> = 3.6 V to 0, V <sub>COM</sub> = 0 to 3.6 V, Switch OFF, See Figure 15	25°C	0 V	–1	0.2	1	μA
			Full		–15		15	
COM ON leakage current	I <sub>COM(ON)</sub>	V <sub>NC</sub> or V <sub>NO</sub> = Open, V <sub>COM</sub> = 1 V, or V <sub>NC</sub> or V <sub>NO</sub> = Open, V <sub>COM</sub> = 3 V, Switch ON, See Figure 16	25°C	3.6 V	–10	2	10	nA
			Full		–20		20	
<b>Digital Control Inputs (IN1, IN2)<sup>(2)</sup></b>								
Input logic high	V <sub>IH</sub>		Full		2		5.5	V
Input logic low	V <sub>IL</sub>		Full		0		0.8	V
Input leakage current	I <sub>IH</sub> , I <sub>IL</sub>	V <sub>I</sub> = 5.5 V or 0	25°C	3.6 V	–2		2	nA
			Full		–20		20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum  
 (2) All unused digital inputs of the device must be held at V<sub>+</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**Electrical Characteristics for 3.3-V Supply<sup>(1)</sup> (continued)**
 $V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 18</a>	25°C	3.3 V	5	11	19	ns
				Full	3 V to 3.6 V	3		22	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 18</a>	25°C	3.3 V	1	5	9	ns
				Full	3 V to 3.6 V	1		9	
Break-before-make time	$t_{BBM}$	$V_{NC} = V_{NO} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 19</a>	25°C	3.3 V	1	7	17	ns
				Full	3 V to 3.6 V	1		20	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 1\text{ nF}$ , See <a href="#">Figure 23</a>	25°C	3.3 V		-4	pC	
NC, NO OFF capacitance	$C_{NC(OFF)}$ , $C_{NO(OFF)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch OFF,	See <a href="#">Figure 17</a>	25°C	3.3 V		18	pF	
NC, NO ON capacitance	$C_{NC(ON)}$ , $C_{NO(ON)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch ON,	See <a href="#">Figure 17</a>	25°C	3.3 V		56	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See <a href="#">Figure 17</a>	25°C	3.3 V		56	pF	
Digital input capacitance	$C_I$	$V_I = V_+$ or GND,	See <a href="#">Figure 17</a>	25°C	3.3 V		2	pF	
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON,	See <a href="#">Figure 20</a>	25°C	3.3 V		100	MHz	
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	Switch OFF, See <a href="#">Figure 21</a>	25°C	3.3 V		-64	dB	
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	Switch ON, See <a href="#">Figure 22</a>	25°C	3.3 V		-64	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ ,	$f = 20\text{ Hz to }20\text{ kHz}$ , See <a href="#">Figure 24</a>	25°C	3.3 V		0.01	%	
<b>Supply</b>									
Positive supply current	$I_+$	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	3.6 V	25		nA	
				Full		150			

### Electrical Characteristics for 2.5-V Supply<sup>(1)</sup>

V<sub>+</sub> = 2.3 V to 2.7 V, T<sub>A</sub> = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T <sub>A</sub>	V <sub>+</sub>	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>									
Analog signal range	V <sub>COM</sub> , V <sub>NO</sub> , V <sub>NC</sub>				0		V <sub>+</sub>	V	
Peak ON resistance	r <sub>peak</sub>	0 ≤ (V <sub>NO</sub> or V <sub>NC</sub> ) ≤ V <sub>+</sub> , I <sub>COM</sub> = –8 mA, Switch ON, See Figure 14	25°C	2.3 V		1.8	2.5	Ω	
			Full			2.7			
ON-state resistance	r <sub>on</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 1.8 V, I <sub>COM</sub> = –8 mA, Switch ON, See Figure 14	25°C	2.3 V		1.5	2	Ω	
			Full			2.4			
ON-state resistance match between channels	Δr <sub>on</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 1.8 V, 0.8 V, I <sub>COM</sub> = –8 mA, Switch ON, See Figure 14	25°C	2.3 V		0.15	0.2	Ω	
			Full			0.2			
ON-state resistance flatness	r <sub>on(flat)</sub>	0 ≤ (V <sub>NO</sub> or V <sub>NC</sub> ) ≤ V <sub>+</sub> , I <sub>COM</sub> = –8 mA, Switch ON, See Figure 14	25°C	2.3 V		0.6		Ω	
			25°C			0.6			
			Full			1			
NC, NO OFF leakage current	I <sub>NO(OFF)</sub> , I <sub>NC(OFF)</sub>	V <sub>NC</sub> or V <sub>NO</sub> = 0.5 V, V <sub>COM</sub> = 0.5 V to 2.3 V, or V <sub>NC</sub> or V <sub>NO</sub> = 2.2 V, V <sub>COM</sub> = 0.5 V to 2.3 V, Switch OFF, See Figure 15	25°C	2.3 V		–20	2	20	nA
			Full			–50	50		
	I <sub>NC(PWROFF)</sub> , I <sub>NO(PWROFF)</sub>	V <sub>NC</sub> or V <sub>NO</sub> = 0 to 2.7 V, V <sub>COM</sub> = 2.7 V to 0, Switch OFF, See Figure 15	25°C	0 V		–1	0.1	1.0	μA
			Full			–10	10		
NC, NO ON leakage current	I <sub>NO(ON)</sub> , I <sub>NC(ON)</sub>	V <sub>NC</sub> or V <sub>NO</sub> = 0.5 V, V <sub>COM</sub> = Open, or V <sub>NC</sub> or V <sub>NO</sub> = 2.2 V, V <sub>COM</sub> = Open, Switch ON, See Figure 16	25°C	2.7 V		–10	2	10	nA
			Full			–20	20		
COM OFF leakage current	I <sub>COM(PWROFF)</sub>	V <sub>NC</sub> or V <sub>NO</sub> = 2.7 V to 0, V <sub>COM</sub> = 0 to 2.7 V, Switch OFF, See Figure 15	25°C	0 V		–1	0.1	1	μA
			Full			–10	10		
COM ON leakage current	I <sub>COM(ON)</sub>	V <sub>NC</sub> or V <sub>NO</sub> = Open, V <sub>COM</sub> = 0.5 V, or V <sub>NC</sub> or V <sub>NO</sub> = Open, V <sub>COM</sub> = 2.2 V, Switch ON, See Figure 16	25°C	2.7 V		–10	2	10	nA
			Full			–20	20		
<b>Digital Control Inputs (IN1, IN2)<sup>(2)</sup></b>									
Input logic high	V <sub>IH</sub>		Full		1.8		5.5	V	
Input logic low	V <sub>IL</sub>		Full		0		0.6	V	
Input leakage current	I <sub>IH</sub> , I <sub>IL</sub>	V <sub>I</sub> = 5.5 V or 0	25°C	2.7 V		–2	2	nA	
			Full			–20	20		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum  
 (2) All unused digital inputs of the device must be held at V<sub>+</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**Electrical Characteristics for 2.5-V Supply<sup>(1)</sup> (Continued)**
 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ , $R_L = 50 \Omega$ ,	$C_L = 35 \text{ pF}$ , See <a href="#">Figure 18</a>	25°C	2.5 V	5	15	28	ns
				Full	2.3 V to 2.7 V	5		32	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ , $R_L = 50 \Omega$ ,	$C_L = 35 \text{ pF}$ , See <a href="#">Figure 18</a>	25°C	2.5 V	2	6	9	ns
				Full	2.3 V to 2.7 V	2		10	
Break-before-make time	$t_{BBM}$	$V_{NC} = V_{NO} = V_+$ , $R_L = 50 \Omega$ ,	$C_L = 35 \text{ pF}$ , See <a href="#">Figure 19</a>	25°C	2.5 V	1	10	27	ns
				Full	2.3 V to 2.7 V	1		30	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 1 \text{ nF}$ , See <a href="#">Figure 23</a>	25°C	2.5 V		-3	pC	
NC, NO OFF capacitance	$C_{NC(OFF)}$ , $C_{NO(OFF)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch OFF,	See <a href="#">Figure 17</a>	25°C	2.5 V		18.5	pF	
NC, NO ON capacitance	$C_{NC(ON)}$ , $C_{NO(ON)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch ON,	See <a href="#">Figure 17</a>	25°C	2.5 V		56.5	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See <a href="#">Figure 17</a>	25°C	2.5 V		56.5	pF	
Digital input capacitance	$C_I$	$V_I = V_+$ or GND,	See <a href="#">Figure 17</a>	25°C	2.5 V		2	pF	
Bandwidth	BW	$R_L = 50 \Omega$ , Switch ON,	See <a href="#">Figure 20</a>	25°C	2.5 V		100	MHz	
OFF isolation	$O_{ISO}$	$R_L = 50 \Omega$ , $f = 1 \text{ MHz}$ ,	Switch OFF, See <a href="#">Figure 21</a>	25°C	2.5 V		-64	dB	
Crosstalk	$X_{TALK}$	$R_L = 50 \Omega$ , $f = 1 \text{ MHz}$ ,	Switch ON, See <a href="#">Figure 22</a>	25°C	2.5 V		-64	dB	
Total harmonic distortion	THD	$R_L = 600 \Omega$ , $C_L = 50 \text{ pF}$ ,	$f = 20 \text{ Hz to } 20 \text{ kHz}$ , See <a href="#">Figure 24</a>	25°C	2.5 V		0.02	%	
<b>Supply</b>									
Positive supply current	$I_+$	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	2.7 V		10	25	nA
				Full				100	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

## Electrical Characteristics for 1.8-V Supply<sup>(1)</sup>

$V_+ = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	$V_{COM}, V_{NO}, V_{NC}$				0		$V_+$	V
Peak ON resistance	$r_{peak}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -2\text{ mA}$ , Switch ON, See <a href="#">Figure 14</a>	25°C	1.65 V	5		15	$\Omega$
			Full					
ON-state resistance	$r_{on}$	$V_{NO} \text{ or } V_{NC} = 1.5\text{ V}$ , $I_{COM} = -2\text{ mA}$ , Switch ON, See <a href="#">Figure 14</a>	25°C	1.65 V	2	2.5	3.5	$\Omega$
			Full					
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} \text{ or } V_{NC} = 0.6\text{ V}, 1.5\text{ V}$ , $I_{COM} = -2\text{ mA}$ , Switch ON, See <a href="#">Figure 14</a>	25°C	1.65 V	0.15	0.4	0.4	$\Omega$
			Full					
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -2\text{ mA}$ , Switch ON, See <a href="#">Figure 14</a>	25°C	1.65 V	5			$\Omega$
			Full					
NC, NO OFF leakage current	$I_{NO(OFF)}, I_{NC(OFF)}$	$V_{NC} \text{ or } V_{NO} = 0.3\text{ V}$ , $V_{COM} = 0.3\text{ V to }1.65\text{ V}$ , or $V_{NC} \text{ or } V_{NO} = 1.65\text{ V}$ , $V_{COM} = 0.3\text{ V to }1.65\text{ V}$ Switch OFF, See <a href="#">Figure 15</a>	25°C	1.65 V	-20	2	20	nA
			Full					
NC, NO ON leakage current	$I_{NO(ON)}, I_{NC(ON)}$	$V_{NC} \text{ or } V_{NO} = 0.3\text{ V}$ , $V_{COM} = \text{Open}$ , or $V_{NC} \text{ or } V_{NO} = 1.65\text{ V}$ , $V_{COM} = \text{Open}$ , Switch ON, See <a href="#">Figure 16</a>	25°C	1.95 V	-5	2	5	nA
			Full					
COM OFF leakage current	$I_{COM(PWROFF)}$	$V_{NC} \text{ or } V_{NO} = 1.95\text{ V to }0$ , $V_{COM} = 0 \text{ to }1.95\text{ V}$ , Switch OFF, See <a href="#">Figure 15</a>	25°C	0 V	-1	0.1	1	$\mu\text{A}$
			Full					
COM ON leakage current	$I_{COM(ON)}$	$V_{NC} \text{ or } V_{NO} = \text{Open}$ , $V_{COM} = 0.3\text{ V}$ , or $V_{NC} \text{ or } V_{NO} = \text{Open}$ , $V_{COM} = 1.65\text{ V}$ , Switch ON, See <a href="#">Figure 16</a>	25°C	1.95 V	-10	2	10	nA
			Full					
<b>Digital Control Inputs (IN1, IN2)<sup>(2)</sup></b>								
Input logic high	$V_{IH}$		Full		1.5		5.5	V
Input logic low	$V_{IL}$		Full		0		0.6	V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or }0$	25°C	1.95 V	-2		2	nA
			Full					

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at  $V_+$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**Electrical Characteristics for 1.8-V Supply<sup>(1)</sup> (Continued)**
 $V_+ = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 18</a>	25°C	1.8 V	10	27.5	48.5	ns
				Full	1.65 V to 1.95 V	10		55	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 18</a>	25°C	1.8 V	2	6.5	11	ns
				Full	1.65 V to 1.95 V	2		12	
Break-before-make time	$t_{BBM}$	$V_{NC} = V_{NO} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 35\text{ pF}$ , See <a href="#">Figure 19</a>	25°C	1.8 V	1	18	50	ns
				Full	1.65 V to 1.95 V	1		55	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 1\text{ nF}$ , See <a href="#">Figure 23</a>	25°C	1.8 V		2	pC	
NC, NO OFF capacitance	$C_{NC(OFF)}$ , $C_{NO(OFF)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch OFF,	See <a href="#">Figure 17</a>	25°C	1.8 V		18.5	pF	
NC, NO ON capacitance	$C_{NC(ON)}$ , $C_{NO(ON)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch ON,	See <a href="#">Figure 17</a>	25°C	1.8 V		56.5	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See <a href="#">Figure 17</a>	25°C	1.8 V		56.5	pF	
Digital input capacitance	$C_I$	$V_I = V_+$ or GND,	See <a href="#">Figure 17</a>	25°C	1.8 V		2	pF	
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON,	See <a href="#">Figure 20</a>	25°C	1.8 V		105	MHz	
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	Switch OFF, See <a href="#">Figure 21</a>	25°C	1.8 V		-64	dB	
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ,	Switch ON, See <a href="#">Figure 22</a>	25°C	1.8 V		-64	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ ,	$f = 20\text{ Hz to }20\text{ kHz}$ , See <a href="#">Figure 24</a>	25°C	1.8 V		0.06	%	
<b>Supply</b>									
Positive supply current	$I_+$	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	1.95 V		10	25	nA
				Full				50	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

TYPICAL PERFORMANCE

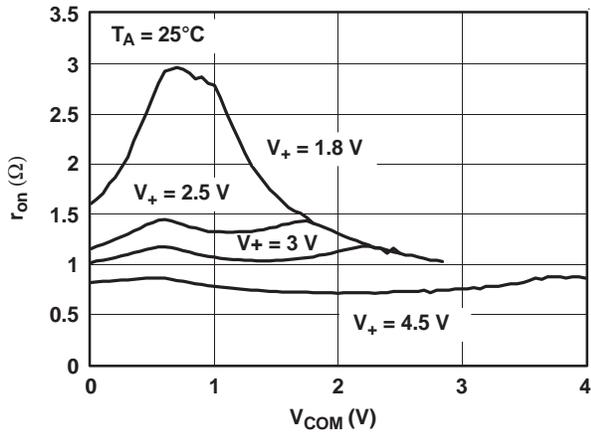


Figure 1.  $r_{on}$  vs  $V_{COM}$

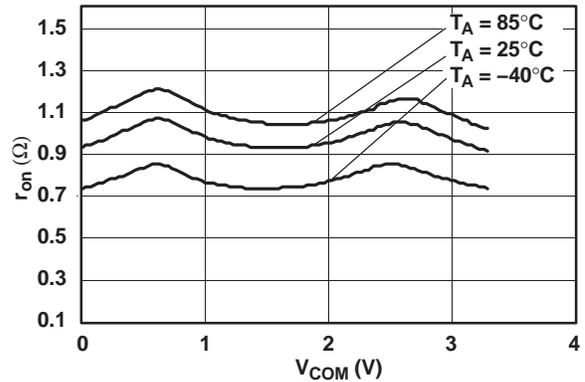


Figure 2.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 3.3\text{ V}$ )

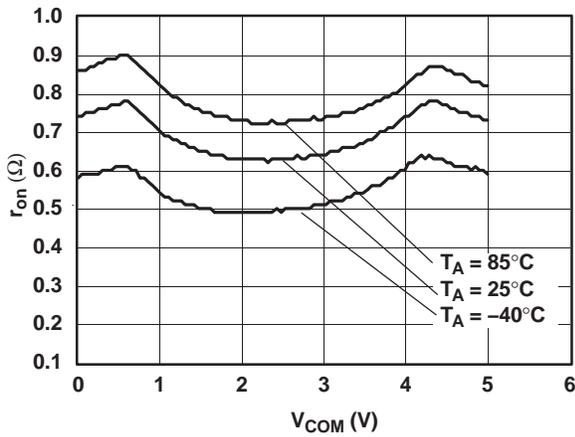


Figure 3.  $r_{on}$  vs  $V_{COM}$  ( $V_+ = 5\text{ V}$ )

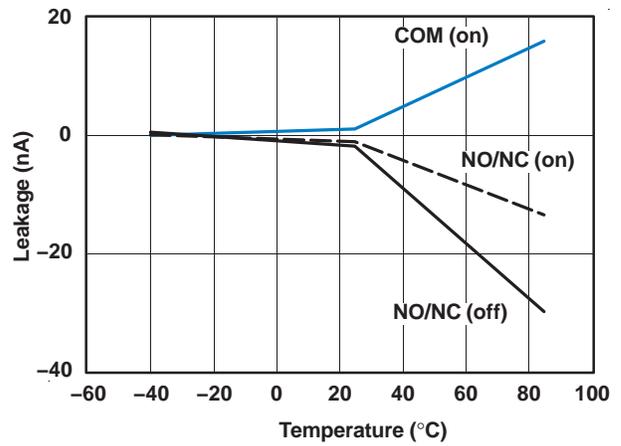


Figure 4. Leakage Current vs Temperature ( $V_+ = 3.3\text{ V}$ )

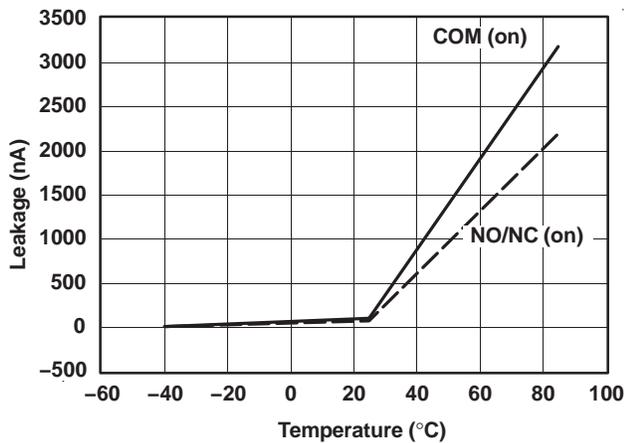


Figure 5. Leakage Current vs Temperature ( $V_+ = 5\text{ V}$ )

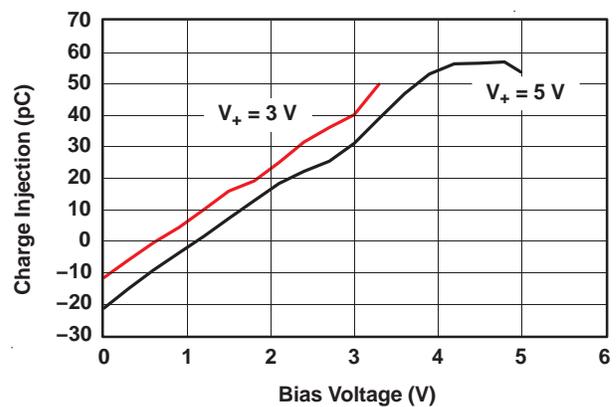


Figure 6. Charge Injection ( $Q_C$ ) vs  $V_{COM}$

TYPICAL PERFORMANCE (continued)

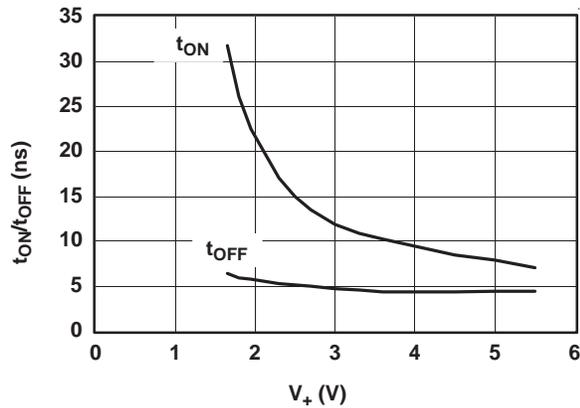


Figure 7.  $t_{ON}$  and  $t_{OFF}$  vs Supply Voltage

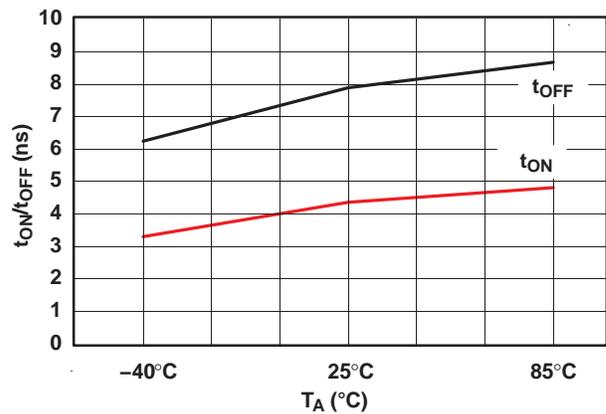


Figure 8.  $t_{ON}$  and  $t_{OFF}$  vs Temperature (5-V Supply)

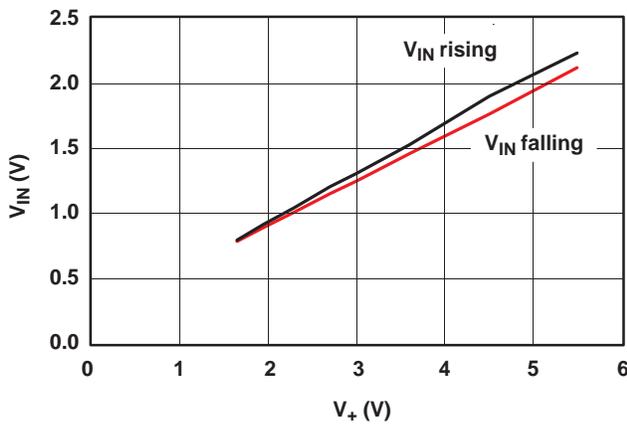


Figure 9. Logic-Level Threshold vs  $V_+$

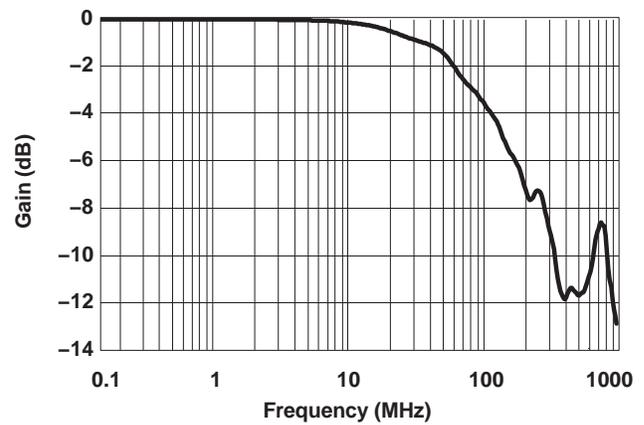


Figure 10. Bandwidth ( $V_+ = 5\text{ V}$ )

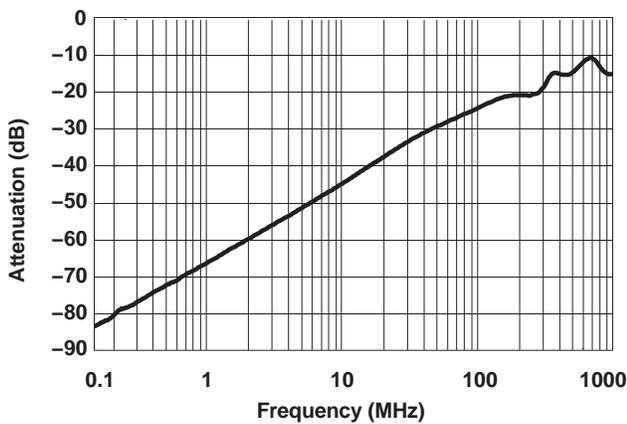


Figure 11. OFF Isolation vs Frequency

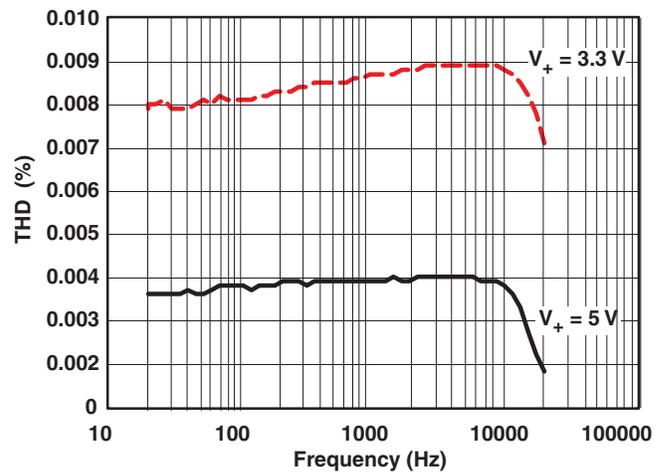
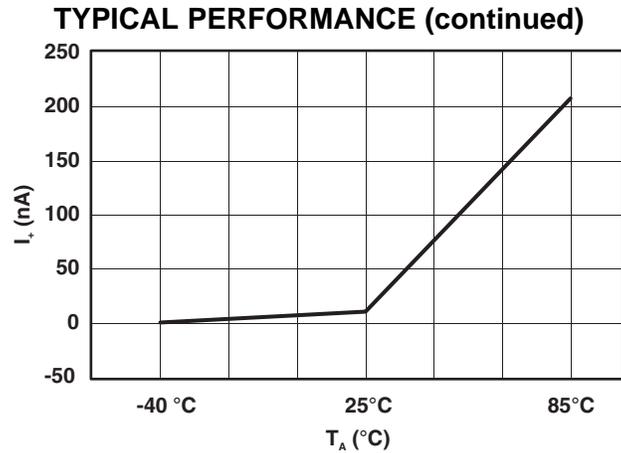


Figure 12. Total Harmonic Distortion vs Frequency

Figure 13. Power-Supply Current vs Temperature ( $V_+ = 5\text{ V}$ )**Table 4. PIN DESCRIPTION**

PIN NO.	NAME	DESCRIPTION
1	IN1	Digital control to connect COM to NO or NC
2	NO1	Normally open
3	GND	Digital ground
4	NO2	Normally open
5	IN2	Digital control to connect COM to NO or NC
6	COM2	Common
7	NC2	Normally closed
8	$V_+$	Power supply
9	NC1	Normally closed
10	COM1	Power supply

**Table 5. PARAMETER DESCRIPTION**

SYMBOL	DESCRIPTION
$V_{COM}$	Voltage at COM
$V_{NC}$	Voltage at NC
$V_{NO}$	Voltage at NO
$r_{on}$	Resistance between COM and NC or COM and NO ports when the channel is ON
$r_{peak}$	Peak on-state resistance over a specified voltage range
$\Delta r_{on}$	Difference of $r_{on}$ between channels in a specific device
$r_{on(Flat)}$	Difference between the maximum and minimum value of $r_{on}$ in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
$I_{NC(PWROFF)}$	Leakage current measured at the NC port during the power-down condition, $V_+ = 0$
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
$I_{NO(PWROFF)}$	Leakage current measured at the NO port during the power-down condition, $V_+ = 0$
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-down condition, $V_+ = 0$
$V_{IH}$	Minimum input voltage for logic high for the control input (IN)
$V_{IL}$	Maximum input voltage for logic low for the control input (IN)
$V_I$	Voltage at the control input (IN)
$I_{IH}, I_{IL}$	Leakage current measured at the control input (IN)
$t_{ON}$	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning ON.
$t_{OFF}$	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning OFF.
$t_{BBM}$	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
$Q_C$	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$ . $C_L$ is the load capacitance and $\Delta V_{COM}$ is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
$C_I$	Capacitance of control input (IN)
$O_{ISO}$	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
$X_{TALK}$	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion is defined as the ratio of the root mean square (RMS) value of the second, third, and higher harmonics to the magnitude of fundamental harmonic.
$I_+$	Static power-supply current with the control (IN) pin at $V_+$ or GND

PARAMETER MEASUREMENT INFORMATION

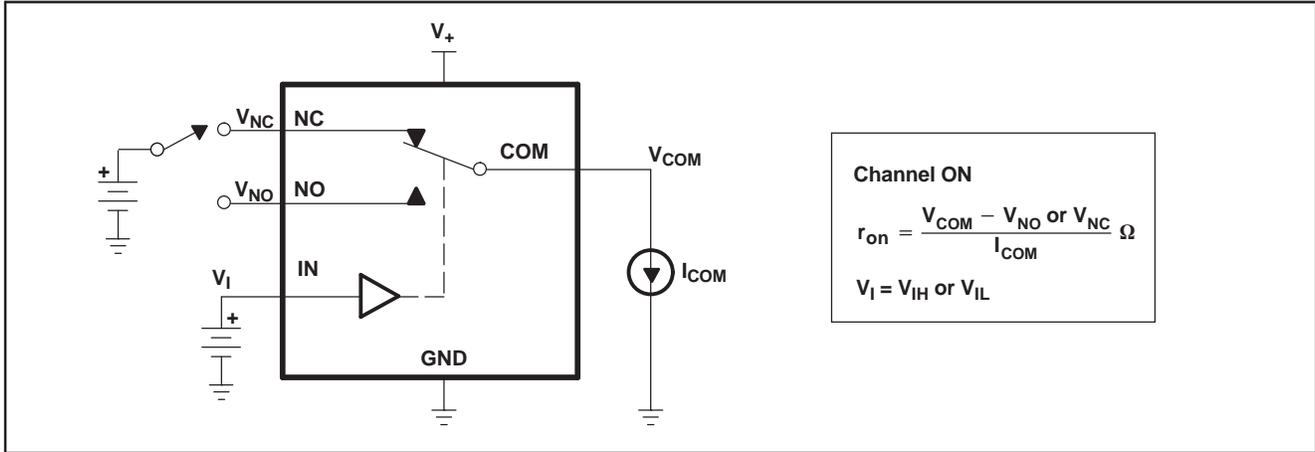


Figure 14. ON-State Resistance ( $r_{on}$ )

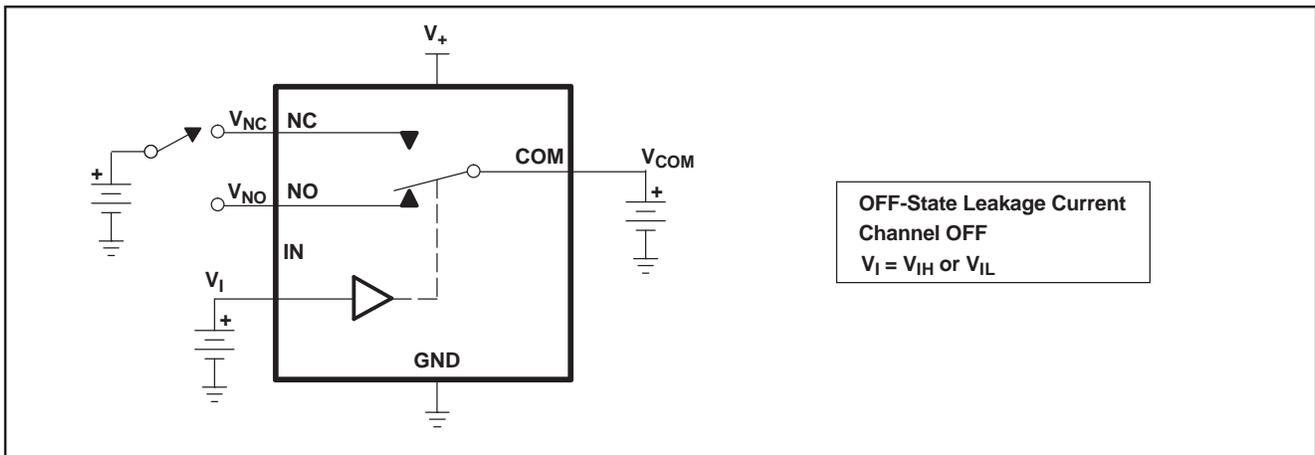


Figure 15. OFF-State Leakage Current  
( $I_{NC(OFF)}$ ,  $I_{NC(PWROFF)}$ ,  $I_{NO(OFF)}$ ,  $I_{NO(PWROFF)}$ ,  $I_{COM(OFF)}$ ,  $I_{COM(PWROFF)}$ )

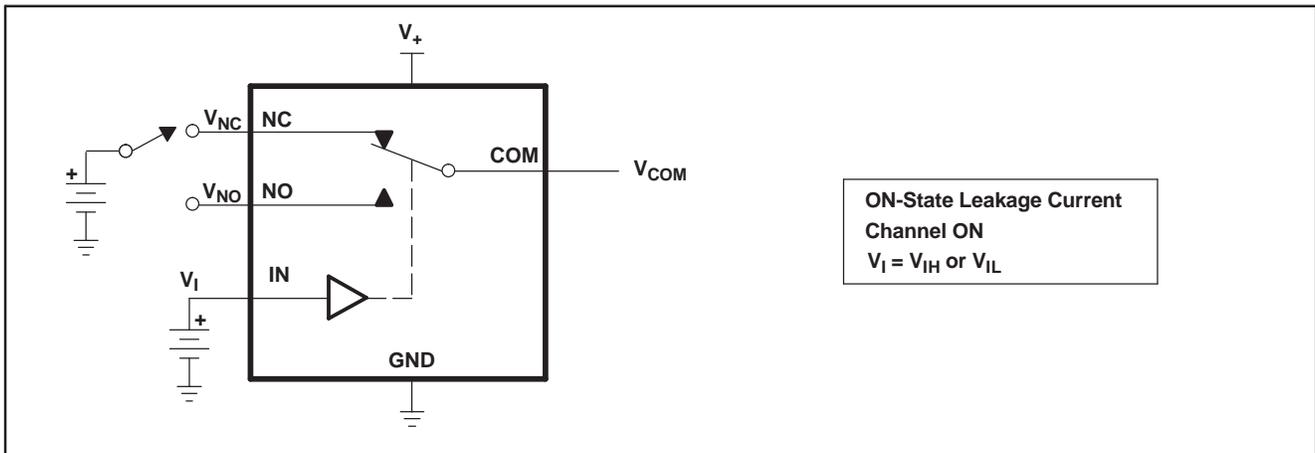


Figure 16. ON-State Leakage Current ( $I_{COM(ON)}$ ,  $I_{NC(ON)}$ ,  $I_{NO(ON)}$ )

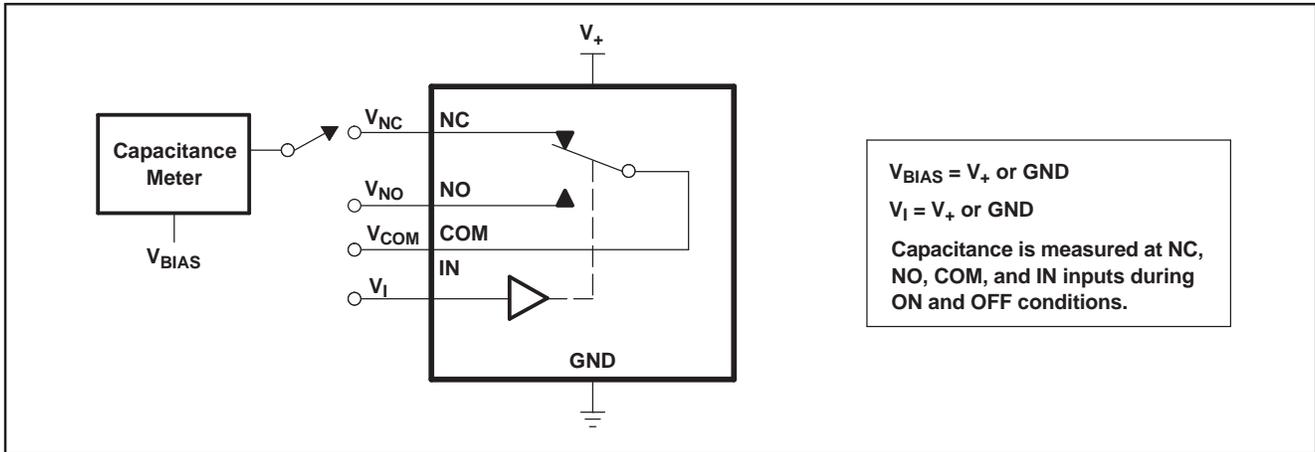
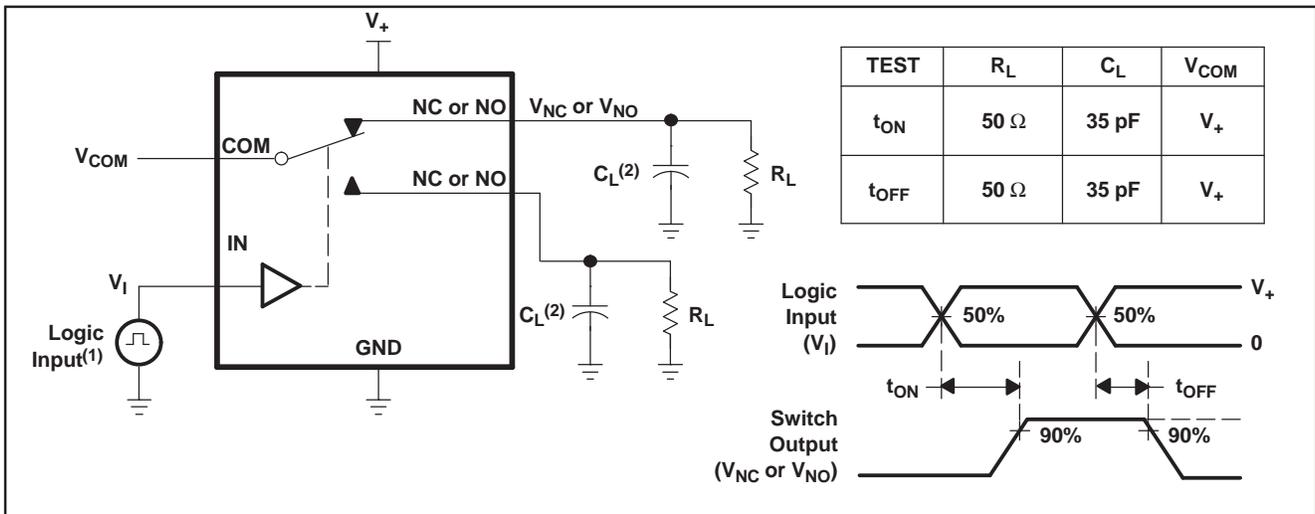
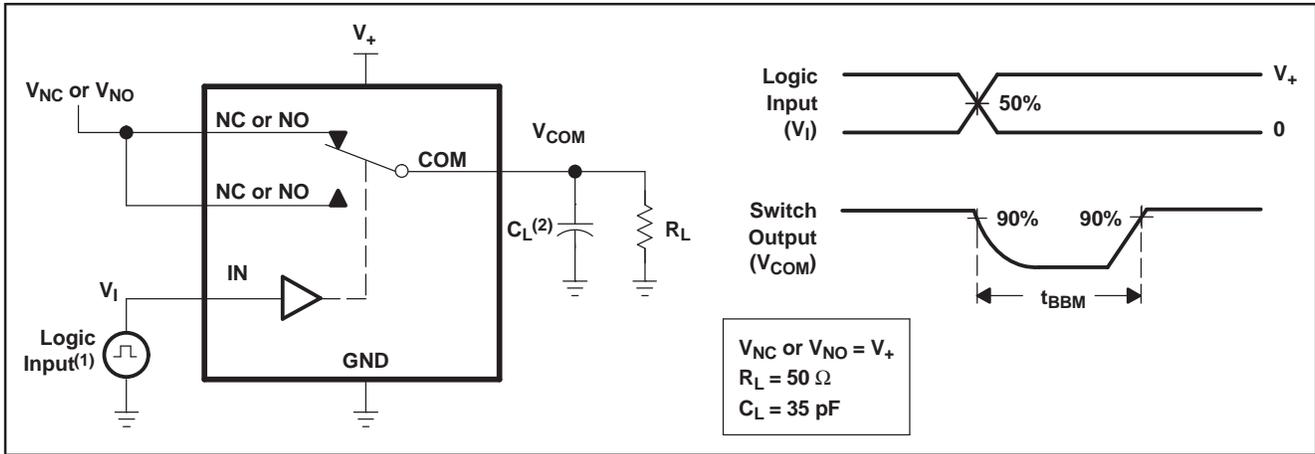


Figure 17. Capacitance ( $C_I$ ,  $C_{COM(ON)}$ ,  $C_{NC(OFF)}$ ,  $C_{NO(OFF)}$ ,  $C_{NC(ON)}$ ,  $C_{NO(ON)}$ )



- (1) All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.
- (2)  $C_L$  includes probe and jig capacitance.

Figure 18. Turn-On ( $t_{ON}$ ) and Turn-Off Time ( $t_{OFF}$ )



- (1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> < 5 ns, t<sub>f</sub> < 5 ns.
- (2) C<sub>L</sub> includes probe and jig capacitance.

Figure 19. Break-Before-Make Time (t<sub>BBM</sub>)

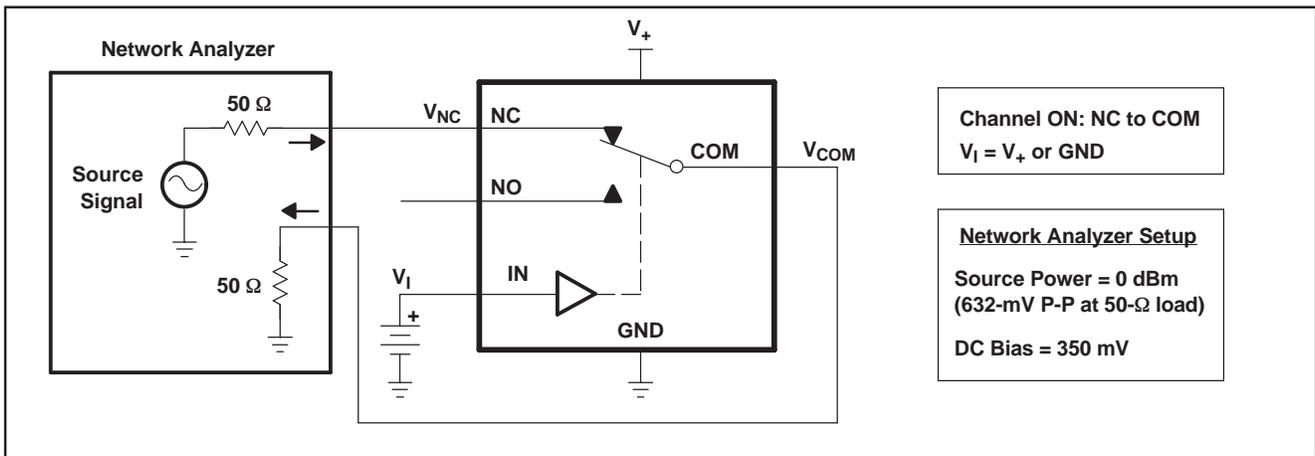


Figure 20. Bandwidth (BW)

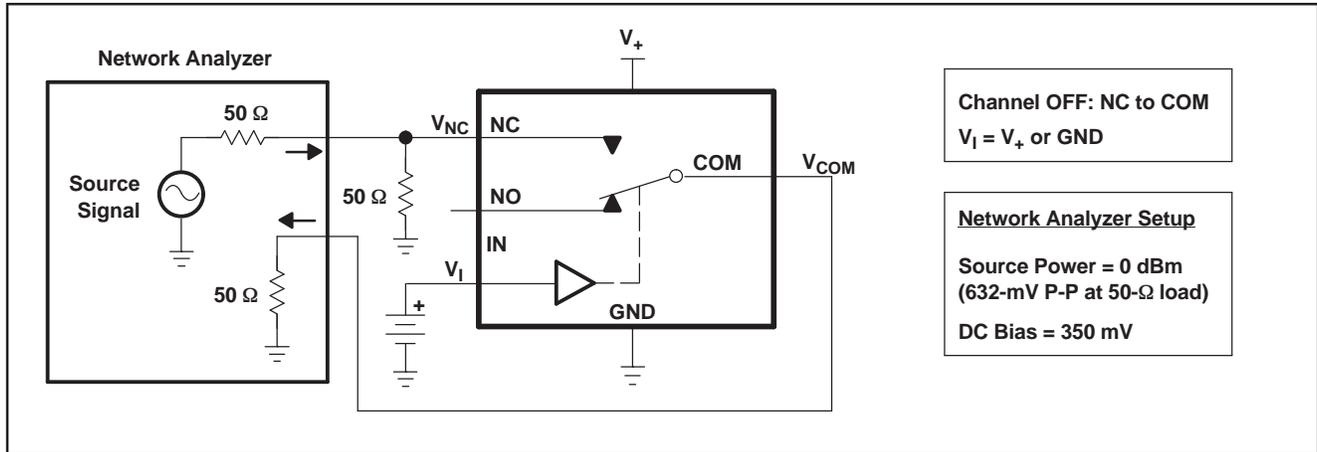


Figure 21. OFF Isolation ( $O_{ISO}$ )

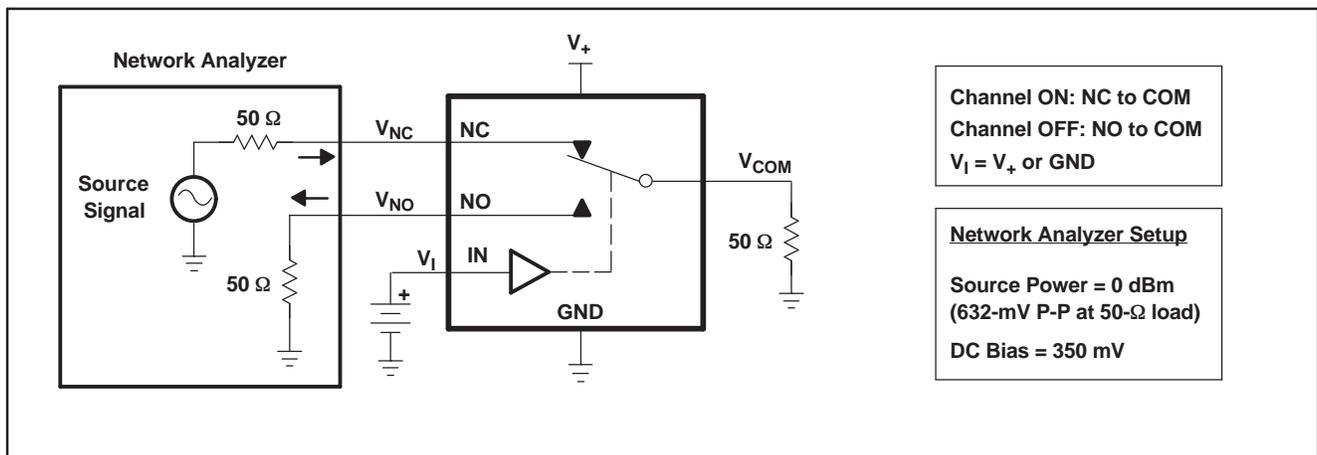
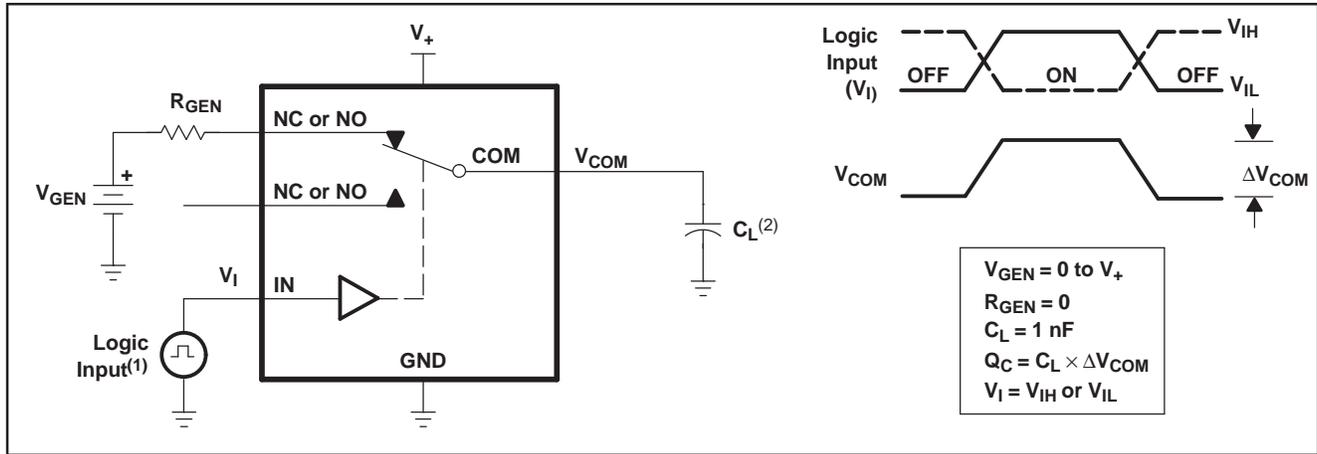
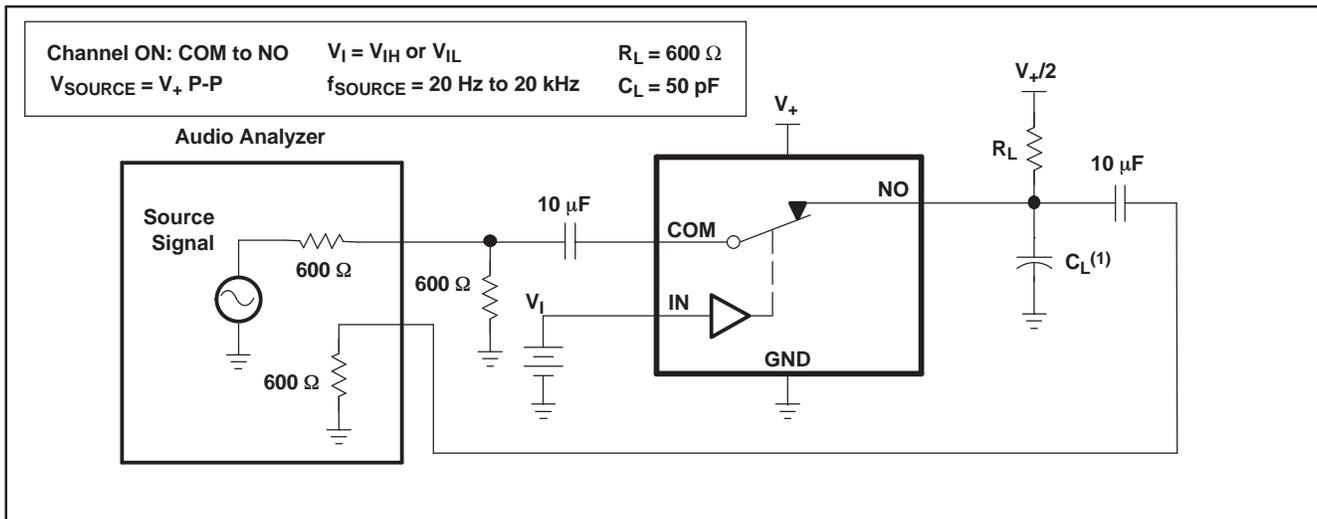


Figure 22. Crosstalk ( $X_{TALK}$ )



- (1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> < 5 ns, t<sub>f</sub> < 5 ns.
- (2) C<sub>L</sub> includes probe and jig capacitance.

**Figure 23. Charge Injection (Q<sub>C</sub>)**



- (1) C<sub>L</sub> includes probe and jig capacitance.

**Figure 24. Total Harmonic Distortion (THD)**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A23159DGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JER	<a href="#">Samples</a>
TS5A23159DGSRE4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JER	<a href="#">Samples</a>
TS5A23159DGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JER	<a href="#">Samples</a>
TS5A23159DGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JER	<a href="#">Samples</a>
TS5A23159DGSTE4	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JER	<a href="#">Samples</a>
TS5A23159DGSTG4	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JER	<a href="#">Samples</a>
TS5A23159RSER	ACTIVE	UQFN	RSE	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JE7 ~ JEO ~ JER)	<a href="#">Samples</a>
TS5A23159RSE4	ACTIVE	UQFN	RSE	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JE7 ~ JEO ~ JER)	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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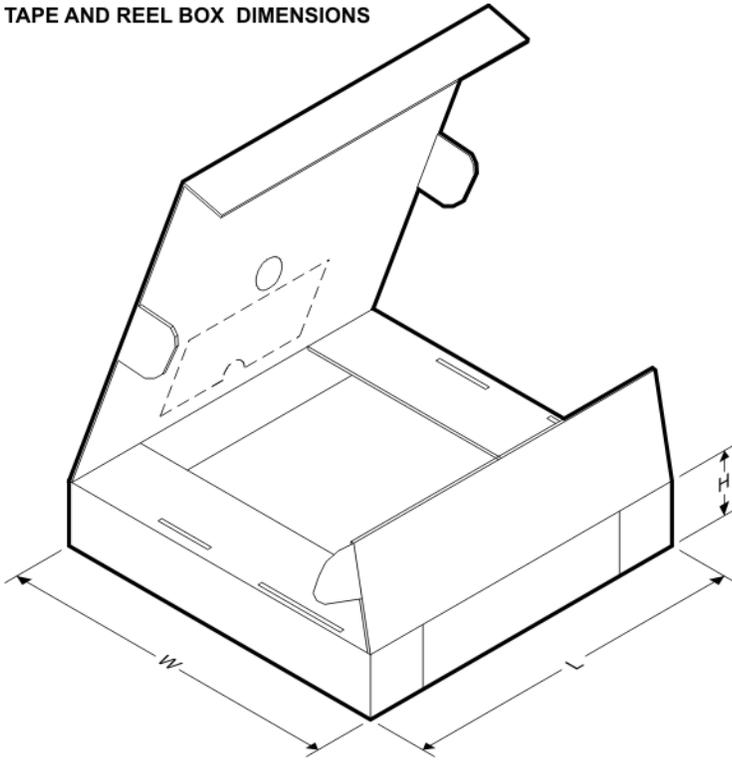
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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A23159DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS5A23159RSER	UQFN	RSE	10	3000	179.0	8.4	1.75	2.25	0.65	4.0	8.0	Q1
TS5A23159RSER	UQFN	RSE	10	3000	180.0	8.4	1.68	2.13	0.76	4.0	8.0	Q1
TS5A23159RSER	UQFN	RSE	10	3000	180.0	9.5	1.68	2.18	0.9	4.0	8.0	Q1

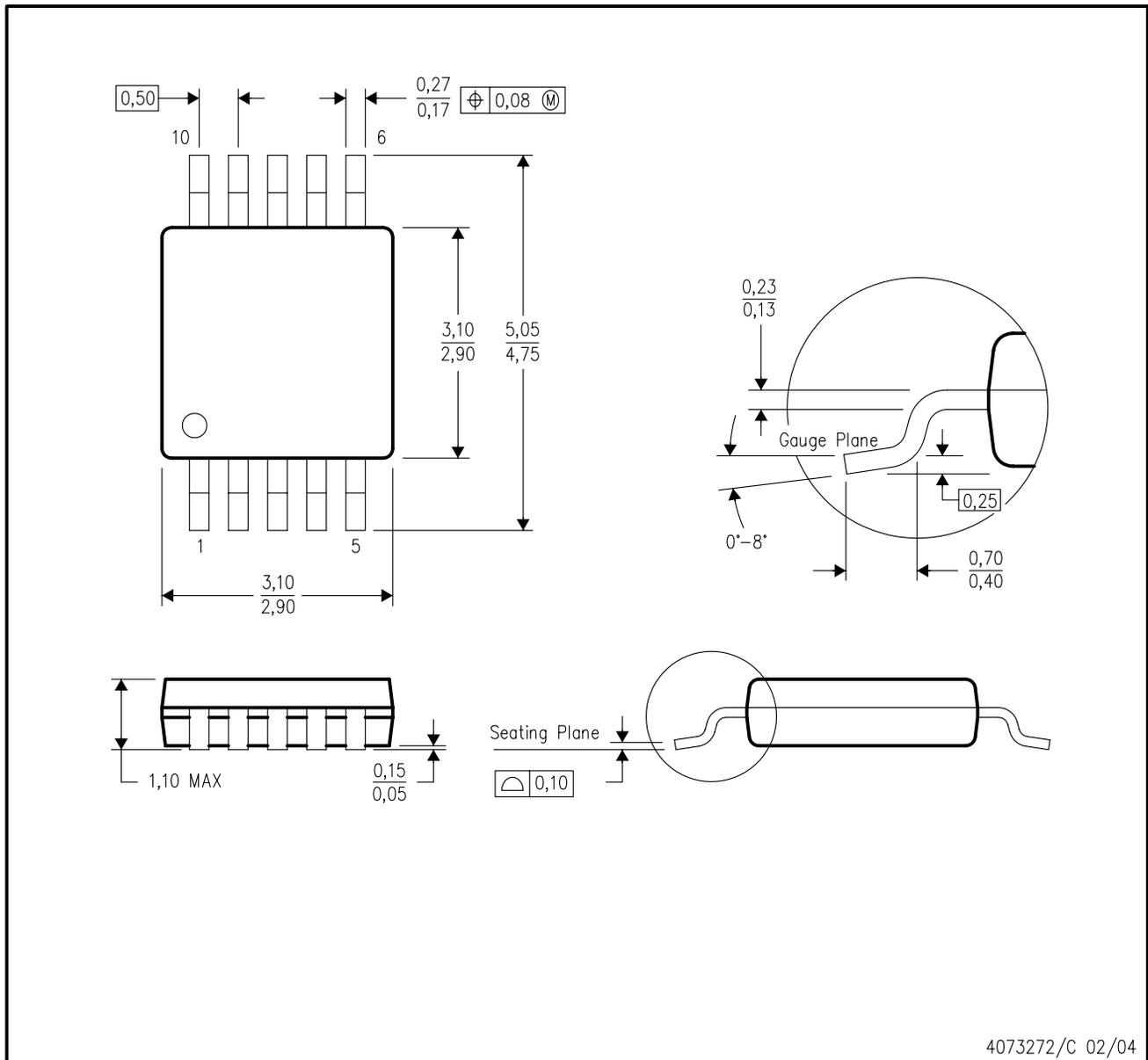
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A23159DGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TS5A23159RSER	UQFN	RSE	10	3000	203.0	203.0	35.0
TS5A23159RSER	UQFN	RSE	10	3000	202.0	201.0	28.0
TS5A23159RSER	UQFN	RSE	10	3000	180.0	180.0	30.0

DGS (S-PDSO-G10)

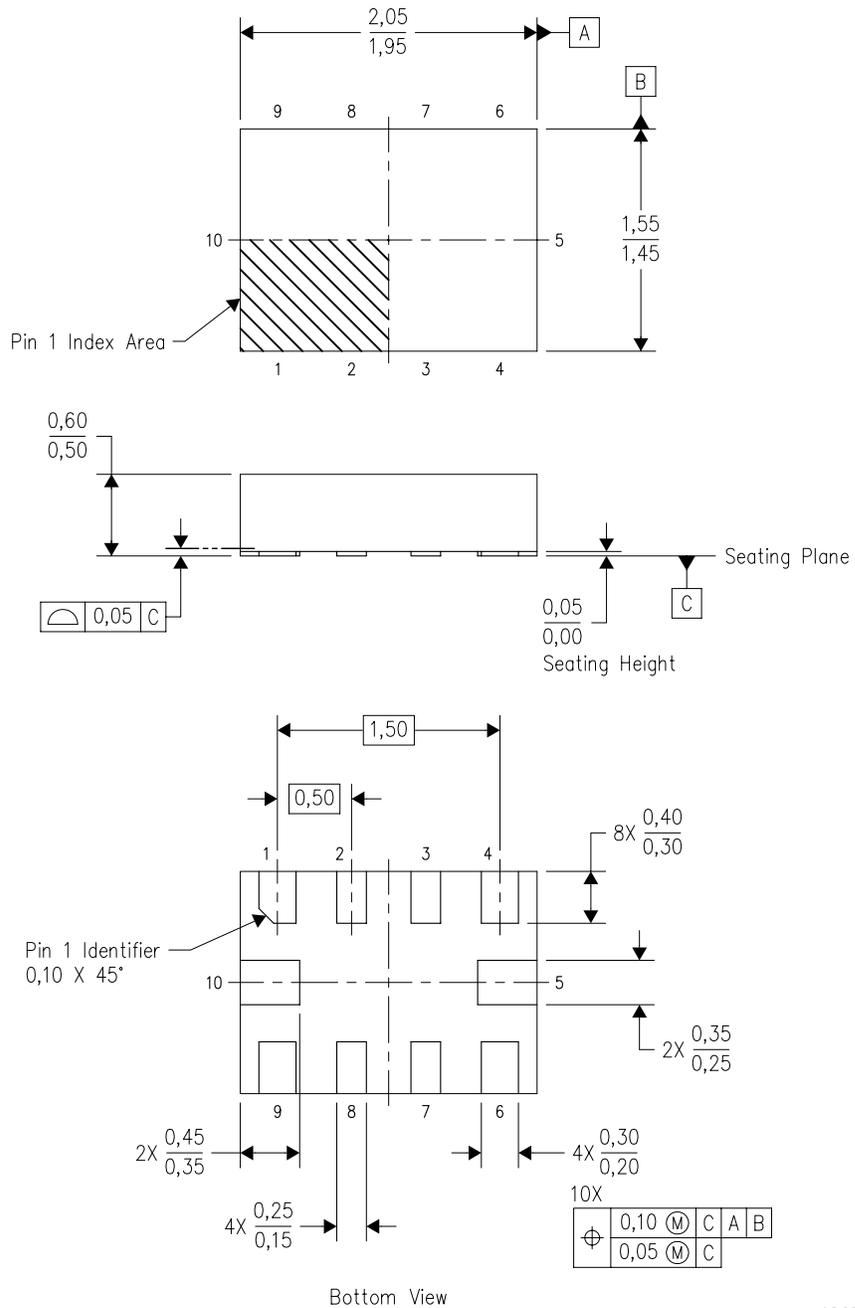
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. Falls within JEDEC MO-187 variation BA.

RSE (R-PUQFN-N10)

PLASTIC QUAD FLATPACK NO-LEAD

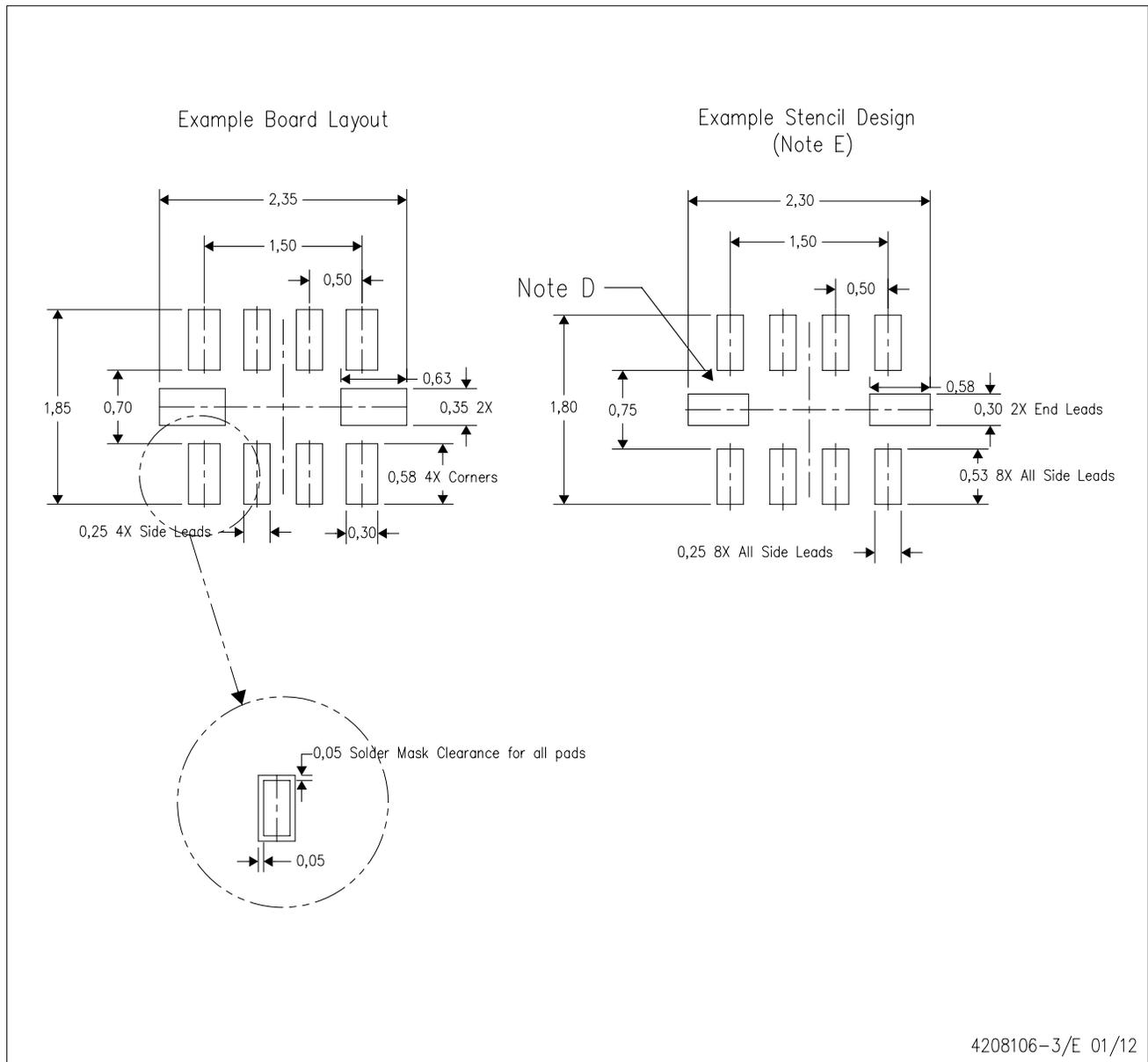


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- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - This package complies to JEDEC MO-288 variation UDFD.

RSE (R-PUQFN-N10)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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