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POTTER CITY CRB

REV 1.0

Wed Oct 27 14:52:59 2010

TITLE PAGE

DEPARTMENT
DCPAE

Intel Corporation
2200 Mission College Blvd.
P.O. BOX 58119
Santa Clara, CA 95052-8119

SIZE	CODE	DOCUMENT NUMBER	REV
B	34649	444359	1.0

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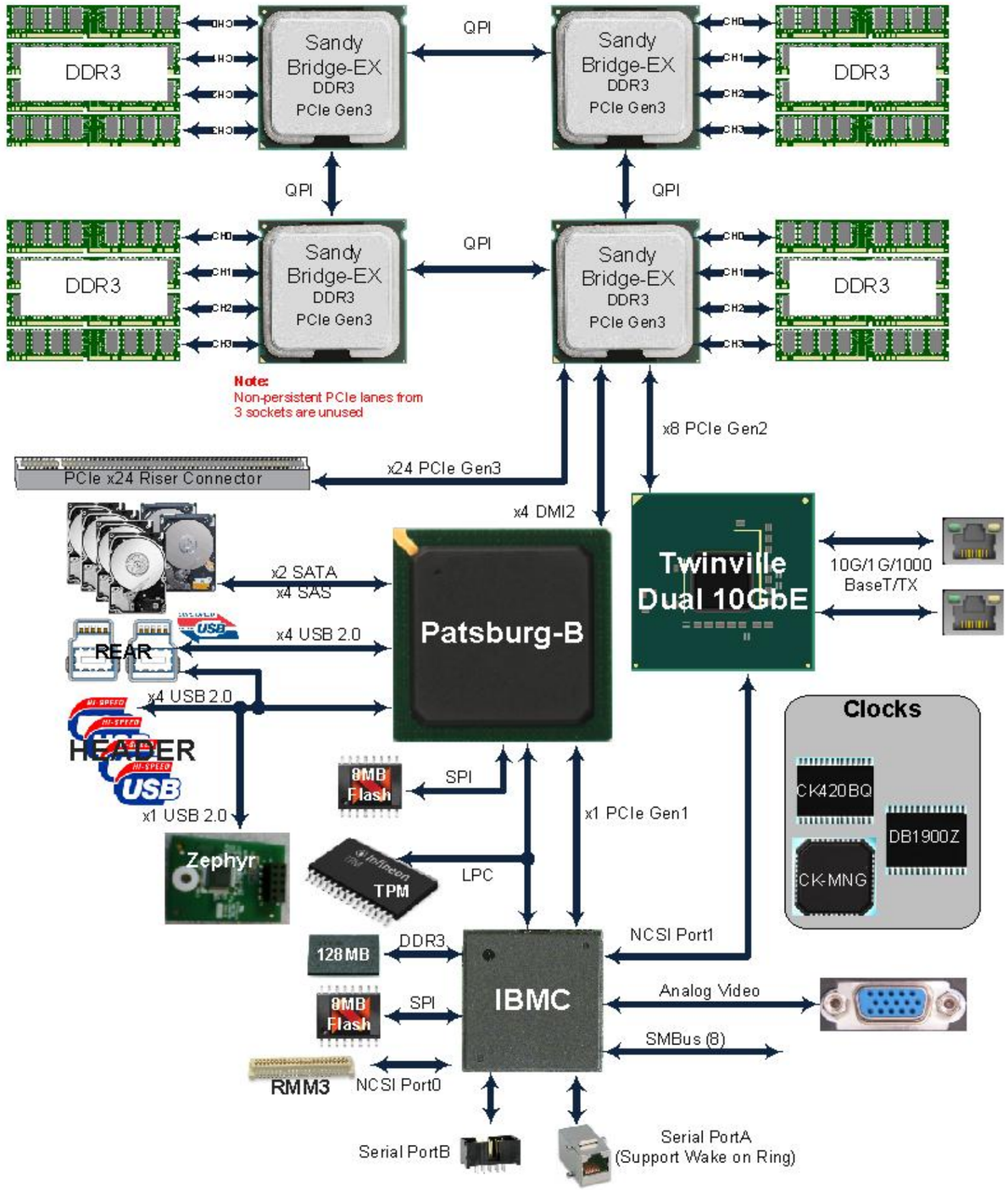

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SYSTEM BLOCK DIAGRAM

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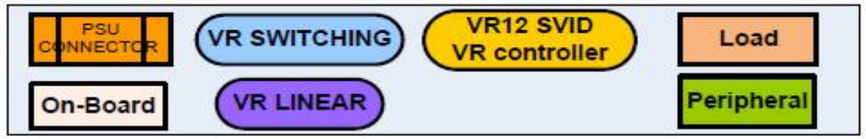
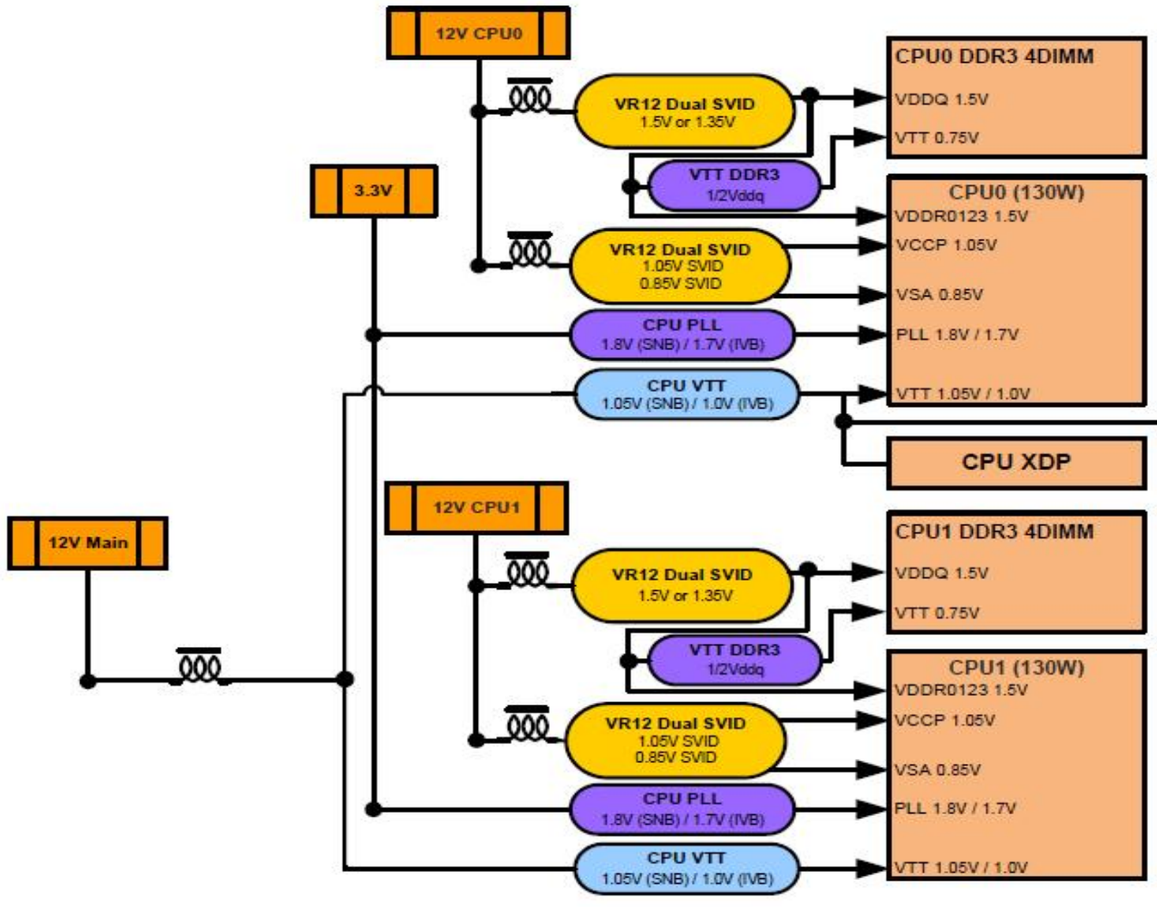
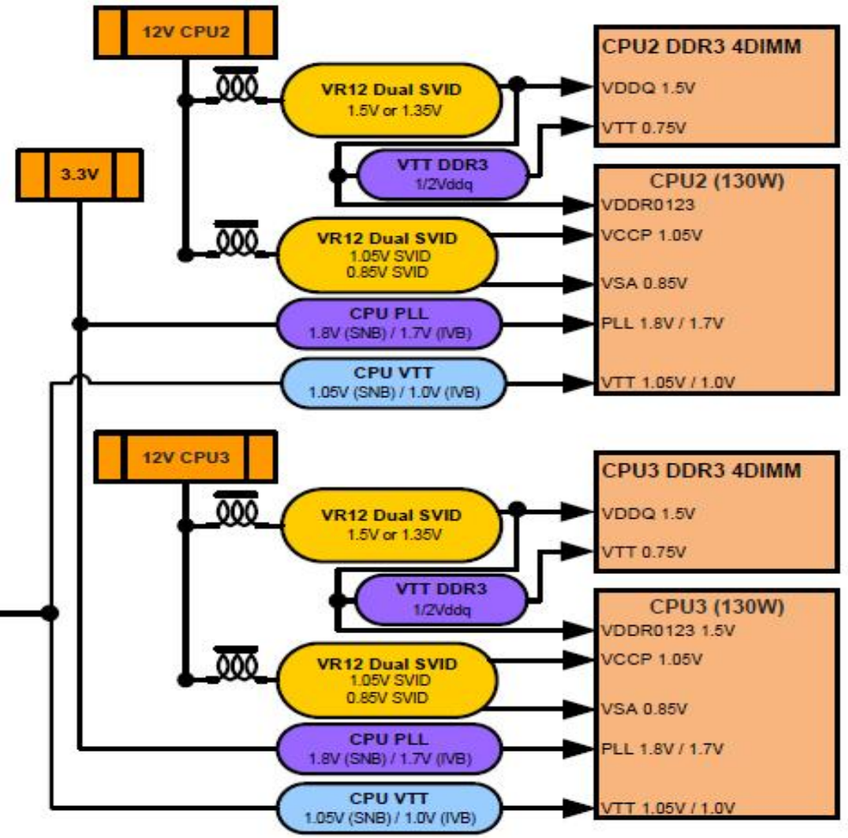
Potter City VR Block Diagram







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POWER BLOCK DIAGRAM (1-2)

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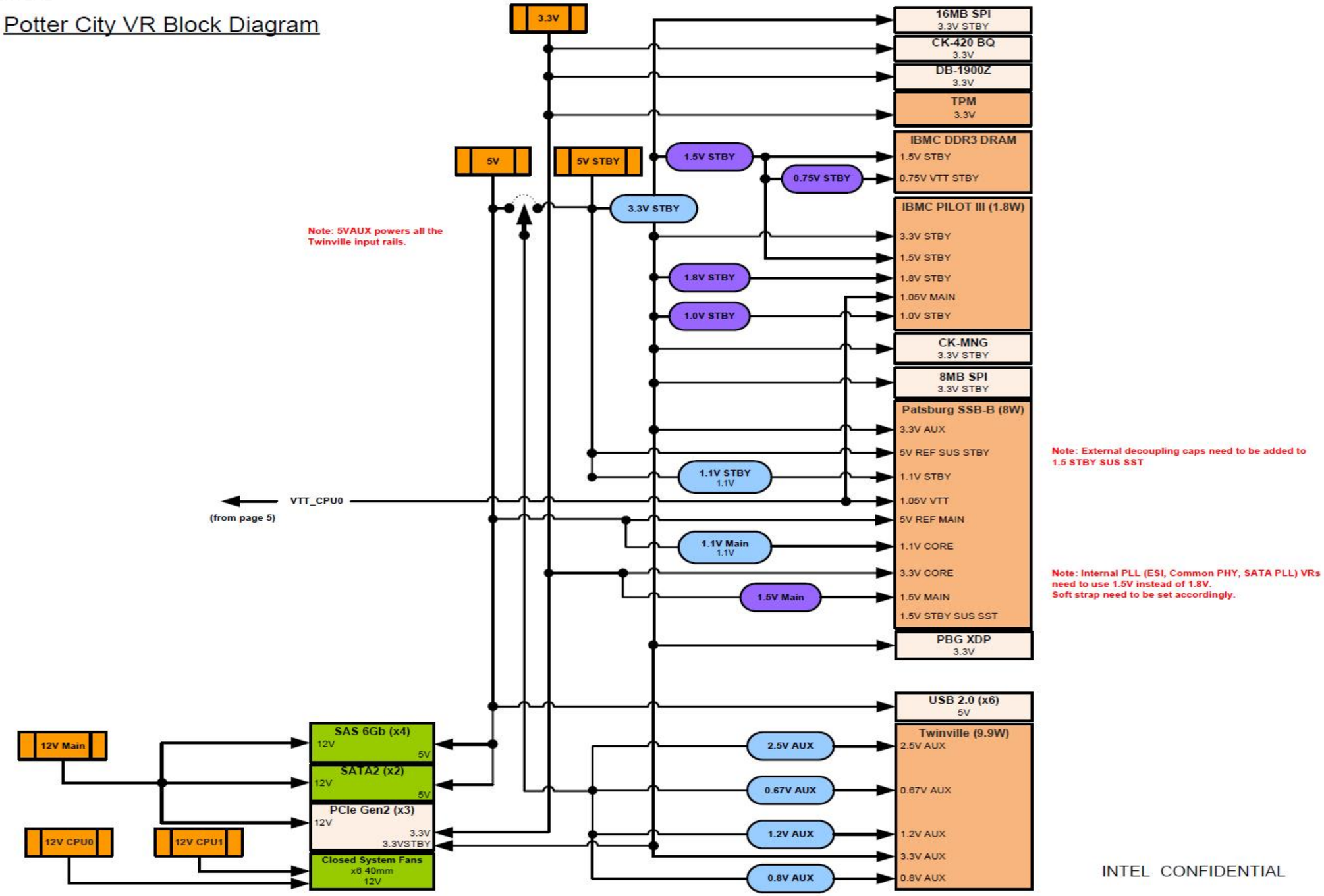
Potter City VR Block Diagram



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POWER BLOCK DIAGRAM (2-2)

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NETNAME	VOLTAGE	SOURCE	USAGE
P12V	12.0V	PSU	CPUs VTT VRDs
N12V	-12.0V	PSU	IBMC Serial Port, PCIE slot, Processor debug leds
P3V3	3.3V	PSU	CPUs PLL VRDs, PBG-B, PCIE slot, CLKs, others
P5V	5.0V	PSU	VRDs, PBG-B, USB ports, TPM, PCIE slot, IBMC video, others
P5V_STBY	5.0V	PSU	VRDs, PBG-B, USB, others
P12V_CPU0	12.0V	PSU	CPU0 VR12 (PVCCP, PVSA, PVDDQ), Fans
P12V_CPU1	12.0V	PSU	CPU1 VR12 (PVCCP, PVSA, PVDDQ), Fans
P12V_CPU2	12.0V	PSU	CPU2 VR12 (PVCCP, PVSA, PVDDQ)
P12V_CPU3	12.0V	PSU	CPU3 VR12 (PVCCP, PVSA, PVDDQ)
P5V_AUX	5.0V	P5V/P5V_STBY	AUX VRDs
P1V05_VCCP_CPU0	1.1V	P12V_CPU0	CPU0
P0V85_VSA_CPU0	0.85V	P12V_CPU1	CPU0
P1V05_VCCP_CPU1	1.1V	P12V_CPU1	CPU1
P0V85_VSA_CPU1	0.85V	P12V_CPU2	CPU1
P1V05_VCCP_CPU2	1.1V	P12V_CPU2	CPU2
P0V85_VSA_CPU2	0.85V	P12V_CPU3	CPU2
P1V05_VCCP_CPU3	1.1V	P12V_CPU3	CPU3
P0V85_VSA_CPU3	0.85V	P12V_CPU4	CPU3
P1V5_DDR3_CPU0	1.5V	P12V_CPU0	CPU0, CPU0 DDR3 DIMMS
P0V75_VTT_DDR3_CPU0	0.75V	P1V5_DDR3_CPU0	CPU0 DDR3 DIMMS
P1V5_DDR3_CPU1	1.5V	P12V_CPU1	CPU1, CPU1 DDR3 DIMMS
P0V75_VTT_DDR3_CPU1	0.75V	P1V5_DDR3_CPU1	CPU1 DDR3 DIMMS
P1V5_DDR3_CPU2	1.5V	P12V_CPU2	CPU2, CPU2 DDR3 DIMMS
P0V75_VTT_DDR3_CPU2	0.75V	P1V5_DDR3_CPU2	CPU2 DDR3 DIMMS
P1V5_DDR3_CPU3	1.5V	P12V_CPU3	CPU3, CPU3 DDR3 DIMMS
P0V75_VTT_DDR3_CPU3	0.75V	P1V5_DDR3_CPU3	CPU3 DDR3 DIMMS
P1V8_PLL_CPU0	1.8V (SNB-EX) or 1.7V (IVB-EXB)	3.3V	CPU0
P1V8_PLL_CPU1	1.8V (SNB-EX) or 1.7V (IVB-EXB)	3.3V	CPU1
P1V8_PLL_CPU2	1.8V (SNB-EX) or 1.7V (IVB-EXB)	3.3V	CPU2
P1V8_PLL_CPU3	1.8V (SNB-EX) or 1.7V (IVB-EXB)	3.3V	CPU3
P1V05_VTT_CPU0	1.05V (SNB-EX) or 1.0V (IVB-EXB)	5V	CPU0, PBG-B, IBMC
P1V05_VTT_CPU1	1.05V (SNB-EX) or 1.0V (IVB-EXB)	5V	CPU1, PBG-B, IBMC
P1V05_VTT_CPU2	1.05V (SNB-EX) or 1.0V (IVB-EXB)	5V	CPU2, PBG-B, IBMC
P1V05_VTT_CPU3	1.05V (SNB-EX) or 1.0V (IVB-EXB)	5V	CPU3, PBG-B, IBMC
P1V1_STBY_PBG	1.1V	P5V_STBY	PBG-B
P1V8_STBY_IBMC	1.8V	P3V3_STBY	IBMC
P1V1_MAIN_PBG	1.1V	P5V	PBG-B
P0V75_STBY_IBMC	0.75V	P5V_STBY	IBMC DDR3
P1V5_MAIN_PBG	1.5V	P3V3	PBG-B
P3V3_STBY	3.3V	P5V_STBY	PBG-B, IBMC, CK-MNG, PCIE slot, others
P1V5_STBY_IBMC	1.5V	P3V3_STBY	IBMC, IBMC DDR3
P1V0_STBY_IBMC	1.0V	P3V3_STBY	IBMC
P2V5_AUX_TWINVILLE	2.5V	P5V_AUX	Twinville
P0V8_AUX_TWINVILLE	0.8V	P5V_AUX	Twinville
P1V2_AUX_TWINVILLE	1.2V	P5V_AUX	Twinville
P0V67_AUX_TWINVILLE	0.67V	P5V_AUX	Twinville

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VOLTAGE TABLE

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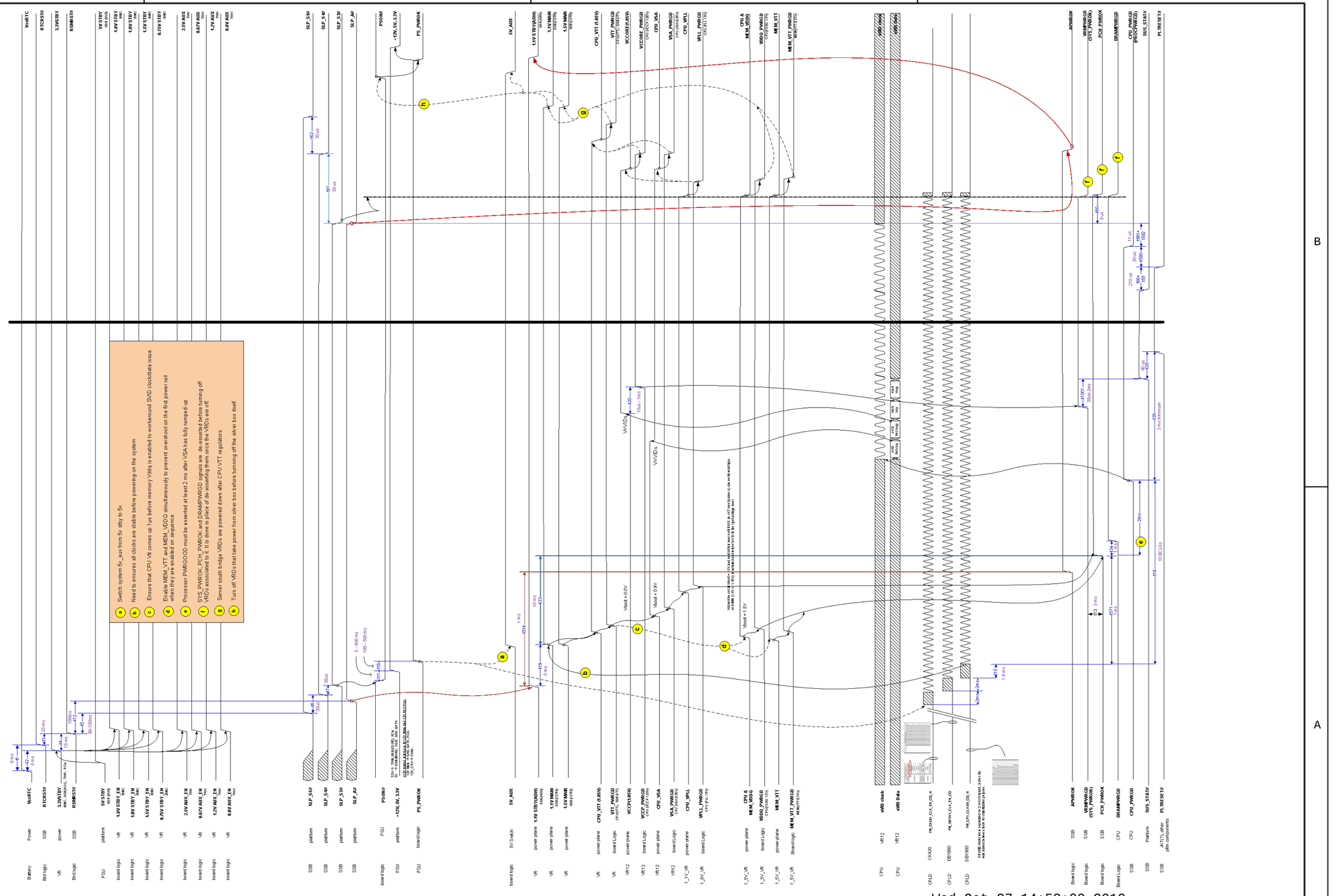

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POWER-ON SEQUENCE TIMING DIAGRAM

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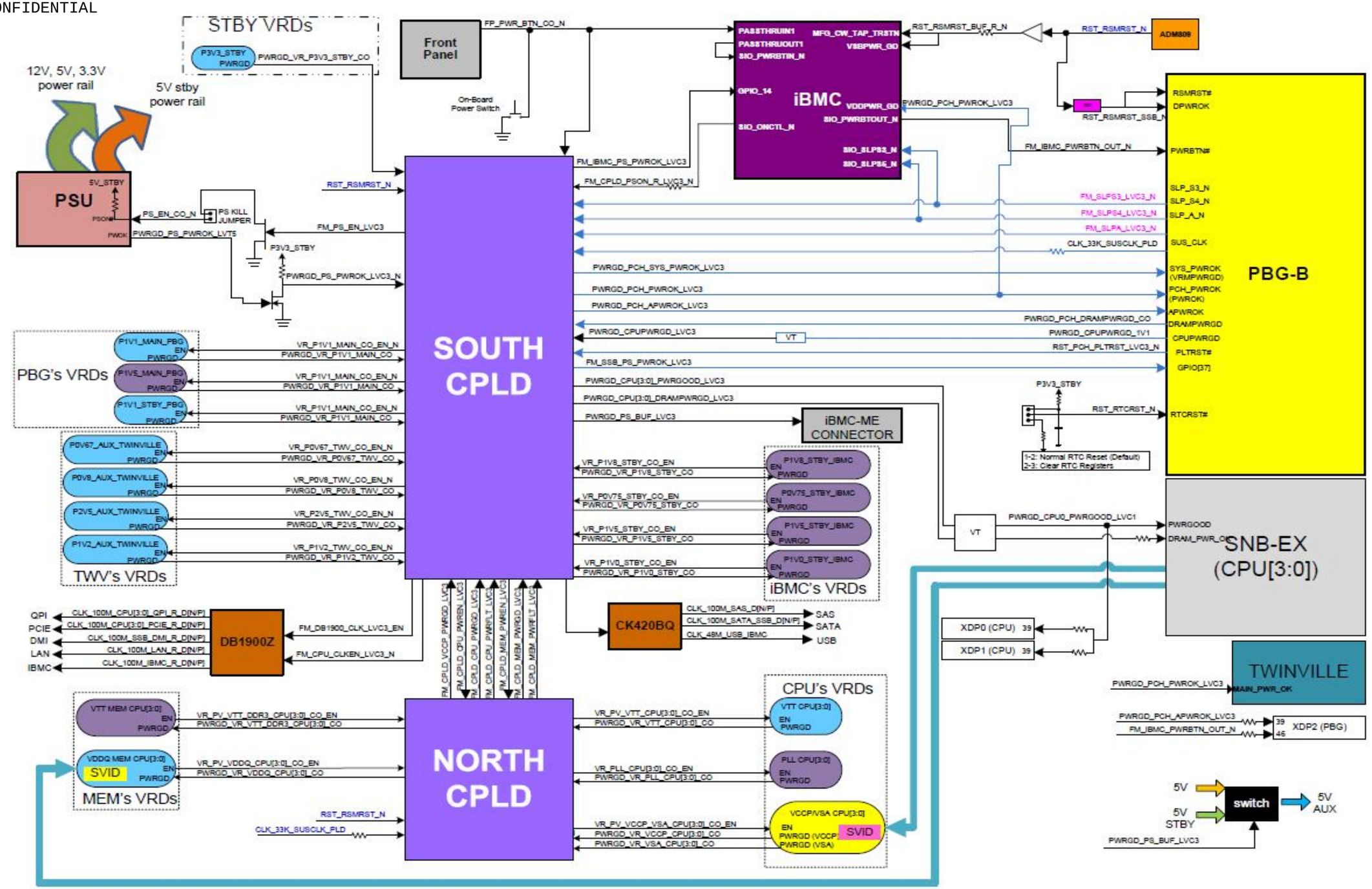

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POWER-ON BLOCK DIAGRAM

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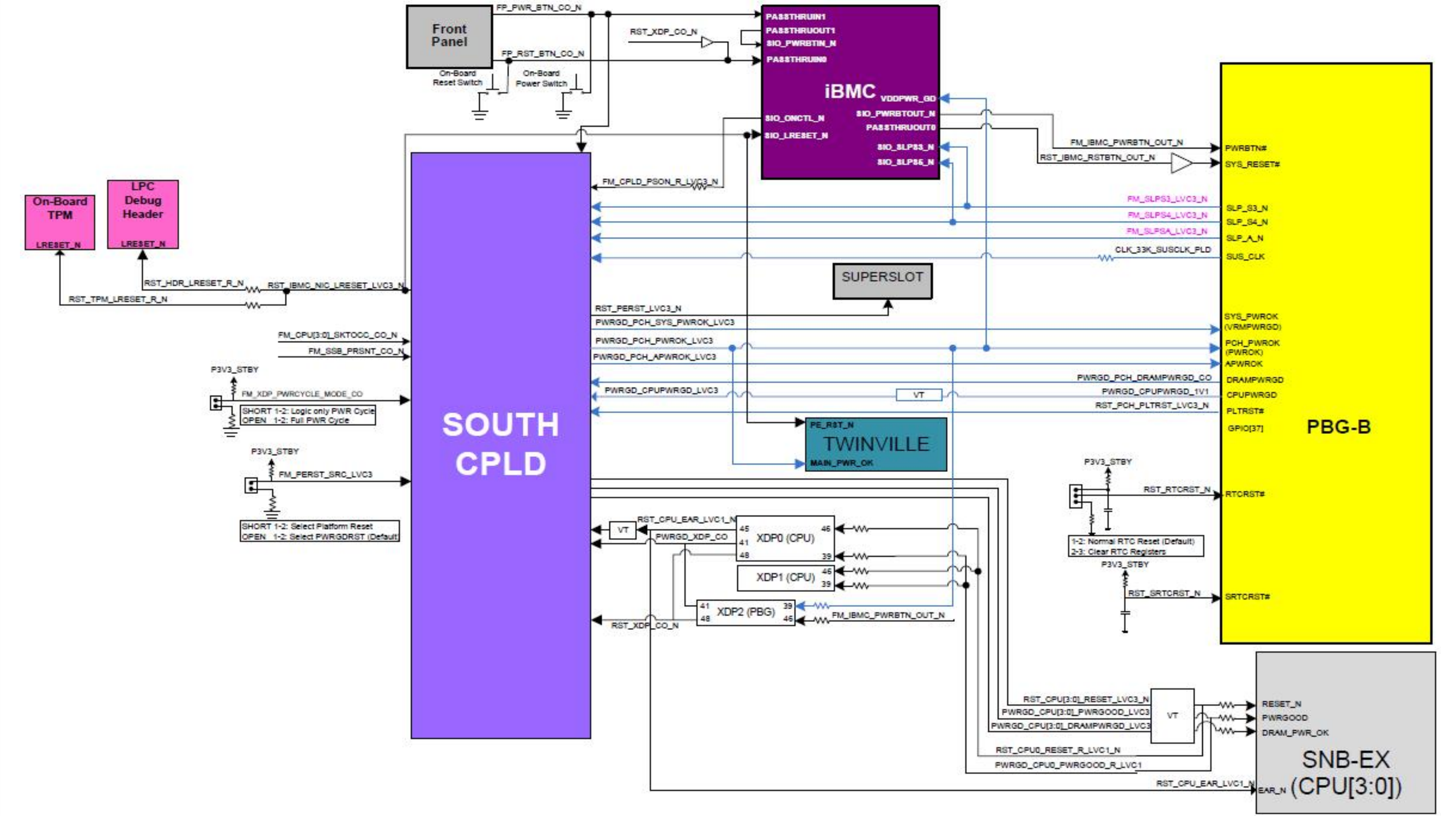

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POWER GOOD/RESET BLOCK DIAGRAM

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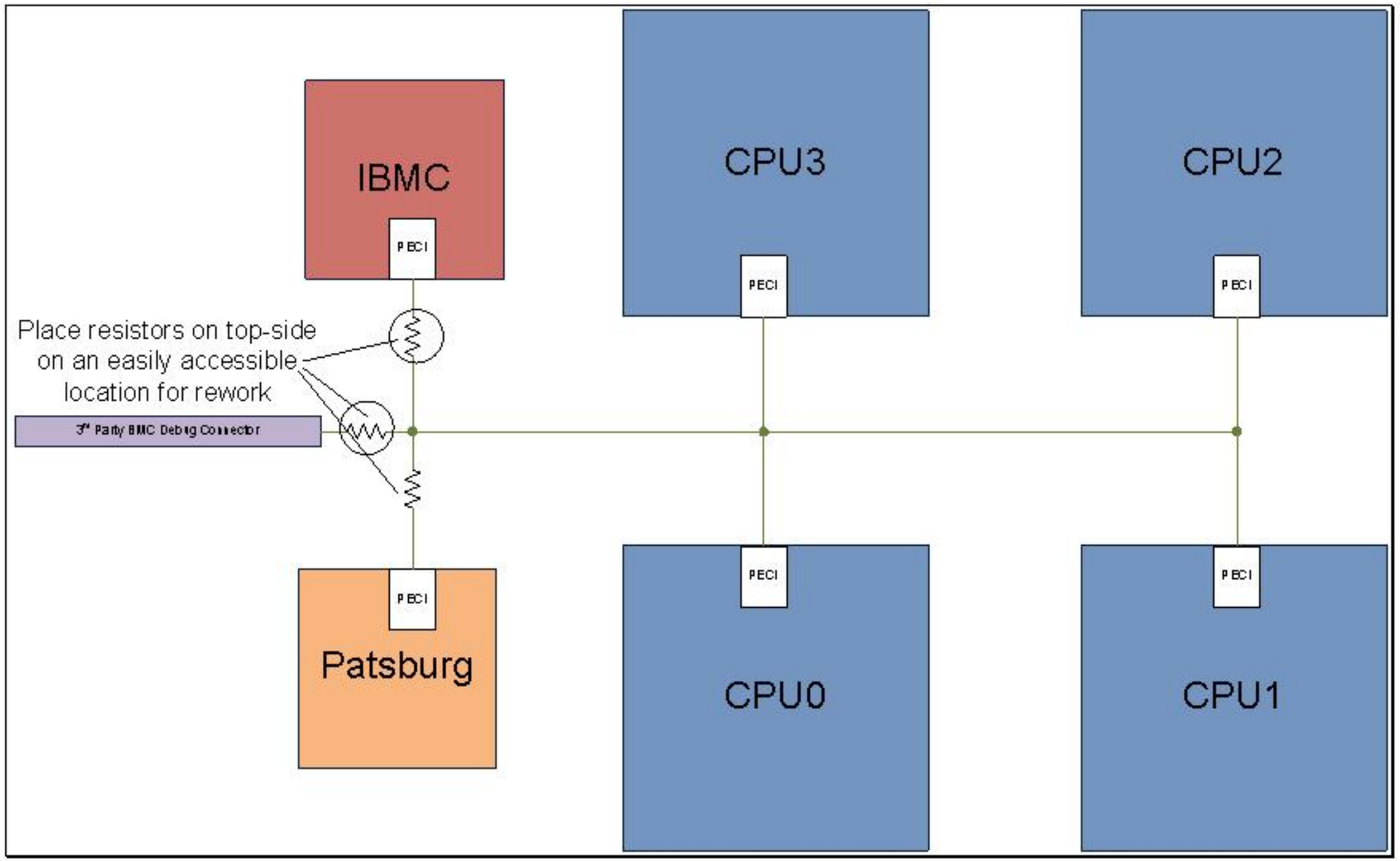

PECI BUS BLOCK DIAGRAM

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Potter City QPI Link Connectivity

SKT	port (RX)	Potter City Lane name	Lane Reversal	Polarity Inversion on lanes	No Polarity Inversion on lanes	
0	0	QPI_CPU3_CPU0_P1P0	Yes	0,1,2,3,5,8,10,11,12,13,14,15,16,17,18,19	4,6,7,9	L8
	1	QPI_CPU1_CPU0_P0P1	Yes	4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19	0,1,2,3	L8
1	0	QPI_CPU0_CPU1_P1P0	Yes	0,1,2,3,5,8,10,11,12,13,14,15,16,17,18,19	4,6,7,9	L3
	1	QPI_CPU2_CPU1_P0P1	Yes	4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19	0,1,2,3	L3
2	0	QPI_CPU1_CPU2_P1P0	Yes	0,1,2,3,5,8,10,11,12,13,14,15,16,17,18,19	4,6,7,9	L8
	1	QPI_CPU3_CPU2_P0P1	Yes	4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19	0,1,2,3	L8
3	0	QPI_CPU2_CPU3_P1P0	Yes	0,1,2,3,5,8,10,11,12,13,14,15,16,17,18,19	4,6,7,9	L3
	1	QPI_CPU0_CPU3_P0P1	Yes	4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19	0,1,2,3	L3

Potter City PCIE Link Connectivity on Riser Connector

Slot Config	Potter City Lane name	CPU 0 pin name	Slotx Pin Name	Lane Reversal	Polarity Inversion on lanes (referred to Slot Pin Name)
x16	P3E_CPU0_RCONN_TX_PE3A<3..0>	PE3A_TX<3:0>	P2E_SLOT5_T<3:0>	NO	NO
	P3E_CPU0_RCONN_TX_PE3B<3..0>	PE3B_TX<7:4>	P2E_SLOT5_T<7:4>		NO
	P3E_CPU0_RCONN_TX_PE3C<3..0>	PE3C_TX<3:0>	P2E_SLOT6_T<3:0>		NO
	P3E_CPU0_RCONN_TX_PE3D<3..0>	PE3D_TX<7:4>	P2E_SLOT6_T<7:4>		NO
	P3E_CPU0_RCONN_RX_PE3A<3..0>	PE3A_RX<3:0>	P2E_SLOT5_R<3:0>		NO
	P3E_CPU0_RCONN_RX_PE3B<3..0>	PE3B_RX<7:4>	P2E_SLOT5_R<7:4>		7,6,5,4
	P3E_CPU0_RCONN_RX_PE3C<3..0>	PE3C_RX<3:0>	P2E_SLOT6_R<3:0>		NO
	P3E_CPU0_RCONN_RX_PE3D<3..0>	PE3D_RX<7:4>	P2E_SLOT6_R<7:4>		NO
x8	P3E_CPU0_RCONN_TX_PE1A<3..0>	PE1A_TX<3:0>	P2E_SLOT4_T<3:0>	NO	2,1,0
	P3E_CPU0_RCONN_TX_PE1B<3..0>	PE1B_TX<7:4>	P2E_SLOT4_T<7:4>		NO
	P3E_CPU0_RCONN_RX_PE1A<3..0>	PE1A_RX<3:0>	P2E_SLOT4_R<3:0>		NO
	P3E_CPU0_RCONN_RX_PE1B<3..0>	PE1B_RX<7:4>	P2E_SLOT4_R<7:4>		NO

Potter City PCIE Link between CPU0 and Twinville (NIC)

Link	Potter City Lane name	CPU 0 pin name	TWV Pin Name	Lane Reversal	Polarity Inversion on lanes (referred to TWV Pin Name)
x8	P2E_CPU0_TWV_TX_PE2C<3..0>	PE2C_TX<11:8>	PET<3:0>	NO	NO
	P2E_CPU0_TWV_TX_PE2D<3..0>	PE2D_TX<15:12>	PET<7:4>		NO
	P2E_CPU0_TWV_RX_PE2C<3..0>	PE2C_RX<11:8>	PER<3:0>		NO
	P2E_CPU0_TWV_RX_PE2D<3..0>	PE2D_RX<15:12>	PER<7:4>		NO

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CPU QPI/PCIE LANE REVERSE & POLARITY INV

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	Lane Reversal	Polarity Inversion
DMI (From CPU0 to PBG)	Yes: FROM UPSTREAM DEVICE (CPU)	No
PCIE from PBG to iBMC	No	No

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PBG PCIE LANE REVERSE & POLARITY INV

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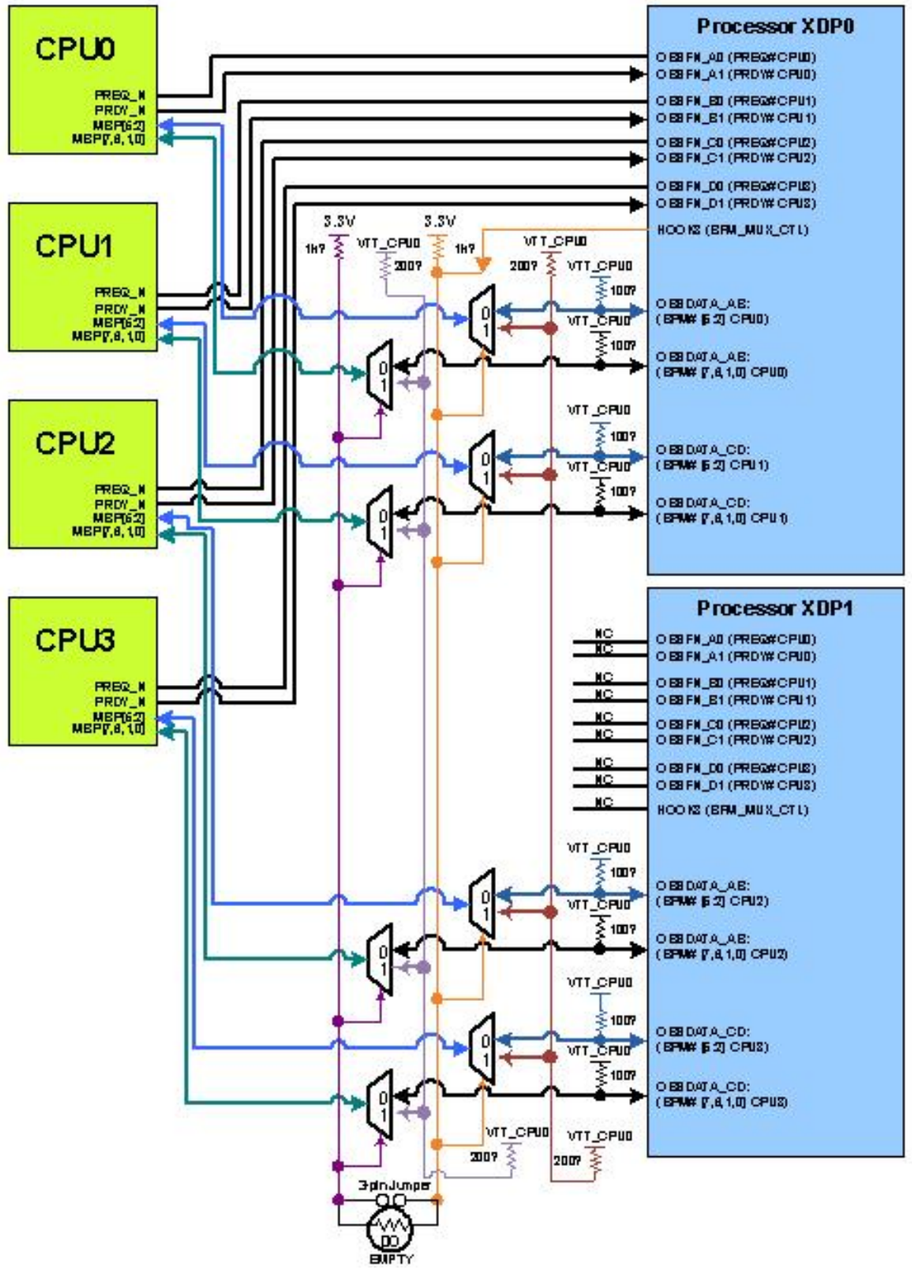
NOTES:
Remove 3-pin jumper for production and stuff 0-ohm



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XDP0/XDP1 (CPU) BLOCK DIAGRAM

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 14 OF 303	

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DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 15 OF 303	

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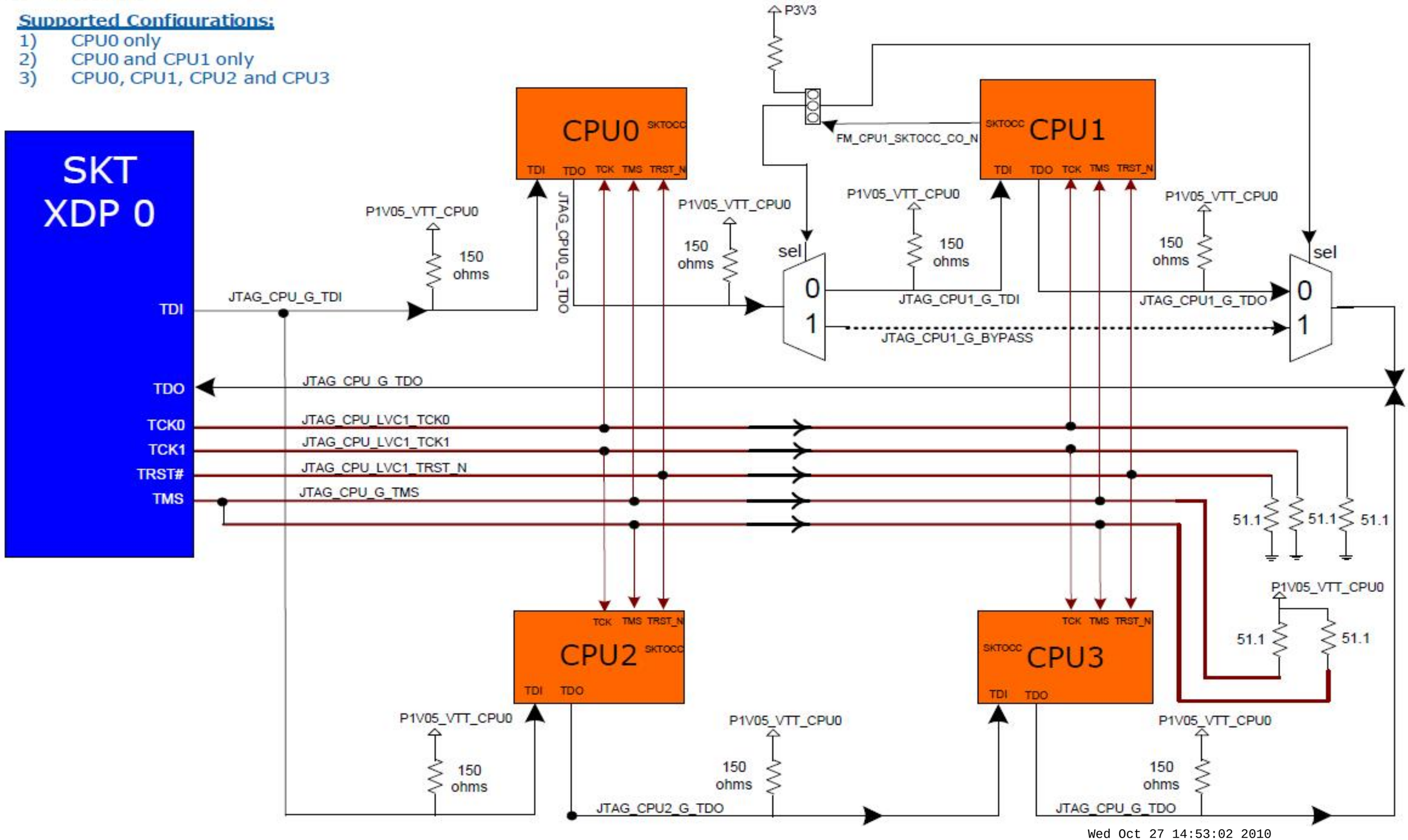
Supported Configurations:

1) CPU0 only
2) CPU0 and CPU1 only
3) CPU0, CPU1, CPU2 and CPU3



Wed Oct 27 14:53:02 2010

JTAG (DEV) BLOCK DIAGRAM

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 16 OF 303

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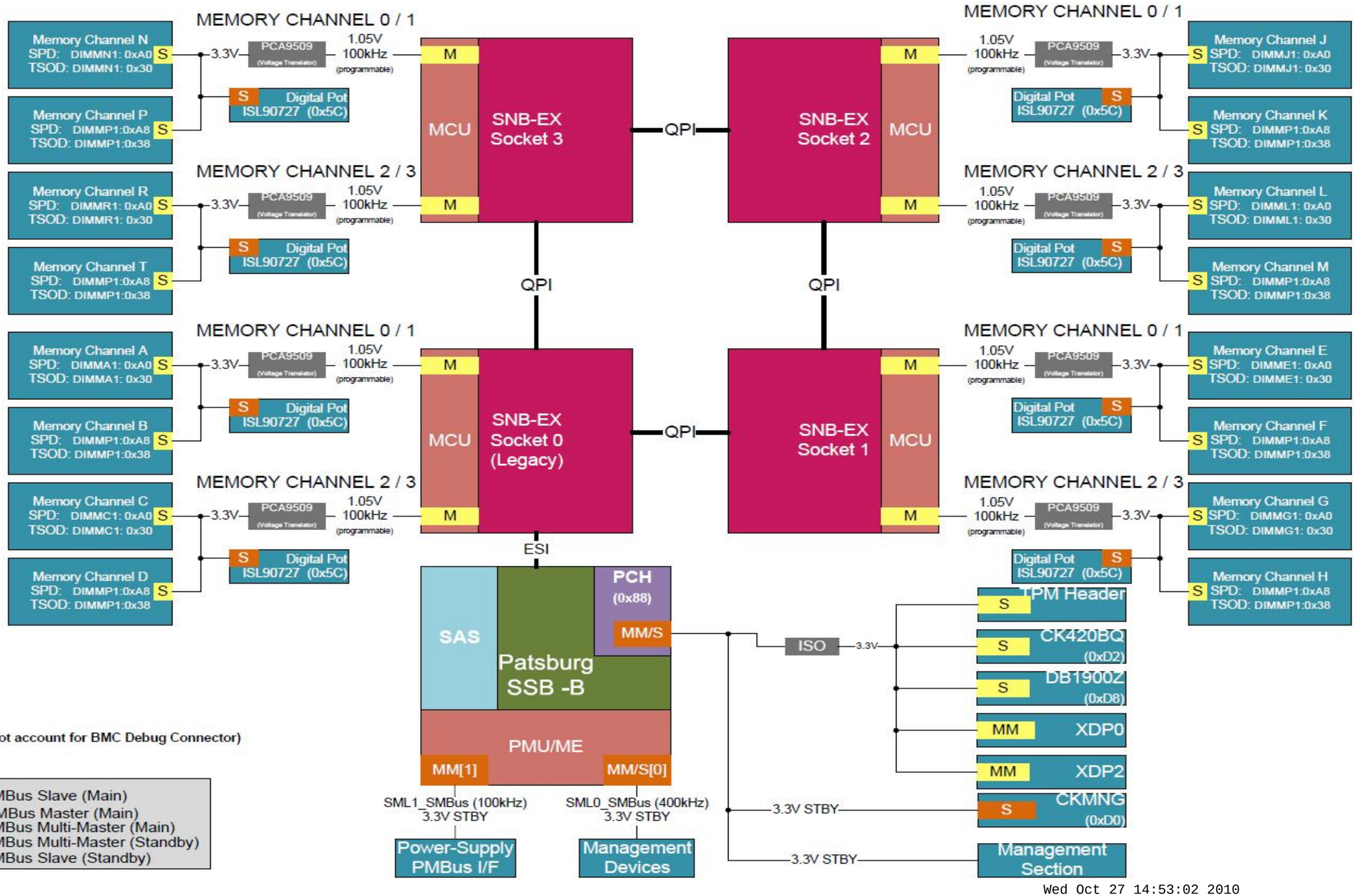
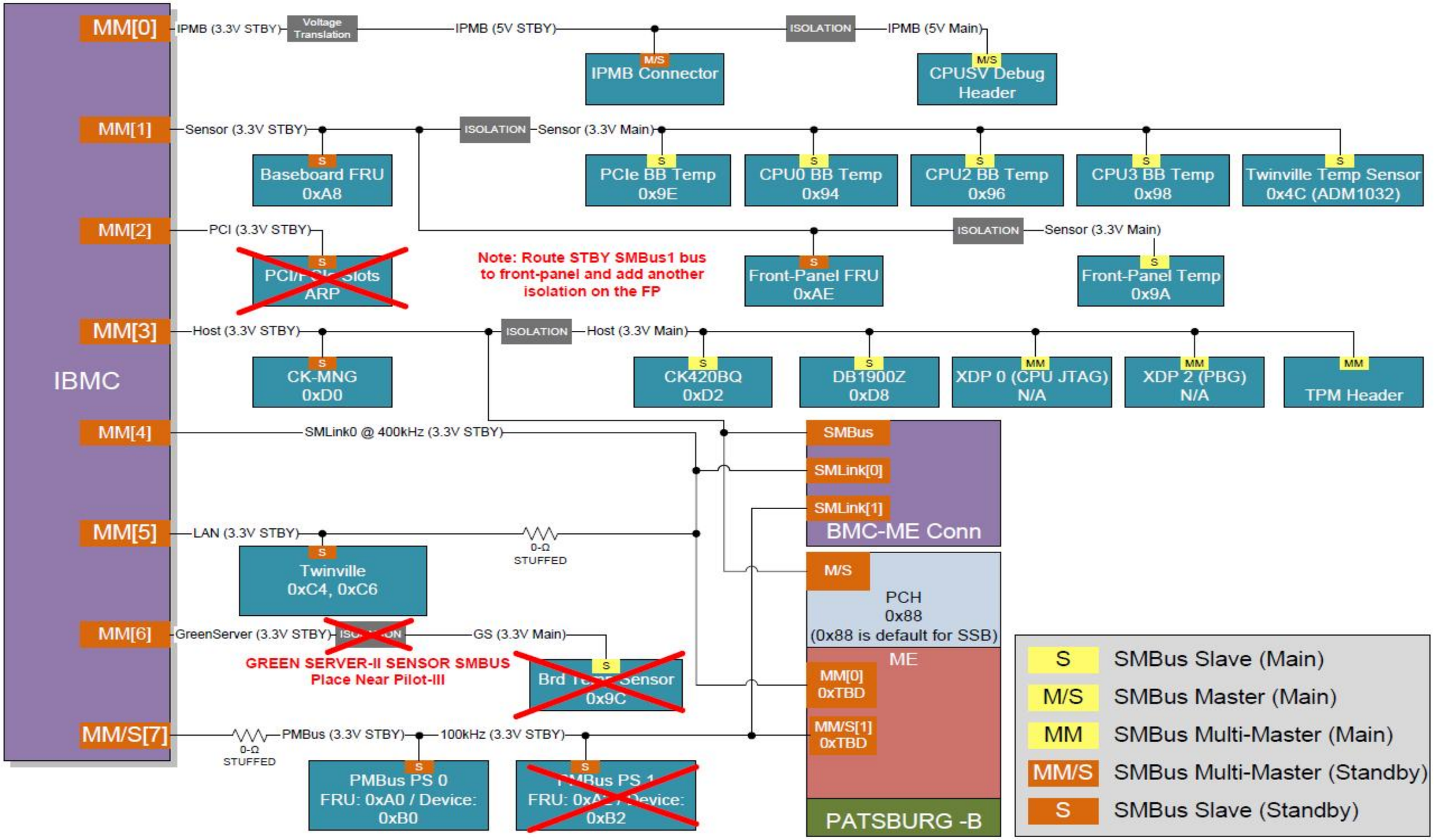


Wed Oct 27 14:53:02 2010

SMBUS BLOCK DIAGRAM (1-2)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 17 OF 303	

INTEL CONFIDENTIAL



Wed Oct 27 14:53:03 2010

SMBUS BLOCK DIAGRAM (2-2)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 18 OF 303	

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DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 19 OF 303	

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DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 20 OF 303	

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DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 21 OF 303	

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DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 22 OF 303	

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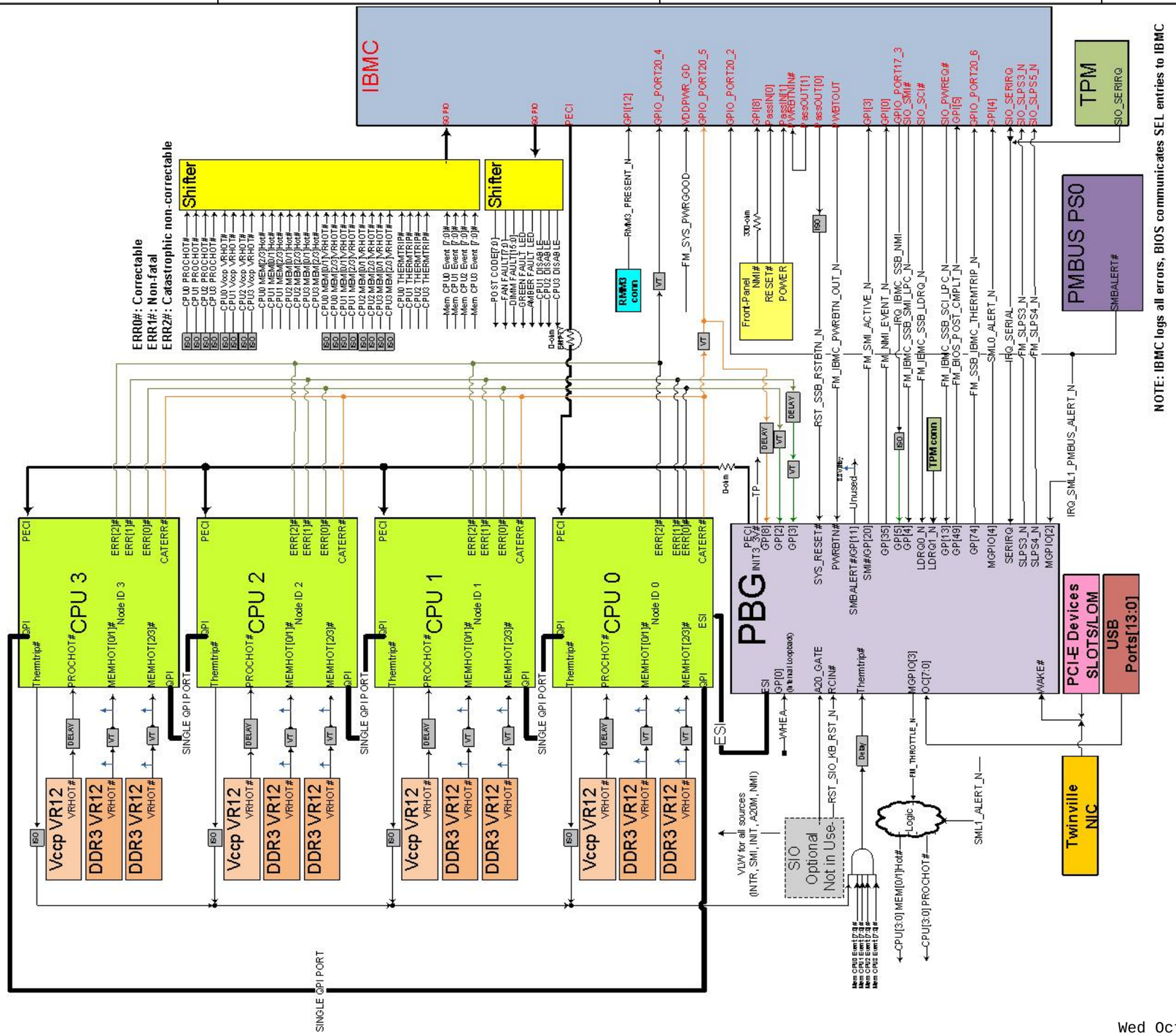

INTERRUPTS DIAGRAM

Wed Oct 27 14:53:04 2010

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 23 OF 303	

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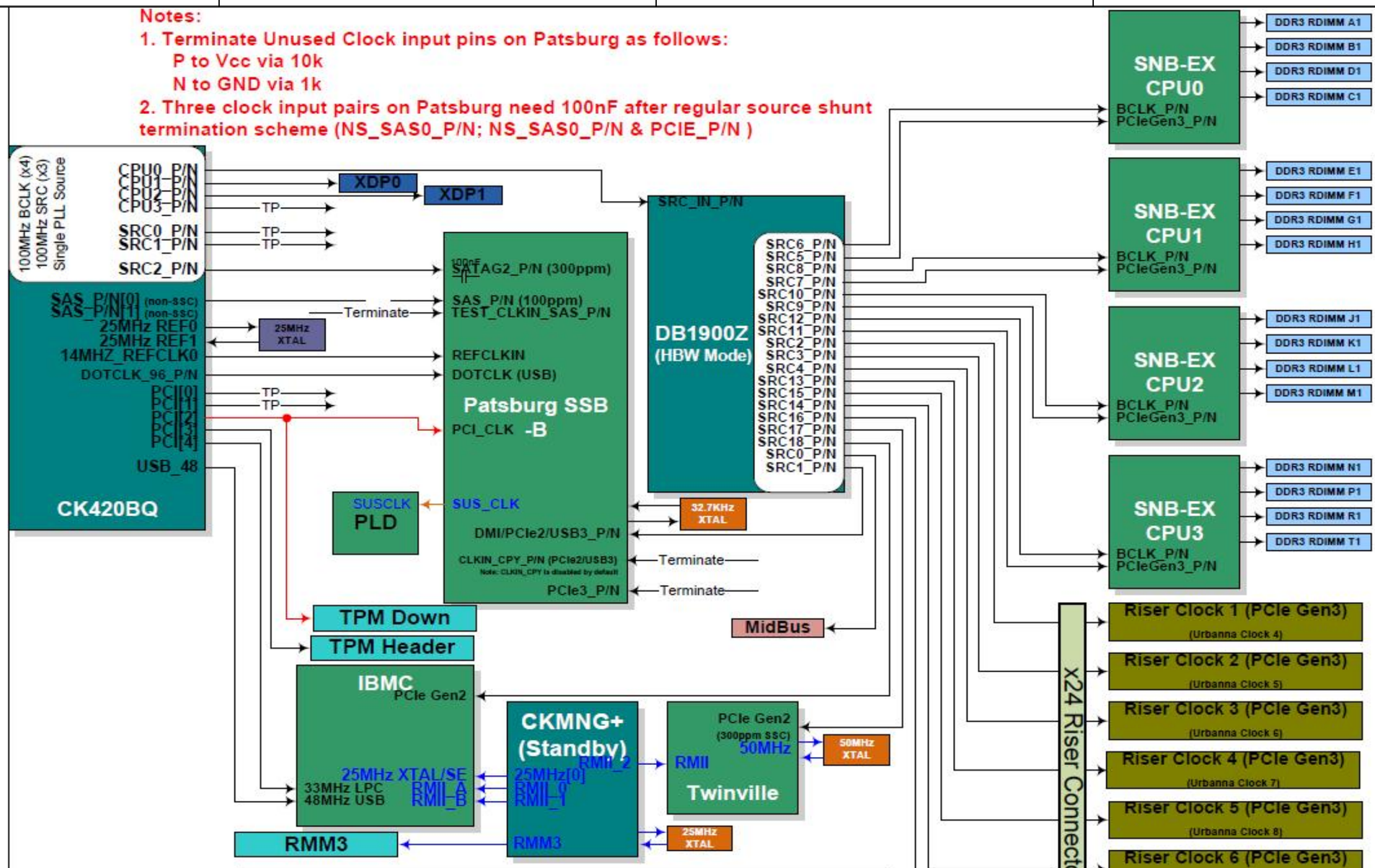
Notes:

1. Terminate Unused Clock input pins on Patsburg as follows:
   P to Vcc via 10k
   N to GND via 1k
2. Three clock input pairs on Patsburg need 100nF after regular source shunt termination scheme (NS_SAS0_P/N; NS_SAS0_P/N & PCIE_P/N)



	Urbanna Schematic Riser Conn						
Card	Clock Slot4	Clock Slot5	Clock Slot6	Clock Slot7	Clock Slot8	Clock Slot9	Clock Slot10
2U PCI-X	Bridge 1	Bridge 2	FH Slot3 x8	LP Slot1 x8			LP Slot2 x8
Butterfly	FH Slot3 x8	Switch 1	FH Slot2 x8	FH Slot1 x16	Switch 2	LP Slot1 x8	LP Slot2 x8
2U PCIe	Slot1 x8		Slot2 x8		Slot3 x8		
1U PCIe	Slot 1 x16						

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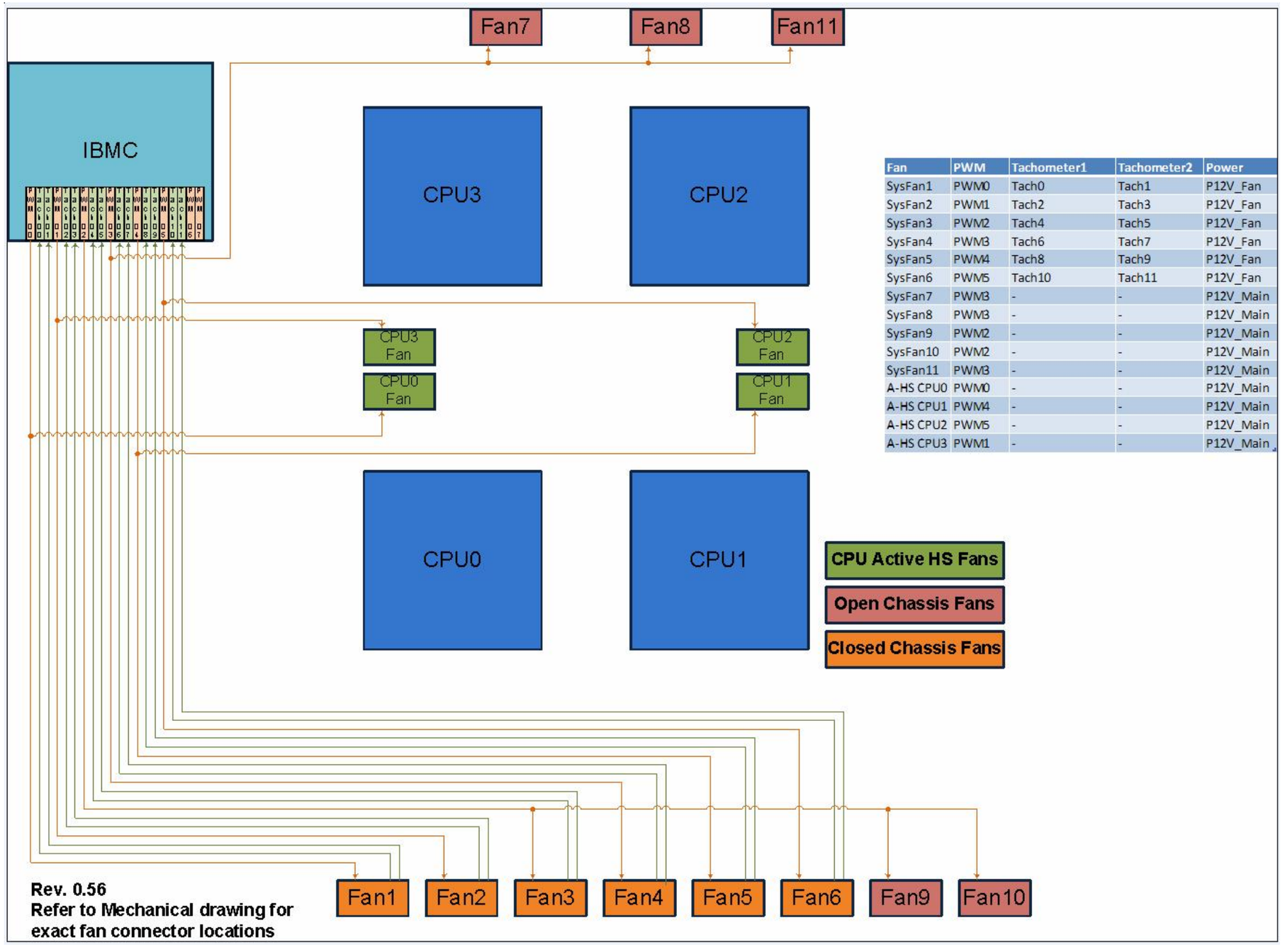
CLOCK DIAGRAM

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 24 OF 303	

INTEL CONFIDENTIAL



Fan	PWM	Tachometer1	Tachometer2	Power
SysFan1	PWM0	Tach0	Tach1	P12V_Fan
SysFan2	PWM1	Tach2	Tach3	P12V_Fan
SysFan3	PWM2	Tach4	Tach5	P12V_Fan
SysFan4	PWM3	Tach6	Tach7	P12V_Fan
SysFan5	PWM4	Tach8	Tach9	P12V_Fan
SysFan6	PWM5	Tach10	Tach11	P12V_Fan
SysFan7	PWM3	-	-	P12V_Main
SysFan8	PWM3	-	-	P12V_Main
SysFan9	PWM2	-	-	P12V_Main
SysFan10	PWM2	-	-	P12V_Main
SysFan11	PWM3	-	-	P12V_Main
A-HS CPU0	PWM0	-	-	P12V_Main
A-HS CPU1	PWM4	-	-	P12V_Main
A-HS CPU2	PWM5	-	-	P12V_Main
A-HS CPU3	PWM1	-	-	P12V_Main

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FAN CONNECTIVITY DIAGRAM

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 25 OF 303	

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TEMP1 TMP75 0X9E
TEMP2 TMP75 0X94
TEMP3 ADM1032 0X4C
TEMP4 TMP75 0X98
TEMP5 TMP75 0X96

ISO P3V3_STBY – P3V3
BB FRU AT24C64 0XA8

ISO P3V3_STBY – P3V3
FP TEMP TMP75 0X9A
FP FRU AT24C64 0XAE
Reset Button
Power Button
Front Panel

Intruder Switch

PSU
FRU: 0XA0
Dev. 0XB0

BMC-ME Connector

Patsburg B
PCH 0X88
ME 0X *TBD*

CK-MNG 0XD0

ISO P3V3_STBY – P3V3

0Ω

CK420BQ 0XD2
XDP0 (CPU JTAG) N/A
DB1900Z 0XD8
XDP2 (PBG) N/A
TPM Header

Voltage Sensors

00 – P12V	08 – P1V5_DDR3_CPU0
01 – P5V	09 – P1V5_DDR3_CPU1
02 – P3V3	10 – P1V5_DDR3_CPU2
03 – P5V_STBY	11 – P1V5_DDR3_CPU3
04 – P3V3_STBY	12 – P1V8_STBY_IBMC
05 – PV_VCCP_CPU2	13 – P1V1_STBY_PBG
06 – PV_VCCP_CPU0	14 – PV_VCCP_CPU3
07 – PV_VCCP_CPU1	15 – P3V_VBAT

GPIO Sensors

08 – FP_NMI_BTN_CO_N
12 – FM_RMM3_PRSNT_N
14 – FM_IBMC_PS_PWROK_LVC3
20_2 – IRQ_SML1_PMBUS_ALERT_N
20_4 – FM_ERR2_LVC3_N
20_5 – IRQ_CPU_CATERR_LVC3_N
20_6 – FM_SSB_IBMC_THERMTRIP_N
20_7 – FM_IBMC_DEBUG_CARD_PRES_N

Fans

Closed Chassis
System Fans
SysFan1~SysFan6
PWM0~PWM5
TACH0~TACH11

Open Chassis
System Fans
SysFan7~SysFan11
PWM2 & PWM3

CPU A-HS Fans
FanCPU0~FanCPU3
PWM0 & PWM1
PWM4 & PWM5

Not Used: PWM6~PWM7 & TACH12~TACH15

NOTE: signals PWM0 to PWM5 are shared by open chassis and closed chassis fans.

SGPO Status & Effectors

00 – LED_POSTCODE_0
01 – LED_POSTCODE_1
02 – LED_POSTCODE_2
03 – LED_POSTCODE_3
04 – LED_POSTCODE_4
05 – LED_POSTCODE_5
06 – LED_POSTCODE_6
07 – LED_POSTCODE_7
08 – FP_LED_STATUS_GREEN_N
09 – FP_LED_STATUS_AMBER_N
10 – N/A
11 – FM_CPU1_DISABLE_N
12 – LED_FAN_FAULT0
13 – LED_FAN_FAULT1
14 – LED_FAN_FAULT2
15 – LED_FAN_FAULT3
16 – LED_FAN_FAULT4
17 – LED_FAN_FAULT5
18 – N/A
19 – N/A
20 – LED_SKT0_DIMM_A1_FAULT_R
21 – LED_SKT0_DIMM_B1_FAULT_R
22 – LED_SKT0_DIMM_C1_FAULT_R
23 – LED_SKT0_DIMM_D1_FAULT_R
24 – LED_SKT1_DIMM_E1_FAULT_R
25 – LED_SKT1_DIMM_F1_FAULT_R
26 – LED_SKT1_DIMM_G1_FAULT_R
27 – LED_SKT1_DIMM_H1_FAULT_R
28 – LED_SKT2_DIMM_J1_FAULT_R
29 – LED_SKT2_DIMM_K1_FAULT_R
30 – LED_SKT2_DIMM_L1_FAULT_R
31 – LED_SKT2_DIMM_M1_FAULT_R
32 – LED_SKT3_DIMM_N1_FAULT_R
33 – LED_SKT3_DIMM_P1_FAULT_R
34 – LED_SKT3_DIMM_R1_FAULT_R
35 – LED_SKT0_DIMM_T1_FAULT_R
36 – FM_CPU2_DISABLE_N
37 – FM_CPU3_DISABLE_N
38 – N/A
39 – N/A

SGPI Sensors

00 – FM_CPU0_SKTOCC_CO_N
01 – FM_CPU1_SKTOCC_CO_N
02 – FM_CPU0_THERMTRIP_LVC3_N
03 – FM_CPU1_THERMTRIP_LVC3_N
04 – IRQ_VCCP_CPU0_VRHOT_N
05 – IRQ_VCCP_CPU1_VRHOT_N
06 & 07 – IRQ_CPU0_MEM_VRHOT_N
08 & 09 – IRQ_CPU1_MEM_VRHOT_N
10 – FM_CPU0_PROCHOT_LVC3_N
11 – FM_CPU1_PROCHOT_LVC3_N
12 – FM_CPU0_MEMAB_HOT_LVC3_N
13 – FM_CPU0_MEMCD_HOT_LVC3_N
14 – FM_CPU1_MEMEF_HOT_LVC3_N
15 – FM_CPU1_MEMGH_HOT_LVC3_N
16 – FM_SYS_FAN_PRSNT_0_N
17 – FM_SYS_FAN_PRSNT_1_N
18 – FM_SYS_FAN_PRSNT_2_N
19 – FM_SYS_FAN_PRSNT_3_N
20 – FM_SYS_FAN_PRSNT_4_N
21 – FM_SYS_FAN_PRSNT_5_N
22 – N/A
23 – N/A
24 – FM_SKT0_DIMM_A1_EVENT_N
25 – FM_SKT0_DIMM_B1_EVENT_N
26 – FM_SKT0_DIMM_C1_EVENT_N
27 – FM_SKT0_DIMM_D1_EVENT_N
28 – FM_SKT1_DIMM_E1_EVENT_N
29 – FM_SKT1_DIMM_F1_EVENT_N
30 – FM_SKT1_DIMM_G1_EVENT_N
31 – FM_SKT1_DIMM_H1_EVENT_N
32 – FM_SKT2_DIMM_J1_EVENT_N
33 – FM_SKT2_DIMM_K1_EVENT_N
34 – FM_SKT2_DIMM_L1_EVENT_N
35 – FM_SKT2_DIMM_M1_EVENT_N
36 – FM_SKT3_DIMM_N1_EVENT_N
37 – FM_SKT3_DIMM_P1_EVENT_N
38 – FM_SKT3_DIMM_R1_EVENT_N
39 – FM_SKT3_DIMM_T1_EVENT_N
40 – FM_CPU0_IVT_ID_LVC3_N
41 – FM_CPU1_IVT_ID_LVC3_N
42 – FM_CPU2_IVT_ID_LVC3_N
43 – FM_CPU3_IVT_ID_LVC3_N
44 – FM_CPU2_SKTOCC_CO_N
45 – FM_CPU3_SKTOCC_CO_N
46 – FM_CPU2_THERMTRIP_LVC3_N
47 – FM_CPU3_THERMTRIP_LVC3_N
48 – IRQ_VCCP_CPU2_VRHOT_N
49 – IRQ_VCCP_CPU3_VRHOT_N
50 & 51 – IRQ_CPU2_MEM_VRHOT_N
52 & 53 – IRQ_CPU3_MEM_VRHOT_N
54 – FM_CPU2_PROCHOT_LVC3_N
55 – FM_CPU3_PROCHOT_LVC3_N
56 – FM_CPU2_MEMJK_HOT_LVC3_N
57 – FM_CPU2_MEMLM_HOT_LVC3_N
58 – FM_CPU3_MEMNP_HOT_LVC3_N
59 – FM_CPU3_MEMRT_HOT_LVC3_N
60 – N/A
61 – N/A
62 – N/A
63 – N/A

SMBus[3] SMBus[7] SMBus[1] SIO_PWRBTOUT_N PASSTRHUOUT0 ADC 15 Channels + Battery Monitor PWM & TACH Signals SIO_PWRBTIN_N PASSTRHUOUT1 GPIO PASSTRHUIN1 PASSTRHUIND CHASI_N SGPIO SMBus[0]

iBMC

ISO P3V3_STBY – P5V_STBY
CPUSV Debug Header
ISO P3V3_STBY – P5V_STBY
IPMB Connector

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SENSORS & FAN DIAGRAM

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 26 OF 303	

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DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 27 OF 303	

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ROOM CK420BQ

U3F1

932SQ420

E65470-001

48M_2X_100M_133M_N

SMBUS ADDRESS = 0XD2

CAD NOTE: AVOID STUBS ON 0-OHM

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CK420BQ (1 OF 2)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 28 OF 303	

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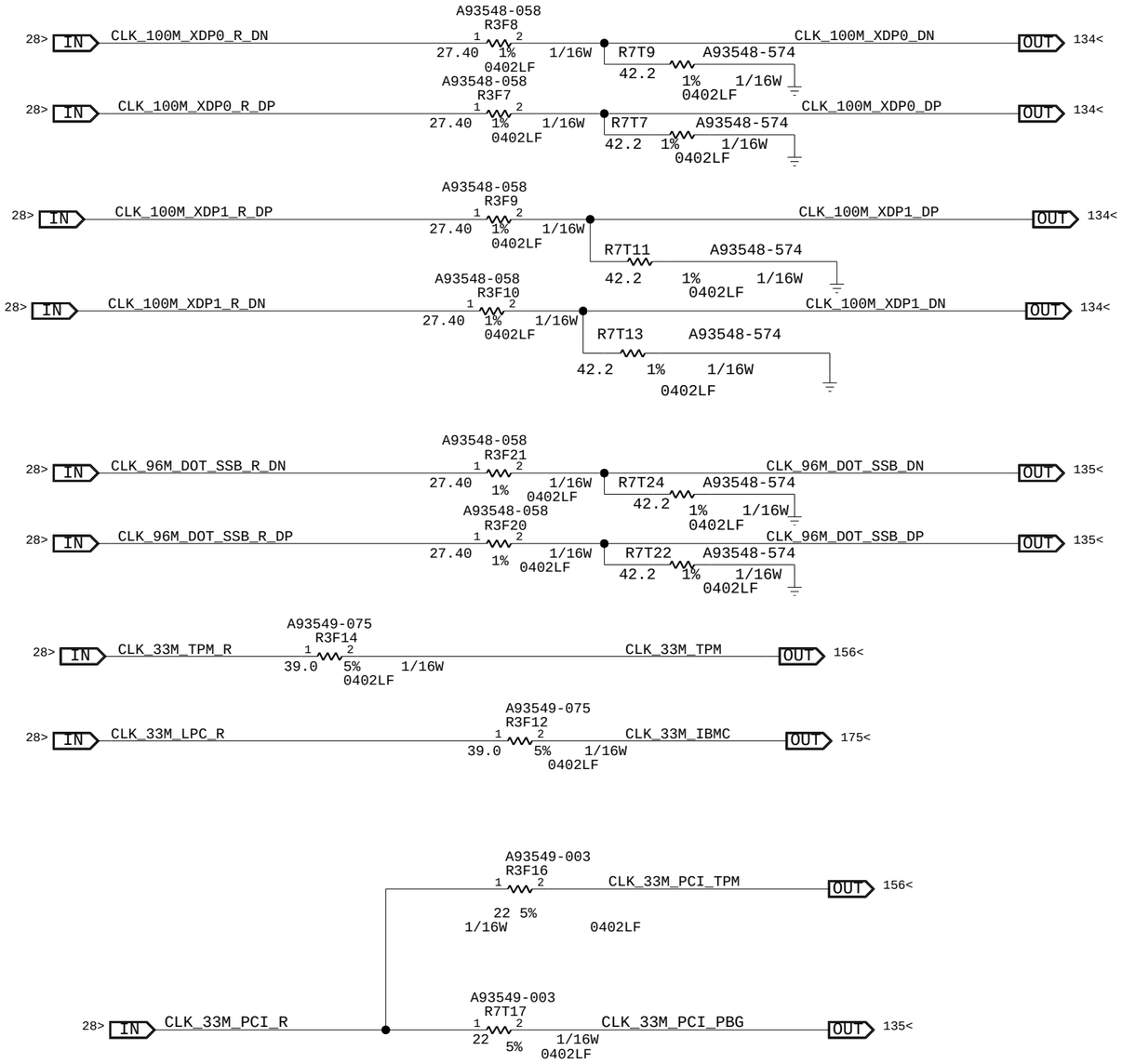

ROOM CK420BQ

CK420BQ (2 OF 2)

Wed Oct 27 15:21:19 2010

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 29 OF 303	

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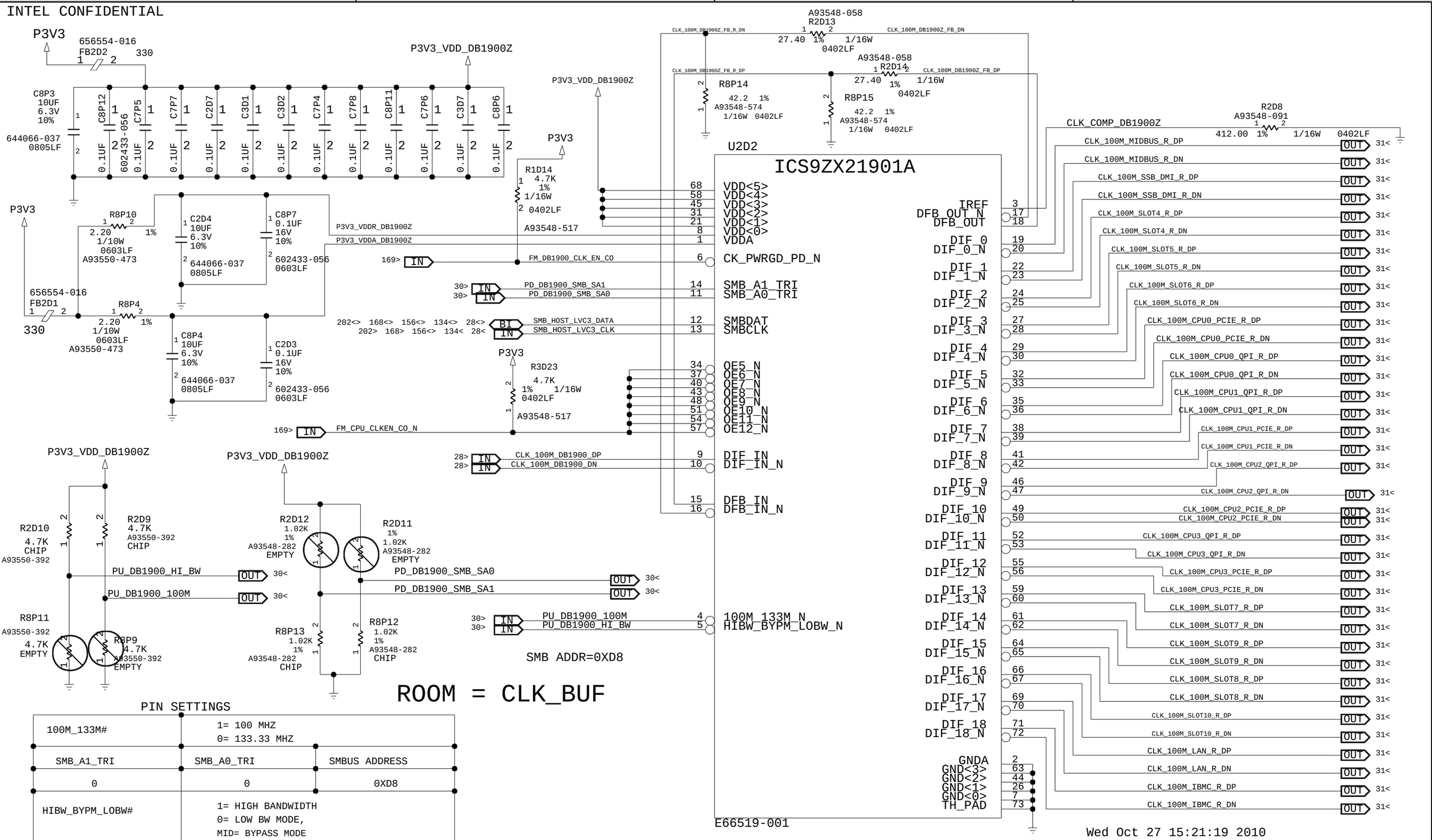

DB1900Z (1 OF 2)

Wed Oct 27 15:21:19 2010

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 30 OF 303	

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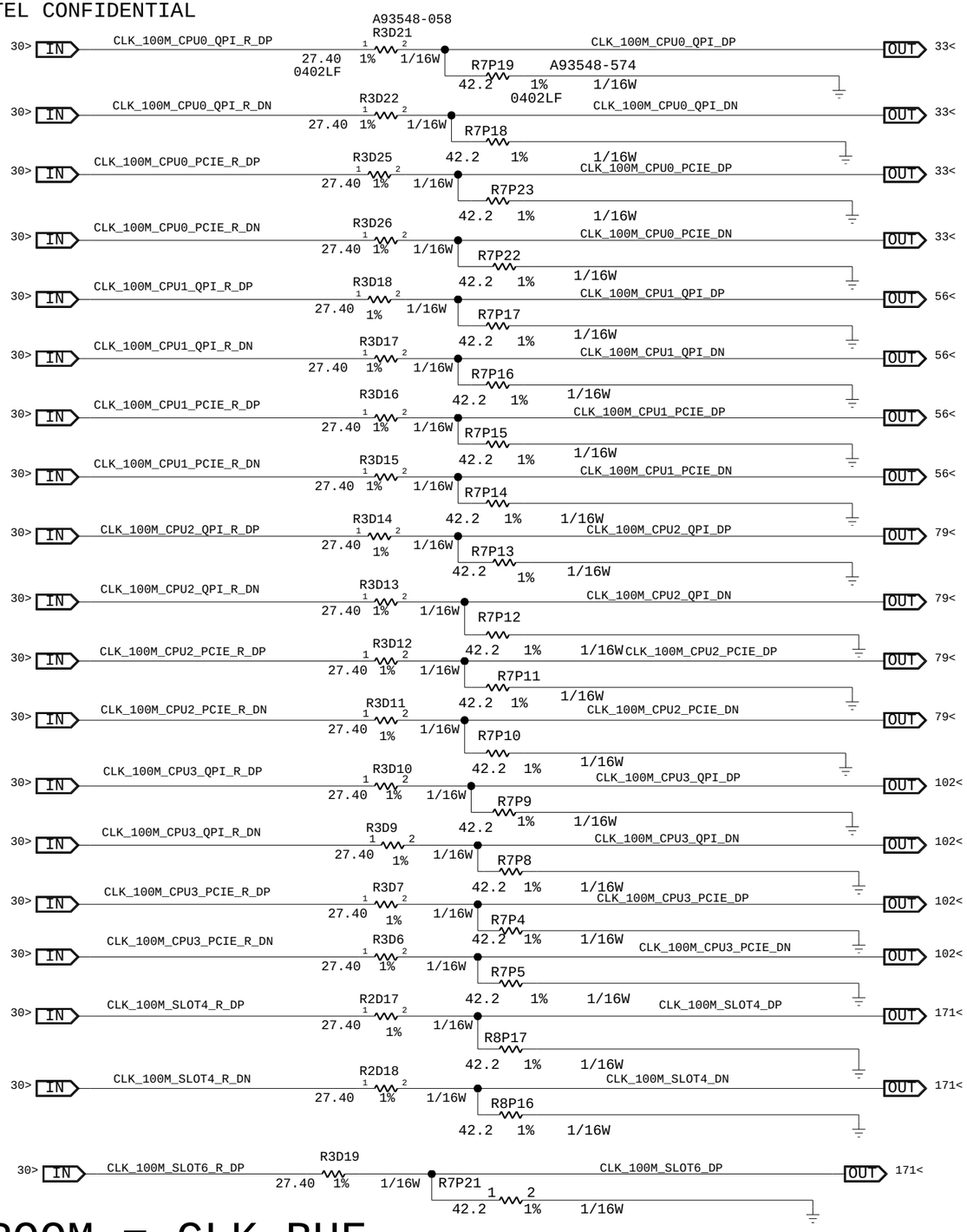

ROOM = CLK_BUF
DB1900Z (2 OF 2)

Wed Oct 27 15:21:20 2010

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 31 OF 303	

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CAD NOTE:
10UF CAP AND 0.1UF CAPS SHOULD BE SEPARATED BY 250MILS
PLACE 10UF CLOSE TO FERRITE BEAD
PLACE ALL 0.1UF NEAR CHIP PIN
CURRENT SHOULD FLOW THROUGH 10UF CAP PAD

P3V3_STBY
656554-043
FB1C1
600 SMLF
C1C2 1.0UF 6.3V 10% A36096-027 0402LF
C1C5 10UF 6.3V 20% 644066-038 0805LF
C1C3 0.1UF 16V 10% A36096-030 0402LF
C9N3 0.1UF 16V 10% A36096-030 0402LF
P3V3_STBY_MNG
C9N2 0.1UF 16V 10% A36096-030 0402LF

CAD NOTE:
PLACE 0.1UF NEAR CHIP PIN

P3V3_STBY_MNG
A93550-473 R1C9 2.20 1% 1/10W 0603LF
P3V3_STBY_MNG_IOH
C9N6 0.01UF 25V 10% A36096-045 0402LF
C9N5 1.0UF 6.3V 10% A36096-027 0402LF

P3V3_STBY_MNG
A93550-473 R1C5 2.20 1% 1/10W 0603LF
P3V3_STBY_MNG_RMII
C9N1 0.01UF 25V 10% A36096-045 0402LF
C9N4 1.0UF 6.3V 10% A36096-027 0402LF

P3V3_STBY_MNG_RMII
P3V3_STBY_MNG
P3V3_STBY_MNG_IOH
U1C1

CK_MNG_133

34	VDD_50<1>	32P768KHZ	13	CLK_33K_SUSCLK_PLD	OUT 169< 170<
26	VDD_50<0>				
2	VDD_96	25MHZ<1>	17	TP_CKMNG_25M1	
9	VDD_133	25MHZ<0>	16	CLK_25M_IBMC_XTAL_SE_R	
23	VDD_33				
15	VDD_REF	50MHZ<7>	24	CLK_50M_TWN_R	
12	VDD_32K	50MHZ<6>	25	TP_CKMNG_50M_6	
		50MHZ<5>	28	CLK_50M_IBMCA_R	
38	SCL	50MHZ<4>	29	CLK_50M_IBMCB_R	
39	SDA	50MHZ<3>	32	TP_CKMNG_50M_3	
		50MHZ<2>	33	TP_CKMNG_50M_2	
30	OE_50B	50MHZ<1>	36	CLK_50M_RMM3_R	
31	OE_50A	50MHZ<0>	37	TP_CKMNG_50M_0	
5	OE_96	DOT_96_P	3	TP_CKMNG_DOT_96M_P	
6	OE_133	DOT_96_N	4	TP_CKMNG_DOT_96M_N	
19	XTAL_IN	CPU_133_P	7	TP_CKMNG_133M_R_DP	
		CPU_133_N	8	TP_CKMNG_133M_R_DN	
		IREF	11	CLK_COMP_CKMNG	
20	XTAL_OUT	GND_50<1>	35		
40	VTT_PWRGD_PWRDWN_N	GND_50<0>	27		
22	33P33MHZ_SMBADR	GND_133	10		
		GND<2>	41		
		GND<1>	21		
		GND<0>	1		
		VSSREF	18		
		GND_32K	14		

D24031-003

P3V3_STBY_MNG
A93548-517 R1C4 4.7K 1% 1/16W 0402LF
202< 190> 188< 177> 139<> IN SMB_HOST_STBY_LVC3_CLK
190<> 188<> 177<> 139<> 202<> BI SMB_HOST_STBY_LVC3_DATA
P3V3_STBY_MNG_R
C1C4 1.0UF 6.3V 10% A36096-027 0402LF

XTAL_CKMNG_IN
CAD NOTE:
PLACE CAPS CLOSE TO CK-MNG PINS
A93545-011 Y1C1 25MHZ
C8M56 27.0PF 50V 5% A36095-038 0402LF
C8M55 27.0PF 50V 5% A36095-038 0402LF
XTAL_CKMNG_OUT
TP_CKMNG_33P_33M_SMBADR
279> 169< IN PWRGD_VR_P3V3_STBY_CO
PD_CKMNG_OE_N
R9N3 1K 1% 1/16W A93548-023 0402LF

R9N2 475 1% 1/16W A93548-059 0402LF

A93548-503 R1C6 33 1% 1/16W CLK_25M_IBMC_XTAL_SE OUT 177<
A93549-003 R1C3 22 5% 1/16W 0402LF CLK_50M_TWN OUT 219< 224<
R1C2 A93549-003 22 5% 1/16W 0402LF CLK_50M_IBMCA OUT 175<
A93549-003 R1C1 22 5% 1/16W 0402LF CLK_50M_IBMCB OUT 176<
A93549-003 R1C7 22 5% 1/16W 0402LF CLK_50M_RMM3 OUT 197<

SMBUS ADDRESS =0XD0

SMBUS ADDRESS SELECTION

SMBADR		
SMBADR = 0	DEFAULT	SMBADR = 1
D0/D1		C0/C1

ROOM = CK-MNG

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CK-MNG

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 32 OF 303	

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CAD NOTE FROM ROMLEY PDG NOTE FOR PE_RBIAS:
THE ROUTING DISTANCE TO THE RESISTOR
SHOULD BE AS CLOSE AS POSSIBLE
(NO LONGER THAN 1.0" AND AT LEAST 15 MILS WIDE)
KEEP THE TRACES SEPARETED 30 MILS FROM ALL OTHERS.

C5T5 0.01UF 25V 10% A36096-045 0402LF

R5U4 49.9 1% 1/16W A93548-045 0402LF

DE NOTE: PE_RBIAS_SENSE NET MUST BE SHORTED
AT THE TOP OF PE_RBIAS 50OHM RESISTOR.
CONNECT SENSE AS CLOSE AS POSIBLE TO OTHER END OF RES

NET NAMES REFLECT ON-DIE TERMINATION AT CPU

LVCO1V05:CMOS INPUT, OD OUTPUT
LVCO1V05:CMOS INPUT, OD OUTPUT
LVC1V5:CMOS 1.5V INPUT

LVC1V5:CMOS 1.5V OUTPUT
LVC1V5:CMOS 1.5V OUTPUT

U5H1
IC

SANDYBRIDGE_EP_EXT_D

		A_CPU0_PE_VREF_CAP	AJ43
			AF52
		A_CPU0_PE_RBIAS	AH52
31>	IN	CLK_100M_CPU0_PCIE_DP	AW45
31>	IN	CLK_100M_CPU0_PCIE_DN	BA45
		TP_SMB_CPU0_PE_HP_1V05_SCL	BH48
		TP_SMB_CPU0_PE_HP_1V05_SDA	BF48
		NC_CPU0_RSVD<12>	D56
		NC_CPU0_RSVD<8>	F56
		NC_CPU0_RSVD<10>	E57
		NC_CPU0_RSVD<7>	F58
		NC_CPU0_RSVD<5>	H58
		NC_CPU0_RSVD<63>	AR55
		NC_CPU0_RSVD<62>	AU55
54>	IN	PU_CPU0_DMIGEN2EN	V52
54>	IN	PD_CPU0_FRMAGENT	AT50
54>	IN	PD_CPU0_BMCINIT	AL47
54>	IN	PD_CPU0_LTEN	AK52
54>	IN	PU_CPU0_BIST_EN	AT48
125< 54>	OUT	FM_CPU0_IVT_ID_LVC1_N	AH42
123<>	BI	FM_CPU0_MEMCD_MEMHOT_LVC1_N	E13
123<>	BI	FM_CPU0_MEMAB_MEMHOT_LVC1_N	CB22
76>	IN	PWRGD_CPU0_DRAMPWRGD_LVC1V5	L15
			CW17
50<	OUT	P1V5_DDR3_CD_VREFDQTX	P42
50<	OUT	P1V5_DDR3_AB_VREFDQTX	CN41
50>	IN	P1V5_DDR3_CD_VREFDQRX	J1
50>	IN	P1V5_DDR3_AB_VREFDQRX	BY16
198<	BI	SMB_DDR_CD_LVC1_SDA	R43
198<	BI	SMB_DDR_AB_LVC1_SDA	CW41
198<>	OUT	SMB_DDR_CD_LVC1_SCL	U43
198<>	OUT	SMB_DDR_AB_LVC1_SCL	CY42
49< 48<	OUT	M_CD_RESET_LVC1V5_N	AE27
47< 46<	OUT	M_AB_RESET_LVC1V5_N	CB18
207< 170< 169< 129< 54>	OUT	FM_CPU0_SKTOCC_CO_N	BU49
		NC_CPU0_RSVD<23>	CY56
99<	BI	IRQ_CPU0_CATERR_LVC1_N	CC51
54>	IN	PD_CPU0_SAFE_MODE	DA55
134> 133< 79<	IN	JTAG_CPU_G_TDI	BW43
134> 133> 56<	IN	JTAG_CPU_LVC1_TCK0	BY44
134> 133> 102< 79< 56<	IN	JTAG_CPU_G_TMS	BV44
134> 133> 102< 79< 56<	IN	JTAG_CPU_LVC1_TRST_N	CT54

PE_VREF_CAP		QPI_VREF_CAP	CU51
PE_RBIAS_SENSE		QPI_RBIAS_SENSE	CC53
PE_RBIAS		QPI_RBIAS	CE53
BCLK1_DP		BCLK0_DP	CN43
BCLK1_DN		BCLK0_DN	CM44
PEHPSCL		RSVD<31>	CA45
PEHPSDA		RSVD<32>	BY46
RSVD<12>		RSVD<18>	DD54
RSVD<8>		RSVD<19>	DC55
RSVD<10>		RSVD<17>	DE55
RSVD<7>		RSVD<21>	DA57
RSVD<5>		RSVD<22>	CY58
RSVD<63>		RSVD<40>	BM46
RSVD<62>		RSVD<37>	BP46
TXT_PLTEN		RSVD<24>	CY48
FRMAGENT		RSVD<25>	CY46
BMCINIT		THERMTRIP_N	BL47
TXT_AGENT		PROCHOT_N	BD52
BIST_ENABLE		TEST4	BA55
		PRDY_N	R53
IVT_ID_N		PREQ_N	U53
MEM_HOT_C23_N			
MEM_HOT_C01_N		SOCKET_ID<1>	BC49
DRAM_PWR_OK_C23		SOCKET_ID<0>	CY52
DRAM_PWR_OK_C01			
DDR_VREFDQTX_C23			
DDR_VREFDQTX_C01			
DDR_VREFDQRX_C23			
DDR_VREFDQRX_C01		PECI	BJ47
DDR_SDA_C23			
DDR_SDA_C01		SVIDCLK	CB44
DDR_SCL_C23		SVIDDATA	BR45
DDR_SCL_C01		SVIDALERT_N	CR43
DDR_RESET_C23_N			
DDR_RESET_C01_N		PMSYNC	K52
		PWRGOOD	BJ53
SKTOCC_N		EAR_N	CH56
		RESET_N	CK44
RSVD<23>			
CAT_ERR_N			
SAFE_MODE_BOOT			
TDI		TDO	CA43
TCK			
TMS			
TRST_N			

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E64556-001

CAD NOTE FROM ROMLEY PDG NOTE FOR QPI_RBIAS:
THE ROUTING DISTANCE TO THE RESISTOR
SHOULD BE AS CLOSE AS POSSIBLE
(POSSIBLY NO LONGER THAN 1.0" AND AT LEAST 10 MILS WIDE)

CU51	A_CPU0_QPI_VREF_CAP		
CC53			
CE53	A_CPU0_QPI_RBIAS		
CN43	CLK_100M_CPU0_QPI_DP	IN 31>	
CM44	CLK_100M_CPU0_QPI_DN	IN 31>	
CA45	NC_CPU0_RSVD<31>		
BY46	NC_CPU0_RSVD<32>		
DD54	NC_CPU0_RSVD<18>		
DC55	NC_CPU0_RSVD<19>		
DE55	NC_CPU0_RSVD<17>		
DA57	NC_CPU0_RSVD<21>		
CY58	NC_CPU0_RSVD<22>		
BM46	NC_CPU0_RSVD<40>		
BP46	NC_CPU0_RSVD<37>		
CY48	NC_CPU0_RSVD<24>		
CY46	NC_CPU0_RSVD<25>		
BL47	FM_CPU0_THERMTRIP_LVC1_N	OUT 100<	LVC1V05: PUSH-PULL OUTPUT
BD52	FM_CPU0_PROCHOT_LVC1_N	BI 122<>	LVCO1V05:CMOS INPUT, OD OUTPUT
BA55	PD_CPU0_TEST<4>		
R53	XDP_CPU0_PRDY_N	OUT 134<>	
U53	XDP_CPU0_PREQ_N	IN 134<>	
BC49	FM_CPU0_SOCKET_ID1_LVC1		
CY52	FM_CPU0_SOCKET_ID0_LVC1		
BJ47	PECI_CPU_LVC1	BI 56<> 79<> 102<> 196<>	
CB44	SVID_CPU0_CLK_LVC1	OUT 55<	
BR45	SVID_CPU0_DAT_LVC1	BI 55<>	
CR43	SVID_CPU0_ALERT_LVC1_N	IN 55>	
K52	IRQ_PM_SYNC_LVC1	IN 56< 135>	
BJ53	PWRGD_CPU0_PWRGOOD_LVC1	IN 52< 76<> 77> 134<	
CH56	RST_CPU_EAR_LVC1_N	BI 56<> 79<> 102<> 125< 134>	
CK44	RST_CPU0_RESET_LVC1_N	IN 76>	
CA43	JTAG_CPU0_G_TDO	OUT 133<	

NOTE: CONNECT TEST4 TO VSS PER PDG

DE NOTE: SOCKET_ID[1:0] NETS HAVE PD ON DIE

DE NOTE: QPI_RBIAS_SENSE NET MUST BE SHORTED
AT THE TOP OF QPI_RBIAS 50OHM RESISTOR.
CONNECT SENSE AS CLOSE AS POSIBLE TO OTHER END OF RES

R5T12 49.9 1% 1/16W A93548-045 0402LF

C5T4 0.01UF 25V 10% A36096-045 0402LF

*DE NOTE: RESISTOR VALUES COULD BE 240 OHM 5%.
CURRENT ONES 1% USED TO REDUCE BOM.

P1V05_VTT_CPU0

1.05

R5F15 240 1% 1/16W A93548-504 0402

R4T20 240 1% 1/16W A93548-504 0402

CPU	SOCKET_ID[2:0]	PECI ADDRESS
CPU0	000B	0X30

EAR_N SIGNAL HAS A 6K OHM PU ON CPU DIE

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CPU SOCKET 0 (1 OF 13)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 33 OF 303	

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IC

SANDYBRIDGE_EP_EXT_D

46<> BI M_A_DQ<63..0>

63	M_A_DQ<63>	CL41	DDR0_DQ<63>	DDR0_DQS_DP<17>	CD16 M_A_DQS_DP<17> 17
62	M_A_DQ<62>	CJ41	DDR0_DQ<62>	DDR0_DQS_DP<16>	CJ39 M_A_DQS_DP<16> 16
61	M_A_DQ<61>	CL37	DDR0_DQ<61>	DDR0_DQS_DP<15>	CC39 M_A_DQS_DP<15> 15
60	M_A_DQ<60>	CJ37	DDR0_DQ<60>	DDR0_DQS_DP<14>	CK32 M_A_DQS_DP<14> 14
59	M_A_DQ<59>	CK42	DDR0_DQ<59>	DDR0_DQS_DP<13>	CD32 M_A_DQS_DP<13> 13
58	M_A_DQ<58>	CH42	DDR0_DQ<58>	DDR0_DQS_DP<12>	CB10 M_A_DQS_DP<12> 12
57	M_A_DQ<57>	CK38	DDR0_DQ<57>	DDR0_DQS_DP<11>	CJ13 M_A_DQS_DP<11> 11
56	M_A_DQ<56>	CH38	DDR0_DQ<56>	DDR0_DQS_DP<10>	CC5 M_A_DQS_DP<10> 10
55	M_A_DQ<55>	CB42	DDR0_DQ<55>	DDR0_DQS_DP<9>	CE7 M_A_DQS_DP<9> 9
54	M_A_DQ<54>	CC41	DDR0_DQ<54>	DDR0_DQS_DP<8>	CC17 M_A_DQS_DP<8> 8
53	M_A_DQ<53>	CE37	DDR0_DQ<53>	DDR0_DQS_DP<7>	CK40 M_A_DQS_DP<7> 7
52	M_A_DQ<52>	CC37	DDR0_DQ<52>	DDR0_DQS_DP<6>	CD40 M_A_DQS_DP<6> 6
51	M_A_DQ<51>	CD42	DDR0_DQ<51>	DDR0_DQS_DP<5>	CJ33 M_A_DQS_DP<5> 5
50	M_A_DQ<50>	CE41	DDR0_DQ<50>	DDR0_DQS_DP<4>	CC33 M_A_DQS_DP<4> 4
49	M_A_DQ<49>	CD38	DDR0_DQ<49>	DDR0_DQS_DP<3>	CE11 M_A_DQS_DP<3> 3
48	M_A_DQ<48>	CB38	DDR0_DQ<48>	DDR0_DQS_DP<2>	CK14 M_A_DQS_DP<2> 2
47	M_A_DQ<47>	CH34	DDR0_DQ<47>	DDR0_DQS_DP<1>	CF4 M_A_DQS_DP<1> 1
46	M_A_DQ<46>	CK34	DDR0_DQ<46>	DDR0_DQS_DP<0>	CH8 M_A_DQS_DP<0> 0
45	M_A_DQ<45>	CH30	DDR0_DQ<45>		
44	M_A_DQ<44>	CK30	DDR0_DQ<44>	DDR0_DQS_DN<17>	CF16 M_A_DQS_DN<17> 17
43	M_A_DQ<43>	CJ35	DDR0_DQ<43>	DDR0_DQS_DN<16>	CL39 M_A_DQS_DN<16> 16
42	M_A_DQ<42>	CL35	DDR0_DQ<42>	DDR0_DQS_DN<15>	CE39 M_A_DQS_DN<15> 15
41	M_A_DQ<41>	CJ31	DDR0_DQ<41>	DDR0_DQS_DN<14>	CH32 M_A_DQS_DN<14> 14
40	M_A_DQ<40>	CL31	DDR0_DQ<40>	DDR0_DQS_DN<13>	CB32 M_A_DQS_DN<13> 13
39	M_A_DQ<39>	CB34	DDR0_DQ<39>	DDR0_DQS_DN<12>	CC11 M_A_DQS_DN<12> 12
38	M_A_DQ<38>	CD34	DDR0_DQ<38>	DDR0_DQS_DN<11>	CL13 M_A_DQS_DN<11> 11
37	M_A_DQ<37>	CB30	DDR0_DQ<37>	DDR0_DQS_DN<10>	CD4 M_A_DQS_DN<10> 10
36	M_A_DQ<36>	CD30	DDR0_DQ<36>	DDR0_DQS_DN<9>	CF8 M_A_DQS_DN<9> 9
35	M_A_DQ<35>	CC35	DDR0_DQ<35>	DDR0_DQS_DN<8>	CE17 M_A_DQS_DN<8> 8
34	M_A_DQ<34>	CE35	DDR0_DQ<34>	DDR0_DQS_DN<7>	CH40 M_A_DQS_DN<7> 7
33	M_A_DQ<33>	CC31	DDR0_DQ<33>	DDR0_DQS_DN<6>	CB40 M_A_DQS_DN<6> 6
32	M_A_DQ<32>	CE31	DDR0_DQ<32>	DDR0_DQS_DN<5>	CL33 M_A_DQS_DN<5> 5
31	M_A_DQ<31>	CF10	DDR0_DQ<31>	DDR0_DQS_DN<4>	CE33 M_A_DQS_DN<4> 4
30	M_A_DQ<30>	CH10	DDR0_DQ<30>	DDR0_DQS_DN<3>	CD10 M_A_DQS_DN<3> 3
29	M_A_DQ<29>	CA9	DDR0_DQ<29>	DDR0_DQS_DN<2>	CH14 M_A_DQS_DN<2> 2
28	M_A_DQ<28>	BW9	DDR0_DQ<28>	DDR0_DQS_DN<1>	CE3 M_A_DQS_DN<1> 1
27	M_A_DQ<27>	CD12	DDR0_DQ<27>	DDR0_DQS_DN<0>	CG7 M_A_DQS_DN<0> 0
26	M_A_DQ<26>	CB12	DDR0_DQ<26>		
25	M_A_DQ<25>	BY12	DDR0_DQ<25>	DDR0_MA<15>	CN19 M_A_MA<15> 15
24	M_A_DQ<24>	BY10	DDR0_DQ<24>	DDR0_MA<14>	CG19 M_A_MA<14> 14
23	M_A_DQ<23>	CL15	DDR0_DQ<23>	DDR0_MA<13>	CG29 M_A_MA<13> 13
22	M_A_DQ<22>	CJ15	DDR0_DQ<22>	DDR0_MA<12>	CK20 M_A_MA<12> 12
21	M_A_DQ<21>	CL11	DDR0_DQ<21>	DDR0_MA<11>	CL21 M_A_MA<11> 11
20	M_A_DQ<20>	CG13	DDR0_DQ<20>	DDR0_MA<10>	CK26 M_A_MA<10> 10
19	M_A_DQ<19>	CM16	DDR0_DQ<19>	DDR0_MA<9>	CN21 M_A_MA<9> 9
18	M_A_DQ<18>	CK16	DDR0_DQ<18>	DDR0_MA<8>	CK22 M_A_MA<8> 8
17	M_A_DQ<17>	CM12	DDR0_DQ<17>	DDR0_MA<7>	CM22 M_A_MA<7> 7
16	M_A_DQ<16>	CK12	DDR0_DQ<16>	DDR0_MA<6>	CN23 M_A_MA<6> 6
15	M_A_DQ<15>	CG5	DDR0_DQ<15>	DDR0_MA<5>	CL23 M_A_MA<5> 5
14	M_A_DQ<14>	CG3	DDR0_DQ<14>	DDR0_MA<4>	CM24 M_A_MA<4> 4
13	M_A_DQ<13>	CA3	DDR0_DQ<13>	DDR0_MA<3>	CK24 M_A_MA<3> 3
12	M_A_DQ<12>	CA1	DDR0_DQ<12>	DDR0_MA<2>	CG25 M_A_MA<2> 2
11	M_A_DQ<11>	CJ5	DDR0_DQ<11>	DDR0_MA<1>	CR25 M_A_MA<1> 1
10	M_A_DQ<10>	CH4	DDR0_DQ<10>	DDR0_MA<0>	CL25 M_A_MA<0> 0
9	M_A_DQ<9>	CB4	DDR0_DQ<9>		
8	M_A_DQ<8>	CB2	DDR0_DQ<8>	DDR0_ECC<7>	CK18 M_A_ECC<7> 7
7	M_A_DQ<7>	CL7	DDR0_DQ<7>	DDR0_ECC<6>	CG17 M_A_ECC<6> 6
6	M_A_DQ<6>	CJ7	DDR0_DQ<6>	DDR0_ECC<5>	CD14 M_A_ECC<5> 5
5	M_A_DQ<5>	CA7	DDR0_DQ<5>	DDR0_ECC<4>	CB14 M_A_ECC<4> 4
4	M_A_DQ<4>	BY6	DDR0_DQ<4>	DDR0_ECC<3>	CF18 M_A_ECC<3> 3
3	M_A_DQ<3>	CL9	DDR0_DQ<3>	DDR0_ECC<2>	CH18 M_A_ECC<2> 2
2	M_A_DQ<2>	CK8	DDR0_DQ<2>	DDR0_ECC<1>	CC15 M_A_ECC<1> 1
1	M_A_DQ<1>	CD8	DDR0_DQ<1>	DDR0_ECC<0>	CE15 M_A_ECC<0> 0
0	M_A_DQ<0>	CC7	DDR0_DQ<0>		
	NC_M_A_CS_N<9>	CK28	DDR0_CS_N<9>	DDR0_CKE<5>	CE19 NC_M_A_CKE<5>
	NC_M_A_CS_N<8>	CL27	DDR0_CS_N<8>	DDR0_CKE<4>	CF20 NC_M_A_CKE<4>
	NC_M_A_CS_N<7>	CC25	DDR0_CS_N<7>	DDR0_CKE<3>	CP18 NC_M_A_CKE<3>
	NC_M_A_CS_N<6>	CB26	DDR0_CS_N<6>	DDR0_CKE<2>	CH20 NC_M_A_CKE<2>
	NC_M_A_CS_N<5>	CF26	DDR0_CS_N<5>	DDR0_CKE<1>	CM18 M_A_CKE<1> 1
	NC_M_A_CS_N<4>	CG27	DDR0_CS_N<4>	DDR0_CKE<0>	CL19 M_A_CKE<0> 0
3	M_A_CS_N<3>	CB28	DDR0_CS_N<3>	DDR0_BA<2>	CM20 M_A_BA<2> 2
2	M_A_CS_N<2>	CC23	DDR0_CS_N<2>	DDR0_BA<1>	CN27 M_A_BA<1> 1
1	M_A_CS_N<1>	CH26	DDR0_CS_N<1>	DDR0_BA<0>	CM28 M_A_BA<0> 0
0	M_A_CS_N<0>	CN25	DDR0_CS_N<0>		
	NC_M_A_CK_DP<3>	CH22	DDR0_CLK_DP<3>	DDR0_ODT<5>	CC27 NC_M_A_ODT<5>
	M_A_CK_DP<2>	CG21	DDR0_CLK_DP<2>	DDR0_ODT<4>	CB24 NC_M_A_ODT<4>
	NC_M_A_CK_DP<1>	CG23	DDR0_CLK_DP<1>	DDR0_ODT<3>	CF28 NC_M_A_ODT<3>
	M_A_CK_DP<0>	CH24	DDR0_CLK_DP<0>	DDR0_ODT<2>	CH28 NC_M_A_ODT<2>
	NC_M_A_CK_DN<3>	CF22	DDR0_CLK_DN<3>	DDR0_ODT<1>	CE27 M_A_ODT<1> 1
	M_A_CK_DN<2>	CE21	DDR0_CLK_DN<2>	DDR0_ODT<0>	CE25 M_A_ODT<0> 0
	NC_M_A_CK_DN<1>	CE23	DDR0_CLK_DN<1>	DDR0_WE_N	CN29 M_A_WE_N
	M_A_CK_DN<0>	CF24	DDR0_CLK_DN<0>	DDR0_RAS_N	CE29 M_A_RAS_N
				DDR0_PAR_ERR_N	CC21 M_A_PAR_ERR_N<0>
				DDR0_CAS_N	CL29 M_A_CAS_N
				DDR0_MA_PAR	CM26 M_A_MA_PAR

M_A_DQS_DP<17..0> BI 46<>

M_A_DQS_DN<17..0> BI 46<>

M_A_MA<15..0> OUT 46<

M_A_ECC<7..0> BI 46<>

M_A_CKE<1..0> OUT 46<

M_A_BA<2..0> OUT 46<

M_A_ODT<1..0> OUT 46<

46< OUT M_A_CS_N<3..0>

46< OUT M_A_CK_DP<2>

46< OUT M_A_CK_DP<0>

46< OUT M_A_CK_DN<2>

46< OUT M_A_CK_DN<0>

NC_M_A_CK_DP<1> NC_M_A_CK_DN<3> NC_M_A_CK_DN<1> NC_M_A_CK_DP<3>

DDR0_WE_N OUT 46<
DDR0_RAS_N OUT 46<
DDR0_PAR_ERR_N IN 46>
DDR0_CAS_N OUT 46<
DDR0_MA_PAR OUT 46<

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CPU SOCKET 0 (2 OF 13)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 34 OF 303	

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U5H1 IC

SANDYBRIDGE_EP_EXT_D

47<> BI M_B_DQ<63..0>

63	M_B_DQ<63>	DF40	DDR1_DQ<63>	
62	M_B_DQ<62>	DA39	DDR1_DQ<62>	
61	M_B_DQ<61>	DC37	DDR1_DQ<61>	
60	M_B_DQ<60>	DA37	DDR1_DQ<60>	
59	M_B_DQ<59>	DB40	DDR1_DQ<59>	
58	M_B_DQ<58>	DD40	DDR1_DQ<58>	
57	M_B_DQ<57>	DF38	DDR1_DQ<57>	
56	M_B_DQ<56>	DE37	DDR1_DQ<56>	
55	M_B_DQ<55>	CV40	DDR1_DQ<55>	
54	M_B_DQ<54>	CT40	DDR1_DQ<54>	
53	M_B_DQ<53>	CV36	DDR1_DQ<53>	
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45	M_B_DQ<45>	CY32	DDR1_DQ<45>	
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42	M_B_DQ<42>	DC35	DDR1_DQ<42>	
41	M_B_DQ<41>	DD32	DDR1_DQ<41>	
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21	M_B_DQ<21>	CT6	DDR1_DQ<21>	
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M_B_CK_DP<0>	CY20	DDR1_CLK_DP<0>	
NC_M_B_CK_DN<3>	DA21	DDR1_CLK_DN<3>	
M_B_CK_DN<2>	CY24	DDR1_CLK_DN<2>	
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47< OUT M_B_CK_DP<2>
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DDR1_DQS_DP<13>	CU31	M_B_DQS_DP<13>	13
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DDR1_DQS_DP<11>	CP8	M_B_DQS_DP<11>	11
DDR1_DQS_DP<10>	DD8	M_B_DQS_DP<10>	10
DDR1_DQS_DP<9>	CT2	M_B_DQS_DP<9>	9
DDR1_DQS_DP<8>	DC15	M_B_DQS_DP<8>	8
DDR1_DQS_DP<7>	DC39	M_B_DQS_DP<7>	7
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DDR1_DQS_DP<1>	DE9	M_B_DQS_DP<1>	1
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M_B_DQS_DP<17..0> BI 47<>

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DDR1_DQS_DN<14>	DE33	M_B_DQS_DN<14>	14
DDR1_DQS_DN<13>	CR31	M_B_DQS_DN<13>	13
DDR1_DQS_DN<12>	CP14	M_B_DQS_DN<12>	12
DDR1_DQS_DN<11>	CT8	M_B_DQS_DN<11>	11
DDR1_DQS_DN<10>	DB8	M_B_DQS_DN<10>	10
DDR1_DQS_DN<9>	CR1	M_B_DQS_DN<9>	9
DDR1_DQS_DN<8>	DE15	M_B_DQS_DN<8>	8
DDR1_DQS_DN<7>	DE39	M_B_DQS_DN<7>	7
DDR1_DQS_DN<6>	CR39	M_B_DQS_DN<6>	6
DDR1_DQS_DN<5>	CY34	M_B_DQS_DN<5>	5
DDR1_DQS_DN<4>	CT32	M_B_DQS_DN<4>	4
DDR1_DQS_DN<3>	CR15	M_B_DQS_DN<3>	3
DDR1_DQS_DN<2>	CV8	M_B_DQS_DN<2>	2
DDR1_DQS_DN<1>	DC9	M_B_DQS_DN<1>	1
DDR1_DQS_DN<0>	CT4	M_B_DQS_DN<0>	0

M_B_DQS_DN<17..0> BI 47<>

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DDR1_MA<13>	DB30	M_B_MA<13>	13
DDR1_MA<12>	DC19	M_B_MA<12>	12
DDR1_MA<11>	DE19	M_B_MA<11>	11
DDR1_MA<10>	DF26	M_B_MA<10>	10
DDR1_MA<9>	DA19	M_B_MA<9>	9
DDR1_MA<8>	DB20	M_B_MA<8>	8
DDR1_MA<7>	DF20	M_B_MA<7>	7
DDR1_MA<6>	DE21	M_B_MA<6>	6
DDR1_MA<5>	DF22	M_B_MA<5>	5
DDR1_MA<4>	DB22	M_B_MA<4>	4
DDR1_MA<3>	DA23	M_B_MA<3>	3
DDR1_MA<2>	DF24	M_B_MA<2>	2
DDR1_MA<1>	DE23	M_B_MA<1>	1
DDR1_MA<0>	DC23	M_B_MA<0>	0

M_B_MA<15..0> OUT 47<

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DDR1_ECC<4>	DA13	M_B_ECC<4>	4
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DDR1_ECC<2>	DD16	M_B_ECC<2>	2
DDR1_ECC<1>	DF14	M_B_ECC<1>	1
DDR1_ECC<0>	DE13	M_B_ECC<0>	0

M_B_ECC<7..0> BI 47<>

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DDR1_CKE<2>	CY18	NC_M_B_CKE<2>	
DDR1_CKE<1>	CU19	M_B_CKE<1>	1
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M_B_CKE<1..0> OUT 47<

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M_B_BA<2..0> OUT 47<

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DDR1_ODT<2>	CY26	NC_M_B_ODT<2>	
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M_B_ODT<1..0> OUT 47<

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DDR1_RAS_N	DB28	M_B_RAS_N	OUT 47<
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DDR1_CAS_N	CY30	M_B_CAS_N	OUT 47<
DDR1_MA_PAR	DE25	M_B_MA_PAR	OUT 47<

3/17

E64556-001

CPU SOCKET 0 (3 OF 13)

Wed Oct 27 15:21:20 2010

DEPARTMENT	Intel Corporation	SIZE	CODE / DOCUMENT NUMBER / REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649 / 444359 / 1.0
		SCALE: DO NOT SCALE DRAWING	SHEET 35 OF 303

INTEL CONFIDENTIAL

U5H1 IC

SANDYBRIDGE_EP_EXT_D

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38	M_C_DQ<38>	AB10	DDR2_DQ<38>	DDR2_DQS_DN<11>	T32
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48< OUT

48< OUT

48< OUT

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4	M_C_DQS_DN<4>	
3	M_C_DQS_DN<3>	
2	M_C_DQS_DN<2>	
1	M_C_DQS_DN<1>	
0	M_C_DQS_DN<0>	

M_C_MA<15..0> OUT 48<

15	M_C_MA<15>	
14	M_C_MA<14>	
13	M_C_MA<13>	
12	M_C_MA<12>	
11	M_C_MA<11>	
10	M_C_MA<10>	
9	M_C_MA<9>	
8	M_C_MA<8>	
7	M_C_MA<7>	
6	M_C_MA<6>	
5	M_C_MA<5>	
4	M_C_MA<4>	
3	M_C_MA<3>	
2	M_C_MA<2>	
1	M_C_MA<1>	
0	M_C_MA<0>	

M_C_ECC<7..0> BI 48<>

7	M_C_ECC<7>	
6	M_C_ECC<6>	
5	M_C_ECC<5>	
4	M_C_ECC<4>	
3	M_C_ECC<3>	
2	M_C_ECC<2>	
1	M_C_ECC<1>	
0	M_C_ECC<0>	

M_C_CKE<1..0> OUT 48<

1	M_C_CKE<1>	
0	M_C_CKE<0>	

M_C_BA<2..0> OUT 48<

2	M_C_BA<2>	
1	M_C_BA<1>	
0	M_C_BA<0>	

M_C_ODT<1..0> OUT 48<

1	M_C_ODT<1>	
0	M_C_ODT<0>	

M_C_WE_N		OUT 48<
M_C_RAS_N		OUT 48<
M_C_PAR_ERR_N<0>		IN 48>
M_C_CAS_N		OUT 48<
M_C_MA_PAR		OUT 48<

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E64556-001

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CPU SOCKET 0 (4 OF 13)

DEPARTMENT: DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	SIZE: B / CODE: 34649 / DOCUMENT NUMBER: 444359 / REV: 1.0	SCALE: DO NOT SCALE DRAWING / SHEET 36 OF 303

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U5H1 IC

SANDYBRIDGE_EP_EXT_D

49<> BI M_D_DQ<63..0>

63	M_D_DQ<63>	M2	DDR3_DQ<63>	DDR3_DQS_DP<17>	F28
62	M_D_DQ<62>	L1	DDR3_DQ<62>	DDR3_DQS_DP<16>	J3
61	M_D_DQ<61>	H4	DDR3_DQ<61>	DDR3_DQS_DP<15>	G7
60	M_D_DQ<60>	F4	DDR3_DQ<60>	DDR3_DQS_DP<14>	K12
59	M_D_DQ<59>	P4	DDR3_DQ<59>	DDR3_DQS_DP<13>	E11
58	M_D_DQ<58>	N3	DDR3_DQ<58>	DDR3_DQS_DP<12>	N31
57	M_D_DQ<57>	H2	DDR3_DQ<57>	DDR3_DQS_DP<11>	D34
56	M_D_DQ<56>	G3	DDR3_DQ<56>	DDR3_DQS_DP<10>	M38
55	M_D_DQ<55>	M6	DDR3_DQ<55>	DDR3_DQS_DP<9>	E39
54	M_D_DQ<54>	L7	DDR3_DQ<54>	DDR3_DQS_DP<8>	E27
53	M_D_DQ<53>	D6	DDR3_DQ<53>	DDR3_DQS_DP<7>	M4
52	M_D_DQ<52>	C7	DDR3_DQ<52>	DDR3_DQS_DP<6>	K6
51	M_D_DQ<51>	P6	DDR3_DQ<51>	DDR3_DQS_DP<5>	N11
50	M_D_DQ<50>	N7	DDR3_DQ<50>	DDR3_DQS_DP<4>	D10
49	M_D_DQ<49>	F6	DDR3_DQ<49>	DDR3_DQS_DP<3>	N29
48	M_D_DQ<48>	E7	DDR3_DQ<48>	DDR3_DQS_DP<2>	E33
47	M_D_DQ<47>	M10	DDR3_DQ<47>	DDR3_DQS_DP<1>	J37
46	M_D_DQ<46>	K10	DDR3_DQ<46>	DDR3_DQS_DP<0>	D38
45	M_D_DQ<45>	M14	DDR3_DQ<45>		
44	M_D_DQ<44>	K14	DDR3_DQ<44>	DDR3_DQS_DN<17>	H28
43	M_D_DQ<43>	L9	DDR3_DQ<43>	DDR3_DQS_DN<16>	K4
42	M_D_DQ<42>	J9	DDR3_DQ<42>	DDR3_DQS_DN<15>	H6
41	M_D_DQ<41>	L13	DDR3_DQ<41>	DDR3_DQS_DN<14>	M12
40	M_D_DQ<40>	J13	DDR3_DQ<40>	DDR3_DQS_DN<13>	G11
39	M_D_DQ<39>	A9	DDR3_DQ<39>	DDR3_DQS_DN<12>	M30
38	M_D_DQ<38>	F10	DDR3_DQ<38>	DDR3_DQS_DN<11>	B34
37	M_D_DQ<37>	B12	DDR3_DQ<37>	DDR3_DQS_DN<10>	K38
36	M_D_DQ<36>	F12	DDR3_DQ<36>	DDR3_DQS_DN<9>	G39
35	M_D_DQ<35>	E9	DDR3_DQ<35>	DDR3_DQS_DN<8>	G27
34	M_D_DQ<34>	C9	DDR3_DQ<34>	DDR3_DQS_DN<7>	L3
33	M_D_DQ<33>	A11	DDR3_DQ<33>	DDR3_DQS_DN<6>	J7
32	M_D_DQ<32>	D12	DDR3_DQ<32>	DDR3_DQS_DN<5>	L11
31	M_D_DQ<31>	M26	DDR3_DQ<31>	DDR3_DQS_DN<4>	B10
30	M_D_DQ<30>	N27	DDR3_DQ<30>	DDR3_DQS_DN<3>	P28
29	M_D_DQ<29>	K32	DDR3_DQ<29>	DDR3_DQS_DN<2>	G33
28	M_D_DQ<28>	L33	DDR3_DQ<28>	DDR3_DQS_DN<1>	L37
27	M_D_DQ<27>	L27	DDR3_DQ<27>	DDR3_DQS_DN<0>	B38
26	M_D_DQ<26>	M28	DDR3_DQ<26>		
25	M_D_DQ<25>	L31	DDR3_DQ<25>	DDR3_MA<15>	F24
24	M_D_DQ<24>	M32	DDR3_DQ<24>	DDR3_MA<14>	D24
23	M_D_DQ<23>	B32	DDR3_DQ<23>	DDR3_MA<13>	A13
22	M_D_DQ<22>	A33	DDR3_DQ<22>	DDR3_MA<12>	E23
21	M_D_DQ<21>	C35	DDR3_DQ<21>	DDR3_MA<11>	A23
20	M_D_DQ<20>	E35	DDR3_DQ<20>	DDR3_MA<10>	D18
19	M_D_DQ<19>	F32	DDR3_DQ<19>	DDR3_MA<9>	G23
18	M_D_DQ<18>	D32	DDR3_DQ<18>	DDR3_MA<8>	D22
17	M_D_DQ<17>	F34	DDR3_DQ<17>	DDR3_MA<7>	B22
16	M_D_DQ<16>	A35	DDR3_DQ<16>	DDR3_MA<6>	F22
15	M_D_DQ<15>	H36	DDR3_DQ<15>	DDR3_MA<5>	A21
14	M_D_DQ<14>	K36	DDR3_DQ<14>	DDR3_MA<4>	D20
13	M_D_DQ<13>	K40	DDR3_DQ<13>	DDR3_MA<3>	B20
12	M_D_DQ<12>	M40	DDR3_DQ<12>	DDR3_MA<2>	F20
11	M_D_DQ<11>	J35	DDR3_DQ<11>	DDR3_MA<1>	E21
10	M_D_DQ<10>	L35	DDR3_DQ<10>	DDR3_MA<0>	A19
9	M_D_DQ<9>	L39	DDR3_DQ<9>		
8	M_D_DQ<8>	N39	DDR3_DQ<8>	DDR3_ECC<7>	H26
7	M_D_DQ<7>	A37	DDR3_DQ<7>	DDR3_ECC<6>	F26
6	M_D_DQ<6>	F38	DDR3_DQ<6>	DDR3_ECC<5>	H30
5	M_D_DQ<5>	D40	DDR3_DQ<5>	DDR3_ECC<4>	F30
4	M_D_DQ<4>	F40	DDR3_DQ<4>	DDR3_ECC<3>	C25
3	M_D_DQ<3>	E37	DDR3_DQ<3>	DDR3_ECC<2>	E25
2	M_D_DQ<2>	C37	DDR3_DQ<2>	DDR3_ECC<1>	J29
1	M_D_DQ<1>	A39	DDR3_DQ<1>	DDR3_ECC<0>	G29
0	M_D_DQ<0>	B40	DDR3_DQ<0>		
	NC_M_D_CS_N<9>	K16		DDR3_CKE<5>	R27
	NC_M_D_CS_N<8>	D16	DDR3_CS_N<9>	DDR3_CKE<4>	R25
	NC_M_D_CS_N<7>	E15	DDR3_CS_N<8>	DDR3_CKE<3>	N25
	NC_M_D_CS_N<6>	F16	DDR3_CS_N<7>	DDR3_CKE<2>	J25
	NC_M_D_CS_N<5>	G17	DDR3_CS_N<6>	DDR3_CKE<1>	M24
	NC_M_D_CS_N<4>	K18	DDR3_CS_N<5>	DDR3_CKE<0>	K24
3	M_D_CS_N<3>	G15	DDR3_CS_N<4>		
2	M_D_CS_N<2>	F14	DDR3_CS_N<3>	DDR3_BA<2>	B24
1	M_D_CS_N<1>	J19	DDR3_CS_N<2>	DDR3_BA<1>	E19
0	M_D_CS_N<0>	G19	DDR3_CS_N<1>	DDR3_BA<0>	A17
	NC_M_D_CK_DP<3>	M22	DDR3_CS_N<0>		
	M_D_CK_DP<2>	K20	DDR3_CLK_DP<3>	DDR3_ODT<5>	M16
	NC_M_D_CK_DP<1>	L21	DDR3_CLK_DP<2>	DDR3_ODT<4>	D14
	M_D_CK_DP<0>	L23	DDR3_CLK_DP<1>	DDR3_ODT<3>	J17
	NC_M_D_CK_DN<3>	K22	DDR3_CLK_DP<0>	DDR3_ODT<2>	E17
	M_D_CK_DN<2>	M20	DDR3_CLK_DN<3>	DDR3_ODT<1>	F18
	NC_M_D_CK_DN<1>	J21	DDR3_CLK_DN<2>	DDR3_ODT<0>	L19
	M_D_CK_DN<0>	J23	DDR3_CLK_DN<1>	DDR3_WE_N	A15
			DDR3_CLK_DN<0>	DDR3_RAS_N	B16
				DDR3_PAR_ERR_N	G21
				DDR3_CAS_N	B14
				DDR3_MA_PAR	B18

M_D_DQS_DP<17..0> BI 49<>

17	M_D_DQS_DP<17>	F28
16	M_D_DQS_DP<16>	J3
15	M_D_DQS_DP<15>	G7
14	M_D_DQS_DP<14>	K12
13	M_D_DQS_DP<13>	E11
12	M_D_DQS_DP<12>	N31
11	M_D_DQS_DP<11>	D34
10	M_D_DQS_DP<10>	M38
9	M_D_DQS_DP<9>	E39
8	M_D_DQS_DP<8>	E27
7	M_D_DQS_DP<7>	M4
6	M_D_DQS_DP<6>	K6
5	M_D_DQS_DP<5>	N11
4	M_D_DQS_DP<4>	D10
3	M_D_DQS_DP<3>	N29
2	M_D_DQS_DP<2>	E33
1	M_D_DQS_DP<1>	J37
0	M_D_DQS_DP<0>	D38

M_D_DQS_DN<17..0> BI 49<>

17	M_D_DQS_DN<17>	H28
16	M_D_DQS_DN<16>	K4
15	M_D_DQS_DN<15>	H6
14	M_D_DQS_DN<14>	M12
13	M_D_DQS_DN<13>	G11
12	M_D_DQS_DN<12>	M30
11	M_D_DQS_DN<11>	B34
10	M_D_DQS_DN<10>	K38
9	M_D_DQS_DN<9>	G39
8	M_D_DQS_DN<8>	G27
7	M_D_DQS_DN<7>	L3
6	M_D_DQS_DN<6>	J7
5	M_D_DQS_DN<5>	L11
4	M_D_DQS_DN<4>	B10
3	M_D_DQS_DN<3>	P28
2	M_D_DQS_DN<2>	G33
1	M_D_DQS_DN<1>	L37
0	M_D_DQS_DN<0>	B38

M_D_MA<15..0> OUT 49<

15	M_D_MA<15>	F24
14	M_D_MA<14>	D24
13	M_D_MA<13>	A13
12	M_D_MA<12>	E23
11	M_D_MA<11>	A23
10	M_D_MA<10>	D18
9	M_D_MA<9>	G23
8	M_D_MA<8>	D22
7	M_D_MA<7>	B22
6	M_D_MA<6>	F22
5	M_D_MA<5>	A21
4	M_D_MA<4>	D20
3	M_D_MA<3>	B20
2	M_D_MA<2>	F20
1	M_D_MA<1>	E21
0	M_D_MA<0>	A19

M_D_ECC<7..0> BI 49<>

7	M_D_ECC<7>	H26
6	M_D_ECC<6>	F26
5	M_D_ECC<5>	H30
4	M_D_ECC<4>	F30
3	M_D_ECC<3>	C25
2	M_D_ECC<2>	E25
1	M_D_ECC<1>	J29
0	M_D_ECC<0>	G29

	NC_M_D_CKE<5>	R27
	NC_M_D_CKE<4>	R25
	NC_M_D_CKE<3>	N25
	NC_M_D_CKE<2>	J25
1	M_D_CKE<1>	M24
0	M_D_CKE<0>	K24

M_D_CKE<1..0> OUT 49<

M_D_BA<2..0> OUT 49<

2	M_D_BA<2>	B24
1	M_D_BA<1>	E19
0	M_D_BA<0>	A17

	NC_M_D_ODT<5>	M16
	NC_M_D_ODT<4>	D14
	NC_M_D_ODT<3>	J17
	NC_M_D_ODT<2>	E17
1	M_D_ODT<1>	F18
0	M_D_ODT<0>	L19

M_D_ODT<1..0> OUT 49<

	M_D_WE_N	A15
	M_D_RAS_N	B16
	M_D_PAR_ERR_N<0>	G21
	M_D_CAS_N	B14
	M_D_MA_PAR	B18

M_D_WE_N OUT 49<
M_D_RAS_N OUT 49<
M_D_PAR_ERR_N<0> IN 49>
M_D_CAS_N OUT 49<
M_D_MA_PAR OUT 49<

49< OUT M_D_CS_N<3..0>

M_D_CK_DP<2> OUT 49<
M_D_CK_DP<0> OUT 49<
M_D_CK_DN<2> OUT 49<
M_D_CK_DN<0> OUT 49<

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CPU SOCKET 0 (5 OF 13)

DEPARTMENT: DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	SIZE: B / CODE: 34649 / DOCUMENT NUMBER: 444359 / REV: 1.0	
		SCALE:	DO NOT SCALE DRAWING / SHEET 37 OF 303

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U5H1
IC

SANDYBRIDGE_EP_EXT_D

171>	IN	P3E_CPU0_RCONN_RX_PE1A_DP<3..0>	3	P3E_CPU0_RCONN_RX_PE1A_DP<3>	E55	PE1A_RX_DP<3>	PE1A_TX_DP<3>	J45	P3E_CPU0_RCONN_TX_PE1A_DP<3> 3
			2	P3E_CPU0_RCONN_RX_PE1A_DP<2>	D54	PE1A_RX_DP<2>	PE1A_TX_DP<2>	H44	P3E_CPU0_RCONN_TX_PE1A_DN<2> 2
			1	P3E_CPU0_RCONN_RX_PE1A_DP<1>	D52	PE1A_RX_DP<1>	PE1A_TX_DP<1>	J43	P3E_CPU0_RCONN_TX_PE1A_DN<1> 1
			0	P3E_CPU0_RCONN_RX_PE1A_DP<0>	C51	PE1A_RX_DP<0>	PE1A_TX_DP<0>	H42	P3E_CPU0_RCONN_TX_PE1A_DN<0> 0
171>	IN	P3E_CPU0_RCONN_RX_PE1A_DN<3..0>	3	P3E_CPU0_RCONN_RX_PE1A_DN<3>	G55	PE1A_RX_DN<3>	PE1A_TX_DN<3>	L45	P3E_CPU0_RCONN_TX_PE1A_DN<3> 3
			2	P3E_CPU0_RCONN_RX_PE1A_DN<2>	F54	PE1A_RX_DN<2>	PE1A_TX_DN<2>	K44	P3E_CPU0_RCONN_TX_PE1A_DP<2> 2
			1	P3E_CPU0_RCONN_RX_PE1A_DN<1>	F52	PE1A_RX_DN<1>	PE1A_TX_DN<1>	L43	P3E_CPU0_RCONN_TX_PE1A_DP<1> 1
			0	P3E_CPU0_RCONN_RX_PE1A_DN<0>	E51	PE1A_RX_DN<0>	PE1A_TX_DN<0>	K42	P3E_CPU0_RCONN_TX_PE1A_DP<0> 0
171>	IN	P3E_CPU0_RCONN_RX_PE1B_DP<3..0>	3	P3E_CPU0_RCONN_RX_PE1B_DP<3>	K56	PE1B_RX_DP<7>	PE1B_TX_DP<7>	J49	P3E_CPU0_RCONN_TX_PE1B_DP<3> 3
			2	P3E_CPU0_RCONN_RX_PE1B_DP<2>	J57	PE1B_RX_DP<6>	PE1B_TX_DP<6>	H48	P3E_CPU0_RCONN_TX_PE1B_DP<2> 2
			1	P3E_CPU0_RCONN_RX_PE1B_DP<1>	K54	PE1B_RX_DP<5>	PE1B_TX_DP<5>	J47	P3E_CPU0_RCONN_TX_PE1B_DP<1> 1
			0	P3E_CPU0_RCONN_RX_PE1B_DP<0>	J53	PE1B_RX_DP<4>	PE1B_TX_DP<4>	H46	P3E_CPU0_RCONN_TX_PE1B_DP<0> 0
171>	IN	P3E_CPU0_RCONN_RX_PE1B_DN<3..0>	3	P3E_CPU0_RCONN_RX_PE1B_DN<3>	M56	PE1B_RX_DN<7>	PE1B_TX_DN<7>	L49	P3E_CPU0_RCONN_TX_PE1B_DN<3> 3
			2	P3E_CPU0_RCONN_RX_PE1B_DN<2>	L57	PE1B_RX_DN<6>	PE1B_TX_DN<6>	K48	P3E_CPU0_RCONN_TX_PE1B_DN<2> 2
			1	P3E_CPU0_RCONN_RX_PE1B_DN<1>	M54	PE1B_RX_DN<5>	PE1B_TX_DN<5>	L47	P3E_CPU0_RCONN_TX_PE1B_DN<1> 1
			0	P3E_CPU0_RCONN_RX_PE1B_DN<0>	L53	PE1B_RX_DN<4>	PE1B_TX_DN<4>	K46	P3E_CPU0_RCONN_TX_PE1B_DN<0> 0
		TP_P3E_CPU0_RX_PE2A_DP<3>			U55	PE2A_RX_DP<3>	PE2A_TX_DP<3>	AM52	TP_P3E_CPU0_TX_PE2A_DP<3>
		TP_P3E_CPU0_RX_PE2A_DP<2>			T56	PE2A_RX_DP<2>	PE2A_TX_DP<2>	AN51	TP_P3E_CPU0_TX_PE2A_DP<2>
		TP_P3E_CPU0_RX_PE2A_DP<1>			T54	PE2A_RX_DP<1>	PE2A_TX_DP<1>	AM50	TP_P3E_CPU0_TX_PE2A_DP<1>
		TP_P3E_CPU0_RX_PE2A_DP<0>			L55	PE2A_RX_DP<0>	PE2A_TX_DP<0>	AN49	TP_P3E_CPU0_TX_PE2A_DP<0>
		TP_P3E_CPU0_RX_PE2A_DN<3>			W55	PE2A_RX_DN<3>	PE2A_TX_DN<3>	AP52	TP_P3E_CPU0_TX_PE2A_DN<3>
		TP_P3E_CPU0_RX_PE2A_DN<2>			V56	PE2A_RX_DN<2>	PE2A_TX_DN<2>	AR51	TP_P3E_CPU0_TX_PE2A_DN<2>
		TP_P3E_CPU0_RX_PE2A_DN<1>			V54	PE2A_RX_DN<1>	PE2A_TX_DN<1>	AP50	TP_P3E_CPU0_TX_PE2A_DN<1>
		TP_P3E_CPU0_RX_PE2A_DN<0>			N55	PE2A_RX_DN<0>	PE2A_TX_DN<0>	AR49	TP_P3E_CPU0_TX_PE2A_DN<0>
		TP_P3E_CPU0_RX_PE2B_DP<3>			AE57	PE2B_RX_DP<7>	PE2B_TX_DP<7>	AP54	TP_P3E_CPU0_TX_PE2B_DP<3>
		TP_P3E_CPU0_RX_PE2B_DP<2>			AC55	PE2B_RX_DP<6>	PE2B_TX_DP<6>	AN53	TP_P3E_CPU0_TX_PE2B_DP<2>
		TP_P3E_CPU0_RX_PE2B_DP<1>			AB56	PE2B_RX_DP<5>	PE2B_TX_DP<5>	AH54	TP_P3E_CPU0_TX_PE2B_DP<1>
		TP_P3E_CPU0_RX_PE2B_DP<0>			AB54	PE2B_RX_DP<4>	PE2B_TX_DP<4>	AG53	TP_P3E_CPU0_TX_PE2B_DP<0>
		TP_P3E_CPU0_RX_PE2B_DN<3>			AF58	PE2B_RX_DN<7>	PE2B_TX_DN<7>	AT54	TP_P3E_CPU0_TX_PE2B_DN<3>
		TP_P3E_CPU0_RX_PE2B_DN<2>			AE55	PE2B_RX_DN<6>	PE2B_TX_DN<6>	AR53	TP_P3E_CPU0_TX_PE2B_DN<2>
		TP_P3E_CPU0_RX_PE2B_DN<1>			AD56	PE2B_RX_DN<5>	PE2B_TX_DN<5>	AK54	TP_P3E_CPU0_TX_PE2B_DN<1>
		TP_P3E_CPU0_RX_PE2B_DN<0>			AD54	PE2B_RX_DN<4>	PE2B_TX_DN<4>	AJ53	TP_P3E_CPU0_TX_PE2B_DN<0>
228< 225>	IN	P2E_CPU0_TWV_RX_PE2C_C_DP<3..0>	3	P2E_CPU0_TWV_RX_PE2C_C_DP<3>	AR57	PE2C_RX_DP<11>	PE2C_TX_DP<11>	AW51	P2E_CPU0_TWV_TX_PE2C_DP<3> 3
			2	P2E_CPU0_TWV_RX_PE2C_C_DP<2>	AJ57	PE2C_RX_DP<10>	PE2C_TX_DP<10>	AY54	P2E_CPU0_TWV_TX_PE2C_DP<2> 2
			1	P2E_CPU0_TWV_RX_PE2C_C_DP<1>	AK58	PE2C_RX_DP<9>	PE2C_TX_DP<9>	AW53	P2E_CPU0_TWV_TX_PE2C_DP<1> 1
			0	P2E_CPU0_TWV_RX_PE2C_C_DP<0>	AH56	PE2C_RX_DP<8>	PE2C_TX_DP<8>	AV52	P2E_CPU0_TWV_TX_PE2C_DP<0> 0
228< 225>	IN	P2E_CPU0_TWV_RX_PE2C_C_DN<3..0>	3	P2E_CPU0_TWV_RX_PE2C_C_DN<3>	AU57	PE2C_RX_DN<11>	PE2C_TX_DN<11>	BA51	P2E_CPU0_TWV_TX_PE2C_DN<3> 3
			2	P2E_CPU0_TWV_RX_PE2C_C_DN<2>	AL57	PE2C_RX_DN<10>	PE2C_TX_DN<10>	BB54	P2E_CPU0_TWV_TX_PE2C_DN<2> 2
			1	P2E_CPU0_TWV_RX_PE2C_C_DN<1>	AM58	PE2C_RX_DN<9>	PE2C_TX_DN<9>	BA53	P2E_CPU0_TWV_TX_PE2C_DN<1> 1
			0	P2E_CPU0_TWV_RX_PE2C_C_DN<0>	AK56	PE2C_RX_DN<8>	PE2C_TX_DN<8>	AY52	P2E_CPU0_TWV_TX_PE2C_DN<0> 0

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P3E_CPU0_RCONN_TX_PE1A_DP<3..0> OUT 173<
P3E_CPU0_RCONN_TX_PE1A_DN<3..0> OUT 173<
P3E_CPU0_RCONN_TX_PE1B_DP<3..0> OUT 173<
P3E_CPU0_RCONN_TX_PE1B_DN<3..0> OUT 173<
P2E_CPU0_TWV_TX_PE2C_DP<3..0> OUT 225<
P2E_CPU0_TWV_TX_PE2C_DN<3..0> OUT 225<

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CPU SOCKET 0 (6 OF 13)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 38 OF 303	

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228< 225>	IN	P2E_CPU0_TWV_RX_PE2D_C_DP<3..0>	3	P2E_CPU0_TWV_RX_PE2D_C_DP<3>	AY56	PE2D_RX_DP<15>	PE2D_TX_DP<15>	AW47	P2E_CPU0_TWV_TX_PE2D_DP<3>	3	P2E_CPU0_TWV_TX_PE2D_DP<3..0> OUT 225<
			2	P2E_CPU0_TWV_RX_PE2D_C_DP<2>	AY58	PE2D_RX_DP<14>	PE2D_TX_DP<14>	AV48	P2E_CPU0_TWV_TX_PE2D_DP<2>	2	
			1	P2E_CPU0_TWV_RX_PE2D_C_DP<1>	AP56	PE2D_RX_DP<13>	PE2D_TX_DP<13>	AW49	P2E_CPU0_TWV_TX_PE2D_DP<1>	1	
			0	P2E_CPU0_TWV_RX_PE2D_C_DP<0>	AT58	PE2D_RX_DP<12>	PE2D_TX_DP<12>	AV50	P2E_CPU0_TWV_TX_PE2D_DP<0>	0	
228< 225>	IN	P2E_CPU0_TWV_RX_PE2D_C_DN<3..0>	3	P2E_CPU0_TWV_RX_PE2D_C_DN<3>	BB56	PE2D_RX_DN<15>	PE2D_TX_DN<15>	BA47	P2E_CPU0_TWV_TX_PE2D_DN<3>	3	P2E_CPU0_TWV_TX_PE2D_DN<3..0> OUT 225<
			2	P2E_CPU0_TWV_RX_PE2D_C_DN<2>	BA57	PE2D_RX_DN<14>	PE2D_TX_DN<14>	AY48	P2E_CPU0_TWV_TX_PE2D_DN<2>	2	
			1	P2E_CPU0_TWV_RX_PE2D_C_DN<1>	AT56	PE2D_RX_DN<13>	PE2D_TX_DN<13>	BA49	P2E_CPU0_TWV_TX_PE2D_DN<1>	1	
			0	P2E_CPU0_TWV_RX_PE2D_C_DN<0>	AV58	PE2D_RX_DN<12>	PE2D_TX_DN<12>	AY50	P2E_CPU0_TWV_TX_PE2D_DN<0>	0	
171>	IN	P3E_CPU0_RCONN_RX_PE3A_DP<3..0>	3	P3E_CPU0_RCONN_RX_PE3A_DP<3>	AA49	PE3A_RX_DP<3>	PE3A_TX_DP<3>	P48	P3E_CPU0_RCONN_TX_PE3A_DP<3>	3	P3E_CPU0_RCONN_TX_PE3A_DP<3..0> OUT 51<
			2	P3E_CPU0_RCONN_RX_PE3A_DP<2>	AF46	PE3A_RX_DP<2>	PE3A_TX_DP<2>	R47	P3E_CPU0_RCONN_TX_PE3A_DP<2>	2	
			1	P3E_CPU0_RCONN_RX_PE3A_DP<1>	AG45	PE3A_RX_DP<1>	PE3A_TX_DP<1>	J51	P3E_CPU0_RCONN_TX_PE3A_DP<1>	1	
			0	P3E_CPU0_RCONN_RX_PE3A_DP<0>	AF44	PE3A_RX_DP<0>	PE3A_TX_DP<0>	H50	P3E_CPU0_RCONN_TX_PE3A_DP<0>	0	
171>	IN	P3E_CPU0_RCONN_RX_PE3A_DN<3..0>	3	P3E_CPU0_RCONN_RX_PE3A_DN<3>	AC49	PE3A_RX_DN<3>	PE3A_TX_DN<3>	T48	P3E_CPU0_RCONN_TX_PE3A_DN<3>	3	P3E_CPU0_RCONN_TX_PE3A_DN<3..0> OUT 51<
			2	P3E_CPU0_RCONN_RX_PE3A_DN<2>	AH46	PE3A_RX_DN<2>	PE3A_TX_DN<2>	U47	P3E_CPU0_RCONN_TX_PE3A_DN<2>	2	
			1	P3E_CPU0_RCONN_RX_PE3A_DN<1>	AJ45	PE3A_RX_DN<1>	PE3A_TX_DN<1>	L51	P3E_CPU0_RCONN_TX_PE3A_DN<1>	1	
			0	P3E_CPU0_RCONN_RX_PE3A_DN<0>	AH44	PE3A_RX_DN<0>	PE3A_TX_DN<0>	K50	P3E_CPU0_RCONN_TX_PE3A_DN<0>	0	
171>	IN	P3E_CPU0_RCONN_RX_PE3B_DP<3..0>	3	P3E_CPU0_RCONN_RX_PE3B_DP<3>	AA51	PE3B_RX_DP<7>	PE3B_TX_DP<7>	R49	P3E_CPU0_RCONN_TX_PE3B_DP<3>	3	P3E_CPU0_RCONN_TX_PE3B_DP<3..0> OUT 51<
			2	P3E_CPU0_RCONN_RX_PE3B_DP<2>	AA53	PE3B_RX_DP<6>	PE3B_TX_DP<6>	P50	P3E_CPU0_RCONN_TX_PE3B_DP<2>	2	
			1	P3E_CPU0_RCONN_RX_PE3B_DP<1>	Y52	PE3B_RX_DP<5>	PE3B_TX_DP<5>	R51	P3E_CPU0_RCONN_TX_PE3B_DP<1>	1	
			0	P3E_CPU0_RCONN_RX_PE3B_DP<0>	Y50	PE3B_RX_DP<4>	PE3B_TX_DP<4>	P52	P3E_CPU0_RCONN_TX_PE3B_DP<0>	0	
171>	IN	P3E_CPU0_RCONN_RX_PE3B_DN<3..0>	3	P3E_CPU0_RCONN_RX_PE3B_DN<3>	AC51	PE3B_RX_DN<7>	PE3B_TX_DN<7>	U49	P3E_CPU0_RCONN_TX_PE3B_DN<3>	3	P3E_CPU0_RCONN_TX_PE3B_DN<3..0> OUT 51<
			2	P3E_CPU0_RCONN_RX_PE3B_DN<2>	AC53	PE3B_RX_DN<6>	PE3B_TX_DN<6>	T50	P3E_CPU0_RCONN_TX_PE3B_DN<2>	2	
			1	P3E_CPU0_RCONN_RX_PE3B_DN<1>	AB52	PE3B_RX_DN<5>	PE3B_TX_DN<5>	U51	P3E_CPU0_RCONN_TX_PE3B_DN<1>	1	
			0	P3E_CPU0_RCONN_RX_PE3B_DN<0>	AB50	PE3B_RX_DN<4>	PE3B_TX_DN<4>	T52	P3E_CPU0_RCONN_TX_PE3B_DN<0>	0	
171>	IN	P3E_CPU0_RCONN_RX_PE3C_DP<3..0>	3	P3E_CPU0_RCONN_RX_PE3C_DP<3>	AG49	PE3C_RX_DP<11>	PE3C_TX_DP<11>	Y46	P3E_CPU0_RCONN_TX_PE3C_DP<3>	3	P3E_CPU0_RCONN_TX_PE3C_DP<3..0> OUT 51<
			2	P3E_CPU0_RCONN_RX_PE3C_DP<2>	AF50	PE3C_RX_DP<10>	PE3C_TX_DP<10>	R45	P3E_CPU0_RCONN_TX_PE3C_DP<2>	2	
			1	P3E_CPU0_RCONN_RX_PE3C_DP<1>	AG51	PE3C_RX_DP<9>	PE3C_TX_DP<9>	AA47	P3E_CPU0_RCONN_TX_PE3C_DP<1>	1	
			0	P3E_CPU0_RCONN_RX_PE3C_DP<0>	AF48	PE3C_RX_DP<8>	PE3C_TX_DP<8>	P46	P3E_CPU0_RCONN_TX_PE3C_DP<0>	0	
171>	IN	P3E_CPU0_RCONN_RX_PE3C_DN<3..0>	3	P3E_CPU0_RCONN_RX_PE3C_DN<3>	AJ49	PE3C_RX_DN<11>	PE3C_TX_DN<11>	AB46	P3E_CPU0_RCONN_TX_PE3C_DN<3>	3	P3E_CPU0_RCONN_TX_PE3C_DN<3..0> OUT 51<
			2	P3E_CPU0_RCONN_RX_PE3C_DN<2>	AH50	PE3C_RX_DN<10>	PE3C_TX_DN<10>	U45	P3E_CPU0_RCONN_TX_PE3C_DN<2>	2	
			1	P3E_CPU0_RCONN_RX_PE3C_DN<1>	AJ51	PE3C_RX_DN<9>	PE3C_TX_DN<9>	AC47	P3E_CPU0_RCONN_TX_PE3C_DN<1>	1	
			0	P3E_CPU0_RCONN_RX_PE3C_DN<0>	AH48	PE3C_RX_DN<8>	PE3C_TX_DN<8>	T46	P3E_CPU0_RCONN_TX_PE3C_DN<0>	0	
171>	IN	P3E_CPU0_RCONN_RX_PE3D_DP<3..0>	3	P3E_CPU0_RCONN_RX_PE3D_DP<3>	AN45	PE3D_RX_DP<15>	PE3D_TX_DP<15>	T44	P3E_CPU0_RCONN_TX_PE3D_DP<3>	3	P3E_CPU0_RCONN_TX_PE3D_DP<3..0> OUT 51<
			2	P3E_CPU0_RCONN_RX_PE3D_DP<2>	AM46	PE3D_RX_DP<14>	PE3D_TX_DP<14>	AC43	P3E_CPU0_RCONN_TX_PE3D_DP<2>	2	
			1	P3E_CPU0_RCONN_RX_PE3D_DP<1>	AN47	PE3D_RX_DP<13>	PE3D_TX_DP<13>	Y44	P3E_CPU0_RCONN_TX_PE3D_DP<1>	1	
			0	P3E_CPU0_RCONN_RX_PE3D_DP<0>	AG47	PE3D_RX_DP<12>	PE3D_TX_DP<12>	AA45	P3E_CPU0_RCONN_TX_PE3D_DP<0>	0	
171>	IN	P3E_CPU0_RCONN_RX_PE3D_DN<3..0>	3	P3E_CPU0_RCONN_RX_PE3D_DN<3>	AR45	PE3D_RX_DN<15>	PE3D_TX_DN<15>	P44	P3E_CPU0_RCONN_TX_PE3D_DN<3>	3	P3E_CPU0_RCONN_TX_PE3D_DN<3..0> OUT 51<
			2	P3E_CPU0_RCONN_RX_PE3D_DN<2>	AP46	PE3D_RX_DN<14>	PE3D_TX_DN<14>	AA43	P3E_CPU0_RCONN_TX_PE3D_DN<2>	2	
			1	P3E_CPU0_RCONN_RX_PE3D_DN<1>	AR47	PE3D_RX_DN<13>	PE3D_TX_DN<13>	AB44	P3E_CPU0_RCONN_TX_PE3D_DN<1>	1	
			0	P3E_CPU0_RCONN_RX_PE3D_DN<0>	AJ47	PE3D_RX_DN<12>	PE3D_TX_DN<12>	AC45	P3E_CPU0_RCONN_TX_PE3D_DN<0>	0	

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CPU SOCKET 0 (7 OF 13)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 39 OF 303	

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SANDYBRIDGE_EP_EXT_D

131< IN XDP_CPU0_MBP_N<7..0>

7	XDP_CPU0_MBP_N<7>	AY44	BPM_N<7>
6	XDP_CPU0_MBP_N<6>	BA43	BPM_N<6>
5	XDP_CPU0_MBP_N<5>	AW43	BPM_N<5>
4	XDP_CPU0_MBP_N<4>	BB44	BPM_N<4>
3	XDP_CPU0_MBP_N<3>	AV44	BPM_N<3>
2	XDP_CPU0_MBP_N<2>	AU43	BPM_N<2>
1	XDP_CPU0_MBP_N<1>	AT44	BPM_N<1>
0	XDP_CPU0_MBP_N<0>	AR43	BPM_N<0>

CAD NOTE: PLACE CLOSE TO CPU

	NC_CPU0_RSVD<16>	A53	RSVD<16>
	NC_CPU0_RSVD<14>	C53	RSVD<14>

86<> 63<> 40> 109<> BI FM_CPU_ONLY_RESET — R5F32 1 2 36.0 A93549-074 1/16W 5% 0402LF — FM_CPU0_ONLY_RESET_R AN43 — CPU_ONLY_RESET

	NC_CPU0_RSVD<15>	B46	RSVD<15>
	NC_CPU0_RSVD<13>	D46	RSVD<13>
	NC_CPU0_RSVD<3>	K58	RSVD<3>
	NC_CPU0_RSVD<60>	AY46	RSVD<60>
	NC_CPU0_RSVD<61>	AV46	RSVD<61>
	NC_CPU0_RSVD<64>	AM44	RSVD<64>
	NC_CPU0_RSVD<65>	AL55	RSVD<65>
	NC_CPU0_RSVD<66>	AJ55	RSVD<66>
	NC_CPU0_RSVD<55>	BD48	RSVD<55>

NOTE: DMI PORT LANE REVERSED FROM UPSTREAM DEVICE (CPU)

154> 154< IN DMI_CPU0_SSB_RX_C_DP<3..0>

0	DMI_CPU0_SSB_RX_C_DP<0>	B50	DMI_RX_DP<3>
1	DMI_CPU0_SSB_RX_C_DP<1>	C49	DMI_RX_DP<2>
2	DMI_CPU0_SSB_RX_C_DP<2>	B48	DMI_RX_DP<1>
3	DMI_CPU0_SSB_RX_C_DP<3>	C47	DMI_RX_DP<0>

154> 154< IN DMI_CPU0_SSB_RX_C_DN<3..0>

0	DMI_CPU0_SSB_RX_C_DN<0>	D50	DMI_RX_DN<3>
1	DMI_CPU0_SSB_RX_C_DN<1>	E49	DMI_RX_DN<2>
2	DMI_CPU0_SSB_RX_C_DN<2>	D48	DMI_RX_DN<1>
3	DMI_CPU0_SSB_RX_C_DN<3>	E47	DMI_RX_DN<0>

53< OUT PD_CPU0_TEST<3..0>

3	PD_CPU0_TEST<3>	D4	TEST3
2	PD_CPU0_TEST<2>	F2	TEST2
1	PD_CPU0_TEST<1>	CW1	TEST1
0	PD_CPU0_TEST<0>	DB4	TEST0

53> IN A_CPU0_DDR23_RCOMP<2..0>

2	A_CPU0_DDR23_RCOMP<2>	Y14	DDR23_RCOMP<2>
1	A_CPU0_DDR23_RCOMP<1>	AC15	DDR23_RCOMP<1>
0	A_CPU0_DDR23_RCOMP<0>	U15	DDR23_RCOMP<0>

53> IN A_CPU0_DDR01_RCOMP<2..0>

2	A_CPU0_DDR01_RCOMP<2>	CB20	DDR01_RCOMP<2>
1	A_CPU0_DDR01_RCOMP<1>	CC19	DDR01_RCOMP<1>
0	A_CPU0_DDR01_RCOMP<0>	CA17	DDR01_RCOMP<0>

109> 86> 78< 63> OUT FM_CPU_ERR_N<2..0>

2	FM_CPU_ERR_N<2>	BC51	ERROR_N<2>
1	FM_CPU_ERR_N<1>	CB54	ERROR_N<1>
0	FM_CPU_ERR_N<0>	BD50	ERROR_N<0>

	NC_CPU0_RSVD<45>	BJ45	RSVD<45>
	NC_CPU0_RSVD<38>	BP44	RSVD<38>
	NC_CPU0_RSVD<49>	BG45	RSVD<49>
	NC_CPU0_RSVD<42>	BL45	RSVD<42>
	NC_CPU0_RSVD<47>	BH46	RSVD<47>
	NC_CPU0_RSVD<44>	BK44	RSVD<44>
	NC_CPU0_RSVD<53>	BE45	RSVD<53>
	NC_CPU0_RSVD<48>	BH44	RSVD<48>
	NC_CPU0_RSVD<57>	BD44	RSVD<57>
	NC_CPU0_RSVD<56>	BD46	RSVD<56>
	NC_CPU0_RSVD<51>	BF46	RSVD<51>
	NC_CPU0_RSVD<36>	BR43	RSVD<36>
	NC_CPU0_RSVD<43>	BL43	RSVD<43>
	NC_CPU0_RSVD<33>	BU43	RSVD<33>
	NC_CPU0_RSVD<50>	BG43	RSVD<50>
	NC_CPU0_RSVD<41>	BM44	RSVD<41>
	NC_CPU0_RSVD<46>	BJ43	RSVD<46>
	NC_CPU0_RSVD<54>	BE43	RSVD<54>

NOTE: DMI PORT WITH LANE REVERSAL FROM UPSTREAM DEVICE (CPU)

DMI_CPU0_SSB_TX_DP<3..0> OUT 154<

0	DMI_CPU0_SSB_TX_DP<0>	C45	DMI_TX_DP<3>
1	DMI_CPU0_SSB_TX_DP<1>	B44	DMI_TX_DP<2>
2	DMI_CPU0_SSB_TX_DP<2>	C43	DMI_TX_DP<1>
3	DMI_CPU0_SSB_TX_DP<3>	B42	DMI_TX_DP<0>

DMI_CPU0_SSB_TX_DN<3..0> OUT 154<

0	DMI_CPU0_SSB_TX_DN<0>	E45	DMI_TX_DN<3>
1	DMI_CPU0_SSB_TX_DN<1>	D44	DMI_TX_DN<2>
2	DMI_CPU0_SSB_TX_DN<2>	E43	DMI_TX_DN<1>
3	DMI_CPU0_SSB_TX_DN<3>	D42	DMI_TX_DN<0>

	NC_CPU0_RSVD<68>	AP48	RSVD<68>
	NC_CPU0_RSVD<11>	E53	RSVD<11>
	NC_CPU0_RSVD<34>	BT44	RSVD<34>
	NC_CPU0_RSVD<52>	BE47	RSVD<52>
	NC_CPU0_RSVD<0>	Y48	RSVD<0>
	NC_CPU0_RSVD<2>	M48	RSVD<2>
	NC_CPU0_RSVD<4>	J15	RSVD<4>
	NC_CPU0_RSVD<6>	H56	RSVD<6>
	NC_CPU0_RSVD<9>	F46	RSVD<9>
	NC_CPU0_RSVD<27>	CG11	RSVD<27>
	NC_CPU0_RSVD<28>	CF44	RSVD<28>
	NC_CPU0_RSVD<29>	CE43	RSVD<29>
	NC_CPU0_RSVD<30>	CD44	RSVD<30>
	NC_CPU0_RSVD<1>	W15	RSVD<1>
	NC_CPU0_RSVD<35>	BR47	RSVD<35>
	NC_CPU0_RSVD<39>	BN47	RSVD<39>
	NC_CPU0_RSVD<26>	CP54	RSVD<26>
	NC_CPU0_RSVD<58>	BC47	RSVD<58>
	NC_CPU0_RSVD<67>	AB48	RSVD<67>

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P1V05_VTT_CPU0

1.05 R4T2 1 330 5% 1/16W 2 A93549-012 0402LF

FM_CPU_ONLY_RESET OUT 40<> 63<> 86<> 109<>

CAD NOTE: PLACE AMONG ALL CPU, SAME LENGTH TO ALL CPUS

CPU SOCKET 0 (8 OF 13)

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DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 40 OF 303	

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NOTE: QPI P0 RX NETS WITH LANE REVERSAL

NOTE: POLARITY INVERSION ON LANES 0,1,2,3,5,8,10,11,12,13,14,15,16,17,18,19

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111> IN	QPI_CPU3_CPU0_P1P0_DP<19..0>								OUT 111< QPI_CPU0_CPU3_P0P1_DP<19..0>
111> IN	QPI_CPU3_CPU0_P1P0_DN<19..0>								OUT 111< QPI_CPU0_CPU3_P0P1_DN<19..0>
0	QPI_CPU3_CPU0_P1P0_DN<0>	BP48	QPI0_DRX_DP<19>	QPI0_DTX_DP<19>	CE49	QPI_CPU0_CPU3_P0P1_DP<19>	19		
1	QPI_CPU3_CPU0_P1P0_DN<1>	BR49	QPI0_DRX_DP<18>	QPI0_DTX_DP<18>	CE51	QPI_CPU0_CPU3_P0P1_DP<18>	18		
2	QPI_CPU3_CPU0_P1P0_DN<2>	BG49	QPI0_DRX_DP<17>	QPI0_DTX_DP<17>	CD52	QPI_CPU0_CPU3_P0P1_DP<17>	17		
3	QPI_CPU3_CPU0_P1P0_DN<3>	BM50	QPI0_DRX_DP<16>	QPI0_DTX_DP<16>	CD50	QPI_CPU0_CPU3_P0P1_DP<16>	16		
4	QPI_CPU3_CPU0_P1P0_DP<4>	BN51	QPI0_DRX_DP<15>	QPI0_DTX_DP<15>	CD48	QPI_CPU0_CPU3_P0P1_DP<15>	15		
5	QPI_CPU3_CPU0_P1P0_DN<5>	BM52	QPI0_DRX_DP<14>	QPI0_DTX_DP<14>	CE47	QPI_CPU0_CPU3_P0P1_DP<14>	14		
6	QPI_CPU3_CPU0_P1P0_DP<6>	BL53	QPI0_DRX_DP<13>	QPI0_DTX_DP<13>	BY50	QPI_CPU0_CPU3_P0P1_DP<13>	13		
7	QPI_CPU3_CPU0_P1P0_DP<7>	BM54	QPI0_DRX_DP<12>	QPI0_DTX_DP<12>	BY48	QPI_CPU0_CPU3_P0P1_DP<12>	12		
8	QPI_CPU3_CPU0_P1P0_DN<8>	BL55	QPI0_DRX_DP<11>	QPI0_DTX_DP<11>	CA51	QPI_CPU0_CPU3_P0P1_DP<11>	11		
9	QPI_CPU3_CPU0_P1P0_DP<9>	BM56	QPI0_DRX_DP<10>	QPI0_DTX_DP<10>	CD46	QPI_CPU0_CPU3_P0P1_DP<10>	10		
10	QPI_CPU3_CPU0_P1P0_DN<10>	BL57	QPI0_DRX_DP<9>	QPI0_DTX_DP<9>	BV46	QPI_CPU0_CPU3_P0P1_DP<9>	9		
11	QPI_CPU3_CPU0_P1P0_DN<11>	BE57	QPI0_DRX_DP<8>	QPI0_DTX_DP<8>	BV56	QPI_CPU0_CPU3_P0P1_DP<8>	8		
12	QPI_CPU3_CPU0_P1P0_DN<12>	BD58	QPI0_DRX_DP<7>	QPI0_DTX_DP<7>	BU57	QPI_CPU0_CPU3_P0P1_DP<7>	7		
13	QPI_CPU3_CPU0_P1P0_DN<13>	BF50	QPI0_DRX_DP<6>	QPI0_DTX_DP<6>	BV48	QPI_CPU0_CPU3_P0P1_DP<6>	6		
14	QPI_CPU3_CPU0_P1P0_DN<14>	BF54	QPI0_DRX_DP<5>	QPI0_DTX_DP<5>	BT58	QPI_CPU0_CPU3_P0P1_DP<5>	5		
15	QPI_CPU3_CPU0_P1P0_DN<15>	BF56	QPI0_DRX_DP<4>	QPI0_DTX_DP<4>	BU55	QPI_CPU0_CPU3_P0P1_DP<4>	4		
16	QPI_CPU3_CPU0_P1P0_DN<16>	BE55	QPI0_DRX_DP<3>	QPI0_DTX_DP<3>	BV54	QPI_CPU0_CPU3_P0P1_DP<3>	3		
17	QPI_CPU3_CPU0_P1P0_DN<17>	BE53	QPI0_DRX_DP<2>	QPI0_DTX_DP<2>	BU53	QPI_CPU0_CPU3_P0P1_DP<2>	2		
18	QPI_CPU3_CPU0_P1P0_DN<18>	BF52	QPI0_DRX_DP<1>	QPI0_DTX_DP<1>	BV52	QPI_CPU0_CPU3_P0P1_DP<1>	1		
19	QPI_CPU3_CPU0_P1P0_DN<19>	BG51	QPI0_DRX_DP<0>	QPI0_DTX_DP<0>	BV50	QPI_CPU0_CPU3_P0P1_DP<0>	0		
0	QPI_CPU3_CPU0_P1P0_DP<0>	BM48	QPI0_DRX_DN<19>	QPI0_DTX_DN<19>	CG49	QPI_CPU0_CPU3_P0P1_DN<19>	19		
1	QPI_CPU3_CPU0_P1P0_DP<1>	BN49	QPI0_DRX_DN<18>	QPI0_DTX_DN<18>	CG51	QPI_CPU0_CPU3_P0P1_DN<18>	18		
2	QPI_CPU3_CPU0_P1P0_DP<2>	BJ49	QPI0_DRX_DN<17>	QPI0_DTX_DN<17>	CF52	QPI_CPU0_CPU3_P0P1_DN<17>	17		
3	QPI_CPU3_CPU0_P1P0_DP<3>	BP50	QPI0_DRX_DN<16>	QPI0_DTX_DN<16>	CF50	QPI_CPU0_CPU3_P0P1_DN<16>	16		
4	QPI_CPU3_CPU0_P1P0_DN<4>	BR51	QPI0_DRX_DN<15>	QPI0_DTX_DN<15>	CF48	QPI_CPU0_CPU3_P0P1_DN<15>	15		
5	QPI_CPU3_CPU0_P1P0_DP<5>	BP52	QPI0_DRX_DN<14>	QPI0_DTX_DN<14>	CG47	QPI_CPU0_CPU3_P0P1_DN<14>	14		
6	QPI_CPU3_CPU0_P1P0_DN<6>	BN53	QPI0_DRX_DN<13>	QPI0_DTX_DN<13>	CA49	QPI_CPU0_CPU3_P0P1_DN<13>	13		
7	QPI_CPU3_CPU0_P1P0_DN<7>	BP54	QPI0_DRX_DN<12>	QPI0_DTX_DN<12>	CA47	QPI_CPU0_CPU3_P0P1_DN<12>	12		
8	QPI_CPU3_CPU0_P1P0_DP<8>	BN55	QPI0_DRX_DN<11>	QPI0_DTX_DN<11>	BY52	QPI_CPU0_CPU3_P0P1_DN<11>	11		
9	QPI_CPU3_CPU0_P1P0_DN<9>	BP56	QPI0_DRX_DN<10>	QPI0_DTX_DN<10>	CF46	QPI_CPU0_CPU3_P0P1_DN<10>	10		
10	QPI_CPU3_CPU0_P1P0_DP<10>	BN57	QPI0_DRX_DN<9>	QPI0_DTX_DN<9>	BW45	QPI_CPU0_CPU3_P0P1_DN<9>	9		
11	QPI_CPU3_CPU0_P1P0_DP<11>	BG57	QPI0_DRX_DN<8>	QPI0_DTX_DN<8>	BY56	QPI_CPU0_CPU3_P0P1_DN<8>	8		
12	QPI_CPU3_CPU0_P1P0_DP<12>	BF58	QPI0_DRX_DN<7>	QPI0_DTX_DN<7>	BW57	QPI_CPU0_CPU3_P0P1_DN<7>	7		
13	QPI_CPU3_CPU0_P1P0_DP<13>	BH50	QPI0_DRX_DN<6>	QPI0_DTX_DN<6>	BW47	QPI_CPU0_CPU3_P0P1_DN<6>	6		
14	QPI_CPU3_CPU0_P1P0_DP<14>	BH54	QPI0_DRX_DN<5>	QPI0_DTX_DN<5>	BV58	QPI_CPU0_CPU3_P0P1_DN<5>	5		
15	QPI_CPU3_CPU0_P1P0_DP<15>	BH56	QPI0_DRX_DN<4>	QPI0_DTX_DN<4>	BW55	QPI_CPU0_CPU3_P0P1_DN<4>	4		
16	QPI_CPU3_CPU0_P1P0_DP<16>	BG55	QPI0_DRX_DN<3>	QPI0_DTX_DN<3>	BY54	QPI_CPU0_CPU3_P0P1_DN<3>	3		
17	QPI_CPU3_CPU0_P1P0_DP<17>	BG53	QPI0_DRX_DN<2>	QPI0_DTX_DN<2>	BW53	QPI_CPU0_CPU3_P0P1_DN<2>	2		
18	QPI_CPU3_CPU0_P1P0_DP<18>	BH52	QPI0_DRX_DN<1>	QPI0_DTX_DN<1>	BW51	QPI_CPU0_CPU3_P0P1_DN<1>	1		
19	QPI_CPU3_CPU0_P1P0_DP<19>	BJ51	QPI0_DRX_DN<0>	QPI0_DTX_DN<0>	BW49	QPI_CPU0_CPU3_P0P1_DN<0>	0		
111> IN	QPI_CPU3_CPU0_P1P0_CLKA_DP	BK58	QPI0_CLKRX_DP	QPI0_CLKTX_DP	CE45	QPI_CPU0_CPU3_P0P1_CLKA_DP		OUT	111<
111> IN	QPI_CPU3_CPU0_P1P0_CLKA_DN	BM58	QPI0_CLKRX_DN	QPI0_CLKTX_DN	CG45	QPI_CPU0_CPU3_P0P1_CLKA_DN		OUT	111<

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E64556-001

CPU SOCKET 0 (9 OF 13)

Wed Oct 27 15:21:22 2010

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 41 OF 303	

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NOTE: QPI P1 RX NETS WITH LANE REVERSAL

NOTE: POLARITY INVERSION ON LANES 4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19

U5H1
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SANDYBRIDGE_EP_EXT_D

64> IN	QPI_CPU1_CPU0_P0P1_DP<19..0>									OUT 64< QPI_CPU0_CPU1_P1P0_DP<19..0>
64> IN	QPI_CPU1_CPU0_P0P1_DN<19..0>									OUT 64< QPI_CPU0_CPU1_P1P0_DN<19..0>
	0	QPI_CPU1_CPU0_P0P1_DP<0>	CL45	QPI1_DRX_DP<19>	QPI1_DTX_DP<19>	DB42	QPI_CPU0_CPU1_P1P0_DP<19>	19		
	1	QPI_CPU1_CPU0_P0P1_DP<1>	CK46	QPI1_DRX_DP<18>	QPI1_DTX_DP<18>	DE43	QPI_CPU0_CPU1_P1P0_DP<18>	18		
	2	QPI_CPU1_CPU0_P0P1_DP<2>	CL47	QPI1_DRX_DP<17>	QPI1_DTX_DP<17>	CU43	QPI_CPU0_CPU1_P1P0_DP<17>	17		
	3	QPI_CPU1_CPU0_P0P1_DP<3>	CK48	QPI1_DRX_DP<16>	QPI1_DTX_DP<16>	DB44	QPI_CPU0_CPU1_P1P0_DP<16>	16		
	4	QPI_CPU1_CPU0_P0P1_DN<4>	CN49	QPI1_DRX_DP<15>	QPI1_DTX_DP<15>	DE45	QPI_CPU0_CPU1_P1P0_DP<15>	15		
	5	QPI_CPU1_CPU0_P0P1_DN<5>	CM50	QPI1_DRX_DP<14>	QPI1_DTX_DP<14>	CT44	QPI_CPU0_CPU1_P1P0_DP<14>	14		
	6	QPI_CPU1_CPU0_P0P1_DN<6>	CN51	QPI1_DRX_DP<13>	QPI1_DTX_DP<13>	DB46	QPI_CPU0_CPU1_P1P0_DP<13>	13		
	7	QPI_CPU1_CPU0_P0P1_DN<7>	CV52	QPI1_DRX_DP<12>	QPI1_DTX_DP<12>	DE47	QPI_CPU0_CPU1_P1P0_DP<12>	12		
	8	QPI_CPU1_CPU0_P0P1_DN<8>	CU53	QPI1_DRX_DP<11>	QPI1_DTX_DP<11>	CU45	QPI_CPU0_CPU1_P1P0_DP<11>	11		
	9	QPI_CPU1_CPU0_P0P1_DN<9>	CK52	QPI1_DRX_DP<10>	QPI1_DTX_DP<10>	DB48	QPI_CPU0_CPU1_P1P0_DP<10>	10		
	10	QPI_CPU1_CPU0_P0P1_DN<10>	CJ53	QPI1_DRX_DP<9>	QPI1_DTX_DP<9>	DC49	QPI_CPU0_CPU1_P1P0_DP<9>	9		
	11	QPI_CPU1_CPU0_P0P1_DN<11>	CT56	QPI1_DRX_DP<8>	QPI1_DTX_DP<8>	CT46	QPI_CPU0_CPU1_P1P0_DP<8>	8		
	12	QPI_CPU1_CPU0_P0P1_DN<12>	CR57	QPI1_DRX_DP<7>	QPI1_DTX_DP<7>	DD50	QPI_CPU0_CPU1_P1P0_DP<7>	7		
	13	QPI_CPU1_CPU0_P0P1_DN<13>	CP58	QPI1_DRX_DP<6>	QPI1_DTX_DP<6>	DC51	QPI_CPU0_CPU1_P1P0_DP<6>	6		
	14	QPI_CPU1_CPU0_P0P1_DN<14>	CK54	QPI1_DRX_DP<5>	QPI1_DTX_DP<5>	CU47	QPI_CPU0_CPU1_P1P0_DP<5>	5		
	15	QPI_CPU1_CPU0_P0P1_DN<15>	CK56	QPI1_DRX_DP<4>	QPI1_DTX_DP<4>	DD52	QPI_CPU0_CPU1_P1P0_DP<4>	4		
	16	QPI_CPU1_CPU0_P0P1_DN<16>	CJ55	QPI1_DRX_DP<3>	QPI1_DTX_DP<3>	DA53	QPI_CPU0_CPU1_P1P0_DP<3>	3		
	17	QPI_CPU1_CPU0_P0P1_DN<17>	CD54	QPI1_DRX_DP<2>	QPI1_DTX_DP<2>	CU49	QPI_CPU0_CPU1_P1P0_DP<2>	2		
	18	QPI_CPU1_CPU0_P0P1_DN<18>	CD56	QPI1_DRX_DP<1>	QPI1_DTX_DP<1>	CT50	QPI_CPU0_CPU1_P1P0_DP<1>	1		
	19	QPI_CPU1_CPU0_P0P1_DN<19>	CC55	QPI1_DRX_DP<0>	QPI1_DTX_DP<0>	CT48	QPI_CPU0_CPU1_P1P0_DP<0>	0		
	0	QPI_CPU1_CPU0_P0P1_DN<0>	CN45	QPI1_DRX_DN<19>	QPI1_DTX_DN<19>	DD42	QPI_CPU0_CPU1_P1P0_DN<19>	19		
	1	QPI_CPU1_CPU0_P0P1_DN<1>	CM46	QPI1_DRX_DN<18>	QPI1_DTX_DN<18>	DC43	QPI_CPU0_CPU1_P1P0_DN<18>	18		
	2	QPI_CPU1_CPU0_P0P1_DN<2>	CN47	QPI1_DRX_DN<17>	QPI1_DTX_DN<17>	CW43	QPI_CPU0_CPU1_P1P0_DN<17>	17		
	3	QPI_CPU1_CPU0_P0P1_DN<3>	CM48	QPI1_DRX_DN<16>	QPI1_DTX_DN<16>	DD44	QPI_CPU0_CPU1_P1P0_DN<16>	16		
	4	QPI_CPU1_CPU0_P0P1_DP<4>	CL49	QPI1_DRX_DN<15>	QPI1_DTX_DN<15>	DC45	QPI_CPU0_CPU1_P1P0_DN<15>	15		
	5	QPI_CPU1_CPU0_P0P1_DP<5>	CK50	QPI1_DRX_DN<14>	QPI1_DTX_DN<14>	CV44	QPI_CPU0_CPU1_P1P0_DN<14>	14		
	6	QPI_CPU1_CPU0_P0P1_DP<6>	CL51	QPI1_DRX_DN<13>	QPI1_DTX_DN<13>	DD46	QPI_CPU0_CPU1_P1P0_DN<13>	13		
	7	QPI_CPU1_CPU0_P0P1_DP<7>	CT52	QPI1_DRX_DN<12>	QPI1_DTX_DN<12>	DC47	QPI_CPU0_CPU1_P1P0_DN<12>	12		
	8	QPI_CPU1_CPU0_P0P1_DP<8>	CR53	QPI1_DRX_DN<11>	QPI1_DTX_DN<11>	CW45	QPI_CPU0_CPU1_P1P0_DN<11>	11		
	9	QPI_CPU1_CPU0_P0P1_DP<9>	CM52	QPI1_DRX_DN<10>	QPI1_DTX_DN<10>	DD48	QPI_CPU0_CPU1_P1P0_DN<10>	10		
	10	QPI_CPU1_CPU0_P0P1_DP<10>	CL53	QPI1_DRX_DN<9>	QPI1_DTX_DN<9>	DE49	QPI_CPU0_CPU1_P1P0_DN<9>	9		
	11	QPI_CPU1_CPU0_P0P1_DP<11>	CV56	QPI1_DRX_DN<8>	QPI1_DTX_DN<8>	CV46	QPI_CPU0_CPU1_P1P0_DN<8>	8		
	12	QPI_CPU1_CPU0_P0P1_DP<12>	CU57	QPI1_DRX_DN<7>	QPI1_DTX_DN<7>	DB50	QPI_CPU0_CPU1_P1P0_DN<7>	7		
	13	QPI_CPU1_CPU0_P0P1_DP<13>	CT58	QPI1_DRX_DN<6>	QPI1_DTX_DN<6>	DE51	QPI_CPU0_CPU1_P1P0_DN<6>	6		
	14	QPI_CPU1_CPU0_P0P1_DP<14>	CM54	QPI1_DRX_DN<5>	QPI1_DTX_DN<5>	CW47	QPI_CPU0_CPU1_P1P0_DN<5>	5		
	15	QPI_CPU1_CPU0_P0P1_DP<15>	CM56	QPI1_DRX_DN<4>	QPI1_DTX_DN<4>	DB52	QPI_CPU0_CPU1_P1P0_DN<4>	4		
	16	QPI_CPU1_CPU0_P0P1_DP<16>	CL55	QPI1_DRX_DN<3>	QPI1_DTX_DN<3>	DC53	QPI_CPU0_CPU1_P1P0_DN<3>	3		
	17	QPI_CPU1_CPU0_P0P1_DP<17>	CF54	QPI1_DRX_DN<2>	QPI1_DTX_DN<2>	CW49	QPI_CPU0_CPU1_P1P0_DN<2>	2		
	18	QPI_CPU1_CPU0_P0P1_DP<18>	CF56	QPI1_DRX_DN<1>	QPI1_DTX_DN<1>	CV50	QPI_CPU0_CPU1_P1P0_DN<1>	1		
	19	QPI_CPU1_CPU0_P0P1_DP<19>	CE55	QPI1_DRX_DN<0>	QPI1_DTX_DN<0>	CV48	QPI_CPU0_CPU1_P1P0_DN<0>	0		
64> IN	QPI_CPU1_CPU0_P0P1_CLKA_DP		CR55	QPI1_CLKRX_DP	QPI1_CLKTX_DP	DB54	QPI_CPU0_CPU1_P1P0_CLKA_DP		OUT 64<	
64> IN	QPI_CPU1_CPU0_P0P1_CLKA_DN		CU55	QPI1_CLKRX_DN	QPI1_CLKTX_DN	CY54	QPI_CPU0_CPU1_P1P0_CLKA_DN		OUT 64<	

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CPU SOCKET 0 (10 OF 13)

DEPARTMENT: DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	SIZE: B	CODE: 34649	DOCUMENT NUMBER: 444359 / REV: 1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 42 OF 303

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P1V05_VCCP_CPU0

1.05

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SANDYBRIDGE_EP_EXT_D

CA29	VCC<207>	VCC<155>	BP10		
CA25	VCC<206>	VCC<154>	BN9		
BY40	VCC<205>	VCC<153>	BN7		
BY38	VCC<204>	VCC<152>	BN5		
BY36	VCC<203>	VCC<151>	BN3		
BY34	VCC<202>	VCC<150>	BN17		
BY32	VCC<201>	VCC<149>	BN15		
BY30	VCC<200>	VCC<148>	BN13		
BY28	VCC<199>	VCC<147>	BN11		
BY26	VCC<198>	VCC<146>	BN1		
BY18	VCC<197>	VCC<145>	BK8		
BV8	VCC<196>	VCC<144>	BK6		
BV6	VCC<195>	VCC<143>	BK4		
BV4	VCC<194>	VCC<142>	BK2		
BV2	VCC<193>	VCC<141>	BK16		
BV16	VCC<192>	VCC<140>	BK14		
BV14	VCC<191>	VCC<139>	BK12		
BV12	VCC<190>	VCC<138>	BK10		
BV10	VCC<189>	VCC<137>	BJ9		
BU9	VCC<188>	VCC<136>	BJ7		
BU7	VCC<187>	VCC<135>	BJ5		
BU5	VCC<186>	VCC<134>	BJ3		
BU3	VCC<185>	VCC<133>	BJ17		
BU17	VCC<184>	VCC<132>	BJ15		
BU15	VCC<183>	VCC<131>	BJ13		
BU13	VCC<182>	VCC<130>	BJ11		
BU11	VCC<181>	VCC<129>	BJ1		
BU1	VCC<180>	VCC<128>	BH8		
BT8	VCC<179>	VCC<127>	BH6		
BT6	VCC<178>	VCC<126>	BH4		
BT4	VCC<177>	VCC<125>	BH2		
BT2	VCC<176>	VCC<124>	BH16		
BT16	VCC<175>	VCC<123>	BH14		
BT14	VCC<174>	VCC<122>	BH12		
BT12	VCC<173>	VCC<121>	BH10		
BT10	VCC<172>	VCC<120>	BG9		
BR9	VCC<171>	VCC<119>	BG7		
BR7	VCC<170>	VCC<118>	BG5		
BR5	VCC<169>	VCC<117>	BG3		
BR3	VCC<168>	VCC<116>	BG17		
BR17	VCC<167>	VCC<115>	BG15		
BR15	VCC<166>	VCC<114>	BG13		
BR13	VCC<165>	VCC<113>	BG11		
BR11	VCC<164>	VCC<112>	BG1		
BR1	VCC<163>	VCC<111>	BF8		
BP8	VCC<162>	VCC<110>	BF6		
BP6	VCC<161>	VCC<109>	BF4		
BP4	VCC<160>	VCC<108>	BF2		
BP2	VCC<159>	VCC<107>	BF16		
BP16	VCC<158>	VCC<106>	BF14		
BP14	VCC<157>	VCC<105>	BF12		
BP12	VCC<156>	VCC<104>	BF10		

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P1V05_VCCP_CPU0

1.05

P1V05_VCCP_CPU0

1.05

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SANDYBRIDGE_EP_EXT_D

BE9	VCC<103>	VCC<51>	AU7
BE7	VCC<102>	VCC<50>	AU5
BE5	VCC<101>	VCC<49>	AU3
BE3	VCC<100>	VCC<48>	AU17
BE17	VCC<99>	VCC<47>	AU15
BE15	VCC<98>	VCC<46>	AU13
BE13	VCC<97>	VCC<45>	AU11
BE11	VCC<96>	VCC<44>	AU1
BE1	VCC<95>	VCC<43>	AP8
BB8	VCC<94>	VCC<42>	AP6
BB6	VCC<93>	VCC<41>	AP4
BB4	VCC<92>	VCC<40>	AP2
BB2	VCC<91>	VCC<39>	AP16
BB16	VCC<90>	VCC<38>	AP14
BB14	VCC<89>	VCC<37>	AP12
BB12	VCC<88>	VCC<36>	AP10
BB10	VCC<87>	VCC<35>	AN9
BA9	VCC<86>	VCC<34>	AN7
BA7	VCC<85>	VCC<33>	AN5
BA5	VCC<84>	VCC<32>	AN3
BA3	VCC<83>	VCC<31>	AN17
BA17	VCC<82>	VCC<30>	AN15
BA15	VCC<81>	VCC<29>	AN13
BA13	VCC<80>	VCC<28>	AN11
BA11	VCC<79>	VCC<27>	AN1
BA1	VCC<78>	VCC<26>	AM8
AY8	VCC<77>	VCC<25>	AM6
AY6	VCC<76>	VCC<24>	AM4
AY4	VCC<75>	VCC<23>	AM2
AY2	VCC<74>	VCC<22>	AM16
AY16	VCC<73>	VCC<21>	AM14
AY14	VCC<72>	VCC<20>	AM12
AY12	VCC<71>	VCC<19>	AM10
AY10	VCC<70>	VCC<18>	AL9
AW9	VCC<69>	VCC<17>	AL7
AW7	VCC<68>	VCC<16>	AL5
AW5	VCC<67>	VCC<15>	AL3
AW3	VCC<66>	VCC<14>	AL17
AW17	VCC<65>	VCC<13>	AL15
AW15	VCC<64>	VCC<12>	AL13
AW13	VCC<63>	VCC<11>	AL11
AW11	VCC<62>	VCC<10>	AL1
AW1	VCC<61>	VCC<9>	AG41
AV8	VCC<60>	VCC<8>	AG39
AV6	VCC<59>	VCC<7>	AG37
AV4	VCC<58>	VCC<6>	AG35
AV2	VCC<57>	VCC<5>	AG33
AV16	VCC<56>	VCC<4>	AG31
AV14	VCC<55>	VCC<3>	AG29
AV12	VCC<54>	VCC<2>	AG27
AV10	VCC<53>	VCC<1>	AG25
AU9	VCC<52>	VCC<0>	AG19

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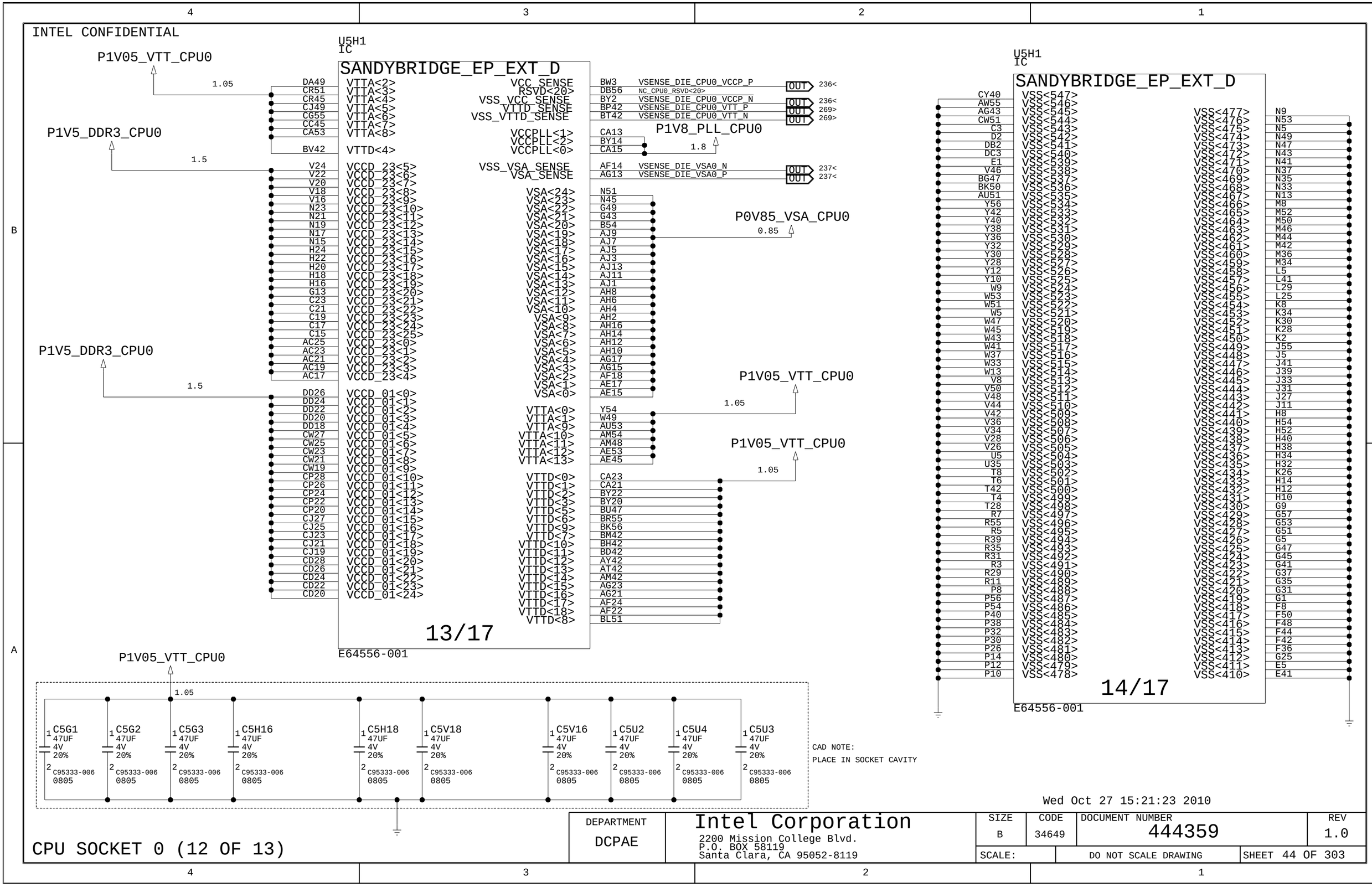
E64556-001

Wed Oct 27 15:21:22 2010

CPU SOCKET 0 (11 OF 13)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 43 OF 303	

INTEL CONFIDENTIAL



CPU SOCKET 0 (12 OF 13)

Wed Oct 27 15:21:23 2010

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 44 OF 303

INTEL CONFIDENTIAL

U5H1
IC

SANDYBRIDGE_EP_EXT_D

E31	VSS<409>	VSS<341>	CV34
E3	VSS<408>	VSS<340>	CV32
E29	VSS<407>	VSS<339>	CV30
DF8	VSS<406>	VSS<338>	CV18
DF52	VSS<405>	VSS<337>	CV14
DF50	VSS<404>	VSS<336>	CU5
DF48	VSS<403>	VSS<335>	CU35
DF46	VSS<402>	VSS<334>	CU3
DF44	VSS<401>	VSS<333>	CU11
DF42	VSS<400>	VSS<332>	CU1
DF36	VSS<399>	VSS<331>	CT42
DF12	VSS<398>	VSS<330>	CT28
DE7	VSS<397>	VSS<329>	CR9
DE53	VSS<396>	VSS<328>	CR5
DE41	VSS<395>	VSS<327>	CR49
DE17	VSS<394>	VSS<326>	CR47
DD6	VSS<393>	VSS<325>	CR35
DD38	VSS<392>	VSS<324>	CR11
DD36	VSS<391>	VSS<323>	CP56
DD34	VSS<390>	VSS<322>	CP52
DD14	VSS<389>	VSS<321>	CP48
DD12	VSS<388>	VSS<320>	CP46
DD10	VSS<387>	VSS<319>	CP44
DC5	VSS<386>	VSS<318>	CP40
DC41	VSS<385>	VSS<317>	CP36
DB58	VSS<384>	VSS<316>	CP16
		VSS<315>	CP12
DB36	VSS<383>	VSS<314>	CN9
DB32	VSS<382>	VSS<313>	CN7
DB12	VSS<381>	VSS<312>	CN57
DA9	VSS<380>	VSS<311>	CN55
DA51	VSS<379>	VSS<310>	CN53
DA5	VSS<378>	VSS<309>	CN5
DA47	VSS<377>	VSS<308>	CP42
DA45	VSS<376>	VSS<307>	CN39
DA43	VSS<375>	VSS<306>	CN37
DA41	VSS<374>	VSS<305>	CN35
DA3	VSS<373>	VSS<304>	CN33
DA11	VSS<372>	VSS<303>	CN31
D8	VSS<371>	VSS<302>	CN3
D36	VSS<370>	VSS<301>	CN17
D26	VSS<369>	VSS<300>	CN15
CY8	VSS<368>	VSS<299>	CN13
CY50	VSS<367>	VSS<298>	CN11
CY44	VSS<366>	VSS<297>	CM8
CY36	VSS<365>	VSS<296>	CM6
CY2	VSS<364>	VSS<295>	CM42
CY16	VSS<363>	VSS<294>	CM40
CY12	VSS<362>	VSS<293>	CM38
CY10	VSS<361>	VSS<292>	CM36
CW7	VSS<360>	VSS<291>	CM34
CW57	VSS<359>	VSS<290>	CM32
CW55	VSS<358>	VSS<289>	CM30
CW53	VSS<357>	VSS<288>	CM14
CW5	VSS<356>	VSS<287>	CM10
CW39	VSS<355>	VSS<286>	CL5
CW37	VSS<354>	VSS<285>	CL43
CW35	VSS<353>	VSS<284>	CL17
CW33	VSS<352>	VSS<283>	CK6
CW31	VSS<351>	VSS<282>	CK4
CW29	VSS<350>	VSS<281>	CK36
CW15	VSS<349>	VSS<280>	CK10
CW13	VSS<348>	VSS<279>	CJ9
CW11	VSS<347>	VSS<278>	CJ51
CV6	VSS<346>	VSS<277>	CJ47
CV58	VSS<345>	VSS<276>	CJ45
CV54	VSS<344>	VSS<275>	CJ43
CV42	VSS<343>	VSS<274>	CJ3
CV38	VSS<342>		

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U5H1
IC

SANDYBRIDGE_EP_EXT_D

CJ29	VSS<273>	VSS<205>	C55
CJ17	VSS<272>	VSS<204>	C5
CJ11	VSS<271>	VSS<203>	C41
CH6	VSS<270>	VSS<202>	C39
CP50	VSS<269>	VSS<201>	C33
CH54	VSS<268>	VSS<200>	C13
CH52	VSS<267>	VSS<199>	C11
CH50	VSS<266>	VSS<198>	BY8
CH48	VSS<265>	VSS<197>	BY58
CH46	VSS<264>	VSS<196>	BY42
CH44	VSS<263>	VSS<195>	BY4
CH36	VSS<262>	VSS<194>	BY24
CH16	VSS<261>	VSS<193>	BW7
CH12	VSS<260>	VSS<192>	BW5
CG9	VSS<259>	VSS<191>	BW17
CG53	VSS<258>	VSS<190>	BW15
CG43	VSS<257>	VSS<189>	BW13
CG41	VSS<256>	VSS<188>	BW11
CG39	VSS<255>	VSS<187>	BW1
CG37	VSS<254>	VSS<186>	BU51
CG35	VSS<253>	VSS<185>	BU45
CG33	VSS<252>	VSS<184>	BT56
CG31	VSS<251>	VSS<183>	BT54
CG15	VSS<250>	VSS<182>	BT52
CF6	VSS<249>	VSS<181>	BT50
CF42	VSS<248>	VSS<180>	BT48
CF40	VSS<247>	VSS<179>	BT46
CF38	VSS<246>	VSS<178>	B52
CF36	VSS<245>	VSS<177>	BR57
CF34	VSS<244>	VSS<176>	BR53
CF32	VSS<243>	VSS<175>	BP58
CF30	VSS<242>	VSS<174>	BN45
CF14	VSS<241>	VSS<173>	BN43
CF12	VSS<240>	VSS<172>	BM8
CE9	VSS<239>	VSS<171>	BM6
CE5	VSS<238>	VSS<170>	BK42
CE13	VSS<237>	VSS<169>	BM4
CD6	VSS<236>	VSS<168>	BM2
CD36	VSS<235>	VSS<167>	BM16
CD18	VSS<234>	VSS<166>	BM14
CC9	VSS<233>	VSS<165>	BM12
CC49	VSS<232>	VSS<164>	BM10
CC47	VSS<231>	VSS<163>	BL9
CC43	VSS<230>	VSS<162>	BL7
CC3	VSS<229>	VSS<161>	BL5
CC29	VSS<228>	VSS<160>	BL49
CC13	VSS<227>	VSS<159>	BK48
CB8	VSS<226>	VSS<158>	BL3
CB6	VSS<225>	VSS<157>	BL17
CB56	VSS<224>	VSS<156>	BL15
CB52	VSS<223>	VSS<155>	BL13
CB50	VSS<222>	VSS<154>	BL11
CB48	VSS<221>	VSS<153>	BL1
CB46	VSS<220>	VSS<152>	BK54
CB36	VSS<219>	VSS<151>	BK52
CB16	VSS<218>	VSS<150>	BK46
CA57	VSS<217>	VSS<149>	BJ57
CA55	VSS<216>	VSS<148>	BJ55
CA5	VSS<215>	VSS<147>	BH58
CA41	VSS<214>	VSS<146>	BF44
CA39	VSS<213>	VSS<145>	BF42
CA37	VSS<212>	VSS<144>	BE51
CA35	VSS<211>	VSS<143>	BE49
CA33	VSS<210>	VSS<142>	BD8
CA31	VSS<209>	VSS<141>	BD6
CA27	VSS<208>	VSS<140>	BD56
CA19	VSS<207>	VSS<139>	BD54
CA11	VSS<206>	VSS<138>	BD4
		VSS<137>	BD2

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U5H1
IC

SANDYBRIDGE_EP_EXT_D

BD16	VSS<136>	VSS<68>	AK46
BD14	VSS<135>	VSS<67>	AK44
BD12	VSS<134>	VSS<66>	AK42
BD10	VSS<133>	VSS<65>	AK4
BC9	VSS<132>	VSS<64>	AK2
BC7	VSS<131>	VSS<63>	AK16
BC57	VSS<130>	VSS<62>	AK14
BC55	VSS<129>	VSS<61>	AK12
BC53	VSS<128>	VSS<60>	AK10
BC5	VSS<127>	VSS<59>	AJ17
BC45	VSS<126>	VSS<58>	AJ15
BC43	VSS<125>	VSS<57>	AH58
BC3	VSS<124>	VSS<56>	AG9
BC17	VSS<123>	VSS<55>	AG57
BC15	VSS<122>	VSS<54>	AG55
BC13	VSS<121>	VSS<53>	AG5
BC11	VSS<120>	VSS<52>	AG3
BC1	VSS<119>	VSS<51>	AG1
BB58	VSS<118>	VSS<50>	AF6
BB52	VSS<117>	VSS<49>	AF56
BB50	VSS<116>	VSS<48>	AF54
BB48	VSS<115>	VSS<47>	AF42
BB46	VSS<114>	VSS<46>	AF40
BB42	VSS<113>	VSS<45>	AF36
B8	VSS<112>	VSS<44>	AF34
B6	VSS<111>	VSS<43>	AF26
B36	VSS<110>	VSS<42>	AF20
AW57	VSS<109>	VSS<41>	AF16
AV56	VSS<108>	VSS<40>	AF12
AV54	VSS<107>	VSS<39>	AE9
AV42	VSS<106>	VSS<38>	AE51
AU49	VSS<105>	VSS<37>	AE49
AU47	VSS<104>	VSS<36>	AE47
AU45	VSS<103>	VSS<35>	AE43
AT8	VSS<102>	VSS<34>	AE39
AT6	VSS<101>	VSS<33>	AE31
AT52	VSS<100>	VSS<32>	AE29
AT46	VSS<99>	VSS<31>	AD6
AT4	VSS<98>	VSS<30>	AD52
AT2	VSS<97>	VSS<29>	AD50
AT16	VSS<96>	VSS<28>	AD48
AT14	VSS<95>	VSS<27>	AD46
AT12	VSS<94>	VSS<26>	AD44
AT10	VSS<93>	VSS<25>	AD42
AR9	VSS<92>	VSS<24>	AD36
AR7	VSS<91>	VSS<23>	AD34
AR5	VSS<90>	VSS<22>	AD26
AR3	VSS<89>	VSS<21>	AC9
AR17	VSS<88>	VSS<20>	AC31
AR15	VSS<87>	VSS<19>	AB6
AR13	VSS<86>	VSS<18>	AB42
AR11	VSS<85>	VSS<17>	AB36
AR1	VSS<84>	VSS<16>	AB14
AP58	VSS<83>	VSS<15>	AA9
AP44	VSS<82>	VSS<14>	AA55
AP42	VSS<81>	VSS<13>	AA5
AN57	VSS<80>	VSS<12>	AA39
AN55	VSS<79>	VSS<11>	AA31
AM56	VSS<78>	VSS<10>	AA3
AL53	VSS<77>	VSS<9>	AA29
AL51	VSS<76>	VSS<8>	AA11
AL49	VSS<75>	VSS<7>	A7
AL45	VSS<74>	VSS<6>	A51
AL43	VSS<73>	VSS<5>	A5
AK8	VSS<72>	VSS<4>	A49
AK6	VSS<71>	VSS<3>	A47
AK50	VSS<70>	VSS<2>	A45
AK48	VSS<69>	VSS<1>	A43
		VSS<0>	A41

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Wed Oct 27 15:21:23 2010

CPU SOCKET 0 (13 OF 13)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 45 OF 303	

INTEL CONFIDENTIAL

J6K2

CONN240_E55582004

34> IN	M_A_BA<2>	52	A16_BA2	DQ<63>	234 63
		15 171	A<15>	DQ<62>	233 62
		14 172	A<14>	DQ<61>	228 61
		13 196	A<13>	DQ<60>	227 60
		12 174	A<12>	DQ<59>	115 59
		11 55	A<11>	DQ<58>	114 58
		10 70	A<10>	DQ<57>	109 57
		9 175	A<9>	DQ<56>	108 56
		8 177	A<8>	DQ<55>	225 55
		7 56	A<7>	DQ<54>	224 54
		6 178	A<6>	DQ<53>	219 53
		5 58	A<5>	DQ<52>	218 52
		4 59	A<4>	DQ<51>	106 51
		3 180	A<3>	DQ<50>	105 50
		2 61	A<2>	DQ<49>	100 49
		1 181	A<1>	DQ<48>	99 48
34> IN	M_A_MA<15..0>	0 188	A<0>	DQ<47>	216 47
34> IN	M_A_BA<1..0>			DQ<46>	215 46
		1 190	BA<1>	DQ<45>	210 45
		0 71	BA<0>	DQ<44>	209 44
				DQ<43>	97 43
34> IN	M_A_CK_DP<2>	63	NC_CK1P	DQ<42>	96 42
34> IN	M_A_CK_DN<2>	64	NC_CK1N	DQ<41>	91 41
34> IN	M_A_CK_DP<0>	184	CK0P	DQ<40>	90 40
34> IN	M_A_CK_DN<0>	185	CK0N	DQ<39>	207 39
34> IN	M_A_CS_N<3..0>			DQ<38>	206 38
		3 198	CS<3>	DQ<37>	201 37
		2 79	CS<2>	DQ<36>	200 36
		1 76	CS<1>	DQ<35>	88 35
		0 193	CS<0>	DQ<34>	87 34
				DQ<33>	82 33
34> IN	M_A_CKE<1>	169	CKE<1>	DQ<32>	81 32
34> IN	M_A_CKE<0>	50	CKE<0>	DQ<31>	156 31
				DQ<30>	155 30
34> IN	M_A_WE_N	73	WE_N	DQ<29>	150 29
34> IN	M_A_RAS_N	192	RAS_N	DQ<28>	149 28
34> IN	M_A_CAS_N	74	CAS_N	DQ<27>	37 27
34> IN	M_A_ODT<1..0>			DQ<26>	36 26
		1 77	ODT<1>	DQ<25>	31 25
		0 195	ODT<0>	DQ<24>	30 24
				DQ<23>	147 23
34> IN	M_A_MA_PAR	68	PAR_IN_NC	DQ<22>	146 22
34< OUT	M_A_PAR_ERR_N<0>	53	ERR_OUT_NC	DQ<21>	141 21
34<> BI	M_A_ECC<7..0>			DQ<20>	140 20
		7 165	CB<7>	DQ<19>	28 19
		6 164	CB<6>	DQ<18>	27 18
		5 159	CB<5>	DQ<17>	22 17
		4 158	CB<4>	DQ<16>	21 16
		3 46	CB<3>	DQ<15>	138 15
		2 45	CB<2>	DQ<14>	137 14
		1 40	CB<1>	DQ<13>	132 13
		0 39	CB<0>	DQ<12>	131 12
				DQ<11>	19 11
47< 33> IN	M_AB_RESET_LVC1V5_N	168	RESET_N	DQ<10>	18 10
				DQ<9>	13 9
P3V3		236	VDDSPD	DQ<8>	12 8
		119	SA<2>	DQ<7>	129 7
3.3		237	SA<1>	DQ<6>	128 6
		117	SA<0>	DQ<5>	123 5
198> 50<> 47<> BI	SMB_DDR_AB_LVC3_SDA	238	SDA	DQ<4>	122 4
198<> 50< 47< IN	SMB_DDR_AB_LVC3_SCL	118	SCL	DQ<3>	10 3
LVCO3V3 100< OUT	FM_SKT0_DIMM_A1_EVENT_N	187	EVENT_N_NC	DQ<2>	9 2
46> 189>	P1V5_DDR3_CPU0_VREF_A_D	1	VREFDQ	DQ<1>	4 1
46> 50> 207< IN	P1V5_DDR3_CPU0_VREF_A_A	67	VREFCA	DQ<0>	3 0

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E55582-004

M_A_DQ<63..0> BI 34<>

SPD ADDRESS = 0XA0

EVENT_N: NO PU ON DIMM, NEEDS PU ON BOARD.
EVENT_N: INDICATES THAT A THERMAL EVENT HAS BEEN DETECTED IN THE THERMAL SENSING DEVICE (TS/SPD).

P1V5_DDR3_CPU0

R6J15 100 1% 1/16W 1.5
A93548-043 0402LF
0.75 P1V5_DDR3_CPU0_VREF_A_D OUT 46< 50>
R6J16 100 1% 1/16W
A93548-043 0402LF
C6J3 0.1UF 16V 10%
A36096-030 0402LF

P1V5_DDR3_CPU0

R6G2 100 1% 1/16W 1.5
A93548-043 0402LF
0.75 P1V5_DDR3_CPU0_VREF_A_A OUT 46<
R6G1 100 1% 1/16W
A93548-043 0402LF
C6G1 0.1UF 16V 10%
A36096-030 0402LF

J6K2

CONN240_E55582004

2	VSS<58>	VDD<21>	51	P1V5_DDR3_CPU0	1.5
5	VSS<57>	VDD<20>	54		
8	VSS<56>	VDD<19>	57		
11	VSS<55>	VDD<18>	60		
14	VSS<54>	VDD<17>	62		
17	VSS<53>	VDD<16>	65		
20	VSS<52>	VDD<15>	66		
23	VSS<51>	VDD<14>	69		
26	VSS<50>	VDD<13>	72		
29	VSS<49>	VDD<12>	75		
32	VSS<48>	VDD<11>	78		
35	VSS<47>	VDD<10>	170		
38	VSS<46>	VDD<9>	173		
41	VSS<45>	VDD<8>	176		
44	VSS<44>	VDD<7>	179		
47	VSS<43>	VDD<6>	182		
80	VSS<42>	VDD<5>	183		
83	VSS<41>	VDD<4>	186		
86	VSS<40>	VDD<3>	189	P0V75_VTT_DDR3_CPU0	
89	VSS<39>	VDD<2>	191		
92	VSS<38>	VDD<1>	194		
95	VSS<37>	VDD<0>	197		
98	VSS<36>				
101	VSS<35>	VTT<3>	49		0.75
104	VSS<34>	VTT<2>	48		
107	VSS<33>	VTT<1>	120		
110	VSS<32>	VTT<0>	240		
113	VSS<31>				
116	VSS<30>				
121	VSS<29>	NC_TEST	167	TP_A_D1_NC2	
124	VSS<28>				
127	VSS<27>				
130	VSS<26>				
133	VSS<25>				
136	VSS<24>				
139	VSS<23>				
142	VSS<22>				
145	VSS<21>				
148	VSS<20>				
151	VSS<19>				
154	VSS<18>				
157	VSS<17>				
160	VSS<16>				
163	VSS<15>				
166	VSS<14>				
199	VSS<13>				
202	VSS<12>				
205	VSS<11>				
208	VSS<10>				
211	VSS<9>				
214	VSS<8>				
217	VSS<7>				
220	VSS<6>				
223	VSS<5>				
226	VSS<4>				
229	VSS<3>				
232	VSS<2>				
235	VSS<1>				
239	VSS<0>				

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E55582-004

P1V5_DDR3_CPU0 1.5
C6H7 10UF 6.3V 20% 602433-075 0603LF
C6H6 10UF 6.3V 20% 602433-075 0603LF

J6K2

CONN240_E55582004

DQS17P_DM8	161	17	M_A_DQS_DP<17..0>	BI 34<>
DQS17N_NC	162	17	M_A_DQS_DN<17..0>	BI 34<>
DQS16P_DM7	230	16		
DQS16N_NC	231	16		
DQS15P_DM6	221	15		
DQS15N_NC	222	15		
DQS14P_DM5	212	14		
DQS14N_NC	213	14		
DQS13P_DM4	203	13		
DQS13N_NC	204	13		
DQS12P_DM3	152	12		
DQS12N_NC	153	12		
DQS11P_DM2	143	11		
DQS11N_NC	144	11		
DQS10P_DM1	134	10		
DQS10N_NC	135	10		
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DQS9N_NC	126	9		
DQS8P	43	8		
DQS8N	42	8		
DQS7P	112	7		
DQS7N	111	7		
DQS6P	103	6		
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DQS5P	94	5		
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DQS4P	85	4		
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DQS3N	33	3		
DQS2P	25	2		
DQS2N	24	2		
DQS1P	16	1		
DQS1N	15	1		
DQS0P	7	0		
DQS0N	6	0		

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E55582-004

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DDR3 CPU0 CHANNEL A DIMM1

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 46 OF 303	

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J6K1

CONN240_E55582004

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	14	172	A<14>	DQ<61>	228 61
	13	196	A<13>	DQ<60>	227 60
	12	174	A<12>	DQ<59>	115 59
	11	55	A<11>	DQ<58>	114 58
	10	70	A<10>	DQ<57>	109 57
	9	175	A<9>	DQ<56>	108 56
	8	177	A<8>	DQ<55>	225 55
	7	56	A<7>	DQ<54>	224 54
	6	178	A<6>	DQ<53>	219 53
	5	58	A<5>	DQ<52>	218 52
	4	59	A<4>	DQ<51>	106 51
	3	180	A<3>	DQ<50>	105 50
	2	61	A<2>	DQ<49>	100 49
	1	181	A<1>	DQ<48>	99 48
35> IN	M_B_MA<15..0>	0 188	A<0>	DQ<47>	216 47
35> IN	M_B_BA<1..0>			DQ<46>	215 46
	1	190	BA<1>	DQ<45>	210 45
	0	71	BA<0>	DQ<44>	209 44
				DQ<43>	97 43
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35> IN	M_B_CK_DN<2>	64	NC_CK1N	DQ<41>	91 41
35> IN	M_B_CK_DP<0>	184	CK0P	DQ<40>	90 40
35> IN	M_B_CK_DN<0>	185	CK0N	DQ<39>	207 39
35> IN	M_B_CS_N<3..0>			DQ<38>	206 38
	3	198	CS<3>	DQ<37>	201 37
	2	79	CS<2>	DQ<36>	200 36
	1	76	CS<1>	DQ<35>	88 35
	0	193	CS<0>	DQ<34>	87 34
				DQ<33>	82 33
35> IN	M_B_CKE<1>	169	CKE<1>	DQ<32>	81 32
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35> IN	M_B_WE_N	73	WE_N	DQ<29>	150 29
35> IN	M_B_RAS_N	192	RAS_N	DQ<28>	149 28
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				DQ<23>	147 23
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	5	159	CB<5>	DQ<17>	22 17
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	3	46	CB<3>	DQ<15>	138 15
	2	45	CB<2>	DQ<14>	137 14
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46< 33> IN	M_AB_RESET_LVC1V5_N	168	RESET_N	DQ<10>	18 10
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M_B_DQ<63..0> BI 35<>

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A93548-043 0402LF 0.75

P1V5_DDR3_CPU0_VREF_B_D OUT 47< 50>

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C6J5 0.1UF 16V 10%

A36096-030 0402LF

P1V5_DDR3_CPU0

R6H1 100 1% 1/16W 1.5

A93548-043 0402LF 0.75

P1V5_DDR3_CPU0_VREF_B_A OUT 47<

R6H2 100 1% 1/16W

C6H5 0.1UF 16V 10%

A36096-030 0402LF

J6K1

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	11	VSS<55>	VDD<18>	60	
	14	VSS<54>	VDD<17>	62	
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	44	VSS<44>	VDD<7>	179	
	47	VSS<43>	VDD<6>	182	
	80	VSS<42>	VDD<5>	183	
	83	VSS<41>	VDD<4>	186	
	86	VSS<40>	VDD<3>	189	
	89	VSS<39>	VDD<2>	191	
	92	VSS<38>	VDD<1>	194	
	95	VSS<37>	VDD<0>	197	
	98	VSS<36>			
	101	VSS<35>	VTT<3>	49	
	104	VSS<34>	VTT<2>	48	
	107	VSS<33>	VTT<1>	120	
	110	VSS<32>	VTT<0>	240	
	113	VSS<31>			
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	124	VSS<28>			
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	151	VSS<19>			
	154	VSS<18>			
	157	VSS<17>			
	160	VSS<16>			
	163	VSS<15>			
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	202	VSS<12>			
	205	VSS<11>			
	208	VSS<10>			
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	214	VSS<8>			
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	220	VSS<6>			
	223	VSS<5>			
	226	VSS<4>			
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	232	VSS<2>			
	235	VSS<1>			
	239	VSS<0>			

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P1V5_DDR3_CPU0

1.5

P0V75_VTT_DDR3_CPU0

0.75

P1V5_DDR3_CPU0

1.5

C6H11 10UF 6.3V 20% 602433-075 0603LF

C6H12 10UF 6.3V 20% 602433-075 0603LF

J6K1

CONN240_E55582004

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M_B_DQS_DN<17..0> BI 35<>

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DQS17N_NC	162		17	
DQS16P_DM7	230	16		
DQS16N_NC	231		16	
DQS15P_DM6	221	15		
DQS15N_NC	222		15	
DQS14P_DM5	212	14		
DQS14N_NC	213		14	
DQS13P_DM4	203	13		
DQS13N_NC	204		13	
DQS12P_DM3	152	12		
DQS12N_NC	153		12	
DQS11P_DM2	143	11		
DQS11N_NC	144		11	
DQS10P_DM1	134	10		
DQS10N_NC	135		10	
DQS9P_DM0	125	9		
DQS9N_NC	126		9	
DQS8P	43	8		
DQS8N	42		8	
DQS7P	112	7		
DQS7N	111		7	
DQS6P	103	6		
DQS6N	102		6	
DQS5P	94	5		
DQS5N	93		5	
DQS4P	85	4		
DQS4N	84		4	
DQS3P	34	3		
DQS3N	33		3	
DQS2P	25	2		
DQS2N	24		2	
DQS1P	16	1		
DQS1N	15		1	
DQS0P	7	0		
DQS0N	6		0	

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DDR3 CPU0 CHANNEL B DIMM1

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 47 OF 303

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J4F2

CONN240_E55582004

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		12 174	A<12>	DQ<59>	115	59	
		11 55	A<11>	DQ<58>	114	58	
		10 70	A<10>	DQ<57>	109	57	
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		8 177	A<8>	DQ<55>	225	55	
		7 56	A<7>	DQ<54>	224	54	
		6 178	A<6>	DQ<53>	219	53	
		5 58	A<5>	DQ<52>	218	52	
		4 59	A<4>	DQ<51>	106	51	
		3 180	A<3>	DQ<50>	105	50	
		2 61	A<2>	DQ<49>	100	49	
		1 181	A<1>	DQ<48>	99	48	
36> IN	M_C_MA<15..0>	0 188	A<0>	DQ<47>	216	47	
36> IN	M_C_BA<1..0>			DQ<46>	215	46	
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36> IN	M_C_CK_DN<0>	185	CK0N	DQ<39>	207	39	
36> IN	M_C_CS_N<3..0>			DQ<38>	206	38	
		3 198	CS<3>	DQ<37>	201	37	
		2 79	CS<2>	DQ<36>	200	36	
		1 76	CS<1>	DQ<35>	88	35	
		0 193	CS<0>	DQ<34>	87	34	
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36> IN	M_C_CKE<1>	169	CKE<1>	DQ<32>	81	32	
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36> IN	M_C_RAS_N	192	RAS_N	DQ<28>	149	28	
36> IN	M_C_CAS_N	74	CAS_N	DQ<27>	37	27	
36> IN	M_C_ODT<1..0>			DQ<26>	36	26	
		1 77	ODT<1>	DQ<25>	31	25	
		0 195	ODT<0>	DQ<24>	30	24	
				DQ<23>	147	23	
36> IN	M_C_MA_PAR	68	PAR_IN_NC	DQ<22>	146	22	
36< OUT	M_C_PAR_ERR_N<0>	53	ERR_OUT_NC	DQ<21>	141	21	
36<> BI	M_C_ECC<7..0>			DQ<20>	140	20	
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		3 46	CB<3>	DQ<15>	138	15	
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198> 50<> 49<> BI	SMB_DDR_CD_LVC3_SDA	238	SDA	DQ<4>	122	4	
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J4F2

CONN240_E55582004

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23	VSS<51>	VDD<14>	69
26	VSS<50>	VDD<13>	72
29	VSS<49>	VDD<12>	75
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35	VSS<47>	VDD<10>	170
38	VSS<46>	VDD<9>	173
41	VSS<45>	VDD<8>	176
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80	VSS<42>	VDD<5>	183
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86	VSS<40>	VDD<3>	189
89	VSS<39>	VDD<2>	191
92	VSS<38>	VDD<1>	194
95	VSS<37>	VDD<0>	197
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104	VSS<34>	VTT<2>	48
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110	VSS<32>	VTT<0>	240
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124	VSS<28>		
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P1V5_DDR3_CPU0

1.5

P0V75_VTT_DDR3_CPU0

0.75

P1V5_DDR3_CPU0

1.5

C4H11 10UF 6.3V 20% 602433-075 0603LF

C4H14 10UF 6.3V 20% 602433-075 0603LF

J4F2

CONN240_E55582004

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DQS14P_DM5	212	14		
DQS14N_NC	213	14		
DQS13P_DM4	203	13		
DQS13N_NC	204	13		
DQS12P_DM3	152	12		
DQS12N_NC	153	12		
DQS11P_DM2	143	11		
DQS11N_NC	144	11		
DQS10P_DM1	134	10		
DQS10N_NC	135	10		
DQS9P_DM0	125	9		
DQS9N_NC	126	9		
DQS8P	43	8		
DQS8N	42	8		
DQS7P	112	7		
DQS7N	111	7		
DQS6P	103	6		
DQS6N	102	6		
DQS5P	94	5		
DQS5N	93	5		
DQS4P	85	4		
DQS4N	84	4		
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DQS3N	33	3		
DQS2P	25	2		
DQS2N	24	2		
DQS1P	16	1		
DQS1N	15	1		
DQS0P	7	0		
DQS0N	6	0		

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P1V5_DDR3_CPU0

R4G3 100 1% 1/16W 1.5

A93548-043 0402LF

0.75

P1V5_DDR3_CPU0_VREF_C_D OUT 48< 50>

R4G2 100 1% 1/16W

C4G1 0.1UF 16V 10%

A93548-043 0402LF

A36096-030 0402LF

P1V5_DDR3_CPU0

R4J12 100 1% 1/16W 1.5

A93548-043 0402LF

0.75

P1V5_DDR3_CPU0_VREF_C_A OUT 48<

R4J11 100 1% 1/16W

C4J4 0.1UF 16V 10%

A93548-043 0402LF

A36096-030 0402LF

Wed Oct 27 15:22:12 2010

DDR3 CPU0 CHANNEL C DIMM1

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 48 OF 303	

INTEL CONFIDENTIAL

J4F3

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			12 174	A<12>	DQ<59>	115	59
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			10 70	A<10>	DQ<57>	109	57
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			8 177	A<8>	DQ<55>	225	55
			7 56	A<7>	DQ<54>	224	54
			6 178	A<6>	DQ<53>	219	53
			5 58	A<5>	DQ<52>	218	52
			4 59	A<4>	DQ<51>	106	51
			3 180	A<3>	DQ<50>	105	50
			2 61	A<2>	DQ<49>	100	49
			1 181	A<1>	DQ<48>	99	48
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37>	IN	M_D_BA<1..0>			DQ<46>	215	46
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			0 71	BA<0>	DQ<44>	209	44
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37>	IN	M_D_CK_DP<2>	63	NC_CK1P	DQ<42>	96	42
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37>	IN	M_D_CK_DP<0>	184	CK0P	DQ<40>	90	40
37>	IN	M_D_CK_DN<0>	185	CK0N	DQ<39>	207	39
37>	IN	M_D_CS_N<3..0>			DQ<38>	206	38
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			2 79	CS<2>	DQ<36>	200	36
			1 76	CS<1>	DQ<35>	88	35
			0 193	CS<0>	DQ<34>	87	34
					DQ<33>	82	33
37>	IN	M_D_CKE<1>	169	CKE<1>	DQ<32>	81	32
37>	IN	M_D_CKE<0>	50	CKE<0>	DQ<31>	156	31
					DQ<30>	155	30
37>	IN	M_D_WE_N	73	WE_N	DQ<29>	150	29
37>	IN	M_D_RAS_N	192	RAS_N	DQ<28>	149	28
37>	IN	M_D_CAS_N	74	CAS_N	DQ<27>	37	27
37>	IN	M_D_ODT<1..0>			DQ<26>	36	26
			1 77	ODT<1>	DQ<25>	31	25
			0 195	ODT<0>	DQ<24>	30	24
					DQ<23>	147	23
37>	IN	M_D_MA_PAR	68	PAR_IN_NC	DQ<22>	146	22
37<	OUT	M_D_PAR_ERR_N<0>	53	ERR_OUT_NC	DQ<21>	141	21
37<>	BI	M_D_ECC<7..0>			DQ<20>	140	20
			7 165	CB<7>	DQ<19>	28	19
			6 164	CB<6>	DQ<18>	27	18
			5 159	CB<5>	DQ<17>	22	17
			4 158	CB<4>	DQ<16>	21	16
			3 46	CB<3>	DQ<15>	138	15
			2 45	CB<2>	DQ<14>	137	14
			1 40	CB<1>	DQ<13>	132	13
			0 39	CB<0>	DQ<12>	131	12
					DQ<11>	19	11
48< 33>	IN	M_CD_RESET_LVC1V5_N	168	RESET_N	DQ<10>	18	10
					DQ<9>	13	9
SPD ADDRESS = 0XA8			236	VDDSPD	DQ<8>	12	8
			119	SA<2>	DQ<7>	129	7
			237	SA<1>	DQ<6>	128	6
			117	SA<0>	DQ<5>	123	5
198> 50<> 48<>	BI	SMB_DDR_CD_LVC3_SDA	238	SDA	DQ<4>	122	4
198<> 50< 48<	IN	SMB_DDR_CD_LVC3_SCL	118	SCL	DQ<3>	10	3
207< 189> 100<	OUT	FM_SKT0_DIMM_D1_EVENT_N	187	EVENT_N_NC	DQ<2>	9	2
50> 49>	IN	P1V5_DDR3_CPU0_VREF_D_D	1	VREFDQ	DQ<1>	4	1
49>	IN	P1V5_DDR3_CPU0_VREF_D_A	67	VREFCA	DQ<0>	3	0

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M_D_DQ<63..0> BI 37<>

P3V3 3.3

R4K16 1K 1% 0402LF 1/16W A93548-023 (M_D_SA<2>)

P1V5_DDR3_CPU0

R4G1 100 1% 1/16W A93548-043 0402LF 1.5 0.75

R4F1 100 1% 1/16W A93548-043 0402LF

C4F3 0.1UF 16V 10% A36096-030 0402LF

P1V5_DDR3_CPU0_VREF_D_D OUT 49< 50>

P1V5_DDR3_CPU0

R4J2 100 1% 1/16W A93548-043 0402LF 1.5 0.75

R4J1 100 1% 1/16W A93548-043 0402LF

C4J2 0.1UF 16V 10% A36096-030 0402LF

P1V5_DDR3_CPU0_VREF_D_A OUT 49<

J4F3

CONN240_E55582004

			2	VSS<58>	VDD<21>	51	
			5	VSS<57>	VDD<20>	54	
			8	VSS<56>	VDD<19>	57	
			11	VSS<55>	VDD<18>	60	
			14	VSS<54>	VDD<17>	62	
			17	VSS<53>	VDD<16>	65	
			20	VSS<52>	VDD<15>	66	
			23	VSS<51>	VDD<14>	69	
			26	VSS<50>	VDD<13>	72	
			29	VSS<49>	VDD<12>	75	
			32	VSS<48>	VDD<11>	78	
			35	VSS<47>	VDD<10>	170	
			38	VSS<46>	VDD<9>	173	
			41	VSS<45>	VDD<8>	176	
			44	VSS<44>	VDD<7>	179	
			47	VSS<43>	VDD<6>	182	
			80	VSS<42>	VDD<5>	183	
			83	VSS<41>	VDD<4>	186	
			86	VSS<40>	VDD<3>	189	
			89	VSS<39>	VDD<2>	191	
			92	VSS<38>	VDD<1>	194	
			95	VSS<37>	VDD<0>	197	
			98	VSS<36>			
			101	VSS<35>	VTT<3>	49	
			104	VSS<34>	VTT<2>	48	
			107	VSS<33>	VTT<1>	120	
			110	VSS<32>	VTT<0>	240	
			113	VSS<31>			
			116	VSS<30>			
			121	VSS<29>	NC_TEST	167	TP_D_D1_NC2
			124	VSS<28>			
			127	VSS<27>			
			130	VSS<26>			
			133	VSS<25>			
			136	VSS<24>			
			139	VSS<23>			
			142	VSS<22>			
			145	VSS<21>			
			148	VSS<20>			
			151	VSS<19>			
			154	VSS<18>			
			157	VSS<17>			
			160	VSS<16>			
			163	VSS<15>			
			166	VSS<14>			
			199	VSS<13>			
			202	VSS<12>			
			205	VSS<11>			
			208	VSS<10>			
			211	VSS<9>			
			214	VSS<8>			
			217	VSS<7>			
			220	VSS<6>			
			223	VSS<5>			
			226	VSS<4>			
			229	VSS<3>			
			232	VSS<2>			
			235	VSS<1>			
			239	VSS<0>			

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P1V5_DDR3_CPU0 1.5

C4H12 10UF 6.3V 20% 602433-075 0603LF

C4H13 10UF 6.3V 20% 602433-075 0603LF

P0V75_VTT_DDR3_CPU0 0.75

J4F3

CONN240_E55582004

	M_D_DQS_DP<17..0>	BI	37<>
	M_D_DQS_DN<17..0>	BI	37<>
DQS17P_DM8	161	17	
DQS17N_NC	162		17
DQS16P_DM7	230	16	
DQS16N_NC	231		16
DQS15P_DM6	221	15	
DQS15N_NC	222		15
DQS14P_DM5	212	14	
DQS14N_NC	213		14
DQS13P_DM4	203	13	
DQS13N_NC	204		13
DQS12P_DM3	152	12	
DQS12N_NC	153		12
DQS11P_DM2	143	11	
DQS11N_NC	144		11
DQS10P_DM1	134	10	
DQS10N_NC	135		10
DQS9P_DM0	125	9	
DQS9N_NC	126		9
DQS8P	43	8	
DQS8N	42		8
DQS7P	112	7	
DQS7N	111		7
DQS6P	103	6	
DQS6N	102		6
DQS5P	94	5	
DQS5N	93		5
DQS4P	85	4	
DQS4N	84		4
DQS3P	34	3	
DQS3N	33		3
DQS2P	25	2	
DQS2N	24		2
DQS1P	16	1	
DQS1N	15		1
DQS0P	7	0	
DQS0N	6		0

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DDR3 CPU0 CHANNEL D DIMM1

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 49 OF 303	

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ROOM = VREFDQ_CPU0

DDR3 PROCESSOR VREF GENERATION

P3V3_AUX NEEDED FOR POT
IF DESIGN SUPPORT S3

P3V3 3.3

C7F2 0.1UF 0402LF 16V X7R 10% A36096-030

DECOUPLING CAP
CAD NOTE:
PLACE CLOSE TO CHIP

R7F4 0 CHIP A93549-001 0402LF 5% 1/16W

198<> 47< 46< IN SMB_DDR_AB_LVC3_SCL — SMB_DDR_AB_DAC_LVC3_SCL

47<> 46<> 198> BI SMB_DDR_AB_LVC3_SDA — SMB_DDR_AB_DAC_LVC3_SDA

R7F3 0 CHIP A93549-001 0402LF 5% 1/16W

U7F2 ISL90727 E47385-001
VCC, SCL, SDA, GND, RW, RH

SMBUS ADDRESS=0X5C

CONNECTION TO THE P1V5_DDR3_CPU0
VOLTAGE RAIL SHOULD BE NEAR THE
P1V5_DDR3VR SENSE POINT

P1V5_DDR3_CPU0 1.5

P1V5_DDR3_CPU0_VREF_AB_RW 0.75

R7F7 12.1K 1% 1/16W CHIP 0402LF A93548-018

R7F5 12.1K 1% 1/16W 0402LF A93548-018

DECOUPLING CAP
CAD NOTE:
PLACE CLOSE TO CHIP

P5V

C4T3 1UF 16V 10% X5R 644066-061 0805LF

P5V_AUX NEEDED FOR OP AMP
IF DESIGN SUPPORT S3

REVIEW DATASHEET OF OPAMP FOR CORRECT DECOUPLING VALUES

WRITE VREF FROM CPU TO THE DIMMS

33> IN P1V5_DDR3_AB_VREFDQTX

R4T10 0 A93549-001 0402LF 5% 1/16W VREFDQ_CPU0

P1V5_DDR3_CPU0_VREF_AB_OPFB

U6F3 LMV321 E21441-001 VREFDQ_CPU0
INN, INP, VSN, VSP, OUT

R6F4 2.20 CHIP A93549-051 0402LF 5% 1/16W

P1V5_DDR3_CPU0_VREF_AB_D 0.75

R6F19 100 1% 1/16W CHIP 0402LF A93549-043

C6F2 1.0UF 6.3V 10% EMPTY A36096-027 0402LF

R4T11 0 CHIP A93549-001 0402LF 5% 1/16W

P1V5_DDR3_CPU0_VREF_A_D 0.75 OUT 46< 46>

R6F6 0 CHIP A93549-001 0402LF 5% 1/16W

P1V5_DDR3_CPU0_VREF_B_D 0.75 OUT 47> 47<

P1V5_DDR3_CPU0

R6J1 100 1% 1/16W A93548-043 0402LF 1.5

CAD NOTE:
PLACE CIRCUIT AS CLOSE AS POSSBIBLE TO CPU
REFER TO RS-ROMLEY PDG FOR LATEST GUIDELINE
FROM ROMLEY PDG:
NOMIMAL TRACE WIDTH = 10 MILS
NOMIMAL TRACE SPACING = 20 MILS
CPU BREAKOUT REQ = 4-MIL WIDTH / 4-MIL SPACING
THE DECOUPLING CAP RECOMMENDED IS 0603 0.1UF

0.75 P1V5_DDR3_AB_VREFDQRX OUT 33<

R6J2 100 1% 1/16W A93548-043 0402LF

C6J1 0.1UF 16V 10% A36096-030 0402LF

CPU0 DDR3 DQ REFERENCE

P3V3_AUX NEEDED FOR POT
IF DESIGN SUPPORT S3

P3V3 3.3

C3J3 0.1UF 0402LF 16V X7R 10% A36096-030

DECOUPLING CAP
CAD NOTE:
PLACE CLOSE TO CHIP

R3J19 0 CHIP A93549-001 0402LF 5% 1/16W

198<> 49< 48< IN SMB_DDR_CD_LVC3_SCL — SMB_DDR_CD_DAC_LVC3_SCL

49<> 48<> 198> BI SMB_DDR_CD_LVC3_SDA — SMB_DDR_CD_DAC_LVC3_SDA

R3J18 0 CHIP A93549-001 0402LF 5% 1/16W

U3J2 ISL90727 E47385-001
VCC, SCL, SDA, GND, RW, RH

SMBUS ADDRESS=0X5C

CONNECTION TO THE P1V5_DDR3_CPU0
VOLTAGE RAIL SHOULD BE NEAR THE
P1V5_DDR3VR SENSE POINT

P1V5_DDR3_CPU0 1.5

P1V5_DDR3_CPU0_VREF_CD_RW 0.75

R3J24 12.1K 1% 1/16W CHIP 0402LF A93548-018

R3J22 12.1K 1% 1/16W 0402LF A93548-018

DECOUPLING CAP
CAD NOTE:
PLACE CLOSE TO CHIP

P5V

C3J8 1UF 16V 10% X5R 644066-061 0805LF

P5V_AUX NEEDED FOR OP AMP
IF DESIGN SUPPORT S3

REVIEW DATASHEET OF OPAMP FOR CORRECT DECOUPLING VALUES

WRITE VREF FROM CPU TO THE DIMMS

33> IN P1V5_DDR3_CD_VREFDQTX

R3J21 0 A93549-001 0402LF 5% 1/16W VREFDQ_CPU0

P1V5_DDR3_CPU0_VREF_CD_OPFB

U3J1 LMV321 E21441-001 VREFDQ_CPU0
INN, INP, VSN, VSP, OUT

R3J20 2.20 CHIP A93549-051 0402LF 5% 1/16W

P1V5_DDR3_CPU0_VREF_CD_D 0.75

R3J16 100 1% 1/16W CHIP 0402LF A93548-043

C3J6 1.0UF 6.3V 10% EMPTY A36096-027 0402LF

R3J25 0 CHIP A93549-001 0402LF 5% 1/16W

P1V5_DDR3_CPU0_VREF_C_D 0.75 OUT 48< 48>

R3J26 0 CHIP A93549-001 0402LF 5% 1/16W

P1V5_DDR3_CPU0_VREF_D_D 0.75 OUT 49< 49>

P1V5_DDR3_CPU0

R4J3 100 1% 1/16W A93548-043 0402LF 1.5

CAD NOTE:
PLACE CIRCUIT AS CLOSE AS POSSBIBLE TO CPU
REFER TO RS-ROMLEY PDG FOR LATEST GUIDELINE
FROM ROMLEY PDG:
NOMIMAL TRACE WIDTH = 10 MILS
NOMIMAL TRACE SPACING = 20 MILS
CPU BREAKOUT REQ = 4-MIL WIDTH / 4-MIL SPACING
THE DECOUPLING CAP RECOMMENDED IS 0603 0.1UF

0.75 P1V5_DDR3_CD_VREFDQRX OUT 33<

R4J6 100 1% 1/16W A93548-043 0402LF

C4J3 0.1UF 16V 10% A36096-030 0402LF

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		SCALE:	DO NOT SCALE DRAWING	SHEET 50 OF 303	

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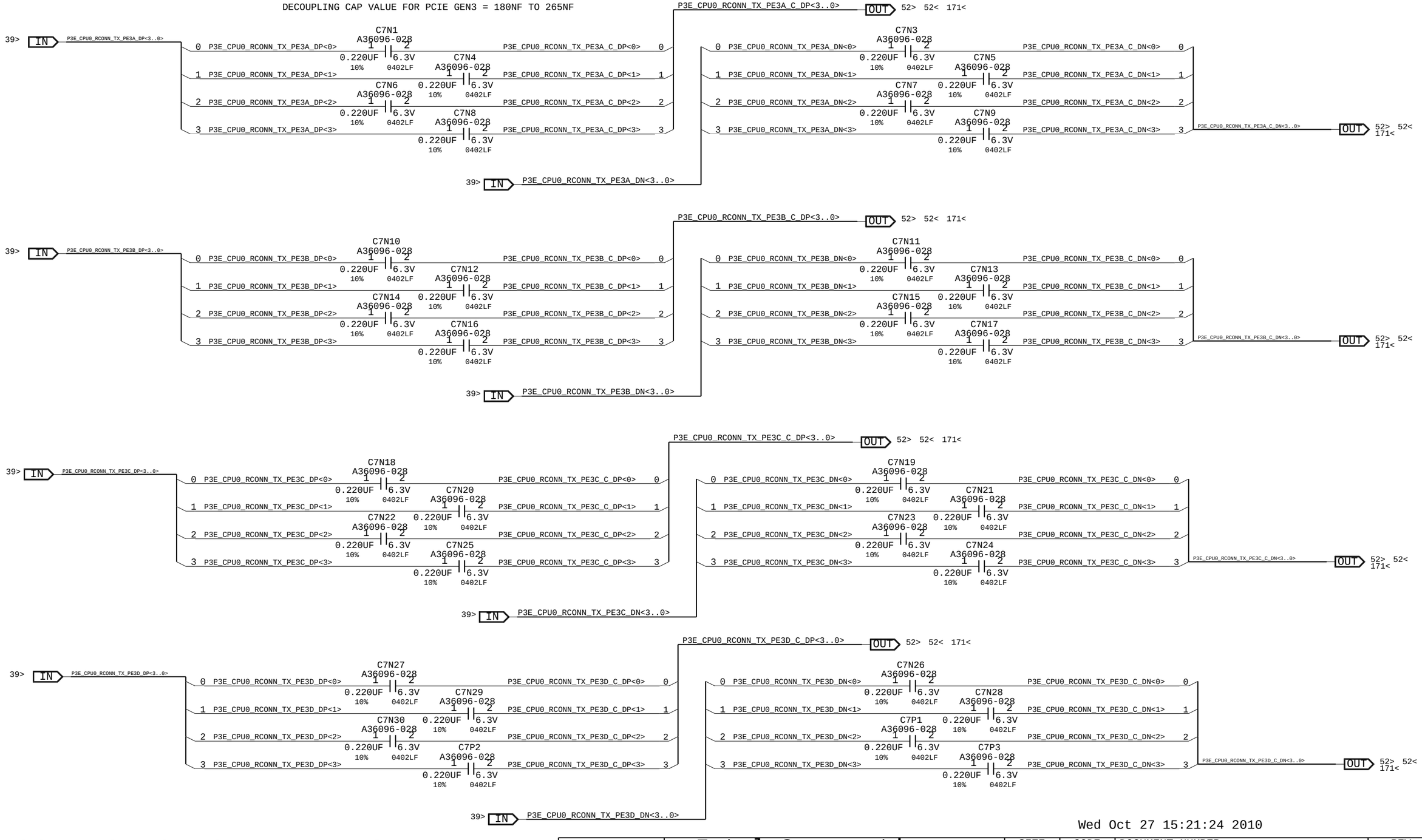
FROM ROMLEY PDG:
DECOUPLING CAP VALUE FOR PCIE GEN3 = 180NF TO 265NF



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ROOM: CPU0 IOU1 MIDBUS

CPU 0 MIDBUS PROBE (1 OF 2)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 51 OF 303	

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******NOTE: NETS PE3C<3>, PE3D<1>, PE3D<0>
HAVE POLARITY INVERSION

J7N1

PCIE_GEN3_FULL_A

TERMINATION RESISTORS ON BOARD VALUE 42.2 OHMS

171< 52> 51>	IN	P3E_CPU0_RCONN_TX_PE3A_C_DP<3..0>	0	P3E_CPU0_RCONN_TX_PE3A_C_DP<0>	C2	IN_0P	OUT_0P
171< 52> 51>	IN	P3E_CPU0_RCONN_TX_PE3A_C_DN<3..0>	0	P3E_CPU0_RCONN_TX_PE3A_C_DN<0>	C3	IN_0N	OUT_0N
			1	P3E_CPU0_RCONN_TX_PE3A_C_DP<1>	A1	IN_1P	OUT_1P
			1	P3E_CPU0_RCONN_TX_PE3A_C_DN<1>	A2	IN_1N	OUT_1N
			2	P3E_CPU0_RCONN_TX_PE3A_C_DP<2>	A4	IN_2P	OUT_2P
			2	P3E_CPU0_RCONN_TX_PE3A_C_DN<2>	A5	IN_2N	OUT_2N
			3	P3E_CPU0_RCONN_TX_PE3A_C_DP<3>	C4	IN_3P	OUT_3P
			3	P3E_CPU0_RCONN_TX_PE3A_C_DN<3>	C5	IN_3N	OUT_3N
171< 52> 51>	IN	P3E_CPU0_RCONN_TX_PE3B_C_DP<3..0>	0	P3E_CPU0_RCONN_TX_PE3B_C_DP<0>	C7	IN_4P	OUT_4P
171< 52> 51>	IN	P3E_CPU0_RCONN_TX_PE3B_C_DN<3..0>	0	P3E_CPU0_RCONN_TX_PE3B_C_DN<0>	C8	IN_4N	OUT_4N
			1	P3E_CPU0_RCONN_TX_PE3B_C_DP<1>	A6	IN_5P	OUT_5P
			1	P3E_CPU0_RCONN_TX_PE3B_C_DN<1>	A7	IN_5N	OUT_5N
			2	P3E_CPU0_RCONN_TX_PE3B_C_DP<2>	A9	IN_6P	OUT_6P
			2	P3E_CPU0_RCONN_TX_PE3B_C_DN<2>	A10	IN_6N	OUT_6N
			3	P3E_CPU0_RCONN_TX_PE3B_C_DP<3>	C9	IN_7P	OUT_7P
			3	P3E_CPU0_RCONN_TX_PE3B_C_DN<3>	C10	IN_7N	OUT_7N
171< 52> 51>	IN	P3E_CPU0_RCONN_TX_PE3C_C_DP<3..0>	0	P3E_CPU0_RCONN_TX_PE3C_C_DP<0>	C12	IN_8P	OUT_8P
171< 52> 51>	IN	P3E_CPU0_RCONN_TX_PE3C_C_DN<3..0>	0	P3E_CPU0_RCONN_TX_PE3C_C_DN<0>	C13	IN_8N	OUT_8N
			1	P3E_CPU0_RCONN_TX_PE3C_C_DP<1>	A11	IN_9P	OUT_9P
			1	P3E_CPU0_RCONN_TX_PE3C_C_DN<1>	A12	IN_9N	OUT_9N
			2	P3E_CPU0_RCONN_TX_PE3C_C_DP<2>	A14	IN_10P	OUT_10P
			2	P3E_CPU0_RCONN_TX_PE3C_C_DN<2>	A15	IN_10N	OUT_10N
			3	P3E_CPU0_RCONN_TX_PE3C_C_DP<3>	C15	IN_11N	OUT_11N
			3	P3E_CPU0_RCONN_TX_PE3C_C_DN<3>	C14	IN_11P	OUT_11P
171< 52> 51>	IN	P3E_CPU0_RCONN_TX_PE3D_C_DP<3..0>	0	P3E_CPU0_RCONN_TX_PE3D_C_DP<0>	C18	IN_12N	OUT_12N
171< 52> 51>	IN	P3E_CPU0_RCONN_TX_PE3D_C_DN<3..0>	0	P3E_CPU0_RCONN_TX_PE3D_C_DN<0>	C17	IN_12P	OUT_12P
			1	P3E_CPU0_RCONN_TX_PE3D_C_DP<1>	A17	IN_13N	OUT_13N
			1	P3E_CPU0_RCONN_TX_PE3D_C_DN<1>	A16	IN_13P	OUT_13P
			2	P3E_CPU0_RCONN_TX_PE3D_C_DP<2>	A19	IN_14P	OUT_14P
			2	P3E_CPU0_RCONN_TX_PE3D_C_DN<2>	A20	IN_14N	OUT_14N
			3	P3E_CPU0_RCONN_TX_PE3D_C_DP<3>	C19	IN_15P	OUT_15P
			3	P3E_CPU0_RCONN_TX_PE3D_C_DN<3>	C20	IN_15N	OUT_15N

		NC_MIDBUS_CPU0_RSVD	D1	RSVD	GND<17> D22
					GND<16> D17
					GND<15> D12
					GND<14> D7
					GND<13> D2
					GND<12> C21
					GND<11> C16
					GND<10> C11
					GND<9> C6
					GND<8> C1
					GND<7> B18
					GND<6> B13
					GND<5> B8
					GND<4> B3
					GND<3> A18
					GND<2> A13
					GND<1> A8
					GND<0> A3

D3	P3E_CPU0_RCONN_TX_PE3A_C_DP<0>	OUT	51> 52< 171<	IN_0P	OUT_0P	P3E_CPU0_RCONN_TX_PE3A_C_DP<0>	C2
D4	P3E_CPU0_RCONN_TX_PE3A_C_DN<0>	OUT	51> 52< 171<	IN_0N	OUT_0N	P3E_CPU0_RCONN_TX_PE3A_C_DN<0>	C3
B1	P3E_CPU0_RCONN_TX_PE3A_C_DP<1>	OUT	51> 52< 171<	IN_1P	OUT_1P	P3E_CPU0_RCONN_TX_PE3A_C_DP<1>	A1
B2	P3E_CPU0_RCONN_TX_PE3A_C_DN<1>	OUT	51> 52< 171<	IN_1N	OUT_1N	P3E_CPU0_RCONN_TX_PE3A_C_DN<1>	A2
B4	P3E_CPU0_RCONN_TX_PE3A_C_DP<2>	OUT	51> 52< 171<	IN_2P	OUT_2P	P3E_CPU0_RCONN_TX_PE3A_C_DP<2>	A4
B5	P3E_CPU0_RCONN_TX_PE3A_C_DN<2>	OUT	51> 52< 171<	IN_2N	OUT_2N	P3E_CPU0_RCONN_TX_PE3A_C_DN<2>	A5
D5	P3E_CPU0_RCONN_TX_PE3A_C_DP<3>	OUT	51> 52< 171<	IN_3P	OUT_3P	P3E_CPU0_RCONN_TX_PE3A_C_DP<3>	C4
D6	P3E_CPU0_RCONN_TX_PE3A_C_DN<3>	OUT	51> 52< 171<	IN_3N	OUT_3N	P3E_CPU0_RCONN_TX_PE3A_C_DN<3>	C5
D8	P3E_CPU0_RCONN_TX_PE3B_C_DP<0>	OUT	51> 52< 171<	IN_4P	OUT_4P	P3E_CPU0_RCONN_TX_PE3B_C_DP<0>	C7
D9	P3E_CPU0_RCONN_TX_PE3B_C_DN<0>	OUT	51> 52< 171<	IN_4N	OUT_4N	P3E_CPU0_RCONN_TX_PE3B_C_DN<0>	C8
B6	P3E_CPU0_RCONN_TX_PE3B_C_DP<1>	OUT	51> 52< 171<	IN_5P	OUT_5P	P3E_CPU0_RCONN_TX_PE3B_C_DP<1>	A6
B7	P3E_CPU0_RCONN_TX_PE3B_C_DN<1>	OUT	51> 52< 171<	IN_5N	OUT_5N	P3E_CPU0_RCONN_TX_PE3B_C_DN<1>	A7
B9	P3E_CPU0_RCONN_TX_PE3B_C_DP<2>	OUT	51> 52< 171<	IN_6P	OUT_6P	P3E_CPU0_RCONN_TX_PE3B_C_DP<2>	A9
B10	P3E_CPU0_RCONN_TX_PE3B_C_DN<2>	OUT	51> 52< 171<	IN_6N	OUT_6N	P3E_CPU0_RCONN_TX_PE3B_C_DN<2>	A10
D10	P3E_CPU0_RCONN_TX_PE3B_C_DP<3>	OUT	51> 52< 171<	IN_7P	OUT_7P	P3E_CPU0_RCONN_TX_PE3B_C_DP<3>	C9
D11	P3E_CPU0_RCONN_TX_PE3B_C_DN<3>	OUT	51> 52< 171<	IN_7N	OUT_7N	P3E_CPU0_RCONN_TX_PE3B_C_DN<3>	C10
D13	P3E_CPU0_RCONN_TX_PE3C_C_DP<0>	OUT	51> 52< 171<	IN_8P	OUT_8P	P3E_CPU0_RCONN_TX_PE3C_C_DP<0>	C12
D14	P3E_CPU0_RCONN_TX_PE3C_C_DN<0>	OUT	51> 52< 171<	IN_8N	OUT_8N	P3E_CPU0_RCONN_TX_PE3C_C_DN<0>	C13
B11	P3E_CPU0_RCONN_TX_PE3C_C_DP<1>	OUT	51> 52< 171<	IN_9P	OUT_9P	P3E_CPU0_RCONN_TX_PE3C_C_DP<1>	A11
B12	P3E_CPU0_RCONN_TX_PE3C_C_DN<1>	OUT	51> 52< 171<	IN_9N	OUT_9N	P3E_CPU0_RCONN_TX_PE3C_C_DN<1>	A12
B14	P3E_CPU0_RCONN_TX_PE3C_C_DP<2>	OUT	51> 52< 171<	IN_10P	OUT_10P	P3E_CPU0_RCONN_TX_PE3C_C_DP<2>	A14
B15	P3E_CPU0_RCONN_TX_PE3C_C_DN<2>	OUT	51> 52< 171<	IN_10N	OUT_10N	P3E_CPU0_RCONN_TX_PE3C_C_DN<2>	A15
D15	P3E_CPU0_RCONN_TX_PE3C_C_DN<3>	OUT	51> 52< 171<	IN_11P	OUT_11P	P3E_CPU0_RCONN_TX_PE3C_C_DN<3>	C14
D16	P3E_CPU0_RCONN_TX_PE3C_C_DP<3>	OUT	51> 52< 171<	IN_11N	OUT_11N	P3E_CPU0_RCONN_TX_PE3C_C_DP<3>	C15
D18	P3E_CPU0_RCONN_TX_PE3D_C_DN<0>	OUT	51> 52< 171<	IN_12P	OUT_12P	P3E_CPU0_RCONN_TX_PE3D_C_DN<0>	C17
D19	P3E_CPU0_RCONN_TX_PE3D_C_DP<0>	OUT	51> 52< 171<	IN_12N	OUT_12N	P3E_CPU0_RCONN_TX_PE3D_C_DP<0>	C18
B16	P3E_CPU0_RCONN_TX_PE3D_C_DN<1>	OUT	51> 52< 171<	IN_13P	OUT_13P	P3E_CPU0_RCONN_TX_PE3D_C_DN<1>	A16
B17	P3E_CPU0_RCONN_TX_PE3D_C_DP<1>	OUT	51> 52< 171<	IN_13N	OUT_13N	P3E_CPU0_RCONN_TX_PE3D_C_DP<1>	A17
B19	P3E_CPU0_RCONN_TX_PE3D_C_DP<2>	OUT	51> 52< 171<	IN_14P	OUT_14P	P3E_CPU0_RCONN_TX_PE3D_C_DP<2>	A19
B20	P3E_CPU0_RCONN_TX_PE3D_C_DN<2>	OUT	51> 52< 171<	IN_14N	OUT_14N	P3E_CPU0_RCONN_TX_PE3D_C_DN<2>	A20
D20	P3E_CPU0_RCONN_TX_PE3D_C_DP<3>	OUT	51> 52< 171<	IN_15P	OUT_15P	P3E_CPU0_RCONN_TX_PE3D_C_DP<3>	C19
D21	P3E_CPU0_RCONN_TX_PE3D_C_DN<3>	OUT	51> 52< 171<	IN_15N	OUT_15N	P3E_CPU0_RCONN_TX_PE3D_C_DN<3>	C20

N/A

134< 77> 76<> 33< IN PWRGD_CPU0_PWRGOOD_LVC1

R5F2
1K 1% 0402LF
1/16W
A93548-023

PWRGD_CPU0_SUTPWRGD_LVC1 D23

ROOM: CPU0 IOU1 MIDBUS

CPU 0 IOU1 MIDBUS PROBE (2 OF 2)

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		SCALE:	DO NOT SCALE DRAWING	SHEET 52 OF 303	

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COMPENSATION RESISTANCE CONTROL

PDG CAD NOTE: NOMINAL TRACE WIDTH = 10 MILS
PDG CAD NOTE: NOMINAL TRACE SPACING = 15 MILS
PDG CAD NOTE: MAX TRACE LENGTH TO RESISTOR = 2"
PDG CAD NOTE: PLACE PADS TOGETHER AND CLOSE TO THE CPU SOCKET

REFER TO PDG FOR PULLDOWN RESISTORS:

RCOMP[0] -> 130 OHM FOR ODT
RCOMP[1] -> 26.1 OHM FOR DQ/DQS
RCOMP[2] -> 200 OHM FOR CMD

ROOM: CPU0_RCOMP

40< OUT A_CPU0_DDR23_RCOMP<2>	R6J3 130 1% 1/16W	R6J5 26.1 1% 1/16W	R6J4 200 1% 1/16W	R5W3 130 1% 1/16W	R5W1 26.1 1% 1/16W	R5W2 200 1% 1/16W
40< OUT A_CPU0_DDR23_RCOMP<1>						
40< OUT A_CPU0_DDR23_RCOMP<0>						
40< OUT A_CPU0_DDR01_RCOMP<2>						
40< OUT A_CPU0_DDR01_RCOMP<1>						
40< OUT A_CPU0_DDR01_RCOMP<0>						
	A93548-078 0402LF	A93548-524 0402	A93548-060 0402LF	A93548-078 0402LF	A93548-524 0402	A93548-060 0402LF

ROOM: CPU1_RCOMP

63< OUT A_CPU1_DDR23_RCOMP<2>	R9J3 130 1% CPU1_RCOMP 1/16W	R9J5 26.1 1% CPU1_RCOMP 1/16W	R9J4 200 1% CPU1_RCOMP 1/16W	R2W3 130 1% CPU1_RCOMP 1/16W	R2W1 26.1 1% CPU1_RCOMP 1/16W	R2W2 200 1% CPU1_RCOMP 1/16W
63< OUT A_CPU1_DDR23_RCOMP<1>						
63< OUT A_CPU1_DDR23_RCOMP<0>						
63< OUT A_CPU1_DDR01_RCOMP<2>						
63< OUT A_CPU1_DDR01_RCOMP<1>						
63< OUT A_CPU1_DDR01_RCOMP<0>						
	A93548-078 0402LF	A93548-524 0402	A93548-060 0402LF	A93548-078 0402LF	A93548-524 0402	A93548-060 0402LF

ROOM: CPU2_RCOMP

86< OUT A_CPU2_DDR23_RCOMP<2>	R7C6 130 1% CPU2_RCOMP 1/16W	R7C4 26.1 1% CPU2_RCOMP 1/16W	R7C5 200 1% CPU2_RCOMP 1/16W	R2N1 130 1% CPU2_RCOMP 1/16W	R2N3 26.1 1% CPU2_RCOMP 1/16W	R2N2 200 1% CPU2_RCOMP 1/16W
86< OUT A_CPU2_DDR23_RCOMP<1>						
86< OUT A_CPU2_DDR23_RCOMP<0>						
86< OUT A_CPU2_DDR01_RCOMP<2>						
86< OUT A_CPU2_DDR01_RCOMP<1>						
86< OUT A_CPU2_DDR01_RCOMP<0>						
	A93548-078 0402LF	A93548-524 0402	A93548-060 0402LF	A93548-078 0402LF	A93548-524 0402	A93548-060 0402LF

ROOM: CPU3_RCOMP

109< OUT A_CPU3_DDR23_RCOMP<2>	R4C6 130 1% CPU3_RCOMP 1/16W	R4C4 26.1 1% CPU3_RCOMP 1/16W	R4C5 200 1% CPU3_RCOMP 1/16W	R5N1 130 1% CPU3_RCOMP 1/16W	R5N3 26.1 1% CPU3_RCOMP 1/16W	R5N2 200 1% CPU3_RCOMP 1/16W
109< OUT A_CPU3_DDR23_RCOMP<1>						
109< OUT A_CPU3_DDR23_RCOMP<0>						
109< OUT A_CPU3_DDR01_RCOMP<2>						
109< OUT A_CPU3_DDR01_RCOMP<1>						
109< OUT A_CPU3_DDR01_RCOMP<0>						
	A93548-078 0402LF	A93548-524 0402	A93548-060 0402LF	A93548-078 0402LF	A93548-524 0402	A93548-060 0402LF

40> IN PD_CPU0_TEST<3>	R6J7 49.9 1% 1/16W	R6J6 49.9 1% 1/16W	R4J9 49.9 1% 1/16W	R4J7 49.9 1% 1/16W
40> IN PD_CPU0_TEST<2>				
40> IN PD_CPU0_TEST<1>				
40> IN PD_CPU0_TEST<0>				
	A93548-045 0402LF	A93548-045 0402LF	A93548-045 0402LF	A93548-045 0402LF

63> IN PD_CPU1_TEST<3>	R9J7 49.9 1% 1/16W	R9J6 49.9 1% 1/16W	R7J9 49.9 1% 1/16W	R7J7 49.9 1% 1/16W
63> IN PD_CPU1_TEST<2>				
63> IN PD_CPU1_TEST<1>				
63> IN PD_CPU1_TEST<0>				
	A93548-045 0402LF	A93548-045 0402LF	A93548-045 0402LF	A93548-045 0402LF

86> IN PD_CPU2_TEST<3>	R7C2 49.9 1% 1/16W	R7C3 49.9 1% 1/16W	R9B25 49.9 1% 1/16W	R9C2 49.9 1% 1/16W
86> IN PD_CPU2_TEST<2>				
86> IN PD_CPU2_TEST<1>				
86> IN PD_CPU2_TEST<0>				
	A93548-045 0402LF	A93548-045 0402LF	A93548-045 0402LF	A93548-045 0402LF

109> IN PD_CPU3_TEST<3>	R4C2 49.9 1% 1/16W	R4C3 49.9 1% 1/16W	R6B26 49.9 1% 1/16W	R6C2 49.9 1% 1/16W
109> IN PD_CPU3_TEST<2>				
109> IN PD_CPU3_TEST<1>				
109> IN PD_CPU3_TEST<0>				
	A93548-045 0402LF	A93548-045 0402LF	A93548-045 0402LF	A93548-045 0402LF

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CPU MISC: DDR3

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		SCALE:	DO NOT SCALE DRAWING		SHEET 53 OF 303

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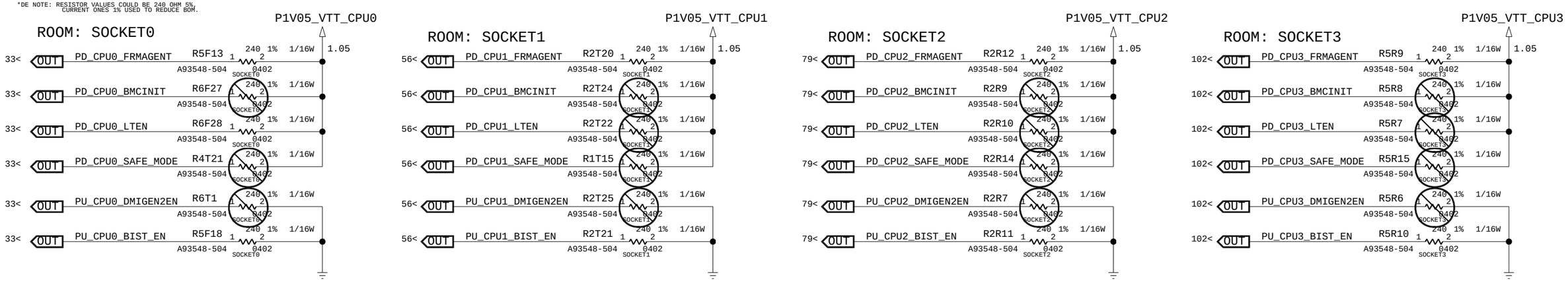
STRAP SIGNALS

NET NAMES REFLECT ON-DIE TERMINATION AT CPU

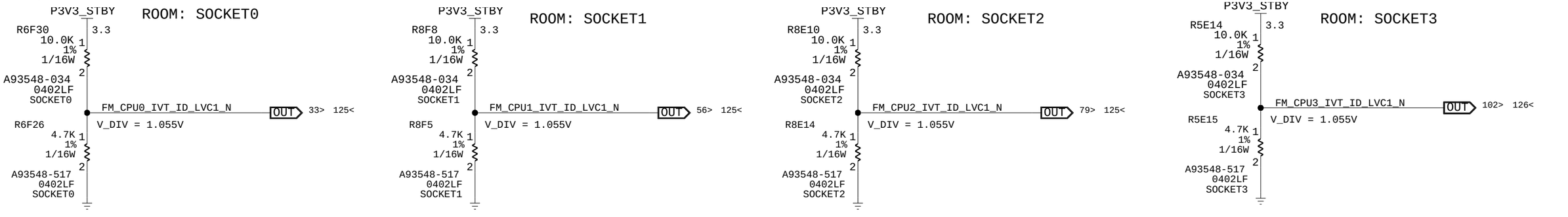
LTENABLE AT CPU0: DE POPULATE RESISTOR ON BRING UP BOARD.
SAFE_MODE_BOOT AT CPU0: ALLOW FOR OPTION OF RESISTOR BEING POPULATED ON BRING UP BOARD.

*DE NOTE: RESISTOR VALUES COULD BE 240 OHM 5%,
CURRENT ONES 1% USED TO REDUCE BOM.



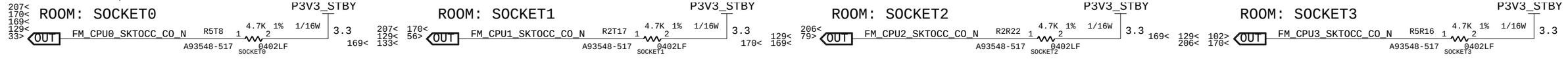
IVT_ID SIGNALS

P3V3_STBY IS REQUIRED IN ORDER FOR THE CPLD
TO REALIZE WHETHER SNB-EX OR IVB-EXB IS PLACED
BEFORE THE PLATFORM IS COMPLETELY ON



SOCKET OCCUPIED SIGNALS

SOCKET/PKG ONLY PINS, CONNECTED TO GND ON THE PACKAGE



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CPU MISC: STRAPS, IVT_ID, SKTOCC

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET	54 OF 303

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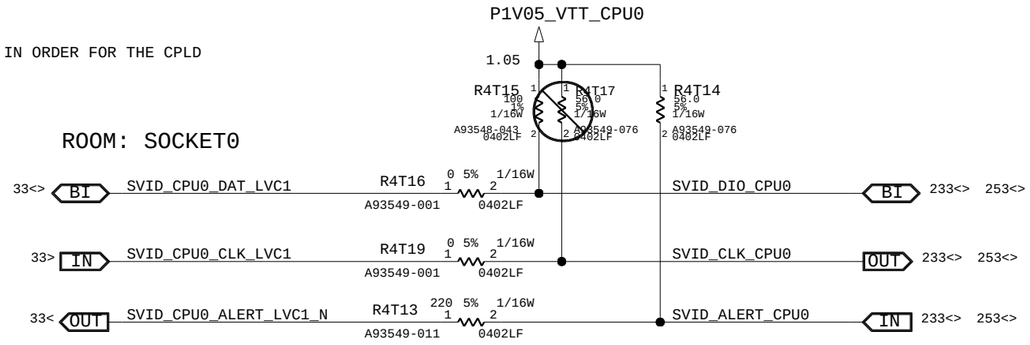
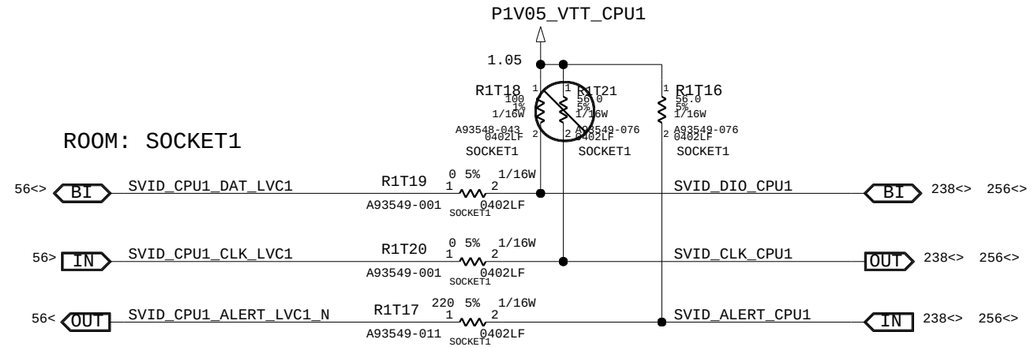
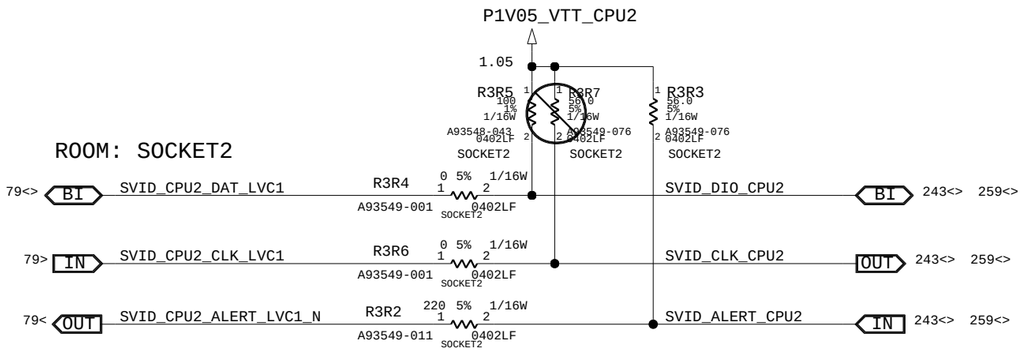
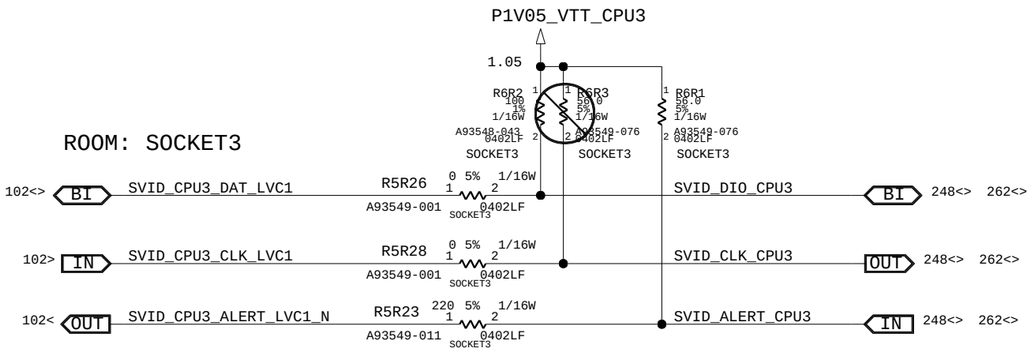
SVID SIGNALS

P3V3_STBY IS REQUIRED IN ORDER FOR THE CPLD









PCIE HOTPLUG SMB INTERFACE

PCIE HOTPLUG NOT SUPPORTED BY PLATFORM
*DE NOTE: ACCORDING TO MOW WW17 IF PE HP SMBUS PINS UNUSED LEAVE THEM NC

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CPUS MISC: SVID, PCIE HP

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 55 OF 303	

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CAD NOTE FROM ROMLEY PDG NOTE FOR PE_RBIAS:
THE ROUTING DISTANCE TO THE RESISTOR
SHOULD BE AS CLOSE AS POSSIBLE
(NO LONGER THAN 1.0" AND AT LEAST 15 MILS WIDE)
KEEP THE TRACES SEPARETED 30 MILS FROM ALL OTHERS.

C2T10 0.01UF 25V 10% A36096-045 0402LF

R2T23 49.9 1% 1/16W A93548-045 0402LF

DE NOTE: PE_RBIAS_SENSE NET MUST BE SHORTED
AT THE TOP OF PE_RBIAS 50OHM RESISTOR.
CONNECT SENSE AS CLOSE AS POSIBLE TO OTHER END OF RES

NET NAMES REFLECT ON-DIE TERMINATION AT CPU

U7H1
IC

SANDYBRIDGE_EP_EXT_D

		A_CPU1_PE_VREF_CAP	AJ43	PE_VREF_CAP	QPI_VREF_CAP	CU51 A_CPU1_QPI_VREF_CAP
			AF52	PE_RBIAS_SENSE	QPI_RBIAS_SENSE	CC53
		A_CPU1_PE_RBIAS	AH52	PE_RBIAS	QPI_RBIAS	CE53 A_CPU1_QPI_RBIAS
31>	IN	CLK_100M_CPU1_PCIE_DP	AW45	BCLK1_DP	BCLK0_DP	CN43 CLK_100M_CPU1_QPI_DP IN 31>
31>	IN	CLK_100M_CPU1_PCIE_DN	BA45	BCLK1_DN	BCLK0_DN	CM44 CLK_100M_CPU1_QPI_DN IN 31>
		TP_SMB_CPU1_PE_HP_1V05_SCL	BH48	PEHPSCL	RSVD<31>	CA45 NC_CPU1_RSVD<31>
		TP_SMB_CPU1_PE_HP_1V05_SDA	BF48	PEHPSDA	RSVD<32>	BY46 NC_CPU1_RSVD<32>
		NC_CPU1_RSVD<12>	D56	RSVD<12>	RSVD<18>	DD54 NC_CPU1_RSVD<18>
		NC_CPU1_RSVD<8>	F56	RSVD<8>	RSVD<19>	DC55 NC_CPU1_RSVD<19>
		NC_CPU1_RSVD<10>	E57	RSVD<10>	RSVD<17>	DE55 NC_CPU1_RSVD<17>
		NC_CPU1_RSVD<7>	F58	RSVD<7>	RSVD<21>	DA57 NC_CPU1_RSVD<21>
		NC_CPU1_RSVD<5>	H58	RSVD<5>	RSVD<22>	CY58 NC_CPU1_RSVD<22>
		NC_CPU1_RSVD<63>	AR55	RSVD<63>	RSVD<40>	BM46 NC_CPU1_RSVD<40>
		NC_CPU1_RSVD<62>	AU55	RSVD<62>	RSVD<37>	BP46 NC_CPU1_RSVD<37>
54>	IN	PU_CPU1_DMIGEN2EN	V52	TXT_PLTEN	RSVD<24>	CY48 NC_CPU1_RSVD<24>
54>	IN	PD_CPU1_FRMAGENT	AT50	FRMAGENT	RSVD<25>	CY46 NC_CPU1_RSVD<25>
54>	IN	PD_CPU1_BMCINIT	AL47	BMCINIT	THERMTRIP_N	BL47 FM_CPU1_THERMTRIP_LVC1_N OUT 100<
54>	IN	PD_CPU1_LTEN	AK52	TXT_AGENT	PROCHOT_N	BD52 FM_CPU1_PROCHOT_LVC1_N BI 122<>
54>	IN	PU_CPU1_BIST_EN	AT48	BIST_ENABLE	TEST4	BA55 PD_CPU1_TEST<4>
						NOTE: CONNECT TEST4 TO VSS PER PDG
125< 54>	OUT	FM_CPU1_IVT_ID_LVC1_N	AH42	IVT_ID_N	PRDY_N	R53 XDP_CPU1_PRDY_N OUT 134<
					PREQ_N	U53 XDP_CPU1_PREQ_N IN 134<
123<>	BI	FM_CPU1_MEMGH_MEMHOT_LVC1_N	E13	MEM_HOT_C23_N		
123<>	BI	FM_CPU1_MEMEF_MEMHOT_LVC1_N	CB22	MEM_HOT_C01_N	SOCKET_ID<1>	BC49 FM_CPU1_SOCKET_ID1_LVC1
76>	IN	PWRGD_CPU1_DRAMPWRGD_LVC1V5	L15	DRAM_PWR_OK_C23	SOCKET_ID<0>	CY52 FM_CPU1_SOCKET_ID0_LVC1
			CW17	DRAM_PWR_OK_C01		
73<	OUT	P1V5_DDR3_GH_VREFDQTX	P42	DDR_VREFDQTX_C23		DE NOTE: SOCKET_ID[1:0] NETS HAVE PD ON DIE
73<	OUT	P1V5_DDR3_EF_VREFDQTX	CN41	DDR_VREFDQTX_C01		
73>	IN	P1V5_DDR3_GH_VREFDQRX	J1	DDR_VREFDQRX_C23		
73>	IN	P1V5_DDR3_EF_VREFDQRX	BY16	DDR_VREFDQRX_C01		
199<	BI	SMB_DDR_GH_LVC1_SDA	R43	DDR_SDA_C23	PECI	BJ47 PECI_CPU_LVC1 BI 33<> 79<> 102<> 196<>
199<	BI	SMB_DDR_EF_LVC1_SDA	CW41	DDR_SDA_C01		
199<>	OUT	SMB_DDR_GH_LVC1_SCL	U43	DDR_SCL_C23	SVIDCLK	CB44 SVID_CPU1_CLK_LVC1 OUT 55<
199<>	OUT	SMB_DDR_EF_LVC1_SCL	CY42	DDR_SCL_C01	SVIDDATA	BR45 SVID_CPU1_DAT_LVC1 BI 55<>
72< 71<	OUT	M_GH_RESET_LVC1V5_N	AE27	DDR_RESET_C23_N	SVIDALERT_N	CR43 SVID_CPU1_ALERT_LVC1_N IN 55>
70< 69<	OUT	M_EF_RESET_LVC1V5_N	CB18	DDR_RESET_C01_N		
					PMSYNC	K52 IRQ_PM_SYNC_LVC1 IN 33< 135>
207< 170< 169< 133< 129< 54>	OUT	FM_CPU1_SKTOCC_CO_N	BU49	SKTOCC_N	PWRGOOD	BJ53 PWRGD_CPU1_PWRGOOD_LVC1 IN 76<> 77>
					EAR_N	CH56 RST_CPU_EAR_LVC1_N BI 33<> 79<> 102<> 125< 134>
		NC_CPU1_RSVD<23>	CY56	RSVD<23>	RESET_N	CK44 RST_CPU1_RESET_LVC1_N IN 76>
99<	BI	IRQ_CPU1_CATERR_LVC1_N	CC51	CAT_ERR_N		
54>	IN	PD_CPU1_SAFE_MODE	DA55	SAFE_MODE_BOOT		
133>	IN	JTAG_CPU1_G_TDI	BW43	TDI	TDO	CA43 JTAG_CPU1_G_TDO OUT 133<
134> 133> 33<	IN	JTAG_CPU_LVC1_TCK0	BY44	TCK		
134> 133> 102< 79< 33<	IN	JTAG_CPU_G_TMS	BV44	TMS		
134> 133> 102< 79< 33<	IN	JTAG_CPU_LVC1_TRST_N	CT54	TRST_N		

1/17

E64556-001

CAD NOTE FROM ROMLEY PDG NOTE FOR QPI_RBIAS:
THE ROUTING DISTANCE TO THE RESISTOR
SHOULD BE AS CLOSE AS POSSIBLE
(POSSIBLY NO LONGER THAN 1.0" AND AT LEAST 10 MILS WIDE)

R1T26 49.9 1% 1/16W A93548-045 0402LF

C1T15 0.01UF 25V 10% A36096-045 0402LF

DE NOTE: QPI_RBIAS_SENSE NET MUST BE SHORTED
AT THE TOP OF QPI_RBIAS 50OHM RESISTOR.
CONNECT SENSE AS CLOSE AS POSIBLE TO OTHER END OF RES

P1V05_VTT_CPU1

*DE NOTE: RESISTOR VALUES COULD BE 240 OHM 5%,
CURRENT ONES 1% USED TO REDUCE BOM.

1.05

R2T19 240 1% 1/16W A93548-504 0402

R1T14 240 1% 1/16W A93548-504 0402

CPU	SOCKET_ID[2:0]	PECI ADDRESS
CPU1	001B	0X31

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CPU SOCKET 1 (1 OF 13)

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		SCALE:	DO NOT SCALE DRAWING	SHEET 56 OF 303	

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SANDYBRIDGE_EP_EXT_D

69<> BI M_E_DQ<63..0>

63	M_E_DQ<63>	CL41	DDR0_DQ<63>	
62	M_E_DQ<62>	CJ41	DDR0_DQ<62>	
61	M_E_DQ<61>	CL37	DDR0_DQ<61>	
60	M_E_DQ<60>	CJ37	DDR0_DQ<60>	
59	M_E_DQ<59>	CK42	DDR0_DQ<59>	
58	M_E_DQ<58>	CH42	DDR0_DQ<58>	
57	M_E_DQ<57>	CK38	DDR0_DQ<57>	
56	M_E_DQ<56>	CH38	DDR0_DQ<56>	
55	M_E_DQ<55>	CB42	DDR0_DQ<55>	
54	M_E_DQ<54>	CC41	DDR0_DQ<54>	
53	M_E_DQ<53>	CE37	DDR0_DQ<53>	
52	M_E_DQ<52>	CC37	DDR0_DQ<52>	
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CPU SOCKET 1 (2 OF 13)

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		SCALE:	DO NOT SCALE DRAWING	SHEET 57 OF 303

INTEL CONFIDENTIAL

U7H1 IC

SANDYBRIDGE_EP_EXT_D

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	NC_M_F_CS_N<5>	CT24	DDR1_CS_N<5>	DDR1_CKE<1>	CU19 M_F_CKE<1> 1
	NC_M_F_CS_N<4>	CU25	DDR1_CS_N<4>	DDR1_CKE<0>	CT20 M_F_CKE<0> 0
3	M_F_CS_N<3>	CR27	DDR1_CS_N<3>		
2	M_F_CS_N<2>	CR23	DDR1_CS_N<2>	DDR1_BA<2>	DF18 M_F_BA<2> 2
1	M_F_CS_N<1>	CU23	DDR1_CS_N<1>	DDR1_BA<1>	DC25 M_F_BA<1> 1
0	M_F_CS_N<0>	DB24	DDR1_CS_N<0>	DDR1_BA<0>	DB26 M_F_BA<0> 0
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	NC_M_F_CK_DP<1>	CY22	DDR1_CLK_DP<1>	DDR1_ODT<3>	CV26 NC_M_F_ODT<3>
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	NC_M_F_CK_DN<3>	DA21	DDR1_CLK_DN<3>	DDR1_ODT<1>	DA25 M_F_ODT<1> 1
	M_F_CK_DN<2>	CY24	DDR1_CLK_DN<2>	DDR1_ODT<0>	CT22 M_F_ODT<0> 0
	NC_M_F_CK_DN<1>	CV22	DDR1_CLK_DN<1>	DDR1_WE_N	CV28 M_F_WE_N
	M_F_CK_DN<0>	CV20	DDR1_CLK_DN<0>	DDR1_RAS_N	DB28 M_F_RAS_N
				DDR1_PAR_ERR_N	CU21 M_F_PAR_ERR_N<0>
				DDR1_CAS_N	CY30 M_F_CAS_N
				DDR1_MA_PAR	DE25 M_F_MA_PAR

M_F_DQS_DP<17..0> BI 70<>

M_F_DQS_DN<17..0> BI 70<>

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M_F_ECC<7..0> BI 70<>

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M_F_ODT<1..0> OUT 70<

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70< OUT M_F_CK_DP<2>

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70< OUT M_F_CK_DN<1>

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M_F_WE_N OUT 70<

M_F_RAS_N OUT 70<

M_F_PAR_ERR_N<0> IN 70>

M_F_CAS_N OUT 70<

M_F_MA_PAR OUT 70<

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CPU SOCKET 1 (3 OF 13)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 58 OF 303	

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U7H1 IC

SANDYBRIDGE_EP_EXT_D

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59	M_G_DQ<59>	AE5	DDR2_DQ<59>	
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48	M_G_DQ<48>	R13	DDR2_DQ<48>	
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46	M_G_DQ<46>	AD8	DDR2_DQ<46>	
45	M_G_DQ<45>	W7	DDR2_DQ<45>	
44	M_G_DQ<44>	U7	DDR2_DQ<44>	
43	M_G_DQ<43>	AG7	DDR2_DQ<43>	
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39	M_G_DQ<39>	AD10	DDR2_DQ<39>	
38	M_G_DQ<38>	AB10	DDR2_DQ<38>	
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	NC_M_G_CS_N<6>	AB16	DDR2_CS_N<6>	
	NC_M_G_CS_N<5>	P18	DDR2_CS_N<5>	
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2	M_G_CS_N<2>	AD16	DDR2_CS_N<2>	
1	M_G_CS_N<1>	AE19	DDR2_CS_N<1>	
0	M_G_CS_N<0>	AB20	DDR2_CS_N<0>	
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71< OUT	M_G_CK_DP<2>	AA21	DDR2_CLK_DP<2>	
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71< OUT	M_G_CK_DP<0>	AB24	DDR2_CLK_DP<0>	
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71< OUT	M_G_CK_DN<2>	W21	DDR2_CLK_DN<2>	
	NC_M_G_CK_DN<1>	Y22	DDR2_CLK_DN<1>	
71< OUT	M_G_CK_DN<0>	Y24	DDR2_CLK_DN<0>	

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	DDR2_DQS_DP<14>	Y8	M_G_DQS_DP<14>	14
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	DDR2_DQS_DP<12>	Y34	M_G_DQS_DP<12>	12
	DDR2_DQS_DP<11>	V32	M_G_DQS_DP<11>	11
	DDR2_DQS_DP<10>	AB40	M_G_DQS_DP<10>	10
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	DDR2_DQS_DP<8>	AC27	M_G_DQS_DP<8>	8
	DDR2_DQS_DP<7>	AB4	M_G_DQS_DP<7>	7
	DDR2_DQS_DP<6>	W11	M_G_DQS_DP<6>	6
	DDR2_DQS_DP<5>	AC7	M_G_DQS_DP<5>	5
	DDR2_DQS_DP<4>	AE11	M_G_DQS_DP<4>	4
	DDR2_DQS_DP<3>	AC33	M_G_DQS_DP<3>	3
	DDR2_DQS_DP<2>	U31	M_G_DQS_DP<2>	2
	DDR2_DQS_DP<1>	AB38	M_G_DQS_DP<1>	1
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M_G_DQS_DP<17..0> BI 71<>

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	DDR2_DQS_DN<15>	V12	M_G_DQS_DN<15>	15
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	DDR2_DQS_DN<13>	AD12	M_G_DQS_DN<13>	13
	DDR2_DQS_DN<12>	AB34	M_G_DQS_DN<12>	12
	DDR2_DQS_DN<11>	T32	M_G_DQS_DN<11>	11
	DDR2_DQS_DN<10>	AC39	M_G_DQS_DN<10>	10
	DDR2_DQS_DN<9>	W39	M_G_DQS_DN<9>	9
	DDR2_DQS_DN<8>	AB28	M_G_DQS_DN<8>	8
	DDR2_DQS_DN<7>	AC3	M_G_DQS_DN<7>	7
	DDR2_DQS_DN<6>	U11	M_G_DQS_DN<6>	6
	DDR2_DQS_DN<5>	AB8	M_G_DQS_DN<5>	5
	DDR2_DQS_DN<4>	AC11	M_G_DQS_DN<4>	4
	DDR2_DQS_DN<3>	AA33	M_G_DQS_DN<3>	3
	DDR2_DQS_DN<2>	W31	M_G_DQS_DN<2>	2
	DDR2_DQS_DN<1>	AD38	M_G_DQS_DN<1>	1
	DDR2_DQS_DN<0>	T38	M_G_DQS_DN<0>	0

M_G_DQS_DN<17..0> BI 71<>

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	DDR2_MA<14>	W25	M_G_MA<14>	14
	DDR2_MA<13>	R15	M_G_MA<13>	13
	DDR2_MA<12>	T24	M_G_MA<12>	12
	DDR2_MA<11>	U23	M_G_MA<11>	11
	DDR2_MA<10>	T18	M_G_MA<10>	10
	DDR2_MA<9>	R23	M_G_MA<9>	9
	DDR2_MA<8>	T22	M_G_MA<8>	8
	DDR2_MA<7>	P22	M_G_MA<7>	7
	DDR2_MA<6>	R21	M_G_MA<6>	6
	DDR2_MA<5>	U21	M_G_MA<5>	5
	DDR2_MA<4>	P20	M_G_MA<4>	4
	DDR2_MA<3>	T20	M_G_MA<3>	3
	DDR2_MA<2>	U19	M_G_MA<2>	2
	DDR2_MA<1>	R19	M_G_MA<1>	1
	DDR2_MA<0>	AB18	M_G_MA<0>	0

M_G_MA<15..0> OUT 71<

	DDR2_ECC<7>	AA27	M_G_ECC<7>	7
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	DDR2_ECC<5>	AD30	M_G_ECC<5>	5
	DDR2_ECC<4>	AB30	M_G_ECC<4>	4
	DDR2_ECC<3>	AB26	M_G_ECC<3>	3
	DDR2_ECC<2>	Y26	M_G_ECC<2>	2
	DDR2_ECC<1>	AF28	M_G_ECC<1>	1
	DDR2_ECC<0>	AF30	M_G_ECC<0>	0

M_G_ECC<7..0> BI 71<>

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	DDR2_CKE<4>	AE25	NC_M_G_CKE<4>	
	DDR2_CKE<3>	AD24	NC_M_G_CKE<3>	
	DDR2_CKE<2>	U27	NC_M_G_CKE<2>	
	DDR2_CKE<1>	T26	M_G_CKE<1>	1
	DDR2_CKE<0>	AA25	M_G_CKE<0>	0

M_G_CKE<1..0> OUT 71<

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	DDR2_BA<1>	L17	M_G_BA<1>	1
	DDR2_BA<0>	R17	M_G_BA<0>	0

M_G_BA<2..0> OUT 71<

	DDR2_ODT<5>	AE21	NC_M_G_ODT<5>	
	DDR2_ODT<4>	AD22	NC_M_G_ODT<4>	
	DDR2_ODT<3>	Y18	NC_M_G_ODT<3>	
	DDR2_ODT<2>	AD18	NC_M_G_ODT<2>	
	DDR2_ODT<1>	W19	M_G_ODT<1>	1
	DDR2_ODT<0>	Y20	M_G_ODT<0>	0

M_G_ODT<1..0> OUT 71<

DDR2_WE_N	P16	M_G_WE_N	OUT 71<
DDR2_RAS_N	U17	M_G_RAS_N	OUT 71<
DDR2_PAR_ERR_N	AD20	M_G_PAR_ERR_N<0>	IN 71>
DDR2_CAS_N	T16	M_G_CAS_N	OUT 71<
DDR2_MA_PAR	M18	M_G_MA_PAR	OUT 71<

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CPU SOCKET 1 (4 OF 13)

DEPARTMENT	Intel Corporation	SIZE / CODE / DOCUMENT NUMBER / REV	
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B / 34649 / 444359 / 1.0	
		SCALE: DO NOT SCALE DRAWING	SHEET 59 OF 303

INTEL CONFIDENTIAL

U7H1 IC

SANDYBRIDGE_EP_EXT_D

72<> BI	M_H_DQ<63..0>	63	M_H_DQ<63>	M2	DDR3_DQ<63>	DDR3_DQS_DP<17>	F28	M_H_DQS_DP<17> 17
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		24	M_H_DQ<24>	M32	DDR3_DQ<24>	DDR3_MA<14>	D24	M_H_MA<14> 14
		23	M_H_DQ<23>	B32	DDR3_DQ<23>	DDR3_MA<13>	A13	M_H_MA<13> 13
		22	M_H_DQ<22>	A33	DDR3_DQ<22>	DDR3_MA<12>	E23	M_H_MA<12> 12
		21	M_H_DQ<21>	C35	DDR3_DQ<21>	DDR3_MA<11>	A23	M_H_MA<11> 11
		20	M_H_DQ<20>	E35	DDR3_DQ<20>	DDR3_MA<10>	D18	M_H_MA<10> 10
		19	M_H_DQ<19>	F32	DDR3_DQ<19>	DDR3_MA<9>	G23	M_H_MA<9> 9
		18	M_H_DQ<18>	D32	DDR3_DQ<18>	DDR3_MA<8>	D22	M_H_MA<8> 8
		17	M_H_DQ<17>	F34	DDR3_DQ<17>	DDR3_MA<7>	B22	M_H_MA<7> 7
		16	M_H_DQ<16>	A35	DDR3_DQ<16>	DDR3_MA<6>	F22	M_H_MA<6> 6
		15	M_H_DQ<15>	H36	DDR3_DQ<15>	DDR3_MA<5>	A21	M_H_MA<5> 5
		14	M_H_DQ<14>	K36	DDR3_DQ<14>	DDR3_MA<4>	D20	M_H_MA<4> 4
		13	M_H_DQ<13>	K40	DDR3_DQ<13>	DDR3_MA<3>	B20	M_H_MA<3> 3
		12	M_H_DQ<12>	M40	DDR3_DQ<12>	DDR3_MA<2>	F20	M_H_MA<2> 2
		11	M_H_DQ<11>	J35	DDR3_DQ<11>	DDR3_MA<1>	E21	M_H_MA<1> 1
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		9	M_H_DQ<9>	L39	DDR3_DQ<9>			
		8	M_H_DQ<8>	N39	DDR3_DQ<8>	DDR3_ECC<7>	H26	M_H_ECC<7> 7
		7	M_H_DQ<7>	A37	DDR3_DQ<7>	DDR3_ECC<6>	F26	M_H_ECC<6> 6
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		4	M_H_DQ<4>	F40	DDR3_DQ<4>	DDR3_ECC<3>	C25	M_H_ECC<3> 3
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			NC_M_H_CS_N<8>	D16	DDR3_CS_N<9>	DDR3_CKE<4>	R25	NC_M_H_CKE<4>
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		1	M_H_CS_N<1>	J19	DDR3_CS_N<2>	DDR3_BA<1>	E19	M_H_BA<1> 1
		0	M_H_CS_N<0>	G19	DDR3_CS_N<1>	DDR3_BA<0>	A17	M_H_BA<0> 0
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			NC_M_H_CK_DP<3>	M22		DDR3_ODT<5>	M16	NC_M_H_ODT<5>
72< OUT			M_H_CK_DP<2>	K20	DDR3_CLK_DP<3>	DDR3_ODT<4>	D14	NC_M_H_ODT<4>
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72< OUT			M_H_CK_DP<0>	L23	DDR3_CLK_DP<1>	DDR3_ODT<2>	E17	NC_M_H_ODT<2>
					DDR3_CLK_DP<0>	DDR3_ODT<1>	F18	M_H_ODT<1> 1
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72< OUT			M_H_CK_DN<0>	J23	DDR3_CLK_DN<1>	DDR3_RAS_N	B16	M_H_RAS_N
					DDR3_CLK_DN<0>	DDR3_PAR_ERR_N	G21	M_H_PAR_ERR_N<0>
						DDR3_CAS_N	B14	M_H_CAS_N
						DDR3_MA_PAR	B18	M_H_MA_PAR

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CPU SOCKET 1 (5 OF 13)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 60 OF 303	

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TP_P3E_CPU1_RX_PE1A_DP<3>	E55	PE1A_RX_DP<3>	PE1A_TX_DP<3>	J45	TP_P3E_CPU1_TX_PE1A_DP<3>
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TP_P3E_CPU1_RX_PE1A_DP<1>	D52	PE1A_RX_DP<1>	PE1A_TX_DP<1>	J43	TP_P3E_CPU1_TX_PE1A_DP<1>
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TP_P3E_CPU1_RX_PE1A_DN<2>	F54	PE1A_RX_DN<2>	PE1A_TX_DN<2>	K44	TP_P3E_CPU1_TX_PE1A_DN<2>
TP_P3E_CPU1_RX_PE1A_DN<1>	F52	PE1A_RX_DN<1>	PE1A_TX_DN<1>	L43	TP_P3E_CPU1_TX_PE1A_DN<1>
TP_P3E_CPU1_RX_PE1A_DN<0>	E51	PE1A_RX_DN<0>	PE1A_TX_DN<0>	K42	TP_P3E_CPU1_TX_PE1A_DN<0>
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TP_P3E_CPU1_RX_PE1B_DP<1>	K54	PE1B_RX_DP<5>	PE1B_TX_DP<5>	J47	TP_P3E_CPU1_TX_PE1B_DP<1>
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TP_P3E_CPU1_RX_PE1B_DN<2>	L57	PE1B_RX_DN<6>	PE1B_TX_DN<6>	K48	TP_P3E_CPU1_TX_PE1B_DN<2>
TP_P3E_CPU1_RX_PE1B_DN<1>	M54	PE1B_RX_DN<5>	PE1B_TX_DN<5>	L47	TP_P3E_CPU1_TX_PE1B_DN<1>
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CPU SOCKET 1 (6 OF 13)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 61 OF 303	

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TP_P3E_CPU1_RX_PE2D_DP<3>	AY56	PE2D_RX_DP<15>	PE2D_TX_DP<15>	AW47	TP_P3E_CPU1_TX_PE2D_DP<3>
TP_P3E_CPU1_RX_PE2D_DP<2>	AY58	PE2D_RX_DP<14>	PE2D_TX_DP<14>	AV48	TP_P3E_CPU1_TX_PE2D_DP<2>
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TP_P3E_CPU1_RX_PE3D_DN<2>	AP46	PE3D_RX_DN<14>	PE3D_TX_DN<14>	AA43	TP_P3E_CPU1_TX_PE3D_DN<2>
TP_P3E_CPU1_RX_PE3D_DN<1>	AR47	PE3D_RX_DN<13>	PE3D_TX_DN<13>	AB44	TP_P3E_CPU1_TX_PE3D_DN<1>
TP_P3E_CPU1_RX_PE3D_DN<0>	AJ47	PE3D_RX_DN<12>	PE3D_TX_DN<12>	AC45	TP_P3E_CPU1_TX_PE3D_DN<0>

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CPU SOCKET 1 (7 OF 13)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 62 OF 303	

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U7H1
IC

SANDYBRIDGE_EP_EXT_D

132< IN XDP_CPU1_MBP_N<7..0>

7	XDP_CPU1_MBP_N<7>	AY44	BPM_N<7>
6	XDP_CPU1_MBP_N<6>	BA43	BPM_N<6>
5	XDP_CPU1_MBP_N<5>	AW43	BPM_N<5>
4	XDP_CPU1_MBP_N<4>	BB44	BPM_N<4>
3	XDP_CPU1_MBP_N<3>	AV44	BPM_N<3>
2	XDP_CPU1_MBP_N<2>	AU43	BPM_N<2>
1	XDP_CPU1_MBP_N<1>	AT44	BPM_N<1>
0	XDP_CPU1_MBP_N<0>	AR43	BPM_N<0>

CAD NOTE: PLACE CLOSE TO CPU

109<> 86<> 40<> 40> BI FM_CPU_ONLY_RESET — R2T16 1 2 36.0 A93549-074 1/16W 5% 0402LF — FM_CPU_ONLY_RESET_R AN43 CPU_ONLY_RESET

SOCKET1

NC_CPU1_RSVD<16>	A53	RSVD<16>	
NC_CPU1_RSVD<14>	C53	RSVD<14>	
NC_CPU1_RSVD<15>	B46	RSVD<15>	
NC_CPU1_RSVD<13>	D46	RSVD<13>	
NC_CPU1_RSVD<3>	K58	RSVD<3>	
NC_CPU1_RSVD<60>	AY46	RSVD<60>	
NC_CPU1_RSVD<61>	AV46	RSVD<61>	
NC_CPU1_RSVD<64>	AM44	RSVD<64>	
NC_CPU1_RSVD<65>	AL55	RSVD<65>	
NC_CPU1_RSVD<66>	AJ55	RSVD<66>	
NC_CPU1_RSVD<55>	BD48	RSVD<55>	

TP_DMI_CPU1_RX_DP<3>	B50	DMI_RX_DP<3>	DMI_TX_DP<3>
TP_DMI_CPU1_RX_DP<2>	C49	DMI_RX_DP<2>	DMI_TX_DP<2>
TP_DMI_CPU1_RX_DP<1>	B48	DMI_RX_DP<1>	DMI_TX_DP<1>
TP_DMI_CPU1_RX_DP<0>	C47	DMI_RX_DP<0>	DMI_TX_DP<0>
TP_DMI_CPU1_RX_DN<3>	D50	DMI_RX_DN<3>	DMI_TX_DN<3>
TP_DMI_CPU1_RX_DN<2>	E49	DMI_RX_DN<2>	DMI_TX_DN<2>
TP_DMI_CPU1_RX_DN<1>	D48	DMI_RX_DN<1>	DMI_TX_DN<1>
TP_DMI_CPU1_RX_DN<0>	E47	DMI_RX_DN<0>	DMI_TX_DN<0>

53< OUT PD_CPU1_TEST<3..0>

3	PD_CPU1_TEST<3>	D4	TEST3
2	PD_CPU1_TEST<2>	F2	TEST2
1	PD_CPU1_TEST<1>	CW1	TEST1
0	PD_CPU1_TEST<0>	DB4	TEST0

53> IN A_CPU1_DDR23_RCOMP<2..0>

2	A_CPU1_DDR23_RCOMP<2>	Y14	DDR23_RCOMP<2>
1	A_CPU1_DDR23_RCOMP<1>	AC15	DDR23_RCOMP<1>
0	A_CPU1_DDR23_RCOMP<0>	U15	DDR23_RCOMP<0>

53> IN A_CPU1_DDR01_RCOMP<2..0>

2	A_CPU1_DDR01_RCOMP<2>	CB20	DDR01_RCOMP<2>
1	A_CPU1_DDR01_RCOMP<1>	CC19	DDR01_RCOMP<1>
0	A_CPU1_DDR01_RCOMP<0>	CA17	DDR01_RCOMP<0>

109> 86> 78< 40> OUT FM_CPU_ERR_N<2..0>

2	FM_CPU_ERR_N<2>	BC51	ERROR_N<2>
1	FM_CPU_ERR_N<1>	CB54	ERROR_N<1>
0	FM_CPU_ERR_N<0>	BD50	ERROR_N<0>

RSVD<45>	BJ45	NC_CPU1_RSVD<45>	
RSVD<38>	BP44	NC_CPU1_RSVD<38>	
RSVD<49>	BG45	NC_CPU1_RSVD<49>	
RSVD<42>	BL45	NC_CPU1_RSVD<42>	
RSVD<47>	BH46	NC_CPU1_RSVD<47>	
RSVD<44>	BK44	NC_CPU1_RSVD<44>	
RSVD<53>	BE45	NC_CPU1_RSVD<53>	
RSVD<48>	BH44	NC_CPU1_RSVD<48>	
RSVD<57>	BD44	NC_CPU1_RSVD<57>	
RSVD<56>	BD46	NC_CPU1_RSVD<56>	
RSVD<51>	BF46	NC_CPU1_RSVD<51>	
RSVD<36>	BR43	NC_CPU1_RSVD<36>	
RSVD<43>	BL43	NC_CPU1_RSVD<43>	
RSVD<33>	BU43	NC_CPU1_RSVD<33>	
RSVD<50>	BG43	NC_CPU1_RSVD<50>	
RSVD<41>	BM44	NC_CPU1_RSVD<41>	
RSVD<46>	BJ43	NC_CPU1_RSVD<46>	
RSVD<54>	BE43	NC_CPU1_RSVD<54>	

RSVD<68>	AP48	NC_CPU1_RSVD<68>	
RSVD<11>	E53	NC_CPU1_RSVD<11>	
RSVD<34>	BT44	NC_CPU1_RSVD<34>	
RSVD<52>	BE47	NC_CPU1_RSVD<52>	
RSVD<0>	Y48	NC_CPU1_RSVD<0>	
RSVD<2>	M48	NC_CPU1_RSVD<2>	
RSVD<4>	J15	NC_CPU1_RSVD<4>	
RSVD<6>	H56	NC_CPU1_RSVD<6>	
RSVD<9>	F46	NC_CPU1_RSVD<9>	
RSVD<27>	CG11	NC_CPU1_RSVD<27>	
RSVD<28>	CF44	NC_CPU1_RSVD<28>	
RSVD<29>	CE43	NC_CPU1_RSVD<29>	
RSVD<30>	CD44	NC_CPU1_RSVD<30>	
RSVD<1>	W15	NC_CPU1_RSVD<1>	
RSVD<35>	BR47	NC_CPU1_RSVD<35>	
RSVD<39>	BN47	NC_CPU1_RSVD<39>	
RSVD<26>	CP54	NC_CPU1_RSVD<26>	
RSVD<58>	BC47	NC_CPU1_RSVD<58>	
RSVD<67>	AB48	NC_CPU1_RSVD<67>	

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CPU SOCKET 1 (8 OF 13)

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DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 63 OF 303	

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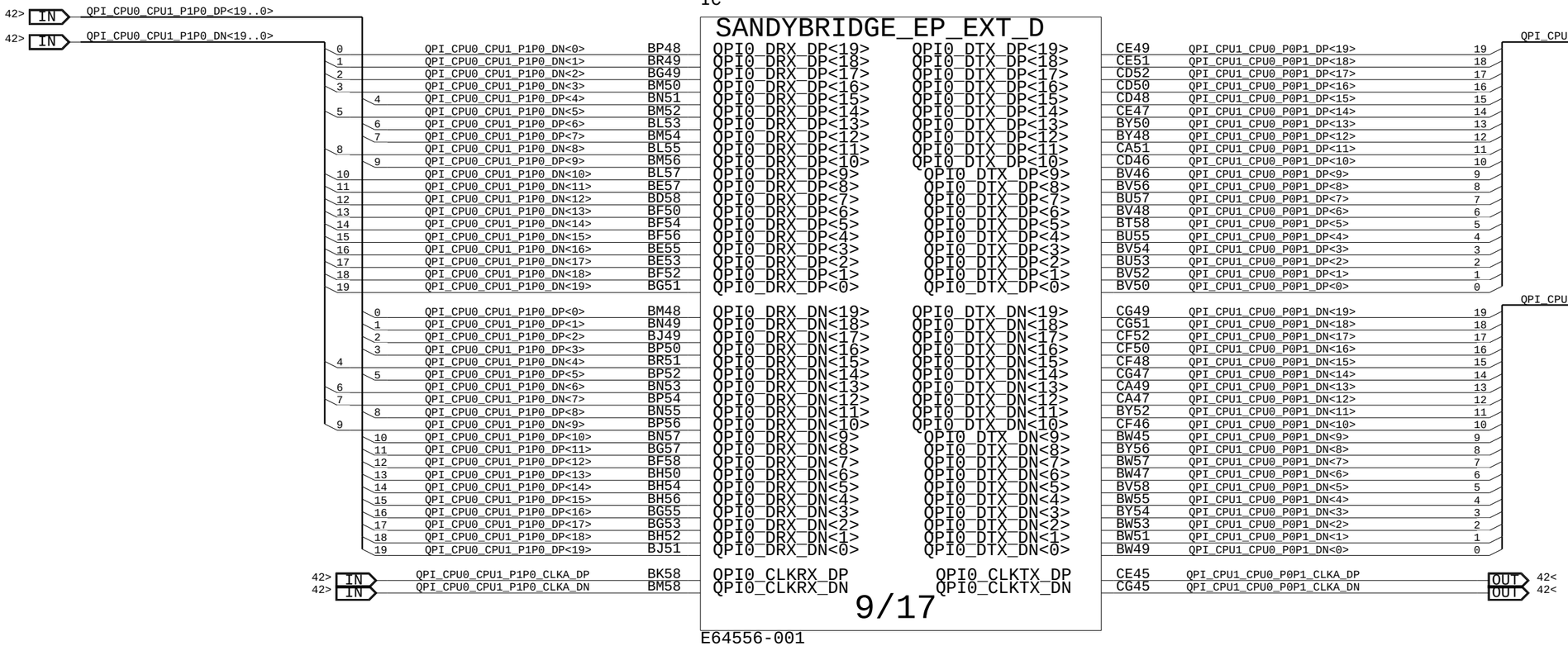
NOTE: QPI P0 RX NETS WITH LANE REVERSAL

NOTE: POLARITY INVERSION ON LANES 0,1,2,3,5,8,10,11,12,13,14,15,16,17,18,19



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CPU SOCKET 1 (9 OF 13)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 64 OF 303	

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NOTE: QPI P1 RX NETS WITH LANE REVERSAL

NOTE: POLARITY INVERSION ON LANES 4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19

U7H1
IC
SANDYBRIDGE_EP_EXT_D

87> IN QPI_CPU2_CPU1_P0P1_DP<19..0>
87> IN QPI_CPU2_CPU1_P0P1_DN<19..0>

0	QPI_CPU2_CPU1_P0P1_DP<0>	CL45	QPI1_DRX_DP<19>	QPI1_DTX_DP<19>	DB42	QPI_CPU1_CPU2_P1P0_DP<19>	19	
1	QPI_CPU2_CPU1_P0P1_DP<1>	CK46	QPI1_DRX_DP<18>	QPI1_DTX_DP<18>	DE43	QPI_CPU1_CPU2_P1P0_DP<18>	18	
2	QPI_CPU2_CPU1_P0P1_DP<2>	CL47	QPI1_DRX_DP<17>	QPI1_DTX_DP<17>	CU43	QPI_CPU1_CPU2_P1P0_DP<17>	17	
3	QPI_CPU2_CPU1_P0P1_DP<3>	CK48	QPI1_DRX_DP<16>	QPI1_DTX_DP<16>	DB44	QPI_CPU1_CPU2_P1P0_DP<16>	16	
4	QPI_CPU2_CPU1_P0P1_DN<4>	CN49	QPI1_DRX_DP<15>	QPI1_DTX_DP<15>	DE45	QPI_CPU1_CPU2_P1P0_DP<15>	15	
5	QPI_CPU2_CPU1_P0P1_DN<5>	CM50	QPI1_DRX_DP<14>	QPI1_DTX_DP<14>	CT44	QPI_CPU1_CPU2_P1P0_DP<14>	14	
6	QPI_CPU2_CPU1_P0P1_DN<6>	CN51	QPI1_DRX_DP<13>	QPI1_DTX_DP<13>	DB46	QPI_CPU1_CPU2_P1P0_DP<13>	13	
7	QPI_CPU2_CPU1_P0P1_DN<7>	CV52	QPI1_DRX_DP<12>	QPI1_DTX_DP<12>	DE47	QPI_CPU1_CPU2_P1P0_DP<12>	12	
8	QPI_CPU2_CPU1_P0P1_DN<8>	CU53	QPI1_DRX_DP<11>	QPI1_DTX_DP<11>	CU45	QPI_CPU1_CPU2_P1P0_DP<11>	11	
9	QPI_CPU2_CPU1_P0P1_DN<9>	CK52	QPI1_DRX_DP<10>	QPI1_DTX_DP<10>	DB48	QPI_CPU1_CPU2_P1P0_DP<10>	10	
10	QPI_CPU2_CPU1_P0P1_DN<10>	CJ53	QPI1_DRX_DP<9>	QPI1_DTX_DP<9>	DC49	QPI_CPU1_CPU2_P1P0_DP<9>	9	
11	QPI_CPU2_CPU1_P0P1_DN<11>	CT56	QPI1_DRX_DP<8>	QPI1_DTX_DP<8>	CT46	QPI_CPU1_CPU2_P1P0_DP<8>	8	
12	QPI_CPU2_CPU1_P0P1_DN<12>	CR57	QPI1_DRX_DP<7>	QPI1_DTX_DP<7>	DD50	QPI_CPU1_CPU2_P1P0_DP<7>	7	
13	QPI_CPU2_CPU1_P0P1_DN<13>	CP58	QPI1_DRX_DP<6>	QPI1_DTX_DP<6>	DC51	QPI_CPU1_CPU2_P1P0_DP<6>	6	
14	QPI_CPU2_CPU1_P0P1_DN<14>	CK54	QPI1_DRX_DP<5>	QPI1_DTX_DP<5>	CU47	QPI_CPU1_CPU2_P1P0_DP<5>	5	
15	QPI_CPU2_CPU1_P0P1_DN<15>	CK56	QPI1_DRX_DP<4>	QPI1_DTX_DP<4>	DD52	QPI_CPU1_CPU2_P1P0_DP<4>	4	
16	QPI_CPU2_CPU1_P0P1_DN<16>	CJ55	QPI1_DRX_DP<3>	QPI1_DTX_DP<3>	DA53	QPI_CPU1_CPU2_P1P0_DP<3>	3	
17	QPI_CPU2_CPU1_P0P1_DN<17>	CD54	QPI1_DRX_DP<2>	QPI1_DTX_DP<2>	CU49	QPI_CPU1_CPU2_P1P0_DP<2>	2	
18	QPI_CPU2_CPU1_P0P1_DN<18>	CD56	QPI1_DRX_DP<1>	QPI1_DTX_DP<1>	CT50	QPI_CPU1_CPU2_P1P0_DP<1>	1	
19	QPI_CPU2_CPU1_P0P1_DN<19>	CC55	QPI1_DRX_DP<0>	QPI1_DTX_DP<0>	CT48	QPI_CPU1_CPU2_P1P0_DP<0>	0	

QPI_CPU1_CPU2_P1P0_DP<19..0> OUT 87<

0	QPI_CPU2_CPU1_P0P1_DN<0>	CN45	QPI1_DRX_DN<19>	QPI1_DTX_DN<19>	DD42	QPI_CPU1_CPU2_P1P0_DN<19>	19	
1	QPI_CPU2_CPU1_P0P1_DN<1>	CM46	QPI1_DRX_DN<18>	QPI1_DTX_DN<18>	DC43	QPI_CPU1_CPU2_P1P0_DN<18>	18	
2	QPI_CPU2_CPU1_P0P1_DN<2>	CN47	QPI1_DRX_DN<17>	QPI1_DTX_DN<17>	CW43	QPI_CPU1_CPU2_P1P0_DN<17>	17	
3	QPI_CPU2_CPU1_P0P1_DN<3>	CM48	QPI1_DRX_DN<16>	QPI1_DTX_DN<16>	DD44	QPI_CPU1_CPU2_P1P0_DN<16>	16	
4	QPI_CPU2_CPU1_P0P1_DP<4>	CL49	QPI1_DRX_DN<15>	QPI1_DTX_DN<15>	DC45	QPI_CPU1_CPU2_P1P0_DN<15>	15	
5	QPI_CPU2_CPU1_P0P1_DP<5>	CK50	QPI1_DRX_DN<14>	QPI1_DTX_DN<14>	CV44	QPI_CPU1_CPU2_P1P0_DN<14>	14	
6	QPI_CPU2_CPU1_P0P1_DP<6>	CL51	QPI1_DRX_DN<13>	QPI1_DTX_DN<13>	DD46	QPI_CPU1_CPU2_P1P0_DN<13>	13	
7	QPI_CPU2_CPU1_P0P1_DP<7>	CT52	QPI1_DRX_DN<12>	QPI1_DTX_DN<12>	DC47	QPI_CPU1_CPU2_P1P0_DN<12>	12	
8	QPI_CPU2_CPU1_P0P1_DP<8>	CR53	QPI1_DRX_DN<11>	QPI1_DTX_DN<11>	CW45	QPI_CPU1_CPU2_P1P0_DN<11>	11	
9	QPI_CPU2_CPU1_P0P1_DP<9>	CM52	QPI1_DRX_DN<10>	QPI1_DTX_DN<10>	DD48	QPI_CPU1_CPU2_P1P0_DN<10>	10	
10	QPI_CPU2_CPU1_P0P1_DP<10>	CL53	QPI1_DRX_DN<9>	QPI1_DTX_DN<9>	DE49	QPI_CPU1_CPU2_P1P0_DN<9>	9	
11	QPI_CPU2_CPU1_P0P1_DP<11>	CV56	QPI1_DRX_DN<8>	QPI1_DTX_DN<8>	CV46	QPI_CPU1_CPU2_P1P0_DN<8>	8	
12	QPI_CPU2_CPU1_P0P1_DP<12>	CU57	QPI1_DRX_DN<7>	QPI1_DTX_DN<7>	DB50	QPI_CPU1_CPU2_P1P0_DN<7>	7	
13	QPI_CPU2_CPU1_P0P1_DP<13>	CT58	QPI1_DRX_DN<6>	QPI1_DTX_DN<6>	DE51	QPI_CPU1_CPU2_P1P0_DN<6>	6	
14	QPI_CPU2_CPU1_P0P1_DP<14>	CM54	QPI1_DRX_DN<5>	QPI1_DTX_DN<5>	CW47	QPI_CPU1_CPU2_P1P0_DN<5>	5	
15	QPI_CPU2_CPU1_P0P1_DP<15>	CM56	QPI1_DRX_DN<4>	QPI1_DTX_DN<4>	DB52	QPI_CPU1_CPU2_P1P0_DN<4>	4	
16	QPI_CPU2_CPU1_P0P1_DP<16>	CL55	QPI1_DRX_DN<3>	QPI1_DTX_DN<3>	DC53	QPI_CPU1_CPU2_P1P0_DN<3>	3	
17	QPI_CPU2_CPU1_P0P1_DP<17>	CF54	QPI1_DRX_DN<2>	QPI1_DTX_DN<2>	CW49	QPI_CPU1_CPU2_P1P0_DN<2>	2	
18	QPI_CPU2_CPU1_P0P1_DP<18>	CF56	QPI1_DRX_DN<1>	QPI1_DTX_DN<1>	CV50	QPI_CPU1_CPU2_P1P0_DN<1>	1	
19	QPI_CPU2_CPU1_P0P1_DP<19>	CE55	QPI1_DRX_DN<0>	QPI1_DTX_DN<0>	CV48	QPI_CPU1_CPU2_P1P0_DN<0>	0	

QPI_CPU1_CPU2_P1P0_DN<19..0> OUT 87<

87> IN	QPI_CPU2_CPU1_P0P1_CLKA_DP	CR55	QPI1_CLKRX_DP	QPI1_CLKTX_DP	DB54	QPI_CPU1_CPU2_P1P0_CLKA_DP		OUT 87<
87> IN	QPI_CPU2_CPU1_P0P1_CLKA_DN	CU55	QPI1_CLKRX_DN	QPI1_CLKTX_DN	CY54	QPI_CPU1_CPU2_P1P0_CLKA_DN		OUT 87<

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CPU SOCKET 1 (10 OF 13)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 65 OF 303	

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P1V05_VCCP_CPU1

1.05

U7H1
IC
SANDYBRIDGE_EP_EXT_D

CA29	VCC<207>	VCC<155>	BP10
CA25	VCC<206>	VCC<154>	BN9
BY40	VCC<205>	VCC<153>	BN7
BY38	VCC<204>	VCC<152>	BN5
BY36	VCC<203>	VCC<151>	BN3
BY34	VCC<202>	VCC<150>	BN17
BY32	VCC<201>	VCC<149>	BN15
BY30	VCC<200>	VCC<148>	BN13
BY28	VCC<199>	VCC<147>	BN11
BY26	VCC<198>	VCC<146>	BN1
BY18	VCC<197>	VCC<145>	BK8
BV8	VCC<196>	VCC<144>	BK6
BV6	VCC<195>	VCC<143>	BK4
BV4	VCC<194>	VCC<142>	BK2
BV2	VCC<193>	VCC<141>	BK16
BV16	VCC<192>	VCC<140>	BK14
BV14	VCC<191>	VCC<139>	BK12
BV12	VCC<190>	VCC<138>	BK10
BV10	VCC<189>	VCC<137>	BJ9
BU9	VCC<188>	VCC<136>	BJ7
BU7	VCC<187>	VCC<135>	BJ5
BU5	VCC<186>	VCC<134>	BJ3
BU3	VCC<185>	VCC<133>	BJ17
BU17	VCC<184>	VCC<132>	BJ15
BU15	VCC<183>	VCC<131>	BJ13
BU13	VCC<182>	VCC<130>	BJ11
BU11	VCC<181>	VCC<129>	BJ1
BU1	VCC<180>	VCC<128>	BH8
BT8	VCC<179>	VCC<127>	BH6
BT6	VCC<178>	VCC<126>	BH4
BT4	VCC<177>	VCC<125>	BH2
BT2	VCC<176>	VCC<124>	BH16
BT16	VCC<175>	VCC<123>	BH14
BT14	VCC<174>	VCC<122>	BH12
BT12	VCC<173>	VCC<121>	BH10
BT10	VCC<172>	VCC<120>	BG9
BR9	VCC<171>	VCC<119>	BG7
BR7	VCC<170>	VCC<118>	BG5
BR5	VCC<169>	VCC<117>	BG3
BR3	VCC<168>	VCC<116>	BG17
BR17	VCC<167>	VCC<115>	BG15
BR15	VCC<166>	VCC<114>	BG13
BR13	VCC<165>	VCC<113>	BG11
BR11	VCC<164>	VCC<112>	BG1
BR1	VCC<163>	VCC<111>	BF8
BP8	VCC<162>	VCC<110>	BF6
BP6	VCC<161>	VCC<109>	BF4
BP4	VCC<160>	VCC<108>	BF2
BP2	VCC<159>	VCC<107>	BF16
BP16	VCC<158>	VCC<106>	BF14
BP14	VCC<157>	VCC<105>	BF12
BP12	VCC<156>	VCC<104>	BF10

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P1V05_VCCP_CPU1

1.05

U7H1
IC
SANDYBRIDGE_EP_EXT_D

BE9	VCC<103>	VCC<51>	AU7
BE7	VCC<102>	VCC<50>	AU5
BE5	VCC<101>	VCC<49>	AU3
BE3	VCC<100>	VCC<48>	AU17
BE17	VCC<99>	VCC<47>	AU15
BE15	VCC<98>	VCC<46>	AU13
BE13	VCC<97>	VCC<45>	AU11
BE11	VCC<96>	VCC<44>	AU1
BE1	VCC<95>	VCC<43>	AP8
BB8	VCC<94>	VCC<42>	AP6
BB6	VCC<93>	VCC<41>	AP4
BB4	VCC<92>	VCC<40>	AP2
BB2	VCC<91>	VCC<39>	AP16
BB16	VCC<90>	VCC<38>	AP14
BB14	VCC<89>	VCC<37>	AP12
BB12	VCC<88>	VCC<36>	AP10
BB10	VCC<87>	VCC<35>	AN9
BA9	VCC<86>	VCC<34>	AN7
BA7	VCC<85>	VCC<33>	AN5
BA5	VCC<84>	VCC<32>	AN3
BA3	VCC<83>	VCC<31>	AN17
BA17	VCC<82>	VCC<30>	AN15
BA15	VCC<81>	VCC<29>	AN13
BA13	VCC<80>	VCC<28>	AN11
BA11	VCC<79>	VCC<27>	AN1
BA1	VCC<78>	VCC<26>	AM8
AY8	VCC<77>	VCC<25>	AM6
AY6	VCC<76>	VCC<24>	AM4
AY4	VCC<75>	VCC<23>	AM2
AY2	VCC<74>	VCC<22>	AM16
AY16	VCC<73>	VCC<21>	AM14
AY14	VCC<72>	VCC<20>	AM12
AY12	VCC<71>	VCC<19>	AM10
AY10	VCC<70>	VCC<18>	AL9
AW9	VCC<69>	VCC<17>	AL7
AW7	VCC<68>	VCC<16>	AL5
AW5	VCC<67>	VCC<15>	AL3
AW3	VCC<66>	VCC<14>	AL17
AW17	VCC<65>	VCC<13>	AL15
AW15	VCC<64>	VCC<12>	AL13
AW13	VCC<63>	VCC<11>	AL11
AW11	VCC<62>	VCC<10>	AL1
AW1	VCC<61>	VCC<9>	AG41
AV8	VCC<60>	VCC<8>	AG39
AV6	VCC<59>	VCC<7>	AG37
AV4	VCC<58>	VCC<6>	AG35
AV2	VCC<57>	VCC<5>	AG33
AV16	VCC<56>	VCC<4>	AG31
AV14	VCC<55>	VCC<3>	AG29
AV12	VCC<54>	VCC<2>	AG27
AV10	VCC<53>	VCC<1>	AG25
AU9	VCC<52>	VCC<0>	AG19

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CPU SOCKET 1 (11 OF 13)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 66 OF 303	

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U7H1
IC
SANDYBRIDGE_EP_EXT_D

P1V05_VTT_CPU1
1.05

P1V5_DDR3_CPU1
1.5

P1V5_DDR3_CPU1
1.5

P1V05_VTT_CPU1
1.05

DA49	VTTA<2>	VCC_SENSE	BW3	VSENSE_DIE_CPU1_VCCP_P	OUT	241<	
CR51	VTTA<3>	RSVD<20>	DB56	NC_CPU1_RSVD<20>			
CR45	VTTA<4>	VSS_VCC_SENSE	BY2	VSENSE_DIE_CPU1_VCCP_N	OUT	241<	
CJ49	VTTA<5>	VTTD_SENSE	BP42	VSENSE_DIE_CPU1_VTT_P	OUT	270>	
CG55	VTTA<6>	VSS_VTTD_SENSE	BT42	VSENSE_DIE_CPU1_VTT_N	OUT	270>	
CC45	VTTA<7>						
CA53	VTTA<8>	VCCPLL<1>	CA13				
		VCCPLL<2>	BY14				
BV42	VTTD<4>	VCCPLL<0>	CA15				
				P1V8_PLL_CPU1			
				1.8			
V24	VCCD_23<5>	VSS_VSA_SENSE	AF14	VSENSE_DIE_VSA1_N	OUT	242<	
V22	VCCD_23<6>	VSA_SENSE	AG13	VSENSE_DIE_VSA1_P	OUT	242<	
V20	VCCD_23<7>						
V18	VCCD_23<8>	VSA<24>	N51				
V16	VCCD_23<9>	VSA<23>	N45				
N23	VCCD_23<10>	VSA<22>	G49				
N21	VCCD_23<11>	VSA<21>	G43				
N19	VCCD_23<12>	VSA<20>	B54				
N17	VCCD_23<13>	VSA<19>	AJ9	P0V85_VSA_CPU1			
N15	VCCD_23<14>	VSA<18>	AJ7	0.85			
H24	VCCD_23<15>	VSA<17>	AJ5				
H22	VCCD_23<16>	VSA<16>	AJ3				
H20	VCCD_23<17>	VSA<15>	AJ13				
H18	VCCD_23<18>	VSA<14>	AJ11				
H16	VCCD_23<19>	VSA<13>	AJ1				
G13	VCCD_23<20>	VSA<12>	AH8				
C23	VCCD_23<21>	VSA<11>	AH6				
C21	VCCD_23<22>	VSA<10>	AH4				
C19	VCCD_23<23>	VSA<9>	AH2				
C17	VCCD_23<24>	VSA<8>	AH16				
C15	VCCD_23<25>	VSA<7>	AH14				
AC25	VCCD_23<0>	VSA<6>	AH12				
AC23	VCCD_23<1>	VSA<5>	AH10				
AC21	VCCD_23<2>	VSA<4>	AG17				
AC19	VCCD_23<3>	VSA<3>	AG15				
AC17	VCCD_23<4>	VSA<2>	AF18				
		VSA<1>	AE17				
		VSA<0>	AE15				
DD26	VCCD_01<0>						
DD24	VCCD_01<1>	VTTA<0>	Y54				
DD22	VCCD_01<2>	VTTA<1>	W49	P1V05_VTT_CPU1			
DD20	VCCD_01<3>	VTTA<9>	AU53	1.05			
DD18	VCCD_01<4>	VTTA<10>	AM54				
CW27	VCCD_01<5>	VTTA<11>	AM48				
CW25	VCCD_01<6>	VTTA<12>	AE53				
CW23	VCCD_01<7>	VTTA<13>	AE45				
CW21	VCCD_01<8>						
CW19	VCCD_01<9>	VTTD<0>	CA23				
CP28	VCCD_01<10>	VTTD<1>	CA21	P1V05_VTT_CPU1			
CP26	VCCD_01<11>	VTTD<2>	BY22	1.05			
CP24	VCCD_01<12>	VTTD<3>	BY20				
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CP20	VCCD_01<14>	VTTD<6>	BR55				
CJ27	VCCD_01<15>	VTTD<9>	BK56				
CJ25	VCCD_01<16>	VTTD<7>	BM42				
CJ23	VCCD_01<17>	VTTD<10>	BH42				
CJ21	VCCD_01<18>	VTTD<11>	BD42				
CJ19	VCCD_01<19>	VTTD<12>	AY42				
CD28	VCCD_01<20>	VTTD<13>	AT42				
CD26	VCCD_01<21>	VTTD<14>	AM42				
CD24	VCCD_01<22>	VTTD<15>	AG23				
CD22	VCCD_01<23>	VTTD<16>	AG21				
CD20	VCCD_01<24>	VTTD<17>	AF24				
		VTTD<18>	AF22				
		VTTD<8>	BL51				

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U7H1
IC
SANDYBRIDGE_EP_EXT_D

CY40	VSS<547>				
AW55	VSS<546>				
AG43	VSS<545>	VSS<477>	N9		
CW51	VSS<544>	VSS<476>	N53		
C3	VSS<543>	VSS<475>	N5		
D2	VSS<542>	VSS<474>	N49		
DB2	VSS<541>	VSS<473>	N47		
DC3	VSS<540>	VSS<472>	N43		
E1	VSS<539>	VSS<471>	N41		
V46	VSS<538>	VSS<470>	N37		
BG47	VSS<537>	VSS<469>	N35		
BK50	VSS<536>	VSS<468>	N33		
AU51	VSS<535>	VSS<467>	N13		
Y56	VSS<534>	VSS<466>	M8		
Y42	VSS<533>	VSS<465>	M52		
Y40	VSS<532>	VSS<464>	M50		
Y38	VSS<531>	VSS<463>	M46		
Y36	VSS<530>	VSS<462>	M44		
Y32	VSS<529>	VSS<461>	M42		
Y30	VSS<528>	VSS<460>	M36		
Y28	VSS<527>	VSS<459>	M34		
Y12	VSS<526>	VSS<458>	L5		
Y10	VSS<525>	VSS<457>	L41		
W9	VSS<524>	VSS<456>	L29		
W53	VSS<523>	VSS<455>	L25		
W51	VSS<522>	VSS<454>	K8		
W5	VSS<521>	VSS<453>	K34		
W47	VSS<520>	VSS<452>	K30		
W45	VSS<519>	VSS<451>	K28		
W43	VSS<518>	VSS<450>	K2		
W41	VSS<517>	VSS<449>	J55		
W37	VSS<516>	VSS<448>	J5		
W33	VSS<515>	VSS<447>	J41		
W13	VSS<514>	VSS<446>	J39		
V8	VSS<513>	VSS<445>	J33		
V50	VSS<512>	VSS<444>	J31		
V48	VSS<511>	VSS<443>	J27		
V44	VSS<510>	VSS<442>	J11		
V42	VSS<509>	VSS<441>	H8		
V36	VSS<508>	VSS<440>	H54		
V34	VSS<507>	VSS<439>	H52		
V28	VSS<506>	VSS<438>	H40		
V26	VSS<505>	VSS<437>	H38		
U5	VSS<504>	VSS<436>	H34		
U35	VSS<503>	VSS<435>	H32		
T8	VSS<502>	VSS<434>	K26		
T6	VSS<501>	VSS<433>	H14		
T42	VSS<500>	VSS<432>	H12		
T4	VSS<499>	VSS<431>	H10		
T28	VSS<498>	VSS<430>	G9		
R7	VSS<497>	VSS<429>	G57		
R55	VSS<496>	VSS<428>	G53		
R5	VSS<495>	VSS<427>	G51		
R39	VSS<494>	VSS<426>	G5		
R35	VSS<493>	VSS<425>	G47		
R31	VSS<492>	VSS<424>	G45		
R3	VSS<491>	VSS<423>	G41		
R29	VSS<490>	VSS<422>	G37		
R11	VSS<489>	VSS<421>	G35		
P8	VSS<488>	VSS<420>	G31		
P56	VSS<487>	VSS<419>	G1		
P54	VSS<486>	VSS<418>	F8		
P40	VSS<485>	VSS<417>	F50		
P38	VSS<484>	VSS<416>	F48		
P32	VSS<483>	VSS<415>	F44		
P30	VSS<482>	VSS<414>	F42		
P26	VSS<481>	VSS<413>	F36		
P14	VSS<480>	VSS<412>	G25		
P12	VSS<479>	VSS<411>	E5		
P10	VSS<478>	VSS<410>	E41		

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P1V05_VTT_CPU1
1.05

SOCKET1	SOCKET1	SOCKET1	SOCKET1	SOCKET1	SOCKET1	SOCKET1	SOCKET1	SOCKET1	SOCKET1
C8H18	C8H16	C8G3	C8G2	C8G1	C2U3	C2U2	C2U4	C2V18	C2V16
22UF	22UF	22UF	22UF	22UF	22UF	22UF	22UF	22UF	22UF
4V	4V	4V	4V	4V	4V	4V	4V	4V	4V
20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
C95333-002	C95333-002	C95333-002	C95333-002	C95333-002	C95333-002	C95333-002	C95333-002	C95333-002	C95333-002
0805LF	0805LF	0805LF	0805LF	0805LF	0805LF	0805LF	0805LF	0805LF	0805LF

CAD NOTE:
PLACE IN SOCKET CAVITY

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CPU SOCKET 1 (12 OF 13)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 67 OF 303	

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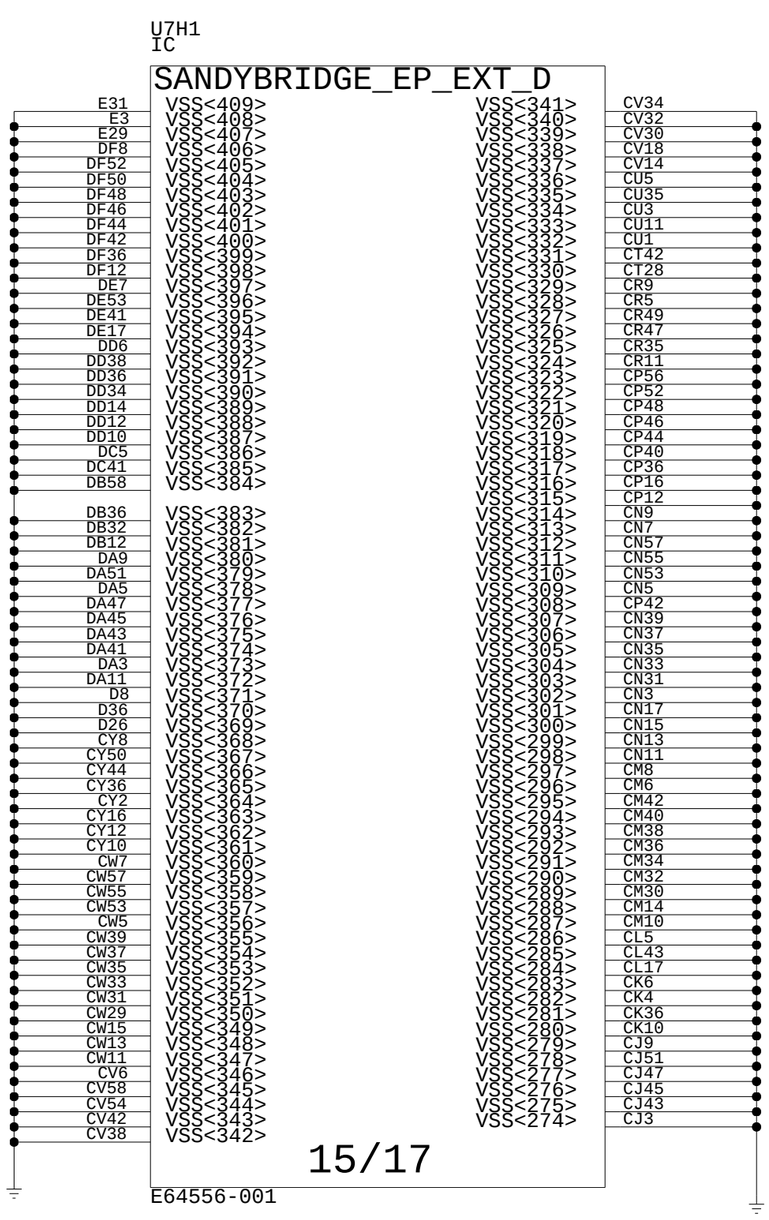

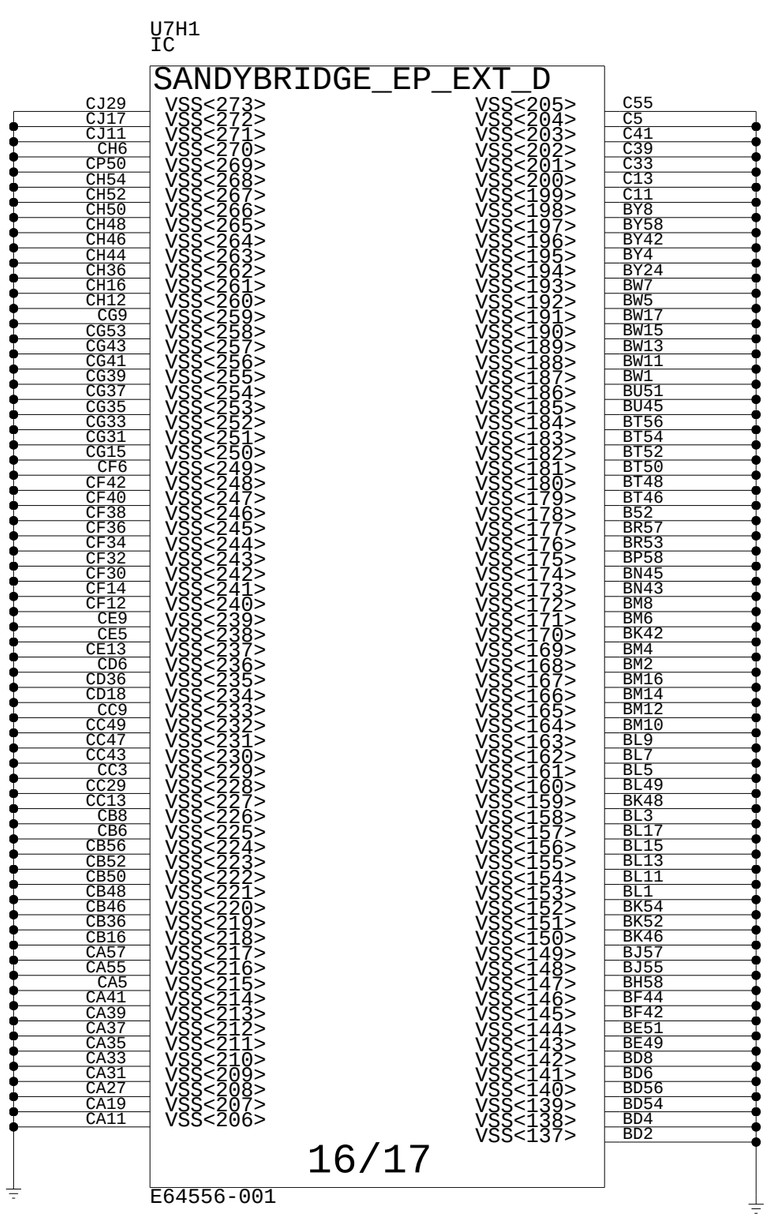

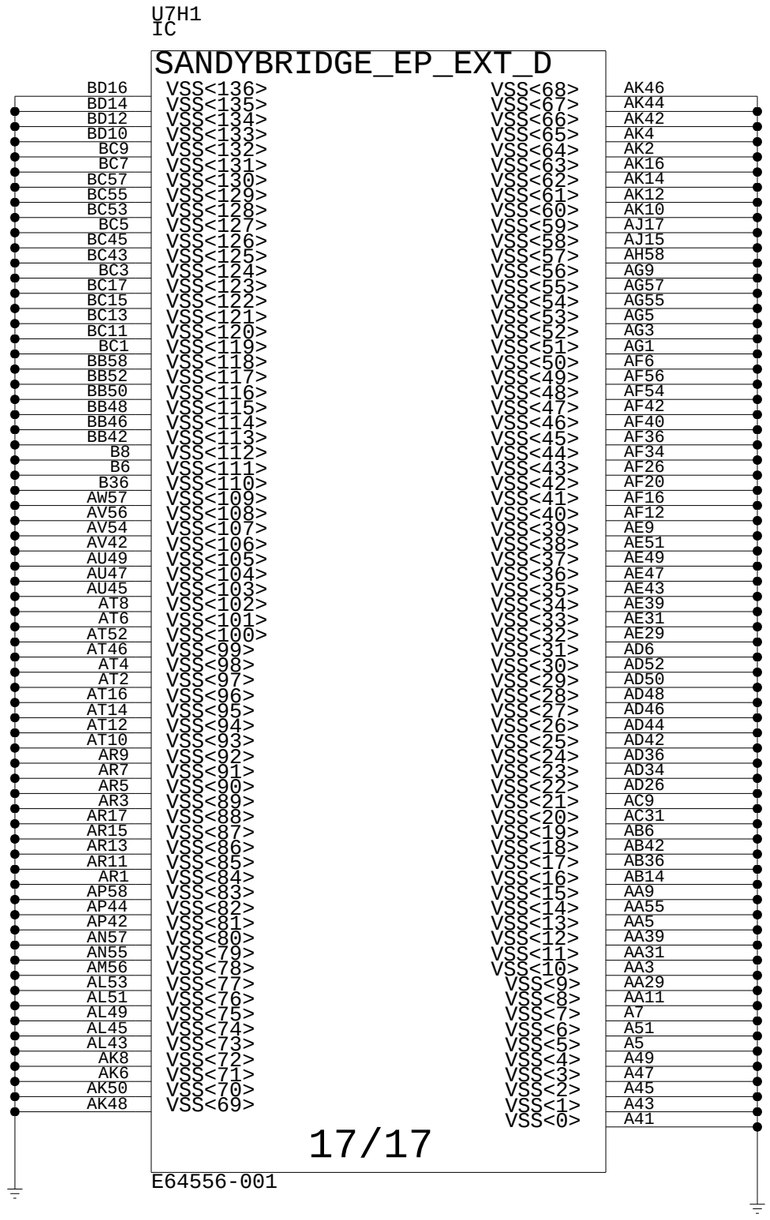

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CPU SOCKET 1 (13 OF 13)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 68 OF 303	

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J9K2

CONN240_E55582004

57> IN	M_E_BA<2>		52	A16_BA2	DQ<63>	234	63
		15	171	A<15>	DQ<62>	233	62
		14	172	A<14>	DQ<61>	228	61
		13	196	A<13>	DQ<60>	227	60
		12	174	A<12>	DQ<59>	115	59
		11	55	A<11>	DQ<58>	114	58
		10	70	A<10>	DQ<57>	109	57
		9	175	A<9>	DQ<56>	108	56
		8	177	A<8>	DQ<55>	225	55
		7	56	A<7>	DQ<54>	224	54
		6	178	A<6>	DQ<53>	219	53
		5	58	A<5>	DQ<52>	218	52
		4	59	A<4>	DQ<51>	106	51
		3	180	A<3>	DQ<50>	105	50
		2	61	A<2>	DQ<49>	100	49
		1	181	A<1>	DQ<48>	99	48
57> IN	M_E_MA<15..0>	0	188	A<0>	DQ<47>	216	47
57> IN	M_E_BA<1..0>				DQ<46>	215	46
		1	190	BA<1>	DQ<45>	210	45
		0	71	BA<0>	DQ<44>	209	44
					DQ<43>	97	43
57> IN	M_E_CK_DP<2>		63	NC_CK1P	DQ<42>	96	42
57> IN	M_E_CK_DN<2>		64	NC_CK1N	DQ<41>	91	41
57> IN	M_E_CK_DP<0>		184	CK0P	DQ<40>	90	40
57> IN	M_E_CK_DN<0>		185	CK0N	DQ<39>	207	39
57> IN	M_E_CS_N<3..0>				DQ<38>	206	38
		3	198	CS<3>	DQ<37>	201	37
		2	79	CS<2>	DQ<36>	200	36
		1	76	CS<1>	DQ<35>	88	35
		0	193	CS<0>	DQ<34>	87	34
					DQ<33>	82	33
57> IN	M_E_CKE<1>		169	CKE<1>	DQ<32>	81	32
57> IN	M_E_CKE<0>		50	CKE<0>	DQ<31>	156	31
					DQ<30>	155	30
57> IN	M_E_WE_N		73	WE_N	DQ<29>	150	29
57> IN	M_E_RAS_N		192	RAS_N	DQ<28>	149	28
57> IN	M_E_CAS_N		74	CAS_N	DQ<27>	37	27
57> IN	M_E_ODT<1..0>				DQ<26>	36	26
		1	77	ODT<1>	DQ<25>	31	25
		0	195	ODT<0>	DQ<24>	30	24
					DQ<23>	147	23
57> IN	M_E_MA_PAR		68	PAR_IN_NC	DQ<22>	146	22
57< OUT	M_E_PAR_ERR_N<0>		53	ERR_OUT_NC	DQ<21>	141	21
57<> BI	M_E_ECC<7..0>				DQ<20>	140	20
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		6	164	CB<6>	DQ<18>	27	18
		5	159	CB<5>	DQ<17>	22	17
		4	158	CB<4>	DQ<16>	21	16
		3	46	CB<3>	DQ<15>	138	15
		2	45	CB<2>	DQ<14>	137	14
		1	40	CB<1>	DQ<13>	132	13
		0	39	CB<0>	DQ<12>	131	12
					DQ<11>	19	11
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					DQ<9>	13	9
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E55582-004

M_E_DQ<63..0> BI 57<>

J9K2

CONN240_E55582004

	VSS<58>	VDD<21>	51	P1V5_DDR3_CPU1 1.5
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8	VSS<55>	VDD<18>	60	
11	VSS<54>	VDD<17>	62	
14	VSS<53>	VDD<16>	65	
17	VSS<52>	VDD<15>	66	
20	VSS<51>	VDD<14>	69	
23	VSS<50>	VDD<13>	72	
26	VSS<49>	VDD<12>	75	
29	VSS<48>	VDD<11>	78	
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41	VSS<44>	VDD<7>	179	
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47	VSS<42>	VDD<5>	183	
80	VSS<41>	VDD<4>	186	
83	VSS<40>	VDD<3>	189	P0V75_VTT_DDR3_CPU1
86	VSS<39>	VDD<2>	191	
89	VSS<38>	VDD<1>	194	0.75
92	VSS<37>	VDD<0>	197	
95	VSS<36>			
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101	VSS<34>	VTT<2>	48	
104	VSS<33>	VTT<1>	120	
107	VSS<32>	VTT<0>	240	
110	VSS<31>			
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223	VSS<4>			
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229	VSS<2>			
232	VSS<1>			
235	VSS<0>			
239				

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E55582-004

P1V5_DDR3_CPU1 1.5

C9H11 10UF 6.3V 20% 602433-075 0603LF

C9H12 10UF 6.3V 20% 602433-075 0603LF

J9K2

CONN240_E55582004

DQS17P_DM8	161	17		M_E_DQS_DP<17..0> BI 57<>
DQS17N_NC	162		17	M_E_DQS_DN<17..0> BI 57<>
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DQS16N_NC	231		16	
DQS15P_DM6	221	15		
DQS15N_NC	222		15	
DQS14P_DM5	212	14		
DQS14N_NC	213		14	
DQS13P_DM4	203	13		
DQS13N_NC	204		13	
DQS12P_DM3	152	12		
DQS12N_NC	153		12	
DQS11P_DM2	143	11		
DQS11N_NC	144		11	
DQS10P_DM1	134	10		
DQS10N_NC	135		10	
DQS9P_DM0	125	9		
DQS9N_NC	126		9	
DQS8P	43	8		
DQS8N	42		8	
DQS7P	112	7		
DQS7N	111		7	
DQS6P	103	6		
DQS6N	102		6	
DQS5P	94	5		
DQS5N	93		5	
DQS4P	85	4		
DQS4N	84		4	
DQS3P	34	3		
DQS3N	33		3	
DQS2P	25	2		
DQS2N	24		2	
DQS1P	16	1		
DQS1N	15		1	
DQS0P	7	0		
DQS0N	6		0	

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E55582-004

P1V5_DDR3_CPU1

R9J15 100 1% 1/16W 1.5

A93548-043 0402LF

0.75 P1V5_DDR3_CPU1_VREF_E_D OUT 69< 73>

R9J16 100 1% 1/16W

C9J3 0.1UF 16V 10%

A93548-043 0402LF

A36096-030 0402LF

P1V5_DDR3_CPU1

R9G2 100 1% 1/16W 1.5

A93548-043 0402LF

0.75 P1V5_DDR3_CPU1_VREF_E_A OUT 69<

R9G1 100 1% 1/16W

C9G1 0.1UF 16V 10%

A93548-043 0402LF

A36096-030 0402LF

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DDR3 CPU1 CHANNEL E DIMM1

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 69 OF 303

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J9K1

CONN240_E55582004

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	14	172	A<14>	DQ<61>	228	61	
	13	196	A<13>	DQ<60>	227	60	
	12	174	A<12>	DQ<59>	115	59	
	11	55	A<11>	DQ<58>	114	58	
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	9	175	A<9>	DQ<56>	108	56	
	8	177	A<8>	DQ<55>	225	55	
	7	56	A<7>	DQ<54>	224	54	
	6	178	A<6>	DQ<53>	219	53	
	5	58	A<5>	DQ<52>	218	52	
	4	59	A<4>	DQ<51>	106	51	
	3	180	A<3>	DQ<50>	105	50	
	2	61	A<2>	DQ<49>	100	49	
	1	181	A<1>	DQ<48>	99	48	
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58> IN	M_F_BA<1..0>			DQ<46>	215	46	
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58> IN	M_F_CK_DP<2>	63	NC_CK1P	DQ<42>	96	42	
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58> IN	M_F_CS_N<3..0>			DQ<38>	206	38	
	3	198	CS<3>	DQ<37>	201	37	
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	1	76	CS<1>	DQ<35>	88	35	
	0	193	CS<0>	DQ<34>	87	34	
				DQ<33>	82	33	
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58> IN	M_F_RAS_N	192	RAS_N	DQ<28>	149	28	
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58> IN	M_F_ODT<1..0>			DQ<26>	36	26	
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58< OUT	M_F_PAR_ERR_N<0>	53	ERR_OUT_NC	DQ<21>	141	21	
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207< 189> 100< OUT	FM_SKT1_DIMM_F1_EVENT_N	187	EVENT_N_NC	DQ<2>	9	2	
73> 70> IN	P1V5_DDR3_CPU1_VREF_F_D	1	VREFDQ	DQ<1>	4	1	
70> IN	P1V5_DDR3_CPU1_VREF_F_A	67	VREFCA	DQ<0>	3	0	

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P3V3

3.3

R9F16 1/16W 1 2 A93548-023 1K 1% 0402LF

SPD ADDRESS = 0XA8

P1V5_DDR3_CPU1

R9J17 100 1% 1/16W 1 2 A93548-043 0402LF — 1.5

0.75

P1V5_DDR3_CPU1_VREF_F_D OUT 70< 73>

R9J18 100 1% 1/16W 1 2 A93548-043 0402LF

C9J5 0.1UF 16V 10% 1 2 A36096-030 0402LF

P1V5_DDR3_CPU1

R9H1 100 1% 1/16W 1 2 A93548-043 0402LF — 1.5

0.75

P1V5_DDR3_CPU1_VREF_F_A OUT 70<

R9H2 100 1% 1/16W 1 2 A93548-043 0402LF

C9H5 0.1UF 16V 10% 1 2 A36096-030 0402LF

J9K1

CONN240_E55582004

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26	VSS<50>	VDD<13>	72
29	VSS<49>	VDD<12>	75
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86	VSS<40>	VDD<3>	189
89	VSS<39>	VDD<2>	191
92	VSS<38>	VDD<1>	194
95	VSS<37>	VDD<0>	197
98	VSS<36>		
101	VSS<35>	VTT<3>	49
104	VSS<34>	VTT<2>	48
107	VSS<33>	VTT<1>	120
110	VSS<32>	VTT<0>	240
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121	VSS<29>	NC_TEST	167 TP_F_D1_NC2
124	VSS<28>		
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166	VSS<14>		
199	VSS<13>		
202	VSS<12>		
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208	VSS<10>		
211	VSS<9>		
214	VSS<8>		
217	VSS<7>		
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223	VSS<5>		
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229	VSS<3>		
232	VSS<2>		
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239	VSS<0>		

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P1V5_DDR3_CPU1 — 1.5

P0V75_VTT_DDR3_CPU1 — 0.75

C9H7 10UF 6.3V 20% 602433-075 0603LF

C9H6 10UF 6.3V 20% 602433-075 0603LF

J9K1

CONN240_E55582004

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DQS17N_NC	162	17	M_F_DQS_DN<17..0> BI 58<>
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DQS16N_NC	231	16	
DQS15P_DM6	221	15	
DQS15N_NC	222	15	
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DQS14N_NC	213	14	
DQS13P_DM4	203	13	
DQS13N_NC	204	13	
DQS12P_DM3	152	12	
DQS12N_NC	153	12	
DQS11P_DM2	143	11	
DQS11N_NC	144	11	
DQS10P_DM1	134	10	
DQS10N_NC	135	10	
DQS9P_DM0	125	9	
DQS9N_NC	126	9	
DQS8P	43	8	
DQS8N	42	8	
DQS7P	112	7	
DQS7N	111	7	
DQS6P	103	6	
DQS6N	102	6	
DQS5P	94	5	
DQS5N	93	5	
DQS4P	85	4	
DQS4N	84	4	
DQS3P	34	3	
DQS3N	33	3	
DQS2P	25	2	
DQS2N	24	2	
DQS1P	16	1	
DQS1N	15	1	
DQS0P	7	0	
DQS0N	6	0	

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Wed Oct 27 15:21:28 2010

DDR3 CPU1 CHANNEL F DIMM1

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 70 OF 303	

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J7F1

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		14 172	A<14>	DQ<61>	228 61
		13 196	A<13>	DQ<60>	227 60
		12 174	A<12>	DQ<59>	115 59
		11 55	A<11>	DQ<58>	114 58
		10 70	A<10>	DQ<57>	109 57
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		8 177	A<8>	DQ<55>	225 55
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		6 178	A<6>	DQ<53>	219 53
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		4 59	A<4>	DQ<51>	106 51
		3 180	A<3>	DQ<50>	105 50
		2 61	A<2>	DQ<49>	100 49
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59> IN	M_G_BA<1..0>			DQ<46>	215 46
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		0 71	BA<0>	DQ<44>	209 44
				DQ<43>	97 43
59> IN	M_G_CK_DP<2>	63	NC_CK1P	DQ<42>	96 42
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59> IN	M_G_CK_DP<0>	184	CK0P	DQ<40>	90 40
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59> IN	M_G_CS_N<3..0>			DQ<38>	206 38
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				DQ<33>	82 33
59> IN	M_G_CKE<1>	169	CKE<1>	DQ<32>	81 32
59> IN	M_G_CKE<0>	50	CKE<0>	DQ<31>	156 31
				DQ<30>	155 30
59> IN	M_G_WE_N	73	WE_N	DQ<29>	150 29
59> IN	M_G_RAS_N	192	RAS_N	DQ<28>	149 28
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59> IN	M_G_ODT<1..0>			DQ<26>	36 26
		1 77	ODT<1>	DQ<25>	31 25
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199> 73<> 72<> BI	SMB_DDR_GH_LVC3_SDA	238	SDA	DQ<4>	122 4
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73> 71> IN	P1V5_DDR3_CPU1_VREF_G_D	1	VREFDQ	DQ<1>	4 1
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J7F1

CONN240_E55582004

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23	VSS<51>	VDD<14>	69
26	VSS<50>	VDD<13>	72
29	VSS<49>	VDD<12>	75
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83	VSS<41>	VDD<4>	186
86	VSS<40>	VDD<3>	189
89	VSS<39>	VDD<2>	191
92	VSS<38>	VDD<1>	194
95	VSS<37>	VDD<0>	197
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104	VSS<34>	VTT<2>	48
107	VSS<33>	VTT<1>	120
110	VSS<32>	VTT<0>	240
113	VSS<31>		
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121	VSS<29>	NC_TEST	167
124	VSS<28>		
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P1V5_DDR3_CPU1

1.5

P1V5_DDR3_CPU1

1.5

C7H14 10UF 6.3V 20% 602433-075 0603LF

C7H11 10UF 6.3V 20% 602433-075 0603LF

P0V75_VTT_DDR3_CPU1

0.75

TP_G_D1_NC2

J7F1

CONN240_E55582004

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DQS17N_NC	162	17	M_G_DQS_DN<17..0>	BI 59<>
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DQS15P_DM6	221	15		
DQS15N_NC	222	15		
DQS14P_DM5	212	14		
DQS14N_NC	213	14		
DQS13P_DM4	203	13		
DQS13N_NC	204	13		
DQS12P_DM3	152	12		
DQS12N_NC	153	12		
DQS11P_DM2	143	11		
DQS11N_NC	144	11		
DQS10P_DM1	134	10		
DQS10N_NC	135	10		
DQS9P_DM0	125	9		
DQS9N_NC	126	9		
DQS8P	43	8		
DQS8N	42	8		
DQS7P	112	7		
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DQS4N	84	4		
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DQS3N	33	3		
DQS2P	25	2		
DQS2N	24	2		
DQS1P	16	1		
DQS1N	15	1		
DQS0P	7	0		
DQS0N	6	0		

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P1V5_DDR3_CPU1

R7G3 100 1% 1/16W 1.5

A93548-043 0402LF 0.75

P1V5_DDR3_CPU1_VREF_G_D OUT 71< 73>

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C7G1 0.1UF 16V 10%

A93548-043 0402LF

A36096-030 0402LF

P1V5_DDR3_CPU1

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A93548-043 0402LF 0.75

P1V5_DDR3_CPU1_VREF_G_A OUT 71<

R7J11 100 1% 1/16W

C7J4 0.1UF 16V 10%

A93548-043 0402LF

A36096-030 0402LF

Wed Oct 27 15:21:28 2010

DDR3 CPU1 CHANNEL G DIMM1

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
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		SCALE:	DO NOT SCALE DRAWING	SHEET 71 OF 303	

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			12 174	A<12>	DQ<59>	115	59
			11 55	A<11>	DQ<58>	114	58
			10 70	A<10>	DQ<57>	109	57
			9 175	A<9>	DQ<56>	108	56
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			4 59	A<4>	DQ<51>	106	51
			3 180	A<3>	DQ<50>	105	50
			2 61	A<2>	DQ<49>	100	49
			1 181	A<1>	DQ<48>	99	48
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					DQ<46>	215	46
60>	IN	M_H_BA<1..0>	1 190	BA<1>	DQ<45>	210	45
			0 71	BA<0>	DQ<44>	209	44
					DQ<43>	97	43
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60>	IN	M_H_CK_DN<2>	64	NC_CK1N	DQ<41>	91	41
60>	IN	M_H_CK_DP<0>	184	CK0P	DQ<40>	90	40
60>	IN	M_H_CK_DN<0>	185	CK0N	DQ<39>	207	39
					DQ<38>	206	38
60>	IN	M_H_CS_N<3..0>			DQ<37>	201	37
			3 198	CS<3>	DQ<36>	200	36
			2 79	CS<2>	DQ<35>	88	35
			1 76	CS<1>	DQ<34>	87	34
			0 193	CS<0>	DQ<33>	82	33
					DQ<32>	81	32
60>	IN	M_H_CKE<1>	169	CKE<1>	DQ<31>	156	31
60>	IN	M_H_CKE<0>	50	CKE<0>	DQ<30>	155	30
					DQ<29>	150	29
60>	IN	M_H_WE_N	73	WE_N	DQ<28>	149	28
60>	IN	M_H_RAS_N	192	RAS_N	DQ<27>	37	27
60>	IN	M_H_CAS_N	74	CAS_N	DQ<26>	36	26
60>	IN	M_H_ODT<1..0>			DQ<25>	31	25
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			0 195	ODT<0>	DQ<23>	147	23
					DQ<22>	146	22
60>	IN	M_H_MA_PAR	68	PAR_IN_NC	DQ<21>	141	21
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60<>	BI	M_H_ECC<7..0>			DQ<19>	28	19
			7 165	CB<7>	DQ<18>	27	18
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			2 45	CB<2>	DQ<13>	132	13
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71<	56> IN	M_GH_RESET_LVC1V5_N	168	RESET_N	DQ<9>	13	9
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			237	SA<1>	DQ<5>	123	5
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199>	73<> 71<> BI	SMB_DDR_GH_LVC3_SDA	238	SDA	DQ<3>	10	3
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M_H_DQ<63..0> BI 60<>

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E55582-004

P3V3

3.3

R7K1 1/16W 1 2 A93548-023 1K 1% 0402LF

SPD ADDRESS = 0XA8

M_H_SA<2>

P1V5_DDR3_CPU1

R7G1 100 1% 1/16W 1 2 A93548-043 0402LF 1.5 0.75

P1V5_DDR3_CPU1_VREF_H_D OUT 72< 73>

R7F12 100 1% 1/16W 1 2 A93548-043 0402LF

C7F5 0.1UF 16V 10% 1 2 A36096-030 0402LF

P1V5_DDR3_CPU1

R7J2 100 1% 1/16W 1 2 A93548-043 0402LF 1.5 0.75

P1V5_DDR3_CPU1_VREF_H_A OUT 72<

R7J1 100 1% 1/16W 1 2 A93548-043 0402LF

C7J2 0.1UF 16V 10% 1 2 A36096-030 0402LF

J7F2

CONN240_E55582004

	2	VSS<58>	VDD<21>	51			
	5	VSS<57>	VDD<20>	54			
	8	VSS<56>	VDD<19>	57			
	11	VSS<55>	VDD<18>	60			
	14	VSS<54>	VDD<17>	62			
	17	VSS<53>	VDD<16>	65			
	20	VSS<52>	VDD<15>	66			
	23	VSS<51>	VDD<14>	69			
	26	VSS<50>	VDD<13>	72			
	29	VSS<49>	VDD<12>	75			
	32	VSS<48>	VDD<11>	78			
	35	VSS<47>	VDD<10>	170			
	38	VSS<46>	VDD<9>	173			
	41	VSS<45>	VDD<8>	176			
	44	VSS<44>	VDD<7>	179			
	47	VSS<43>	VDD<6>	182			
	80	VSS<42>	VDD<5>	183			
	83	VSS<41>	VDD<4>	186			
	86	VSS<40>	VDD<3>	189			
	89	VSS<39>	VDD<2>	191			
	92	VSS<38>	VDD<1>	194			
	95	VSS<37>	VDD<0>	197			
	98	VSS<36>					
	101	VSS<35>	VTT<3>	49			
	104	VSS<34>	VTT<2>	48			
	107	VSS<33>	VTT<1>	120			
	110	VSS<32>	VTT<0>	240			
	113	VSS<31>					
	116	VSS<30>					
	121	VSS<29>	NC_TEST	167	TP_H_D1_NC2		
	124	VSS<28>					
	127	VSS<27>					
	130	VSS<26>					
	133	VSS<25>					
	136	VSS<24>					
	139	VSS<23>					
	142	VSS<22>					
	145	VSS<21>					
	148	VSS<20>					
	151	VSS<19>					
	154	VSS<18>					
	157	VSS<17>					
	160	VSS<16>					
	163	VSS<15>					
	166	VSS<14>					
	199	VSS<13>					
	202	VSS<12>					
	205	VSS<11>					
	208	VSS<10>					
	211	VSS<9>					
	214	VSS<8>					
	217	VSS<7>					
	220	VSS<6>					
	223	VSS<5>					
	226	VSS<4>					
	229	VSS<3>					
	232	VSS<2>					
	235	VSS<1>					
	239	VSS<0>					

3/3

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P1V5_DDR3_CPU1

1.5

P0V75_VTT_DDR3_CPU1

0.75

P1V5_DDR3_CPU1

1.5

C7H12 10UF 6.3V 20% 602433-075 0603LF

C7H13 10UF 6.3V 20% 602433-075 0603LF

J7F2

CONN240_E55582004

DQS17P_DM8			161	17	M_H_DQS_DP<17..0>	BI	60<>
DQS17N_NC			162	17	M_H_DQS_DN<17..0>	BI	60<>
DQS16P_DM7			230	16			
DQS16N_NC			231	16			
DQS15P_DM6			221	15			
DQS15N_NC			222	15			
DQS14P_DM5			212	14			
DQS14N_NC			213	14			
DQS13P_DM4			203	13			
DQS13N_NC			204	13			
DQS12P_DM3			152	12			
DQS12N_NC			153	12			
DQS11P_DM2			143	11			
DQS11N_NC			144	11			
DQS10P_DM1			134	10			
DQS10N_NC			135	10			
DQS9P_DM0			125	9			
DQS9N_NC			126	9			
DQS8P			43	8			
DQS8N			42	8			
DQS7P			112	7			
DQS7N			111	7			
DQS6P			103	6			
DQS6N			102	6			
DQS5P			94	5			
DQS5N			93	5			
DQS4P			85	4			
DQS4N			84	4			
DQS3P			34	3			
DQS3N			33	3			
DQS2P			25	2			
DQS2N			24	2			
DQS1P			16	1			
DQS1N			15	1			
DQS0P			7	0			
DQS0N			6	0			

2/3

E55582-004

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DDR3 CPU1 CHANNEL H DIMM1

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 72 OF 303	

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ROOM = VREFDQ_CPU1

P3V3_AUX NEEDED FOR POT
IF DESIGN SUPPORT S3

P3V3 3.3

DECOUPLING CAP
CAD NOTE:
PLACE CLOSE TO CHIP

C9F6 0.1UF 0402LF 16V X7R 10% A36096-030 VREFDQ_CPU1

U9F5 VREFDQ_CPU1
ISL90727
VCC SCL SDA GND RW RH

R9F6 0 CHIP A93549-001 VREFDQ_CPU1 0402LF 5% 1/16W
R9F5 0 CHIP A93549-001 VREFDQ_CPU1 0402LF 5% 1/16W

70< 69< 199<> IN SMB_DDR_EF_LVC3_SCL
70<> 69<> 199> BI SMB_DDR_EF_LVC3_SDA
SMB_DDR_EF_DAC_LVC3_SCL
SMB_DDR_EF_DAC_LVC3_SDA

E47385-001
SMBUS ADDRESS=0X5C

CONNECTION TO THE P1V5_DDR3_CPU0
VOLTAGE RAIL SHOULD BE NEAR THE
P1V5_DDR3VR SENSE POINT

P1V5_DDR3_CPU1 1.5

P1V5_DDR3_CPU1_VREF_EF_RW 0.75

R9F9 12.1K 1% 1/16W CHIP 0402LF A93548-018 VREFDQ_CPU1

R9F7 12.1K 1% 1/16W 0402LF A93548-018 VREFDQ_CPU1

WRITE VREF FROM CPU TO THE DIMMS

56> IN P1V5_DDR3_EF_VREFDQTX

R1T8 A93549-001 0402LF 5% 1/16W VREFDQ_CPU1

P1V5_DDR3_CPU1_VREF_EF_OPFB

U9F4
INN INP VSN VSP OUT
LMV321

E21441-001 VREFDQ_CPU1

R9F4 2.20 CHIP A93549-051 VREFDQ_CPU1 0402LF 5% 1/16W
P1V5_DDR3_CPU1_VREF_EF_D 0.75

R9F3 100 1% 1/16W CHIP 0402LF A93548-043 VREFDQ_CPU1

C9F4 1.0UF 6.3V 10% EMPTY A36096-027 0402LF VREFDQ_CPU1

R1T7 0 CHIP A93549-001 VREFDQ_CPU1 0402LF 5% 1/16W
P1V5_DDR3_CPU1_VREF_E_D 0.75 OUT 69> 69<

R9F8 0 CHIP A93549-001 VREFDQ_CPU1 0402LF 5% 1/16W
P1V5_DDR3_CPU1_VREF_F_D 0.75 OUT 70< 70>

DDR3 PROCESSOR VREF GENERATION

P1V5_DDR3_CPU1

R9J1 100 1% 1/16W 1.5
A93548-043 0402LF 0.75
P1V5_DDR3_EF_VREFDQRX OUT 56<

R9J2 100 1% 1/16W
C9J1 0.1UF 16V 10%
A93548-043 0402LF
A36096-030 0402LF

CAD NOTE:
PLACE CIRCUIT AS CLOSE AS POSSBIBLE TO CPU
REFER TO RS-ROMLEY PDG FOR LATEST GUIDELINE
FROM ROMLEY PDG:
NOMIMAL TRACE WIDTH = 10 MILS
NOMIMAL TRACE SPACING = 20 MILS
CPU BREAKOUT REQ = 4-MIL WIDTH / 4-MIL SPACING
THE DECOUPLING CAP RECOMMENDED IS 0603 0.1UF

DECOUPLING CAP
CAD NOTE:
PLACE CLOSE TO CHIP

P5V
C1T11 1UF 16V 10% X5R 644066-061 0805LF VREFDQ_CPU1

P5V AUX NEEDED FOR OP AMP
IF DESIGN SUPPORT S3

REVIEW DATASHEET OF OPAMP FOR CORRECT DECOUPLING VALUES

P3V3_AUX NEEDED FOR POT
IF DESIGN SUPPORT S3

P3V3 3.3

DECOUPLING CAP
CAD NOTE:
PLACE CLOSE TO CHIP

C7F3 0.1UF 0402LF 16V X7R 10% A36096-030 VREFDQ_CPU1

U7F3 VREFDQ_CPU1
ISL90727
VCC SCL SDA GND RW RH

R7F9 0 CHIP A93549-001 VREFDQ_CPU1 0402LF 5% 1/16W
R7F8 0 CHIP A93549-001 VREFDQ_CPU1 0402LF 5% 1/16W

72< 71< 199<> IN SMB_DDR_GH_LVC3_SCL
72<> 71<> 199> BI SMB_DDR_GH_LVC3_SDA
SMB_DDR_GH_DAC_LVC3_SCL
SMB_DDR_GH_DAC_LVC3_SDA

E47385-001
SMBUS ADDRESS=0X5C

CONNECTION TO THE P1V5_DDR3_CPU0
VOLTAGE RAIL SHOULD BE NEAR THE
P1V5_DDR3VR SENSE POINT

P1V5_DDR3_CPU1 1.5

P1V5_DDR3_CPU1_VREF_GH_RW 0.75

R7F11 12.1K 1% 1/16W CHIP 0402LF A93548-018 VREFDQ_CPU1

R7F10 12.1K 1% 1/16W 0402LF A93548-018 VREFDQ_CPU1

WRITE VREF FROM CPU TO THE DIMMS

56> IN P1V5_DDR3_GH_VREFDQTX

R3T2 A93549-001 0402LF 5% 1/16W VREFDQ_CPU1

P1V5_DDR3_CPU1_VREF_GH_OPFB

U7F1
INN INP VSN VSP OUT
LMV321

E21441-001 VREFDQ_CPU1

R7F1 2.20 CHIP A93549-051 VREFDQ_CPU1 0402LF 5% 1/16W
P1V5_DDR3_CPU1_VREF_GH_D 0.75

R7F2 100 1% 1/16W CHIP 0402LF A93548-043 VREFDQ_CPU1

C7F1 1.0UF 6.3V 10% EMPTY A36096-027 0402LF VREFDQ_CPU1

R3T1 0 CHIP A93549-001 VREFDQ_CPU1 0402LF 5% 1/16W
P1V5_DDR3_CPU1_VREF_H_D 0.75 OUT 72> 72<

R7F6 0 CHIP A93549-001 VREFDQ_CPU1 0402LF 5% 1/16W
P1V5_DDR3_CPU1_VREF_G_D 0.75 OUT 71< 71>

DDR3 PROCESSOR VREF GENERATION

P1V5_DDR3_CPU1

R7J3 100 1% 1/16W 1.5
A93548-043 0402LF 0.75
P1V5_DDR3_GH_VREFDQRX OUT 56<

R7J6 100 1% 1/16W
C7J3 0.1UF 16V 10%
A93548-043 0402LF
A36096-030 0402LF

CAD NOTE:
PLACE CIRCUIT AS CLOSE AS POSSBIBLE TO CPU
REFER TO RS-ROMLEY PDG FOR LATEST GUIDELINE
FROM ROMLEY PDG:
NOMIMAL TRACE WIDTH = 10 MILS
NOMIMAL TRACE SPACING = 20 MILS
CPU BREAKOUT REQ = 4-MIL WIDTH / 4-MIL SPACING
THE DECOUPLING CAP RECOMMENDED IS 0603 0.1UF

DECOUPLING CAP
CAD NOTE:
PLACE CLOSE TO CHIP

P5V
C3T1 1UF 16V 10% X5R 644066-061 0805LF VREFDQ_CPU1

P5V AUX NEEDED FOR OP AMP
IF DESIGN SUPPORT S3

REVIEW DATASHEET OF OPAMP FOR CORRECT DECOUPLING VALUES

CPU1 DDR3 DQ REFERENCE

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DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 73 OF 303	

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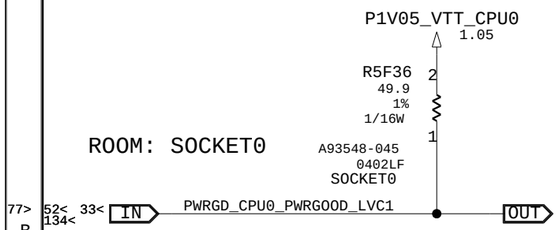
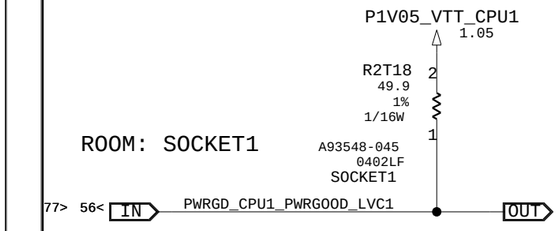
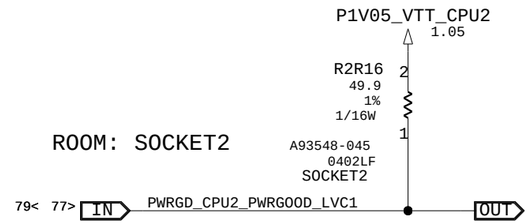
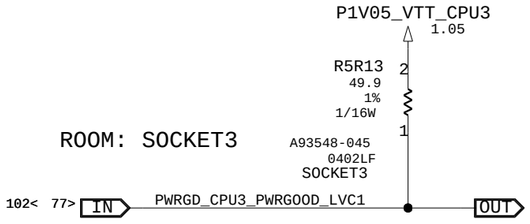
POWER GOOD CIRCUITRY

CAD NOTE: GTL2005 TO PULLUP RES = 3" TO 23"
CAD NOTE: PULLUP RES TO CPU = LESS THAN 2.5"





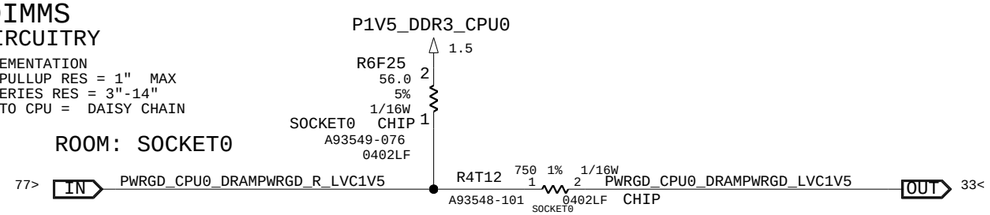


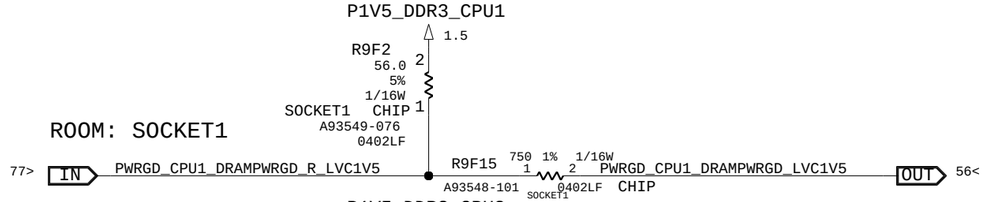


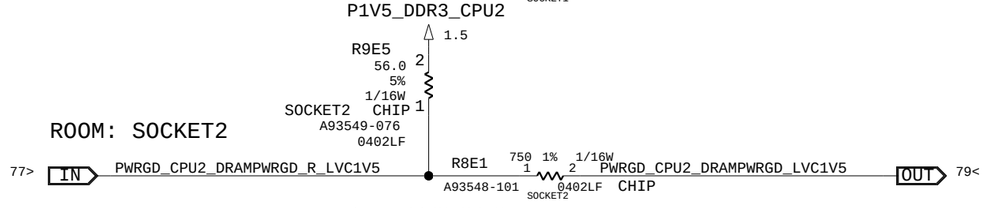
POWERGOOD DIMMS

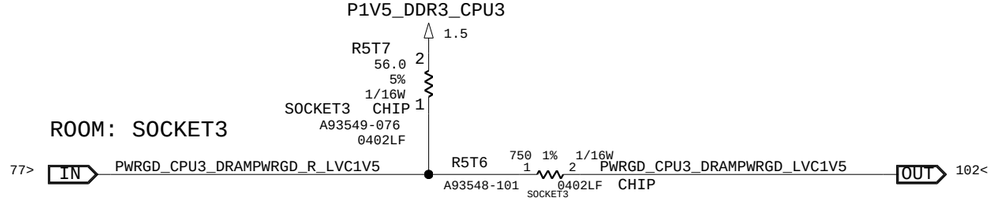
DRAM_PWR_OK CIRCUITRY

REFER TO PDG FOR IMPLEMENTATION
CAD NOTE: GTL2005 TO PULLUP RES = 1" MAX
CAD NOTE: PULLUP TO SERIES RES = 3"-14"
CAD NOTE: SERIES RES TO CPU = DAISY CHAIN



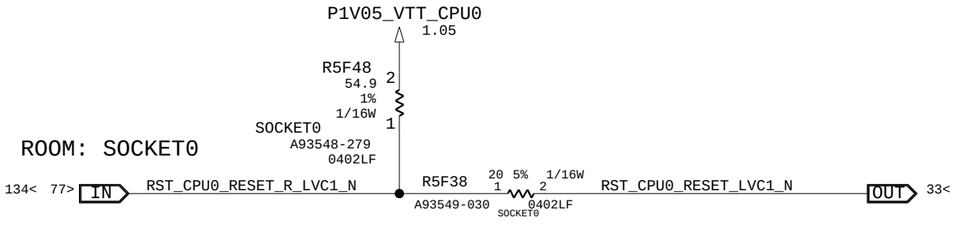


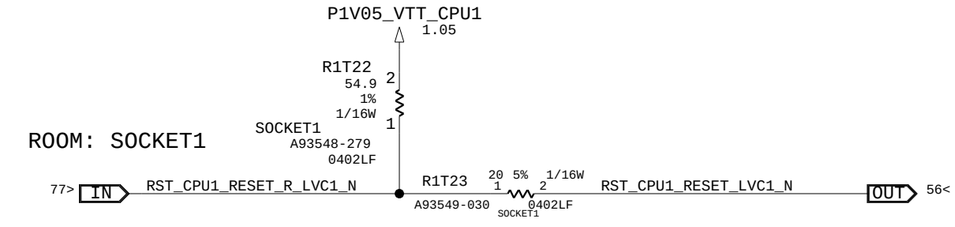


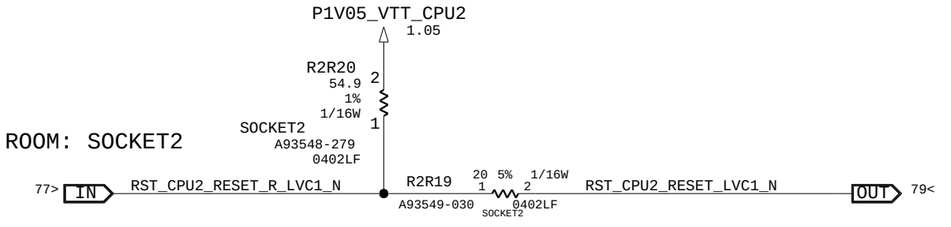


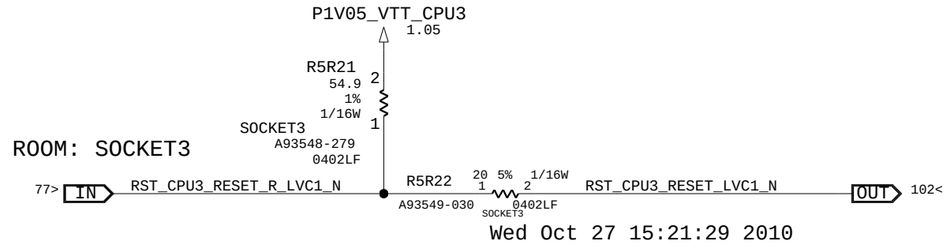
RESET CIRCUITRY

CAD NOTE: GTL2005 TO PULLUP RES = 3" TO 23"
CAD NOTE: PLACE TOGETHER PULLUP RES AND SERIES RES
CAD NOTE: SERIES RES TO CPU = LESS THAN 1.5"









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CPUS POWERGOOD, RESET, DRAMPWRGD CIRCUITRY

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 76 OF 303	

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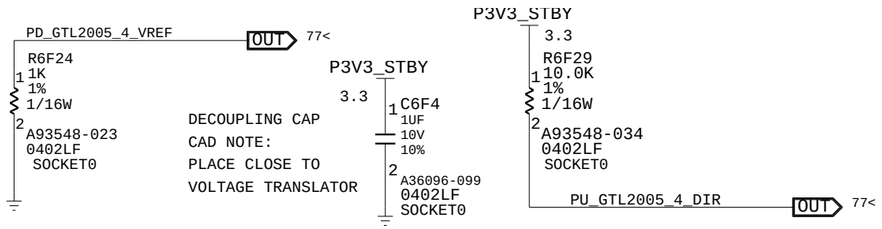
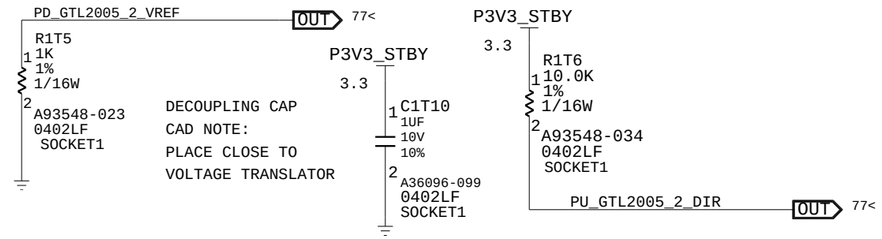
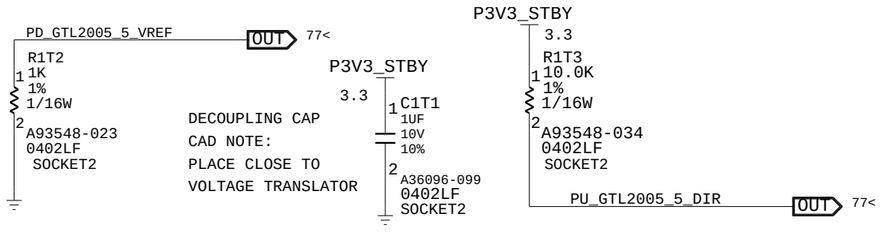
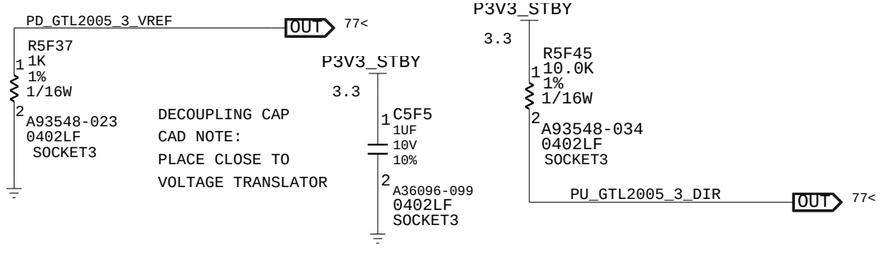


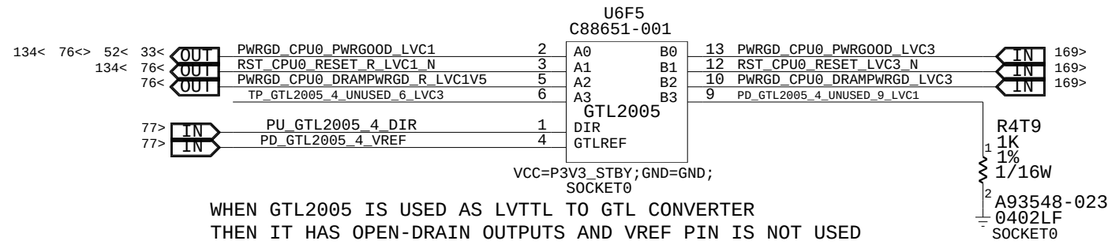






SIGNALS TO CPU0 DRIVEN BY SOUTH CPLD

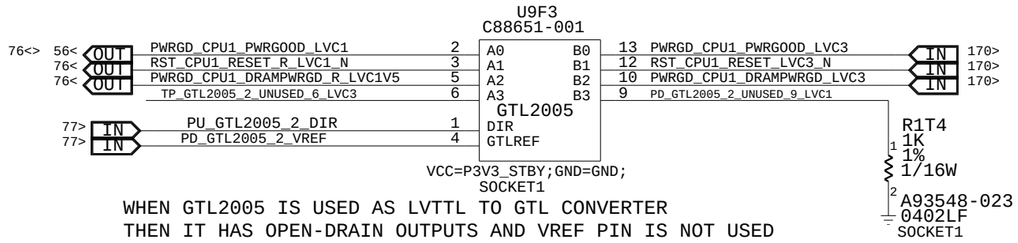
LVTTL TO GTL/GTL+ CONVERTER



WHEN GTL2005 IS USED AS LVTTL TO GTL CONVERTER
THEN IT HAS OPEN-DRAIN OUTPUTS AND VREF PIN IS NOT USED

SIGNALS TO CPU1 DRIVEN BY NORTH CPLD

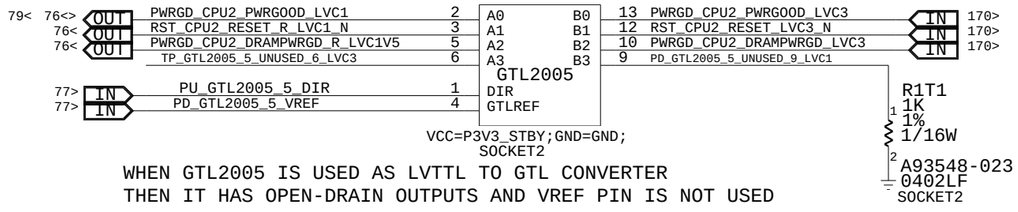
LVTTL TO GTL/GTL+ CONVERTER



WHEN GTL2005 IS USED AS LVTTL TO GTL CONVERTER
THEN IT HAS OPEN-DRAIN OUTPUTS AND VREF PIN IS NOT USED

SIGNALS TO CPU2 DRIVEN BY NORTH CPLD

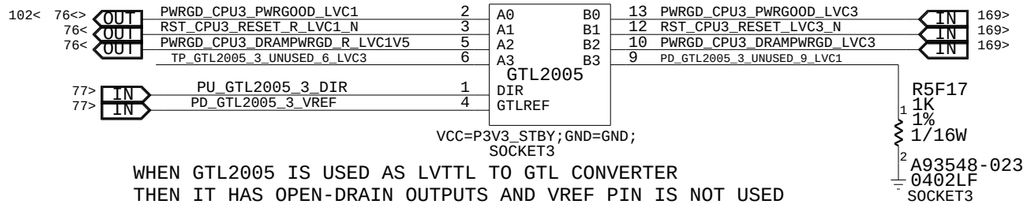
LVTTL TO GTL/GTL+ CONVERTER



WHEN GTL2005 IS USED AS LVTTL TO GTL CONVERTER
THEN IT HAS OPEN-DRAIN OUTPUTS AND VREF PIN IS NOT USED

SIGNALS TO CPU3 DRIVEN BY SOUTH CPLD

LVTTL TO GTL/GTL+ CONVERTER



WHEN GTL2005 IS USED AS LVTTL TO GTL CONVERTER
THEN IT HAS OPEN-DRAIN OUTPUTS AND VREF PIN IS NOT USED

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CPUS POWERGOOD, RESET, DRAMPWRGD CIRCUITRY

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 77 OF 303	

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ERROR SIGNALS

VTT_CPU0 USED SINCE IT IS ALWAYS PRESENT, AVOIDING FALSE SIGNAL ASSERTION
CAD NOTE: FOLLOW A STAR TOPOLOGY
CAD NOTE: EACH CPU TO PULLUP AT COMMON NODE: 5"-15"
CAD NOTE: NO TRACE LENGTH MATCHING REQUIRED
CAD NOTE: PLACE SERIES RESISTOR RIGHT WHERE THE STUB SPRINGS

CAD NOTE:
REFER TO ROMLEY PDG
FOR LAYOUT CONSTRAINTS

ROOM: ERROR0

P1V05_VTT_CPU0
1.05
R4T1
51.10 1%
1/16W
A93548-072
0402LF
ERROR0

109> 63> 40> 86> IN FM_CPU_ERR_N<0> R5F44 1K 1% 1/16W FM_CPU_ERR_R_N<0> OUT 78<
A93548-023 0402LF ERROR0

ROOM: ERROR1

P1V05_VTT_CPU0
1.05
R4T3
51.10 1%
1/16W
A93548-072
0402LF
ERROR1

86> 63> 40> 109> IN FM_CPU_ERR_N<1> R5F42 1K 1% 1/16W FM_CPU_ERR_R_N<1> OUT 78<
A93548-023 0402LF ERROR1

ROOM: ERROR2

P1V05_VTT_CPU0
1.05
R4T5
51.10 1%
1/16W
A93548-072
0402LF
ERROR2

86> 63> 40> 109> IN FM_CPU_ERR_N<2> R5F41 1K 1% 1/16W FM_CPU_ERR_R_N<2> OUT 78<
A93548-023 0402LF ERROR2

ROOM: ERRORS

GTL TO LVTTL CONVERTER
WHEN GTL2005 IS USED AS GTL TO LVTTL CONVERTER
THEN IT HAS PUSHPULL OUTPUTS

U5F3
C88651-001
GTL2005

78> IN FM_CPU_ERR_R_N<2> 2 A0 B0 13 FM_ERR2_LVC3_N OUT 129< 176<
78> IN FM_CPU_ERR_R_N<1> 3 A1 B1 12 FM_ERR1_LVC3_N OUT 129< 169<
78> IN FM_CPU_ERR_R_N<0> 5 A2 B2 10 FM_ERR0_LVC3_N OUT 129< 138<
PD_GTL2005_1_UNUSED_6_LVC1 6 A3 B3 9 TP_GTL2005_1_UNUSED_9_LVC3
78> IN PD_GTL2005_1_DIR 1 DIR
78> IN P0V7_GTL2005_1_VREF 4 GTLREF

R5F33 1K 1% 1/16W
A93548-023 0402LF ERRORS

VCC=P3V3;GND=GND;
ERRORS

P1V05_VTT_CPU0
1.05
R5F43 49.9 1% 1/16W
A93548-045 0402LF ERRORS

0.7 P0V7_GTL2005_1_VREF OUT 78<
R5F35 100 1% 1/16W
A93548-043 0402LF ERRORS
C5F6 0.1UF 16V 10%
A36096-030 0402LF ERRORS

PD_GTL2005_1_DIR OUT 78<
R5F34 1K 1% 1/16W
A93548-023 0402LF ERRORS

DECOUPLING CAP
CAD NOTE:
PLACE CLOSE TO
VOLTAGE TRANSLATOR

P3V3
3.3
C5F4 1UF 10V 10%
A36096-099 0402LF ERRORS

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CPU SIDEBAND: ERRORS CIRCUITRY

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 78 OF 303	

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CAD NOTE FROM ROMLEY PDG NOTE FOR PE_RBIAS:
THE ROUTING DISTANCE TO THE RESISTOR
SHOULD BE AS CLOSE AS POSSIBLE
(NO LONGER THAN 1.0" AND AT LEAST 15 MILS WIDE)
KEEP THE TRACES SEPARETED 30 MILS FROM ALL OTHERS.

C2R2 0.01UF 25V 10% — A36096-045 0402LF SOCKET2

R2R8 49.9 1% 1/16W — A93548-045 0402LF SOCKET2

DE NOTE: PE_RBIAS_SENSE NET MUST BE SHORTED
AT THE TOP OF PE_RBIAS 50OHM RESISTOR.
CONNECT SENSE AS CLOSE AS POSIBLE TO OTHER END OF RES

NET NAMES REFLECT ON-DIE TERMINATION AT CPU

U8C1
IC

SANDYBRIDGE_EP_EXT_D

		A_CPU2_PE_VREF_CAP	AJ43	PE_VREF_CAP			
			AF52	PE_RBIAS_SENSE			
		A_CPU2_PE_RBIAS	AH52	PE_RBIAS			
31>	IN	CLK_100M_CPU2_PCIE_DP	AW45	BCLK1_DP			
31>	IN	CLK_100M_CPU2_PCIE_DN	BA45	BCLK1_DN			
		TP_SMB_CPU2_PE_HP_1V05_SCL	BH48	PEHPSCL			
		TP_SMB_CPU2_PE_HP_1V05_SDA	BF48	PEHPSDA			
		NC_CPU2_RSVD<12>	D56	RSVD<12>			
		NC_CPU2_RSVD<8>	F56	RSVD<8>			
		NC_CPU2_RSVD<10>	E57	RSVD<10>			
		NC_CPU2_RSVD<7>	F58	RSVD<7>			
		NC_CPU2_RSVD<5>	H58	RSVD<5>			
		NC_CPU2_RSVD<63>	AR55	RSVD<63>			
		NC_CPU2_RSVD<62>	AU55	RSVD<62>			
54>	IN	PU_CPU2_DMIGEN2EN	V52	TXT_PLTEN			
54>	IN	PD_CPU2_FRMAGENT	AT50	FRMAGENT			
54>	IN	PD_CPU2_BMCINIT	AL47	BMCINIT			
54>	IN	PD_CPU2_LTEN	AK52	TXT_AGENT			
54>	IN	PU_CPU2_BIST_EN	AT48	BIST_ENABLE			
125< 54>	OUT	FM_CPU2_IVT_ID_LVC1_N	AH42	IVT_ID_N			
123<>	BI	FM_CPU2_MEMLM_MEMHOT_LVC1_N	E13	MEM_HOT_C23_N			
123<>	BI	FM_CPU2_MEMJK_MEMHOT_LVC1_N	CB22	MEM_HOT_C01_N			
76>	IN	PWRGD_CPU2_DRAMPWRGD_LVC1V5	L15	DRAM_PWR_OK_C23			
			CW17	DRAM_PWR_OK_C01			
96<	OUT	P1V5_DDR3_LM_VREFDQTX	P42	DDR_VREFDQTX_C23			
96<	OUT	P1V5_DDR3_JK_VREFDQTX	CN41	DDR_VREFDQTX_C01			
96>	IN	P1V5_DDR3_LM_VREFDQRX	J1	DDR_VREFDQRX_C23			
96>	IN	P1V5_DDR3_JK_VREFDQRX	BY16	DDR_VREFDQRX_C01			
200<	BI	SMB_DDR_LM_LVC1_SDA	R43	DDR_SDA_C23			
200<	BI	SMB_DDR_JK_LVC1_SDA	CW41	DDR_SDA_C01			
200<>	OUT	SMB_DDR_LM_LVC1_SCL	U43	DDR_SCL_C23			
200<>	OUT	SMB_DDR_JK_LVC1_SCL	CY42	DDR_SCL_C01			
95< 94<	OUT	M_LM_RESET_LVC1V5_N	AE27	DDR_RESET_C23_N			
93< 92<	OUT	M_JK_RESET_LVC1V5_N	CB18	DDR_RESET_C01_N			
206< 170< 169< 129< 54>	OUT	FM_CPU2_SKTOCC_CO_N	BU49	SKTOCC_N			
		NC_CPU2_RSVD<23>	CY56	RSVD<23>			
99<	BI	IRQ_CPU2_CATERR_LVC1_N	CC51	CAT_ERR_N			
54>	IN	PD_CPU2_SAFE_MODE	DA55	SAFE_MODE_BOOT			
134> 133< 33<	IN	JTAG_CPU_G_TDI	BW43	TDI			
134> 133> 102<	IN	JTAG_CPU_LVC1_TCK1	BY44	TCK			
134> 133> 102< 56< 33<	IN	JTAG_CPU_G_TMS	BV44	TMS			
134> 133> 102< 56< 33<	IN	JTAG_CPU_LVC1_TRST_N	CT54	TRST_N			
				QPI_VREF_CAP	CU51	A_CPU2_QPI_VREF_CAP	
				QPI_RBIAS_SENSE	CC53		
				QPI_RBIAS	CE53	A_CPU2_QPI_RBIAS	
				BCLK0_DP	CN43	CLK_100M_CPU2_QPI_DP	IN 31>
				BCLK0_DN	CM44	CLK_100M_CPU2_QPI_DN	IN 31>
				RSVD<31>	CA45	NC_CPU2_RSVD<31>	
				RSVD<32>	BY46	NC_CPU2_RSVD<32>	
				RSVD<18>	DD54	NC_CPU2_RSVD<18>	
				RSVD<19>	DC55	NC_CPU2_RSVD<19>	
				RSVD<17>	DE55	NC_CPU2_RSVD<17>	
				RSVD<21>	DA57	NC_CPU2_RSVD<21>	
				RSVD<22>	CY58	NC_CPU2_RSVD<22>	
				RSVD<40>	BM46	NC_CPU2_RSVD<40>	
				RSVD<37>	BP46	NC_CPU2_RSVD<37>	
				RSVD<24>	CY48	NC_CPU2_RSVD<24>	
				RSVD<25>	CY46	NC_CPU2_RSVD<25>	
				THERMTRIP_N	BL47	FM_CPU2_THERMTRIP_LVC1_N	OUT 100<
				PROCHOT_N	BD52	FM_CPU2_PROCHOT_LVC1_N	BI 122<>
				TEST4	BA55	PD_CPU2_TEST<4>	
				PRDY_N	R53	XDP_CPU2_PRDY_N	OUT 134<>
				PREQ_N	U53	XDP_CPU2_PREQ_N	IN 134<>
				SOCKET_ID<1>	BC49	FM_CPU2_SOCKET_ID1_LVC1	
				SOCKET_ID<0>	CY52	FM_CPU2_SOCKET_ID0_LVC1	
				PECI	BJ47	PECI_CPU_LVC1	BI 33<> 56<> 102<> 196<>
				SVIDCLK	CB44	SVID_CPU2_CLK_LVC1	OUT 55<
				SVIDDATA	BR45	SVID_CPU2_DAT_LVC1	BI 55<>
				SVIDALERT_N	CR43	SVID_CPU2_ALERT_LVC1_N	IN 55>
				PMSYNC	K52	IRQ_PM_SYNC2_LVC1	IN 102< 135>
				PWRGOOD	BJ53	PWRGD_CPU2_PWRGOOD_LVC1	IN 76<> 77>
				EAR_N	CH56	RST_CPU_EAR_LVC1_N	BI 108<>
				RESET_N	CK44	RST_CPU2_RESET_LVC1_N	IN 76>
				TDO	CA43	JTAG_CPU2_G_TDO	OUT 102< 133>

1/17

E64556-001

CAD NOTE FROM ROMLEY PDG NOTE FOR QPI_RBIAS:
THE ROUTING DISTANCE TO THE RESISTOR
SHOULD BE AS CLOSE AS POSSIBLE
(POSSIBLY NO LONGER THAN 1.0" AND AT LEAST 10 MILS WIDE)

R2R13 49.9 1% 1/16W — A93548-045 0402LF SOCKET2

C3R1 0.01UF 25V 10% — A36096-045 0402LF SOCKET2

DE NOTE: QPI_RBIAS_SENSE NET MUST BE SHORTED
AT THE TOP OF QPI_RBIAS 50OHM RESISTOR.
CONNECT SENSE AS CLOSE AS POSIBLE TO OTHER END OF RES

NOTE: CONNECT TEST4 TO VSS PER PDG

P1V05_VTT_CPU2
1.05

*DE NOTE: RESISTOR VALUES COULD BE 240 OHM 5% CURRENT ONES 1% USED TO REDUCE BOM.

R2R15 240 1% 1/16W — A93548-504 0402 SOCKET2

R3R1 240 1% 1/16W — A93548-504 0402 SOCKET2

DE NOTE: SOCKET_ID[1:0] NETS HAVE PD ON DIE

CPU	SOCKET_ID[2:0]	PECI ADDRESS
CPU2	010B	0X32

EAR_N SIGNAL HAS A 6K OHM PU ON CPU DIE

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CPU SOCKET 2 (1 OF 13)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 79 OF 303	

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SANDYBRIDGE_EP_EXT_D

63	M_J_DQ<63>	CL41	DDR0_DQ<63>	DDR0_DQS_DP<17>	CD16	M_J_DQS_DP<17>	17
62	M_J_DQ<62>	CJ41	DDR0_DQ<62>	DDR0_DQS_DP<16>	CJ39	M_J_DQS_DP<16>	16
61	M_J_DQ<61>	CL37	DDR0_DQ<61>	DDR0_DQS_DP<15>	CC39	M_J_DQS_DP<15>	15
60	M_J_DQ<60>	CJ37	DDR0_DQ<60>	DDR0_DQS_DP<14>	CK32	M_J_DQS_DP<14>	14
59	M_J_DQ<59>	CK42	DDR0_DQ<59>	DDR0_DQS_DP<13>	CD32	M_J_DQS_DP<13>	13
58	M_J_DQ<58>	CH42	DDR0_DQ<58>	DDR0_DQS_DP<12>	CB10	M_J_DQS_DP<12>	12
57	M_J_DQ<57>	CK38	DDR0_DQ<57>	DDR0_DQS_DP<11>	CJ13	M_J_DQS_DP<11>	11
56	M_J_DQ<56>	CH38	DDR0_DQ<56>	DDR0_DQS_DP<10>	CC5	M_J_DQS_DP<10>	10
55	M_J_DQ<55>	CB42	DDR0_DQ<55>	DDR0_DQS_DP<9>	CE7	M_J_DQS_DP<9>	9
54	M_J_DQ<54>	CC41	DDR0_DQ<54>	DDR0_DQS_DP<8>	CC17	M_J_DQS_DP<8>	8
53	M_J_DQ<53>	CE37	DDR0_DQ<53>	DDR0_DQS_DP<7>	CK40	M_J_DQS_DP<7>	7
52	M_J_DQ<52>	CC37	DDR0_DQ<52>	DDR0_DQS_DP<6>	CD40	M_J_DQS_DP<6>	6
51	M_J_DQ<51>	CD42	DDR0_DQ<51>	DDR0_DQS_DP<5>	CJ33	M_J_DQS_DP<5>	5
50	M_J_DQ<50>	CE41	DDR0_DQ<50>	DDR0_DQS_DP<4>	CC33	M_J_DQS_DP<4>	4
49	M_J_DQ<49>	CD38	DDR0_DQ<49>	DDR0_DQS_DP<3>	CE11	M_J_DQS_DP<3>	3
48	M_J_DQ<48>	CB38	DDR0_DQ<48>	DDR0_DQS_DP<2>	CK14	M_J_DQS_DP<2>	2
47	M_J_DQ<47>	CH34	DDR0_DQ<47>	DDR0_DQS_DP<1>	CF4	M_J_DQS_DP<1>	1
46	M_J_DQ<46>	CK34	DDR0_DQ<46>	DDR0_DQS_DP<0>	CH8	M_J_DQS_DP<0>	0
45	M_J_DQ<45>	CH30	DDR0_DQ<45>				
44	M_J_DQ<44>	CK30	DDR0_DQ<44>	DDR0_DQS_DN<17>	CF16	M_J_DQS_DN<17>	17
43	M_J_DQ<43>	CJ35	DDR0_DQ<43>	DDR0_DQS_DN<16>	CL39	M_J_DQS_DN<16>	16
42	M_J_DQ<42>	CL35	DDR0_DQ<42>	DDR0_DQS_DN<15>	CE39	M_J_DQS_DN<15>	15
41	M_J_DQ<41>	CJ31	DDR0_DQ<41>	DDR0_DQS_DN<14>	CH32	M_J_DQS_DN<14>	14
40	M_J_DQ<40>	CL31	DDR0_DQ<40>	DDR0_DQS_DN<13>	CB32	M_J_DQS_DN<13>	13
39	M_J_DQ<39>	CB34	DDR0_DQ<39>	DDR0_DQS_DN<12>	CC11	M_J_DQS_DN<12>	12
38	M_J_DQ<38>	CD34	DDR0_DQ<38>	DDR0_DQS_DN<11>	CL13	M_J_DQS_DN<11>	11
37	M_J_DQ<37>	CB30	DDR0_DQ<37>	DDR0_DQS_DN<10>	CD4	M_J_DQS_DN<10>	10
36	M_J_DQ<36>	CD30	DDR0_DQ<36>	DDR0_DQS_DN<9>	CF8	M_J_DQS_DN<9>	9
35	M_J_DQ<35>	CC35	DDR0_DQ<35>	DDR0_DQS_DN<8>	CE17	M_J_DQS_DN<8>	8
34	M_J_DQ<34>	CE35	DDR0_DQ<34>	DDR0_DQS_DN<7>	CH40	M_J_DQS_DN<7>	7
33	M_J_DQ<33>	CC31	DDR0_DQ<33>	DDR0_DQS_DN<6>	CB40	M_J_DQS_DN<6>	6
32	M_J_DQ<32>	CE31	DDR0_DQ<32>	DDR0_DQS_DN<5>	CL33	M_J_DQS_DN<5>	5
31	M_J_DQ<31>	CF10	DDR0_DQ<31>	DDR0_DQS_DN<4>	CE33	M_J_DQS_DN<4>	4
30	M_J_DQ<30>	CH10	DDR0_DQ<30>	DDR0_DQS_DN<3>	CD10	M_J_DQS_DN<3>	3
29	M_J_DQ<29>	CA9	DDR0_DQ<29>	DDR0_DQS_DN<2>	CH14	M_J_DQS_DN<2>	2
28	M_J_DQ<28>	BW9	DDR0_DQ<28>	DDR0_DQS_DN<1>	CE3	M_J_DQS_DN<1>	1
27	M_J_DQ<27>	CD12	DDR0_DQ<27>	DDR0_DQS_DN<0>	CG7	M_J_DQS_DN<0>	0
26	M_J_DQ<26>	CB12	DDR0_DQ<26>				
25	M_J_DQ<25>	BY12	DDR0_DQ<25>	DDR0_MA<15>	CN19	M_J_MA<15>	15
24	M_J_DQ<24>	BY10	DDR0_DQ<24>	DDR0_MA<14>	CG19	M_J_MA<14>	14
23	M_J_DQ<23>	CL15	DDR0_DQ<23>	DDR0_MA<13>	CG29	M_J_MA<13>	13
22	M_J_DQ<22>	CJ15	DDR0_DQ<22>	DDR0_MA<12>	CK20	M_J_MA<12>	12
21	M_J_DQ<21>	CL11	DDR0_DQ<21>	DDR0_MA<11>	CL21	M_J_MA<11>	11
20	M_J_DQ<20>	CG13	DDR0_DQ<20>	DDR0_MA<10>	CK26	M_J_MA<10>	10
19	M_J_DQ<19>	CM16	DDR0_DQ<19>	DDR0_MA<9>	CN21	M_J_MA<9>	9
18	M_J_DQ<18>	CK16	DDR0_DQ<18>	DDR0_MA<8>	CK22	M_J_MA<8>	8
17	M_J_DQ<17>	CM12	DDR0_DQ<17>	DDR0_MA<7>	CM22	M_J_MA<7>	7
16	M_J_DQ<16>	CK12	DDR0_DQ<16>	DDR0_MA<6>	CN23	M_J_MA<6>	6
15	M_J_DQ<15>	CG5	DDR0_DQ<15>	DDR0_MA<5>	CL23	M_J_MA<5>	5
14	M_J_DQ<14>	CG3	DDR0_DQ<14>	DDR0_MA<4>	CM24	M_J_MA<4>	4
13	M_J_DQ<13>	CA3	DDR0_DQ<13>	DDR0_MA<3>	CK24	M_J_MA<3>	3
12	M_J_DQ<12>	CA1	DDR0_DQ<12>	DDR0_MA<2>	CG25	M_J_MA<2>	2
11	M_J_DQ<11>	CJ5	DDR0_DQ<11>	DDR0_MA<1>	CR25	M_J_MA<1>	1
10	M_J_DQ<10>	CH4	DDR0_DQ<10>	DDR0_MA<0>	CL25	M_J_MA<0>	0
9	M_J_DQ<9>	CB4	DDR0_DQ<9>				
8	M_J_DQ<8>	CB2	DDR0_DQ<8>	DDR0_ECC<7>	CK18	M_J_ECC<7>	7
7	M_J_DQ<7>	CL7	DDR0_DQ<7>	DDR0_ECC<6>	CG17	M_J_ECC<6>	6
6	M_J_DQ<6>	CJ7	DDR0_DQ<6>	DDR0_ECC<5>	CD14	M_J_ECC<5>	5
5	M_J_DQ<5>	CA7	DDR0_DQ<5>	DDR0_ECC<4>	CB14	M_J_ECC<4>	4
4	M_J_DQ<4>	BY6	DDR0_DQ<4>	DDR0_ECC<3>	CF18	M_J_ECC<3>	3
3	M_J_DQ<3>	CL9	DDR0_DQ<3>	DDR0_ECC<2>	CH18	M_J_ECC<2>	2
2	M_J_DQ<2>	CK8	DDR0_DQ<2>	DDR0_ECC<1>	CC15	M_J_ECC<1>	1
1	M_J_DQ<1>	CD8	DDR0_DQ<1>	DDR0_ECC<0>	CE15	M_J_ECC<0>	0
0	M_J_DQ<0>	CC7	DDR0_DQ<0>				
	NC_M_J_CS_N<9>	CK28	DDR0_CS_N<9>	DDR0_CKE<5>	CE19	NC_M_J_CKE<5>	
	NC_M_J_CS_N<8>	CL27	DDR0_CS_N<8>	DDR0_CKE<4>	CF20	NC_M_J_CKE<4>	
	NC_M_J_CS_N<7>	CC25	DDR0_CS_N<7>	DDR0_CKE<3>	CP18	NC_M_J_CKE<3>	
	NC_M_J_CS_N<6>	CB26	DDR0_CS_N<6>	DDR0_CKE<2>	CH20	NC_M_J_CKE<2>	
	NC_M_J_CS_N<5>	CF26	DDR0_CS_N<5>	DDR0_CKE<1>	CM18	M_J_CKE<1>	1
	NC_M_J_CS_N<4>	CG27	DDR0_CS_N<4>	DDR0_CKE<0>	CL19	M_J_CKE<0>	0
3	M_J_CS_N<3>	CB28	DDR0_CS_N<3>	DDR0_BA<2>	CM20	M_J_BA<2>	2
2	M_J_CS_N<2>	CC23	DDR0_CS_N<2>	DDR0_BA<1>	CN27	M_J_BA<1>	1
1	M_J_CS_N<1>	CH26	DDR0_CS_N<1>	DDR0_BA<0>	CM28	M_J_BA<0>	0
0	M_J_CS_N<0>	CN25	DDR0_CS_N<0>				
	NC_M_J_CK_DP<3>	CH22	DDR0_CLK_DP<3>	DDR0_ODT<5>	CC27	NC_M_J_ODT<5>	
	M_J_CK_DP<2>	CG21	DDR0_CLK_DP<2>	DDR0_ODT<4>	CB24	NC_M_J_ODT<4>	
	NC_M_J_CK_DP<1>	CG23	DDR0_CLK_DP<1>	DDR0_ODT<3>	CF28	NC_M_J_ODT<3>	
	M_J_CK_DP<0>	CH24	DDR0_CLK_DP<0>	DDR0_ODT<2>	CH28	NC_M_J_ODT<2>	
	NC_M_J_CK_DN<3>	CF22	DDR0_CLK_DN<3>	DDR0_ODT<1>	CE27	M_J_ODT<1>	1
	M_J_CK_DN<2>	CE21	DDR0_CLK_DN<2>	DDR0_ODT<0>	CE25	M_J_ODT<0>	0
	NC_M_J_CK_DN<1>	CE23	DDR0_CLK_DN<1>				
	M_J_CK_DN<0>	CF24	DDR0_CLK_DN<0>	DDR0_WE_N	CN29	M_J_WE_N	
				DDR0_RAS_N	CE29	M_J_RAS_N	
				DDR0_PAR_ERR_N	CC21	M_J_PAR_ERR_N<0>	
				DDR0_CAS_N	CL29	M_J_CAS_N	
				DDR0_MA_PAR	CM26	M_J_MA_PAR	

92<> BI M_J_DQ<63..0>

M_J_DQS_DP<17..0> BI 92<>

M_J_DQS_DN<17..0> BI 92<>

M_J_MA<15..0> OUT 92<

M_J_ECC<7..0> BI 92<>

92< OUT M_J_CS_N<3..0>

M_J_CKE<1..0> OUT 92<

M_J_BA<2..0> OUT 92<

M_J_ODT<1..0> OUT 92<

92< OUT M_J_CK_DP<2>

92< OUT M_J_CK_DP<0>

92< OUT M_J_CK_DN<2>

92< OUT M_J_CK_DN<0>

M_J_PAR_ERR_N<0> IN 92<

M_J_CAS_N OUT 92<

M_J_MA_PAR OUT 92<

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CPU SOCKET 2 (2 OF 13)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 80 OF 303	

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U8C1 IC

SANDYBRIDGE_EP_EXT_D

93<> BI M_K_DQ<63..0>

63	M_K_DQ<63>	DF40	DDR1_DQ<63>	
62	M_K_DQ<62>	DA39	DDR1_DQ<62>	
61	M_K_DQ<61>	DC37	DDR1_DQ<61>	
60	M_K_DQ<60>	DA37	DDR1_DQ<60>	
59	M_K_DQ<59>	DB40	DDR1_DQ<59>	
58	M_K_DQ<58>	DD40	DDR1_DQ<58>	
57	M_K_DQ<57>	DF38	DDR1_DQ<57>	
56	M_K_DQ<56>	DE37	DDR1_DQ<56>	
55	M_K_DQ<55>	CV40	DDR1_DQ<55>	
54	M_K_DQ<54>	CT40	DDR1_DQ<54>	
53	M_K_DQ<53>	CV36	DDR1_DQ<53>	
52	M_K_DQ<52>	CT36	DDR1_DQ<52>	
51	M_K_DQ<51>	CU41	DDR1_DQ<51>	
50	M_K_DQ<50>	CR41	DDR1_DQ<50>	
49	M_K_DQ<49>	CU37	DDR1_DQ<49>	
48	M_K_DQ<48>	CR37	DDR1_DQ<48>	
47	M_K_DQ<47>	DE35	DDR1_DQ<47>	
46	M_K_DQ<46>	DF34	DDR1_DQ<46>	
45	M_K_DQ<45>	CY32	DDR1_DQ<45>	
44	M_K_DQ<44>	DA31	DDR1_DQ<44>	
43	M_K_DQ<43>	DA35	DDR1_DQ<43>	
42	M_K_DQ<42>	DC35	DDR1_DQ<42>	
41	M_K_DQ<41>	DD32	DDR1_DQ<41>	
40	M_K_DQ<40>	DA33	DDR1_DQ<40>	
39	M_K_DQ<39>	CR33	DDR1_DQ<39>	
38	M_K_DQ<38>	CU33	DDR1_DQ<38>	
37	M_K_DQ<37>	CR29	DDR1_DQ<37>	
36	M_K_DQ<36>	CU29	DDR1_DQ<36>	
35	M_K_DQ<35>	CP34	DDR1_DQ<35>	
34	M_K_DQ<34>	CT34	DDR1_DQ<34>	
33	M_K_DQ<33>	CP30	DDR1_DQ<33>	
32	M_K_DQ<32>	CT30	DDR1_DQ<32>	
31	M_K_DQ<31>	CV16	DDR1_DQ<31>	
30	M_K_DQ<30>	CT16	DDR1_DQ<30>	
29	M_K_DQ<29>	CV12	DDR1_DQ<29>	
28	M_K_DQ<28>	CT12	DDR1_DQ<28>	
27	M_K_DQ<27>	CU17	DDR1_DQ<27>	
26	M_K_DQ<26>	CR17	DDR1_DQ<26>	
25	M_K_DQ<25>	CU13	DDR1_DQ<25>	
24	M_K_DQ<24>	CR13	DDR1_DQ<24>	
23	M_K_DQ<23>	CV10	DDR1_DQ<23>	
22	M_K_DQ<22>	CW9	DDR1_DQ<22>	
21	M_K_DQ<21>	CT6	DDR1_DQ<21>	
20	M_K_DQ<20>	CP6	DDR1_DQ<20>	
19	M_K_DQ<19>	CP10	DDR1_DQ<19>	
18	M_K_DQ<18>	CT10	DDR1_DQ<18>	
17	M_K_DQ<17>	CU7	DDR1_DQ<17>	
16	M_K_DQ<16>	CR7	DDR1_DQ<16>	
15	M_K_DQ<15>	DF10	DDR1_DQ<15>	
14	M_K_DQ<14>	DB10	DDR1_DQ<14>	
13	M_K_DQ<13>	DB6	DDR1_DQ<13>	
12	M_K_DQ<12>	CY6	DDR1_DQ<12>	
11	M_K_DQ<11>	DE11	DDR1_DQ<11>	
10	M_K_DQ<10>	DC11	DDR1_DQ<10>	
9	M_K_DQ<9>	DC7	DDR1_DQ<9>	
8	M_K_DQ<8>	DA7	DDR1_DQ<8>	
7	M_K_DQ<7>	CW3	DDR1_DQ<7>	
6	M_K_DQ<6>	CV2	DDR1_DQ<6>	
5	M_K_DQ<5>	CL3	DDR1_DQ<5>	
4	M_K_DQ<4>	CM4	DDR1_DQ<4>	
3	M_K_DQ<3>	CY4	DDR1_DQ<3>	
2	M_K_DQ<2>	CV4	DDR1_DQ<2>	
1	M_K_DQ<1>	CP2	DDR1_DQ<1>	
0	M_K_DQ<0>	CP4	DDR1_DQ<0>	

93< OUT M_K_CS_N<3..0>

	NC_M_K_CS_N<9>	DA27	DDR1_CS_N<9>
	NC_M_K_CS_N<8>	CR21	DDR1_CS_N<8>
	NC_M_K_CS_N<7>	CT26	DDR1_CS_N<7>
	NC_M_K_CS_N<6>	DA29	DDR1_CS_N<6>
	NC_M_K_CS_N<5>	CT24	DDR1_CS_N<5>
	NC_M_K_CS_N<4>	CU25	DDR1_CS_N<4>
3	M_K_CS_N<3>	CR27	DDR1_CS_N<3>
2	M_K_CS_N<2>	CR23	DDR1_CS_N<2>
1	M_K_CS_N<1>	CU23	DDR1_CS_N<1>
0	M_K_CS_N<0>	DB24	DDR1_CS_N<0>

	NC_M_K_CK_DP<3>	DC21	DDR1_CLK_DP<3>
93< OUT	M_K_CK_DP<2>	CV24	DDR1_CLK_DP<2>
	NC_M_K_CK_DP<1>	CY22	DDR1_CLK_DP<1>
93< OUT	M_K_CK_DP<0>	CY20	DDR1_CLK_DP<0>
	NC_M_K_CK_DN<3>	DA21	DDR1_CLK_DN<3>
93< OUT	M_K_CK_DN<2>	CY24	DDR1_CLK_DN<2>
	NC_M_K_CK_DN<1>	CV22	DDR1_CLK_DN<1>
93< OUT	M_K_CK_DN<0>	CV20	DDR1_CLK_DN<0>

			DDR1_DQS_DP<17>
			DDR1_DQS_DP<16>
			DDR1_DQS_DP<15>
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			DDR1_DQS_DP<13>
			DDR1_DQS_DP<12>
			DDR1_DQS_DP<11>
			DDR1_DQS_DP<10>
			DDR1_DQS_DP<9>
			DDR1_DQS_DP<8>
			DDR1_DQS_DP<7>
			DDR1_DQS_DP<6>
			DDR1_DQS_DP<5>
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			DDR1_DQS_DP<3>
			DDR1_DQS_DP<2>
			DDR1_DQS_DP<1>
			DDR1_DQS_DP<0>
			DDR1_DQS_DN<17>
			DDR1_DQS_DN<16>
			DDR1_DQS_DN<15>
			DDR1_DQS_DN<14>
			DDR1_DQS_DN<13>
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			DDR1_DQS_DN<11>
			DDR1_DQS_DN<10>
			DDR1_DQS_DN<9>
			DDR1_DQS_DN<8>
			DDR1_DQS_DN<7>
			DDR1_DQS_DN<6>
			DDR1_DQS_DN<5>
			DDR1_DQS_DN<4>
			DDR1_DQS_DN<3>
			DDR1_DQS_DN<2>
			DDR1_DQS_DN<1>
			DDR1_DQS_DN<0>
			DDR1_MA<15>
			DDR1_MA<14>
			DDR1_MA<13>
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			DDR1_MA<11>
			DDR1_MA<10>
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			DDR1_MA<4>
			DDR1_MA<3>
			DDR1_MA<2>
			DDR1_MA<1>
			DDR1_MA<0>
			DDR1_ECC<7>
			DDR1_ECC<6>
			DDR1_ECC<5>
			DDR1_ECC<4>
			DDR1_ECC<3>
			DDR1_ECC<2>
			DDR1_ECC<1>
			DDR1_ECC<0>
			DDR1_CKE<5>
			DDR1_CKE<4>
			DDR1_CKE<3>
			DDR1_CKE<2>
			DDR1_CKE<1>
			DDR1_CKE<0>
			DDR1_BA<2>
			DDR1_BA<1>
			DDR1_BA<0>
			DDR1_ODT<5>
			DDR1_ODT<4>
			DDR1_ODT<3>
			DDR1_ODT<2>
			DDR1_ODT<1>
			DDR1_ODT<0>
			DDR1_WE_N
			DDR1_RAS_N
			DDR1_PAR_ERR_N
			DDR1_CAS_N
			DDR1_MA_PAR

M_K_DQS_DP<17..0> 93<> BI

CY14	M_K_DQS_DP<17>	17	
DB38	M_K_DQS_DP<16>	16	
CP38	M_K_DQS_DP<15>	15	
DC33	M_K_DQS_DP<14>	14	
CU31	M_K_DQS_DP<13>	13	
CT14	M_K_DQS_DP<12>	12	
CP8	M_K_DQS_DP<11>	11	
DD8	M_K_DQS_DP<10>	10	
CT2	M_K_DQS_DP<9>	9	
DC15	M_K_DQS_DP<8>	8	
DC39	M_K_DQS_DP<7>	7	
CU39	M_K_DQS_DP<6>	6	
DB34	M_K_DQS_DP<5>	5	
CP32	M_K_DQS_DP<4>	4	
CU15	M_K_DQS_DP<3>	3	
CU9	M_K_DQS_DP<2>	2	
DE9	M_K_DQS_DP<1>	1	
CR3	M_K_DQS_DP<0>	0	

M_K_DQS_DN<17..0> 93<> BI

DB14	M_K_DQS_DN<17>	17	
CY38	M_K_DQS_DN<16>	16	
CT38	M_K_DQS_DN<15>	15	
DE33	M_K_DQS_DN<14>	14	
CR31	M_K_DQS_DN<13>	13	
CP14	M_K_DQS_DN<12>	12	
CT8	M_K_DQS_DN<11>	11	
DB8	M_K_DQS_DN<10>	10	
CR1	M_K_DQS_DN<9>	9	
DE15	M_K_DQS_DN<8>	8	
DE39	M_K_DQS_DN<7>	7	
CR39	M_K_DQS_DN<6>	6	
CY34	M_K_DQS_DN<5>	5	
CT32	M_K_DQS_DN<4>	4	
CR15	M_K_DQS_DN<3>	3	
CV8	M_K_DQS_DN<2>	2	
DC9	M_K_DQS_DN<1>	1	
CT4	M_K_DQS_DN<0>	0	

M_K_MA<15..0> 93< OUT

DC17	M_K_MA<15>	15	
DB18	M_K_MA<14>	14	
DB30	M_K_MA<13>	13	
DC19	M_K_MA<12>	12	
DE19	M_K_MA<11>	11	
DF26	M_K_MA<10>	10	
DA19	M_K_MA<9>	9	
DB20	M_K_MA<8>	8	
DF20	M_K_MA<7>	7	
DE21	M_K_MA<6>	6	
DF22	M_K_MA<5>	5	
DB22	M_K_MA<4>	4	
DA23	M_K_MA<3>	3	
DF24	M_K_MA<2>	2	
DE23	M_K_MA<1>	1	
DC23	M_K_MA<0>	0	

M_K_ECC<7..0> 93<> BI

DF16	M_K_ECC<7>	7	
DA15	M_K_ECC<6>	6	
DC13	M_K_ECC<5>	5	
DA13	M_K_ECC<4>	4	
DB16	M_K_ECC<3>	3	
DD16	M_K_ECC<2>	2	
DF14	M_K_ECC<1>	1	
DE13	M_K_ECC<0>	0	

CT18	NC_M_K_CKE<5>		
CR19	NC_M_K_CKE<4>		
DA17	NC_M_K_CKE<3>		
CY18	NC_M_K_CKE<2>		
CU19	M_K_CKE<1>	1	
CT20	M_K_CKE<0>	0	

M_K_CKE<1..0> 93< OUT

M_K_BA<2..0> 93< OUT

DF18	M_K_BA<2>	2	
DC25	M_K_BA<1>	1	
DB26	M_K_BA<0>	0	

CY28	NC_M_K_ODT<5>		
CU27	NC_M_K_ODT<4>		
CV26	NC_M_K_ODT<3>		
CY26	NC_M_K_ODT<2>		
DA25	M_K_ODT<1>	1	
CT22	M_K_ODT<0>	0	

M_K_ODT<1..0> 93< OUT

CV28	M_K_WE_N		93< OUT
DB28	M_K_RAS_N		93< OUT
CU21	M_K_PAR_ERR_N<0>		93< IN
CY30	M_K_CAS_N		93< OUT
DE25	M_K_MA_PAR		93< OUT

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CPU SOCKET 2 (3 OF 13)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 81 OF 303	

INTEL CONFIDENTIAL

U8C1 IC

SANDYBRIDGE_EP_EXT_D

94<> BI M_L_DQ<63..0>

63	M_L_DQ<63>	AE3	DDR2_DQ<63>	
62	M_L_DQ<62>	AF2	DDR2_DQ<62>	
61	M_L_DQ<61>	V4	DDR2_DQ<61>	
60	M_L_DQ<60>	U3	DDR2_DQ<60>	
59	M_L_DQ<59>	AE5	DDR2_DQ<59>	
58	M_L_DQ<58>	AF4	DDR2_DQ<58>	
57	M_L_DQ<57>	Y4	DDR2_DQ<57>	
56	M_L_DQ<56>	W3	DDR2_DQ<56>	
55	M_L_DQ<55>	U9	DDR2_DQ<55>	
54	M_L_DQ<54>	R9	DDR2_DQ<54>	
53	M_L_DQ<53>	V14	DDR2_DQ<53>	
52	M_L_DQ<52>	T14	DDR2_DQ<52>	
51	M_L_DQ<51>	V10	DDR2_DQ<51>	
50	M_L_DQ<50>	T10	DDR2_DQ<50>	
49	M_L_DQ<49>	U13	DDR2_DQ<49>	
48	M_L_DQ<48>	R13	DDR2_DQ<48>	
47	M_L_DQ<47>	AE7	DDR2_DQ<47>	
46	M_L_DQ<46>	AD8	DDR2_DQ<46>	
45	M_L_DQ<45>	W7	DDR2_DQ<45>	
44	M_L_DQ<44>	U7	DDR2_DQ<44>	
43	M_L_DQ<43>	AG7	DDR2_DQ<43>	
42	M_L_DQ<42>	AF8	DDR2_DQ<42>	
41	M_L_DQ<41>	Y6	DDR2_DQ<41>	
40	M_L_DQ<40>	V6	DDR2_DQ<40>	
39	M_L_DQ<39>	AD10	DDR2_DQ<39>	
38	M_L_DQ<38>	AB10	DDR2_DQ<38>	
37	M_L_DQ<37>	AA13	DDR2_DQ<37>	
36	M_L_DQ<36>	AD14	DDR2_DQ<36>	
35	M_L_DQ<35>	AF10	DDR2_DQ<35>	
34	M_L_DQ<34>	AG11	DDR2_DQ<34>	
33	M_L_DQ<33>	AE13	DDR2_DQ<33>	
32	M_L_DQ<32>	AC13	DDR2_DQ<32>	
31	M_L_DQ<31>	AD32	DDR2_DQ<31>	
30	M_L_DQ<30>	AB32	DDR2_DQ<30>	
29	M_L_DQ<29>	W35	DDR2_DQ<29>	
28	M_L_DQ<28>	AA35	DDR2_DQ<28>	
27	M_L_DQ<27>	AF32	DDR2_DQ<27>	
26	M_L_DQ<26>	AE33	DDR2_DQ<26>	
25	M_L_DQ<25>	AE35	DDR2_DQ<25>	
24	M_L_DQ<24>	AC35	DDR2_DQ<24>	
23	M_L_DQ<23>	T30	DDR2_DQ<23>	
22	M_L_DQ<22>	V30	DDR2_DQ<22>	
21	M_L_DQ<21>	P34	DDR2_DQ<21>	
20	M_L_DQ<20>	T34	DDR2_DQ<20>	
19	M_L_DQ<19>	U29	DDR2_DQ<19>	
18	M_L_DQ<18>	W29	DDR2_DQ<18>	
17	M_L_DQ<17>	R33	DDR2_DQ<17>	
16	M_L_DQ<16>	U33	DDR2_DQ<16>	
15	M_L_DQ<15>	AE37	DDR2_DQ<15>	
14	M_L_DQ<14>	AF38	DDR2_DQ<14>	
13	M_L_DQ<13>	AA41	DDR2_DQ<13>	
12	M_L_DQ<12>	AC41	DDR2_DQ<12>	
11	M_L_DQ<11>	AC37	DDR2_DQ<11>	
10	M_L_DQ<10>	AA37	DDR2_DQ<10>	
9	M_L_DQ<9>	AD40	DDR2_DQ<9>	
8	M_L_DQ<8>	AE41	DDR2_DQ<8>	
7	M_L_DQ<7>	U37	DDR2_DQ<7>	
6	M_L_DQ<6>	R37	DDR2_DQ<6>	
5	M_L_DQ<5>	U41	DDR2_DQ<5>	
4	M_L_DQ<4>	R41	DDR2_DQ<4>	
3	M_L_DQ<3>	T36	DDR2_DQ<3>	
2	M_L_DQ<2>	P36	DDR2_DQ<2>	
1	M_L_DQ<1>	V40	DDR2_DQ<1>	
0	M_L_DQ<0>	T40	DDR2_DQ<0>	

94< OUT M_L_CS_N<3..0>

NC_M_L_CS_N<9>	AA17	DDR2_CS_N<9>	
NC_M_L_CS_N<8>	W17	DDR2_CS_N<8>	
NC_M_L_CS_N<7>	Y16	DDR2_CS_N<7>	
NC_M_L_CS_N<6>	AB16	DDR2_CS_N<6>	
NC_M_L_CS_N<5>	P18	DDR2_CS_N<5>	
NC_M_L_CS_N<4>	AA19	DDR2_CS_N<4>	
3 M_L_CS_N<3>	AA15	DDR2_CS_N<3>	
2 M_L_CS_N<2>	AD16	DDR2_CS_N<2>	
1 M_L_CS_N<1>	AE19	DDR2_CS_N<1>	
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NC_M_L_CK_DP<3>	AA23	DDR2_CLK_DP<3>	
94< OUT M_L_CK_DP<2>	AA21	DDR2_CLK_DP<2>	
NC_M_L_CK_DP<1>	AB22	DDR2_CLK_DP<1>	
94< OUT M_L_CK_DP<0>	AB24	DDR2_CLK_DP<0>	
NC_M_L_CK_DN<3>	W23	DDR2_CLK_DN<3>	
94< OUT M_L_CK_DN<2>	W21	DDR2_CLK_DN<2>	
NC_M_L_CK_DN<1>	Y22	DDR2_CLK_DN<1>	
94< OUT M_L_CK_DN<0>	Y24	DDR2_CLK_DN<0>	

DDR2_DQS_DP<17>	AC29	M_L_DQS_DP<17>	17	
DDR2_DQS_DP<16>	AC5	M_L_DQS_DP<16>	16	
DDR2_DQS_DP<15>	T12	M_L_DQS_DP<15>	15	
DDR2_DQS_DP<14>	Y8	M_L_DQS_DP<14>	14	
DDR2_DQS_DP<13>	AB12	M_L_DQS_DP<13>	13	
DDR2_DQS_DP<12>	Y34	M_L_DQS_DP<12>	12	
DDR2_DQS_DP<11>	V32	M_L_DQS_DP<11>	11	
DDR2_DQS_DP<10>	AB40	M_L_DQS_DP<10>	10	
DDR2_DQS_DP<9>	U39	M_L_DQS_DP<9>	9	
DDR2_DQS_DP<8>	AC27	M_L_DQS_DP<8>	8	
DDR2_DQS_DP<7>	AB4	M_L_DQS_DP<7>	7	
DDR2_DQS_DP<6>	W11	M_L_DQS_DP<6>	6	
DDR2_DQS_DP<5>	AC7	M_L_DQS_DP<5>	5	
DDR2_DQS_DP<4>	AE11	M_L_DQS_DP<4>	4	
DDR2_DQS_DP<3>	AC33	M_L_DQS_DP<3>	3	
DDR2_DQS_DP<2>	U31	M_L_DQS_DP<2>	2	
DDR2_DQS_DP<1>	AB38	M_L_DQS_DP<1>	1	
DDR2_DQS_DP<0>	V38	M_L_DQS_DP<0>	0	

M_L_DQS_DP<17..0> BI 94<>

DDR2_DQS_DN<17>	AD28	M_L_DQS_DN<17>	17	
DDR2_DQS_DN<16>	AD4	M_L_DQS_DN<16>	16	
DDR2_DQS_DN<15>	V12	M_L_DQS_DN<15>	15	
DDR2_DQS_DN<14>	AA7	M_L_DQS_DN<14>	14	
DDR2_DQS_DN<13>	AD12	M_L_DQS_DN<13>	13	
DDR2_DQS_DN<12>	AB34	M_L_DQS_DN<12>	12	
DDR2_DQS_DN<11>	T32	M_L_DQS_DN<11>	11	
DDR2_DQS_DN<10>	AC39	M_L_DQS_DN<10>	10	
DDR2_DQS_DN<9>	W39	M_L_DQS_DN<9>	9	
DDR2_DQS_DN<8>	AB28	M_L_DQS_DN<8>	8	
DDR2_DQS_DN<7>	AC3	M_L_DQS_DN<7>	7	
DDR2_DQS_DN<6>	U11	M_L_DQS_DN<6>	6	
DDR2_DQS_DN<5>	AB8	M_L_DQS_DN<5>	5	
DDR2_DQS_DN<4>	AC11	M_L_DQS_DN<4>	4	
DDR2_DQS_DN<3>	AA33	M_L_DQS_DN<3>	3	
DDR2_DQS_DN<2>	W31	M_L_DQS_DN<2>	2	
DDR2_DQS_DN<1>	AD38	M_L_DQS_DN<1>	1	
DDR2_DQS_DN<0>	T38	M_L_DQS_DN<0>	0	

M_L_DQS_DN<17..0> BI 94<>

DDR2_MA<15>	U25	M_L_MA<15>	15	
DDR2_MA<14>	W25	M_L_MA<14>	14	
DDR2_MA<13>	R15	M_L_MA<13>	13	
DDR2_MA<12>	T24	M_L_MA<12>	12	
DDR2_MA<11>	U23	M_L_MA<11>	11	
DDR2_MA<10>	T18	M_L_MA<10>	10	
DDR2_MA<9>	R23	M_L_MA<9>	9	
DDR2_MA<8>	T22	M_L_MA<8>	8	
DDR2_MA<7>	P22	M_L_MA<7>	7	
DDR2_MA<6>	R21	M_L_MA<6>	6	
DDR2_MA<5>	U21	M_L_MA<5>	5	
DDR2_MA<4>	P20	M_L_MA<4>	4	
DDR2_MA<3>	T20	M_L_MA<3>	3	
DDR2_MA<2>	U19	M_L_MA<2>	2	
DDR2_MA<1>	R19	M_L_MA<1>	1	
DDR2_MA<0>	AB18	M_L_MA<0>	0	

M_L_MA<15..0> OUT 94<

DDR2_ECC<7>	AA27	M_L_ECC<7>	7	
DDR2_ECC<6>	W27	M_L_ECC<6>	6	
DDR2_ECC<5>	AD30	M_L_ECC<5>	5	
DDR2_ECC<4>	AB30	M_L_ECC<4>	4	
DDR2_ECC<3>	AB26	M_L_ECC<3>	3	
DDR2_ECC<2>	Y26	M_L_ECC<2>	2	
DDR2_ECC<1>	AF28	M_L_ECC<1>	1	
DDR2_ECC<0>	AF30	M_L_ECC<0>	0	

M_L_ECC<7..0> BI 94<>

DDR2_CKE<5>	AE23	NC_M_L_CKE<5>	
DDR2_CKE<4>	AE25	NC_M_L_CKE<4>	
DDR2_CKE<3>	AD24	NC_M_L_CKE<3>	
DDR2_CKE<2>	U27	NC_M_L_CKE<2>	
DDR2_CKE<1>	T26	M_L_CKE<1>	1
DDR2_CKE<0>	AA25	M_L_CKE<0>	0

M_L_CKE<1..0> OUT 94<

DDR2_BA<2>	P24	M_L_BA<2>	2	
DDR2_BA<1>	L17	M_L_BA<1>	1	
DDR2_BA<0>	R17	M_L_BA<0>	0	

M_L_BA<2..0> OUT 94<

DDR2_ODT<5>	AE21	NC_M_L_ODT<5>	
DDR2_ODT<4>	AD22	NC_M_L_ODT<4>	
DDR2_ODT<3>	Y18	NC_M_L_ODT<3>	
DDR2_ODT<2>	AD18	NC_M_L_ODT<2>	
DDR2_ODT<1>	W19	M_L_ODT<1>	1
DDR2_ODT<0>	Y20	M_L_ODT<0>	0

M_L_ODT<1..0> OUT 94<

DDR2_WE_N	P16	M_L_WE_N	OUT 94<
DDR2_RAS_N	U17	M_L_RAS_N	OUT 94<
DDR2_PAR_ERR_N	AD20	M_L_PAR_ERR_N<0>	IN 94>
DDR2_CAS_N	T16	M_L_CAS_N	OUT 94<
DDR2_MA_PAR	M18	M_L_MA_PAR	OUT 94<

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E64556-001

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CPU SOCKET 2 (4 OF 13)

DEPARTMENT	Intel Corporation	SIZE / CODE / DOCUMENT NUMBER / REV	
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B / 34649 / 444359 / 1.0	
		SCALE: DO NOT SCALE DRAWING	SHEET 82 OF 303

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U8C1 IC

SANDYBRIDGE_EP_EXT_D

95<> BI	M_M_DQ<63..0>	63	M_M_DQ<63>	M2	DDR3_DQ<63>		
		62	M_M_DQ<62>	L1	DDR3_DQ<62>		
		61	M_M_DQ<61>	H4	DDR3_DQ<61>		
		60	M_M_DQ<60>	F4	DDR3_DQ<60>		
		59	M_M_DQ<59>	P4	DDR3_DQ<59>		
		58	M_M_DQ<58>	N3	DDR3_DQ<58>		
		57	M_M_DQ<57>	H2	DDR3_DQ<57>		
		56	M_M_DQ<56>	G3	DDR3_DQ<56>		
		55	M_M_DQ<55>	M6	DDR3_DQ<55>		
		54	M_M_DQ<54>	L7	DDR3_DQ<54>		
		53	M_M_DQ<53>	D6	DDR3_DQ<53>		
		52	M_M_DQ<52>	C7	DDR3_DQ<52>		
		51	M_M_DQ<51>	P6	DDR3_DQ<51>		
		50	M_M_DQ<50>	N7	DDR3_DQ<50>		
		49	M_M_DQ<49>	F6	DDR3_DQ<49>		
		48	M_M_DQ<48>	E7	DDR3_DQ<48>		
		47	M_M_DQ<47>	M10	DDR3_DQ<47>		
		46	M_M_DQ<46>	K10	DDR3_DQ<46>		
		45	M_M_DQ<45>	M14	DDR3_DQ<45>		
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		43	M_M_DQ<43>	L9	DDR3_DQ<43>		
		42	M_M_DQ<42>	J9	DDR3_DQ<42>		
		41	M_M_DQ<41>	L13	DDR3_DQ<41>		
		40	M_M_DQ<40>	J13	DDR3_DQ<40>		
		39	M_M_DQ<39>	A9	DDR3_DQ<39>		
		38	M_M_DQ<38>	F10	DDR3_DQ<38>		
		37	M_M_DQ<37>	B12	DDR3_DQ<37>		
		36	M_M_DQ<36>	F12	DDR3_DQ<36>		
		35	M_M_DQ<35>	E9	DDR3_DQ<35>		
		34	M_M_DQ<34>	C9	DDR3_DQ<34>		
		33	M_M_DQ<33>	A11	DDR3_DQ<33>		
		32	M_M_DQ<32>	D12	DDR3_DQ<32>		
		31	M_M_DQ<31>	M26	DDR3_DQ<31>		
		30	M_M_DQ<30>	N27	DDR3_DQ<30>		
		29	M_M_DQ<29>	K32	DDR3_DQ<29>		
		28	M_M_DQ<28>	L33	DDR3_DQ<28>		
		27	M_M_DQ<27>	L27	DDR3_DQ<27>		
		26	M_M_DQ<26>	M28	DDR3_DQ<26>		
		25	M_M_DQ<25>	L31	DDR3_DQ<25>		
		24	M_M_DQ<24>	M32	DDR3_DQ<24>		
		23	M_M_DQ<23>	B32	DDR3_DQ<23>		
		22	M_M_DQ<22>	A33	DDR3_DQ<22>		
		21	M_M_DQ<21>	C35	DDR3_DQ<21>		
		20	M_M_DQ<20>	E35	DDR3_DQ<20>		
		19	M_M_DQ<19>	F32	DDR3_DQ<19>		
		18	M_M_DQ<18>	D32	DDR3_DQ<18>		
		17	M_M_DQ<17>	F34	DDR3_DQ<17>		
		16	M_M_DQ<16>	A35	DDR3_DQ<16>		
		15	M_M_DQ<15>	H36	DDR3_DQ<15>		
		14	M_M_DQ<14>	K36	DDR3_DQ<14>		
		13	M_M_DQ<13>	K40	DDR3_DQ<13>		
		12	M_M_DQ<12>	M40	DDR3_DQ<12>		
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		10	M_M_DQ<10>	L35	DDR3_DQ<10>		
		9	M_M_DQ<9>	L39	DDR3_DQ<9>		
		8	M_M_DQ<8>	N39	DDR3_DQ<8>		
		7	M_M_DQ<7>	A37	DDR3_DQ<7>		
		6	M_M_DQ<6>	F38	DDR3_DQ<6>		
		5	M_M_DQ<5>	D40	DDR3_DQ<5>		
		4	M_M_DQ<4>	F40	DDR3_DQ<4>		
		3	M_M_DQ<3>	E37	DDR3_DQ<3>		
		2	M_M_DQ<2>	C37	DDR3_DQ<2>		
		1	M_M_DQ<1>	A39	DDR3_DQ<1>		
		0	M_M_DQ<0>	B40	DDR3_DQ<0>		
			NC_M_M_CS_N<9>	K16	DDR3_CS_N<9>		
			NC_M_M_CS_N<8>	D16	DDR3_CS_N<8>		
			NC_M_M_CS_N<7>	E15	DDR3_CS_N<7>		
			NC_M_M_CS_N<6>	F16	DDR3_CS_N<6>		
			NC_M_M_CS_N<5>	G17	DDR3_CS_N<5>		
			NC_M_M_CS_N<4>	K18	DDR3_CS_N<4>		
95< OUT	M_M_CS_N<3..0>	3	M_M_CS_N<3>	G15	DDR3_CS_N<3>		
		2	M_M_CS_N<2>	F14	DDR3_CS_N<2>		
		1	M_M_CS_N<1>	J19	DDR3_CS_N<1>		
		0	M_M_CS_N<0>	G19	DDR3_CS_N<0>		
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95< OUT			M_M_CK_DP<2>	K20	DDR3_CLK_DP<2>		
			NC_M_M_CK_DP<1>	L21	DDR3_CLK_DP<1>		
95< OUT			M_M_CK_DP<0>	L23	DDR3_CLK_DP<0>		
			NC_M_M_CK_DN<3>	K22	DDR3_CLK_DN<3>		
95< OUT			M_M_CK_DN<2>	M20	DDR3_CLK_DN<2>		
			NC_M_M_CK_DN<1>	J21	DDR3_CLK_DN<1>		
95< OUT			M_M_CK_DN<0>	J23	DDR3_CLK_DN<0>		

	M_M_DQS_DP<17..0>	95<> BI			DDR3_DQS_DP<17>	F28	M_M_DQS_DP<17> 17
					DDR3_DQS_DP<16>	J3	M_M_DQS_DP<16> 16
					DDR3_DQS_DP<15>	G7	M_M_DQS_DP<15> 15
					DDR3_DQS_DP<14>	K12	M_M_DQS_DP<14> 14
					DDR3_DQS_DP<13>	E11	M_M_DQS_DP<13> 13
					DDR3_DQS_DP<12>	N31	M_M_DQS_DP<12> 12
					DDR3_DQS_DP<11>	D34	M_M_DQS_DP<11> 11
					DDR3_DQS_DP<10>	M38	M_M_DQS_DP<10> 10
					DDR3_DQS_DP<9>	E39	M_M_DQS_DP<9> 9
					DDR3_DQS_DP<8>	E27	M_M_DQS_DP<8> 8
					DDR3_DQS_DP<7>	M4	M_M_DQS_DP<7> 7
					DDR3_DQS_DP<6>	K6	M_M_DQS_DP<6> 6
					DDR3_DQS_DP<5>	N11	M_M_DQS_DP<5> 5
					DDR3_DQS_DP<4>	D10	M_M_DQS_DP<4> 4
					DDR3_DQS_DP<3>	N29	M_M_DQS_DP<3> 3
					DDR3_DQS_DP<2>	E33	M_M_DQS_DP<2> 2
					DDR3_DQS_DP<1>	J37	M_M_DQS_DP<1> 1
					DDR3_DQS_DP<0>	D38	M_M_DQS_DP<0> 0
	M_M_DQS_DN<17..0>	95<> BI			DDR3_DQS_DN<17>	H28	M_M_DQS_DN<17> 17
					DDR3_DQS_DN<16>	K4	M_M_DQS_DN<16> 16
					DDR3_DQS_DN<15>	H6	M_M_DQS_DN<15> 15
					DDR3_DQS_DN<14>	M12	M_M_DQS_DN<14> 14
					DDR3_DQS_DN<13>	G11	M_M_DQS_DN<13> 13
					DDR3_DQS_DN<12>	M30	M_M_DQS_DN<12> 12
					DDR3_DQS_DN<11>	B34	M_M_DQS_DN<11> 11
					DDR3_DQS_DN<10>	K38	M_M_DQS_DN<10> 10
					DDR3_DQS_DN<9>	G39	M_M_DQS_DN<9> 9
					DDR3_DQS_DN<8>	G27	M_M_DQS_DN<8> 8
					DDR3_DQS_DN<7>	L3	M_M_DQS_DN<7> 7
					DDR3_DQS_DN<6>	J7	M_M_DQS_DN<6> 6
					DDR3_DQS_DN<5>	L11	M_M_DQS_DN<5> 5
					DDR3_DQS_DN<4>	B10	M_M_DQS_DN<4> 4
					DDR3_DQS_DN<3>	P28	M_M_DQS_DN<3> 3
					DDR3_DQS_DN<2>	G33	M_M_DQS_DN<2> 2
					DDR3_DQS_DN<1>	L37	M_M_DQS_DN<1> 1
					DDR3_DQS_DN<0>	B38	M_M_DQS_DN<0> 0
	M_M_MA<15..0>	95< OUT			DDR3_MA<15>	F24	M_M_MA<15> 15
					DDR3_MA<14>	D24	M_M_MA<14> 14
					DDR3_MA<13>	A13	M_M_MA<13> 13
					DDR3_MA<12>	E23	M_M_MA<12> 12
					DDR3_MA<11>	A23	M_M_MA<11> 11
					DDR3_MA<10>	D18	M_M_MA<10> 10
					DDR3_MA<9>	G23	M_M_MA<9> 9
					DDR3_MA<8>	D22	M_M_MA<8> 8
					DDR3_MA<7>	B22	M_M_MA<7> 7
					DDR3_MA<6>	F22	M_M_MA<6> 6
					DDR3_MA<5>	A21	M_M_MA<5> 5
					DDR3_MA<4>	D20	M_M_MA<4> 4
					DDR3_MA<3>	B20	M_M_MA<3> 3
					DDR3_MA<2>	F20	M_M_MA<2> 2
					DDR3_MA<1>	E21	M_M_MA<1> 1
					DDR3_MA<0>	A19	M_M_MA<0> 0
	M_M_ECC<7..0>	95<> BI			DDR3_ECC<7>	H26	M_M_ECC<7> 7
					DDR3_ECC<6>	F26	M_M_ECC<6> 6
					DDR3_ECC<5>	H30	M_M_ECC<5> 5
					DDR3_ECC<4>	F30	M_M_ECC<4> 4
					DDR3_ECC<3>	C25	M_M_ECC<3> 3
					DDR3_ECC<2>	E25	M_M_ECC<2> 2
					DDR3_ECC<1>	J29	M_M_ECC<1> 1
					DDR3_ECC<0>	G29	M_M_ECC<0> 0
					DDR3_CKE<5>	R27	NC_M_M_CKE<5>
					DDR3_CKE<4>	R25	NC_M_M_CKE<4>
					DDR3_CKE<3>	N25	NC_M_M_CKE<3>
					DDR3_CKE<2>	J25	NC_M_M_CKE<2>
	M_M_CKE<1..0>	95< OUT			DDR3_CKE<1>	M24	M_M_CKE<1> 1
					DDR3_CKE<0>	K24	M_M_CKE<0> 0
	M_M_BA<2..0>	95< OUT			DDR3_BA<2>	B24	M_M_BA<2> 2
					DDR3_BA<1>	E19	M_M_BA<1> 1
					DDR3_BA<0>	A17	M_M_BA<0> 0
					DDR3_ODT<5>	M16	NC_M_M_ODT<5>
					DDR3_ODT<4>	D14	NC_M_M_ODT<4>
					DDR3_ODT<3>	J17	NC_M_M_ODT<3>
	M_M_ODT<1..0>	95< OUT			DDR3_ODT<2>	E17	NC_M_M_ODT<2>
					DDR3_ODT<1>	F18	M_M_ODT<1> 1
					DDR3_ODT<0>	L19	M_M_ODT<0> 0
		95< OUT			DDR3_WE_N	A15	M_M_WE_N
		95< OUT			DDR3_RAS_N	B16	M_M_RAS_N
		95> IN			DDR3_PAR_ERR_N	G21	M_M_PAR_ERR_N<0>
		95< OUT			DDR3_CAS_N	B14	M_M_CAS_N
		95< OUT			DDR3_MA_PAR	B18	M_M_MA_PAR

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CPU SOCKET 2 (5 OF 13)

DEPARTMENT: DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	SIZE: B / CODE: 34649 / DOCUMENT NUMBER: 444359 / REV: 1.0	SCALE: DO NOT SCALE DRAWING / SHEET 83 OF 303

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U8C1
IC

SANDYBRIDGE_EP_EXT_D

TP_P3E_CPU2_RX_PE1A_DP<3>	E55	PE1A_RX_DP<3>	PE1A_TX_DP<3>	J45	TP_P3E_CPU2_TX_PE1A_DP<3>
TP_P3E_CPU2_RX_PE1A_DP<2>	D54	PE1A_RX_DP<2>	PE1A_TX_DP<2>	H44	TP_P3E_CPU2_TX_PE1A_DP<2>
TP_P3E_CPU2_RX_PE1A_DP<1>	D52	PE1A_RX_DP<1>	PE1A_TX_DP<1>	J43	TP_P3E_CPU2_TX_PE1A_DP<1>
TP_P3E_CPU2_RX_PE1A_DP<0>	C51	PE1A_RX_DP<0>	PE1A_TX_DP<0>	H42	TP_P3E_CPU2_TX_PE1A_DP<0>
TP_P3E_CPU2_RX_PE1A_DN<3>	G55	PE1A_RX_DN<3>	PE1A_TX_DN<3>	L45	TP_P3E_CPU2_TX_PE1A_DN<3>
TP_P3E_CPU2_RX_PE1A_DN<2>	F54	PE1A_RX_DN<2>	PE1A_TX_DN<2>	K44	TP_P3E_CPU2_TX_PE1A_DN<2>
TP_P3E_CPU2_RX_PE1A_DN<1>	F52	PE1A_RX_DN<1>	PE1A_TX_DN<1>	L43	TP_P3E_CPU2_TX_PE1A_DN<1>
TP_P3E_CPU2_RX_PE1A_DN<0>	E51	PE1A_RX_DN<0>	PE1A_TX_DN<0>	K42	TP_P3E_CPU2_TX_PE1A_DN<0>
TP_P3E_CPU2_RX_PE1B_DP<3>	K56	PE1B_RX_DP<7>	PE1B_TX_DP<7>	J49	TP_P3E_CPU2_TX_PE1B_DP<3>
TP_P3E_CPU2_RX_PE1B_DP<2>	J57	PE1B_RX_DP<6>	PE1B_TX_DP<6>	H48	TP_P3E_CPU2_TX_PE1B_DP<2>
TP_P3E_CPU2_RX_PE1B_DP<1>	K54	PE1B_RX_DP<5>	PE1B_TX_DP<5>	J47	TP_P3E_CPU2_TX_PE1B_DP<1>
TP_P3E_CPU2_RX_PE1B_DP<0>	J53	PE1B_RX_DP<4>	PE1B_TX_DP<4>	H46	TP_P3E_CPU2_TX_PE1B_DP<0>
TP_P3E_CPU2_RX_PE1B_DN<3>	M56	PE1B_RX_DN<7>	PE1B_TX_DN<7>	L49	TP_P3E_CPU2_TX_PE1B_DN<3>
TP_P3E_CPU2_RX_PE1B_DN<2>	L57	PE1B_RX_DN<6>	PE1B_TX_DN<6>	K48	TP_P3E_CPU2_TX_PE1B_DN<2>
TP_P3E_CPU2_RX_PE1B_DN<1>	M54	PE1B_RX_DN<5>	PE1B_TX_DN<5>	L47	TP_P3E_CPU2_TX_PE1B_DN<1>
TP_P3E_CPU2_RX_PE1B_DN<0>	L53	PE1B_RX_DN<4>	PE1B_TX_DN<4>	K46	TP_P3E_CPU2_TX_PE1B_DN<0>
TP_P3E_CPU2_RX_PE2A_DP<3>	U55	PE2A_RX_DP<3>	PE2A_TX_DP<3>	AM52	TP_P3E_CPU2_TX_PE2A_DP<3>
TP_P3E_CPU2_RX_PE2A_DP<2>	T56	PE2A_RX_DP<2>	PE2A_TX_DP<2>	AN51	TP_P3E_CPU2_TX_PE2A_DP<2>
TP_P3E_CPU2_RX_PE2A_DP<1>	T54	PE2A_RX_DP<1>	PE2A_TX_DP<1>	AM50	TP_P3E_CPU2_TX_PE2A_DP<1>
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TP_P3E_CPU2_RX_PE2A_DN<3>	W55	PE2A_RX_DN<3>	PE2A_TX_DN<3>	AP52	TP_P3E_CPU2_TX_PE2A_DN<3>
TP_P3E_CPU2_RX_PE2A_DN<2>	V56	PE2A_RX_DN<2>	PE2A_TX_DN<2>	AR51	TP_P3E_CPU2_TX_PE2A_DN<2>
TP_P3E_CPU2_RX_PE2A_DN<1>	V54	PE2A_RX_DN<1>	PE2A_TX_DN<1>	AP50	TP_P3E_CPU2_TX_PE2A_DN<1>
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TP_P3E_CPU2_RX_PE2B_DP<3>	AE57	PE2B_RX_DP<7>	PE2B_TX_DP<7>	AP54	TP_P3E_CPU2_TX_PE2B_DP<3>
TP_P3E_CPU2_RX_PE2B_DP<2>	AC55	PE2B_RX_DP<6>	PE2B_TX_DP<6>	AN53	TP_P3E_CPU2_TX_PE2B_DP<2>
TP_P3E_CPU2_RX_PE2B_DP<1>	AB56	PE2B_RX_DP<5>	PE2B_TX_DP<5>	AH54	TP_P3E_CPU2_TX_PE2B_DP<1>
TP_P3E_CPU2_RX_PE2B_DP<0>	AB54	PE2B_RX_DP<4>	PE2B_TX_DP<4>	AG53	TP_P3E_CPU2_TX_PE2B_DP<0>
TP_P3E_CPU2_RX_PE2B_DN<3>	AF58	PE2B_RX_DN<7>	PE2B_TX_DN<7>	AT54	TP_P3E_CPU2_TX_PE2B_DN<3>
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TP_P3E_CPU2_RX_PE2B_DN<1>	AD56	PE2B_RX_DN<5>	PE2B_TX_DN<5>	AK54	TP_P3E_CPU2_TX_PE2B_DN<1>
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TP_P3E_CPU2_RX_PE2C_DP<2>	AJ57	PE2C_RX_DP<10>	PE2C_TX_DP<10>	AY54	TP_P3E_CPU2_TX_PE2C_DP<2>
TP_P3E_CPU2_RX_PE2C_DP<1>	AK58	PE2C_RX_DP<9>	PE2C_TX_DP<9>	AW53	TP_P3E_CPU2_TX_PE2C_DP<1>
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TP_P3E_CPU2_RX_PE2C_DN<1>	AM58	PE2C_RX_DN<9>	PE2C_TX_DN<9>	BA53	TP_P3E_CPU2_TX_PE2C_DN<1>
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CPU SOCKET 2 (6 OF 13)

DEPARTMENT: DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	SIZE: B	CODE: 34649	DOCUMENT NUMBER: 444359 / REV: 1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 84 OF 303

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IC

SANDYBRIDGE_EP_EXT_D

TP_P3E_CPU2_RX_PE2D_DP<3>	AY56	PE2D_RX_DP<15>	PE2D_TX_DP<15>	AW47	TP_P3E_CPU2_TX_PE2D_DP<3>
TP_P3E_CPU2_RX_PE2D_DP<2>	AY58	PE2D_RX_DP<14>	PE2D_TX_DP<14>	AV48	TP_P3E_CPU2_TX_PE2D_DP<2>
TP_P3E_CPU2_RX_PE2D_DP<1>	AP56	PE2D_RX_DP<13>	PE2D_TX_DP<13>	AW49	TP_P3E_CPU2_TX_PE2D_DP<1>
TP_P3E_CPU2_RX_PE2D_DP<0>	AT58	PE2D_RX_DP<12>	PE2D_TX_DP<12>	AV50	TP_P3E_CPU2_TX_PE2D_DP<0>
TP_P3E_CPU2_RX_PE2D_DN<3>	BB56	PE2D_RX_DN<15>	PE2D_TX_DN<15>	BA47	TP_P3E_CPU2_TX_PE2D_DN<3>
TP_P3E_CPU2_RX_PE2D_DN<2>	BA57	PE2D_RX_DN<14>	PE2D_TX_DN<14>	AY48	TP_P3E_CPU2_TX_PE2D_DN<2>
TP_P3E_CPU2_RX_PE2D_DN<1>	AT56	PE2D_RX_DN<13>	PE2D_TX_DN<13>	BA49	TP_P3E_CPU2_TX_PE2D_DN<1>
TP_P3E_CPU2_RX_PE2D_DN<0>	AV58	PE2D_RX_DN<12>	PE2D_TX_DN<12>	AY50	TP_P3E_CPU2_TX_PE2D_DN<0>
TP_P3E_CPU2_RX_PE3A_DP<3>	AA49	PE3A_RX_DP<3>	PE3A_TX_DP<3>	P48	TP_P3E_CPU2_TX_PE3A_DP<3>
TP_P3E_CPU2_RX_PE3A_DP<2>	AF46	PE3A_RX_DP<2>	PE3A_TX_DP<2>	R47	TP_P3E_CPU2_TX_PE3A_DP<2>
TP_P3E_CPU2_RX_PE3A_DP<1>	AG45	PE3A_RX_DP<1>	PE3A_TX_DP<1>	J51	TP_P3E_CPU2_TX_PE3A_DP<1>
TP_P3E_CPU2_RX_PE3A_DP<0>	AF44	PE3A_RX_DP<0>	PE3A_TX_DP<0>	H50	TP_P3E_CPU2_TX_PE3A_DP<0>
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TP_P3E_CPU2_RX_PE3B_DP<2>	AA53	PE3B_RX_DP<6>	PE3B_TX_DP<6>	P50	TP_P3E_CPU2_TX_PE3B_DP<2>
TP_P3E_CPU2_RX_PE3B_DP<1>	Y52	PE3B_RX_DP<5>	PE3B_TX_DP<5>	R51	TP_P3E_CPU2_TX_PE3B_DP<1>
TP_P3E_CPU2_RX_PE3B_DP<0>	Y50	PE3B_RX_DP<4>	PE3B_TX_DP<4>	P52	TP_P3E_CPU2_TX_PE3B_DP<0>
TP_P3E_CPU2_RX_PE3B_DN<3>	AC51	PE3B_RX_DN<7>	PE3B_TX_DN<7>	U49	TP_P3E_CPU2_TX_PE3B_DN<3>
TP_P3E_CPU2_RX_PE3B_DN<2>	AC53	PE3B_RX_DN<6>	PE3B_TX_DN<6>	T50	TP_P3E_CPU2_TX_PE3B_DN<2>
TP_P3E_CPU2_RX_PE3B_DN<1>	AB52	PE3B_RX_DN<5>	PE3B_TX_DN<5>	U51	TP_P3E_CPU2_TX_PE3B_DN<1>
TP_P3E_CPU2_RX_PE3B_DN<0>	AB50	PE3B_RX_DN<4>	PE3B_TX_DN<4>	T52	TP_P3E_CPU2_TX_PE3B_DN<0>
TP_P3E_CPU2_RX_PE3C_DP<3>	AG49	PE3C_RX_DP<11>	PE3C_TX_DP<11>	Y46	TP_P3E_CPU2_TX_PE3C_DP<3>
TP_P3E_CPU2_RX_PE3C_DP<2>	AF50	PE3C_RX_DP<10>	PE3C_TX_DP<10>	R45	TP_P3E_CPU2_TX_PE3C_DP<2>
TP_P3E_CPU2_RX_PE3C_DP<1>	AG51	PE3C_RX_DP<9>	PE3C_TX_DP<9>	AA47	TP_P3E_CPU2_TX_PE3C_DP<1>
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TP_P3E_CPU2_RX_PE3C_DN<3>	AJ49	PE3C_RX_DN<11>	PE3C_TX_DN<11>	AB46	TP_P3E_CPU2_TX_PE3C_DN<3>
TP_P3E_CPU2_RX_PE3C_DN<2>	AH50	PE3C_RX_DN<10>	PE3C_TX_DN<10>	U45	TP_P3E_CPU2_TX_PE3C_DN<2>
TP_P3E_CPU2_RX_PE3C_DN<1>	AJ51	PE3C_RX_DN<9>	PE3C_TX_DN<9>	AC47	TP_P3E_CPU2_TX_PE3C_DN<1>
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TP_P3E_CPU2_RX_PE3D_DP<2>	AM46	PE3D_RX_DP<14>	PE3D_TX_DP<14>	AC43	TP_P3E_CPU2_TX_PE3D_DP<2>
TP_P3E_CPU2_RX_PE3D_DP<1>	AN47	PE3D_RX_DP<13>	PE3D_TX_DP<13>	Y44	TP_P3E_CPU2_TX_PE3D_DP<1>
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TP_P3E_CPU2_RX_PE3D_DN<3>	AR45	PE3D_RX_DN<15>	PE3D_TX_DN<15>	P44	TP_P3E_CPU2_TX_PE3D_DN<3>
TP_P3E_CPU2_RX_PE3D_DN<2>	AP46	PE3D_RX_DN<14>	PE3D_TX_DN<14>	AA43	TP_P3E_CPU2_TX_PE3D_DN<2>
TP_P3E_CPU2_RX_PE3D_DN<1>	AR47	PE3D_RX_DN<13>	PE3D_TX_DN<13>	AB44	TP_P3E_CPU2_TX_PE3D_DN<1>
TP_P3E_CPU2_RX_PE3D_DN<0>	AJ47	PE3D_RX_DN<12>	PE3D_TX_DN<12>	AC45	TP_P3E_CPU2_TX_PE3D_DN<0>

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CPU SOCKET 2 (7 OF 13)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 85 OF 303	

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IC

SANDYBRIDGE_EP_EXT_D

132< IN XDP_CPU2_MBP_N<7..0>

7	XDP_CPU2_MBP_N<7>	AY44	BPM_N<7>
6	XDP_CPU2_MBP_N<6>	BA43	BPM_N<6>
5	XDP_CPU2_MBP_N<5>	AW43	BPM_N<5>
4	XDP_CPU2_MBP_N<4>	BB44	BPM_N<4>
3	XDP_CPU2_MBP_N<3>	AV44	BPM_N<3>
2	XDP_CPU2_MBP_N<2>	AU43	BPM_N<2>
1	XDP_CPU2_MBP_N<1>	AT44	BPM_N<1>
0	XDP_CPU2_MBP_N<0>	AR43	BPM_N<0>

CAD NOTE: PLACE CLOSE TO CPU

R2R18
36.0 1/16W 5% A93549-074 0402LF
SOCKET2

109<> 63<> 40<> 40<> BI FM_CPU_ONLY_RESET — 1 2 — FM_CPU2_ONLY_RESET_R AN43

NC_CPU2_RSVD<16>	A53	RSVD<16>
NC_CPU2_RSVD<14>	C53	RSVD<14>
		CPU_ONLY_RESET
NC_CPU2_RSVD<15>	B46	RSVD<15>
NC_CPU2_RSVD<13>	D46	RSVD<13>
NC_CPU2_RSVD<3>	K58	RSVD<3>
NC_CPU2_RSVD<60>	AY46	RSVD<60>
NC_CPU2_RSVD<61>	AV46	RSVD<61>
NC_CPU2_RSVD<64>	AM44	RSVD<64>
NC_CPU2_RSVD<65>	AL55	RSVD<65>
NC_CPU2_RSVD<66>	AJ55	RSVD<66>
NC_CPU2_RSVD<55>	BD48	RSVD<55>

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TP_DMI_CPU2_RX_DP<1>	B48	DMI_RX_DP<1>	DMI_TX_DP<1>
TP_DMI_CPU2_RX_DP<0>	C47	DMI_RX_DP<0>	DMI_TX_DP<0>
TP_DMI_CPU2_RX_DN<3>	D50	DMI_RX_DN<3>	DMI_TX_DN<3>
TP_DMI_CPU2_RX_DN<2>	E49	DMI_RX_DN<2>	DMI_TX_DN<2>
TP_DMI_CPU2_RX_DN<1>	D48	DMI_RX_DN<1>	DMI_TX_DN<1>
TP_DMI_CPU2_RX_DN<0>	E47	DMI_RX_DN<0>	DMI_TX_DN<0>

53< OUT PD_CPU2_TEST<3..0>

3	PD_CPU2_TEST<3>	D4	TEST3
2	PD_CPU2_TEST<2>	F2	TEST2
1	PD_CPU2_TEST<1>	CW1	TEST1
0	PD_CPU2_TEST<0>	DB4	TEST0

53> IN A_CPU2_DDR23_RCOMP<2..0>

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1	A_CPU2_DDR23_RCOMP<1>	AC15	DDR23_RCOMP<1>
0	A_CPU2_DDR23_RCOMP<0>	U15	DDR23_RCOMP<0>

53> IN A_CPU2_DDR01_RCOMP<2..0>

2	A_CPU2_DDR01_RCOMP<2>	CB20	DDR01_RCOMP<2>
1	A_CPU2_DDR01_RCOMP<1>	CC19	DDR01_RCOMP<1>
0	A_CPU2_DDR01_RCOMP<0>	CA17	DDR01_RCOMP<0>

109> 78< 63> 40> OUT FM_CPU_ERR_N<2..0>

2	FM_CPU_ERR_N<2>	BC51	ERROR_N<2>
1	FM_CPU_ERR_N<1>	CB54	ERROR_N<1>
0	FM_CPU_ERR_N<0>	BD50	ERROR_N<0>

RSVD<45>	BJ45	NC_CPU2_RSVD<45>
RSVD<38>	BP44	NC_CPU2_RSVD<38>
RSVD<49>	BG45	NC_CPU2_RSVD<49>
RSVD<42>	BL45	NC_CPU2_RSVD<42>
RSVD<47>	BH46	NC_CPU2_RSVD<47>
RSVD<44>	BK44	NC_CPU2_RSVD<44>
RSVD<53>	BE45	NC_CPU2_RSVD<53>
RSVD<48>	BH44	NC_CPU2_RSVD<48>
RSVD<57>	BD44	NC_CPU2_RSVD<57>
RSVD<56>	BD46	NC_CPU2_RSVD<56>
RSVD<51>	BF46	NC_CPU2_RSVD<51>
RSVD<36>	BR43	NC_CPU2_RSVD<36>
RSVD<43>	BL43	NC_CPU2_RSVD<43>
RSVD<33>	BU43	NC_CPU2_RSVD<33>
RSVD<50>	BG43	NC_CPU2_RSVD<50>
RSVD<41>	BM44	NC_CPU2_RSVD<41>
RSVD<46>	BJ43	NC_CPU2_RSVD<46>
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RSVD<68>	AP48	NC_CPU2_RSVD<68>
RSVD<11>	E53	NC_CPU2_RSVD<11>
RSVD<34>	BT44	NC_CPU2_RSVD<34>
RSVD<52>	BE47	NC_CPU2_RSVD<52>
RSVD<0>	Y48	NC_CPU2_RSVD<0>
RSVD<2>	M48	NC_CPU2_RSVD<2>
RSVD<4>	J15	NC_CPU2_RSVD<4>
RSVD<6>	H56	NC_CPU2_RSVD<6>
RSVD<9>	F46	NC_CPU2_RSVD<9>
RSVD<27>	CG11	NC_CPU2_RSVD<27>
RSVD<28>	CF44	NC_CPU2_RSVD<28>
RSVD<29>	CE43	NC_CPU2_RSVD<29>
RSVD<30>	CD44	NC_CPU2_RSVD<30>
RSVD<1>	W15	NC_CPU2_RSVD<1>
RSVD<35>	BR47	NC_CPU2_RSVD<35>
RSVD<39>	BN47	NC_CPU2_RSVD<39>
RSVD<26>	CP54	NC_CPU2_RSVD<26>
RSVD<58>	BC47	NC_CPU2_RSVD<58>
RSVD<67>	AB48	NC_CPU2_RSVD<67>

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CPU SOCKET 2 (8 OF 13)

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DEPARTMENT: DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	SIZE: B	CODE: 34649	DOCUMENT NUMBER: 444359 — REV: 1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 86 OF 303

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NOTE: QPI P0 RX NETS WITH LANE REVERSAL

NOTE: POLARITY INVERSION ON LANES 0,1,2,3,5,8,10,11,12,13,14,15,16,17,18,19

U8C1
IC
SANDYBRIDGE_EP_EXT_D

65> IN QPI_CPU1_CPU2_P1P0_DP<19..0>
65> IN QPI_CPU1_CPU2_P1P0_DN<19..0>

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1	QPI_CPU1_CPU2_P1P0_DN<1>	BR49	QPI0_DRX_DP<18>	QPI0_DTX_DP<18>	CE51	QPI_CPU2_CPU1_P0P1_DP<18>	18		
2	QPI_CPU1_CPU2_P1P0_DN<2>	BG49	QPI0_DRX_DP<17>	QPI0_DTX_DP<17>	CD52	QPI_CPU2_CPU1_P0P1_DP<17>	17		
3	QPI_CPU1_CPU2_P1P0_DN<3>	BM50	QPI0_DRX_DP<16>	QPI0_DTX_DP<16>	CD50	QPI_CPU2_CPU1_P0P1_DP<16>	16		
4	QPI_CPU1_CPU2_P1P0_DP<4>	BN51	QPI0_DRX_DP<15>	QPI0_DTX_DP<15>	CD48	QPI_CPU2_CPU1_P0P1_DP<15>	15		
5	QPI_CPU1_CPU2_P1P0_DN<5>	BM52	QPI0_DRX_DP<14>	QPI0_DTX_DP<14>	CE47	QPI_CPU2_CPU1_P0P1_DP<14>	14		
6	QPI_CPU1_CPU2_P1P0_DP<6>	BL53	QPI0_DRX_DP<13>	QPI0_DTX_DP<13>	BY50	QPI_CPU2_CPU1_P0P1_DP<13>	13		
7	QPI_CPU1_CPU2_P1P0_DP<7>	BM54	QPI0_DRX_DP<12>	QPI0_DTX_DP<12>	BY48	QPI_CPU2_CPU1_P0P1_DP<12>	12		
8	QPI_CPU1_CPU2_P1P0_DN<8>	BL55	QPI0_DRX_DP<11>	QPI0_DTX_DP<11>	CA51	QPI_CPU2_CPU1_P0P1_DP<11>	11		
9	QPI_CPU1_CPU2_P1P0_DP<9>	BM56	QPI0_DRX_DP<10>	QPI0_DTX_DP<10>	CD46	QPI_CPU2_CPU1_P0P1_DP<10>	10		
10	QPI_CPU1_CPU2_P1P0_DN<10>	BL57	QPI0_DRX_DP<9>	QPI0_DTX_DP<9>	BV46	QPI_CPU2_CPU1_P0P1_DP<9>	9		
11	QPI_CPU1_CPU2_P1P0_DN<11>	BE57	QPI0_DRX_DP<8>	QPI0_DTX_DP<8>	BV56	QPI_CPU2_CPU1_P0P1_DP<8>	8		
12	QPI_CPU1_CPU2_P1P0_DN<12>	BD58	QPI0_DRX_DP<7>	QPI0_DTX_DP<7>	BU57	QPI_CPU2_CPU1_P0P1_DP<7>	7		
13	QPI_CPU1_CPU2_P1P0_DN<13>	BF50	QPI0_DRX_DP<6>	QPI0_DTX_DP<6>	BV48	QPI_CPU2_CPU1_P0P1_DP<6>	6		
14	QPI_CPU1_CPU2_P1P0_DN<14>	BF54	QPI0_DRX_DP<5>	QPI0_DTX_DP<5>	BT58	QPI_CPU2_CPU1_P0P1_DP<5>	5		
15	QPI_CPU1_CPU2_P1P0_DN<15>	BF56	QPI0_DRX_DP<4>	QPI0_DTX_DP<4>	BU55	QPI_CPU2_CPU1_P0P1_DP<4>	4		
16	QPI_CPU1_CPU2_P1P0_DN<16>	BE55	QPI0_DRX_DP<3>	QPI0_DTX_DP<3>	BV54	QPI_CPU2_CPU1_P0P1_DP<3>	3		
17	QPI_CPU1_CPU2_P1P0_DN<17>	BE53	QPI0_DRX_DP<2>	QPI0_DTX_DP<2>	BU53	QPI_CPU2_CPU1_P0P1_DP<2>	2		
18	QPI_CPU1_CPU2_P1P0_DN<18>	BF52	QPI0_DRX_DP<1>	QPI0_DTX_DP<1>	BV52	QPI_CPU2_CPU1_P0P1_DP<1>	1		
19	QPI_CPU1_CPU2_P1P0_DN<19>	BG51	QPI0_DRX_DP<0>	QPI0_DTX_DP<0>	BV50	QPI_CPU2_CPU1_P0P1_DP<0>	0		
0	QPI_CPU1_CPU2_P1P0_DP<0>	BM48	QPI0_DRX_DN<19>	QPI0_DTX_DN<19>	CG49	QPI_CPU2_CPU1_P0P1_DN<19>	19	QPI_CPU2_CPU1_P0P1_DN<19..0>	OUT 65<
1	QPI_CPU1_CPU2_P1P0_DP<1>	BN49	QPI0_DRX_DN<18>	QPI0_DTX_DN<18>	CG51	QPI_CPU2_CPU1_P0P1_DN<18>	18		
2	QPI_CPU1_CPU2_P1P0_DP<2>	BJ49	QPI0_DRX_DN<17>	QPI0_DTX_DN<17>	CF52	QPI_CPU2_CPU1_P0P1_DN<17>	17		
3	QPI_CPU1_CPU2_P1P0_DP<3>	BP50	QPI0_DRX_DN<16>	QPI0_DTX_DN<16>	CF50	QPI_CPU2_CPU1_P0P1_DN<16>	16		
4	QPI_CPU1_CPU2_P1P0_DN<4>	BR51	QPI0_DRX_DN<15>	QPI0_DTX_DN<15>	CF48	QPI_CPU2_CPU1_P0P1_DN<15>	15		
5	QPI_CPU1_CPU2_P1P0_DP<5>	BP52	QPI0_DRX_DN<14>	QPI0_DTX_DN<14>	CG47	QPI_CPU2_CPU1_P0P1_DN<14>	14		
6	QPI_CPU1_CPU2_P1P0_DN<6>	BN53	QPI0_DRX_DN<13>	QPI0_DTX_DN<13>	CA49	QPI_CPU2_CPU1_P0P1_DN<13>	13		
7	QPI_CPU1_CPU2_P1P0_DN<7>	BP54	QPI0_DRX_DN<12>	QPI0_DTX_DN<12>	CA47	QPI_CPU2_CPU1_P0P1_DN<12>	12		
8	QPI_CPU1_CPU2_P1P0_DP<8>	BN55	QPI0_DRX_DN<11>	QPI0_DTX_DN<11>	BY52	QPI_CPU2_CPU1_P0P1_DN<11>	11		
9	QPI_CPU1_CPU2_P1P0_DN<9>	BP56	QPI0_DRX_DN<10>	QPI0_DTX_DN<10>	CF46	QPI_CPU2_CPU1_P0P1_DN<10>	10		
10	QPI_CPU1_CPU2_P1P0_DP<10>	BN57	QPI0_DRX_DN<9>	QPI0_DTX_DN<9>	BW45	QPI_CPU2_CPU1_P0P1_DN<9>	9		
11	QPI_CPU1_CPU2_P1P0_DP<11>	BG57	QPI0_DRX_DN<8>	QPI0_DTX_DN<8>	BY56	QPI_CPU2_CPU1_P0P1_DN<8>	8		
12	QPI_CPU1_CPU2_P1P0_DP<12>	BF58	QPI0_DRX_DN<7>	QPI0_DTX_DN<7>	BW57	QPI_CPU2_CPU1_P0P1_DN<7>	7		
13	QPI_CPU1_CPU2_P1P0_DP<13>	BH50	QPI0_DRX_DN<6>	QPI0_DTX_DN<6>	BW47	QPI_CPU2_CPU1_P0P1_DN<6>	6		
14	QPI_CPU1_CPU2_P1P0_DP<14>	BH54	QPI0_DRX_DN<5>	QPI0_DTX_DN<5>	BV58	QPI_CPU2_CPU1_P0P1_DN<5>	5		
15	QPI_CPU1_CPU2_P1P0_DP<15>	BH56	QPI0_DRX_DN<4>	QPI0_DTX_DN<4>	BW55	QPI_CPU2_CPU1_P0P1_DN<4>	4		
16	QPI_CPU1_CPU2_P1P0_DP<16>	BG55	QPI0_DRX_DN<3>	QPI0_DTX_DN<3>	BY54	QPI_CPU2_CPU1_P0P1_DN<3>	3		
17	QPI_CPU1_CPU2_P1P0_DP<17>	BG53	QPI0_DRX_DN<2>	QPI0_DTX_DN<2>	BW53	QPI_CPU2_CPU1_P0P1_DN<2>	2		
18	QPI_CPU1_CPU2_P1P0_DP<18>	BH52	QPI0_DRX_DN<1>	QPI0_DTX_DN<1>	BW51	QPI_CPU2_CPU1_P0P1_DN<1>	1		
19	QPI_CPU1_CPU2_P1P0_DP<19>	BJ51	QPI0_DRX_DN<0>	QPI0_DTX_DN<0>	BW49	QPI_CPU2_CPU1_P0P1_DN<0>	0		
65> IN	QPI_CPU1_CPU2_P1P0_CLKA_DP	BK58	QPI0_CLKRX_DP	QPI0_CLKTX_DP	CE45	QPI_CPU2_CPU1_P0P1_CLKA_DP		OUT 65<	
65> IN	QPI_CPU1_CPU2_P1P0_CLKA_DN	BM58	QPI0_CLKRX_DN	QPI0_CLKTX_DN	CG45	QPI_CPU2_CPU1_P0P1_CLKA_DN		OUT 65<	

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CPU SOCKET 2 (9 OF 13)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 87 OF 303	

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NOTE: QPI P1 RX NETS WITH LANE REVERSAL

NOTE: POLARITY INVERSION ON LANES 4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19

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110> IN	QPI_CPU3_CPU2_P0P1_DP<19..0>								QPI_CPU2_CPU3_P1P0_DP<19..0>	OUT 110<
110> IN	QPI_CPU3_CPU2_P0P1_DN<19..0>								QPI_CPU2_CPU3_P1P0_DN<19..0>	OUT 110<
0	QPI_CPU3_CPU2_P0P1_DP<0>	CL45	QPI1_DRX_DP<19>	QPI1_DTX_DP<19>	DB42	QPI_CPU2_CPU3_P1P0_DP<19>	19			
1	QPI_CPU3_CPU2_P0P1_DP<1>	CK46	QPI1_DRX_DP<18>	QPI1_DTX_DP<18>	DE43	QPI_CPU2_CPU3_P1P0_DP<18>	18			
2	QPI_CPU3_CPU2_P0P1_DP<2>	CL47	QPI1_DRX_DP<17>	QPI1_DTX_DP<17>	CU43	QPI_CPU2_CPU3_P1P0_DP<17>	17			
3	QPI_CPU3_CPU2_P0P1_DP<3>	CK48	QPI1_DRX_DP<16>	QPI1_DTX_DP<16>	DB44	QPI_CPU2_CPU3_P1P0_DP<16>	16			
4	QPI_CPU3_CPU2_P0P1_DN<4>	CN49	QPI1_DRX_DP<15>	QPI1_DTX_DP<15>	DE45	QPI_CPU2_CPU3_P1P0_DP<15>	15			
5	QPI_CPU3_CPU2_P0P1_DN<5>	CM50	QPI1_DRX_DP<14>	QPI1_DTX_DP<14>	CT44	QPI_CPU2_CPU3_P1P0_DP<14>	14			
6	QPI_CPU3_CPU2_P0P1_DN<6>	CN51	QPI1_DRX_DP<13>	QPI1_DTX_DP<13>	DB46	QPI_CPU2_CPU3_P1P0_DP<13>	13			
7	QPI_CPU3_CPU2_P0P1_DN<7>	CV52	QPI1_DRX_DP<12>	QPI1_DTX_DP<12>	DE47	QPI_CPU2_CPU3_P1P0_DP<12>	12			
8	QPI_CPU3_CPU2_P0P1_DN<8>	CU53	QPI1_DRX_DP<11>	QPI1_DTX_DP<11>	CU45	QPI_CPU2_CPU3_P1P0_DP<11>	11			
9	QPI_CPU3_CPU2_P0P1_DN<9>	CK52	QPI1_DRX_DP<10>	QPI1_DTX_DP<10>	DB48	QPI_CPU2_CPU3_P1P0_DP<10>	10			
10	QPI_CPU3_CPU2_P0P1_DN<10>	CJ53	QPI1_DRX_DP<9>	QPI1_DTX_DP<9>	DC49	QPI_CPU2_CPU3_P1P0_DP<9>	9			
11	QPI_CPU3_CPU2_P0P1_DN<11>	CT56	QPI1_DRX_DP<8>	QPI1_DTX_DP<8>	CT46	QPI_CPU2_CPU3_P1P0_DP<8>	8			
12	QPI_CPU3_CPU2_P0P1_DN<12>	CR57	QPI1_DRX_DP<7>	QPI1_DTX_DP<7>	DD50	QPI_CPU2_CPU3_P1P0_DP<7>	7			
13	QPI_CPU3_CPU2_P0P1_DN<13>	CP58	QPI1_DRX_DP<6>	QPI1_DTX_DP<6>	DC51	QPI_CPU2_CPU3_P1P0_DP<6>	6			
14	QPI_CPU3_CPU2_P0P1_DN<14>	CK54	QPI1_DRX_DP<5>	QPI1_DTX_DP<5>	CU47	QPI_CPU2_CPU3_P1P0_DP<5>	5			
15	QPI_CPU3_CPU2_P0P1_DN<15>	CK56	QPI1_DRX_DP<4>	QPI1_DTX_DP<4>	DD52	QPI_CPU2_CPU3_P1P0_DP<4>	4			
16	QPI_CPU3_CPU2_P0P1_DN<16>	CJ55	QPI1_DRX_DP<3>	QPI1_DTX_DP<3>	DA53	QPI_CPU2_CPU3_P1P0_DP<3>	3			
17	QPI_CPU3_CPU2_P0P1_DN<17>	CD54	QPI1_DRX_DP<2>	QPI1_DTX_DP<2>	CU49	QPI_CPU2_CPU3_P1P0_DP<2>	2			
18	QPI_CPU3_CPU2_P0P1_DN<18>	CD56	QPI1_DRX_DP<1>	QPI1_DTX_DP<1>	CT50	QPI_CPU2_CPU3_P1P0_DP<1>	1			
19	QPI_CPU3_CPU2_P0P1_DN<19>	CC55	QPI1_DRX_DP<0>	QPI1_DTX_DP<0>	CT48	QPI_CPU2_CPU3_P1P0_DP<0>	0			
0	QPI_CPU3_CPU2_P0P1_DN<0>	CN45	QPI1_DRX_DN<19>	QPI1_DTX_DN<19>	DD42	QPI_CPU2_CPU3_P1P0_DN<19>	19			
1	QPI_CPU3_CPU2_P0P1_DN<1>	CM46	QPI1_DRX_DN<18>	QPI1_DTX_DN<18>	DC43	QPI_CPU2_CPU3_P1P0_DN<18>	18			
2	QPI_CPU3_CPU2_P0P1_DN<2>	CN47	QPI1_DRX_DN<17>	QPI1_DTX_DN<17>	CW43	QPI_CPU2_CPU3_P1P0_DN<17>	17			
3	QPI_CPU3_CPU2_P0P1_DN<3>	CM48	QPI1_DRX_DN<16>	QPI1_DTX_DN<16>	DD44	QPI_CPU2_CPU3_P1P0_DN<16>	16			
4	QPI_CPU3_CPU2_P0P1_DP<4>	CL49	QPI1_DRX_DN<15>	QPI1_DTX_DN<15>	DC45	QPI_CPU2_CPU3_P1P0_DN<15>	15			
5	QPI_CPU3_CPU2_P0P1_DP<5>	CK50	QPI1_DRX_DN<14>	QPI1_DTX_DN<14>	CV44	QPI_CPU2_CPU3_P1P0_DN<14>	14			
6	QPI_CPU3_CPU2_P0P1_DP<6>	CL51	QPI1_DRX_DN<13>	QPI1_DTX_DN<13>	DD46	QPI_CPU2_CPU3_P1P0_DN<13>	13			
7	QPI_CPU3_CPU2_P0P1_DP<7>	CT52	QPI1_DRX_DN<12>	QPI1_DTX_DN<12>	DC47	QPI_CPU2_CPU3_P1P0_DN<12>	12			
8	QPI_CPU3_CPU2_P0P1_DP<8>	CR53	QPI1_DRX_DN<11>	QPI1_DTX_DN<11>	CW45	QPI_CPU2_CPU3_P1P0_DN<11>	11			
9	QPI_CPU3_CPU2_P0P1_DP<9>	CM52	QPI1_DRX_DN<10>	QPI1_DTX_DN<10>	DD48	QPI_CPU2_CPU3_P1P0_DN<10>	10			
10	QPI_CPU3_CPU2_P0P1_DP<10>	CL53	QPI1_DRX_DN<9>	QPI1_DTX_DN<9>	DE49	QPI_CPU2_CPU3_P1P0_DN<9>	9			
11	QPI_CPU3_CPU2_P0P1_DP<11>	CV56	QPI1_DRX_DN<8>	QPI1_DTX_DN<8>	CV46	QPI_CPU2_CPU3_P1P0_DN<8>	8			
12	QPI_CPU3_CPU2_P0P1_DP<12>	CU57	QPI1_DRX_DN<7>	QPI1_DTX_DN<7>	DB50	QPI_CPU2_CPU3_P1P0_DN<7>	7			
13	QPI_CPU3_CPU2_P0P1_DP<13>	CT58	QPI1_DRX_DN<6>	QPI1_DTX_DN<6>	DE51	QPI_CPU2_CPU3_P1P0_DN<6>	6			
14	QPI_CPU3_CPU2_P0P1_DP<14>	CM54	QPI1_DRX_DN<5>	QPI1_DTX_DN<5>	CW47	QPI_CPU2_CPU3_P1P0_DN<5>	5			
15	QPI_CPU3_CPU2_P0P1_DP<15>	CM56	QPI1_DRX_DN<4>	QPI1_DTX_DN<4>	DB52	QPI_CPU2_CPU3_P1P0_DN<4>	4			
16	QPI_CPU3_CPU2_P0P1_DP<16>	CL55	QPI1_DRX_DN<3>	QPI1_DTX_DN<3>	DC53	QPI_CPU2_CPU3_P1P0_DN<3>	3			
17	QPI_CPU3_CPU2_P0P1_DP<17>	CF54	QPI1_DRX_DN<2>	QPI1_DTX_DN<2>	CW49	QPI_CPU2_CPU3_P1P0_DN<2>	2			
18	QPI_CPU3_CPU2_P0P1_DP<18>	CF56	QPI1_DRX_DN<1>	QPI1_DTX_DN<1>	CV50	QPI_CPU2_CPU3_P1P0_DN<1>	1			
19	QPI_CPU3_CPU2_P0P1_DP<19>	CE55	QPI1_DRX_DN<0>	QPI1_DTX_DN<0>	CV48	QPI_CPU2_CPU3_P1P0_DN<0>	0			
110> IN	QPI_CPU3_CPU2_P0P1_CLKA_DP	CR55	QPI1_CLKRX_DP	QPI1_CLKTX_DP	DB54	QPI_CPU2_CPU3_P1P0_CLKA_DP				
110> IN	QPI_CPU3_CPU2_P0P1_CLKA_DN	CU55	QPI1_CLKRX_DN	QPI1_CLKTX_DN	CY54	QPI_CPU2_CPU3_P1P0_CLKA_DN				

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CPU SOCKET 2 (10 OF 13)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 88 OF 303	

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P1V05_VCCP_CPU2

1.05

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CA29	VCC<207>		VCC<155>	BP10	
CA25	VCC<206>		VCC<154>	BN9	
BY40	VCC<205>		VCC<153>	BN7	
BY38	VCC<204>		VCC<152>	BN5	
BY36	VCC<203>		VCC<151>	BN3	
BY34	VCC<202>		VCC<150>	BN17	
BY32	VCC<201>		VCC<149>	BN15	
BY30	VCC<200>		VCC<148>	BN13	
BY28	VCC<199>		VCC<147>	BN11	
BY26	VCC<198>		VCC<146>	BN1	
BY18	VCC<197>		VCC<145>	BK8	
BV8	VCC<196>		VCC<144>	BK6	
BV6	VCC<195>		VCC<143>	BK4	
BV4	VCC<194>		VCC<142>	BK2	
BV2	VCC<193>		VCC<141>	BK16	
BV16	VCC<192>		VCC<140>	BK14	
BV14	VCC<191>		VCC<139>	BK12	
BV12	VCC<190>		VCC<138>	BK10	
BV10	VCC<189>		VCC<137>	BJ9	
BU9	VCC<188>		VCC<136>	BJ7	
BU7	VCC<187>		VCC<135>	BJ5	
BU5	VCC<186>		VCC<134>	BJ3	
BU3	VCC<185>		VCC<133>	BJ17	
BU17	VCC<184>		VCC<132>	BJ15	
BU15	VCC<183>		VCC<131>	BJ13	
BU13	VCC<182>		VCC<130>	BJ11	
BU11	VCC<181>		VCC<129>	BJ1	
BU1	VCC<180>		VCC<128>	BH8	
BT8	VCC<179>		VCC<127>	BH6	
BT6	VCC<178>		VCC<126>	BH4	
BT4	VCC<177>		VCC<125>	BH2	
BT2	VCC<176>		VCC<124>	BH16	
BT16	VCC<175>		VCC<123>	BH14	
BT14	VCC<174>		VCC<122>	BH12	
BT12	VCC<173>		VCC<121>	BH10	
BT10	VCC<172>		VCC<120>	BG9	
BR9	VCC<171>		VCC<119>	BG7	
BR7	VCC<170>		VCC<118>	BG5	
BR5	VCC<169>		VCC<117>	BG3	
BR3	VCC<168>		VCC<116>	BG17	
BR17	VCC<167>		VCC<115>	BG15	
BR15	VCC<166>		VCC<114>	BG13	
BR13	VCC<165>		VCC<113>	BG11	
BR11	VCC<164>		VCC<112>	BG1	
BR1	VCC<163>		VCC<111>	BF8	
BP8	VCC<162>		VCC<110>	BF6	
BP6	VCC<161>		VCC<109>	BF4	
BP4	VCC<160>		VCC<108>	BF2	
BP2	VCC<159>		VCC<107>	BF16	
BP16	VCC<158>		VCC<106>	BF14	
BP14	VCC<157>		VCC<105>	BF12	
BP12	VCC<156>		VCC<104>	BF10	

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P1V05_VCCP_CPU2

1.05

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BE9	VCC<103>		VCC<51>	AU7	
BE7	VCC<102>		VCC<50>	AU5	
BE5	VCC<101>		VCC<49>	AU3	
BE3	VCC<100>		VCC<48>	AU17	
BE17	VCC<99>		VCC<47>	AU15	
BE15	VCC<98>		VCC<46>	AU13	
BE13	VCC<97>		VCC<45>	AU11	
BE11	VCC<96>		VCC<44>	AU1	
BE1	VCC<95>		VCC<43>	AP8	
BB8	VCC<94>		VCC<42>	AP6	
BB6	VCC<93>		VCC<41>	AP4	
BB4	VCC<92>		VCC<40>	AP2	
BB2	VCC<91>		VCC<39>	AP16	
BB16	VCC<90>		VCC<38>	AP14	
BB14	VCC<89>		VCC<37>	AP12	
BB12	VCC<88>		VCC<36>	AP10	
BB10	VCC<87>		VCC<35>	AN9	
BA9	VCC<86>		VCC<34>	AN7	
BA7	VCC<85>		VCC<33>	AN5	
BA5	VCC<84>		VCC<32>	AN3	
BA3	VCC<83>		VCC<31>	AN17	
BA17	VCC<82>		VCC<30>	AN15	
BA15	VCC<81>		VCC<29>	AN13	
BA13	VCC<80>		VCC<28>	AN11	
BA11	VCC<79>		VCC<27>	AN1	
BA1	VCC<78>		VCC<26>	AM8	
AY8	VCC<77>		VCC<25>	AM6	
AY6	VCC<76>		VCC<24>	AM4	
AY4	VCC<75>		VCC<23>	AM2	
AY2	VCC<74>		VCC<22>	AM16	
AY16	VCC<73>		VCC<21>	AM14	
AY14	VCC<72>		VCC<20>	AM12	
AY12	VCC<71>		VCC<19>	AM10	
AY10	VCC<70>		VCC<18>	AL9	
AW9	VCC<69>		VCC<17>	AL7	
AW7	VCC<68>		VCC<16>	AL5	
AW5	VCC<67>		VCC<15>	AL3	
AW3	VCC<66>		VCC<14>	AL17	
AW17	VCC<65>		VCC<13>	AL15	
AW15	VCC<64>		VCC<12>	AL13	
AW13	VCC<63>		VCC<11>	AL11	
AW11	VCC<62>		VCC<10>	AL1	
AW1	VCC<61>		VCC<9>	AG41	
AV8	VCC<60>		VCC<8>	AG39	
AV6	VCC<59>		VCC<7>	AG37	
AV4	VCC<58>		VCC<6>	AG35	
AV2	VCC<57>		VCC<5>	AG33	
AV16	VCC<56>		VCC<4>	AG31	
AV14	VCC<55>		VCC<3>	AG29	
AV12	VCC<54>		VCC<2>	AG27	
AV10	VCC<53>		VCC<1>	AG25	
AU9	VCC<52>		VCC<0>	AG19	

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CPU SOCKET 2 (11 OF 13)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 89 OF 303	

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P1V05_VTT_CPU2 1.05
P1V5_DDR3_CPU2 1.5
P1V5_DDR3_CPU2 1.5
P1V05_VTT_CPU2 1.05

DA49 CR51 CR45 CJ49 CG55 CC45 CA53 → VTTA<2> VTTA<3> VTTA<4> VTTA<5> VTTA<6> VTTA<7> VTTA<8>
BV42 → VTTD<4>

V24 V22 V20 V18 V16 N23 N21 N19 N17 N15 H24 H22 H20 H18 H16 G13 C23 C21 C19 C17 C15 → VCCD_23<5> VCCD_23<6> VCCD_23<7> VCCD_23<8> VCCD_23<9> VCCD_23<10> VCCD_23<11> VCCD_23<12> VCCD_23<13> VCCD_23<14> VCCD_23<15> VCCD_23<16> VCCD_23<17> VCCD_23<18> VCCD_23<19> VCCD_23<20> VCCD_23<21> VCCD_23<22> VCCD_23<23> VCCD_23<24> VCCD_23<25>
AC25 AC23 AC21 AC19 AC17 → VCCD_23<0> VCCD_23<1> VCCD_23<2> VCCD_23<3> VCCD_23<4>

DD26 DD24 DD22 DD20 DD18 CW27 CW25 CW23 CW21 CW19 CP28 CP26 CP24 CP22 CP20 CJ27 CJ25 CJ23 CJ21 CJ19 CD28 CD26 CD24 CD22 CD20 → VCCD_01<0> VCCD_01<1> VCCD_01<2> VCCD_01<3> VCCD_01<4> VCCD_01<5> VCCD_01<6> VCCD_01<7> VCCD_01<8> VCCD_01<9> VCCD_01<10> VCCD_01<11> VCCD_01<12> VCCD_01<13> VCCD_01<14> VCCD_01<15> VCCD_01<16> VCCD_01<17> VCCD_01<18> VCCD_01<19> VCCD_01<20> VCCD_01<21> VCCD_01<22> VCCD_01<23> VCCD_01<24>

VCC_SENSE
RSVD<20>
VSS_VCC_SENSE
VTTD_SENSE
VSS_VTTD_SENSE

VCCPLL<1>
VCCPLL<2>
VCCPLL<0>

VSS_VSA_SENSE
VSA_SENSE

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VTTD<0> VTTD<1> VTTD<2> VTTD<3> VTTD<5> VTTD<6> VTTD<9> VTTD<7> VTTD<10> VTTD<11> VTTD<12> VTTD<13> VTTD<14> VTTD<15> VTTD<16> VTTD<17> VTTD<18> VTTD<8>

BW3 VSENSE_DIE_CPU2_VCCP_P → OUT 246<
DB56 NC_CPU2_RSVD<20>
BY2 VSENSE_DIE_CPU2_VCCP_N → OUT 246<
BP42 VSENSE_DIE_CPU2_VTT_P → OUT 271>
BT42 VSENSE_DIE_CPU2_VTT_N → OUT 271>

P1V8_PLL_CPU2 1.8
CA13 BY14 CA15

AF14 VSENSE_DIE_VSA2_N → OUT 247<
AG13 VSENSE_DIE_VSA2_P → OUT 247<

P0V85_VSA_CPU2 0.85
N51 N45 G49 G43 B54 AJ9 AJ7 AJ5 AJ3 AJ13 AJ11 AJ1 AH8 AH6 AH4 AH2 AH16 AH14 AH12 AH10 AG17 AG15 AF18 AE17 AE15

P1V05_VTT_CPU2 1.05
Y54 W49 AU53 AM54 AM48 AE53 AE45

P1V05_VTT_CPU2 1.05
CA23 CA21 BY22 BY20 BU47 BR55 BK56 BM42 BH42 BD42 AY42 AT42 AM42 AG23 AG21 AF24 AF22 BL51

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CY40 AW55 AG43 CW51 C3 D2 DB2 DC3 E1 V46 BG47 BK50 AU51 Y56 Y42 Y40 Y38 Y36 Y32 Y30 Y28 Y12 Y10 W9 W53 W51 W5 W47 W45 W43 W41 W37 W33 W13 V8 V50 V48 V44 V42 V36 V34 V28 V26 U5 U35 T8 T6 T42 T4 T28 R7 R55 R5 R39 R35 R31 R3 R29 R11 P8 P56 P54 P40 P38 P32 P30 P26 P14 P12 P10 → VSS<547> VSS<546> VSS<545> VSS<544> VSS<543> VSS<542> VSS<541> VSS<540> VSS<539> VSS<538> VSS<537> VSS<536> VSS<535> VSS<534> VSS<533> VSS<532> VSS<531> VSS<530> VSS<529> VSS<528> VSS<527> VSS<526> VSS<525> VSS<524> VSS<523> VSS<522> VSS<521> VSS<520> VSS<519> VSS<518> VSS<517> VSS<516> VSS<515> VSS<514> VSS<513> VSS<512> VSS<511> VSS<510> VSS<509> VSS<508> VSS<507> VSS<506> VSS<505> VSS<504> VSS<503> VSS<502> VSS<501> VSS<500> VSS<499> VSS<498> VSS<497> VSS<496> VSS<495> VSS<494> VSS<493> VSS<492> VSS<491> VSS<490> VSS<489> VSS<488> VSS<487> VSS<486> VSS<485> VSS<484> VSS<483> VSS<482> VSS<481> VSS<480> VSS<479> VSS<478>

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N9 N53 N5 N49 N47 N43 N41 N37 N35 N33 N13 M8 M52 M50 M46 M44 M42 M36 M34 L5 L41 L29 L25 K8 K34 K30 K28 K2 J55 J5 J41 J39 J33 J31 J27 J11 H8 H54 H52 H40 H38 H34 H32 K26 H14 H12 H10 G9 G57 G53 G51 G5 G47 G45 G41 G37 G35 G31 G1 F8 F50 F48 F44 F42 F36 G25 E5 E41

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P1V05_VTT_CPU2 1.05

SOCKET2	SOCKET2	SOCKET2	SOCKET2	SOCKET2	SOCKET2	SOCKET2	SOCKET2	SOCKET2	SOCKET2	SOCKET2	SOCKET2	SOCKET2	SOCKET2
C8D28	C8D29	C8D3	C8D30	C2P1	C2P3	C2P28	C2P29	C2P30	C8D1				
22UF	22UF	22UF	22UF	22UF	22UF	22UF	22UF	22UF	22UF				
4V	4V	4V	4V	4V	4V	4V	4V	4V	4V				
20%	20%	20%	20%	20%	20%	20%	20%	20%	20%				
C95333-002	C95333-002	C95333-002	C95333-002	C95333-002	C95333-002	C95333-002	C95333-002	C95333-002	C95333-002				
0805LF	0805LF	0805LF	0805LF	0805LF	0805LF	0805LF	0805LF	0805LF	0805LF				

CAD NOTE:
PLACE IN SOCKET CAVITY

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CPU SOCKET 2 (12 OF 13)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 90 OF 303	

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E31	VSS<409>	VSS<341>	CV34
E3	VSS<408>	VSS<340>	CV32
E29	VSS<407>	VSS<339>	CV30
DF8	VSS<406>	VSS<338>	CV18
DF52	VSS<405>	VSS<337>	CV14
DF50	VSS<404>	VSS<336>	CU5
DF48	VSS<403>	VSS<335>	CU35
DF46	VSS<402>	VSS<334>	CU3
DF44	VSS<401>	VSS<333>	CU11
DF42	VSS<400>	VSS<332>	CU1
DF36	VSS<399>	VSS<331>	CT42
DF12	VSS<398>	VSS<330>	CT28
DE7	VSS<397>	VSS<329>	CR9
DE53	VSS<396>	VSS<328>	CR5
DE41	VSS<395>	VSS<327>	CR49
DE17	VSS<394>	VSS<326>	CR47
DD6	VSS<393>	VSS<325>	CR35
DD38	VSS<392>	VSS<324>	CR11
DD36	VSS<391>	VSS<323>	CP56
DD34	VSS<390>	VSS<322>	CP52
DD14	VSS<389>	VSS<321>	CP48
DD12	VSS<388>	VSS<320>	CP46
DD10	VSS<387>	VSS<319>	CP44
DC5	VSS<386>	VSS<318>	CP40
DC41	VSS<385>	VSS<317>	CP36
DB58	VSS<384>	VSS<316>	CP16
		VSS<315>	CP12
DB36	VSS<383>	VSS<314>	CN9
DB32	VSS<382>	VSS<313>	CN7
DB12	VSS<381>	VSS<312>	CN57
DA9	VSS<380>	VSS<311>	CN55
DA51	VSS<379>	VSS<310>	CN53
DA5	VSS<378>	VSS<309>	CN5
DA47	VSS<377>	VSS<308>	CP42
DA45	VSS<376>	VSS<307>	CN39
DA43	VSS<375>	VSS<306>	CN37
DA41	VSS<374>	VSS<305>	CN35
DA3	VSS<373>	VSS<304>	CN33
DA11	VSS<372>	VSS<303>	CN31
D8	VSS<371>	VSS<302>	CN3
D36	VSS<370>	VSS<301>	CN17
D26	VSS<369>	VSS<300>	CN15
CY8	VSS<368>	VSS<299>	CN13
CY50	VSS<367>	VSS<298>	CN11
CY44	VSS<366>	VSS<297>	CM8
CY36	VSS<365>	VSS<296>	CM6
CY2	VSS<364>	VSS<295>	CM42
CY16	VSS<363>	VSS<294>	CM40
CY12	VSS<362>	VSS<293>	CM38
CY10	VSS<361>	VSS<292>	CM36
CW7	VSS<360>	VSS<291>	CM34
CW57	VSS<359>	VSS<290>	CM32
CW55	VSS<358>	VSS<289>	CM30
CW53	VSS<357>	VSS<288>	CM14
CW5	VSS<356>	VSS<287>	CM10
CW39	VSS<355>	VSS<286>	CL5
CW37	VSS<354>	VSS<285>	CL43
CW35	VSS<353>	VSS<284>	CL17
CW33	VSS<352>	VSS<283>	CK6
CW31	VSS<351>	VSS<282>	CK4
CW29	VSS<350>	VSS<281>	CK36
CW15	VSS<349>	VSS<280>	CK10
CW13	VSS<348>	VSS<279>	CJ9
CW11	VSS<347>	VSS<278>	CJ51
CV6	VSS<346>	VSS<277>	CJ47
CV58	VSS<345>	VSS<276>	CJ45
CV54	VSS<344>	VSS<275>	CJ43
CV42	VSS<343>	VSS<274>	CJ3
CV38	VSS<342>		

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CJ29	VSS<273>	VSS<205>	C55
CJ17	VSS<272>	VSS<204>	C5
CJ11	VSS<271>	VSS<203>	C41
CH6	VSS<270>	VSS<202>	C39
CP50	VSS<269>	VSS<201>	C33
CH54	VSS<268>	VSS<200>	C13
CH52	VSS<267>	VSS<199>	C11
CH50	VSS<266>	VSS<198>	BY8
CH48	VSS<265>	VSS<197>	BY58
CH46	VSS<264>	VSS<196>	BY42
CH44	VSS<263>	VSS<195>	BY4
CH36	VSS<262>	VSS<194>	BY24
CH16	VSS<261>	VSS<193>	BW7
CH12	VSS<260>	VSS<192>	BW5
CG9	VSS<259>	VSS<191>	BW17
CG53	VSS<258>	VSS<190>	BW15
CG43	VSS<257>	VSS<189>	BW13
CG41	VSS<256>	VSS<188>	BW11
CG39	VSS<255>	VSS<187>	BW1
CG37	VSS<254>	VSS<186>	BU51
CG35	VSS<253>	VSS<185>	BU45
CG33	VSS<252>	VSS<184>	BT56
CG31	VSS<251>	VSS<183>	BT54
CG15	VSS<250>	VSS<182>	BT52
CF6	VSS<249>	VSS<181>	BT50
CF42	VSS<248>	VSS<180>	BT48
CF40	VSS<247>	VSS<179>	BT46
CF38	VSS<246>	VSS<178>	B52
CF36	VSS<245>	VSS<177>	BR57
CF34	VSS<244>	VSS<176>	BR53
CF32	VSS<243>	VSS<175>	BP58
CF30	VSS<242>	VSS<174>	BN45
CF14	VSS<241>	VSS<173>	BN43
CF12	VSS<240>	VSS<172>	BM8
CE9	VSS<239>	VSS<171>	BM6
CE5	VSS<238>	VSS<170>	BK42
CE13	VSS<237>	VSS<169>	BM4
CD6	VSS<236>	VSS<168>	BM2
CD36	VSS<235>	VSS<167>	BM16
CD18	VSS<234>	VSS<166>	BM14
CC9	VSS<233>	VSS<165>	BM12
CC49	VSS<232>	VSS<164>	BM10
CC47	VSS<231>	VSS<163>	BL9
CC43	VSS<230>	VSS<162>	BL7
CC3	VSS<229>	VSS<161>	BL5
CC29	VSS<228>	VSS<160>	BL49
CC13	VSS<227>	VSS<159>	BK48
CB8	VSS<226>	VSS<158>	BL3
CB6	VSS<225>	VSS<157>	BL17
CB56	VSS<224>	VSS<156>	BL15
CB52	VSS<223>	VSS<155>	BL13
CB50	VSS<222>	VSS<154>	BL11
CB48	VSS<221>	VSS<153>	BL1
CB46	VSS<220>	VSS<152>	BK54
CB36	VSS<219>	VSS<151>	BK52
CB16	VSS<218>	VSS<150>	BK46
CA57	VSS<217>	VSS<149>	BJ57
CA55	VSS<216>	VSS<148>	BJ55
CA5	VSS<215>	VSS<147>	BH58
CA41	VSS<214>	VSS<146>	BF44
CA39	VSS<213>	VSS<145>	BF42
CA37	VSS<212>	VSS<144>	BE51
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CA33	VSS<210>	VSS<142>	BD8
CA31	VSS<209>	VSS<141>	BD6
CA27	VSS<208>	VSS<140>	BD56
CA19	VSS<207>	VSS<139>	BD54
CA11	VSS<206>	VSS<138>	BD4
		VSS<137>	BD2

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BD16	VSS<136>	VSS<68>	AK46
BD14	VSS<135>	VSS<67>	AK44
BD12	VSS<134>	VSS<66>	AK42
BD10	VSS<133>	VSS<65>	AK4
BC9	VSS<132>	VSS<64>	AK2
BC7	VSS<131>	VSS<63>	AK16
BC57	VSS<130>	VSS<62>	AK14
BC55	VSS<129>	VSS<61>	AK12
BC53	VSS<128>	VSS<60>	AK10
BC5	VSS<127>	VSS<59>	AJ17
BC45	VSS<126>	VSS<58>	AJ15
BC43	VSS<125>	VSS<57>	AH58
BC3	VSS<124>	VSS<56>	AG9
BC17	VSS<123>	VSS<55>	AG57
BC15	VSS<122>	VSS<54>	AG55
BC13	VSS<121>	VSS<53>	AG5
BC11	VSS<120>	VSS<52>	AG3
BC1	VSS<119>	VSS<51>	AG1
BB58	VSS<118>	VSS<50>	AF6
BB52	VSS<117>	VSS<49>	AF56
BB50	VSS<116>	VSS<48>	AF54
BB48	VSS<115>	VSS<47>	AF42
BB46	VSS<114>	VSS<46>	AF40
BB42	VSS<113>	VSS<45>	AF36
B8	VSS<112>	VSS<44>	AF34
B6	VSS<111>	VSS<43>	AF26
B36	VSS<110>	VSS<42>	AF20
AW57	VSS<109>	VSS<41>	AF16
AV56	VSS<108>	VSS<40>	AF12
AV54	VSS<107>	VSS<39>	AE9
AV42	VSS<106>	VSS<38>	AE51
AU49	VSS<105>	VSS<37>	AE49
AU47	VSS<104>	VSS<36>	AE47
AU45	VSS<103>	VSS<35>	AE43
AT8	VSS<102>	VSS<34>	AE39
AT6	VSS<101>	VSS<33>	AE31
AT52	VSS<100>	VSS<32>	AE29
AT46	VSS<99>	VSS<31>	AD6
AT4	VSS<98>	VSS<30>	AD52
AT2	VSS<97>	VSS<29>	AD50
AT16	VSS<96>	VSS<28>	AD48
AT14	VSS<95>	VSS<27>	AD46
AT12	VSS<94>	VSS<26>	AD44
AT10	VSS<93>	VSS<25>	AD42
AR9	VSS<92>	VSS<24>	AD36
AR7	VSS<91>	VSS<23>	AD34
AR5	VSS<90>	VSS<22>	AD26
AR3	VSS<89>	VSS<21>	AC9
AR17	VSS<88>	VSS<20>	AC31
AR15	VSS<87>	VSS<19>	AB6
AR13	VSS<86>	VSS<18>	AB42
AR11	VSS<85>	VSS<17>	AB36
AR1	VSS<84>	VSS<16>	AB14
AP58	VSS<83>	VSS<15>	AA9
AP44	VSS<82>	VSS<14>	AA55
AP42	VSS<81>	VSS<13>	AA5
AN57	VSS<80>	VSS<12>	AA39
AN55	VSS<79>	VSS<11>	AA31
AM56	VSS<78>	VSS<10>	AA3
AL53	VSS<77>	VSS<9>	AA29
AL51	VSS<76>	VSS<8>	AA11
AL49	VSS<75>	VSS<7>	A7
AL45	VSS<74>	VSS<6>	A51
AL43	VSS<73>	VSS<5>	A5
AK8	VSS<72>	VSS<4>	A49
AK6	VSS<71>	VSS<3>	A47
AK50	VSS<70>	VSS<2>	A45
AK48	VSS<69>	VSS<1>	A43
		VSS<0>	A41

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CPU SOCKET 2 (13 OF 13)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 91 OF 303	

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CONN240_E55582004

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		15 171	A<15>	DQ<62>	233 62
		14 172	A<14>	DQ<61>	228 61
		13 196	A<13>	DQ<60>	227 60
		12 174	A<12>	DQ<59>	115 59
		11 55	A<11>	DQ<58>	114 58
		10 70	A<10>	DQ<57>	109 57
		9 175	A<9>	DQ<56>	108 56
		8 177	A<8>	DQ<55>	225 55
		7 56	A<7>	DQ<54>	224 54
		6 178	A<6>	DQ<53>	219 53
		5 58	A<5>	DQ<52>	218 52
		4 59	A<4>	DQ<51>	106 51
		3 180	A<3>	DQ<50>	105 50
		2 61	A<2>	DQ<49>	100 49
		1 181	A<1>	DQ<48>	99 48
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80> IN	M_J_BA<1..0>			DQ<46>	215 46
		1 190	BA<1>	DQ<45>	210 45
		0 71	BA<0>	DQ<44>	209 44
				DQ<43>	97 43
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80> IN	M_J_CK_DN<2>	64	NC_CK1N	DQ<41>	91 41
80> IN	M_J_CK_DP<0>	184	CK0P	DQ<40>	90 40
80> IN	M_J_CK_DN<0>	185	CK0N	DQ<39>	207 39
80> IN	M_J_CS_N<3..0>			DQ<38>	206 38
		3 198	CS<3>	DQ<37>	201 37
		2 79	CS<2>	DQ<36>	200 36
		1 76	CS<1>	DQ<35>	88 35
		0 193	CS<0>	DQ<34>	87 34
				DQ<33>	82 33
80> IN	M_J_CKE<1>	169	CKE<1>	DQ<32>	81 32
80> IN	M_J_CKE<0>	50	CKE<0>	DQ<31>	156 31
				DQ<30>	155 30
80> IN	M_J_WE_N	73	WE_N	DQ<29>	150 29
80> IN	M_J_RAS_N	192	RAS_N	DQ<28>	149 28
80> IN	M_J_CAS_N	74	CAS_N	DQ<27>	37 27
80> IN	M_J_ODT<1..0>			DQ<26>	36 26
		1 77	ODT<1>	DQ<25>	31 25
		0 195	ODT<0>	DQ<24>	30 24
				DQ<23>	147 23
80> IN	M_J_MA_PAR	68	PAR_IN_NC	DQ<22>	146 22
80< OUT	M_J_PAR_ERR_N<0>	53	ERR_OUT_NC	DQ<21>	141 21
80<> BI	M_J_ECC<7..0>			DQ<20>	140 20
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		6 164	CB<6>	DQ<18>	27 18
		5 159	CB<5>	DQ<17>	22 17
		4 158	CB<4>	DQ<16>	21 16
		3 46	CB<3>	DQ<15>	138 15
		2 45	CB<2>	DQ<14>	137 14
		1 40	CB<1>	DQ<13>	132 13
		0 39	CB<0>	DQ<12>	131 12
				DQ<11>	19 11
93< 79> IN	M_JK_RESET_LVC1V5_N	168	RESET_N	DQ<10>	18 10
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M_J_DQ<63..0> BI 80<>

SPD ADDRESS = 0XA0

P3V3 3.3

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E55582-004

J7B1

CONN240_E55582004

2	VSS<58>	VDD<21>	51
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11	VSS<55>	VDD<18>	60
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20	VSS<52>	VDD<15>	66
23	VSS<51>	VDD<14>	69
26	VSS<50>	VDD<13>	72
29	VSS<49>	VDD<12>	75
32	VSS<48>	VDD<11>	78
35	VSS<47>	VDD<10>	170
38	VSS<46>	VDD<9>	173
41	VSS<45>	VDD<8>	176
44	VSS<44>	VDD<7>	179
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80	VSS<42>	VDD<5>	183
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86	VSS<40>	VDD<3>	189
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92	VSS<38>	VDD<1>	194
95	VSS<37>	VDD<0>	197
98	VSS<36>		
101	VSS<35>	VTT<3>	49
104	VSS<34>	VTT<2>	48
107	VSS<33>	VTT<1>	120
110	VSS<32>	VTT<0>	240
113	VSS<31>		
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P1V5_DDR3_CPU2 1.5

P0V75_VTT_DDR3_CPU2 0.75

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E55582-004

P1V5_DDR3_CPU2

C7D1 10UF 6.3V 20% 602433-075 0603LF

C7C10 10UF 6.3V 20% 602433-075 0603LF

J7B1

CONN240_E55582004

	DQS17P_DM8	161	17	M_J_DQS_DP<17..0>	BI 80<>
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	DQS16P_DM7	230	16		
	DQS16N_NC	231	16		
	DQS15P_DM6	221	15		
	DQS15N_NC	222	15		
	DQS14P_DM5	212	14		
	DQS14N_NC	213	14		
	DQS13P_DM4	203	13		
	DQS13N_NC	204	13		
	DQS12P_DM3	152	12		
	DQS12N_NC	153	12		
	DQS11P_DM2	143	11		
	DQS11N_NC	144	11		
	DQS10P_DM1	134	10		
	DQS10N_NC	135	10		
	DQS9P_DM0	125	9		
	DQS9N_NC	126	9		
	DQS8P	43	8		
	DQS8N	42	8		
	DQS7P	112	7		
	DQS7N	111	7		
	DQS6P	103	6		
	DQS6N	102	6		
	DQS5P	94	5		
	DQS5N	93	5		
	DQS4P	85	4		
	DQS4N	84	4		
	DQS3P	34	3		
	DQS3N	33	3		
	DQS2P	25	2		
	DQS2N	24	2		
	DQS1P	16	1		
	DQS1N	15	1		
	DQS0P	7	0		
	DQS0N	6	0		

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E55582-004

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P1V5_DDR3_CPU2

R7B11 100 1% 1/16W 1.5

A93548-043 0402LF 0.75

P1V5_DDR3_CPU2_VREF_J_D OUT 92< 96>

R7B10 100 1% 1/16W

C7B15 0.1UF 16V 10%

A93548-043 0402LF A36096-030 0402LF

P1V5_DDR3_CPU2

R7D3 100 1% 1/16W 1.5

A93548-043 0402LF 0.75

P1V5_DDR3_CPU2_VREF_J_A OUT 92<

R7D4 100 1% 1/16W

C7D10 0.1UF 16V 10%

A93548-043 0402LF A36096-030 0402LF

DDR3 CPU2 CHANNEL J DIMM1

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 92 OF 303	

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J7B2

CONN240_E55582004

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			14 172	A<14>	DQ<61>	228	61
			13 196	A<13>	DQ<60>	227	60
			12 174	A<12>	DQ<59>	115	59
			11 55	A<11>	DQ<58>	114	58
			10 70	A<10>	DQ<57>	109	57
			9 175	A<9>	DQ<56>	108	56
			8 177	A<8>	DQ<55>	225	55
			7 56	A<7>	DQ<54>	224	54
			6 178	A<6>	DQ<53>	219	53
			5 58	A<5>	DQ<52>	218	52
			4 59	A<4>	DQ<51>	106	51
			3 180	A<3>	DQ<50>	105	50
			2 61	A<2>	DQ<49>	100	49
			1 181	A<1>	DQ<48>	99	48
81>	IN	M_K_MA<15..0>	0 188	A<0>	DQ<47>	216	47
81>	IN	M_K_BA<1..0>			DQ<46>	215	46
			1 190	BA<1>	DQ<45>	210	45
			0 71	BA<0>	DQ<44>	209	44
					DQ<43>	97	43
81>	IN	M_K_CK_DP<2>	63	NC_CK1P	DQ<42>	96	42
81>	IN	M_K_CK_DN<2>	64	NC_CK1N	DQ<41>	91	41
81>	IN	M_K_CK_DP<0>	184	CK0P	DQ<40>	90	40
81>	IN	M_K_CK_DN<0>	185	CK0N	DQ<39>	207	39
81>	IN	M_K_CS_N<3..0>			DQ<38>	206	38
			3 198	CS<3>	DQ<37>	201	37
			2 79	CS<2>	DQ<36>	200	36
			1 76	CS<1>	DQ<35>	88	35
			0 193	CS<0>	DQ<34>	87	34
					DQ<33>	82	33
81>	IN	M_K_CKE<1>	169	CKE<1>	DQ<32>	81	32
81>	IN	M_K_CKE<0>	50	CKE<0>	DQ<31>	156	31
					DQ<30>	155	30
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81>	IN	M_K_RAS_N	192	RAS_N	DQ<28>	149	28
81>	IN	M_K_CAS_N	74	CAS_N	DQ<27>	37	27
81>	IN	M_K_ODT<1..0>			DQ<26>	36	26
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			0 195	ODT<0>	DQ<24>	30	24
					DQ<23>	147	23
81>	IN	M_K_MA_PAR	68	PAR_IN_NC	DQ<22>	146	22
81<	OUT	M_K_PAR_ERR_N<0>	53	ERR_OUT_NC	DQ<21>	141	21
81<>	BI	M_K_ECC<7..0>			DQ<20>	140	20
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			5 159	CB<5>	DQ<17>	22	17
			4 158	CB<4>	DQ<16>	21	16
			3 46	CB<3>	DQ<15>	138	15
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			1 40	CB<1>	DQ<13>	132	13
			0 39	CB<0>	DQ<12>	131	12
					DQ<11>	19	11
92< 79>	IN	M_JK_RESET_LVC1V5_N	168	RESET_N	DQ<10>	18	10
					DQ<9>	13	9
			236	VDDSPD	DQ<8>	12	8
		SPD ADDRESS = 0XA8	119	SA<2>	DQ<7>	129	7
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200> 96<> 92<>	BI	SMB_DDR_JK_LVC3_SDA	238	SDA	DQ<4>	122	4
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93>	IN	P1V5_DDR3_CPU2_VREF_K_A	67	VREFCA	DQ<0>	3	0

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M_K_DQ<63..0> BI 81<>

P3V3

3.3 — R7E1 1/16W 1% 1 2 A93548-023 1K 1% 0402LF

J7B2

CONN240_E55582004

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			20	VSS<52>	VDD<15>	66	
			23	VSS<51>	VDD<14>	69	
			26	VSS<50>	VDD<13>	72	
			29	VSS<49>	VDD<12>	75	
			32	VSS<48>	VDD<11>	78	
			35	VSS<47>	VDD<10>	170	
			38	VSS<46>	VDD<9>	173	
			41	VSS<45>	VDD<8>	176	
			44	VSS<44>	VDD<7>	179	
			47	VSS<43>	VDD<6>	182	
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			86	VSS<40>	VDD<3>	189	
			89	VSS<39>	VDD<2>	191	
			92	VSS<38>	VDD<1>	194	
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			98	VSS<36>			
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			107	VSS<33>	VTT<1>	120	
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			229	VSS<3>			
			232	VSS<2>			
			235	VSS<1>			
			239	VSS<0>			

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P1V5_DDR3_CPU2 — 1.5

P0V75_VTT_DDR3_CPU2 — 0.75

P1V5_DDR3_CPU2 — 1.5

C7C6 10UF 6.3V 20% 602433-075 0603LF

C7C5 10UF 6.3V 20% 602433-075 0603LF

J7B2

CONN240_E55582004

DQS17P_DM8	161	17		
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DQS16P_DM7	230	16		
DQS16N_NC	231		16	
DQS15P_DM6	221	15		
DQS15N_NC	222		15	
DQS14P_DM5	212	14		
DQS14N_NC	213		14	
DQS13P_DM4	203	13		
DQS13N_NC	204		13	
DQS12P_DM3	152	12		
DQS12N_NC	153		12	
DQS11P_DM2	143	11		
DQS11N_NC	144		11	
DQS10P_DM1	134	10		
DQS10N_NC	135		10	
DQS9P_DM0	125	9		
DQS9N_NC	126		9	
DQS8P	43	8		
DQS8N	42		8	
DQS7P	112	7		
DQS7N	111		7	
DQS6P	103	6		
DQS6N	102		6	
DQS5P	94	5		
DQS5N	93		5	
DQS4P	85	4		
DQS4N	84		4	
DQS3P	34	3		
DQS3N	33		3	
DQS2P	25	2		
DQS2N	24		2	
DQS1P	16	1		
DQS1N	15		1	
DQS0P	7	0		
DQS0N	6		0	

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M_K_DQS_DN<17..0> BI 81<>

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P1V5_DDR3_CPU2

R7B9 100 1% 1/16W 1 2 1.5

A93548-043 0402LF 0.75

P1V5_DDR3_CPU2_VREF_K_D OUT 93< 96>

R7B8 100 1% 1/16W 1 2

C7B13 0.1UF 16V 10% 1 2

A93548-043 0402LF

A36096-030 0402LF

P1V5_DDR3_CPU2

R7D2 100 1% 1/16W 1 2 1.5

A93548-043 0402LF 0.75

P1V5_DDR3_CPU2_VREF_K_A OUT 93<

R7D1 100 1% 1/16W 1 2

C7D2 0.1UF 16V 10% 1 2

A93548-043 0402LF

A36096-030 0402LF

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DDR3 CPU2 CHANNEL K DIMM1

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 93 OF 303	

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J9E2

CONN240_E55582004

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		14 172	A<14>	DQ<61>	228 61
		13 196	A<13>	DQ<60>	227 60
		12 174	A<12>	DQ<59>	115 59
		11 55	A<11>	DQ<58>	114 58
		10 70	A<10>	DQ<57>	109 57
		9 175	A<9>	DQ<56>	108 56
		8 177	A<8>	DQ<55>	225 55
		7 56	A<7>	DQ<54>	224 54
		6 178	A<6>	DQ<53>	219 53
		5 58	A<5>	DQ<52>	218 52
		4 59	A<4>	DQ<51>	106 51
		3 180	A<3>	DQ<50>	105 50
		2 61	A<2>	DQ<49>	100 49
		1 181	A<1>	DQ<48>	99 48
82> IN	M_L_MA<15..0>	0 188	A<0>	DQ<47>	216 47
82> IN	M_L_BA<1..0>			DQ<46>	215 46
		1 190	BA<1>	DQ<45>	210 45
		0 71	BA<0>	DQ<44>	209 44
				DQ<43>	97 43
82> IN	M_L_CK_DP<2>	63	NC_CK1P	DQ<42>	96 42
82> IN	M_L_CK_DN<2>	64	NC_CK1N	DQ<41>	91 41
82> IN	M_L_CK_DP<0>	184	CK0P	DQ<40>	90 40
82> IN	M_L_CK_DN<0>	185	CK0N	DQ<39>	207 39
82> IN	M_L_CS_N<3..0>			DQ<38>	206 38
		3 198	CS<3>	DQ<37>	201 37
		2 79	CS<2>	DQ<36>	200 36
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				DQ<33>	82 33
82> IN	M_L_CKE<1>	169	CKE<1>	DQ<32>	81 32
82> IN	M_L_CKE<0>	50	CKE<0>	DQ<31>	156 31
				DQ<30>	155 30
82> IN	M_L_WE_N	73	WE_N	DQ<29>	150 29
82> IN	M_L_RAS_N	192	RAS_N	DQ<28>	149 28
82> IN	M_L_CAS_N	74	CAS_N	DQ<27>	37 27
82> IN	M_L_ODT<1..0>			DQ<26>	36 26
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		0 195	ODT<0>	DQ<24>	30 24
				DQ<23>	147 23
82> IN	M_L_MA_PAR	68	PAR_IN_NC	DQ<22>	146 22
82< OUT	M_L_PAR_ERR_N<0>	53	ERR_OUT_NC	DQ<21>	141 21
82<> BI	M_L_ECC<7..0>			DQ<20>	140 20
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		6 164	CB<6>	DQ<18>	27 18
		5 159	CB<5>	DQ<17>	22 17
		4 158	CB<4>	DQ<16>	21 16
		3 46	CB<3>	DQ<15>	138 15
		2 45	CB<2>	DQ<14>	137 14
		1 40	CB<1>	DQ<13>	132 13
		0 39	CB<0>	DQ<12>	131 12
				DQ<11>	19 11
95< 79> IN	M_LM_RESET_LVC1V5_N	168	RESET_N	DQ<10>	18 10
				DQ<9>	13 9
P3V3		236	VDDSPD	DQ<8>	12 8
3.3	SPD ADDRESS = 0XA0	119	SA<2>	DQ<7>	129 7
		237	SA<1>	DQ<6>	128 6
		117	SA<0>	DQ<5>	123 5
200> 96<> 95<> BI	SMB_DDR_LM_LVC3_SDA	238	SDA	DQ<4>	122 4
200<> 96< 95< IN	SMB_DDR_LM_LVC3_SCL	118	SCL	DQ<3>	10 3
206< 189> 100< OUT	FM_SKT2_DIMM_L1_EVENT_N	187	EVENT_N_NC	DQ<2>	9 2
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94> IN	P1V5_DDR3_CPU2_VREF_L_A	67	VREFCA	DQ<0>	3 0

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E55582-004

M_L_DQ<63..0> BI 82<>

J9E2

CONN240_E55582004

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23	VSS<51>	VDD<14>	69
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29	VSS<49>	VDD<12>	75
32	VSS<48>	VDD<11>	78
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44	VSS<44>	VDD<7>	179
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92	VSS<38>	VDD<1>	194
95	VSS<37>	VDD<0>	197
98	VSS<36>		
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104	VSS<34>	VTT<2>	48
107	VSS<33>	VTT<1>	120
110	VSS<32>	VTT<0>	240
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223	VSS<5>		
226	VSS<4>		
229	VSS<3>		
232	VSS<2>		
235	VSS<1>		
239	VSS<0>		

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E55582-004

P1V5_DDR3_CPU2

1.5

C9C4
10UF
6.3V
20%

602433-075
0603LF

P1V5_DDR3_CPU2

1.5

C9C7
10UF
6.3V
20%

602433-075
0603LF

P0V75_VTT_DDR3_CPU2

0.75

J9E2

CONN240_E55582004

DQS17P_DM8	161	17	
DQS17N_NC	162		17
DQS16P_DM7	230	16	
DQS16N_NC	231		16
DQS15P_DM6	221	15	
DQS15N_NC	222		15
DQS14P_DM5	212	14	
DQS14N_NC	213		14
DQS13P_DM4	203	13	
DQS13N_NC	204		13
DQS12P_DM3	152	12	
DQS12N_NC	153		12
DQS11P_DM2	143	11	
DQS11N_NC	144		11
DQS10P_DM1	134	10	
DQS10N_NC	135		10
DQS9P_DM0	125	9	
DQS9N_NC	126		9
DQS8P	43	8	
DQS8N	42		8
DQS7P	112	7	
DQS7N	111		7
DQS6P	103	6	
DQS6N	102		6
DQS5P	94	5	
DQS5N	93		5
DQS4P	85	4	
DQS4N	84		4
DQS3P	34	3	
DQS3N	33		3
DQS2P	25	2	
DQS2N	24		2
DQS1P	16	1	
DQS1N	15		1
DQS0P	7	0	
DQS0N	6		0

M_L_DQS_DP<17..0> BI 82<>

M_L_DQS_DN<17..0> BI 82<>

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E55582-004

P1V5_DDR3_CPU2

R9E1
100
1%
1/16W
A93548-043
0402LF

1.5

0.75

P1V5_DDR3_CPU2_VREF_L_D OUT 94< 96>

R9E2
100
1%
1/16W
A93548-043
0402LF

C9E1
0.1UF
16V
10%
A36096-030
0402LF

P1V5_DDR3_CPU2

R9B22
100
1%
1/16W
A93548-043
0402LF

1.5

0.75

P1V5_DDR3_CPU2_VREF_L_A OUT 94<

R9B23
100
1%
1/16W
A93548-043
0402LF

C9B9
0.1UF
16V
10%
A36096-030
0402LF

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DDR3 CPU2 CHANNEL L DIMM1

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 94 OF 303	

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J9E1

CONN240_E55582004

83> IN	M_M_BA<2>		52	A16_BA2	DQ<63>	234	63
		15	171	A<15>	DQ<62>	233	62
		14	172	A<14>	DQ<61>	228	61
		13	196	A<13>	DQ<60>	227	60
		12	174	A<12>	DQ<59>	115	59
		11	55	A<11>	DQ<58>	114	58
		10	70	A<10>	DQ<57>	109	57
		9	175	A<9>	DQ<56>	108	56
		8	177	A<8>	DQ<55>	225	55
		7	56	A<7>	DQ<54>	224	54
		6	178	A<6>	DQ<53>	219	53
		5	58	A<5>	DQ<52>	218	52
		4	59	A<4>	DQ<51>	106	51
		3	180	A<3>	DQ<50>	105	50
		2	61	A<2>	DQ<49>	100	49
		1	181	A<1>	DQ<48>	99	48
83> IN	M_M_MA<15..0>	0	188	A<0>	DQ<47>	216	47
83> IN	M_M_BA<1..0>				DQ<46>	215	46
		1	190	BA<1>	DQ<45>	210	45
		0	71	BA<0>	DQ<44>	209	44
					DQ<43>	97	43
83> IN	M_M_CK_DP<2>		63	NC_CK1P	DQ<42>	96	42
83> IN	M_M_CK_DN<2>		64	NC_CK1N	DQ<41>	91	41
83> IN	M_M_CK_DP<0>		184	CK0P	DQ<40>	90	40
83> IN	M_M_CK_DN<0>		185	CK0N	DQ<39>	207	39
83> IN	M_M_CS_N<3..0>				DQ<38>	206	38
		3	198	CS<3>	DQ<37>	201	37
		2	79	CS<2>	DQ<36>	200	36
		1	76	CS<1>	DQ<35>	88	35
		0	193	CS<0>	DQ<34>	87	34
					DQ<33>	82	33
83> IN	M_M_CKE<1>		169	CKE<1>	DQ<32>	81	32
83> IN	M_M_CKE<0>		50	CKE<0>	DQ<31>	156	31
					DQ<30>	155	30
83> IN	M_M_WE_N		73	WE_N	DQ<29>	150	29
83> IN	M_M_RAS_N		192	RAS_N	DQ<28>	149	28
83> IN	M_M_CAS_N		74	CAS_N	DQ<27>	37	27
83> IN	M_M_ODT<1..0>				DQ<26>	36	26
		1	77	ODT<1>	DQ<25>	31	25
		0	195	ODT<0>	DQ<24>	30	24
					DQ<23>	147	23
83> IN	M_M_MA_PAR		68	PAR_IN_NC	DQ<22>	146	22
83< OUT	M_M_PAR_ERR_N<0>		53	ERR_OUT_NC	DQ<21>	141	21
83<> BI	M_M_ECC<7..0>				DQ<20>	140	20
		7	165	CB<7>	DQ<19>	28	19
		6	164	CB<6>	DQ<18>	27	18
		5	159	CB<5>	DQ<17>	22	17
		4	158	CB<4>	DQ<16>	21	16
		3	46	CB<3>	DQ<15>	138	15
		2	45	CB<2>	DQ<14>	137	14
		1	40	CB<1>	DQ<13>	132	13
		0	39	CB<0>	DQ<12>	131	12
					DQ<11>	19	11
94< 79> IN	M_LM_RESET_LVC1V5_N		168	RESET_N	DQ<10>	18	10
					DQ<9>	13	9
			236	VDDSPD	DQ<8>	12	8
	SPD ADDRESS = 0XA8		119	SA<2>	DQ<7>	129	7
	M_M_SA<2>		237	SA<1>	DQ<6>	128	6
			117	SA<0>	DQ<5>	123	5
200> 96<> 94<> BI	SMB_DDR_LM_LVC3_SDA		238	SDA	DQ<4>	122	4
200<> 96< 94< IN	SMB_DDR_LM_LVC3_SCL		118	SCL	DQ<3>	10	3
206< 189> 100< OUT	FM_SKT2_DIMM_M1_EVENT_N		187	EVENT_N_NC	DQ<2>	9	2
96> 95> IN	P1V5_DDR3_CPU2_VREF_M_D		1	VREFDQ	DQ<1>	4	1
95> IN	P1V5_DDR3_CPU2_VREF_M_A		67	VREFCA	DQ<0>	3	0

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M_M_DQ<63..0> BI 83<>

P3V3

3.3 — R9B4 1K 1% 1/16W 0402LF — A93548-023

SMB_DDR_LM_LVC3_SDA, SMB_DDR_LM_LVC3_SCL, FM_SKT2_DIMM_M1_EVENT_N

P1V5_DDR3_CPU2

R9E3 100 1% 1/16W — 1.5 — 0.75 — A93548-043 0402LF

P1V5_DDR3_CPU2_VREF_M_D OUT 95< 96>

R9E4 100 1% 1/16W — A93548-043 0402LF

C9E2 0.1UF 16V 10% — A36096-030 0402LF

P1V5_DDR3_CPU2

R9C7 100 1% 1/16W — 1.5 — 0.75 — A93548-043 0402LF

P1V5_DDR3_CPU2_VREF_M_A OUT 95<

R9C8 100 1% 1/16W — A93548-043 0402LF

C9C1 0.1UF 16V 10% — A36096-030 0402LF

J9E1

CONN240_E55582004

2	VSS<58>	VDD<21>	51
5	VSS<57>	VDD<20>	54
8	VSS<56>	VDD<19>	57
11	VSS<55>	VDD<18>	60
14	VSS<54>	VDD<17>	62
17	VSS<53>	VDD<16>	65
20	VSS<52>	VDD<15>	66
23	VSS<51>	VDD<14>	69
26	VSS<50>	VDD<13>	72
29	VSS<49>	VDD<12>	75
32	VSS<48>	VDD<11>	78
35	VSS<47>	VDD<10>	170
38	VSS<46>	VDD<9>	173
41	VSS<45>	VDD<8>	176
44	VSS<44>	VDD<7>	179
47	VSS<43>	VDD<6>	182
80	VSS<42>	VDD<5>	183
83	VSS<41>	VDD<4>	186
86	VSS<40>	VDD<3>	189
89	VSS<39>	VDD<2>	191
92	VSS<38>	VDD<1>	194
95	VSS<37>	VDD<0>	197
98	VSS<36>		
101	VSS<35>	VTT<3>	49
104	VSS<34>	VTT<2>	48
107	VSS<33>	VTT<1>	120
110	VSS<32>	VTT<0>	240
113	VSS<31>		
116	VSS<30>		
121	VSS<29>	NC_TEST	167 TP_M_D1_NC2
124	VSS<28>		
127	VSS<27>		
130	VSS<26>		
133	VSS<25>		
136	VSS<24>		
139	VSS<23>		
142	VSS<22>		
145	VSS<21>		
148	VSS<20>		
151	VSS<19>		
154	VSS<18>		
157	VSS<17>		
160	VSS<16>		
163	VSS<15>		
166	VSS<14>		
199	VSS<13>		
202	VSS<12>		
205	VSS<11>		
208	VSS<10>		
211	VSS<9>		
214	VSS<8>		
217	VSS<7>		
220	VSS<6>		
223	VSS<5>		
226	VSS<4>		
229	VSS<3>		
232	VSS<2>		
235	VSS<1>		
239	VSS<0>		

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P1V5_DDR3_CPU2 — 1.5

P0V75_VTT_DDR3_CPU2 — 0.75

P1V5_DDR3_CPU2 — 1.5

C9C6 10UF 6.3V 20% 602433-075 0603LF

C9C5 10UF 6.3V 20% 602433-075 0603LF

J9E1

CONN240_E55582004

DQS17P_DM8	161	17	
DQS17N_NC	162		17
DQS16P_DM7	230	16	
DQS16N_NC	231		16
DQS15P_DM6	221	15	
DQS15N_NC	222		15
DQS14P_DM5	212	14	
DQS14N_NC	213		14
DQS13P_DM4	203	13	
DQS13N_NC	204		13
DQS12P_DM3	152	12	
DQS12N_NC	153		12
DQS11P_DM2	143	11	
DQS11N_NC	144		11
DQS10P_DM1	134	10	
DQS10N_NC	135		10
DQS9P_DM0	125	9	
DQS9N_NC	126		9
DQS8P	43	8	
DQS8N	42		8
DQS7P	112	7	
DQS7N	111		7
DQS6P	103	6	
DQS6N	102		6
DQS5P	94	5	
DQS5N	93		5
DQS4P	85	4	
DQS4N	84		4
DQS3P	34	3	
DQS3N	33		3
DQS2P	25	2	
DQS2N	24		2
DQS1P	16	1	
DQS1N	15		1
DQS0P	7	0	
DQS0N	6		0

M_M_DQS_DP<17..0> BI 83<>

M_M_DQS_DN<17..0> BI 83<>

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E55582-004

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DDR3 CPU2 CHANNEL M DIMM1

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 95 OF 303	

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ROOM = VREFDQ_CPU2

P3V3_AUX NEEDED FOR POT IF DESIGN SUPPORT S3

P3V3

3.3

DECOUPLING CAP
CAD NOTE:
PLACE CLOSE TO CHIP

C7E4 0.1UF 0402LF 16V X7R 10% A36096-030 VREFDQ_CPU2

R7E10 0 CHIP A93549-001 VREFDQ_CPU2 0402LF 5% 1/16W

R7E11 0 CHIP A93549-001 VREFDQ_CPU2 0402LF 5% 1/16W

200<> 93< 92< IN SMB_DDR_JK_LVC3_SCL — SMB_DDR_JK_DAC_LVC3_SCL

93<> 92<> 200> BI SMB_DDR_JK_LVC3_SDA — SMB_DDR_JK_DAC_LVC3_SDA

U7E2 VREFDQ_CPU2 ISL90727

VCC (1) SCL (3) SDA (4) GND (2) RW (5) RH (6)

E47385-001

SMBUS ADDRESS=0X5C

CONNECTION TO THE P1V5_DDR3_CPU2 VOLTAGE RAIL SHOULD BE NEAR THE P1V5_DDR3VR SENSE POINT

P1V5_DDR3_CPU2

1.5

R7E8 12.1K 1% 1/16W CHIP 0402LF A93548-018 VREFDQ_CPU2

P1V5_DDR3_CPU2_VREF_JK_RW

0.75

R7E9 12.1K 1% 1/16W 0402LF A93548-018 VREFDQ_CPU2

WRITE VREF FROM CPU TO THE DIMMS

79> IN P1V5_DDR3_JK_VREFDQTX

R7E5 A93549-001 0402LF 5% 1/16W VREFDQ_CPU2

P1V5_DDR3_CPU2_VREF_JK_OPFB

U7E3 INN INP VSN VSP OUT LMV321

E21441-001 VREFDQ_CPU2

R7E6 2.20 CHIP A93549-051 VREFDQ_CPU2 0402LF 5% 1/16W

R7E7 100 1% 1/16W CHIP 0402LF A93548-043 VREFDQ_CPU2

C7E5 1.0UF 6.3V 10% EMPTY A36096-027 0402LF VREFDQ_CPU2

P1V5_DDR3_CPU2_VREF_J_D — 0.75 — VREFDQ_CPU2 OUT 92< 92>

R3R11 0 CHIP A93549-001 VREFDQ_CPU2 0402LF 5% 1/16W

P1V5_DDR3_CPU2_VREF_K_D — 0.75 — VREFDQ_CPU2 OUT 93< 93>

R3R10 0 CHIP A93549-001 VREFDQ_CPU2 0402LF 5% 1/16W

DDR3 PROCESSOR VREF GENERATION

P1V5_DDR3_CPU2

R7C8 100 1% 1/16W A93548-043 0402LF VREFDQ_CPU2

R7C7 100 1% 1/16W A93548-043 0402LF VREFDQ_CPU2

C7C2 0.1UF 16V 10% A36096-030 0402LF VREFDQ_CPU2

P1V5_DDR3_JK_VREFDQRX OUT 79<

CAD NOTE:
PLACE CIRCUIT AS CLOSE AS POSSBIBLE TO CPU
REFER TO RS-ROMLEY PDG FOR LATEST GUIDELINE
FROM ROMLEY PDG:
NOMIMAL TRACE WIDTH = 10 MILS
NOMIMAL TRACE SPACING = 20 MILS
CPU BREAKOUT REQ = 4-MIL WIDTH / 4-MIL SPACING
THE DECOUPLING CAP RECOMMENDED IS 0603 0.1UF

DECOUPLING CAP
CAD NOTE:
PLACE CLOSE TO CHIP

P5V

C3R4 1UF 16V 10% X5R 644066-061 0805LF VREFDQ_CPU2

P5V_AUX NEEDED FOR OP AMP IF DESIGN SUPPORT S3

REVIEW DATASHEET OF OPAMP FOR CORRECT DECOUPLING VALUES

P3V3_AUX NEEDED FOR POT IF DESIGN SUPPORT S3

P3V3

3.3

DECOUPLING CAP
CAD NOTE:
PLACE CLOSE TO CHIP

C9E8 0.1UF 0402LF 16V X7R 10% A36096-030 VREFDQ_CPU2

R9E9 0 CHIP A93549-001 VREFDQ_CPU2 0402LF 5% 1/16W

R9E8 0 CHIP A93549-001 VREFDQ_CPU2 0402LF 5% 1/16W

200<> 95< 94< IN SMB_DDR_LM_LVC3_SCL — SMB_DDR_LM_DAC_LVC3_SCL

200> 95<> 94<> BI SMB_DDR_LM_LVC3_SDA — SMB_DDR_LM_DAC_LVC3_SDA

U9E3 VREFDQ_CPU2 ISL90727

VCC (1) SCL (3) SDA (4) GND (2) RW (5) RH (6)

E47385-001

SMBUS ADDRESS=0X5C

CONNECTION TO THE P1V5_DDR3_CPU2 VOLTAGE RAIL SHOULD BE NEAR THE P1V5_DDR3VR SENSE POINT

P1V5_DDR3_CPU2

1.5

R9E14 12.1K 1% 1/16W CHIP 0402LF A93548-018 VREFDQ_CPU2

P1V5_DDR3_CPU2_VREF_LM_RW

0.75

R9E11 12.1K 1% 1/16W 0402LF A93548-018 VREFDQ_CPU2

WRITE VREF FROM CPU TO THE DIMMS

79> IN P1V5_DDR3_LM_VREFDQTX

R1R6 A93549-001 0402LF 5% 1/16W VREFDQ_CPU2

P1V5_DDR3_CPU2_VREF_LM_OPFB

U9E2 INN INP VSN VSP OUT LMV321

E21441-001 VREFDQ_CPU2

R9E7 2.20 CHIP A93549-051 VREFDQ_CPU2 0402LF 5% 1/16W

R9E6 100 1% 1/16W CHIP 0402LF A93548-043 VREFDQ_CPU2

C9E7 1.0UF 6.3V 10% EMPTY A36096-027 0402LF VREFDQ_CPU2

P1V5_DDR3_CPU2_VREF_LM_D — 0.75 — VREFDQ_CPU2 OUT 94< 94>

R1R5 0 CHIP A93549-001 VREFDQ_CPU2 0402LF 5% 1/16W

P1V5_DDR3_CPU2_VREF_M_D — 0.75 — VREFDQ_CPU2 OUT 95< 95>

R9E12 0 CHIP A93549-001 VREFDQ_CPU2 0402LF 5% 1/16W

DDR3 PROCESSOR VREF GENERATION

P1V5_DDR3_CPU2

R9C6 100 1% 1/16W A93548-043 0402LF VREFDQ_CPU2

R9C3 100 1% 1/16W A93548-043 0402LF VREFDQ_CPU2

C9B10 0.1UF 16V 10% A36096-030 0402LF VREFDQ_CPU2

P1V5_DDR3_LM_VREFDQRX OUT 79<

CAD NOTE:
PLACE CIRCUIT AS CLOSE AS POSSBIBLE TO CPU
REFER TO RS-ROMLEY PDG FOR LATEST GUIDELINE
FROM ROMLEY PDG:
NOMIMAL TRACE WIDTH = 10 MILS
NOMIMAL TRACE SPACING = 20 MILS
CPU BREAKOUT REQ = 4-MIL WIDTH / 4-MIL SPACING
THE DECOUPLING CAP RECOMMENDED IS 0603 0.1UF

DECOUPLING CAP
CAD NOTE:
PLACE CLOSE TO CHIP

P5V

C1R3 1UF 16V 10% X5R 644066-061 0805LF VREFDQ_CPU2

P5V_AUX NEEDED FOR OP AMP IF DESIGN SUPPORT S3

REVIEW DATASHEET OF OPAMP FOR CORRECT DECOUPLING VALUES

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CPU2 DDR3 DQ REFERENCE

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 96 OF 303	

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CATERROR_N

COMMON CATERROR SIGNAL IS PULLED UP TO VTT_CPU0 SINCE IT IS ALWAYS PRESENT, AVOIDING FALSE SIGNAL ASSERTION
CAD NOTE: FOLLOW A STAR TOPOLOGY
CAD NOTE: CPU TO PULLUP RES = LESS THAN 2"
CAD NOTE: EACH CPU TO PULLUP AT COMMON NODE: 5"-15"
CAD NOTE: TRACE LENGTH MATCHING REQUIRED (5%)
CAD NOTE: PLACE SERIES RESISTOR RIGHT WHERE THE STUB SPRINGS

DE NOTE:

NORMAL OPERATION (AND PRODUCTION):
STUFF SERIES RESISTOR,
UNSTUFF PULL-UP AT CPU SIDE

DEBUG OPERATION:
ABILITY TO ISOLATE CAT ERROR FROM A CPU TO OTHERS.
EMPTY SERIES RESISTOR AND STUFF PULL-UP AT CPU SIDE

ROOM: CATERR0

CAD NOTE
FROM ROMLEY PDG:
PLACE WITHIN 2" FROM CPU
TO CPU

P1V05_VTT_CPU0
VTT_CPU0 USED WHEN THIS CPU IS ISOLATED

R5F27 51.10 1% 1/16W 1.05
A93548-072 0402LF CATERR0

ROMLEY PDG: 51.1OHM

CAD NOTE:
REFER TO ROMLEY PDG
FOR LENGTH CONSTRAINS

33<> IN IRQ_CPU0_CATERR_LVC1_N — R5F24 0 5% 1/16W — A93549-001 0402LF CATERR0 — IRQ_CPU_CATERR_LVC1_N

P1V05_VTT_CPU0
VTT_CPU0 USED SINCE IT IS ALWAYS PRESENT
AVOIDING FALSE SIGNAL ASSERTION

R2T12 51.10 1% 1/16W 1.05
A93548-072 0402LF CATERR0

IRQ_CPU_CATERR_LVC1_N — R6F34 1K 1% 1/16W — A93548-023 0402LF CATERR — IRQ_CPU_CATERR_R_LVC1_N — OUT 125<

0-OHM STUFFED	INCLUDE CPU CATERR <DEFAULT>
0-OHM UNSTUFFED	ISOLATE CPU CATERR

ROOM: CATERR1

P1V05_VTT_CPU1
VTT_CPU1 USED WHEN THIS CPU IS ISOLATED

R9F11 51.10 1% 1/16W 1.05
A93548-072 0402LF CATERR1

56<> IN IRQ_CPU1_CATERR_LVC1_N — R9F10 0 5% 1/16W — A93549-001 0402LF CATERR1 — IRQ_CPU_CATERR_LVC1_N

0-OHM STUFFED	INCLUDE CPU CATERR <DEFAULT>
0-OHM UNSTUFFED	ISOLATE CPU CATERR

ROOM: CATERR2

P1V05_VTT_CPU2
VTT_CPU2 USED WHEN THIS CPU IS ISOLATED

R8E19 51.10 1% 1/16W 1.05
A93548-072 0402LF CATERR2

79<> IN IRQ_CPU2_CATERR_LVC1_N — R8E20 0 5% 1/16W — A93549-001 0402LF CATERR2 — IRQ_CPU_CATERR_LVC1_N

0-OHM STUFFED	INCLUDE CPU CATERR <DEFAULT>
0-OHM UNSTUFFED	ISOLATE CPU CATERR

ROOM: CATERR3

P1V05_VTT_CPU3
VTT_CPU3 USED WHEN THIS CPU IS ISOLATED

R5E7 51.10 1% 1/16W 1.05
A93548-072 0402LF CATERR3

102<> IN IRQ_CPU3_CATERR_LVC1_N — R5E10 0 5% 1/16W — A93549-001 0402LF CATERR3 — IRQ_CPU_CATERR_LVC1_N

0-OHM STUFFED	INCLUDE CPU CATERR <DEFAULT>
0-OHM UNSTUFFED	ISOLATE CPU CATERR

ROOM: CATERR

J5F1
CONN2_A91829027
STAKE PIN FOR MONITORING
SUITABLE FOR 093ST
IO1 IO2
A91829-027 CATERR

P3V3_STBY
3.3 R6F5 1K 1% 1/16W
A93548-023 0402LF CATERR

125> IN IRQ_CPU_CATERR_R_LVC3_N — R6F7 33 1% 1/16W — A93548-503 0402LF CATERR — IRQ_CPU_CATERR_LVC3_N — OUT 130< 148< 169< 176<

CAD NOTE: PLACE SERIES RESISTORS AS CLOSE AS POSSIBLE TO THE OUTPUT OF THEIR CORRESSPONDING VOLTAGE TRANSLATOR GTL2107: WITHIN 0.5"

CPU SIDEBAND: CATERROR_N CIRCUITRY

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DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 99 OF 303	

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THERMTRIP CIRCUITRY

CAD NOTE: CPU TO PULLUP RES = 2" TO 22"
CAD NOTE: PULLUP TO GTL2107 = LESS THAN 1.5"
ALL CATERROR SIGNALS ARE PULLED UP TO VTT_CPU0 SINCE IT IS ALWAYS PRESENT, AVOIDING FALSE SIGNAL ASSERTION

P1V05_VTT_CPU0 — VTT_CPU0 USED SINCE IT IS ALWAYS PRESENT AVOIDING FALSE SIGNAL ASSERTION

R5F46 — 75 1% 1/16W — A93548-003 0402LF

CAD NOTE: REFER TO ROMLEY PDG FOR LAYOUT CONSTRAINTS

33> IN FM_CPU0_THERMTRIP_LVC1_N — R6F31 0 5% 1/16W A93549-001 0402LF SOCKET0 — FM_CPU0_THERMTRIP_R_LVC1_N OUT 125<

P1V05_VTT_CPU0 — VTT_CPU0 USED SINCE IT IS ALWAYS PRESENT AVOIDING FALSE SIGNAL ASSERTION

R8F10 — 75 1% 1/16W — A93548-003 0402LF SOCKET1

CAD NOTE: REFER TO ROMLEY PDG FOR LAYOUT CONSTRAINTS

56> IN FM_CPU1_THERMTRIP_LVC1_N — R8F9 0 5% 1/16W A93549-001 0402LF SOCKET1 — FM_CPU1_THERMTRIP_R_LVC1_N OUT 125<

P1V05_VTT_CPU0 — VTT_CPU0 USED SINCE IT IS ALWAYS PRESENT AVOIDING FALSE SIGNAL ASSERTION

R8E5 — 75 1% 1/16W — A93548-003 0402LF SOCKET2

CAD NOTE: REFER TO ROMLEY PDG FOR LAYOUT CONSTRAINTS

79> IN FM_CPU2_THERMTRIP_LVC1_N — R8E4 0 5% 1/16W A93549-001 0402LF SOCKET2 — FM_CPU2_THERMTRIP_R_LVC1_N OUT 125<

P1V05_VTT_CPU0 — VTT_CPU0 USED SINCE IT IS ALWAYS PRESENT AVOIDING FALSE SIGNAL ASSERTION

R5E11 — 75 1% 1/16W — A93548-003 0402LF SOCKET3

CAD NOTE: REFER TO ROMLEY PDG FOR LAYOUT CONSTRAINTS

102> IN FM_CPU3_THERMTRIP_LVC1_N — R5E13 0 5% 1/16W A93549-001 0402LF SOCKET3 — FM_CPU3_THERMTRIP_R_LVC1_N OUT 126<

PULL-UP RES IS AT PAGE 190

THERMTRIP

CAD NOTE: PLACE SERIES RESISTORS AS CLOSE AS POSSIBLE TO THE OUTPUT OF THEIR CORRESSPONDING VOLTAGE TRANSLATOR GTL2107: WITHIN 0.5"

125> IN FM_CPU0_THERMTRIP_R_LVC3_N — R6F8 33 1% 1/16W A93548-503 0402LF SOCKET0 — FM_CPU0_THERMTRIP_LVC3_N OUT 100< 207< 128< 190>

125> IN FM_CPU1_THERMTRIP_R_LVC3_N — R2T8 33 1% 1/16W A93548-503 0402LF SOCKET1 — FM_CPU1_THERMTRIP_LVC3_N OUT 100< 128< 190> 207<

125> IN FM_CPU2_THERMTRIP_R_LVC3_N — R8E27 33 1% 1/16W A93548-503 0402LF SOCKET2 — FM_CPU2_THERMTRIP_LVC3_N OUT 100< 206< 128< 190>

126> IN FM_CPU3_THERMTRIP_R_LVC3_N — R5E12 33 1% 1/16W A93548-503 0402LF SOCKET3 — FM_CPU3_THERMTRIP_LVC3_N OUT 100< 128< 190> 206<

MEM_EVENTS & THERMTRIP SIGNALS COMBINED THRU WIRED AND

74LVC07A BUFFER WITH OPENDRAIN OUTPUTS

P3V3_STBY — R1C40 4.7K 1% 1/16W A93548-517 0402LF SOCKET0 — 3.3

207< 190> 128< 100> IN FM_CPU0_THERMTRIP_LVC3_N — EU1D7 74LVC07A 1 2 — FM_THERMTRIP_LVC3_N OUT 169<
207< 190> 128< 100> IN FM_CPU1_THERMTRIP_LVC3_N — EU1D7 74LVC07A 3 4
206< 190> 128< 100> IN FM_CPU2_THERMTRIP_LVC3_N — EU1D7 74LVC07A 5 6
206< 190> 128< 100> IN FM_CPU3_THERMTRIP_LVC3_N — EU1D7 74LVC07A 9 8
207< 189> 46> IN FM_SKT0_DIMM_A1_EVENT_N — EU1D7 74LVC07A 11 10
207< 189> 47> IN FM_SKT0_DIMM_B1_EVENT_N — EU1D7 74LVC07A 13 12
207< 189> 48> IN FM_SKT0_DIMM_C1_EVENT_N — EU9P7 74LVC07A 1 2
207< 189> 49> IN FM_SKT0_DIMM_D1_EVENT_N — EU9P7 74LVC07A 3 4
207< 189> 69> IN FM_SKT1_DIMM_E1_EVENT_N — EU9P7 74LVC07A 5 6
207< 189> 70> IN FM_SKT1_DIMM_F1_EVENT_N — EU9P7 74LVC07A 9 8
207< 189> 71> IN FM_SKT1_DIMM_G1_EVENT_N — EU9P7 74LVC07A 11 10
207< 189> 72> IN FM_SKT1_DIMM_H1_EVENT_N — EU9P7 74LVC07A 13 12
206< 189> 92> IN FM_SKT2_DIMM_J1_EVENT_N — EU1D8 74LVC07A 1 2
206< 189> 93> IN FM_SKT2_DIMM_K1_EVENT_N — EU1D8 74LVC07A 3 4
206< 189> 94> IN FM_SKT2_DIMM_L1_EVENT_N — EU1D8 74LVC07A 5 6
206< 189> 95> IN FM_SKT2_DIMM_M1_EVENT_N — EU1D8 74LVC07A 9 8
206< 189> 117> IN FM_SKT3_DIMM_R1_EVENT_N — EU1D8 74LVC07A 11 10
206< 189> 118> IN FM_SKT3_DIMM_T1_EVENT_N — EU1D8 74LVC07A 13 12
206< 189> 115> IN FM_SKT3_DIMM_N1_EVENT_N — EU7M2 74LVC07A 1 2
206< 189> 116> IN FM_SKT3_DIMM_P1_EVENT_N — EU7M2 74LVC07A 3 4

All D90453-001 VCC=P3V3_STBY;GND=GND;TH=GND;

P3V3_STBY — C1D12 DECOUPLING CAP PLACE CLOSE TO EACH 74LVC07A — 1UF 10V 10% — A36096-099 0402LF SOCKET0 — 3.3
P3V3_STBY — C1D15 DECOUPLING CAP PLACE CLOSE TO EACH 74LVC07A — 1UF 10V 10% — A36096-099 0402LF SOCKET0 — 3.3
P3V3_STBY — C1D14 DECOUPLING CAP PLACE CLOSE TO EACH 74LVC07A — 1UF 10V 10% — A36096-099 0402LF SOCKET0 — 3.3
P3V3_STBY — C7M18 DECOUPLING CAP PLACE CLOSE TO EACH 74LVC07A — 1UF 10V 10% — A36096-099 0402LF NIC — 3.3

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CPU SIDEBAND: THERMTRIP CIRCUITRY

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 100 OF 303

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CAD NOTE FROM ROMLEY PDG NOTE FOR PE_RBIAS:
THE ROUTING DISTANCE TO THE RESISTOR
SHOULD BE AS CLOSE AS POSSIBLE
(NO LONGER THAN 1.0" AND AT LEAST 15 MILS WIDE)
KEEP THE TRACES SEPARETED 30 MILS FROM ALL OTHERS.

C5R2 0.01UF 25V 10% A36096-045 0402LF SOCKET3

R5R11 49.9 1% 1/16W A93548-045 0402LF SOCKET3

DE NOTE: PE_RBIAS_SENSE NET MUST BE SHORTED
AT THE TOP OF PE_RBIAS 50OHM RESISTOR.
CONNECT SENSE AS CLOSE AS POSIBLE TO OTHER END OF RES

NET NAMES REFLECT ON-DIE TERMINATION AT CPU

U6C1
IC

SANDYBRIDGE_EP_EXT_D

PE_VREF_CAP	AJ43	A_CPU3_PE_VREF_CAP	QPI_VREF_CAP	CU51	A_CPU3_QPI_VREF_CAP
PE_RBIAS_SENSE	AF52		QPI_RBIAS_SENSE	CC53	
PE_RBIAS	AH52	A_CPU3_PE_RBIAS	QPI_RBIAS	CE53	A_CPU3_QPI_RBIAS
BCLK1_DP	AW45	31> IN CLK_100M_CPU3_PCIE_DP	BCLK0_DP	CN43	CLK_100M_CPU3_QPI_DP IN 31>
BCLK1_DN	BA45	31> IN CLK_100M_CPU3_PCIE_DN	BCLK0_DN	CM44	CLK_100M_CPU3_QPI_DN IN 31>
PEHPSCL	BH48	TP_SMB_CPU3_PE_HP_1V05_SCL	RSVD<31>	CA45	NC_CPU3_RSVD<31>
PEHPSDA	BF48	TP_SMB_CPU3_PE_HP_1V05_SDA	RSVD<32>	BY46	NC_CPU3_RSVD<32>
RSVD<12>	D56	NC_CPU3_RSVD<12>	RSVD<18>	DD54	NC_CPU3_RSVD<18>
RSVD<8>	F56	NC_CPU3_RSVD<8>	RSVD<19>	DC55	NC_CPU3_RSVD<19>
RSVD<10>	E57	NC_CPU3_RSVD<10>	RSVD<17>	DE55	NC_CPU3_RSVD<17>
RSVD<7>	F58	NC_CPU3_RSVD<7>	RSVD<21>	DA57	NC_CPU3_RSVD<21>
RSVD<5>	H58	NC_CPU3_RSVD<5>	RSVD<22>	CY58	NC_CPU3_RSVD<22>
RSVD<63>	AR55	NC_CPU3_RSVD<63>	RSVD<40>	BM46	NC_CPU3_RSVD<40>
RSVD<62>	AU55	NC_CPU3_RSVD<62>	RSVD<37>	BP46	NC_CPU3_RSVD<37>
TXT_PLTEN	V52	54> IN PU_CPU3_DMIGEN2EN	RSVD<24>	CY48	NC_CPU3_RSVD<24>
FRMAGENT	AT50	54> IN PD_CPU3_FRMAGENT	RSVD<25>	CY46	NC_CPU3_RSVD<25>
BMCINIT	AL47	54> IN PD_CPU3_BMCINIT	THERMTRIP_N	BL47	FM_CPU3_THERMTRIP_LVC1_N OUT 100<
TXT_AGENT	AK52	54> IN PD_CPU3_LTEN	PROCHOT_N	BD52	FM_CPU3_PROCHOT_LVC1_N BI 122<>
BIST_ENABLE	AT48	54> IN PU_CPU3_BIST_EN	TEST4	BA55	PD_CPU3_TEST<4>
					NOTE: CONNECT TEST4 TO VSS PER PDG
IVT_ID_N	AH42	126< 54> OUT FM_CPU3_IVT_ID_LVC1_N	PRDY_N	R53	XDP_CPU3_PRDY_N OUT 134<>
			PREQ_N	U53	XDP_CPU3_PREQ_N IN 134<>
MEM_HOT_C23_N	E13	123<> BI FM_CPU3_MEMRT_MEMHOT_LVC1_N			
MEM_HOT_C01_N	CB22	123<> BI FM_CPU3_MEMNP_MEMHOT_LVC1_N	SOCKET_ID<1>	BC49	FM_CPU3_SOCKET_ID1_LVC1
DRAM_PWR_OK_C23	L15	76> IN PWRGD_CPU3_DRAMPWRGD_LVC1V5	SOCKET_ID<0>	CY52	FM_CPU3_SOCKET_ID0_LVC1
DRAM_PWR_OK_C01	CW17				
DDR_VREFDQTX_C23	P42	119< OUT P1V5_DDR3_RT_VREFDQTX			DE NOTE: SOCKET_ID[1:0] NETS HAVE PD ON DIE
DDR_VREFDQTX_C01	CN41	119< OUT P1V5_DDR3_NP_VREFDQTX			
DDR_VREFDQRX_C23	J1	119> IN P1V5_DDR3_RT_VREFDQRX			
DDR_VREFDQRX_C01	BY16	119> IN P1V5_DDR3_NP_VREFDQRX			
DDR_SDA_C23	R43	201< BI SMB_DDR_RT_LVC1_SDA	PECI	BJ47	PECI_CPU_LVC1 BI 33<> 56<> 79<> 196<>
DDR_SDA_C01	CW41	201< BI SMB_DDR_NP_LVC1_SDA			
DDR_SCL_C23	U43	201<> OUT SMB_DDR_RT_LVC1_SCL	SVIDCLK	CB44	SVID_CPU3_CLK_LVC1 OUT 55<
DDR_SCL_C01	CY42	201<> OUT SMB_DDR_NP_LVC1_SCL	SVIDDATA	BR45	SVID_CPU3_DAT_LVC1 BI 55<>
DDR_RESET_C23_N	AE27	118< 117< OUT M_RT_RESET_LVC1V5_N	SVIDALERT_N	CR43	SVID_CPU3_ALERT_LVC1_N IN 55>
DDR_RESET_C01_N	CB18	116< 115< OUT M_NP_RESET_LVC1V5_N			
			PMSYNC	K52	IRQ_PM_SYNC2_LVC1 IN 79< 135>
SKTOCC_N	BU49	206< 170< 169< 129< 54> OUT FM_CPU3_SKTOCC_CO_N	PWRGOOD	BJ53	PWRGD_CPU3_PWRGOOD_LVC1 IN 76<> 77>
			EAR_N	CH56	RST_CPU_EAR_LVC1_N BI 33<> 56<> 79<> 125< 134>
RSVD<23>	CY56	NC_CPU3_RSVD<23>	RESET_N	CK44	RST_CPU3_RESET_LVC1_N IN 76>
CAT_ERR_N	CC51	99< BI IRQ_CPU3_CATERR_LVC1_N			
SAFE_MODE_BOOT	DA55	54> IN PD_CPU3_SAFE_MODE			
TDI	BW43	133> 79> IN JTAG_CPU2_G_TDO	TDO	CA43	JTAG_CPU_G_TDO OUT 133> 134<
TCK	BY44	134> 133> 79< IN JTAG_CPU_LVC1_TCK1			
TMS	BV44	134> 133> 79< 56< 33< IN JTAG_CPU_G_TMS			
TRST_N	CT54	134> 133> 79< 56< 33< IN JTAG_CPU_LVC1_TRST_N			

1/17

E64556-001

CAD NOTE FROM ROMLEY PDG NOTE FOR QPI_RBIAS:
THE ROUTING DISTANCE TO THE RESISTOR
SHOULD BE AS CLOSE AS POSSIBLE
(POSSIBLY NO LONGER THAN 1.0" AND AT LEAST 10 MILS WIDE)

R5R17 49.9 1% 1/16W A93548-045 0402LF SOCKET3

C5R3 0.01UF 25V 10% A36096-045 0402LF SOCKET3

DE NOTE: QPI_RBIAS_SENSE NET MUST BE SHORTED
AT THE TOP OF QPI_RBIAS 50OHM RESISTOR.
CONNECT SENSE AS CLOSE AS POSIBLE TO OTHER END OF RES

P1V05_VTT_CPU3
1.05

*DE NOTE: RESISTOR VALUES COULD BE 240 OHM 5%,
CURRENT ONES 1% USED TO REDUCE BOM.

R5R12 240 1% 1/16W A93548-504 0402 SOCKET3

R5R14 240 1% 1/16W A93548-504 0402 SOCKET3

CPU	SOCKET_ID[2:0]	PECI ADDRESS
CPU3	011B	0X33

EAR_N SIGNAL HAS A 6K OHM PU ON CPU DIE

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CPU SOCKET 3 (1 OF 13)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 102 OF 303	

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U6C1

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SANDYBRIDGE_EP_EXT_D

63	M_N_DQ<63>	CL41	DDR0_DQ<63>	DDR0_DQS_DP<17>	CD16	M_N_DQS_DP<17>	17
62	M_N_DQ<62>	CJ41	DDR0_DQ<62>	DDR0_DQS_DP<16>	CJ39	M_N_DQS_DP<16>	16
61	M_N_DQ<61>	CL37	DDR0_DQ<61>	DDR0_DQS_DP<15>	CC39	M_N_DQS_DP<15>	15
60	M_N_DQ<60>	CJ37	DDR0_DQ<60>	DDR0_DQS_DP<14>	CK32	M_N_DQS_DP<14>	14
59	M_N_DQ<59>	CK42	DDR0_DQ<59>	DDR0_DQS_DP<13>	CD32	M_N_DQS_DP<13>	13
58	M_N_DQ<58>	CH42	DDR0_DQ<58>	DDR0_DQS_DP<12>	CB10	M_N_DQS_DP<12>	12
57	M_N_DQ<57>	CK38	DDR0_DQ<57>	DDR0_DQS_DP<11>	CJ13	M_N_DQS_DP<11>	11
56	M_N_DQ<56>	CH38	DDR0_DQ<56>	DDR0_DQS_DP<10>	CC5	M_N_DQS_DP<10>	10
55	M_N_DQ<55>	CB42	DDR0_DQ<55>	DDR0_DQS_DP<9>	CE7	M_N_DQS_DP<9>	9
54	M_N_DQ<54>	CC41	DDR0_DQ<54>	DDR0_DQS_DP<8>	CC17	M_N_DQS_DP<8>	8
53	M_N_DQ<53>	CE37	DDR0_DQ<53>	DDR0_DQS_DP<7>	CK40	M_N_DQS_DP<7>	7
52	M_N_DQ<52>	CC37	DDR0_DQ<52>	DDR0_DQS_DP<6>	CD40	M_N_DQS_DP<6>	6
51	M_N_DQ<51>	CD42	DDR0_DQ<51>	DDR0_DQS_DP<5>	CJ33	M_N_DQS_DP<5>	5
50	M_N_DQ<50>	CE41	DDR0_DQ<50>	DDR0_DQS_DP<4>	CC33	M_N_DQS_DP<4>	4
49	M_N_DQ<49>	CD38	DDR0_DQ<49>	DDR0_DQS_DP<3>	CE11	M_N_DQS_DP<3>	3
48	M_N_DQ<48>	CB38	DDR0_DQ<48>	DDR0_DQS_DP<2>	CK14	M_N_DQS_DP<2>	2
47	M_N_DQ<47>	CH34	DDR0_DQ<47>	DDR0_DQS_DP<1>	CF4	M_N_DQS_DP<1>	1
46	M_N_DQ<46>	CK34	DDR0_DQ<46>	DDR0_DQS_DP<0>	CH8	M_N_DQS_DP<0>	0
45	M_N_DQ<45>	CH30	DDR0_DQ<45>				
44	M_N_DQ<44>	CK30	DDR0_DQ<44>	DDR0_DQS_DN<17>	CF16	M_N_DQS_DN<17>	17
43	M_N_DQ<43>	CJ35	DDR0_DQ<43>	DDR0_DQS_DN<16>	CL39	M_N_DQS_DN<16>	16
42	M_N_DQ<42>	CL35	DDR0_DQ<42>	DDR0_DQS_DN<15>	CE39	M_N_DQS_DN<15>	15
41	M_N_DQ<41>	CJ31	DDR0_DQ<41>	DDR0_DQS_DN<14>	CH32	M_N_DQS_DN<14>	14
40	M_N_DQ<40>	CL31	DDR0_DQ<40>	DDR0_DQS_DN<13>	CB32	M_N_DQS_DN<13>	13
39	M_N_DQ<39>	CB34	DDR0_DQ<39>	DDR0_DQS_DN<12>	CC11	M_N_DQS_DN<12>	12
38	M_N_DQ<38>	CD34	DDR0_DQ<38>	DDR0_DQS_DN<11>	CL13	M_N_DQS_DN<11>	11
37	M_N_DQ<37>	CB30	DDR0_DQ<37>	DDR0_DQS_DN<10>	CD4	M_N_DQS_DN<10>	10
36	M_N_DQ<36>	CD30	DDR0_DQ<36>	DDR0_DQS_DN<9>	CF8	M_N_DQS_DN<9>	9
35	M_N_DQ<35>	CC35	DDR0_DQ<35>	DDR0_DQS_DN<8>	CE17	M_N_DQS_DN<8>	8
34	M_N_DQ<34>	CE35	DDR0_DQ<34>	DDR0_DQS_DN<7>	CH40	M_N_DQS_DN<7>	7
33	M_N_DQ<33>	CC31	DDR0_DQ<33>	DDR0_DQS_DN<6>	CB40	M_N_DQS_DN<6>	6
32	M_N_DQ<32>	CE31	DDR0_DQ<32>	DDR0_DQS_DN<5>	CL33	M_N_DQS_DN<5>	5
31	M_N_DQ<31>	CF10	DDR0_DQ<31>	DDR0_DQS_DN<4>	CE33	M_N_DQS_DN<4>	4
30	M_N_DQ<30>	CH10	DDR0_DQ<30>	DDR0_DQS_DN<3>	CD10	M_N_DQS_DN<3>	3
29	M_N_DQ<29>	CA9	DDR0_DQ<29>	DDR0_DQS_DN<2>	CH14	M_N_DQS_DN<2>	2
28	M_N_DQ<28>	BW9	DDR0_DQ<28>	DDR0_DQS_DN<1>	CE3	M_N_DQS_DN<1>	1
27	M_N_DQ<27>	CD12	DDR0_DQ<27>	DDR0_DQS_DN<0>	CG7	M_N_DQS_DN<0>	0
26	M_N_DQ<26>	CB12	DDR0_DQ<26>				
25	M_N_DQ<25>	BY12	DDR0_DQ<25>	DDR0_MA<15>	CN19	M_N_MA<15>	15
24	M_N_DQ<24>	BY10	DDR0_DQ<24>	DDR0_MA<14>	CG19	M_N_MA<14>	14
23	M_N_DQ<23>	CL15	DDR0_DQ<23>	DDR0_MA<13>	CG29	M_N_MA<13>	13
22	M_N_DQ<22>	CJ15	DDR0_DQ<22>	DDR0_MA<12>	CK20	M_N_MA<12>	12
21	M_N_DQ<21>	CL11	DDR0_DQ<21>	DDR0_MA<11>	CL21	M_N_MA<11>	11
20	M_N_DQ<20>	CG13	DDR0_DQ<20>	DDR0_MA<10>	CK26	M_N_MA<10>	10
19	M_N_DQ<19>	CM16	DDR0_DQ<19>	DDR0_MA<9>	CN21	M_N_MA<9>	9
18	M_N_DQ<18>	CK16	DDR0_DQ<18>	DDR0_MA<8>	CK22	M_N_MA<8>	8
17	M_N_DQ<17>	CM12	DDR0_DQ<17>	DDR0_MA<7>	CM22	M_N_MA<7>	7
16	M_N_DQ<16>	CK12	DDR0_DQ<16>	DDR0_MA<6>	CN23	M_N_MA<6>	6
15	M_N_DQ<15>	CG5	DDR0_DQ<15>	DDR0_MA<5>	CL23	M_N_MA<5>	5
14	M_N_DQ<14>	CG3	DDR0_DQ<14>	DDR0_MA<4>	CM24	M_N_MA<4>	4
13	M_N_DQ<13>	CA3	DDR0_DQ<13>	DDR0_MA<3>	CK24	M_N_MA<3>	3
12	M_N_DQ<12>	CA1	DDR0_DQ<12>	DDR0_MA<2>	CG25	M_N_MA<2>	2
11	M_N_DQ<11>	CJ5	DDR0_DQ<11>	DDR0_MA<1>	CR25	M_N_MA<1>	1
10	M_N_DQ<10>	CH4	DDR0_DQ<10>	DDR0_MA<0>	CL25	M_N_MA<0>	0
9	M_N_DQ<9>	CB4	DDR0_DQ<9>				
8	M_N_DQ<8>	CB2	DDR0_DQ<8>	DDR0_ECC<7>	CK18	M_N_ECC<7>	7
7	M_N_DQ<7>	CL7	DDR0_DQ<7>	DDR0_ECC<6>	CG17	M_N_ECC<6>	6
6	M_N_DQ<6>	CJ7	DDR0_DQ<6>	DDR0_ECC<5>	CD14	M_N_ECC<5>	5
5	M_N_DQ<5>	CA7	DDR0_DQ<5>	DDR0_ECC<4>	CB14	M_N_ECC<4>	4
4	M_N_DQ<4>	BY6	DDR0_DQ<4>	DDR0_ECC<3>	CF18	M_N_ECC<3>	3
3	M_N_DQ<3>	CL9	DDR0_DQ<3>	DDR0_ECC<2>	CH18	M_N_ECC<2>	2
2	M_N_DQ<2>	CK8	DDR0_DQ<2>	DDR0_ECC<1>	CC15	M_N_ECC<1>	1
1	M_N_DQ<1>	CD8	DDR0_DQ<1>	DDR0_ECC<0>	CE15	M_N_ECC<0>	0
0	M_N_DQ<0>	CC7	DDR0_DQ<0>				
	NC_M_N_CS_N<9>	CK28	DDR0_CS_N<9>	DDR0_CKE<5>	CE19	NC_M_N_CKE<5>	
	NC_M_N_CS_N<8>	CL27	DDR0_CS_N<8>	DDR0_CKE<4>	CF20	NC_M_N_CKE<4>	
	NC_M_N_CS_N<7>	CC25	DDR0_CS_N<7>	DDR0_CKE<3>	CP18	NC_M_N_CKE<3>	
	NC_M_N_CS_N<6>	CB26	DDR0_CS_N<6>	DDR0_CKE<2>	CH20	NC_M_N_CKE<2>	
	NC_M_N_CS_N<5>	CF26	DDR0_CS_N<5>	DDR0_CKE<1>	CM18	M_N_CKE<1>	1
	NC_M_N_CS_N<4>	CG27	DDR0_CS_N<4>	DDR0_CKE<0>	CL19	M_N_CKE<0>	0
3	M_N_CS_N<3>	CB28	DDR0_CS_N<3>	DDR0_BA<2>	CM20	M_N_BA<2>	2
2	M_N_CS_N<2>	CC23	DDR0_CS_N<2>	DDR0_BA<1>	CN27	M_N_BA<1>	1
1	M_N_CS_N<1>	CH26	DDR0_CS_N<1>	DDR0_BA<0>	CM28	M_N_BA<0>	0
0	M_N_CS_N<0>	CN25	DDR0_CS_N<0>				
	NC_M_N_CK_DP<3>	CH22	DDR0_CLK_DP<3>	DDR0_ODT<5>	CC27	NC_M_N_ODT<5>	
	M_N_CK_DP<2>	CG21	DDR0_CLK_DP<2>	DDR0_ODT<4>	CB24	NC_M_N_ODT<4>	
	NC_M_N_CK_DP<1>	CG23	DDR0_CLK_DP<1>	DDR0_ODT<3>	CF28	NC_M_N_ODT<3>	
	M_N_CK_DP<0>	CH24	DDR0_CLK_DP<0>	DDR0_ODT<2>	CH28	NC_M_N_ODT<2>	
	NC_M_N_CK_DN<3>	CF22	DDR0_CLK_DN<3>	DDR0_ODT<1>	CE27	M_N_ODT<1>	1
	M_N_CK_DN<2>	CE21	DDR0_CLK_DN<2>	DDR0_ODT<0>	CE25	M_N_ODT<0>	0
	NC_M_N_CK_DN<1>	CE23	DDR0_CLK_DN<1>				
	M_N_CK_DN<0>	CF24	DDR0_CLK_DN<0>	DDR0_WE_N	CN29	M_N_WE_N	
				DDR0_RAS_N	CE29	M_N_RAS_N	
				DDR0_PAR_ERR_N	CC21	M_N_PAR_ERR_N<0>	
				DDR0_CAS_N	CL29	M_N_CAS_N	
				DDR0_MA_PAR	CM26	M_N_MA_PAR	

M_N_DQ<63..0> BI 115<>

M_N_DQS_DP<17..0> BI 115<>

M_N_DQS_DN<17..0> BI 115<>

M_N_MA<15..0> OUT 115<

M_N_ECC<7..0> BI 115<>

M_N_CS_N<3..0> OUT 115<

M_N_CKE<1..0> OUT 115<

M_N_BA<2..0> OUT 115<

M_N_ODT<1..0> OUT 115<

NC_M_N_CK_DP<3> OUT 115<

M_N_CK_DP<2> OUT 115<

NC_M_N_CK_DP<1> OUT 115<

M_N_CK_DP<0> OUT 115<

NC_M_N_CK_DN<3> OUT 115<

M_N_CK_DN<2> OUT 115<

NC_M_N_CK_DN<1> OUT 115<

M_N_CK_DN<0> OUT 115<

DDR0_WE_N OUT 115<

DDR0_RAS_N OUT 115<

DDR0_PAR_ERR_N IN 115>

DDR0_CAS_N OUT 115<

DDR0_MA_PAR OUT 115<

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CPU SOCKET 3 (2 OF 13)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 103 OF 303	

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U6C1 IC

SANDYBRIDGE_EP_EXT_D

116<> BI	M_P_DQ<63..0>	63	M_P_DQ<63>	DF40	DDR1_DQ<63>	DDR1_DQS_DP<17>	CY14	M_P_DQS_DP<17> 17
		62	M_P_DQ<62>	DA39	DDR1_DQ<62>	DDR1_DQS_DP<16>	DB38	M_P_DQS_DP<16> 16
		61	M_P_DQ<61>	DC37	DDR1_DQ<61>	DDR1_DQS_DP<15>	CP38	M_P_DQS_DP<15> 15
		60	M_P_DQ<60>	DA37	DDR1_DQ<60>	DDR1_DQS_DP<14>	DC33	M_P_DQS_DP<14> 14
		59	M_P_DQ<59>	DB40	DDR1_DQ<59>	DDR1_DQS_DP<13>	CU31	M_P_DQS_DP<13> 13
		58	M_P_DQ<58>	DD40	DDR1_DQ<58>	DDR1_DQS_DP<12>	CT14	M_P_DQS_DP<12> 12
		57	M_P_DQ<57>	DF38	DDR1_DQ<57>	DDR1_DQS_DP<11>	CP8	M_P_DQS_DP<11> 11
		56	M_P_DQ<56>	DE37	DDR1_DQ<56>	DDR1_DQS_DP<10>	DD8	M_P_DQS_DP<10> 10
		55	M_P_DQ<55>	CV40	DDR1_DQ<55>	DDR1_DQS_DP<9>	CT2	M_P_DQS_DP<9> 9
		54	M_P_DQ<54>	CT40	DDR1_DQ<54>	DDR1_DQS_DP<8>	DC15	M_P_DQS_DP<8> 8
		53	M_P_DQ<53>	CV36	DDR1_DQ<53>	DDR1_DQS_DP<7>	DC39	M_P_DQS_DP<7> 7
		52	M_P_DQ<52>	CT36	DDR1_DQ<52>	DDR1_DQS_DP<6>	CU39	M_P_DQS_DP<6> 6
		51	M_P_DQ<51>	CU41	DDR1_DQ<51>	DDR1_DQS_DP<5>	DB34	M_P_DQS_DP<5> 5
		50	M_P_DQ<50>	CR41	DDR1_DQ<50>	DDR1_DQS_DP<4>	CP32	M_P_DQS_DP<4> 4
		49	M_P_DQ<49>	CU37	DDR1_DQ<49>	DDR1_DQS_DP<3>	CU15	M_P_DQS_DP<3> 3
		48	M_P_DQ<48>	CR37	DDR1_DQ<48>	DDR1_DQS_DP<2>	CU9	M_P_DQS_DP<2> 2
		47	M_P_DQ<47>	DE35	DDR1_DQ<47>	DDR1_DQS_DP<1>	DE9	M_P_DQS_DP<1> 1
		46	M_P_DQ<46>	DF34	DDR1_DQ<46>	DDR1_DQS_DP<0>	CR3	M_P_DQS_DP<0> 0
		45	M_P_DQ<45>	CY32	DDR1_DQ<45>			
		44	M_P_DQ<44>	DA31	DDR1_DQ<44>	DDR1_DQS_DN<17>	DB14	M_P_DQS_DN<17> 17
		43	M_P_DQ<43>	DA35	DDR1_DQ<43>	DDR1_DQS_DN<16>	CY38	M_P_DQS_DN<16> 16
		42	M_P_DQ<42>	DC35	DDR1_DQ<42>	DDR1_DQS_DN<15>	CT38	M_P_DQS_DN<15> 15
		41	M_P_DQ<41>	DD32	DDR1_DQ<41>	DDR1_DQS_DN<14>	DE33	M_P_DQS_DN<14> 14
		40	M_P_DQ<40>	DA33	DDR1_DQ<40>	DDR1_DQS_DN<13>	CR31	M_P_DQS_DN<13> 13
		39	M_P_DQ<39>	CR33	DDR1_DQ<39>	DDR1_DQS_DN<12>	CP14	M_P_DQS_DN<12> 12
		38	M_P_DQ<38>	CU33	DDR1_DQ<38>	DDR1_DQS_DN<11>	CT8	M_P_DQS_DN<11> 11
		37	M_P_DQ<37>	CR29	DDR1_DQ<37>	DDR1_DQS_DN<10>	DB8	M_P_DQS_DN<10> 10
		36	M_P_DQ<36>	CU29	DDR1_DQ<36>	DDR1_DQS_DN<9>	CR1	M_P_DQS_DN<9> 9
		35	M_P_DQ<35>	CP34	DDR1_DQ<35>	DDR1_DQS_DN<8>	DE15	M_P_DQS_DN<8> 8
		34	M_P_DQ<34>	CT34	DDR1_DQ<34>	DDR1_DQS_DN<7>	DE39	M_P_DQS_DN<7> 7
		33	M_P_DQ<33>	CP30	DDR1_DQ<33>	DDR1_DQS_DN<6>	CR39	M_P_DQS_DN<6> 6
		32	M_P_DQ<32>	CT30	DDR1_DQ<32>	DDR1_DQS_DN<5>	CY34	M_P_DQS_DN<5> 5
		31	M_P_DQ<31>	CV16	DDR1_DQ<31>	DDR1_DQS_DN<4>	CT32	M_P_DQS_DN<4> 4
		30	M_P_DQ<30>	CT16	DDR1_DQ<30>	DDR1_DQS_DN<3>	CR15	M_P_DQS_DN<3> 3
		29	M_P_DQ<29>	CV12	DDR1_DQ<29>	DDR1_DQS_DN<2>	CV8	M_P_DQS_DN<2> 2
		28	M_P_DQ<28>	CT12	DDR1_DQ<28>	DDR1_DQS_DN<1>	DC9	M_P_DQS_DN<1> 1
		27	M_P_DQ<27>	CU17	DDR1_DQ<27>	DDR1_DQS_DN<0>	CT4	M_P_DQS_DN<0> 0
		26	M_P_DQ<26>	CR17	DDR1_DQ<26>			
		25	M_P_DQ<25>	CU13	DDR1_DQ<25>	DDR1_MA<15>	DC17	M_P_MA<15> 15
		24	M_P_DQ<24>	CR13	DDR1_DQ<24>	DDR1_MA<14>	DB18	M_P_MA<14> 14
		23	M_P_DQ<23>	CV10	DDR1_DQ<23>	DDR1_MA<13>	DB30	M_P_MA<13> 13
		22	M_P_DQ<22>	CW9	DDR1_DQ<22>	DDR1_MA<12>	DC19	M_P_MA<12> 12
		21	M_P_DQ<21>	CT6	DDR1_DQ<21>	DDR1_MA<11>	DE19	M_P_MA<11> 11
		20	M_P_DQ<20>	CP6	DDR1_DQ<20>	DDR1_MA<10>	DF26	M_P_MA<10> 10
		19	M_P_DQ<19>	CP10	DDR1_DQ<19>	DDR1_MA<9>	DA19	M_P_MA<9> 9
		18	M_P_DQ<18>	CT10	DDR1_DQ<18>	DDR1_MA<8>	DB20	M_P_MA<8> 8
		17	M_P_DQ<17>	CU7	DDR1_DQ<17>	DDR1_MA<7>	DF20	M_P_MA<7> 7
		16	M_P_DQ<16>	CR7	DDR1_DQ<16>	DDR1_MA<6>	DE21	M_P_MA<6> 6
		15	M_P_DQ<15>	DF10	DDR1_DQ<15>	DDR1_MA<5>	DF22	M_P_MA<5> 5
		14	M_P_DQ<14>	DB10	DDR1_DQ<14>	DDR1_MA<4>	DB22	M_P_MA<4> 4
		13	M_P_DQ<13>	DB6	DDR1_DQ<13>	DDR1_MA<3>	DA23	M_P_MA<3> 3
		12	M_P_DQ<12>	CY6	DDR1_DQ<12>	DDR1_MA<2>	DF24	M_P_MA<2> 2
		11	M_P_DQ<11>	DE11	DDR1_DQ<11>	DDR1_MA<1>	DE23	M_P_MA<1> 1
		10	M_P_DQ<10>	DC11	DDR1_DQ<10>	DDR1_MA<0>	DC23	M_P_MA<0> 0
		9	M_P_DQ<9>	DC7	DDR1_DQ<9>			
		8	M_P_DQ<8>	DA7	DDR1_DQ<8>	DDR1_ECC<7>	DF16	M_P_ECC<7> 7
		7	M_P_DQ<7>	CW3	DDR1_DQ<7>	DDR1_ECC<6>	DA15	M_P_ECC<6> 6
		6	M_P_DQ<6>	CV2	DDR1_DQ<6>	DDR1_ECC<5>	DC13	M_P_ECC<5> 5
		5	M_P_DQ<5>	CL3	DDR1_DQ<5>	DDR1_ECC<4>	DA13	M_P_ECC<4> 4
		4	M_P_DQ<4>	CM4	DDR1_DQ<4>	DDR1_ECC<3>	DB16	M_P_ECC<3> 3
		3	M_P_DQ<3>	CY4	DDR1_DQ<3>	DDR1_ECC<2>	DD16	M_P_ECC<2> 2
		2	M_P_DQ<2>	CV4	DDR1_DQ<2>	DDR1_ECC<1>	DF14	M_P_ECC<1> 1
		1	M_P_DQ<1>	CP2	DDR1_DQ<1>	DDR1_ECC<0>	DE13	M_P_ECC<0> 0
		0	M_P_DQ<0>	CP4	DDR1_DQ<0>			
			NC_M_P_CS_N<9>	DA27	DDR1_CS_N<9>	DDR1_CKE<5>	CT18	NC_M_P_CKE<5>
			NC_M_P_CS_N<8>	CR21	DDR1_CS_N<8>	DDR1_CKE<4>	CR19	NC_M_P_CKE<4>
			NC_M_P_CS_N<7>	CT26	DDR1_CS_N<7>	DDR1_CKE<3>	DA17	NC_M_P_CKE<3>
			NC_M_P_CS_N<6>	DA29	DDR1_CS_N<6>	DDR1_CKE<2>	CY18	NC_M_P_CKE<2>
			NC_M_P_CS_N<5>	CT24	DDR1_CS_N<5>	DDR1_CKE<1>	CU19	M_P_CKE<1> 1
116< OUT	M_P_CS_N<3..0>		NC_M_P_CS_N<4>	CU25	DDR1_CS_N<4>	DDR1_CKE<0>	CT20	M_P_CKE<0> 0
	3		M_P_CS_N<3>	CR27	DDR1_CS_N<3>			
	2		M_P_CS_N<2>	CR23	DDR1_CS_N<2>	DDR1_BA<2>	DF18	M_P_BA<2> 2
	1		M_P_CS_N<1>	CU23	DDR1_CS_N<1>	DDR1_BA<1>	DC25	M_P_BA<1> 1
	0		M_P_CS_N<0>	DB24	DDR1_CS_N<0>	DDR1_BA<0>	DB26	M_P_BA<0> 0
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116< OUT			M_P_CK_DP<2>	CV24	DDR1_CLK_DP<2>	DDR1_ODT<4>	CU27	NC_M_P_ODT<4>
			NC_M_P_CK_DP<1>	CY22	DDR1_CLK_DP<1>	DDR1_ODT<3>	CV26	NC_M_P_ODT<3>
116< OUT			M_P_CK_DP<0>	CY20	DDR1_CLK_DP<0>	DDR1_ODT<2>	CY26	NC_M_P_ODT<2>
						DDR1_ODT<1>	DA25	M_P_ODT<1> 1
			NC_M_P_CK_DN<3>	DA21	DDR1_CLK_DN<3>	DDR1_ODT<0>	CT22	M_P_ODT<0> 0
116< OUT			M_P_CK_DN<2>	CY24	DDR1_CLK_DN<2>			
			NC_M_P_CK_DN<1>	CV22	DDR1_CLK_DN<1>	DDR1_WE_N	CV28	M_P_WE_N
116< OUT			M_P_CK_DN<0>	CV20	DDR1_CLK_DN<0>	DDR1_RAS_N	DB28	M_P_RAS_N
						DDR1_PAR_ERR_N	CU21	M_P_PAR_ERR_N<0>
						DDR1_CAS_N	CY30	M_P_CAS_N
						DDR1_MA_PAR	DE25	M_P_MA_PAR

M_P_DQS_DP<17..0> BI 116<>

M_P_DQS_DN<17..0> BI 116<>

M_P_MA<15..0> OUT 116<

M_P_ECC<7..0> BI 116<>

M_P_CKE<1..0> OUT 116<

M_P_BA<2..0> OUT 116<

M_P_ODT<1..0> OUT 116<

M_P_WE_N OUT 116<

M_P_RAS_N OUT 116<

M_P_PAR_ERR_N<0> IN 116>

M_P_CAS_N OUT 116<

M_P_MA_PAR OUT 116<

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CPU SOCKET 3 (3 OF 13)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 104 OF 303	

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IC

SANDYBRIDGE_EP_EXT_D

117<> BI M_R_DQ<63..0>

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62	M_R_DQ<62>	AF2	DDR2_DQ<62>
61	M_R_DQ<61>	V4	DDR2_DQ<61>
60	M_R_DQ<60>	U3	DDR2_DQ<60>
59	M_R_DQ<59>	AE5	DDR2_DQ<59>
58	M_R_DQ<58>	AF4	DDR2_DQ<58>
57	M_R_DQ<57>	Y4	DDR2_DQ<57>
56	M_R_DQ<56>	W3	DDR2_DQ<56>
55	M_R_DQ<55>	U9	DDR2_DQ<55>
54	M_R_DQ<54>	R9	DDR2_DQ<54>
53	M_R_DQ<53>	V14	DDR2_DQ<53>
52	M_R_DQ<52>	T14	DDR2_DQ<52>
51	M_R_DQ<51>	V10	DDR2_DQ<51>
50	M_R_DQ<50>	T10	DDR2_DQ<50>
49	M_R_DQ<49>	U13	DDR2_DQ<49>
48	M_R_DQ<48>	R13	DDR2_DQ<48>
47	M_R_DQ<47>	AE7	DDR2_DQ<47>
46	M_R_DQ<46>	AD8	DDR2_DQ<46>
45	M_R_DQ<45>	W7	DDR2_DQ<45>
44	M_R_DQ<44>	U7	DDR2_DQ<44>
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42	M_R_DQ<42>	AF8	DDR2_DQ<42>
41	M_R_DQ<41>	Y6	DDR2_DQ<41>
40	M_R_DQ<40>	V6	DDR2_DQ<40>
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38	M_R_DQ<38>	AB10	DDR2_DQ<38>
37	M_R_DQ<37>	AA13	DDR2_DQ<37>
36	M_R_DQ<36>	AD14	DDR2_DQ<36>
35	M_R_DQ<35>	AF10	DDR2_DQ<35>
34	M_R_DQ<34>	AG11	DDR2_DQ<34>
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32	M_R_DQ<32>	AC13	DDR2_DQ<32>
31	M_R_DQ<31>	AD32	DDR2_DQ<31>
30	M_R_DQ<30>	AB32	DDR2_DQ<30>
29	M_R_DQ<29>	W35	DDR2_DQ<29>
28	M_R_DQ<28>	AA35	DDR2_DQ<28>
27	M_R_DQ<27>	AF32	DDR2_DQ<27>
26	M_R_DQ<26>	AE33	DDR2_DQ<26>
25	M_R_DQ<25>	AE35	DDR2_DQ<25>
24	M_R_DQ<24>	AC35	DDR2_DQ<24>
23	M_R_DQ<23>	T30	DDR2_DQ<23>
22	M_R_DQ<22>	V30	DDR2_DQ<22>
21	M_R_DQ<21>	P34	DDR2_DQ<21>
20	M_R_DQ<20>	T34	DDR2_DQ<20>
19	M_R_DQ<19>	U29	DDR2_DQ<19>
18	M_R_DQ<18>	W29	DDR2_DQ<18>
17	M_R_DQ<17>	R33	DDR2_DQ<17>
16	M_R_DQ<16>	U33	DDR2_DQ<16>
15	M_R_DQ<15>	AE37	DDR2_DQ<15>
14	M_R_DQ<14>	AF38	DDR2_DQ<14>
13	M_R_DQ<13>	AA41	DDR2_DQ<13>
12	M_R_DQ<12>	AC41	DDR2_DQ<12>
11	M_R_DQ<11>	AC37	DDR2_DQ<11>
10	M_R_DQ<10>	AA37	DDR2_DQ<10>
9	M_R_DQ<9>	AD40	DDR2_DQ<9>
8	M_R_DQ<8>	AE41	DDR2_DQ<8>
7	M_R_DQ<7>	U37	DDR2_DQ<7>
6	M_R_DQ<6>	R37	DDR2_DQ<6>
5	M_R_DQ<5>	U41	DDR2_DQ<5>
4	M_R_DQ<4>	R41	DDR2_DQ<4>
3	M_R_DQ<3>	T36	DDR2_DQ<3>
2	M_R_DQ<2>	P36	DDR2_DQ<2>
1	M_R_DQ<1>	V40	DDR2_DQ<1>
0	M_R_DQ<0>	T40	DDR2_DQ<0>

NC_M_R_CS_N<9>	AA17	DDR2_CS_N<9>
NC_M_R_CS_N<8>	W17	DDR2_CS_N<8>
NC_M_R_CS_N<7>	Y16	DDR2_CS_N<7>
NC_M_R_CS_N<6>	AB16	DDR2_CS_N<6>
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NC_M_R_CS_N<4>	AA19	DDR2_CS_N<4>
M_R_CS_N<3>	AA15	DDR2_CS_N<3>
M_R_CS_N<2>	AD16	DDR2_CS_N<2>
M_R_CS_N<1>	AE19	DDR2_CS_N<1>
M_R_CS_N<0>	AB20	DDR2_CS_N<0>

117< OUT M_R_CS_N<3..0>

NC_M_R_CK_DP<3>	AA23	DDR2_CLK_DP<3>
M_R_CK_DP<2>	AA21	DDR2_CLK_DP<2>
NC_M_R_CK_DP<1>	AB22	DDR2_CLK_DP<1>
M_R_CK_DP<0>	AB24	DDR2_CLK_DP<0>

117< OUT

NC_M_R_CK_DN<3>	W23	DDR2_CLK_DN<3>
M_R_CK_DN<2>	W21	DDR2_CLK_DN<2>
NC_M_R_CK_DN<1>	Y22	DDR2_CLK_DN<1>
M_R_CK_DN<0>	Y24	DDR2_CLK_DN<0>

117< OUT

DDR2_DQS_DP<17>	AC29	M_R_DQS_DP<17>	17
DDR2_DQS_DP<16>	AC5	M_R_DQS_DP<16>	16
DDR2_DQS_DP<15>	T12	M_R_DQS_DP<15>	15
DDR2_DQS_DP<14>	Y8	M_R_DQS_DP<14>	14
DDR2_DQS_DP<13>	AB12	M_R_DQS_DP<13>	13
DDR2_DQS_DP<12>	Y34	M_R_DQS_DP<12>	12
DDR2_DQS_DP<11>	V32	M_R_DQS_DP<11>	11
DDR2_DQS_DP<10>	AB40	M_R_DQS_DP<10>	10
DDR2_DQS_DP<9>	U39	M_R_DQS_DP<9>	9
DDR2_DQS_DP<8>	AC27	M_R_DQS_DP<8>	8
DDR2_DQS_DP<7>	AB4	M_R_DQS_DP<7>	7
DDR2_DQS_DP<6>	W11	M_R_DQS_DP<6>	6
DDR2_DQS_DP<5>	AC7	M_R_DQS_DP<5>	5
DDR2_DQS_DP<4>	AE11	M_R_DQS_DP<4>	4
DDR2_DQS_DP<3>	AC33	M_R_DQS_DP<3>	3
DDR2_DQS_DP<2>	U31	M_R_DQS_DP<2>	2
DDR2_DQS_DP<1>	AB38	M_R_DQS_DP<1>	1
DDR2_DQS_DP<0>	V38	M_R_DQS_DP<0>	0

M_R_DQS_DP<17..0> BI 117<>

DDR2_DQS_DN<17>	AD28	M_R_DQS_DN<17>	17
DDR2_DQS_DN<16>	AD4	M_R_DQS_DN<16>	16
DDR2_DQS_DN<15>	V12	M_R_DQS_DN<15>	15
DDR2_DQS_DN<14>	AA7	M_R_DQS_DN<14>	14
DDR2_DQS_DN<13>	AD12	M_R_DQS_DN<13>	13
DDR2_DQS_DN<12>	AB34	M_R_DQS_DN<12>	12
DDR2_DQS_DN<11>	T32	M_R_DQS_DN<11>	11
DDR2_DQS_DN<10>	AC39	M_R_DQS_DN<10>	10
DDR2_DQS_DN<9>	W39	M_R_DQS_DN<9>	9
DDR2_DQS_DN<8>	AB28	M_R_DQS_DN<8>	8
DDR2_DQS_DN<7>	AC3	M_R_DQS_DN<7>	7
DDR2_DQS_DN<6>	U11	M_R_DQS_DN<6>	6
DDR2_DQS_DN<5>	AB8	M_R_DQS_DN<5>	5
DDR2_DQS_DN<4>	AC11	M_R_DQS_DN<4>	4
DDR2_DQS_DN<3>	AA33	M_R_DQS_DN<3>	3
DDR2_DQS_DN<2>	W31	M_R_DQS_DN<2>	2
DDR2_DQS_DN<1>	AD38	M_R_DQS_DN<1>	1
DDR2_DQS_DN<0>	T38	M_R_DQS_DN<0>	0

M_R_DQS_DN<17..0> BI 117<>

DDR2_MA<15>	U25	M_R_MA<15>	15
DDR2_MA<14>	W25	M_R_MA<14>	14
DDR2_MA<13>	R15	M_R_MA<13>	13
DDR2_MA<12>	T24	M_R_MA<12>	12
DDR2_MA<11>	U23	M_R_MA<11>	11
DDR2_MA<10>	T18	M_R_MA<10>	10
DDR2_MA<9>	R23	M_R_MA<9>	9
DDR2_MA<8>	T22	M_R_MA<8>	8
DDR2_MA<7>	P22	M_R_MA<7>	7
DDR2_MA<6>	R21	M_R_MA<6>	6
DDR2_MA<5>	U21	M_R_MA<5>	5
DDR2_MA<4>	P20	M_R_MA<4>	4
DDR2_MA<3>	T20	M_R_MA<3>	3
DDR2_MA<2>	U19	M_R_MA<2>	2
DDR2_MA<1>	R19	M_R_MA<1>	1
DDR2_MA<0>	AB18	M_R_MA<0>	0

M_R_MA<15..0> OUT 117<

DDR2_ECC<7>	AA27	M_R_ECC<7>	7
DDR2_ECC<6>	W27	M_R_ECC<6>	6
DDR2_ECC<5>	AD30	M_R_ECC<5>	5
DDR2_ECC<4>	AB30	M_R_ECC<4>	4
DDR2_ECC<3>	AB26	M_R_ECC<3>	3
DDR2_ECC<2>	Y26	M_R_ECC<2>	2
DDR2_ECC<1>	AF28	M_R_ECC<1>	1
DDR2_ECC<0>	AF30	M_R_ECC<0>	0

M_R_ECC<7..0> BI 117<>

DDR2_CKE<5>	AE23	NC_M_R_CKE<5>
DDR2_CKE<4>	AE25	NC_M_R_CKE<4>
DDR2_CKE<3>	AD24	NC_M_R_CKE<3>
DDR2_CKE<2>	U27	NC_M_R_CKE<2>
DDR2_CKE<1>	T26	M_R_CKE<1> 1
DDR2_CKE<0>	AA25	M_R_CKE<0> 0

M_R_CKE<1..0> OUT 117<

DDR2_BA<2>	P24	M_R_BA<2>	2
DDR2_BA<1>	L17	M_R_BA<1>	1
DDR2_BA<0>	R17	M_R_BA<0>	0

M_R_BA<2..0> OUT 117<

DDR2_ODT<5>	AE21	NC_M_R_ODT<5>
DDR2_ODT<4>	AD22	NC_M_R_ODT<4>
DDR2_ODT<3>	Y18	NC_M_R_ODT<3>
DDR2_ODT<2>	AD18	NC_M_R_ODT<2>
DDR2_ODT<1>	W19	M_R_ODT<1> 1
DDR2_ODT<0>	Y20	M_R_ODT<0> 0

M_R_ODT<1..0> OUT 117<

DDR2_WE_N	P16	M_R_WE_N	OUT 117<
DDR2_RAS_N	U17	M_R_RAS_N	OUT 117<
DDR2_PAR_ERR_N	AD20	M_R_PAR_ERR_N<0>	IN 117>
DDR2_CAS_N	T16	M_R_CAS_N	OUT 117<
DDR2_MA_PAR	M18	M_R_MA_PAR	OUT 117<

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E64556-001

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CPU SOCKET 3 (4 OF 13)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER / REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359 / 1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 105 OF 303

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SANDYBRIDGE_EP_EXT_D

118<> BI	M_T_DQ<63..0>	63	M_T_DQ<63>	M2	DDR3_DQ<63>	DDR3_DQS_DP<17>	F28	M_T_DQS_DP<17>	17
		62	M_T_DQ<62>	L1	DDR3_DQ<62>	DDR3_DQS_DP<16>	J3	M_T_DQS_DP<16>	16
		61	M_T_DQ<61>	H4	DDR3_DQ<61>	DDR3_DQS_DP<15>	G7	M_T_DQS_DP<15>	15
		60	M_T_DQ<60>	F4	DDR3_DQ<60>	DDR3_DQS_DP<14>	K12	M_T_DQS_DP<14>	14
		59	M_T_DQ<59>	P4	DDR3_DQ<59>	DDR3_DQS_DP<13>	E11	M_T_DQS_DP<13>	13
		58	M_T_DQ<58>	N3	DDR3_DQ<58>	DDR3_DQS_DP<12>	N31	M_T_DQS_DP<12>	12
		57	M_T_DQ<57>	H2	DDR3_DQ<57>	DDR3_DQS_DP<11>	D34	M_T_DQS_DP<11>	11
		56	M_T_DQ<56>	G3	DDR3_DQ<56>	DDR3_DQS_DP<10>	M38	M_T_DQS_DP<10>	10
		55	M_T_DQ<55>	M6	DDR3_DQ<55>	DDR3_DQS_DP<9>	E39	M_T_DQS_DP<9>	9
		54	M_T_DQ<54>	L7	DDR3_DQ<54>	DDR3_DQS_DP<8>	E27	M_T_DQS_DP<8>	8
		53	M_T_DQ<53>	D6	DDR3_DQ<53>	DDR3_DQS_DP<7>	M4	M_T_DQS_DP<7>	7
		52	M_T_DQ<52>	C7	DDR3_DQ<52>	DDR3_DQS_DP<6>	K6	M_T_DQS_DP<6>	6
		51	M_T_DQ<51>	P6	DDR3_DQ<51>	DDR3_DQS_DP<5>	N11	M_T_DQS_DP<5>	5
		50	M_T_DQ<50>	N7	DDR3_DQ<50>	DDR3_DQS_DP<4>	D10	M_T_DQS_DP<4>	4
		49	M_T_DQ<49>	F6	DDR3_DQ<49>	DDR3_DQS_DP<3>	N29	M_T_DQS_DP<3>	3
		48	M_T_DQ<48>	E7	DDR3_DQ<48>	DDR3_DQS_DP<2>	E33	M_T_DQS_DP<2>	2
		47	M_T_DQ<47>	M10	DDR3_DQ<47>	DDR3_DQS_DP<1>	J37	M_T_DQS_DP<1>	1
		46	M_T_DQ<46>	K10	DDR3_DQ<46>	DDR3_DQS_DP<0>	D38	M_T_DQS_DP<0>	0
		45	M_T_DQ<45>	M14	DDR3_DQ<45>				
		44	M_T_DQ<44>	K14	DDR3_DQ<44>	DDR3_DQS_DN<17>	H28	M_T_DQS_DN<17>	17
		43	M_T_DQ<43>	L9	DDR3_DQ<43>	DDR3_DQS_DN<16>	K4	M_T_DQS_DN<16>	16
		42	M_T_DQ<42>	J9	DDR3_DQ<42>	DDR3_DQS_DN<15>	H6	M_T_DQS_DN<15>	15
		41	M_T_DQ<41>	L13	DDR3_DQ<41>	DDR3_DQS_DN<14>	M12	M_T_DQS_DN<14>	14
		40	M_T_DQ<40>	J13	DDR3_DQ<40>	DDR3_DQS_DN<13>	G11	M_T_DQS_DN<13>	13
		39	M_T_DQ<39>	A9	DDR3_DQ<39>	DDR3_DQS_DN<12>	M30	M_T_DQS_DN<12>	12
		38	M_T_DQ<38>	F10	DDR3_DQ<38>	DDR3_DQS_DN<11>	B34	M_T_DQS_DN<11>	11
		37	M_T_DQ<37>	B12	DDR3_DQ<37>	DDR3_DQS_DN<10>	K38	M_T_DQS_DN<10>	10
		36	M_T_DQ<36>	F12	DDR3_DQ<36>	DDR3_DQS_DN<9>	G39	M_T_DQS_DN<9>	9
		35	M_T_DQ<35>	E9	DDR3_DQ<35>	DDR3_DQS_DN<8>	G27	M_T_DQS_DN<8>	8
		34	M_T_DQ<34>	C9	DDR3_DQ<34>	DDR3_DQS_DN<7>	L3	M_T_DQS_DN<7>	7
		33	M_T_DQ<33>	A11	DDR3_DQ<33>	DDR3_DQS_DN<6>	J7	M_T_DQS_DN<6>	6
		32	M_T_DQ<32>	D12	DDR3_DQ<32>	DDR3_DQS_DN<5>	L11	M_T_DQS_DN<5>	5
		31	M_T_DQ<31>	M26	DDR3_DQ<31>	DDR3_DQS_DN<4>	B10	M_T_DQS_DN<4>	4
		30	M_T_DQ<30>	N27	DDR3_DQ<30>	DDR3_DQS_DN<3>	P28	M_T_DQS_DN<3>	3
		29	M_T_DQ<29>	K32	DDR3_DQ<29>	DDR3_DQS_DN<2>	G33	M_T_DQS_DN<2>	2
		28	M_T_DQ<28>	L33	DDR3_DQ<28>	DDR3_DQS_DN<1>	L37	M_T_DQS_DN<1>	1
		27	M_T_DQ<27>	L27	DDR3_DQ<27>	DDR3_DQS_DN<0>	B38	M_T_DQS_DN<0>	0
		26	M_T_DQ<26>	M28	DDR3_DQ<26>				
		25	M_T_DQ<25>	L31	DDR3_DQ<25>	DDR3_MA<15>	F24	M_T_MA<15>	15
		24	M_T_DQ<24>	M32	DDR3_DQ<24>	DDR3_MA<14>	D24	M_T_MA<14>	14
		23	M_T_DQ<23>	B32	DDR3_DQ<23>	DDR3_MA<13>	A13	M_T_MA<13>	13
		22	M_T_DQ<22>	A33	DDR3_DQ<22>	DDR3_MA<12>	E23	M_T_MA<12>	12
		21	M_T_DQ<21>	C35	DDR3_DQ<21>	DDR3_MA<11>	A23	M_T_MA<11>	11
		20	M_T_DQ<20>	E35	DDR3_DQ<20>	DDR3_MA<10>	D18	M_T_MA<10>	10
		19	M_T_DQ<19>	F32	DDR3_DQ<19>	DDR3_MA<9>	G23	M_T_MA<9>	9
		18	M_T_DQ<18>	D32	DDR3_DQ<18>	DDR3_MA<8>	D22	M_T_MA<8>	8
		17	M_T_DQ<17>	F34	DDR3_DQ<17>	DDR3_MA<7>	B22	M_T_MA<7>	7
		16	M_T_DQ<16>	A35	DDR3_DQ<16>	DDR3_MA<6>	F22	M_T_MA<6>	6
		15	M_T_DQ<15>	H36	DDR3_DQ<15>	DDR3_MA<5>	A21	M_T_MA<5>	5
		14	M_T_DQ<14>	K36	DDR3_DQ<14>	DDR3_MA<4>	D20	M_T_MA<4>	4
		13	M_T_DQ<13>	K40	DDR3_DQ<13>	DDR3_MA<3>	B20	M_T_MA<3>	3
		12	M_T_DQ<12>	M40	DDR3_DQ<12>	DDR3_MA<2>	F20	M_T_MA<2>	2
		11	M_T_DQ<11>	J35	DDR3_DQ<11>	DDR3_MA<1>	E21	M_T_MA<1>	1
		10	M_T_DQ<10>	L35	DDR3_DQ<10>	DDR3_MA<0>	A19	M_T_MA<0>	0
		9	M_T_DQ<9>	L39	DDR3_DQ<9>				
		8	M_T_DQ<8>	N39	DDR3_DQ<8>	DDR3_ECC<7>	H26	M_T_ECC<7>	7
		7	M_T_DQ<7>	A37	DDR3_DQ<7>	DDR3_ECC<6>	F26	M_T_ECC<6>	6
		6	M_T_DQ<6>	F38	DDR3_DQ<6>	DDR3_ECC<5>	H30	M_T_ECC<5>	5
		5	M_T_DQ<5>	D40	DDR3_DQ<5>	DDR3_ECC<4>	F30	M_T_ECC<4>	4
		4	M_T_DQ<4>	F40	DDR3_DQ<4>	DDR3_ECC<3>	C25	M_T_ECC<3>	3
		3	M_T_DQ<3>	E37	DDR3_DQ<3>	DDR3_ECC<2>	E25	M_T_ECC<2>	2
		2	M_T_DQ<2>	C37	DDR3_DQ<2>	DDR3_ECC<1>	J29	M_T_ECC<1>	1
		1	M_T_DQ<1>	A39	DDR3_DQ<1>	DDR3_ECC<0>	G29	M_T_ECC<0>	0
		0	M_T_DQ<0>	B40	DDR3_DQ<0>				
			NC_M_T_CS_N<9>	K16	DDR3_CS_N<9>	DDR3_CKE<5>	R27	NC_M_T_CKE<5>	
			NC_M_T_CS_N<8>	D16	DDR3_CS_N<8>	DDR3_CKE<4>	R25	NC_M_T_CKE<4>	
			NC_M_T_CS_N<7>	E15	DDR3_CS_N<7>	DDR3_CKE<3>	N25	NC_M_T_CKE<3>	
			NC_M_T_CS_N<6>	F16	DDR3_CS_N<6>	DDR3_CKE<2>	J25	NC_M_T_CKE<2>	
			NC_M_T_CS_N<5>	G17	DDR3_CS_N<5>	DDR3_CKE<1>	M24	M_T_CKE<1>	1
			NC_M_T_CS_N<4>	K18	DDR3_CS_N<4>	DDR3_CKE<0>	K24	M_T_CKE<0>	0
118< OUT	M_T_CS_N<3..0>	3	M_T_CS_N<3>	G15	DDR3_CS_N<3>	DDR3_BA<2>	B24	M_T_BA<2>	2
		2	M_T_CS_N<2>	F14	DDR3_CS_N<2>	DDR3_BA<1>	E19	M_T_BA<1>	1
		1	M_T_CS_N<1>	J19	DDR3_CS_N<1>	DDR3_BA<0>	A17	M_T_BA<0>	0
		0	M_T_CS_N<0>	G19	DDR3_CS_N<0>				
			NC_M_T_CK_DP<3>	M22	DDR3_CLK_DP<3>	DDR3_ODT<5>	M16	NC_M_T_ODT<5>	
118< OUT			M_T_CK_DP<2>	K20	DDR3_CLK_DP<2>	DDR3_ODT<4>	D14	NC_M_T_ODT<4>	
			NC_M_T_CK_DP<1>	L21	DDR3_CLK_DP<1>	DDR3_ODT<3>	J17	NC_M_T_ODT<3>	
118< OUT			M_T_CK_DP<0>	L23	DDR3_CLK_DP<0>	DDR3_ODT<2>	E17	NC_M_T_ODT<2>	
						DDR3_ODT<1>	F18	M_T_ODT<1>	1
			NC_M_T_CK_DN<3>	K22	DDR3_CLK_DN<3>	DDR3_ODT<0>	L19	M_T_ODT<0>	0
118< OUT			M_T_CK_DN<2>	M20	DDR3_CLK_DN<2>	DDR3_WE_N	A15	M_T_WE_N	
			NC_M_T_CK_DN<1>	J21	DDR3_CLK_DN<1>	DDR3_RAS_N	B16	M_T_RAS_N	
118< OUT			M_T_CK_DN<0>	J23	DDR3_CLK_DN<0>	DDR3_PAR_ERR_N	G21	M_T_PAR_ERR_N<0>	
						DDR3_CAS_N	B14	M_T_CAS_N	
						DDR3_MA_PAR	B18	M_T_MA_PAR	

M_T_DQS_DP<17..0> — 118<> BI

M_T_DQS_DN<17..0> — 118<> BI

M_T_MA<15..0> — 118< OUT

M_T_ECC<7..0> — 118<> BI

M_T_CKE<1..0> — 118< OUT

M_T_BA<2..0> — 118< OUT

M_T_ODT<1..0> — 118< OUT

M_T_WE_N — 118< OUT

M_T_RAS_N — 118< OUT

M_T_PAR_ERR_N<0> — 118> IN

M_T_CAS_N — 118< OUT

M_T_MA_PAR — 118< OUT

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CPU SOCKET 3 (5 OF 13)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 106 OF 303	

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SANDYBRIDGE_EP_EXT_D

TP_P3E_CPU3_RX_PE1A_DP<3>	E55	PE1A_RX_DP<3>	PE1A_TX_DP<3>	J45	TP_P3E_CPU3_TX_PE1A_DP<3>
TP_P3E_CPU3_RX_PE1A_DP<2>	D54	PE1A_RX_DP<2>	PE1A_TX_DP<2>	H44	TP_P3E_CPU3_TX_PE1A_DP<2>
TP_P3E_CPU3_RX_PE1A_DP<1>	D52	PE1A_RX_DP<1>	PE1A_TX_DP<1>	J43	TP_P3E_CPU3_TX_PE1A_DP<1>
TP_P3E_CPU3_RX_PE1A_DP<0>	C51	PE1A_RX_DP<0>	PE1A_TX_DP<0>	H42	TP_P3E_CPU3_TX_PE1A_DP<0>
TP_P3E_CPU3_RX_PE1A_DN<3>	G55	PE1A_RX_DN<3>	PE1A_TX_DN<3>	L45	TP_P3E_CPU3_TX_PE1A_DN<3>
TP_P3E_CPU3_RX_PE1A_DN<2>	F54	PE1A_RX_DN<2>	PE1A_TX_DN<2>	K44	TP_P3E_CPU3_TX_PE1A_DN<2>
TP_P3E_CPU3_RX_PE1A_DN<1>	F52	PE1A_RX_DN<1>	PE1A_TX_DN<1>	L43	TP_P3E_CPU3_TX_PE1A_DN<1>
TP_P3E_CPU3_RX_PE1A_DN<0>	E51	PE1A_RX_DN<0>	PE1A_TX_DN<0>	K42	TP_P3E_CPU3_TX_PE1A_DN<0>
TP_P3E_CPU3_RX_PE1B_DP<3>	K56	PE1B_RX_DP<7>	PE1B_TX_DP<7>	J49	TP_P3E_CPU3_TX_PE1B_DP<3>
TP_P3E_CPU3_RX_PE1B_DP<2>	J57	PE1B_RX_DP<6>	PE1B_TX_DP<6>	H48	TP_P3E_CPU3_TX_PE1B_DP<2>
TP_P3E_CPU3_RX_PE1B_DP<1>	K54	PE1B_RX_DP<5>	PE1B_TX_DP<5>	J47	TP_P3E_CPU3_TX_PE1B_DP<1>
TP_P3E_CPU3_RX_PE1B_DP<0>	J53	PE1B_RX_DP<4>	PE1B_TX_DP<4>	H46	TP_P3E_CPU3_TX_PE1B_DP<0>
TP_P3E_CPU3_RX_PE1B_DN<3>	M56	PE1B_RX_DN<7>	PE1B_TX_DN<7>	L49	TP_P3E_CPU3_TX_PE1B_DN<3>
TP_P3E_CPU3_RX_PE1B_DN<2>	L57	PE1B_RX_DN<6>	PE1B_TX_DN<6>	K48	TP_P3E_CPU3_TX_PE1B_DN<2>
TP_P3E_CPU3_RX_PE1B_DN<1>	M54	PE1B_RX_DN<5>	PE1B_TX_DN<5>	L47	TP_P3E_CPU3_TX_PE1B_DN<1>
TP_P3E_CPU3_RX_PE1B_DN<0>	L53	PE1B_RX_DN<4>	PE1B_TX_DN<4>	K46	TP_P3E_CPU3_TX_PE1B_DN<0>
TP_P3E_CPU3_RX_PE2A_DP<3>	U55	PE2A_RX_DP<3>	PE2A_TX_DP<3>	AM52	TP_P3E_CPU3_TX_PE2A_DP<3>
TP_P3E_CPU3_RX_PE2A_DP<2>	T56	PE2A_RX_DP<2>	PE2A_TX_DP<2>	AN51	TP_P3E_CPU3_TX_PE2A_DP<2>
TP_P3E_CPU3_RX_PE2A_DP<1>	T54	PE2A_RX_DP<1>	PE2A_TX_DP<1>	AM50	TP_P3E_CPU3_TX_PE2A_DP<1>
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TP_P3E_CPU3_RX_PE2B_DP<3>	AE57	PE2B_RX_DP<7>	PE2B_TX_DP<7>	AP54	TP_P3E_CPU3_TX_PE2B_DP<3>
TP_P3E_CPU3_RX_PE2B_DP<2>	AC55	PE2B_RX_DP<6>	PE2B_TX_DP<6>	AN53	TP_P3E_CPU3_TX_PE2B_DP<2>
TP_P3E_CPU3_RX_PE2B_DP<1>	AB56	PE2B_RX_DP<5>	PE2B_TX_DP<5>	AH54	TP_P3E_CPU3_TX_PE2B_DP<1>
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TP_P3E_CPU3_RX_PE2B_DN<3>	AF58	PE2B_RX_DN<7>	PE2B_TX_DN<7>	AT54	TP_P3E_CPU3_TX_PE2B_DN<3>
TP_P3E_CPU3_RX_PE2B_DN<2>	AE55	PE2B_RX_DN<6>	PE2B_TX_DN<6>	AR53	TP_P3E_CPU3_TX_PE2B_DN<2>
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TP_P3E_CPU3_RX_PE2C_DP<3>	AR57	PE2C_RX_DP<11>	PE2C_TX_DP<11>	AW51	TP_P3E_CPU3_TX_PE2C_DP<3>
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TP_P3E_CPU3_RX_PE2C_DN<2>	AL57	PE2C_RX_DN<10>	PE2C_TX_DN<10>	BB54	TP_P3E_CPU3_TX_PE2C_DN<2>
TP_P3E_CPU3_RX_PE2C_DN<1>	AM58	PE2C_RX_DN<9>	PE2C_TX_DN<9>	BA53	TP_P3E_CPU3_TX_PE2C_DN<1>
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CPU SOCKET 3 (6 OF 13)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 107 OF 303	

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SANDYBRIDGE_EP_EXT_D

TP_P3E_CPU3_RX_PE2D_DP<3>	AY56	PE2D_RX_DP<15>	PE2D_TX_DP<15>	AW47	TP_P3E_CPU3_TX_PE2D_DP<3>
TP_P3E_CPU3_RX_PE2D_DP<2>	AY58	PE2D_RX_DP<14>	PE2D_TX_DP<14>	AV48	TP_P3E_CPU3_TX_PE2D_DP<2>
TP_P3E_CPU3_RX_PE2D_DP<1>	AP56	PE2D_RX_DP<13>	PE2D_TX_DP<13>	AW49	TP_P3E_CPU3_TX_PE2D_DP<1>
TP_P3E_CPU3_RX_PE2D_DP<0>	AT58	PE2D_RX_DP<12>	PE2D_TX_DP<12>	AV50	TP_P3E_CPU3_TX_PE2D_DP<0>
TP_P3E_CPU3_RX_PE2D_DN<3>	BB56	PE2D_RX_DN<15>	PE2D_TX_DN<15>	BA47	TP_P3E_CPU3_TX_PE2D_DN<3>
TP_P3E_CPU3_RX_PE2D_DN<2>	BA57	PE2D_RX_DN<14>	PE2D_TX_DN<14>	AY48	TP_P3E_CPU3_TX_PE2D_DN<2>
TP_P3E_CPU3_RX_PE2D_DN<1>	AT56	PE2D_RX_DN<13>	PE2D_TX_DN<13>	BA49	TP_P3E_CPU3_TX_PE2D_DN<1>
TP_P3E_CPU3_RX_PE2D_DN<0>	AV58	PE2D_RX_DN<12>	PE2D_TX_DN<12>	AY50	TP_P3E_CPU3_TX_PE2D_DN<0>
TP_P3E_CPU3_RX_PE3A_DP<3>	AA49	PE3A_RX_DP<3>	PE3A_TX_DP<3>	P48	TP_P3E_CPU3_TX_PE3A_DP<3>
TP_P3E_CPU3_RX_PE3A_DP<2>	AF46	PE3A_RX_DP<2>	PE3A_TX_DP<2>	R47	TP_P3E_CPU3_TX_PE3A_DP<2>
TP_P3E_CPU3_RX_PE3A_DP<1>	AG45	PE3A_RX_DP<1>	PE3A_TX_DP<1>	J51	TP_P3E_CPU3_TX_PE3A_DP<1>
TP_P3E_CPU3_RX_PE3A_DP<0>	AF44	PE3A_RX_DP<0>	PE3A_TX_DP<0>	H50	TP_P3E_CPU3_TX_PE3A_DP<0>
TP_P3E_CPU3_RX_PE3A_DN<3>	AC49	PE3A_RX_DN<3>	PE3A_TX_DN<3>	T48	TP_P3E_CPU3_TX_PE3A_DN<3>
TP_P3E_CPU3_RX_PE3A_DN<2>	AH46	PE3A_RX_DN<2>	PE3A_TX_DN<2>	U47	TP_P3E_CPU3_TX_PE3A_DN<2>
TP_P3E_CPU3_RX_PE3A_DN<1>	AJ45	PE3A_RX_DN<1>	PE3A_TX_DN<1>	L51	TP_P3E_CPU3_TX_PE3A_DN<1>
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TP_P3E_CPU3_RX_PE3B_DP<2>	AA53	PE3B_RX_DP<6>	PE3B_TX_DP<6>	P50	TP_P3E_CPU3_TX_PE3B_DP<2>
TP_P3E_CPU3_RX_PE3B_DP<1>	Y52	PE3B_RX_DP<5>	PE3B_TX_DP<5>	R51	TP_P3E_CPU3_TX_PE3B_DP<1>
TP_P3E_CPU3_RX_PE3B_DP<0>	Y50	PE3B_RX_DP<4>	PE3B_TX_DP<4>	P52	TP_P3E_CPU3_TX_PE3B_DP<0>
TP_P3E_CPU3_RX_PE3B_DN<3>	AC51	PE3B_RX_DN<7>	PE3B_TX_DN<7>	U49	TP_P3E_CPU3_TX_PE3B_DN<3>
TP_P3E_CPU3_RX_PE3B_DN<2>	AC53	PE3B_RX_DN<6>	PE3B_TX_DN<6>	T50	TP_P3E_CPU3_TX_PE3B_DN<2>
TP_P3E_CPU3_RX_PE3B_DN<1>	AB52	PE3B_RX_DN<5>	PE3B_TX_DN<5>	U51	TP_P3E_CPU3_TX_PE3B_DN<1>
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TP_P3E_CPU3_RX_PE3C_DP<3>	AG49	PE3C_RX_DP<11>	PE3C_TX_DP<11>	Y46	TP_P3E_CPU3_TX_PE3C_DP<3>
TP_P3E_CPU3_RX_PE3C_DP<2>	AF50	PE3C_RX_DP<10>	PE3C_TX_DP<10>	R45	TP_P3E_CPU3_TX_PE3C_DP<2>
TP_P3E_CPU3_RX_PE3C_DP<1>	AG51	PE3C_RX_DP<9>	PE3C_TX_DP<9>	AA47	TP_P3E_CPU3_TX_PE3C_DP<1>
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TP_P3E_CPU3_RX_PE3C_DN<3>	AJ49	PE3C_RX_DN<11>	PE3C_TX_DN<11>	AB46	TP_P3E_CPU3_TX_PE3C_DN<3>
TP_P3E_CPU3_RX_PE3C_DN<2>	AH50	PE3C_RX_DN<10>	PE3C_TX_DN<10>	U45	TP_P3E_CPU3_TX_PE3C_DN<2>
TP_P3E_CPU3_RX_PE3C_DN<1>	AJ51	PE3C_RX_DN<9>	PE3C_TX_DN<9>	AC47	TP_P3E_CPU3_TX_PE3C_DN<1>
TP_P3E_CPU3_RX_PE3C_DN<0>	AH48	PE3C_RX_DN<8>	PE3C_TX_DN<8>	T46	TP_P3E_CPU3_TX_PE3C_DN<0>
TP_P3E_CPU3_RX_PE3D_DP<3>	AN45	PE3D_RX_DP<15>	PE3D_TX_DP<15>	T44	TP_P3E_CPU3_TX_PE3D_DP<3>
TP_P3E_CPU3_RX_PE3D_DP<2>	AM46	PE3D_RX_DP<14>	PE3D_TX_DP<14>	AC43	TP_P3E_CPU3_TX_PE3D_DP<2>
TP_P3E_CPU3_RX_PE3D_DP<1>	AN47	PE3D_RX_DP<13>	PE3D_TX_DP<13>	Y44	TP_P3E_CPU3_TX_PE3D_DP<1>
TP_P3E_CPU3_RX_PE3D_DP<0>	AG47	PE3D_RX_DP<12>	PE3D_TX_DP<12>	AA45	TP_P3E_CPU3_TX_PE3D_DP<0>
TP_P3E_CPU3_RX_PE3D_DN<3>	AR45	PE3D_RX_DN<15>	PE3D_TX_DN<15>	P44	TP_P3E_CPU3_TX_PE3D_DN<3>
TP_P3E_CPU3_RX_PE3D_DN<2>	AP46	PE3D_RX_DN<14>	PE3D_TX_DN<14>	AA43	TP_P3E_CPU3_TX_PE3D_DN<2>
TP_P3E_CPU3_RX_PE3D_DN<1>	AR47	PE3D_RX_DN<13>	PE3D_TX_DN<13>	AB44	TP_P3E_CPU3_TX_PE3D_DN<1>
TP_P3E_CPU3_RX_PE3D_DN<0>	AJ47	PE3D_RX_DN<12>	PE3D_TX_DN<12>	AC45	TP_P3E_CPU3_TX_PE3D_DN<0>

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CPU SOCKET 3 (7 OF 13)

DEPARTMENT: DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	SIZE: B	CODE: 34649	DOCUMENT NUMBER: 444359 / REV: 1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 108 OF 303

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IC

SANDYBRIDGE_EP_EXT_D

131< IN XDP_CPU3_MBP_N<7..0>

7	XDP_CPU3_MBP_N<7>	AY44	BPM_N<7>
6	XDP_CPU3_MBP_N<6>	BA43	BPM_N<6>
5	XDP_CPU3_MBP_N<5>	AW43	BPM_N<5>
4	XDP_CPU3_MBP_N<4>	BB44	BPM_N<4>
3	XDP_CPU3_MBP_N<3>	AV44	BPM_N<3>
2	XDP_CPU3_MBP_N<2>	AU43	BPM_N<2>
1	XDP_CPU3_MBP_N<1>	AT44	BPM_N<1>
0	XDP_CPU3_MBP_N<0>	AR43	BPM_N<0>

CAD NOTE: PLACE CLOSE TO CPU

R5R18
1 2
36.0 A93549-074
1/16W 5% 0402LF
SOCKET3

86<> 63<> 40<> 40> BI FM_CPU_ONLY_RESET — FM_CPU3_ONLY_RESET_R AN43 — CPU_ONLY_RESET

NC_CPU3_RSVD<16>	A53	RSVD<16>
NC_CPU3_RSVD<14>	C53	RSVD<14>
NC_CPU3_RSVD<15>	B46	RSVD<15>
NC_CPU3_RSVD<13>	D46	RSVD<13>
NC_CPU3_RSVD<3>	K58	RSVD<3>
NC_CPU3_RSVD<60>	AY46	RSVD<60>
NC_CPU3_RSVD<61>	AV46	RSVD<61>
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NC_CPU3_RSVD<66>	AJ55	RSVD<66>
NC_CPU3_RSVD<55>	BD48	RSVD<55>

TP_DMI_CPU3_RX_DP<3>	B50	DMI_RX_DP<3>
TP_DMI_CPU3_RX_DP<2>	C49	DMI_RX_DP<2>
TP_DMI_CPU3_RX_DP<1>	B48	DMI_RX_DP<1>
TP_DMI_CPU3_RX_DP<0>	C47	DMI_RX_DP<0>
TP_DMI_CPU3_RX_DN<3>	D50	DMI_RX_DN<3>
TP_DMI_CPU3_RX_DN<2>	E49	DMI_RX_DN<2>
TP_DMI_CPU3_RX_DN<1>	D48	DMI_RX_DN<1>
TP_DMI_CPU3_RX_DN<0>	E47	DMI_RX_DN<0>

53< OUT PD_CPU3_TEST<3..0>

3	PD_CPU3_TEST<3>	D4	TEST3
2	PD_CPU3_TEST<2>	F2	TEST2
1	PD_CPU3_TEST<1>	CW1	TEST1
0	PD_CPU3_TEST<0>	DB4	TEST0

53> IN A_CPU3_DDR23_RCOMP<2..0>
53> IN A_CPU3_DDR01_RCOMP<2..0>

2	A_CPU3_DDR23_RCOMP<2>	Y14	DDR23_RCOMP<2>
1	A_CPU3_DDR23_RCOMP<1>	AC15	DDR23_RCOMP<1>
0	A_CPU3_DDR23_RCOMP<0>	U15	DDR23_RCOMP<0>
2	A_CPU3_DDR01_RCOMP<2>	CB20	DDR01_RCOMP<2>
1	A_CPU3_DDR01_RCOMP<1>	CC19	DDR01_RCOMP<1>
0	A_CPU3_DDR01_RCOMP<0>	CA17	DDR01_RCOMP<0>

86> 78< 63> 40> OUT FM_CPU_ERR_N<2..0>

2	FM_CPU_ERR_N<2>	BC51	ERROR_N<2>
1	FM_CPU_ERR_N<1>	CB54	ERROR_N<1>
0	FM_CPU_ERR_N<0>	BD50	ERROR_N<0>

RSVD<45>	BJ45	NC_CPU3_RSVD<45>
RSVD<38>	BP44	NC_CPU3_RSVD<38>
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RSVD<42>	BL45	NC_CPU3_RSVD<42>
RSVD<47>	BH46	NC_CPU3_RSVD<47>
RSVD<44>	BK44	NC_CPU3_RSVD<44>
RSVD<53>	BE45	NC_CPU3_RSVD<53>
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RSVD<57>	BD44	NC_CPU3_RSVD<57>
RSVD<56>	BD46	NC_CPU3_RSVD<56>
RSVD<51>	BF46	NC_CPU3_RSVD<51>
RSVD<36>	BR43	NC_CPU3_RSVD<36>
RSVD<43>	BL43	NC_CPU3_RSVD<43>
RSVD<33>	BU43	NC_CPU3_RSVD<33>
RSVD<50>	BG43	NC_CPU3_RSVD<50>
RSVD<41>	BM44	NC_CPU3_RSVD<41>
RSVD<46>	BJ43	NC_CPU3_RSVD<46>
RSVD<54>	BE43	NC_CPU3_RSVD<54>

DMI_TX_DP<3>	C45	TP_DMI_CPU3_TX_DP<3>
DMI_TX_DP<2>	B44	TP_DMI_CPU3_TX_DP<2>
DMI_TX_DP<1>	C43	TP_DMI_CPU3_TX_DP<1>
DMI_TX_DP<0>	B42	TP_DMI_CPU3_TX_DP<0>
DMI_TX_DN<3>	E45	TP_DMI_CPU3_TX_DN<3>
DMI_TX_DN<2>	D44	TP_DMI_CPU3_TX_DN<2>
DMI_TX_DN<1>	E43	TP_DMI_CPU3_TX_DN<1>
DMI_TX_DN<0>	D42	TP_DMI_CPU3_TX_DN<0>

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RSVD<11>	E53	NC_CPU3_RSVD<11>
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RSVD<52>	BE47	NC_CPU3_RSVD<52>
RSVD<0>	Y48	NC_CPU3_RSVD<0>
RSVD<2>	M48	NC_CPU3_RSVD<2>
RSVD<4>	J15	NC_CPU3_RSVD<4>
RSVD<6>	H56	NC_CPU3_RSVD<6>
RSVD<9>	F46	NC_CPU3_RSVD<9>
RSVD<27>	CG11	NC_CPU3_RSVD<27>
RSVD<28>	CF44	NC_CPU3_RSVD<28>
RSVD<29>	CE43	NC_CPU3_RSVD<29>
RSVD<30>	CD44	NC_CPU3_RSVD<30>
RSVD<1>	W15	NC_CPU3_RSVD<1>
RSVD<35>	BR47	NC_CPU3_RSVD<35>
RSVD<39>	BN47	NC_CPU3_RSVD<39>
RSVD<26>	CP54	NC_CPU3_RSVD<26>
RSVD<58>	BC47	NC_CPU3_RSVD<58>
RSVD<67>	AB48	NC_CPU3_RSVD<67>

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CPU SOCKET 3 (8 OF 13)

DEPARTMENT: DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	SIZE: B	CODE: 34649	DOCUMENT NUMBER: 444359 / REV: 1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 109 OF 303

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NOTE: QPI P0 RX NETS WITH LANE REVERSAL
NOTE: POLARITY INVERSION ON LANES 0,1,2,3,5,8,10,11,12,13,14,15,16,17,18,19

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IC
SANDYBRIDGE_EP_EXT_D

88> IN QPI_CPU2_CPU3_P1P0_DP<19..0>
88> IN QPI_CPU2_CPU3_P1P0_DN<19..0>

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1	QPI_CPU2_CPU3_P1P0_DN<1>	BR49	QPI0_DRX_DP<18>	QPI0_DTX_DP<18>	CE51	QPI_CPU3_CPU2_P0P1_DP<18>	18		
2	QPI_CPU2_CPU3_P1P0_DN<2>	BG49	QPI0_DRX_DP<17>	QPI0_DTX_DP<17>	CD52	QPI_CPU3_CPU2_P0P1_DP<17>	17		
3	QPI_CPU2_CPU3_P1P0_DN<3>	BM50	QPI0_DRX_DP<16>	QPI0_DTX_DP<16>	CD50	QPI_CPU3_CPU2_P0P1_DP<16>	16		
4	QPI_CPU2_CPU3_P1P0_DP<4>	BN51	QPI0_DRX_DP<15>	QPI0_DTX_DP<15>	CD48	QPI_CPU3_CPU2_P0P1_DP<15>	15		
5	QPI_CPU2_CPU3_P1P0_DN<5>	BM52	QPI0_DRX_DP<14>	QPI0_DTX_DP<14>	CE47	QPI_CPU3_CPU2_P0P1_DP<14>	14		
6	QPI_CPU2_CPU3_P1P0_DP<6>	BL53	QPI0_DRX_DP<13>	QPI0_DTX_DP<13>	BY50	QPI_CPU3_CPU2_P0P1_DP<13>	13		
7	QPI_CPU2_CPU3_P1P0_DP<7>	BM54	QPI0_DRX_DP<12>	QPI0_DTX_DP<12>	BY48	QPI_CPU3_CPU2_P0P1_DP<12>	12		
8	QPI_CPU2_CPU3_P1P0_DN<8>	BL55	QPI0_DRX_DP<11>	QPI0_DTX_DP<11>	CA51	QPI_CPU3_CPU2_P0P1_DP<11>	11		
9	QPI_CPU2_CPU3_P1P0_DP<9>	BM56	QPI0_DRX_DP<10>	QPI0_DTX_DP<10>	CD46	QPI_CPU3_CPU2_P0P1_DP<10>	10		
10	QPI_CPU2_CPU3_P1P0_DN<10>	BL57	QPI0_DRX_DP<9>	QPI0_DTX_DP<9>	BV46	QPI_CPU3_CPU2_P0P1_DP<9>	9		
11	QPI_CPU2_CPU3_P1P0_DN<11>	BE57	QPI0_DRX_DP<8>	QPI0_DTX_DP<8>	BV56	QPI_CPU3_CPU2_P0P1_DP<8>	8		
12	QPI_CPU2_CPU3_P1P0_DN<12>	BD58	QPI0_DRX_DP<7>	QPI0_DTX_DP<7>	BU57	QPI_CPU3_CPU2_P0P1_DP<7>	7		
13	QPI_CPU2_CPU3_P1P0_DN<13>	BF50	QPI0_DRX_DP<6>	QPI0_DTX_DP<6>	BV48	QPI_CPU3_CPU2_P0P1_DP<6>	6		
14	QPI_CPU2_CPU3_P1P0_DN<14>	BF54	QPI0_DRX_DP<5>	QPI0_DTX_DP<5>	BT58	QPI_CPU3_CPU2_P0P1_DP<5>	5		
15	QPI_CPU2_CPU3_P1P0_DN<15>	BF56	QPI0_DRX_DP<4>	QPI0_DTX_DP<4>	BU55	QPI_CPU3_CPU2_P0P1_DP<4>	4		
16	QPI_CPU2_CPU3_P1P0_DN<16>	BE55	QPI0_DRX_DP<3>	QPI0_DTX_DP<3>	BV54	QPI_CPU3_CPU2_P0P1_DP<3>	3		
17	QPI_CPU2_CPU3_P1P0_DN<17>	BE53	QPI0_DRX_DP<2>	QPI0_DTX_DP<2>	BU53	QPI_CPU3_CPU2_P0P1_DP<2>	2		
18	QPI_CPU2_CPU3_P1P0_DN<18>	BF52	QPI0_DRX_DP<1>	QPI0_DTX_DP<1>	BV52	QPI_CPU3_CPU2_P0P1_DP<1>	1		
19	QPI_CPU2_CPU3_P1P0_DN<19>	BG51	QPI0_DRX_DP<0>	QPI0_DTX_DP<0>	BV50	QPI_CPU3_CPU2_P0P1_DP<0>	0		
0	QPI_CPU2_CPU3_P1P0_DP<0>	BM48	QPI0_DRX_DN<19>	QPI0_DTX_DN<19>	CG49	QPI_CPU3_CPU2_P0P1_DN<19>	19	QPI_CPU3_CPU2_P0P1_DN<19..0>	OUT 88<
1	QPI_CPU2_CPU3_P1P0_DP<1>	BN49	QPI0_DRX_DN<18>	QPI0_DTX_DN<18>	CG51	QPI_CPU3_CPU2_P0P1_DN<18>	18		
2	QPI_CPU2_CPU3_P1P0_DP<2>	BJ49	QPI0_DRX_DN<17>	QPI0_DTX_DN<17>	CF52	QPI_CPU3_CPU2_P0P1_DN<17>	17		
3	QPI_CPU2_CPU3_P1P0_DP<3>	BP50	QPI0_DRX_DN<16>	QPI0_DTX_DN<16>	CF50	QPI_CPU3_CPU2_P0P1_DN<16>	16		
4	QPI_CPU2_CPU3_P1P0_DN<4>	BR51	QPI0_DRX_DN<15>	QPI0_DTX_DN<15>	CF48	QPI_CPU3_CPU2_P0P1_DN<15>	15		
5	QPI_CPU2_CPU3_P1P0_DP<5>	BP52	QPI0_DRX_DN<14>	QPI0_DTX_DN<14>	CG47	QPI_CPU3_CPU2_P0P1_DN<14>	14		
6	QPI_CPU2_CPU3_P1P0_DN<6>	BN53	QPI0_DRX_DN<13>	QPI0_DTX_DN<13>	CA49	QPI_CPU3_CPU2_P0P1_DN<13>	13		
7	QPI_CPU2_CPU3_P1P0_DN<7>	BP54	QPI0_DRX_DN<12>	QPI0_DTX_DN<12>	CA47	QPI_CPU3_CPU2_P0P1_DN<12>	12		
8	QPI_CPU2_CPU3_P1P0_DP<8>	BN55	QPI0_DRX_DN<11>	QPI0_DTX_DN<11>	BY52	QPI_CPU3_CPU2_P0P1_DN<11>	11		
9	QPI_CPU2_CPU3_P1P0_DN<9>	BP56	QPI0_DRX_DN<10>	QPI0_DTX_DN<10>	CF46	QPI_CPU3_CPU2_P0P1_DN<10>	10		
10	QPI_CPU2_CPU3_P1P0_DP<10>	BN57	QPI0_DRX_DN<9>	QPI0_DTX_DN<9>	BW45	QPI_CPU3_CPU2_P0P1_DN<9>	9		
11	QPI_CPU2_CPU3_P1P0_DP<11>	BG57	QPI0_DRX_DN<8>	QPI0_DTX_DN<8>	BY56	QPI_CPU3_CPU2_P0P1_DN<8>	8		
12	QPI_CPU2_CPU3_P1P0_DP<12>	BF58	QPI0_DRX_DN<7>	QPI0_DTX_DN<7>	BW57	QPI_CPU3_CPU2_P0P1_DN<7>	7		
13	QPI_CPU2_CPU3_P1P0_DP<13>	BH50	QPI0_DRX_DN<6>	QPI0_DTX_DN<6>	BW47	QPI_CPU3_CPU2_P0P1_DN<6>	6		
14	QPI_CPU2_CPU3_P1P0_DP<14>	BH54	QPI0_DRX_DN<5>	QPI0_DTX_DN<5>	BV58	QPI_CPU3_CPU2_P0P1_DN<5>	5		
15	QPI_CPU2_CPU3_P1P0_DP<15>	BH56	QPI0_DRX_DN<4>	QPI0_DTX_DN<4>	BW55	QPI_CPU3_CPU2_P0P1_DN<4>	4		
16	QPI_CPU2_CPU3_P1P0_DP<16>	BG55	QPI0_DRX_DN<3>	QPI0_DTX_DN<3>	BY54	QPI_CPU3_CPU2_P0P1_DN<3>	3		
17	QPI_CPU2_CPU3_P1P0_DP<17>	BG53	QPI0_DRX_DN<2>	QPI0_DTX_DN<2>	BW53	QPI_CPU3_CPU2_P0P1_DN<2>	2		
18	QPI_CPU2_CPU3_P1P0_DP<18>	BH52	QPI0_DRX_DN<1>	QPI0_DTX_DN<1>	BW51	QPI_CPU3_CPU2_P0P1_DN<1>	1		
19	QPI_CPU2_CPU3_P1P0_DP<19>	BJ51	QPI0_DRX_DN<0>	QPI0_DTX_DN<0>	BW49	QPI_CPU3_CPU2_P0P1_DN<0>	0		
88> IN	QPI_CPU2_CPU3_P1P0_CLKA_DP	BK58	QPI0_CLKRX_DP	QPI0_CLKTX_DP	CE45	QPI_CPU3_CPU2_P0P1_CLKA_DP			OUT 88<
88> IN	QPI_CPU2_CPU3_P1P0_CLKA_DN	BM58	QPI0_CLKRX_DN	QPI0_CLKTX_DN	CG45	QPI_CPU3_CPU2_P0P1_CLKA_DN			OUT 88<

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CPU SOCKET 3 (9 OF 13)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 110 OF 303	

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NOTE: QPI P1 RX NETS WITH LANE REVERSAL

NOTE: POLARITY INVERSION ON LANES 4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19

U6C1
IC

SANDYBRIDGE_EP_EXT_D

41> IN	QPI_CPU0_CPU3_P0P1_DP<19..0>										
41> IN	QPI_CPU0_CPU3_P0P1_DN<19..0>										
0	QPI_CPU0_CPU3_P0P1_DP<0>	CL45	QPI1_DRX_DP<19>	QPI1_DTX_DP<19>	DB42	QPI_CPU3_CPU0_P1P0_DP<19>	19	QPI_CPU3_CPU0_P1P0_DP<19..0>	OUT	41<
1	QPI_CPU0_CPU3_P0P1_DP<1>	CK46	QPI1_DRX_DP<18>	QPI1_DTX_DP<18>	DE43	QPI_CPU3_CPU0_P1P0_DP<18>	18			
2	QPI_CPU0_CPU3_P0P1_DP<2>	CL47	QPI1_DRX_DP<17>	QPI1_DTX_DP<17>	CU43	QPI_CPU3_CPU0_P1P0_DP<17>	17			
3	QPI_CPU0_CPU3_P0P1_DP<3>	CK48	QPI1_DRX_DP<16>	QPI1_DTX_DP<16>	DB44	QPI_CPU3_CPU0_P1P0_DP<16>	16			
4	QPI_CPU0_CPU3_P0P1_DP<4>	CN49	QPI1_DRX_DP<15>	QPI1_DTX_DP<15>	DE45	QPI_CPU3_CPU0_P1P0_DP<15>	15			
5	QPI_CPU0_CPU3_P0P1_DP<5>	CM50	QPI1_DRX_DP<14>	QPI1_DTX_DP<14>	CT44	QPI_CPU3_CPU0_P1P0_DP<14>	14			
6	QPI_CPU0_CPU3_P0P1_DP<6>	CN51	QPI1_DRX_DP<13>	QPI1_DTX_DP<13>	DB46	QPI_CPU3_CPU0_P1P0_DP<13>	13			
7	QPI_CPU0_CPU3_P0P1_DP<7>	CV52	QPI1_DRX_DP<12>	QPI1_DTX_DP<12>	DE47	QPI_CPU3_CPU0_P1P0_DP<12>	12			
8	QPI_CPU0_CPU3_P0P1_DP<8>	CU53	QPI1_DRX_DP<11>	QPI1_DTX_DP<11>	CU45	QPI_CPU3_CPU0_P1P0_DP<11>	11			
9	QPI_CPU0_CPU3_P0P1_DP<9>	CK52	QPI1_DRX_DP<10>	QPI1_DTX_DP<10>	DB48	QPI_CPU3_CPU0_P1P0_DP<10>	10			
10	QPI_CPU0_CPU3_P0P1_DP<10>	CJ53	QPI1_DRX_DP<9>	QPI1_DTX_DP<9>	DC49	QPI_CPU3_CPU0_P1P0_DP<9>	9			
11	QPI_CPU0_CPU3_P0P1_DP<11>	CT56	QPI1_DRX_DP<8>	QPI1_DTX_DP<8>	CT46	QPI_CPU3_CPU0_P1P0_DP<8>	8			
12	QPI_CPU0_CPU3_P0P1_DP<12>	CR57	QPI1_DRX_DP<7>	QPI1_DTX_DP<7>	DD50	QPI_CPU3_CPU0_P1P0_DP<7>	7			
13	QPI_CPU0_CPU3_P0P1_DP<13>	CP58	QPI1_DRX_DP<6>	QPI1_DTX_DP<6>	DC51	QPI_CPU3_CPU0_P1P0_DP<6>	6			
14	QPI_CPU0_CPU3_P0P1_DP<14>	CK54	QPI1_DRX_DP<5>	QPI1_DTX_DP<5>	CU47	QPI_CPU3_CPU0_P1P0_DP<5>	5			
15	QPI_CPU0_CPU3_P0P1_DP<15>	CK56	QPI1_DRX_DP<4>	QPI1_DTX_DP<4>	DD52	QPI_CPU3_CPU0_P1P0_DP<4>	4			
16	QPI_CPU0_CPU3_P0P1_DP<16>	CJ55	QPI1_DRX_DP<3>	QPI1_DTX_DP<3>	DA53	QPI_CPU3_CPU0_P1P0_DP<3>	3			
17	QPI_CPU0_CPU3_P0P1_DP<17>	CD54	QPI1_DRX_DP<2>	QPI1_DTX_DP<2>	CU49	QPI_CPU3_CPU0_P1P0_DP<2>	2			
18	QPI_CPU0_CPU3_P0P1_DP<18>	CD56	QPI1_DRX_DP<1>	QPI1_DTX_DP<1>	CT50	QPI_CPU3_CPU0_P1P0_DP<1>	1			
19	QPI_CPU0_CPU3_P0P1_DP<19>	CC55	QPI1_DRX_DP<0>	QPI1_DTX_DP<0>	CT48	QPI_CPU3_CPU0_P1P0_DP<0>	0			
0	QPI_CPU0_CPU3_P0P1_DN<0>	CN45	QPI1_DRX_DN<19>	QPI1_DTX_DN<19>	DD42	QPI_CPU3_CPU0_P1P0_DN<19>	19	QPI_CPU3_CPU0_P1P0_DN<19..0>	OUT	41<
1	QPI_CPU0_CPU3_P0P1_DN<1>	CM46	QPI1_DRX_DN<18>	QPI1_DTX_DN<18>	DC43	QPI_CPU3_CPU0_P1P0_DN<18>	18			
2	QPI_CPU0_CPU3_P0P1_DN<2>	CN47	QPI1_DRX_DN<17>	QPI1_DTX_DN<17>	CW43	QPI_CPU3_CPU0_P1P0_DN<17>	17			
3	QPI_CPU0_CPU3_P0P1_DN<3>	CM48	QPI1_DRX_DN<16>	QPI1_DTX_DN<16>	DD44	QPI_CPU3_CPU0_P1P0_DN<16>	16			
4	QPI_CPU0_CPU3_P0P1_DP<4>	CL49	QPI1_DRX_DN<15>	QPI1_DTX_DN<15>	DC45	QPI_CPU3_CPU0_P1P0_DN<15>	15			
5	QPI_CPU0_CPU3_P0P1_DP<5>	CK50	QPI1_DRX_DN<14>	QPI1_DTX_DN<14>	CV44	QPI_CPU3_CPU0_P1P0_DN<14>	14			
6	QPI_CPU0_CPU3_P0P1_DP<6>	CL51	QPI1_DRX_DN<13>	QPI1_DTX_DN<13>	DD46	QPI_CPU3_CPU0_P1P0_DN<13>	13			
7	QPI_CPU0_CPU3_P0P1_DP<7>	CT52	QPI1_DRX_DN<12>	QPI1_DTX_DN<12>	DC47	QPI_CPU3_CPU0_P1P0_DN<12>	12			
8	QPI_CPU0_CPU3_P0P1_DP<8>	CR53	QPI1_DRX_DN<11>	QPI1_DTX_DN<11>	CW45	QPI_CPU3_CPU0_P1P0_DN<11>	11			
9	QPI_CPU0_CPU3_P0P1_DP<9>	CM52	QPI1_DRX_DN<10>	QPI1_DTX_DN<10>	DD48	QPI_CPU3_CPU0_P1P0_DN<10>	10			
10	QPI_CPU0_CPU3_P0P1_DP<10>	CL53	QPI1_DRX_DN<9>	QPI1_DTX_DN<9>	DE49	QPI_CPU3_CPU0_P1P0_DN<9>	9			
11	QPI_CPU0_CPU3_P0P1_DP<11>	CV56	QPI1_DRX_DN<8>	QPI1_DTX_DN<8>	CV46	QPI_CPU3_CPU0_P1P0_DN<8>	8			
12	QPI_CPU0_CPU3_P0P1_DP<12>	CU57	QPI1_DRX_DN<7>	QPI1_DTX_DN<7>	DB50	QPI_CPU3_CPU0_P1P0_DN<7>	7			
13	QPI_CPU0_CPU3_P0P1_DP<13>	CT58	QPI1_DRX_DN<6>	QPI1_DTX_DN<6>	DE51	QPI_CPU3_CPU0_P1P0_DN<6>	6			
14	QPI_CPU0_CPU3_P0P1_DP<14>	CM54	QPI1_DRX_DN<5>	QPI1_DTX_DN<5>	CW47	QPI_CPU3_CPU0_P1P0_DN<5>	5			
15	QPI_CPU0_CPU3_P0P1_DP<15>	CM56	QPI1_DRX_DN<4>	QPI1_DTX_DN<4>	DB52	QPI_CPU3_CPU0_P1P0_DN<4>	4			
16	QPI_CPU0_CPU3_P0P1_DP<16>	CL55	QPI1_DRX_DN<3>	QPI1_DTX_DN<3>	DC53	QPI_CPU3_CPU0_P1P0_DN<3>	3			
17	QPI_CPU0_CPU3_P0P1_DP<17>	CF54	QPI1_DRX_DN<2>	QPI1_DTX_DN<2>	CW49	QPI_CPU3_CPU0_P1P0_DN<2>	2			
18	QPI_CPU0_CPU3_P0P1_DP<18>	CF56	QPI1_DRX_DN<1>	QPI1_DTX_DN<1>	CV50	QPI_CPU3_CPU0_P1P0_DN<1>	1			
19	QPI_CPU0_CPU3_P0P1_DP<19>	CE55	QPI1_DRX_DN<0>	QPI1_DTX_DN<0>	CV48	QPI_CPU3_CPU0_P1P0_DN<0>	0			
41> IN	QPI_CPU0_CPU3_P0P1_CLKA_DP	CR55	QPI1_CLKRX_DP	QPI1_CLKTX_DP	DB54	QPI_CPU3_CPU0_P1P0_CLKA_DP			OUT	41<
41> IN	QPI_CPU0_CPU3_P0P1_CLKA_DN	CU55	QPI1_CLKRX_DN	QPI1_CLKTX_DN	CY54	QPI_CPU3_CPU0_P1P0_CLKA_DN			OUT	41<

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CPU SOCKET 3 (10 OF 13)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 111 OF 303	

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P1V05_VCCP_CPU3

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IC
SANDYBRIDGE_EP_EXT_D

CA29	VCC<207>	VCC<155>	BP10
CA25	VCC<206>	VCC<154>	BN9
BY40	VCC<205>	VCC<153>	BN7
BY38	VCC<204>	VCC<152>	BN5
BY36	VCC<203>	VCC<151>	BN3
BY34	VCC<202>	VCC<150>	BN17
BY32	VCC<201>	VCC<149>	BN15
BY30	VCC<200>	VCC<148>	BN13
BY28	VCC<199>	VCC<147>	BN11
BY26	VCC<198>	VCC<146>	BN1
BY18	VCC<197>	VCC<145>	BK8
BV8	VCC<196>	VCC<144>	BK6
BV6	VCC<195>	VCC<143>	BK4
BV4	VCC<194>	VCC<142>	BK2
BV2	VCC<193>	VCC<141>	BK16
BV16	VCC<192>	VCC<140>	BK14
BV14	VCC<191>	VCC<139>	BK12
BV12	VCC<190>	VCC<138>	BK10
BV10	VCC<189>	VCC<137>	BJ9
BU9	VCC<188>	VCC<136>	BJ7
BU7	VCC<187>	VCC<135>	BJ5
BU5	VCC<186>	VCC<134>	BJ3
BU3	VCC<185>	VCC<133>	BJ17
BU17	VCC<184>	VCC<132>	BJ15
BU15	VCC<183>	VCC<131>	BJ13
BU13	VCC<182>	VCC<130>	BJ11
BU11	VCC<181>	VCC<129>	BJ1
BU1	VCC<180>	VCC<128>	BH8
BT8	VCC<179>	VCC<127>	BH6
BT6	VCC<178>	VCC<126>	BH4
BT4	VCC<177>	VCC<125>	BH2
BT2	VCC<176>	VCC<124>	BH16
BT16	VCC<175>	VCC<123>	BH14
BT14	VCC<174>	VCC<122>	BH12
BT12	VCC<173>	VCC<121>	BH10
BT10	VCC<172>	VCC<120>	BG9
BR9	VCC<171>	VCC<119>	BG7
BR7	VCC<170>	VCC<118>	BG5
BR5	VCC<169>	VCC<117>	BG3
BR3	VCC<168>	VCC<116>	BG17
BR17	VCC<167>	VCC<115>	BG15
BR15	VCC<166>	VCC<114>	BG13
BR13	VCC<165>	VCC<113>	BG11
BR11	VCC<164>	VCC<112>	BG1
BR1	VCC<163>	VCC<111>	BF8
BP8	VCC<162>	VCC<110>	BF6
BP6	VCC<161>	VCC<109>	BF4
BP4	VCC<160>	VCC<108>	BF2
BP2	VCC<159>	VCC<107>	BF16
BP16	VCC<158>	VCC<106>	BF14
BP14	VCC<157>	VCC<105>	BF12
BP12	VCC<156>	VCC<104>	BF10

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P1V05_VCCP_CPU3

U6C1
IC
SANDYBRIDGE_EP_EXT_D

BE9	VCC<103>	VCC<51>	AU7
BE7	VCC<102>	VCC<50>	AU5
BE5	VCC<101>	VCC<49>	AU3
BE3	VCC<100>	VCC<48>	AU17
BE17	VCC<99>	VCC<47>	AU15
BE15	VCC<98>	VCC<46>	AU13
BE13	VCC<97>	VCC<45>	AU11
BE11	VCC<96>	VCC<44>	AU1
BE1	VCC<95>	VCC<43>	AP8
BB8	VCC<94>	VCC<42>	AP6
BB6	VCC<93>	VCC<41>	AP4
BB4	VCC<92>	VCC<40>	AP2
BB2	VCC<91>	VCC<39>	AP16
BB16	VCC<90>	VCC<38>	AP14
BB14	VCC<89>	VCC<37>	AP12
BB12	VCC<88>	VCC<36>	AP10
BB10	VCC<87>	VCC<35>	AN9
BA9	VCC<86>	VCC<34>	AN7
BA7	VCC<85>	VCC<33>	AN5
BA5	VCC<84>	VCC<32>	AN3
BA3	VCC<83>	VCC<31>	AN17
BA17	VCC<82>	VCC<30>	AN15
BA15	VCC<81>	VCC<29>	AN13
BA13	VCC<80>	VCC<28>	AN11
BA11	VCC<79>	VCC<27>	AN1
BA1	VCC<78>	VCC<26>	AM8
AY8	VCC<77>	VCC<25>	AM6
AY6	VCC<76>	VCC<24>	AM4
AY4	VCC<75>	VCC<23>	AM2
AY2	VCC<74>	VCC<22>	AM16
AY16	VCC<73>	VCC<21>	AM14
AY14	VCC<72>	VCC<20>	AM12
AY12	VCC<71>	VCC<19>	AM10
AY10	VCC<70>	VCC<18>	AL9
AW9	VCC<69>	VCC<17>	AL7
AW7	VCC<68>	VCC<16>	AL5
AW5	VCC<67>	VCC<15>	AL3
AW3	VCC<66>	VCC<14>	AL17
AW17	VCC<65>	VCC<13>	AL15
AW15	VCC<64>	VCC<12>	AL13
AW13	VCC<63>	VCC<11>	AL11
AW11	VCC<62>	VCC<10>	AL1
AW1	VCC<61>	VCC<9>	AG41
AV8	VCC<60>	VCC<8>	AG39
AV6	VCC<59>	VCC<7>	AG37
AV4	VCC<58>	VCC<6>	AG35
AV2	VCC<57>	VCC<5>	AG33
AV16	VCC<56>	VCC<4>	AG31
AV14	VCC<55>	VCC<3>	AG29
AV12	VCC<54>	VCC<2>	AG27
AV10	VCC<53>	VCC<1>	AG25
AU9	VCC<52>	VCC<0>	AG19

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CPU SOCKET 3 (11 OF 13)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 112 OF 303

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IC
SANDYBRIDGE_EP_EXT_D

P1V05_VTT_CPU3
1.05

P1V5_DDR3_CPU3
1.5

P1V5_DDR3_CPU3
1.5

P1V05_VTT_CPU3
1.05

P1V8_PLL_CPU3
1.8

P0V85_VSA_CPU3
0.85

P1V05_VTT_CPU3
1.05

P1V05_VTT_CPU3
1.05

DA49	VTTA<2>	VCC_SENSE	BW3	VSENSE_DIE_CPU3_VCCP_P	OUT	251<	
CR51	VTTA<3>	RSVD<20>	DB56	NC_CPU3_RSVD<20>			
CR45	VTTA<4>	VSS_VCC_SENSE	BY2	VSENSE_DIE_CPU3_VCCP_N	OUT	251<	
CJ49	VTTA<5>	VTTD_SENSE	BP42	VSENSE_DIE_CPU3_VTT_P	OUT	272>	
CG55	VTTA<6>	VSS_VTTD_SENSE	BT42	VSENSE_DIE_CPU3_VTT_N	OUT	272>	
CC45	VTTA<7>						
CA53	VTTA<8>	VCCPLL<1>	CA13				
		VCCPLL<2>	BY14				
BV42	VTTD<4>	VCCPLL<0>	CA15				
		VSS_VSA_SENSE	AF14	VSENSE_DIE_VSA3_N	OUT	252<	
		VSA_SENSE	AG13	VSENSE_DIE_VSA3_P	OUT	252<	
V24	VCCD_23<5>	VSA<24>	N51				
V22	VCCD_23<6>	VSA<23>	N45				
V20	VCCD_23<7>	VSA<22>	G49				
V18	VCCD_23<8>	VSA<21>	G43				
V16	VCCD_23<9>	VSA<20>	B54				
N23	VCCD_23<10>	VSA<19>	AJ9				
N21	VCCD_23<11>	VSA<18>	AJ7				
N19	VCCD_23<12>	VSA<17>	AJ5				
N17	VCCD_23<13>	VSA<16>	AJ3				
N15	VCCD_23<14>	VSA<15>	AJ13				
H24	VCCD_23<15>	VSA<14>	AJ11				
H22	VCCD_23<16>	VSA<13>	AJ1				
H20	VCCD_23<17>	VSA<12>	AH8				
H18	VCCD_23<18>	VSA<11>	AH6				
H16	VCCD_23<19>	VSA<10>	AH4				
G13	VCCD_23<20>	VSA<9>	AH2				
C23	VCCD_23<21>	VSA<8>	AH16				
C21	VCCD_23<22>	VSA<7>	AH14				
C19	VCCD_23<23>	VSA<6>	AH12				
C17	VCCD_23<24>	VSA<5>	AH10				
C15	VCCD_23<25>	VSA<4>	AG17				
AC25	VCCD_23<0>	VSA<3>	AG15				
AC23	VCCD_23<1>	VSA<2>	AF18				
AC21	VCCD_23<2>	VSA<1>	AE17				
AC19	VCCD_23<3>	VSA<0>	AE15				
AC17	VCCD_23<4>						
		VTTA<0>	Y54				
		VTTA<1>	W49				
		VTTA<9>	AU53				
		VTTA<10>	AM54				
		VTTA<11>	AM48				
		VTTA<12>	AE53				
		VTTA<13>	AE45				
		VTTD<0>	CA23				
		VTTD<1>	CA21				
		VTTD<2>	BY22				
		VTTD<3>	BY20				
		VTTD<5>	BU47				
		VTTD<6>	BR55				
		VTTD<9>	BK56				
		VTTD<7>	BM42				
		VTTD<10>	BH42				
		VTTD<11>	BD42				
		VTTD<12>	AY42				
		VTTD<13>	AT42				
		VTTD<14>	AM42				
		VTTD<15>	AG23				
		VTTD<16>	AG21				
		VTTD<17>	AF24				
		VTTD<18>	AF22				
DD26	VCCD_01<0>	VTTD<8>	BL51				
DD24	VCCD_01<1>						
DD22	VCCD_01<2>						
DD20	VCCD_01<3>						
DD18	VCCD_01<4>						
CW27	VCCD_01<5>						
CW25	VCCD_01<6>						
CW23	VCCD_01<7>						
CW21	VCCD_01<8>						
CW19	VCCD_01<9>						
CP28	VCCD_01<10>						
CP26	VCCD_01<11>						
CP24	VCCD_01<12>						
CP22	VCCD_01<13>						
CP20	VCCD_01<14>						
CJ27	VCCD_01<15>						
CJ25	VCCD_01<16>						
CJ23	VCCD_01<17>						
CJ21	VCCD_01<18>						
CJ19	VCCD_01<19>						
CD28	VCCD_01<20>						
CD26	VCCD_01<21>						
CD24	VCCD_01<22>						
CD22	VCCD_01<23>						
CD20	VCCD_01<24>						

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CY40	VSS<547>		
AW55	VSS<546>		
AG43	VSS<545>	VSS<477>	N9
CW51	VSS<544>	VSS<476>	N53
C3	VSS<543>	VSS<475>	N5
D2	VSS<542>	VSS<474>	N49
DB2	VSS<541>	VSS<473>	N47
DC3	VSS<540>	VSS<472>	N43
E1	VSS<539>	VSS<471>	N41
V46	VSS<538>	VSS<470>	N37
BG47	VSS<537>	VSS<469>	N35
BK50	VSS<536>	VSS<468>	N33
AU51	VSS<535>	VSS<467>	N13
Y56	VSS<534>	VSS<466>	M8
Y42	VSS<533>	VSS<465>	M52
Y40	VSS<532>	VSS<464>	M50
Y38	VSS<531>	VSS<463>	M46
Y36	VSS<530>	VSS<462>	M44
Y32	VSS<529>	VSS<461>	M42
Y30	VSS<528>	VSS<460>	M36
Y28	VSS<527>	VSS<459>	M34
Y12	VSS<526>	VSS<458>	L5
Y10	VSS<525>	VSS<457>	L41
W9	VSS<524>	VSS<456>	L29
W53	VSS<523>	VSS<455>	L25
W51	VSS<522>	VSS<454>	K8
W5	VSS<521>	VSS<453>	K34
W47	VSS<520>	VSS<452>	K30
W45	VSS<519>	VSS<451>	K28
W43	VSS<518>	VSS<450>	K2
W41	VSS<517>	VSS<449>	J55
W37	VSS<516>	VSS<448>	J5
W33	VSS<515>	VSS<447>	J41
W13	VSS<514>	VSS<446>	J39
V8	VSS<513>	VSS<445>	J33
V50	VSS<512>	VSS<444>	J31
V48	VSS<511>	VSS<443>	J27
V44	VSS<510>	VSS<442>	J11
V42	VSS<509>	VSS<441>	H8
V36	VSS<508>	VSS<440>	H54
V34	VSS<507>	VSS<439>	H52
V28	VSS<506>	VSS<438>	H40
V26	VSS<505>	VSS<437>	H38
U5	VSS<504>	VSS<436>	H34
U35	VSS<503>	VSS<435>	H32
T8	VSS<502>	VSS<434>	K26
T6	VSS<501>	VSS<433>	H14
T42	VSS<500>	VSS<432>	H12
T4	VSS<499>	VSS<431>	H10
T28	VSS<498>	VSS<430>	G9
R7	VSS<497>	VSS<429>	G57
R55	VSS<496>	VSS<428>	G53
R5	VSS<495>	VSS<427>	G51
R39	VSS<494>	VSS<426>	G5
R35	VSS<493>	VSS<425>	G47
R31	VSS<492>	VSS<424>	G45
R3	VSS<491>	VSS<423>	G41
R29	VSS<490>	VSS<422>	G37
R11	VSS<489>	VSS<421>	G35
P8	VSS<488>	VSS<420>	G31
P56	VSS<487>	VSS<419>	G1
P54	VSS<486>	VSS<418>	F8
P40	VSS<485>	VSS<417>	F50
P38	VSS<484>	VSS<416>	F48
P32	VSS<483>	VSS<415>	F44
P30	VSS<482>	VSS<414>	F42
P26	VSS<481>	VSS<413>	F36
P14	VSS<480>	VSS<412>	G25
P12	VSS<479>	VSS<411>	E5
P10	VSS<478>	VSS<410>	E41

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SOCKET3	SOCKET3	SOCKET3	SOCKET3	SOCKET3	SOCKET3	SOCKET3	SOCKET3	SOCKET3	SOCKET3
C5P30	C5P29	C5P28	C5P1	C5P2	C5D1	C5D3	C5D28	C5D30	C5D29
22UF	22UF	22UF	22UF	22UF	22UF	22UF	22UF	22UF	22UF
4V	4V	4V	4V	4V	4V	4V	4V	4V	4V
20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
C95333-002	C95333-002	C95333-002	C95333-002	C95333-002	C95333-002	C95333-002	C95333-002	C95333-002	C95333-002
0805LF	0805LF	0805LF	0805LF	0805LF	0805LF	0805LF	0805LF	0805LF	0805LF

CAD NOTE:
PLACE IN SOCKET CAVITY

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CPU SOCKET 3 (12 OF 13)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359
		SCALE:	DO NOT SCALE DRAWING	SHEET 113 OF 303

REV 1.0

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IC
SANDYBRIDGE_EP_EXT_D

E31	VSS<409>	VSS<341>	CV34	CJ29	VSS<273>	VSS<205>	C55
E3	VSS<408>	VSS<340>	CV32	CJ17	VSS<272>	VSS<204>	C5
E29	VSS<407>	VSS<339>	CV30	CJ11	VSS<271>	VSS<203>	C41
DF8	VSS<406>	VSS<338>	CV18	CH6	VSS<270>	VSS<202>	C39
DF52	VSS<405>	VSS<337>	CV14	CP50	VSS<269>	VSS<201>	C33
DF50	VSS<404>	VSS<336>	CU5	CH54	VSS<268>	VSS<200>	C13
DF48	VSS<403>	VSS<335>	CU35	CH52	VSS<267>	VSS<199>	C11
DF46	VSS<402>	VSS<334>	CU3	CH50	VSS<266>	VSS<198>	BY8
DF44	VSS<401>	VSS<333>	CU11	CH48	VSS<265>	VSS<197>	BY58
DF42	VSS<400>	VSS<332>	CU1	CH46	VSS<264>	VSS<196>	BY42
DF36	VSS<399>	VSS<331>	CT42	CH44	VSS<263>	VSS<195>	BY4
DF12	VSS<398>	VSS<330>	CT28	CH36	VSS<262>	VSS<194>	BY24
DE7	VSS<397>	VSS<329>	CR9	CH16	VSS<261>	VSS<193>	BW7
DE53	VSS<396>	VSS<328>	CR5	CH12	VSS<260>	VSS<192>	BW5
DE41	VSS<395>	VSS<327>	CR49	CG9	VSS<259>	VSS<191>	BW17
DE17	VSS<394>	VSS<326>	CR47	CG53	VSS<258>	VSS<190>	BW15
DD6	VSS<393>	VSS<325>	CR35	CG43	VSS<257>	VSS<189>	BW13
DD38	VSS<392>	VSS<324>	CR11	CG41	VSS<256>	VSS<188>	BW11
DD36	VSS<391>	VSS<323>	CP56	CG39	VSS<255>	VSS<187>	BW1
DD34	VSS<390>	VSS<322>	CP52	CG37	VSS<254>	VSS<186>	BU51
DD14	VSS<389>	VSS<321>	CP48	CG35	VSS<253>	VSS<185>	BU45
DD12	VSS<388>	VSS<320>	CP46	CG33	VSS<252>	VSS<184>	BT56
DD10	VSS<387>	VSS<319>	CP44	CG31	VSS<251>	VSS<183>	BT54
DC5	VSS<386>	VSS<318>	CP40	CG15	VSS<250>	VSS<182>	BT52
DC41	VSS<385>	VSS<317>	CP36	CF6	VSS<249>	VSS<181>	BT50
DB58	VSS<384>	VSS<316>	CP16	CF42	VSS<248>	VSS<180>	BT48
		VSS<315>	CP12	CF40	VSS<247>	VSS<179>	BT46
DB36	VSS<383>	VSS<314>	CN9	CF38	VSS<246>	VSS<178>	B52
DB32	VSS<382>	VSS<313>	CN7	CF36	VSS<245>	VSS<177>	BR57
DB12	VSS<381>	VSS<312>	CN57	CF34	VSS<244>	VSS<176>	BR53
DA9	VSS<380>	VSS<311>	CN55	CF32	VSS<243>	VSS<175>	BP58
DA51	VSS<379>	VSS<310>	CN53	CF30	VSS<242>	VSS<174>	BN45
DA5	VSS<378>	VSS<309>	CN5	CF14	VSS<241>	VSS<173>	BN43
DA47	VSS<377>	VSS<308>	CP42	CF12	VSS<240>	VSS<172>	BM8
DA45	VSS<376>	VSS<307>	CN39	CE9	VSS<239>	VSS<171>	BM6
DA43	VSS<375>	VSS<306>	CN37	CE5	VSS<238>	VSS<170>	BK42
DA41	VSS<374>	VSS<305>	CN35	CE13	VSS<237>	VSS<169>	BM4
DA3	VSS<373>	VSS<304>	CN33	CD6	VSS<236>	VSS<168>	BM2
DA11	VSS<372>	VSS<303>	CN31	CD36	VSS<235>	VSS<167>	BM16
D8	VSS<371>	VSS<302>	CN3	CD18	VSS<234>	VSS<166>	BM14
D36	VSS<370>	VSS<301>	CN17	CC9	VSS<233>	VSS<165>	BM12
D26	VSS<369>	VSS<300>	CN15	CC49	VSS<232>	VSS<164>	BM10
CY8	VSS<368>	VSS<299>	CN13	CC47	VSS<231>	VSS<163>	BL9
CY50	VSS<367>	VSS<298>	CN11	CC43	VSS<230>	VSS<162>	BL7
CY44	VSS<366>	VSS<297>	CM8	CC3	VSS<229>	VSS<161>	BL5
CY36	VSS<365>	VSS<296>	CM6	CC29	VSS<228>	VSS<160>	BL49
CY2	VSS<364>	VSS<295>	CM42	CC13	VSS<227>	VSS<159>	BK48
CY16	VSS<363>	VSS<294>	CM40	CB8	VSS<226>	VSS<158>	BL3
CY12	VSS<362>	VSS<293>	CM38	CB6	VSS<225>	VSS<157>	BL17
CY10	VSS<361>	VSS<292>	CM36	CB56	VSS<224>	VSS<156>	BL15
CW7	VSS<360>	VSS<291>	CM34	CB52	VSS<223>	VSS<155>	BL13
CW57	VSS<359>	VSS<290>	CM32	CB50	VSS<222>	VSS<154>	BL11
CW55	VSS<358>	VSS<289>	CM30	CB48	VSS<221>	VSS<153>	BL1
CW53	VSS<357>	VSS<288>	CM14	CB46	VSS<220>	VSS<152>	BK54
CW5	VSS<356>	VSS<287>	CM10	CB36	VSS<219>	VSS<151>	BK52
CW39	VSS<355>	VSS<286>	CL5	CB16	VSS<218>	VSS<150>	BK46
CW37	VSS<354>	VSS<285>	CL43	CA57	VSS<217>	VSS<149>	BJ57
CW35	VSS<353>	VSS<284>	CL17	CA55	VSS<216>	VSS<148>	BJ55
CW33	VSS<352>	VSS<283>	CK6	CA5	VSS<215>	VSS<147>	BH58
CW31	VSS<351>	VSS<282>	CK4	CA41	VSS<214>	VSS<146>	BF44
CW29	VSS<350>	VSS<281>	CK36	CA39	VSS<213>	VSS<145>	BF42
CW15	VSS<349>	VSS<280>	CK10	CA37	VSS<212>	VSS<144>	BE51
CW13	VSS<348>	VSS<279>	CJ9	CA35	VSS<211>	VSS<143>	BE49
CW11	VSS<347>	VSS<278>	CJ51	CA33	VSS<210>	VSS<142>	BD8
CV6	VSS<346>	VSS<277>	CJ47	CA31	VSS<209>	VSS<141>	BD6
CV58	VSS<345>	VSS<276>	CJ45	CA27	VSS<208>	VSS<140>	BD56
CV54	VSS<344>	VSS<275>	CJ43	CA19	VSS<207>	VSS<139>	BD54
CV42	VSS<343>	VSS<274>	CJ3	CA11	VSS<206>	VSS<138>	BD4
CV38	VSS<342>					VSS<137>	BD2

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IC
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BD16	VSS<136>	VSS<68>	AK46
BD14	VSS<135>	VSS<67>	AK44
BD12	VSS<134>	VSS<66>	AK42
BD10	VSS<133>	VSS<65>	AK4
BC9	VSS<132>	VSS<64>	AK2
BC7	VSS<131>	VSS<63>	AK16
BC57	VSS<130>	VSS<62>	AK14
BC55	VSS<129>	VSS<61>	AK12
BC53	VSS<128>	VSS<60>	AK10
BC5	VSS<127>	VSS<59>	AJ17
BC45	VSS<126>	VSS<58>	AJ15
BC43	VSS<125>	VSS<57>	AH58
BC3	VSS<124>	VSS<56>	AG9
BC17	VSS<123>	VSS<55>	AG57
BC15	VSS<122>	VSS<54>	AG55
BC13	VSS<121>	VSS<53>	AG5
BC11	VSS<120>	VSS<52>	AG3
BC1	VSS<119>	VSS<51>	AG1
BB58	VSS<118>	VSS<50>	AF6
BB52	VSS<117>	VSS<49>	AF56
BB50	VSS<116>	VSS<48>	AF54
BB48	VSS<115>	VSS<47>	AF42
BB46	VSS<114>	VSS<46>	AF40
BB42	VSS<113>	VSS<45>	AF36
B8	VSS<112>	VSS<44>	AF34
B6	VSS<111>	VSS<43>	AF26
B36	VSS<110>	VSS<42>	AF20
AW57	VSS<109>	VSS<41>	AF16
AV56	VSS<108>	VSS<40>	AF12
AV54	VSS<107>	VSS<39>	AE9
AV42	VSS<106>	VSS<38>	AE51
AU49	VSS<105>	VSS<37>	AE49
AU47	VSS<104>	VSS<36>	AE47
AU45	VSS<103>	VSS<35>	AE43
AT8	VSS<102>	VSS<34>	AE39
AT6	VSS<101>	VSS<33>	AE31
AT52	VSS<100>	VSS<32>	AE29
AT46	VSS<99>	VSS<31>	AD6
AT4	VSS<98>	VSS<30>	AD52
AT2	VSS<97>	VSS<29>	AD50
AT16	VSS<96>	VSS<28>	AD48
AT14	VSS<95>	VSS<27>	AD46
AT12	VSS<94>	VSS<26>	AD44
AT10	VSS<93>	VSS<25>	AD42
AR9	VSS<92>	VSS<24>	AD36
AR7	VSS<91>	VSS<23>	AD34
AR5	VSS<90>	VSS<22>	AD26
AR3	VSS<89>	VSS<21>	AC9
AR17	VSS<88>	VSS<20>	AC31
AR15	VSS<87>	VSS<19>	AB6
AR13	VSS<86>	VSS<18>	AB42
AR11	VSS<85>	VSS<17>	AB36
AR1	VSS<84>	VSS<16>	AB14
AP58	VSS<83>	VSS<15>	AA9
AP44	VSS<82>	VSS<14>	AA55
AP42	VSS<81>	VSS<13>	AA5
AN57	VSS<80>	VSS<12>	AA39
AN55	VSS<79>	VSS<11>	AA31
AM56	VSS<78>	VSS<10>	AA3
AL53	VSS<77>	VSS<9>	AA29
AL51	VSS<76>	VSS<8>	AA11
AL49	VSS<75>	VSS<7>	A7
AL45	VSS<74>	VSS<6>	A51
AL43	VSS<73>	VSS<5>	A5
AK8	VSS<72>	VSS<4>	A49
AK6	VSS<71>	VSS<3>	A47
AK50	VSS<70>	VSS<2>	A45
AK48	VSS<69>	VSS<1>	A43
		VSS<0>	A41

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CPU SOCKET 3 (13 OF 13)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 114 OF 303	

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CONN240_E55582004

103>	IN	M_N_BA<2>		52	A16_BA2	DQ<63>	234 63
			15	171	A<15>	DQ<62>	233 62
			14	172	A<14>	DQ<61>	228 61
			13	196	A<13>	DQ<60>	227 60
			12	174	A<12>	DQ<59>	115 59
			11	55	A<11>	DQ<58>	114 58
			10	70	A<10>	DQ<57>	109 57
			9	175	A<9>	DQ<56>	108 56
			8	177	A<8>	DQ<55>	225 55
			7	56	A<7>	DQ<54>	224 54
			6	178	A<6>	DQ<53>	219 53
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			4	59	A<4>	DQ<51>	106 51
			3	180	A<3>	DQ<50>	105 50
			2	61	A<2>	DQ<49>	100 49
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103>	IN	M_N_BA<1..0>				DQ<46>	215 46
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			0	71	BA<0>	DQ<44>	209 44
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103>	IN	M_N_CS_N<3..0>				DQ<38>	206 38
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			0	193	CS<0>	DQ<34>	87 34
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103>	IN	M_N_CKE<1>		169	CKE<1>	DQ<32>	81 32
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103>	IN	M_N_WE_N		73	WE_N	DQ<29>	150 29
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103>	IN	M_N_ODT<1..0>				DQ<26>	36 26
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103>	IN	M_N_MA_PAR		68	PAR_IN_NC	DQ<22>	146 22
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J4B1

CONN240_E55582004

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23	VSS<51>	VDD<14>	69	
26	VSS<50>	VDD<13>	72	
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86	VSS<40>	VDD<3>	189	P0V75_VTT_DDR3_CPU3
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P1V5_DDR3_CPU3 1.5

C4D1 10UF 6.3V 20% 602433-075 0603LF

C4C10 10UF 6.3V 20% 602433-075 0603LF

J4B1

CONN240_E55582004

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DQS15P_DM6	221	15		
DQS15N_NC	222	15		
DQS14P_DM5	212	14		
DQS14N_NC	213	14		
DQS13P_DM4	203	13		
DQS13N_NC	204	13		
DQS12P_DM3	152	12		
DQS12N_NC	153	12		
DQS11P_DM2	143	11		
DQS11N_NC	144	11		
DQS10P_DM1	134	10		
DQS10N_NC	135	10		
DQS9P_DM0	125	9		
DQS9N_NC	126	9		
DQS8P	43	8		
DQS8N	42	8		
DQS7P	112	7		
DQS7N	111	7		
DQS6P	103	6		
DQS6N	102	6		
DQS5P	94	5		
DQS5N	93	5		
DQS4P	85	4		
DQS4N	84	4		
DQS3P	34	3		
DQS3N	33	3		
DQS2P	25	2		
DQS2N	24	2		
DQS1P	16	1		
DQS1N	15	1		
DQS0P	7	0		
DQS0N	6	0		

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P1V5_DDR3_CPU3

R4B11 100 1% 1/16W 1.5

A93548-043 0402LF 0.75

P1V5_DDR3_CPU3_VREF_N_D OUT 115< 119>

R4B10 100 1% 1/16W

C4B15 0.1UF 16V 10%

A93548-043 0402LF A36096-030 0402LF

P1V5_DDR3_CPU3

R4D3 100 1% 1/16W 1.5

A93548-043 0402LF 0.75

P1V5_DDR3_CPU3_VREF_N_A OUT 115<

R4D4 100 1% 1/16W

C4D10 0.1UF 16V 10%

A93548-043 0402LF A36096-030 0402LF

DDR3 CPU3 CHANNEL N DIMM1

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 115 OF 303	

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J4B2

CONN240_E55582004

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			6	178	A<6>	DQ<53>	219 53
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			4	59	A<4>	DQ<51>	106 51
			3	180	A<3>	DQ<50>	105 50
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104>	IN	M_P_MA<15..0>	0	188	A<0>	DQ<47>	216 47
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			1	190	BA<1>	DQ<45>	210 45
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						DQ<43>	97 43
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104>	IN	M_P_CK_DN<2>		64	NC_CK1N	DQ<41>	91 41
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104>	IN	M_P_CK_DN<0>		185	CK0N	DQ<39>	207 39
104>	IN	M_P_CS_N<3..0>				DQ<38>	206 38
			3	198	CS<3>	DQ<37>	201 37
			2	79	CS<2>	DQ<36>	200 36
			1	76	CS<1>	DQ<35>	88 35
			0	193	CS<0>	DQ<34>	87 34
						DQ<33>	82 33
104>	IN	M_P_CKE<1>		169	CKE<1>	DQ<32>	81 32
104>	IN	M_P_CKE<0>		50	CKE<0>	DQ<31>	156 31
						DQ<30>	155 30
104>	IN	M_P_WE_N		73	WE_N	DQ<29>	150 29
104>	IN	M_P_RAS_N		192	RAS_N	DQ<28>	149 28
104>	IN	M_P_CAS_N		74	CAS_N	DQ<27>	37 27
104>	IN	M_P_ODT<1..0>				DQ<26>	36 26
			1	77	ODT<1>	DQ<25>	31 25
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						DQ<23>	147 23
104>	IN	M_P_MA_PAR		68	PAR_IN_NC	DQ<22>	146 22
104<	OUT	M_P_PAR_ERR_N<0>		53	ERR_OUT_NC	DQ<21>	141 21
104<>	BI	M_P_ECC<7..0>				DQ<20>	140 20
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			3	46	CB<3>	DQ<15>	138 15
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			1	40	CB<1>	DQ<13>	132 13
			0	39	CB<0>	DQ<12>	131 12
						DQ<11>	19 11
115<	102> IN	M_NP_RESET_LVC1V5_N		168	RESET_N	DQ<10>	18 10
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M_P_DQ<63..0> BI 104<>

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P1V5_DDR3_CPU3

R4B9 100 1% 1/16W 1 2 — 1.5

A93548-043 0402LF — 0.75

P1V5_DDR3_CPU3_VREF_P_D — OUT 116< 119>

R4B8 100 1% 1/16W — C4B13 0.1UF 16V 10% — A36096-030 0402LF

P1V5_DDR3_CPU3

R4D2 100 1% 1/16W 1 2 — 1.5

A93548-043 0402LF — 0.75

P1V5_DDR3_CPU3_VREF_P_A — OUT 116<

R4D1 100 1% 1/16W — C4D2 0.1UF 16V 10% — A36096-030 0402LF

J4B2

CONN240_E55582004

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	20	VSS<52>	VDD<15>	66			
	23	VSS<51>	VDD<14>	69			
	26	VSS<50>	VDD<13>	72			
	29	VSS<49>	VDD<12>	75			
	32	VSS<48>	VDD<11>	78			
	35	VSS<47>	VDD<10>	170			
	38	VSS<46>	VDD<9>	173			
	41	VSS<45>	VDD<8>	176			
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	47	VSS<43>	VDD<6>	182			
	80	VSS<42>	VDD<5>	183			
	83	VSS<41>	VDD<4>	186			
	86	VSS<40>	VDD<3>	189			
	89	VSS<39>	VDD<2>	191			
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P1V5_DDR3_CPU3 — 1.5

C4C6 10UF 6.3V 20% 602433-075 0603LF

C4C5 10UF 6.3V 20% 602433-075 0603LF

P0V75_VTT_DDR3_CPU3 — 0.75

J4B2

CONN240_E55582004

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DQS15N_NC	222		15
DQS14P_DM5	212	14	
DQS14N_NC	213		14
DQS13P_DM4	203	13	
DQS13N_NC	204		13
DQS12P_DM3	152	12	
DQS12N_NC	153		12
DQS11P_DM2	143	11	
DQS11N_NC	144		11
DQS10P_DM1	134	10	
DQS10N_NC	135		10
DQS9P_DM0	125	9	
DQS9N_NC	126		9
DQS8P	43	8	
DQS8N	42		8
DQS7P	112	7	
DQS7N	111		7
DQS6P	103	6	
DQS6N	102		6
DQS5P	94	5	
DQS5N	93		5
DQS4P	85	4	
DQS4N	84		4
DQS3P	34	3	
DQS3N	33		3
DQS2P	25	2	
DQS2N	24		2
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DQS1N	15		1
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DDR3 CPU3 CHANNEL P DIMM1

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
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		SCALE:	DO NOT SCALE DRAWING	SHEET 116 OF 303	

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		11 55	A<11>	DQ<58>	114 58
		10 70	A<10>	DQ<57>	109 57
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		5 58	A<5>	DQ<52>	218 52
		4 59	A<4>	DQ<51>	106 51
		3 180	A<3>	DQ<50>	105 50
		2 61	A<2>	DQ<49>	100 49
		1 181	A<1>	DQ<48>	99 48
105> IN	M_R_MA<15..0>	0 188	A<0>	DQ<47>	216 47
105> IN	M_R_BA<1..0>			DQ<46>	215 46
		1 190	BA<1>	DQ<45>	210 45
		0 71	BA<0>	DQ<44>	209 44
				DQ<43>	97 43
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105> IN	M_R_CK_DN<2>	64	NC_CK1N	DQ<41>	91 41
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105> IN	M_R_CK_DN<0>	185	CK0N	DQ<39>	207 39
105> IN	M_R_CS_N<3..0>			DQ<38>	206 38
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		2 79	CS<2>	DQ<36>	200 36
		1 76	CS<1>	DQ<35>	88 35
		0 193	CS<0>	DQ<34>	87 34
				DQ<33>	82 33
105> IN	M_R_CKE<1>	169	CKE<1>	DQ<32>	81 32
105> IN	M_R_CKE<0>	50	CKE<0>	DQ<31>	156 31
				DQ<30>	155 30
105> IN	M_R_WE_N	73	WE_N	DQ<29>	150 29
105> IN	M_R_RAS_N	192	RAS_N	DQ<28>	149 28
105> IN	M_R_CAS_N	74	CAS_N	DQ<27>	37 27
105> IN	M_R_ODT<1..0>			DQ<26>	36 26
		1 77	ODT<1>	DQ<25>	31 25
		0 195	ODT<0>	DQ<24>	30 24
				DQ<23>	147 23
105> IN	M_R_MA_PAR	68	PAR_IN_NC	DQ<22>	146 22
105< OUT	M_R_PAR_ERR_N<0>	53	ERR_OUT_NC	DQ<21>	141 21
105<> BI	M_R_ECC<7..0>			DQ<20>	140 20
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		3 46	CB<3>	DQ<15>	138 15
		2 45	CB<2>	DQ<14>	137 14
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				DQ<11>	19 11
118< 102> IN	M_RT_RESET_LVC1V5_N	168	RESET_N	DQ<10>	18 10
				DQ<9>	13 9
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3.3		237	SA<1>	DQ<6>	128 6
		117	SA<0>	DQ<5>	123 5
201> 119<> 118<> BI	SMB_DDR_RT_LVC3_SDA	238	SDA	DQ<4>	122 4
201<> 119< 118< IN	SMB_DDR_RT_LVC3_SCL	118	SCL	DQ<3>	10 3
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M_R_DQ<63..0> BI 105<>

P1V5_DDR3_CPU3

R6E1 100 1% 1/16W 1.5 — A93548-043 0402LF — 0.75

P1V5_DDR3_CPU3_VREF_R_D OUT 117< 119>

R6E2 100 1% 1/16W — A93548-043 0402LF

C6E1 0.1UF 16V 10% — A36096-030 0402LF

P1V5_DDR3_CPU3

R6B23 100 1% 1/16W 1.5 — A93548-043 0402LF — 0.75

P1V5_DDR3_CPU3_VREF_R_A OUT 117<

R6B24 100 1% 1/16W — A93548-043 0402LF

C6B9 0.1UF 16V 10% — A36096-030 0402LF

J6E2

CONN240_E55582004

		2	VSS<58>	VDD<21>	51
		5	VSS<57>	VDD<20>	54
		8	VSS<56>	VDD<19>	57
		11	VSS<55>	VDD<18>	60
		14	VSS<54>	VDD<17>	62
		17	VSS<53>	VDD<16>	65
		20	VSS<52>	VDD<15>	66
		23	VSS<51>	VDD<14>	69
		26	VSS<50>	VDD<13>	72
		29	VSS<49>	VDD<12>	75
		32	VSS<48>	VDD<11>	78
		35	VSS<47>	VDD<10>	170
		38	VSS<46>	VDD<9>	173
		41	VSS<45>	VDD<8>	176
		44	VSS<44>	VDD<7>	179
		47	VSS<43>	VDD<6>	182
		80	VSS<42>	VDD<5>	183
		83	VSS<41>	VDD<4>	186
		86	VSS<40>	VDD<3>	189
		89	VSS<39>	VDD<2>	191
		92	VSS<38>	VDD<1>	194
		95	VSS<37>	VDD<0>	197
		98	VSS<36>		
		101	VSS<35>	VTT<3>	49
		104	VSS<34>	VTT<2>	48
		107	VSS<33>	VTT<1>	120
		110	VSS<32>	VTT<0>	240
		113	VSS<31>		
		116	VSS<30>		
		121	VSS<29>	NC_TEST	167 TP_R_D1_NC2
		124	VSS<28>		
		127	VSS<27>		
		130	VSS<26>		
		133	VSS<25>		
		136	VSS<24>		
		139	VSS<23>		
		142	VSS<22>		
		145	VSS<21>		
		148	VSS<20>		
		151	VSS<19>		
		154	VSS<18>		
		157	VSS<17>		
		160	VSS<16>		
		163	VSS<15>		
		166	VSS<14>		
		199	VSS<13>		
		202	VSS<12>		
		205	VSS<11>		
		208	VSS<10>		
		211	VSS<9>		
		214	VSS<8>		
		217	VSS<7>		
		220	VSS<6>		
		223	VSS<5>		
		226	VSS<4>		
		229	VSS<3>		
		232	VSS<2>		
		235	VSS<1>		
		239	VSS<0>		

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P1V5_DDR3_CPU3

1.5 — C6C7 10UF 6.3V 20% — 602433-075 0603LF

P1V5_DDR3_CPU3

1.5 — C6C4 10UF 6.3V 20% — 602433-075 0603LF

P0V75_VTT_DDR3_CPU3

0.75

J6E2

CONN240_E55582004

		M_R_DQS_DP<17..0>	BI	105<>
		M_R_DQS_DN<17..0>	BI	105<>
DQS17P_DM8	161 17			
DQS17N_NC	162		17	
DQS16P_DM7	230 16			
DQS16N_NC	231		16	
DQS15P_DM6	221 15			
DQS15N_NC	222		15	
DQS14P_DM5	212 14			
DQS14N_NC	213		14	
DQS13P_DM4	203 13			
DQS13N_NC	204		13	
DQS12P_DM3	152 12			
DQS12N_NC	153		12	
DQS11P_DM2	143 11			
DQS11N_NC	144		11	
DQS10P_DM1	134 10			
DQS10N_NC	135		10	
DQS9P_DM0	125 9			
DQS9N_NC	126		9	
DQS8P	43 8			
DQS8N	42		8	
DQS7P	112 7			
DQS7N	111		7	
DQS6P	103 6			
DQS6N	102		6	
DQS5P	94 5			
DQS5N	93		5	
DQS4P	85 4			
DQS4N	84		4	
DQS3P	34 3			
DQS3N	33		3	
DQS2P	25 2			
DQS2N	24		2	
DQS1P	16 1			
DQS1N	15		1	
DQS0P	7 0			
DQS0N	6		0	

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DDR3 CPU3 CHANNEL R DIMM1

DEPARTMENT			SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119		B	34649	444359	1.0
			SCALE:	DO NOT SCALE DRAWING		SHEET 117 OF 303

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J6E1

CONN240_E55582004

106>	IN	M_T_BA<2>		52	A16_BA2	DQ<63>	234 63
			15	171	A<15>	DQ<62>	233 62
			14	172	A<14>	DQ<61>	228 61
			13	196	A<13>	DQ<60>	227 60
			12	174	A<12>	DQ<59>	115 59
			11	55	A<11>	DQ<58>	114 58
			10	70	A<10>	DQ<57>	109 57
			9	175	A<9>	DQ<56>	108 56
			8	177	A<8>	DQ<55>	225 55
			7	56	A<7>	DQ<54>	224 54
			6	178	A<6>	DQ<53>	219 53
			5	58	A<5>	DQ<52>	218 52
			4	59	A<4>	DQ<51>	106 51
			3	180	A<3>	DQ<50>	105 50
			2	61	A<2>	DQ<49>	100 49
			1	181	A<1>	DQ<48>	99 48
106>	IN	M_T_MA<15..0>	0	188	A<0>	DQ<47>	216 47
106>	IN	M_T_BA<1..0>				DQ<46>	215 46
			1	190	BA<1>	DQ<45>	210 45
			0	71	BA<0>	DQ<44>	209 44
						DQ<43>	97 43
106>	IN	M_T_CK_DP<2>		63	NC_CK1P	DQ<42>	96 42
106>	IN	M_T_CK_DN<2>		64	NC_CK1N	DQ<41>	91 41
106>	IN	M_T_CK_DP<0>		184	CK0P	DQ<40>	90 40
106>	IN	M_T_CK_DN<0>		185	CK0N	DQ<39>	207 39
106>	IN	M_T_CS_N<3..0>				DQ<38>	206 38
			3	198	CS<3>	DQ<37>	201 37
			2	79	CS<2>	DQ<36>	200 36
			1	76	CS<1>	DQ<35>	88 35
			0	193	CS<0>	DQ<34>	87 34
						DQ<33>	82 33
106>	IN	M_T_CKE<1>		169	CKE<1>	DQ<32>	81 32
106>	IN	M_T_CKE<0>		50	CKE<0>	DQ<31>	156 31
						DQ<30>	155 30
106>	IN	M_T_WE_N		73	WE_N	DQ<29>	150 29
106>	IN	M_T_RAS_N		192	RAS_N	DQ<28>	149 28
106>	IN	M_T_CAS_N		74	CAS_N	DQ<27>	37 27
106>	IN	M_T_ODT<1..0>				DQ<26>	36 26
			1	77	ODT<1>	DQ<25>	31 25
			0	195	ODT<0>	DQ<24>	30 24
						DQ<23>	147 23
106>	IN	M_T_MA_PAR		68	PAR_IN_NC	DQ<22>	146 22
106<	OUT	M_T_PAR_ERR_N<0>		53	ERR_OUT_NC	DQ<21>	141 21
106<>	BI	M_T_ECC<7..0>				DQ<20>	140 20
			7	165	CB<7>	DQ<19>	28 19
			6	164	CB<6>	DQ<18>	27 18
			5	159	CB<5>	DQ<17>	22 17
			4	158	CB<4>	DQ<16>	21 16
			3	46	CB<3>	DQ<15>	138 15
			2	45	CB<2>	DQ<14>	137 14
			1	40	CB<1>	DQ<13>	132 13
			0	39	CB<0>	DQ<12>	131 12
						DQ<11>	19 11
117<	102> IN	M_RT_RESET_LVC1V5_N		168	RESET_N	DQ<10>	18 10
						DQ<9>	13 9
				236	VDDSPD	DQ<8>	12 8
				119	SA<2>	DQ<7>	129 7
				237	SA<1>	DQ<6>	128 6
				117	SA<0>	DQ<5>	123 5
201>	119<> 117<> BI	SMB_DDR_RT_LVC3_SDA		238	SDA	DQ<4>	122 4
201<>	119< 117< IN	SMB_DDR_RT_LVC3_SCL		118	SCL	DQ<3>	10 3
206<	189> 100< OUT	FM_SKT3_DIMM_T1_EVENT_N		187	EVENT_N_NC	DQ<2>	9 2
119>	118> IN	P1V5_DDR3_CPU3_VREF_T_D		1	VREFDQ	DQ<1>	4 1
	118> IN	P1V5_DDR3_CPU3_VREF_T_A		67	VREFCA	DQ<0>	3 0

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M_T_DQ<63..0> BI 106<>

P3V3

3.3 — R6B20 1/16W 1K 1% 0402LF — A93548-023 — SPD ADDRESS = 0XA8 — M_T_SA<2>

J6E1

CONN240_E55582004

2	VSS<58>	VDD<21>	51	P1V5_DDR3_CPU3 1.5
5	VSS<57>	VDD<20>	54	
8	VSS<56>	VDD<19>	57	
11	VSS<55>	VDD<18>	60	
14	VSS<54>	VDD<17>	62	
17	VSS<53>	VDD<16>	65	
20	VSS<52>	VDD<15>	66	
23	VSS<51>	VDD<14>	69	
26	VSS<50>	VDD<13>	72	
29	VSS<49>	VDD<12>	75	
32	VSS<48>	VDD<11>	78	
35	VSS<47>	VDD<10>	170	
38	VSS<46>	VDD<9>	173	
41	VSS<45>	VDD<8>	176	
44	VSS<44>	VDD<7>	179	
47	VSS<43>	VDD<6>	182	
80	VSS<42>	VDD<5>	183	
83	VSS<41>	VDD<4>	186	
86	VSS<40>	VDD<3>	189	P0V75_VTT_DDR3_CPU3
89	VSS<39>	VDD<2>	191	
92	VSS<38>	VDD<1>	194	
95	VSS<37>	VDD<0>	197	0.75
98	VSS<36>			
101	VSS<35>	VTT<3>	49	
104	VSS<34>	VTT<2>	48	
107	VSS<33>	VTT<1>	120	
110	VSS<32>	VTT<0>	240	
113	VSS<31>			
116	VSS<30>			
121	VSS<29>	NC_TEST	167	TP_T_D1_NC2
124	VSS<28>			
127	VSS<27>			
130	VSS<26>			
133	VSS<25>			
136	VSS<24>			
139	VSS<23>			
142	VSS<22>			
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223	VSS<5>			
226	VSS<4>			
229	VSS<3>			
232	VSS<2>			
235	VSS<1>			
239	VSS<0>			

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E55582-004

P1V5_DDR3_CPU3 — 1.5 — C6C5 10UF 6.3V 20% 602433-075 0603LF — C6C6 10UF 6.3V 20% 602433-075 0603LF

J6E1

CONN240_E55582004

DQS17P_DM8	161	17	M_T_DQS_DP<17..0> BI 106<>
DQS17N_NC	162	17	M_T_DQS_DN<17..0> BI 106<>
DQS16P_DM7	230	16	
DQS16N_NC	231	16	
DQS15P_DM6	221	15	
DQS15N_NC	222	15	
DQS14P_DM5	212	14	
DQS14N_NC	213	14	
DQS13P_DM4	203	13	
DQS13N_NC	204	13	
DQS12P_DM3	152	12	
DQS12N_NC	153	12	
DQS11P_DM2	143	11	
DQS11N_NC	144	11	
DQS10P_DM1	134	10	
DQS10N_NC	135	10	
DQS9P_DM0	125	9	
DQS9N_NC	126	9	
DQS8P	43	8	
DQS8N	42	8	
DQS7P	112	7	
DQS7N	111	7	
DQS6P	103	6	
DQS6N	102	6	
DQS5P	94	5	
DQS5N	93	5	
DQS4P	85	4	
DQS4N	84	4	
DQS3P	34	3	
DQS3N	33	3	
DQS2P	25	2	
DQS2N	24	2	
DQS1P	16	1	
DQS1N	15	1	
DQS0P	7	0	
DQS0N	6	0	

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P1V5_DDR3_CPU3 — R6E3 100 1% 1/16W — A93548-043 0402LF — 1.5 — 0.75 — P1V5_DDR3_CPU3_VREF_T_D OUT 118< 119> — R6E4 100 1% 1/16W — A93548-043 0402LF — C6E2 0.1UF 16V 10% — A36096-030 0402LF

P1V5_DDR3_CPU3 — R6C7 100 1% 1/16W — A93548-043 0402LF — 1.5 — 0.75 — P1V5_DDR3_CPU3_VREF_T_A OUT 118< — R6C8 100 1% 1/16W — A93548-043 0402LF — C6C1 0.1UF 16V 10% — A36096-030 0402LF

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DDR3 CPU3 CHANNEL T DIMM1

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 118 OF 303	

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ROOM = VREFDQ_CPU3

P3V3_AUX NEEDED FOR POT
IF DESIGN SUPPORT S3

P3V3 3.3

DECOUPLING CAP
CAD NOTE:
PLACE CLOSE TO CHIP

C3E7 0.1UF 0402LF 16V X7R 10% A36096-030 VREFDQ_CPU3

R3E10 0 CHIP A93549-001 VREFDQ_CPU3 0402LF 5% 1/16W

201<> 116< 115< IN SMB_DDR_NP_LVC3_SCL — SMB_DDR_NP_DAC_LVC3_SCL

201> 116<> 115<> BI SMB_DDR_NP_LVC3_SDA — SMB_DDR_NP_DAC_LVC3_SDA

R3E11 0 CHIP A93549-001 VREFDQ_CPU3 0402LF 5% 1/16W

U3E3 VREFDQ_CPU3
ISL90727
VCC SCL SDA GND RW RH
E47385-001
SMBUS ADDRESS=0X5C

CONNECTION TO THE P1V5_DDR3_CPU3
VOLTAGE RAIL SHOULD BE NEAR THE
P1V5_DDR3VR SENSE POINT

P1V5_DDR3_CPU3 1.5

P1V5_DDR3_CPU3_VREF_NP_RW 0.75

R3E8 12.1K 1% 1/16W CHIP 0402LF A93548-018 VREFDQ_CPU3

R3E9 12.1K 1% 1/16W 0402LF A93548-018 VREFDQ_CPU3

WRITE VREF FROM CPU TO THE DIMMS

102> IN P1V5_DDR3_NP_VREFDQTX

R7R2 A93549-001 0402LF 5% 1/16W VREFDQ_CPU3

P1V5_DDR3_CPU3_VREF_NP_OPFB

U3E2
LMV321
INN INP VSN VSP OUT
E21441-001 VREFDQ_CPU3

R3E6 2.20 CHIP A93549-051 VREFDQ_CPU3 0402LF 5% 1/16W

P1V5_DDR3_CPU3_VREF_NP_D 0.75

R3E7 100 1% 1/16W CHIP 0402LF A93548-043 VREFDQ_CPU3

C3E6 1.0UF 6.3V 10% EMPTY A36096-027 0402LF VREFDQ_CPU3

R3E5 0 CHIP A93549-001 VREFDQ_CPU3 0402LF 5% 1/16W

P1V5_DDR3_CPU3_VREF_N_D 0.75 OUT 115< 115<

R7R1 0 CHIP A93549-001 VREFDQ_CPU3 0402LF 5% 1/16W

P1V5_DDR3_CPU3_VREF_P_D 0.75 OUT 116< 116<

DDR3 PROCESSOR VREF GENERATION

P1V5_DDR3_CPU3 1.5

R4C8 100 1% 1/16W A93548-043 0402LF VREFDQ_CPU3

0.75

P1V5_DDR3_NP_VREFDQRX OUT 102<

R4C7 100 1% 1/16W A93548-043 0402LF VREFDQ_CPU3

C4C2 0.1UF 16V 10% A36096-030 0402LF VREFDQ_CPU3

CAD NOTE:
PLACE CIRCUIT AS CLOSE AS POSSBIBLE TO CPU
REFER TO RS-ROMLEY PDG FOR LATEST GUIDELINE
FROM ROMLEY PDG:
NOMIMAL TRACE WIDTH = 10 MILS
NOMIMAL TRACE SPACING = 20 MILS
CPU BREAKOUT REQ = 4-MIL WIDTH / 4-MIL SPACING
THE DECOUPLING CAP RECOMMENDED IS 0603 0.1UF

DECOUPLING CAP
CAD NOTE:
PLACE CLOSE TO CHIP

P5V

C7R1 1UF 16V 10% X5R 644066-061 0805LF VREFDQ_CPU3

P5V_AUX NEEDED FOR OP AMP
IF DESIGN SUPPORT S3

REVIEW DATASHEET OF OPAMP FOR CORRECT DECOUPLING VALUES

P3V3_AUX NEEDED FOR POT
IF DESIGN SUPPORT S3

P3V3 3.3

DECOUPLING CAP
CAD NOTE:
PLACE CLOSE TO CHIP

C7A7 0.1UF 0402LF 16V X7R 10% A36096-030 VREFDQ_CPU3

R7A24 0 CHIP A93549-001 VREFDQ_CPU3 0402LF 5% 1/16W

201<> 118< 117< IN SMB_DDR_RT_LVC3_SCL — SMB_DDR_RT_DAC_LVC3_SCL

201> 118<> 117<> BI SMB_DDR_RT_LVC3_SDA — SMB_DDR_RT_DAC_LVC3_SDA

R7A12 0 CHIP A93549-001 VREFDQ_CPU3 0402LF 5% 1/16W

U7A2 VREFDQ_CPU3
ISL90727
VCC SCL SDA GND RW RH
E47385-001
SMBUS ADDRESS=0X5C

CONNECTION TO THE P1V5_DDR3_CPU3
VOLTAGE RAIL SHOULD BE NEAR THE
P1V5_DDR3VR SENSE POINT

P1V5_DDR3_CPU3 1.5

P1V5_DDR3_CPU3_VREF_RT_RW 0.75

R7A13 12.1K 1% 1/16W CHIP 0402LF A93548-018 VREFDQ_CPU3

R7A11 12.1K 1% 1/16W 0402LF A93548-018 VREFDQ_CPU3

WRITE VREF FROM CPU TO THE DIMMS

102> IN P1V5_DDR3_RT_VREFDQTX

R3L11 A93549-001 0402LF 5% 1/16W VREFDQ_CPU3

P1V5_DDR3_CPU3_VREF_RT_OPFB

U7A1
LMV321
INN INP VSN VSP OUT
E21441-001 VREFDQ_CPU3

R7A22 2.20 CHIP A93549-051 VREFDQ_CPU3 0402LF 5% 1/16W

P1V5_DDR3_CPU3_VREF_RT_D 0.75

R7A21 100 1% 1/16W CHIP 0402LF A93548-043 VREFDQ_CPU3

C7A5 1.0UF 6.3V 10% EMPTY A36096-027 0402LF VREFDQ_CPU3

R7A23 0 CHIP A93549-001 VREFDQ_CPU3 0402LF 5% 1/16W

P1V5_DDR3_CPU3_VREF_R_D 0.75 OUT 117< 117>

R3L14 0 CHIP A93549-001 VREFDQ_CPU3 0402LF 5% 1/16W

P1V5_DDR3_CPU3_VREF_T_D 0.75 OUT 118< 118>

DDR3 PROCESSOR VREF GENERATION

P1V5_DDR3_CPU3 1.5

R6C6 100 1% 1/16W A93548-043 0402LF VREFDQ_CPU3

0.75

P1V5_DDR3_RT_VREFDQRX OUT 102<

R6C3 100 1% 1/16W A93548-043 0402LF VREFDQ_CPU3

C6B10 0.1UF 16V 10% A36096-030 0402LF VREFDQ_CPU3

CAD NOTE:
PLACE CIRCUIT AS CLOSE AS POSSIBLE TO CPU
REFER TO RS-ROMLEY PDG FOR LATEST GUIDELINE
FROM ROMLEY PDG:
NOMIMAL TRACE WIDTH = 10 MILS
NOMIMAL TRACE SPACING = 20 MILS
CPU BREAKOUT REQ = 4-MIL WIDTH / 4-MIL SPACING
THE DECOUPLING CAP RECOMMENDED IS 0603 0.1UF

DECOUPLING CAP
CAD NOTE:
PLACE CLOSE TO CHIP

P5V

C3L10 1UF 16V 10% X5R 644066-061 0805LF VREFDQ_CPU3

P5V_AUX NEEDED FOR OP AMP
IF DESIGN SUPPORT S3

REVIEW DATASHEET OF OPAMP FOR CORRECT DECOUPLING VALUES

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CPU3 DDR3 DQ REFERENCE

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 119 OF 303

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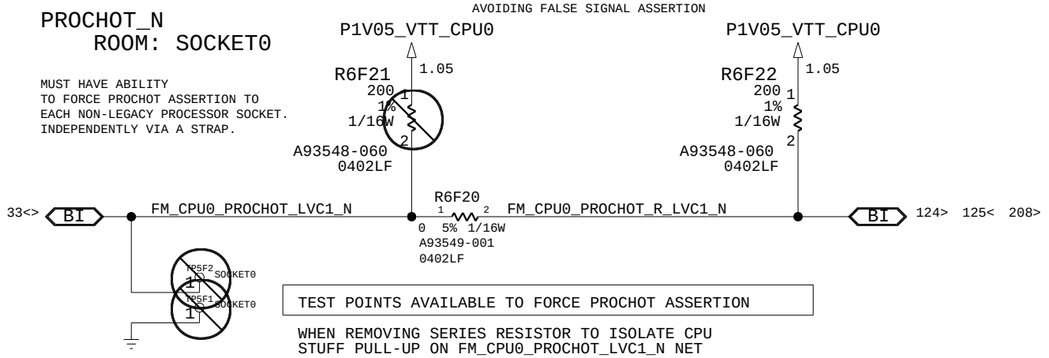
PROCHOT_N

PROCHOT_N ROOM: SOCKET0

MUST HAVE ABILITY
TO FORCE PROCHOT ASSERTION TO
EACH NON-LEGACY PROCESSOR SOCKET.
INDEPENDENTLY VIA A STRAP.

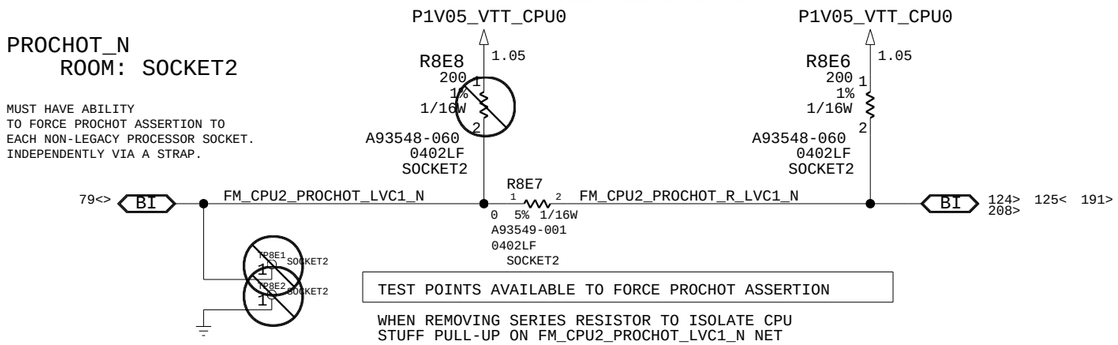
VTT_CPU0 USED SINCE IT IS ALWAYS PRESENT
AVOIDING FALSE SIGNAL ASSERTION



PROCHOT_N ROOM: SOCKET2

MUST HAVE ABILITY
TO FORCE PROCHOT ASSERTION TO
EACH NON-LEGACY PROCESSOR SOCKET.
INDEPENDENTLY VIA A STRAP.

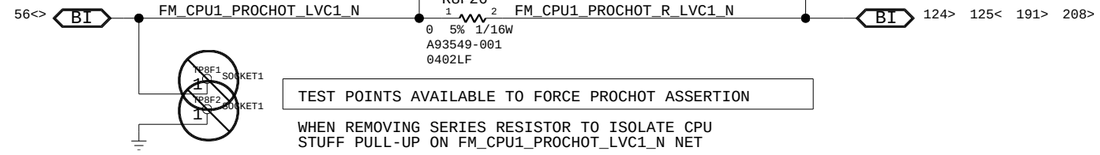
VTT_CPU0 USED SINCE IT IS ALWAYS PRESENT
AVOIDING FALSE SIGNAL ASSERTION



PROCHOT_N ROOM: SOCKET1

MUST HAVE ABILITY
TO FORCE PROCHOT ASSERTION TO
EACH NON-LEGACY PROCESSOR SOCKET.
INDEPENDENTLY VIA A STRAP.

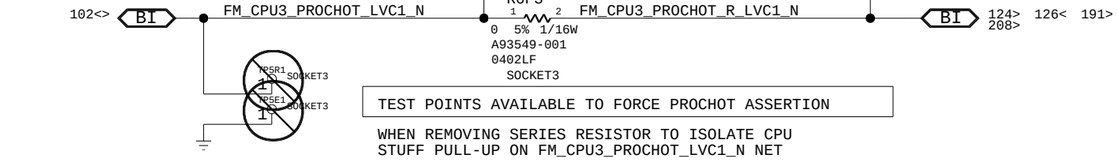
VTT_CPU0 USED SINCE IT IS ALWAYS PRESENT
AVOIDING FALSE SIGNAL ASSERTION



PROCHOT_N ROOM: SOCKET3

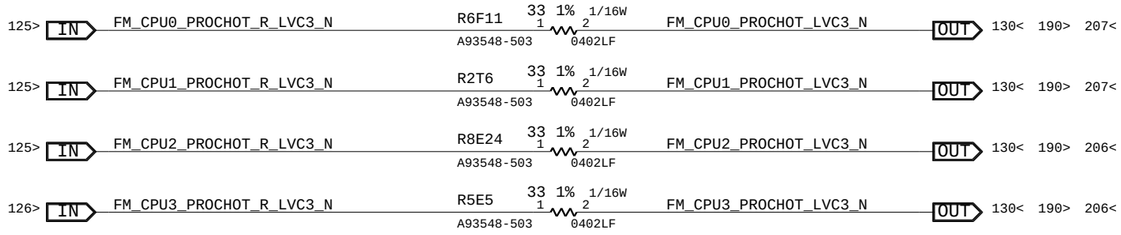
MUST HAVE ABILITY
TO FORCE PROCHOT ASSERTION TO
EACH NON-LEGACY PROCESSOR SOCKET.
INDEPENDENTLY VIA A STRAP.

VTT_CPU0 USED SINCE IT IS ALWAYS PRESENT
AVOIDING FALSE SIGNAL ASSERTION



PROCHOT

CAD NOTE: PLACE SERIES RESISTORS AS CLOSE AS POSSIBLE TO THE OUTPUT
OF THEIR CORRESSPONDING VOLTAGE TRANSLATOR GTL2107: WITHIN 0.5"



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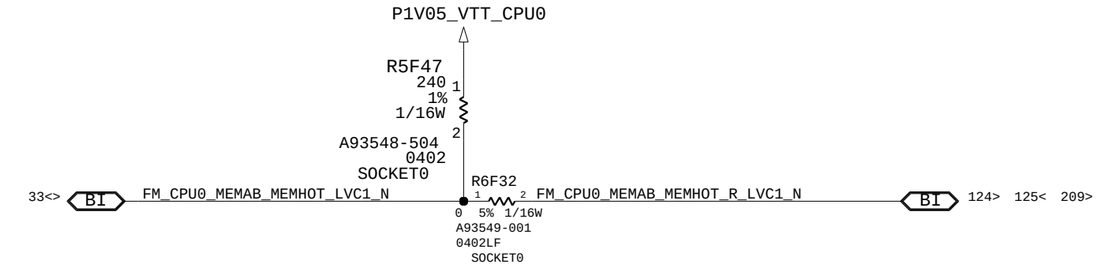
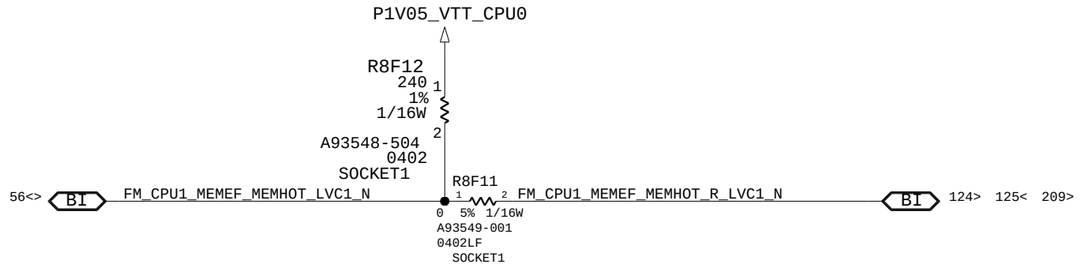
CPU SIDEBAND: PROCHOT_N CIRCUITRY

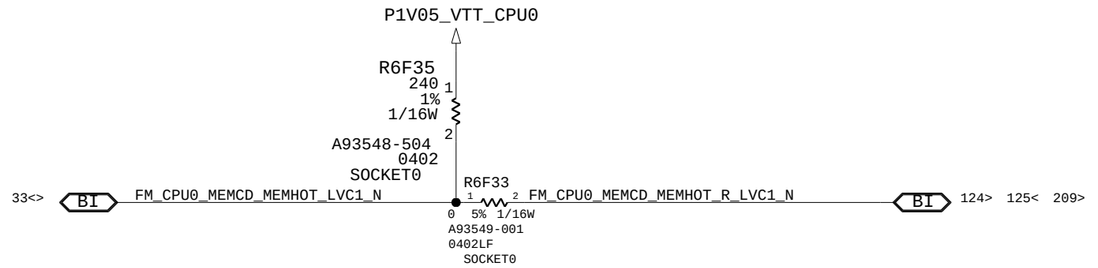
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 122 OF 303	

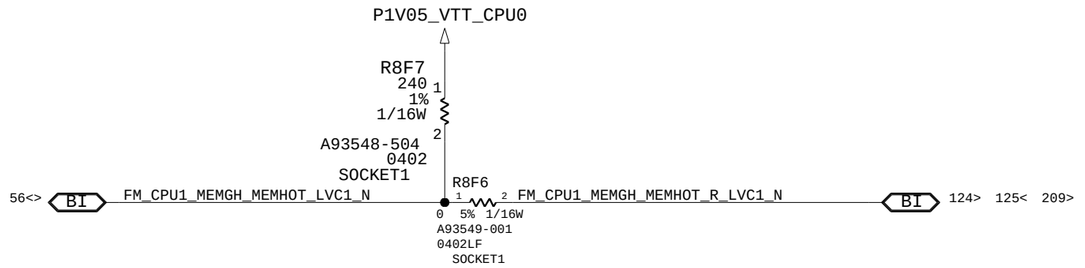
INTEL CONFIDENTIAL

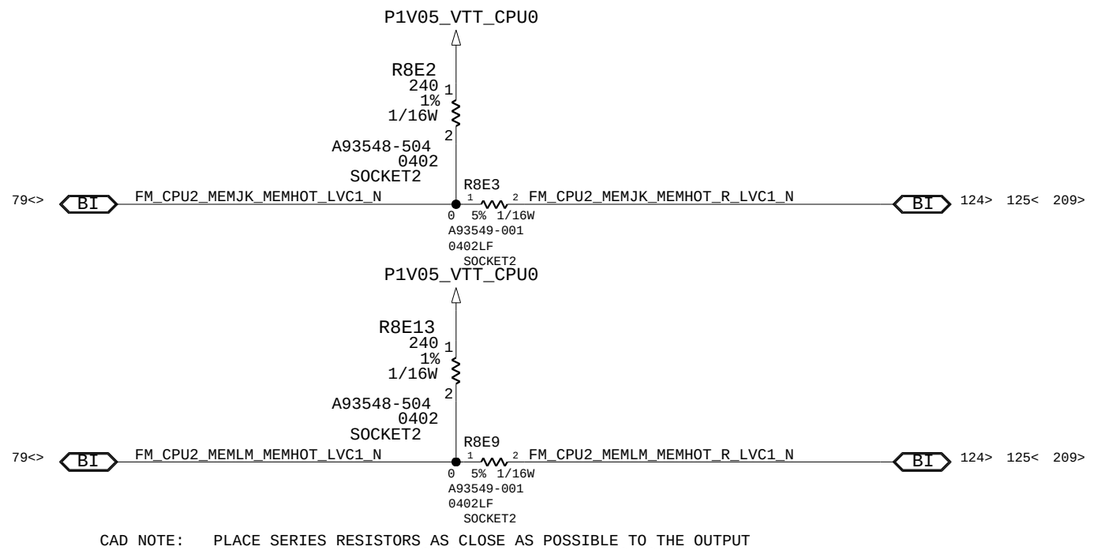
MEMHOT

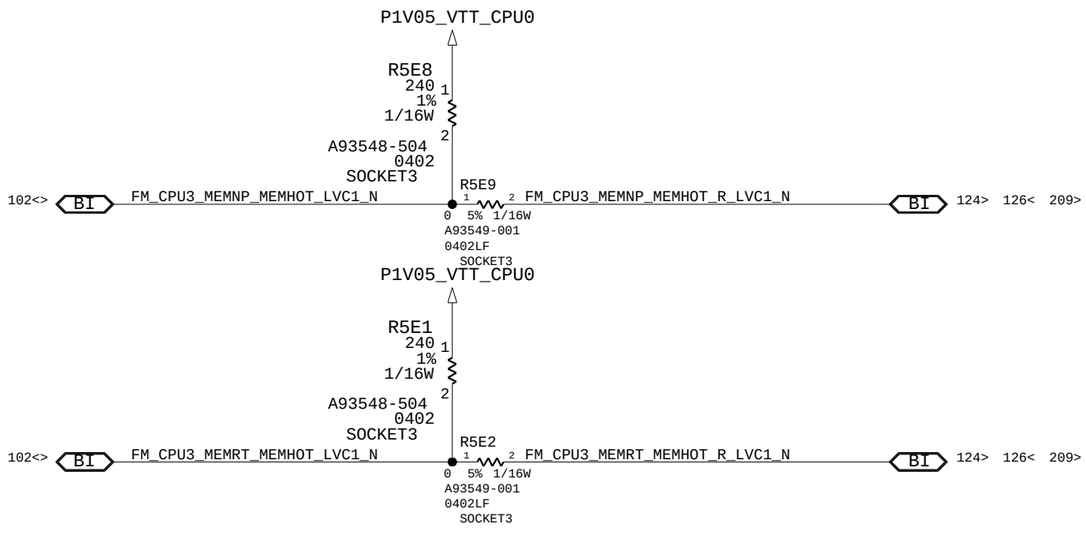




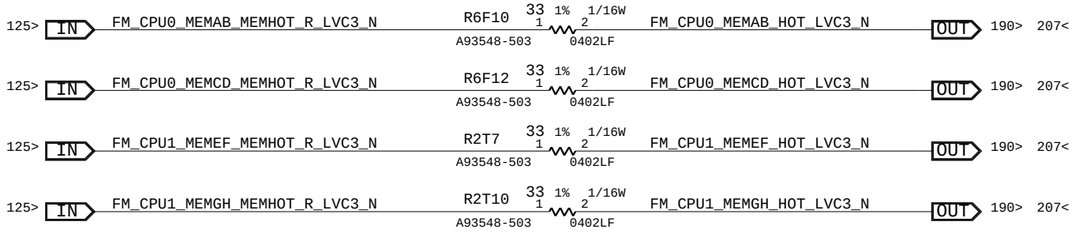


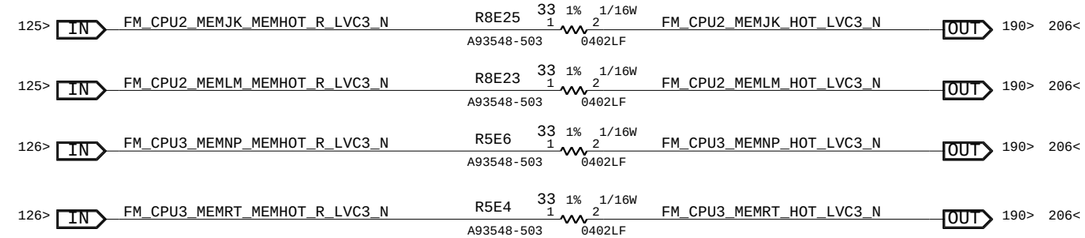






CAD NOTE: PLACE SERIES RESISTORS AS CLOSE AS POSSIBLE TO THE OUTPUT OF THEIR CORRESSPONDING VOLTAGE TRANSLATOR GTL2107





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CPU SIDEBAND: MEMHOT_N CIRCUITRY

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 123 OF 303	

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CPU SIDEBAND: THROTLE CIRCUITRY

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 124 OF 303	

INTEL CONFIDENTIAL

VREF: (2/3)*VTT
WORST CASE FOR VREF WHEN IVB: (2/3)*0.95V

P3V3_STBY
1.05
R6F16
422 1% 1/16W
A93548-092 0402LF
DECOUPLING CAP
CAD NOTE:
PLACE CLOSE TO
VOLTAGE TRANSLATOR
P3V3_STBY
3.3
C6F6 1UF 10V 10%
A36096-099 0402LF
0.63V
P0V7_CPU0_VTT_VREF
OUT 125<
R6F13 100 1% 1/16W
A93548-043 0402LF
C6F3 0.1UF 16V 10%
A36096-030 0402LF
VREF: CONSIDERING LOWEST VTT_IVB = 0.95V AS WORST CASE
VREF: (2/3)*VTT_IVB_MIN = 0.63V

125> IN P0V7_CPU0_VTT_VREF 1
99> IN IRQ_CPU_CATERR_R_LVC1_N 27
209> 124> 123<> IN FM_CPU0_MEMCD_MEMHOT_R_LVC1_N 26
100> IN FM_CPU0_THERMTRIP_R_LVC1_N 19
54> 33> IN FM_CPU0_IVT_ID_LVC1_N 18
208> 124> 122<> IN FM_CPU0_PROCHOT_R_LVC1_N 21
TP_CPU0_GTL2107_UNUSED_25_LVC1 25
209> 124> 123<> IN FM_CPU0_MEMAB_MEMHOT_R_LVC1_N 20
TP_CPU0_GTL2107_UNUSED_24_LVC1 24
134> 102<> 79<> 56<> 33<> IN RST_CPU_EAR_LVC1_N 9
TP_CPU0_GTL2107_UNUSED_12_LVC1 12
TP_CPU0_GTL2107_UNUSED_13_LVC1 13
TP_CPU0_GTL2107_UNUSED_7_LVC1 7

U6F4
GTL2107
VREF
1BI 1AO 2 IRQ_CPU_CATERR_R_LVC3_N OUT 99<
2BI 2AO 3 FM_CPU0_MEMCD_MEMHOT_R_LVC3_N OUT 123<
3BI 3AO 10 FM_CPU0_THERMTRIP_R_LVC3_N OUT 100<
4BI 4AO 11 FM_CPU0_IVT_ID_LVC3_N OUT 170< 206< 265<
5BI 5A 4 FM_CPU0_PROCHOT_R_LVC3_N OUT 122<
7BO1
6BI 6A 5 FM_CPU0_MEMAB_MEMHOT_R_LVC3_N OUT 123<
7BO2
EN2 23 FM_CPU0_GTL2107_LVC3_EN
EN1 6
9BI 9AO 15 RST_CPU_EAR_LVC3_N OUT 169<
10AI1 10BO1 17 TP_CPU0_GTL2107_UNUSED_17_LVC1
10AI2 10BO2 16 TP_CPU0_GTL2107_UNUSED_16_LVC1
11BI 11BO 22 TP_CPU0_GTL2107_UNUSED_22_LVC1
11A 8 TP_CPU0_GTL2107_UNUSED_8_LVC1
D78251-001
GND=GND; VCC=P3V3_STBY;

P3V3_STBY
R6F9 10.0K 1% 1/16W A93548-034 0402LF
3.3
RST_CPU_EAR_LVC3_N IS PUSH PULL

P3V3_STBY
1.05
R2T9
422 1% 1/16W
A93548-092 0402LF SOCKET1
DECOUPLING CAP
CAD NOTE:
PLACE CLOSE TO
VOLTAGE TRANSLATOR
P3V3_STBY
3.3
C8F2 1UF 10V 10%
A36096-099 0402LF SOCKET1
0.63V
P0V7_CPU1_VTT_VREF
OUT 125<
R8F3 100 1% 1/16W
A93548-043 0402LF SOCKET1
C8F1 0.1UF 16V 10%
A36096-030 0402LF SOCKET1

125> IN P0V7_CPU1_VTT_VREF 1
TP_CPU1_GTL2107_UNUSED_27_LVC1 27
209> 124> 123<> IN FM_CPU1_MEMGH_MEMHOT_R_LVC1_N 26
100> IN FM_CPU1_THERMTRIP_R_LVC1_N 19
56> 54> IN FM_CPU1_IVT_ID_LVC1_N 18
191> 124> 122<> 208> IN FM_CPU1_PROCHOT_R_LVC1_N 21
TP_CPU1_GTL2107_UNUSED_25_LVC1 25
209> 124> 123<> IN FM_CPU1_MEMEF_MEMHOT_R_LVC1_N 20
TP_CPU1_GTL2107_UNUSED_24_LVC1 24
TP_CPU1_GTL2107_UNUSED_9_LVC1 9
TP_CPU1_GTL2107_UNUSED_12_LVC1 12
TP_CPU1_GTL2107_UNUSED_13_LVC1 13
TP_CPU1_GTL2107_UNUSED_7_LVC1 7

U8F2
SOCKET1
GTL2107
VREF
1BI 1AO 2 TP_CPU1_GTL2107_UNUSED_2_LVC1
2BI 2AO 3 FM_CPU1_MEMGH_MEMHOT_R_LVC3_N OUT 123<
3BI 3AO 10 FM_CPU1_THERMTRIP_R_LVC3_N OUT 100<
4BI 4AO 11 FM_CPU1_IVT_ID_LVC3_N OUT 170< 206< 266<
5BI 5A 4 FM_CPU1_PROCHOT_R_LVC3_N OUT 122<
7BO1
6BI 6A 5 FM_CPU1_MEMEF_MEMHOT_R_LVC3_N OUT 123<
7BO2
EN2 23 FM_CPU1_GTL2107_LVC3_EN
EN1 6
9BI 9AO 15 TP_CPU1_GTL2107_UNUSED_15_LVC1
10AI1 10BO1 17 TP_CPU1_GTL2107_UNUSED_17_LVC1
10AI2 10BO2 16 TP_CPU1_GTL2107_UNUSED_16_LVC1
11BI 11BO 22 TP_CPU1_GTL2107_UNUSED_22_LVC1
11A 8 TP_CPU1_GTL2107_UNUSED_8_LVC1
D78251-001
GND=GND; VCC=P3V3_STBY;

P3V3_STBY
R2T11 10.0K 1% 1/16W A93548-034 0402LF SOCKET0
3.3

P3V3_STBY
1.05
R2R24
422 1% 1/16W
A93548-092 0402LF SOCKET2
DECOUPLING CAP
CAD NOTE:
PLACE CLOSE TO
VOLTAGE TRANSLATOR
P3V3_STBY
3.3
C2R5 1UF 10V 10%
A36096-099 0402LF SOCKET2
0.63V
P0V7_CPU2_VTT_VREF
OUT 125<
R2R23 100 1% 1/16W
A93548-043 0402LF SOCKET2
C2R8 0.1UF 16V 10%
A36096-030 0402LF SOCKET2

125> IN P0V7_CPU2_VTT_VREF 1
TP_CPU2_GTL2107_UNUSED_27_LVC1 27
209> 124> 123<> IN FM_CPU2_MEMLM_MEMHOT_R_LVC1_N 26
100> IN FM_CPU2_THERMTRIP_R_LVC1_N 19
79> 54> IN FM_CPU2_IVT_ID_LVC1_N 18
208> 191> 124> 122<> IN FM_CPU2_PROCHOT_R_LVC1_N 21
TP_CPU2_GTL2107_UNUSED_25_LVC1 25
209> 124> 123<> IN FM_CPU2_MEMJK_MEMHOT_R_LVC1_N 20
TP_CPU2_GTL2107_UNUSED_24_LVC1 24
TP_CPU2_GTL2107_UNUSED_9_LVC1 9
TP_CPU2_GTL2107_UNUSED_12_LVC1 12
TP_CPU2_GTL2107_UNUSED_13_LVC1 13
TP_CPU2_GTL2107_UNUSED_7_LVC1 7

U8E3
SOCKET2
GTL2107
VREF
1BI 1AO 2 TP_CPU2_GTL2107_UNUSED_2_LVC1
2BI 2AO 3 FM_CPU2_MEMLM_MEMHOT_R_LVC3_N OUT 123<
3BI 3AO 10 FM_CPU2_THERMTRIP_R_LVC3_N OUT 100<
4BI 4AO 11 FM_CPU2_IVT_ID_LVC3_N OUT 170< 206< 267<
5BI 5A 4 FM_CPU2_PROCHOT_R_LVC3_N OUT 122<
7BO1
6BI 6A 5 FM_CPU2_MEMJK_MEMHOT_R_LVC3_N OUT 123<
7BO2
EN2 23 FM_CPU2_GTL2107_LVC3_EN
EN1 6
9BI 9AO 15 TP_CPU2_GTL2107_UNUSED_15_LVC1
10AI1 10BO1 17 TP_CPU2_GTL2107_UNUSED_17_LVC1
10AI2 10BO2 16 TP_CPU2_GTL2107_UNUSED_16_LVC1
11BI 11BO 22 TP_CPU2_GTL2107_UNUSED_22_LVC1
11A 8 TP_CPU2_GTL2107_UNUSED_8_LVC1
D78251-001
GND=GND; VCC=P3V3_STBY;

P3V3_STBY
R8E26 10.0K 1% 1/16W A93548-034 0402LF SOCKET0
3.3

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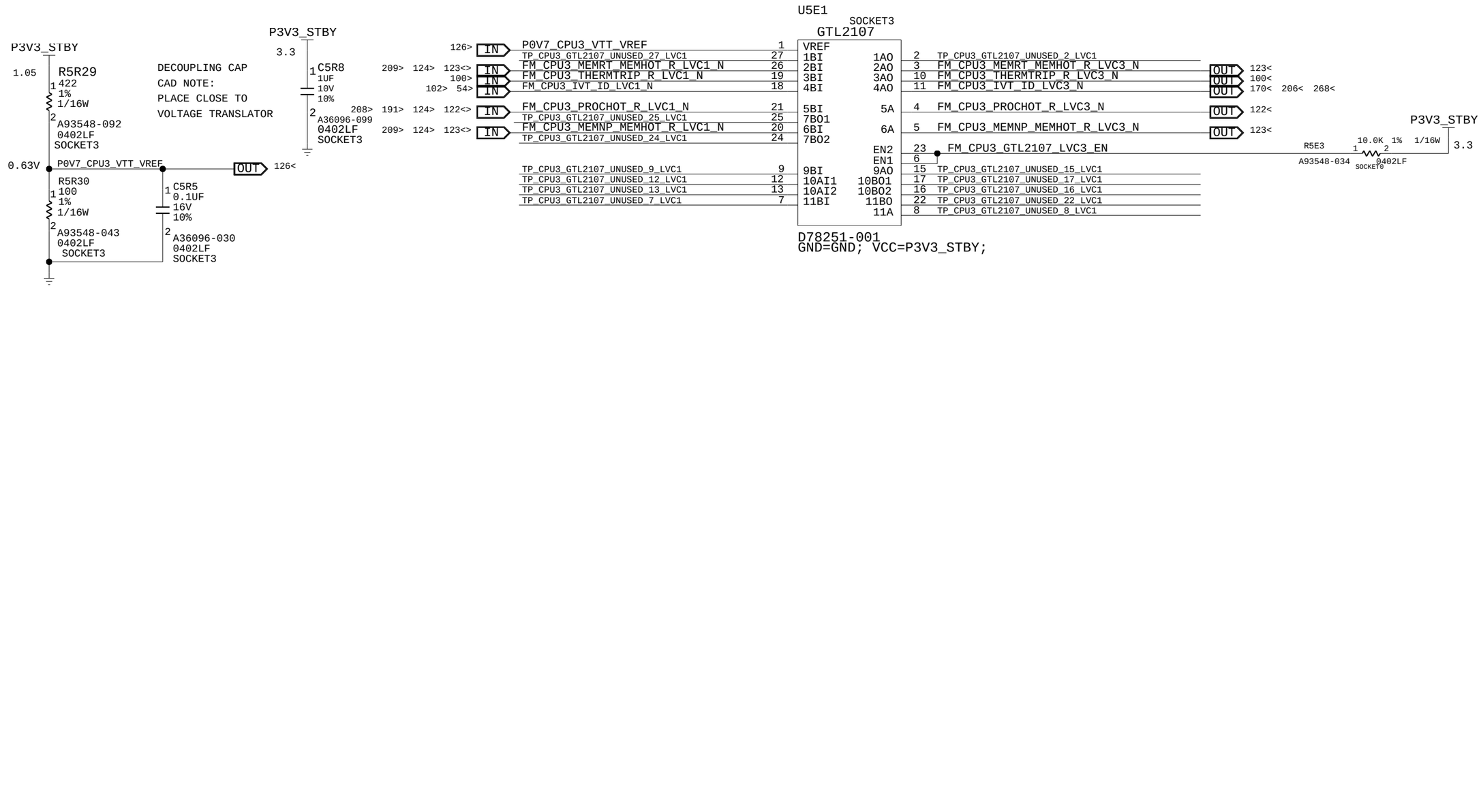
CPU MISC: GTL TO TTL CONVERTERS (1 OF 2)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 125 OF 303	

INTEL CONFIDENTIAL



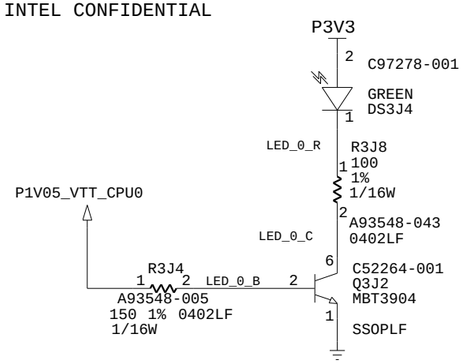
CPU MISC: GTL TO TTL CONVERTERS (2 OF 2)

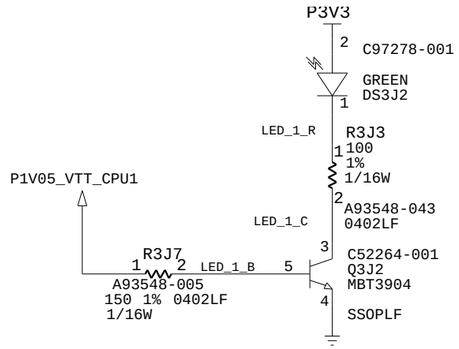
Wed Oct 27 15:21:38 2010

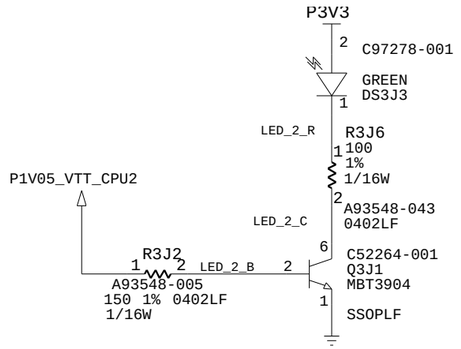
DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 126 OF 303

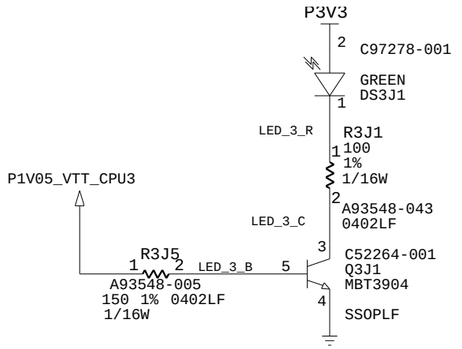
DEBUG
CR-127 : @POTTERCITY_LIB.POTTERCITY(SCH_1):PAGE127

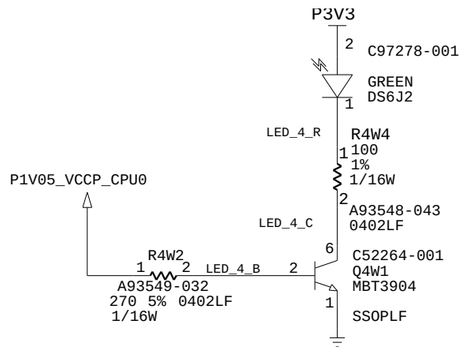
INTEL CONFIDENTIAL

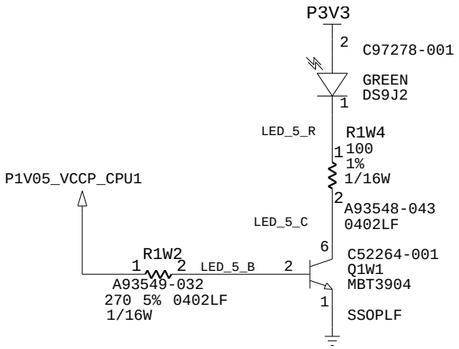


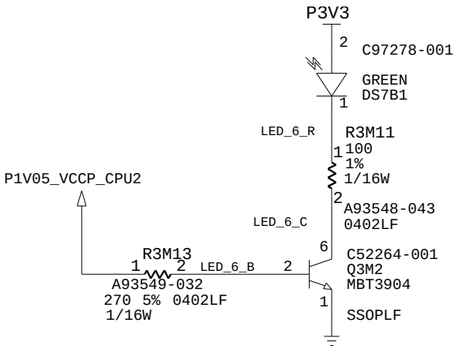


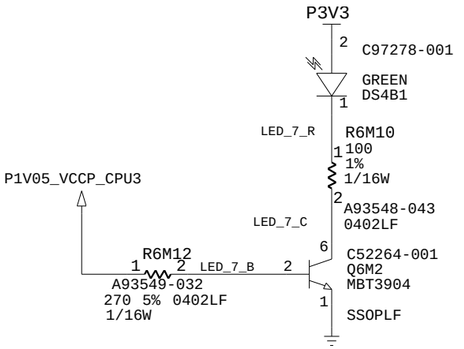


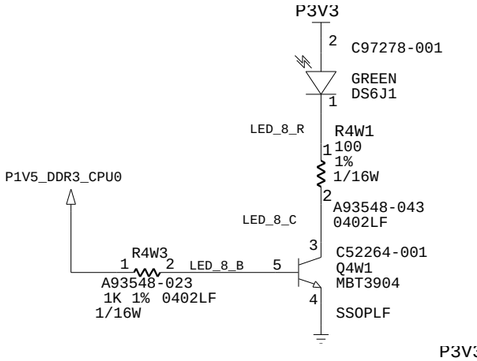


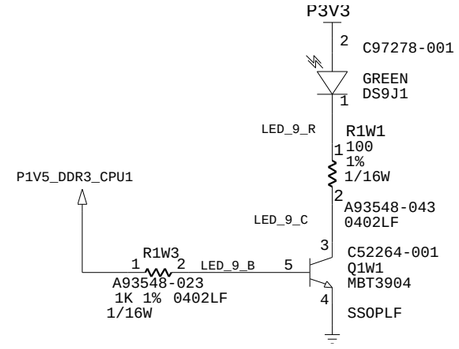


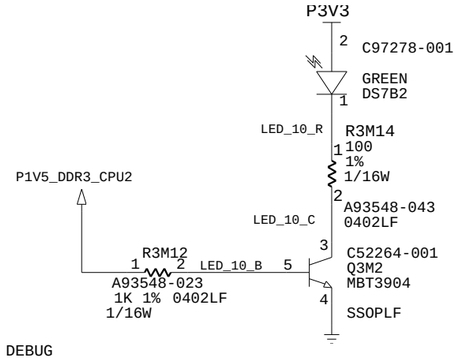


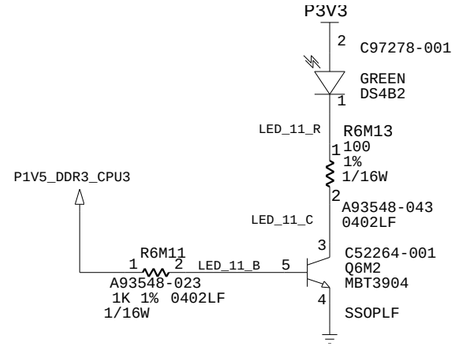


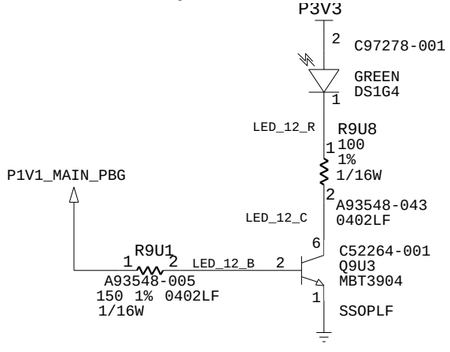


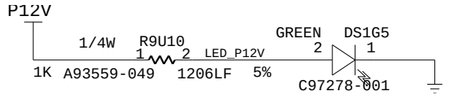


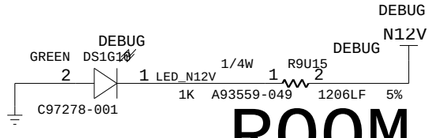


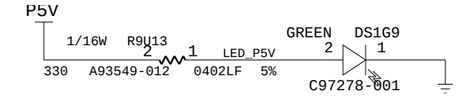


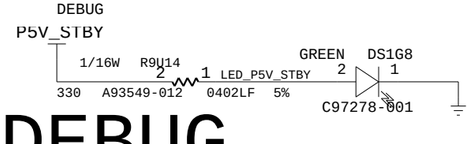


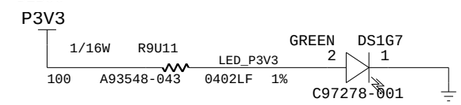


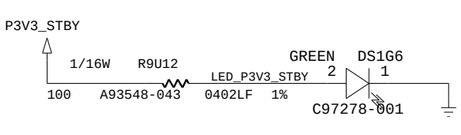












ROOM = DEBUG

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PROC DEBUG LEDS (1 OF 4)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 127 OF 303	

INTEL CONFIDENTIAL

ROOM = DEBUG

PROC DEBUG LEDS (2 OF 4):THERMTRIP

P3V3_STBY
DEBUG C1H1 1.0UF 6.3V 10% A36096-027 0402LF
DEBUG R1H6 15K 5% 1/16W A93549-024 0402LF
PD_LATCH_EN_PORST

DEBUG U9V3 74LVC1G17 D52325-001 VCC=P3V3_STBY; GND=GND;
DEBUG U1H1 74LVC32 C88296-001 VCC=P3V3_STBY; GND=GND;
FM_CPU0_LATCH_EN_PORST
FM_CPU0_THTRIP_LATCH_EN_LVC3
RST_PCH_PLTRST_LVC3_N
DEBUG U9V4

DEBUG U9V2 74LVC1G17 D52325-001 VCC=P3V3_STBY; GND=GND;
DEBUG U1H1 74LVC32 C88296-001 VCC=P3V3_STBY; GND=GND;
FM_CPU1_LATCH_EN_PORST
FM_CPU1_THTRIP_LATCH_EN_LVC3
RST_PCH_PLTRST_LVC3_N

DEBUG U9V1 74LVC1G17 D52325-001 VCC=P3V3_STBY; GND=GND;
DEBUG U1H1 74LVC32 C88296-001 VCC=P3V3_STBY; GND=GND;
FM_CPU2_LATCH_EN_PORST
FM_CPU2_THTRIP_LATCH_EN_LVC3
RST_PCH_PLTRST_LVC3_N

DEBUG U9V8 74LVC1G17 D52325-001 VCC=P3V3_STBY; GND=GND;
DEBUG U1H1 74LVC32 C88296-001 VCC=P3V3_STBY; GND=GND;
FM_CPU3_LATCH_EN_PORST
FM_CPU3_THTRIP_LATCH_EN_LVC3
RST_PCH_PLTRST_LVC3_N

P3V3_STBY
DEBUG C1H2 1.0UF 6.3V 10% A36096-027 0402LF
DEBUG R1H7 51K 1% 1/16W D33128-001 0402LF
PD_THTRIP_PORST

DEBUG U9V5 74LVC1G17 D52325-001 VCC=P3V3_STBY; GND=GND;
DEBUG U1H5 74LVC32 C88296-001 VCC=P3V3_STBY; GND=GND;
FM_CPU0_THTRIP_PORST
FM_CPU0_THTRIP_LVC3_N
FM_CPU0_THERMTRIP_LVC3_N

DEBUG U9V6 74LVC1G17 D52325-001 VCC=P3V3_STBY; GND=GND;
DEBUG U1H5 74LVC32 C88296-001 VCC=P3V3_STBY; GND=GND;
FM_CPU1_THTRIP_PORST
FM_CPU1_THTRIP_LVC3_N
FM_CPU1_THERMTRIP_LVC3_N

DEBUG U9V7 74LVC1G17 D52325-001 VCC=P3V3_STBY; GND=GND;
DEBUG U1H5 74LVC32 C88296-001 VCC=P3V3_STBY; GND=GND;
FM_CPU2_THTRIP_PORST
FM_CPU2_THTRIP_LVC3_N
FM_CPU2_THERMTRIP_LVC3_N

74LVC1G17 D52325-001 VCC=P3V3_STBY; GND=GND;
DEBUG U1H5 74LVC32 C88296-001 VCC=P3V3_STBY; GND=GND;
FM_CPU3_THTRIP_PORST
FM_CPU3_THTRIP_LVC3_N
FM_CPU3_THERMTRIP_LVC3_N

REVIEW IF PULLDOWN REQUIRED FOR DFT

U1H6 SMLF NC7SZ373 C85570-001 VCC=P3V3_STBY; GND=GND;
FM_CPU0_THTRIP_LVC3_N
FM_CPU0_THTRIP_LATCH_EN_LVC3
LED_CPU0_THRMTRP_Q_N
DS1H9 AMBER C97278-002
LED_CPU0_THRMTRP_R_N
A93549-011 R9V4 220 5% 1/16W 0402LF

U1H2 SMLF NC7SZ373 C85570-001 VCC=P3V3_STBY; GND=GND;
FM_CPU1_THTRIP_LVC3_N
FM_CPU1_THTRIP_LATCH_EN_LVC3
LED_CPU1_THRMTRP_Q_N
DS1H10 AMBER C97278-002
LED_CPU1_THRMTRP_R_N
A93549-011 R9V3 220 5% 1/16W 0402LF

U1H4 SMLF NC7SZ373 C85570-001 VCC=P3V3_STBY; GND=GND;
FM_CPU2_THTRIP_LVC3_N
FM_CPU2_THTRIP_LATCH_EN_LVC3
LED_CPU2_THRMTRP_Q_N
DS1H11 AMBER C97278-002
LED_CPU2_THRMTRP_R_N
A93549-011 R9V2 220 5% 1/16W 0402LF

U1H3 SMLF NC7SZ373 C85570-001 VCC=P3V3_STBY; GND=GND;
FM_CPU3_THTRIP_LVC3_N
FM_CPU3_THTRIP_LATCH_EN_LVC3
LED_CPU3_THRMTRP_Q_N
DS1H12 AMBER C97278-002
LED_CPU3_THRMTRP_R_N
A93549-011 R9V1 220 5% 1/16W 0402LF

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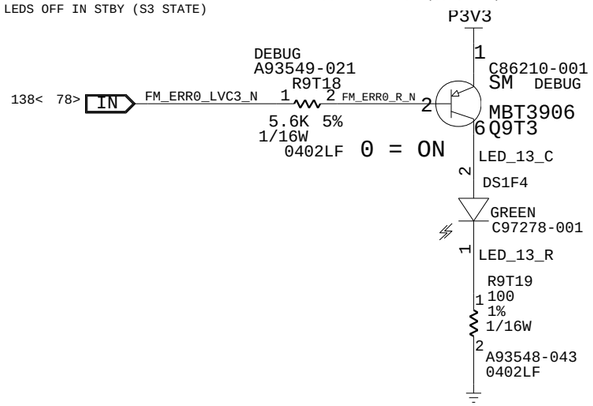
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 128 OF 303	

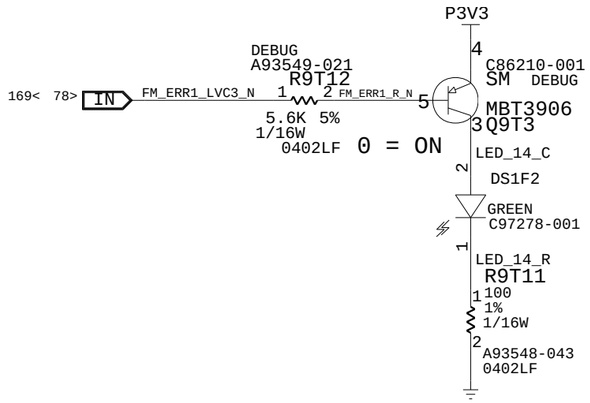
INTEL CONFIDENTIAL

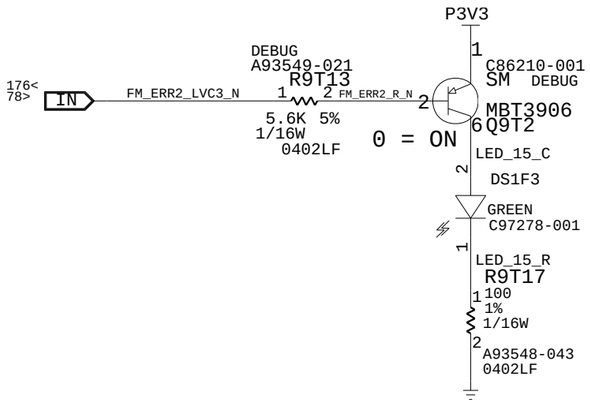
ROOM = DEBUG

ERROR[2:0] LEDS

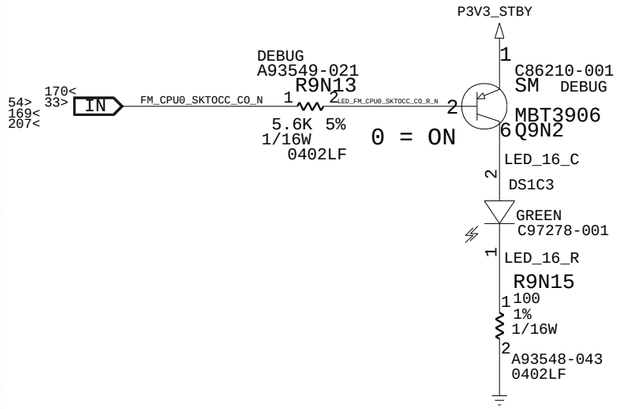
LEDS REFLECTING ERROR STATE WHEN PLATFORM COMPLETELY ON (S0 STATE)
LEDS OFF IN STBY (S3 STATE)

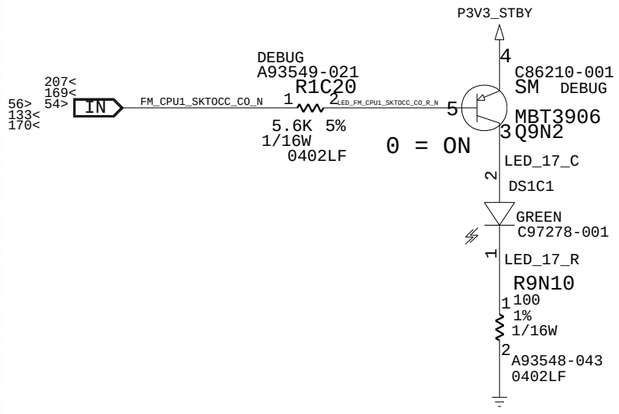


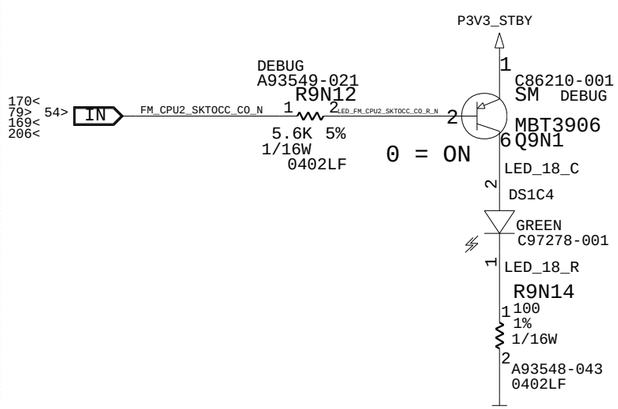


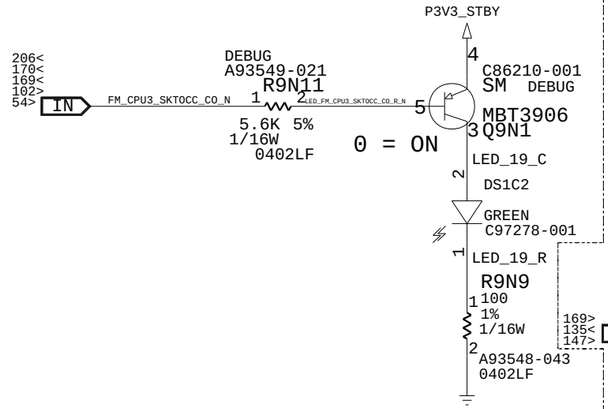


CPU_SKTOCC LEDS

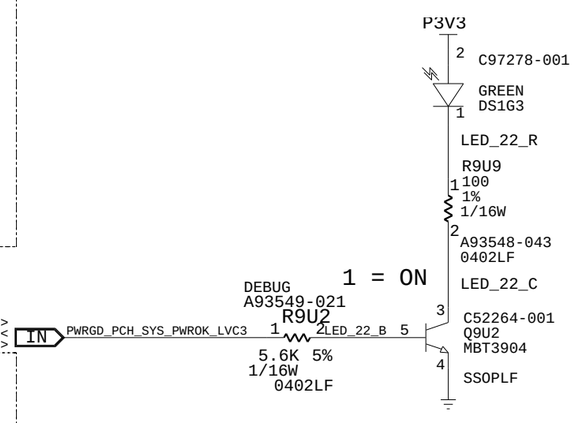




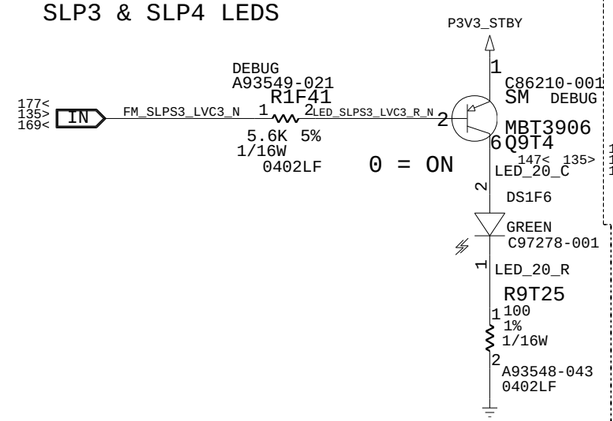


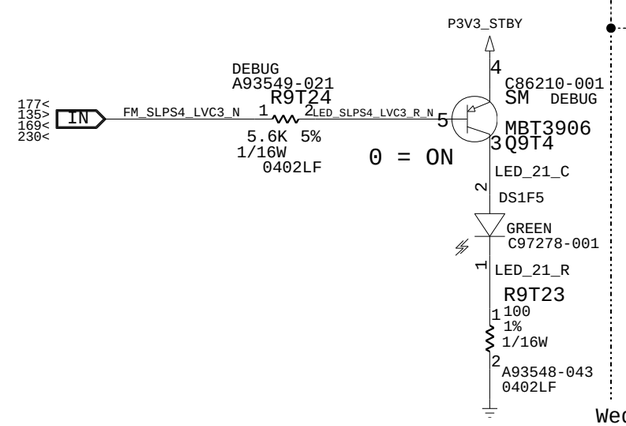


SYSTEM POWER OK LED

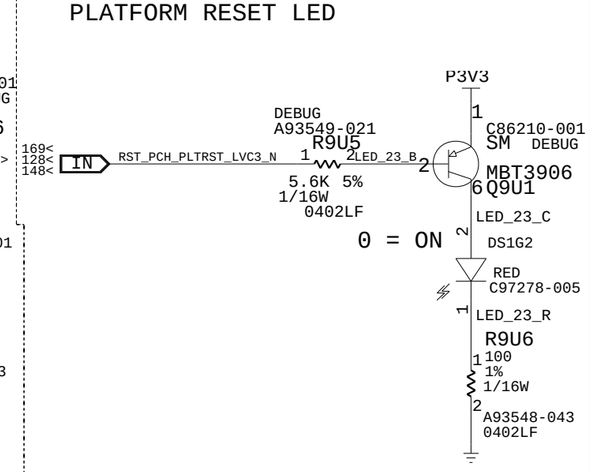


SLP3 & SLP4 LEDS





PLATFORM RESET LED



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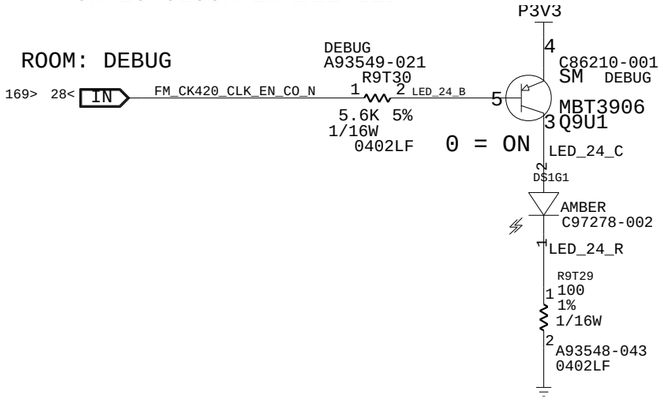
PROC DEBUG LEDS (3 OF 4)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 129 OF 303	

INTEL CONFIDENTIAL

CK420 CLOCK ENABLE LED

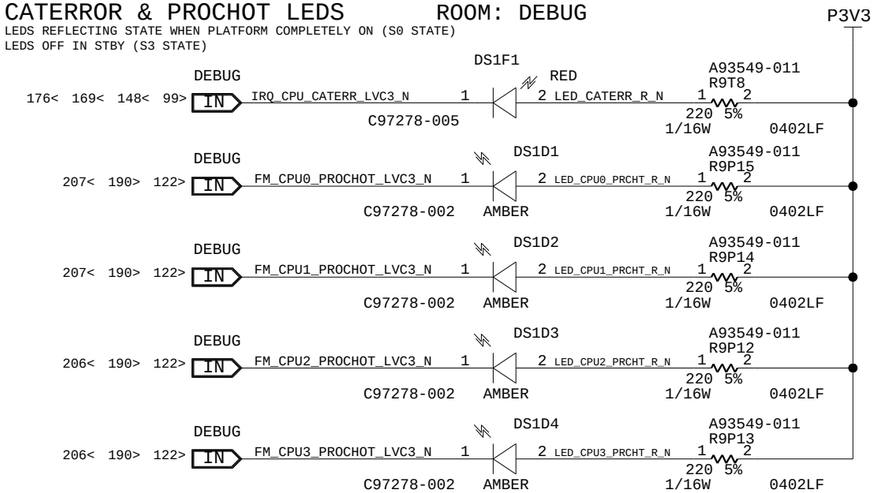
ROOM: DEBUG



CATERROR & PROCHOT LEDS

ROOM: DEBUG

LEDS REFLECTING STATE WHEN PLATFORM COMPLETELY ON (S0 STATE)
LEDS OFF IN STBY (S3 STATE)



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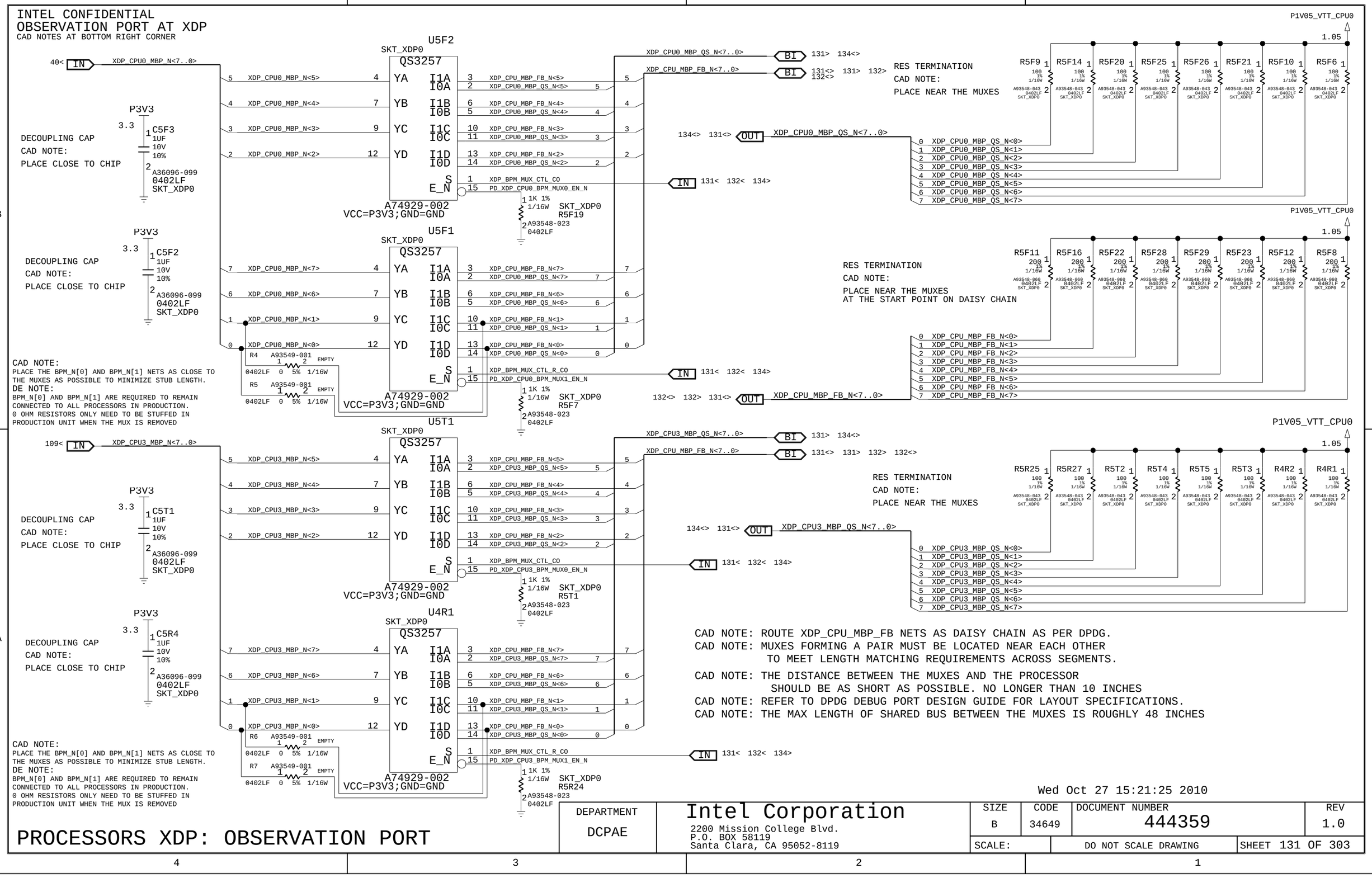
PROC DEBUG LEDS (4 OF 4)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 130 OF 303

INTEL CONFIDENTIAL
OBSERVATION PORT AT XDP

CAD NOTES AT BOTTOM RIGHT CORNER



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PROCESSORS XDP: OBSERVATION PORT

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 131 OF 303	

INTEL CONFIDENTIAL
OBSERVATION PORT AT XDP

63< IN XDP_CPU1_MBP_N<7..0>

P3V3 3.3 — C8F6 1UF 10V 10% — A36096-099 0402LF SKT_XDP1

DECOUPLING CAP
CAD NOTE:
PLACE CLOSE TO CHIP

P3V3 3.3 — C8F3 1UF 10V 10% — A36096-099 0402LF SKT_XDP1

DECOUPLING CAP
CAD NOTE:
PLACE CLOSE TO CHIP

U8F3 SKT_XDP1 QS3257 — A74929-002 VCC=P3V3;GND=GND

5	XDP_CPU1_MBP_N<5>	4	YA	I1A I0A	3 XDP_CPU_MBP_FB_N<5> / 2 XDP_CPU1_MBP_QS_N<5> 5
4	XDP_CPU1_MBP_N<4>	7	YB	I1B I0B	6 XDP_CPU_MBP_FB_N<4> / 5 XDP_CPU1_MBP_QS_N<4> 4
3	XDP_CPU1_MBP_N<3>	9	YC	I1C I0C	10 XDP_CPU_MBP_FB_N<3> / 11 XDP_CPU1_MBP_QS_N<3> 3
2	XDP_CPU1_MBP_N<2>	12	YD	I1D I0D	13 XDP_CPU_MBP_FB_N<2> / 14 XDP_CPU1_MBP_QS_N<2> 2
			S	E_N	1 XDP_BPM_MUX_CTL_CO / 15 PD_XDP_CPU1_BPM_MUX0_EN_N

1K 1% 1/16W SKT_XDP1 R8F15 — A93548-023 0402LF

U8F4 SKT_XDP1 QS3257 — A74929-002 VCC=P3V3;GND=GND

7	XDP_CPU1_MBP_N<7>	4	YA	I1A I0A	3 XDP_CPU_MBP_FB_N<7> / 2 XDP_CPU1_MBP_QS_N<7> 7
6	XDP_CPU1_MBP_N<6>	7	YB	I1B I0B	6 XDP_CPU_MBP_FB_N<6> / 5 XDP_CPU1_MBP_QS_N<6> 6
1	XDP_CPU1_MBP_N<1>	9	YC	I1C I0C	10 XDP_CPU_MBP_FB_N<1> / 11 XDP_CPU1_MBP_QS_N<1> 1
0	XDP_CPU1_MBP_N<0>	12	YD	I1D I0D	13 XDP_CPU_MBP_FB_N<0> / 14 XDP_CPU1_MBP_QS_N<0> 0
			S	E_N	1 XDP_BPM_MUX_CTL_R_CO / 15 PD_XDP_CPU1_BPM_MUX1_EN_N

R8 A93549-001 EMPTY 0402LF 0 5% 1/16W
R9 A93549-001 EMPTY 0402LF 0 5% 1/16W

1K 1% 1/16W SKT_XDP1 R8F14 — A93548-023 0402LF

CAD NOTE:
PLACE THE BPM_N[0] AND BPM_N[1] NETS AS CLOSE TO THE MUXES AS POSSIBLE TO MINIMIZE STUB LENGTH.
DE NOTE:

XDP_CPU1_MBP_QS_N<7..0> BI 132> 134<>
XDP_CPU_MBP_FB_N<7..0> BI 131<> 131> 132<> 132>

134<> 132<> OUT XDP_CPU1_MBP_QS_N<7..0>
IN 131< 132< 134>

RES TERMINATION
CAD NOTE:
PLACE NEAR THE MUXES

P1V05_VTT_CPU0 1.05

R9F12 R9F14 R8F18 R8F24 R8F20 R8F13 R8F22 R8F16 — 100 1% 1/16W — A93548-043 0402LF SKT_XDP1

0 XDP_CPU1_MBP_QS_N<0>
1 XDP_CPU1_MBP_QS_N<1>
2 XDP_CPU1_MBP_QS_N<2>
3 XDP_CPU1_MBP_QS_N<3>
4 XDP_CPU1_MBP_QS_N<4>
5 XDP_CPU1_MBP_QS_N<5>
6 XDP_CPU1_MBP_QS_N<6>
7 XDP_CPU1_MBP_QS_N<7>

CAD NOTE: ROUTE XDP_CPU_MBP_FB NETS AS DAISY CHAIN AS PER DPDG.
CAD NOTE: MUXES FORMING A PAIR MUST BE LOCATED NEAR EACH OTHER TO MEET LENGTH MATCHING REQUIREMENTS ACROSS SEGMENTS.
CAD NOTE: THE DISTANCE BETWEEN THE MUXES AND THE PROCESSOR SHOULD BE AS SHORT AS POSSIBLE. NO LONGER THAN 10 INCHES
CAD NOTE: REFER TO DPDG DEBUG PORT DESIGN GUIDE FOR LAYOUT SPECIFICATIONS.
CAD NOTE: THE MAX LENGTH OF SHARED BUS BETWEEN THE MUXES IS ROUGHLY 48 INCHES

U7E1 SKT_XDP1 QS3257 — A74929-002 VCC=P3V3;GND=GND

5	XDP_CPU2_MBP_N<5>	4	YA	I1A I0A	3 XDP_CPU_MBP_FB_N<5> / 2 XDP_CPU2_MBP_QS_N<5> 5
4	XDP_CPU2_MBP_N<4>	7	YB	I1B I0B	6 XDP_CPU_MBP_FB_N<4> / 5 XDP_CPU2_MBP_QS_N<4> 4
3	XDP_CPU2_MBP_N<3>	9	YC	I1C I0C	10 XDP_CPU_MBP_FB_N<3> / 11 XDP_CPU2_MBP_QS_N<3> 3
2	XDP_CPU2_MBP_N<2>	12	YD	I1D I0D	13 XDP_CPU_MBP_FB_N<2> / 14 XDP_CPU2_MBP_QS_N<2> 2
			S	E_N	1 XDP_BPM_MUX_CTL_CO / 15 PD_XDP_CPU2_BPM_MUX0_EN_N

1K 1% 1/16W SKT_XDP1 R7E2 — A93548-023 0402LF

U8E2 SKT_XDP1 QS3257 — A74929-002 VCC=P3V3;GND=GND

7	XDP_CPU2_MBP_N<7>	4	YA	I1A I0A	3 XDP_CPU_MBP_FB_N<7> / 2 XDP_CPU2_MBP_QS_N<7> 7
6	XDP_CPU2_MBP_N<6>	7	YB	I1B I0B	6 XDP_CPU_MBP_FB_N<6> / 5 XDP_CPU2_MBP_QS_N<6> 6
1	XDP_CPU2_MBP_N<1>	9	YC	I1C I0C	10 XDP_CPU_MBP_FB_N<1> / 11 XDP_CPU2_MBP_QS_N<1> 1
0	XDP_CPU2_MBP_N<0>	12	YD	I1D I0D	13 XDP_CPU_MBP_FB_N<0> / 14 XDP_CPU2_MBP_QS_N<0> 0
			S	E_N	1 XDP_BPM_MUX_CTL_R_CO / 15 PD_XDP_CPU2_BPM_MUX1_EN_N

R10 A93549-001 EMPTY 0402LF 0 5% 1/16W
R11 A93549-001 EMPTY 0402LF 0 5% 1/16W

1K 1% 1/16W SKT_XDP1 R9E10 — A93548-023 0402LF

CAD NOTE:
PLACE THE BPM_N[0] AND BPM_N[1] NETS AS CLOSE TO THE MUXES AS POSSIBLE TO MINIMIZE STUB LENGTH.
DE NOTE:
BPM_N[0] AND BPM_N[1] ARE REQUIRED TO REMAIN CONNECTED TO ALL PROCESSORS IN PRODUCTION.
0 OHM RESISTORS ONLY NEED TO BE STUFFED IN PRODUCTION UNIT WHEN THE MUX IS REMOVED

86< IN XDP_CPU2_MBP_N<7..0>

XDP_CPU2_MBP_QS_N<7..0> BI 132> 134<>
XDP_CPU_MBP_FB_N<7..0> BI 131<> 131> 132> 132<>

134<> 132<> OUT XDP_CPU2_MBP_QS_N<7..0>
IN 131< 132< 134>

RES TERMINATION
CAD NOTE:
PLACE NEAR THE MUXES

P1V05_VTT_CPU0 1.05

R9E13 R9E15 R8E17 R8E18 R7E4 R7E3 R8E22 R8E21 — 100 1% 1/16W — A93548-043 0402LF SKT_XDP1

0 XDP_CPU2_MBP_QS_N<0>
1 XDP_CPU2_MBP_QS_N<1>
2 XDP_CPU2_MBP_QS_N<2>
3 XDP_CPU2_MBP_QS_N<3>
4 XDP_CPU2_MBP_QS_N<4>
5 XDP_CPU2_MBP_QS_N<5>
6 XDP_CPU2_MBP_QS_N<6>
7 XDP_CPU2_MBP_QS_N<7>

RES TERMINATION
CAD NOTE:
PLACE NEAR THE MUXES
AT THE END POINT ON DAISY CHAIN

P1V05_VTT_CPU0 1.05

R9F13 R1T13 R8F21 R8F28 R8F23 R8F17 R8F25 R8F19 — 200 1% 1/16W — A93548-060 0402LF SKT_XDP1

0 XDP_CPU_MBP_FB_N<0>
1 XDP_CPU_MBP_FB_N<1>
2 XDP_CPU_MBP_FB_N<2>
3 XDP_CPU_MBP_FB_N<3>
4 XDP_CPU_MBP_FB_N<4>
5 XDP_CPU_MBP_FB_N<5>
6 XDP_CPU_MBP_FB_N<6>
7 XDP_CPU_MBP_FB_N<7>

132<> 131> 131<> OUT XDP_CPU_MBP_FB_N<7..0>

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PROCESSORS XDP: OBSERVATION PORT

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 132 OF 303	

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P1V05_VTT_CPU0

CAD NOTE:
PLACE CLOSE TO
CPU0, WITHIN 1"

R5T9 1 2 1% 150 1/16W A93548-005 0402LF

P1V05_VTT_CPU0

ROOM=SOCKET0

R4T18 1 2 1% 150 1/16W A93548-005 0402LF

134> 79< 33< IN JTAG_CPU_G_TDI

33> IN JTAG_CPU0_G_TDO

THE SWITCH NEEDS TO BE REMOVED FOR PRODUCTION.

U2T2
C99406-001
NC7SB3157
SMLF

4	A	S	6
		B0	3
		B1	1
2	GND	VCC	5

P3V3

R9F1 1K 1% 1/16W A93548-023 0402LF

PU_JTAG_CPU1_SKTOCC_LVC3

THE PU RES NEEDS TO BE REMOVED FOR PRODUCTION.

J9F1
C95678-002
CONN3

THE HEADER NEEDS TO BE REMOVED FOR PRODUCTION.

FM_CPU1_SKTOCC_CO_N IN 54> 56> 129< 169< 170< 207<

JUMPER

SHORT 1-2 FOR NORMAL OPERATION (DEFAULT)

SHORT 2-3 TO FORCE JTAG BYPASS OF CPU1

JTAG_CPU1_SKTOCC_CO_N

P1V05_VTT_CPU0

CAD NOTE:
PLACE CLOSE TO
CPU 2, WITHIN 1"

R2R21 1 2 1% 150 1/16W A93548-005 0402LF

ROOM=SOCKET2

P1V05_VTT_CPU0

CAD NOTE:
PLACE CLOSE TO
CPU 3, WITHIN 1"

R5R19 1 2 1% 150 1/16W A93548-005 0402LF

ROOM=SOCKET3

CAD NOTE:
PLACE CLOSE
TO VCC (PIN 5)

P3V3

C2T9 1 2 0.01UF 25V 10% A36096-045 0402LF

C2T7 1 2 1.0UF 16V 10% 603269-067 0603LF

THE DECOUPLING CAPS NEED TO BE REMOVED FOR PRODUCTION.

P1V05_VTT_CPU0

R2T15 1 2 1% 150 1/16W A93548-005 0402LF

P1V05_VTT_CPU0

R2T14 1 2 1% 150 1/16W A93548-005 0402LF

CAD NOTE:
PLACE CLOSE TO
CPU 1, WITHIN 1"

ROOM=SOCKET1

JTAG_CPU1_G_TDI OUT 56<

JTAG_CPU1_G_TDO IN 56>

102< 79> OUT JTAG_CPU2_G_TDO

THE SWITCH NEEDS TO BE REMOVED FOR PRODUCTION.

U2T1
C99406-001
NC7SB3157
SMLF

6	S		
3	B0		
JTAG_CPU1_G_BYPASS 1	B1	A	4 JTAG_CPU_G_TDO OUT 102> 134<
5	VCC	GND	2

CAD NOTE:
PLACE CLOSE
TO VCC (PIN 5)

P3V3

C2T8 1 2 0.01UF 25V 10% A36096-045 0402LF

C2T6 1 2 1.0UF 16V 10% 603269-067 0603LF

THE DECOUPLING CAPS NEED TO BE REMOVED FOR PRODUCTION.

P1V05_VTT_CPU0

ROOM=SOCKET3

R5R20 1 2 1% 150 1/16W A93548-005 0402LF

CAD NOTE:
PLACE CLOSE TO
CPU 3, WITHIN 1"

P1V05_VTT_CPU0

CAD NOTE:
SEE DPDG DOC. FOR ADDITIONAL
LAYOUT REQUIREMENTS

R2T13 2 1 51.10 1% 1/16W 0402LF A93548-072

R2R17 2 1 51.10 1% 1/16W 0402LF A93548-072

JTAG_CPU_G_TMS OUT 33< 56< 79< 102< 134>

THE TMS SIGNAL SHOULD FORK AT THE DEBUG PORT. EACH OF THE TWO BRANCHES IS CONNECTED DAISY-CHAIN STYLE TO TWO CPUS AND FINALLY TERMINATES AT THE END OF THE LINE.

R2U5 2 1 51.10 1% 1/16W 0402LF A93548-072 JTAG_CPU_LVC1_TCK0 OUT 33< 56< 134>

R2R2 2 1 51.10 1% 1/16W 0402LF A93548-072 JTAG_CPU_LVC1_TCK1 OUT 79< 102< 134>

TCK0 (TCK1) IS ALSO CONNECTED DAISY-CHAIN STYLE TO TWO CPUS WITH A TERMINATION RESISTOR TO GROUND AT THE END OF THE TRACE

R2T1 2 1 51.10 1% 1/16W 0402LF A93548-072 JTAG_CPU_LVC1_TRST_N OUT 33< 56< 79< 102< 134>

ROOM=SKT_JTAG

SOME PU RESISTORS

DON'T BELONG TO THIS ROOM

SUPPORT CONFIGURATIONS

1. CPU0 ONLY
2. CPU0 AND CPU1 ONLY
3. CPU0, CPU1, CPU2 AND CPU3

PROCESSORS JTAG CHAIN

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DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 133 OF 303	

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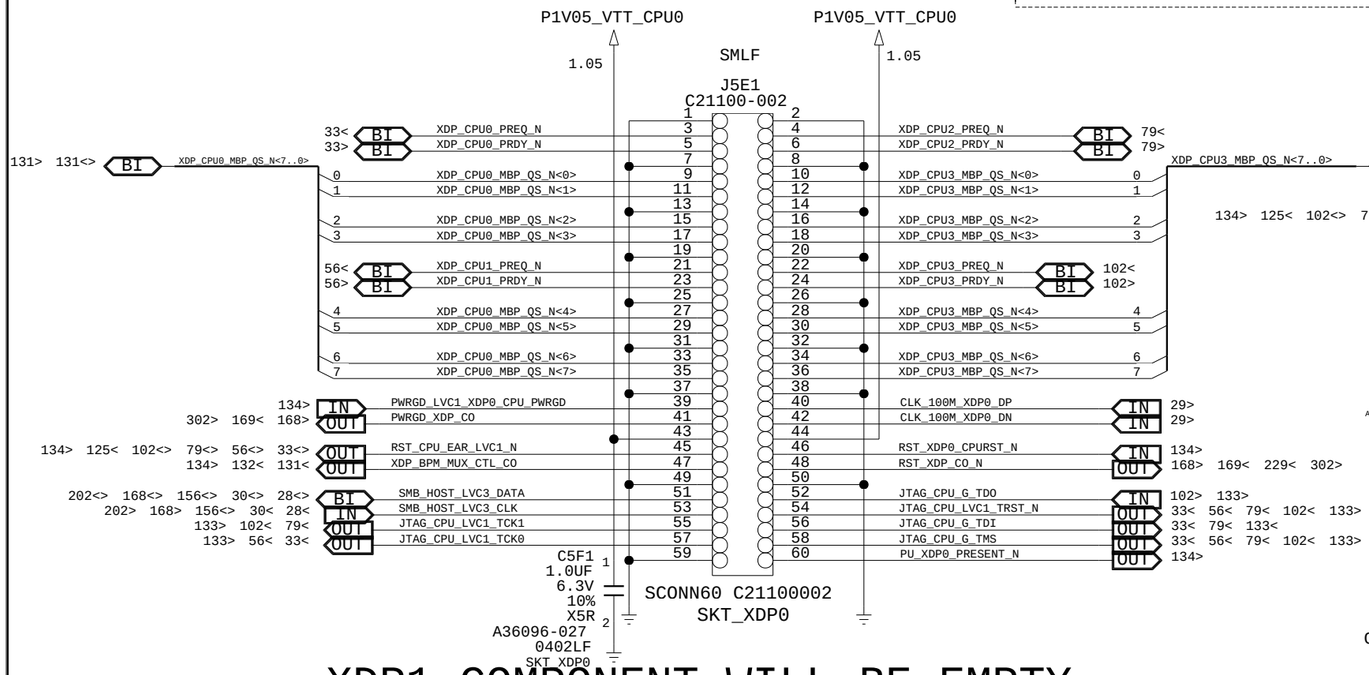
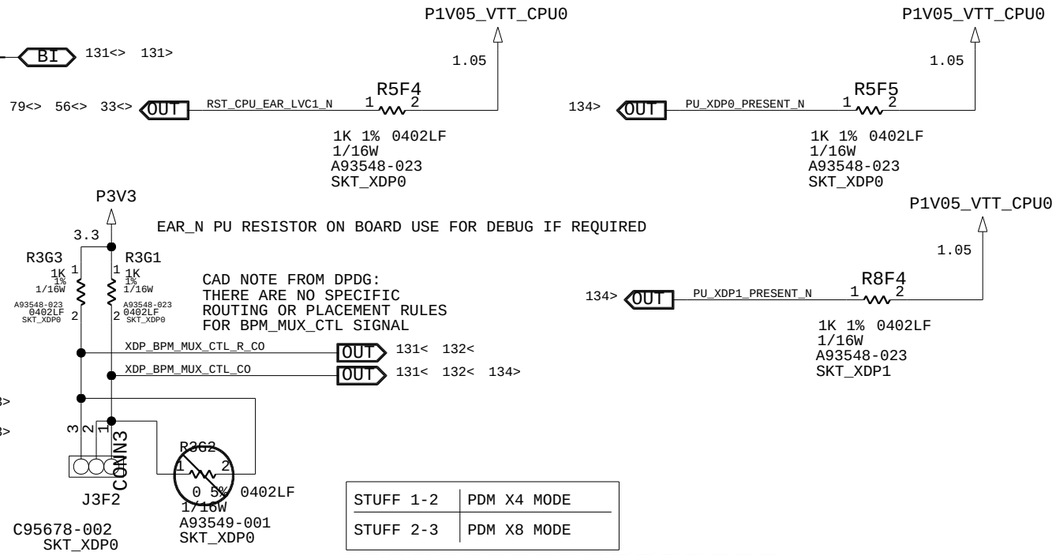
ROOM=SKT_XDP0

XDP0 & XDP1 MUST BE REMOVED FOR PRODUCTION



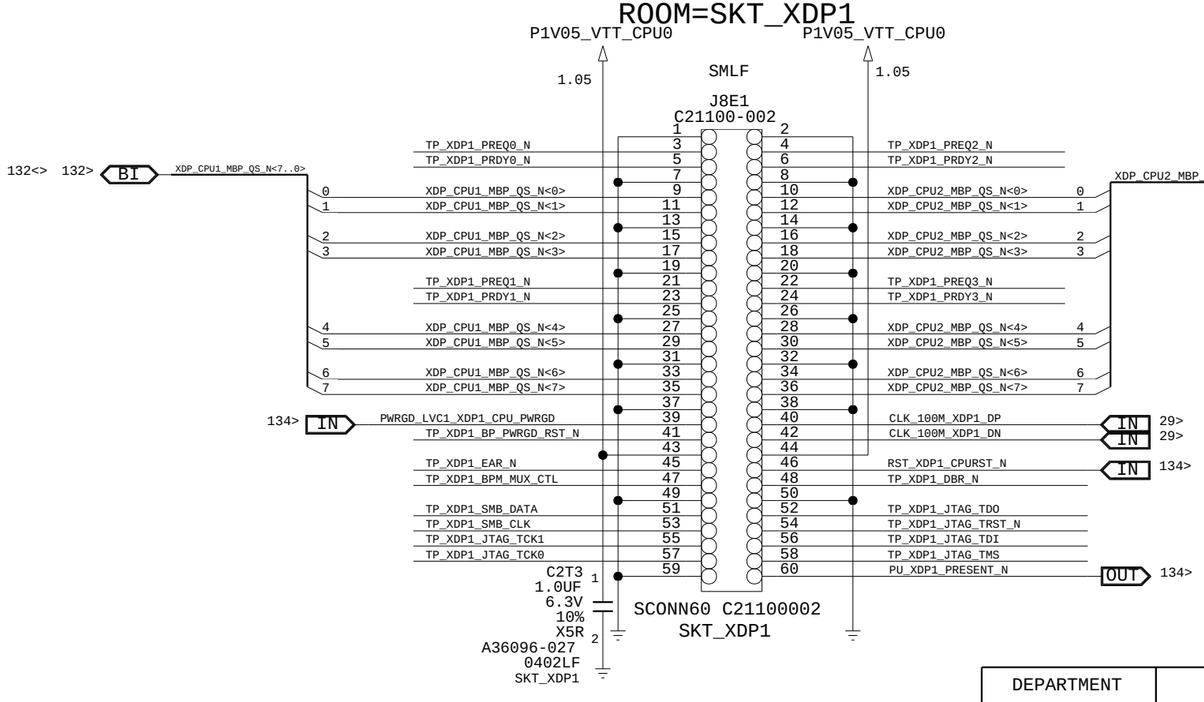


STUFF 1-2	PDM X4 MODE
STUFF 2-3	PDM X8 MODE

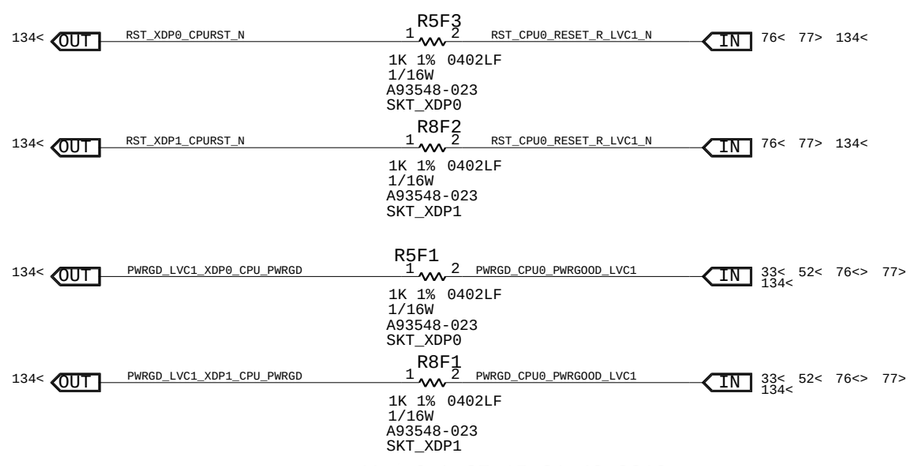
REMOVE 3-PIN JUMPER FOR PRODUCTION
AND STUFF 0-OHM RESISTOR

XDP1 COMPONENT WILL BE EMPTY

ROOM=SKT_XDP1



PWRGD_XDP_CO IS OPEN-DRAIN AND ITS PU IS AT PWR_SEQ PAGE: 301
RST_XDP_CO_N IS OPEN-DRAIN AND ITS PU IS AT RST_SEQ PAGE: 302
RST_CPU_EAR_LVC1_N IS OPEN-DRAIN WITH A 6K-OHM PU ON EACH CPU DIE, REFER TO CCAT



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PROCESSORS XDP: CONNECTORS

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 134 OF 303	

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U2F1
IC

PBG_EXT_F

		CLKIN_GND0P	Y4		
		CLKIN_GND0N	Y5		
31>	IN	CLK_100M_SSB_DMI_DP	M2	CLKIN_DMIP	
31>	IN	CLK_100M_SSB_DMI_DN	M1	CLKIN_DMIN	
29>	IN	CLK_96M_DOT_SSB_DP	R31	CLKIN_DOT96P	
29>	IN	CLK_96M_DOT_SSB_DN	R32	CLKIN_DOT96N	
		NC_CLKIN_PEG0P	AM2	CLKIN_SPCIE0P	
		NC_CLKIN_PEG0N	AN1	CLKIN_SPCIE0N	
28>	IN	CLK_100M_SAS_DP	AV27	CLKIN_SAS0P	
28>	IN	CLK_100M_SAS_DN	AU28	CLKIN_SAS0N	
28>	IN	CLK_100M_SATA_SSB_DP	A17	CLKIN_SATAP	
28>	IN	CLK_100M_SATA_SSB_DN	B17	CLKIN_SATAN	
		NC_TEST_CLKIN_SAS1P	AW33	CLKIN_SAS1P	
		NC_TEST_CLKIN_SAS1N	AV33	CLKIN_SAS1N	
			W8	VSS<248>	
			W9	VSS<247>	
			M3	VSS<250>	
			N2	VSS<249>	
			A10	VSS<252>	
			B9	VSS<251>	
29>	IN	CLK_33M_PCI_PBG	AK22	CLKIN_PCI	
28>	B1	CLK_14M_SSB	AV12	REFCLK14IN	
		XTAL_OUT_32K_PBG	P36	RTCX2	
		XTAL_IN_32K_PBG	R36	RTCX1	
		NC_SSB_TP1	W4	TP1	
		NC_SSB_TP4	P11	TP4	
		NC_SSB_TP20	A15	TP20	
		NC_SSB_TP2	W5	TP2	
		NC_SSB_TP5	P9	TP5	
		NC_SSB_TP21	J19	TP21	
147>	IN	PU_A20GATE	B26	A20GATE	
148<	OUT	PWRGD_CPUPWRGD_1V1	J9	PROCPWRGD	
147>	OUT	IRQ_INIT3_3V_N	C31	INIT3_3V_N	
196<>	B1	PECI_SSB_LVC1	E4	PECI	
56< 33<	OUT	IRQ_PM_SYNC_LVC1	J6	PM_SYNC	
102< 79<	OUT	IRQ_PM_SYNC2_LVC1	H4	PM_SYNC2	
147>	IN	PU_SIO_KBRST_N	B28	RCIN_N	
191< 147>	OUT	SPEAKER_SSB	A28	SPKR	
		P1V1_TEST_RNG	AP13	NC_1	
148>	IN	FM_THERMTRIP_DLY_LVC1_N	J7	THRMTRIP_N	

			V29	HDA_BCLK	NC_AUD_HDA_BCLK
			AW22	HDA_RST_N	NC_AUD_HDA_RST_N
			AH38	HDA_SDIN<3>	NC_AUD_HDA_SDI3
			AH39	HDA_SDIN<2>	NC_AUD_HDA_SDI2
			AG38	HDA_SDIN<1>	NC_AUD_HDA_SDI1
			AH37	HDA_SDIN<0>	NC_AUD_HDA_SDI0
			V30	HDA_SDO	FM_MFG_MODE_FLSH_SEC_OVRD
			AV17	HDA_SYNC	PU_VRM_VOLTAGE_SELECT
			E37	SLP_A_N	FM_SLPA_LVC3_N
			H28	SLP_LAN_N_GPIO29	FM_THROTTLE_LVC3_N
			F30	SLP_S3_N	FM_SLPS3_LVC3_N
			E31	SLP_S4_N	FM_SLPS4_LVC3_N
			B35	SLP_S5_N_GPIO63	TP_SLPS5_N
			M39	SLP_SUS_N	TP_SLPSUS_N
			F33	APWROK	PWRGD_PCH_APWROK_LVC3
			E24	BMBUSY_N_GPIO0	CLK2_R_IRQ_SSB_SCI_WHEA_N
			R37	DPWROK	RST_RSMRST_SSB_N
			J28	DRAMPWROK	PWRGD_PCH_DRAMPWRGD_CO
			R39	DSWODVREN	PU_1V1_DSW_ODVR_EN
			E34	PLTRST_N	RST_PCH_PLTRST_LVC3_N
			K31	PWRBTN_N	FM_IBMC_PWRBTN_OUT_N
			G39	RI_N	PU_RI_N
			E36	SUS_STAT_N_GPIO61	LPC_TPM_PD_N
			H33	SUSACK_N	PU_SUSACK_N
			C35	SUSCLK_GPIO62	TP__SUSCLK
			N38	SUSWARN_N_SUSPWRDNACK_GPIO30	PU_SUS_WARN_N
			C33	SYS_PWROK	PWRGD_PCH_SYS_PWROK_LVC3
			C30	SYS_RESET_N	RST_SSB_RSTBTN_N
			J36	WAKE_N	IRQ_SSB_WAKE_LVC3_N
			P34	INTRUDER_N	FM_PASSWORD_CLEAR_N
			M34	INTVRMEN	PU_1V1_SUS_ODVR_EN
			R34	PCH_PWROK	PWRGD_PCH_PWROK_LVC3
			M30	RSMRST_N	RST_RSMRST_SSB_N
			R38	RTCRST_N	RST_RTCRST_N
			P38	SRTCRST_N	RST_SRTCRST_N
			H37	ADR_COMPLETE	NC_ADR_COMPLETE

E93039-001

1/10

P3V3_STBY

R2G17
10.0K
0402LF 1% 1/16W
A93548-034

169< 135> IN FM_THROTTLE_LVC3_N

147> 149> IN
147> IN

169<
135< 169<
129< 169< 177<
129< 169< 177< 230<

147> 168< 169> IN
168< OUT

135< 148> IN
147< 169> OUT
147> IN
128< 129< 147< 148< OUT
177> 169< IN
147> IN
156< OUT

155> IN
129< 147> 169> IN
148> IN

171> 218> IN

150> IN
147> IN
147> 169> 177< 204< 219> 219< IN
135< 148> IN
150> IN
150> IN

R2F16
10.0K
1%
1/16W
0402LF
A93548-034

R1F28
1K
1%
1/16W
A93548-023
0402LF

32.768KHZ
C13544-012
XTAL_OUT_32K_PBG
XTAL_IN_32K_PBG

R9T15 10M
5% 1/10W
A93551-141 0603LF

C9T10 15PF 50V 5% C9T9
603275-167
0603LF

P1V1_STBY_PBG

R8R22
0
5%
1/10W
A93552-004
0603LF

R8R21
0
5%
1/10W
EMPTY
A93552-004
0603LF

PLTRST DELAY AND SMART-CLST CIRCUIT
IMPLEMENTED IN CPLD.

CAD NOTE: PLACE 32KHZ XTAL CLOSE TO PBG
KEEP ROUTING < 1 INCH AND ADD GROUND GUARD
PLANE IF POSSIBLE

ROOM INTEL_SI
ROOM SB

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PATSBURG (1 OF 8)

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		SCALE:	DO NOT SCALE DRAWING	SHEET 135 OF 303	

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NOTE: DMI PORT LANE REVERSED
FROM UPSTREAM DEVICE (CPU)

U2F1
IC

PBG_EXT_F

154> 154< IN	DMI_CPU0_SSB_TX_C_DP<3..0>		DMI_RXP<3>	N4	
	3 DMI_CPU0_SSB_TX_C_DP<3>		DMI_RXN<3>	N5	
	3 DMI_CPU0_SSB_TX_C_DN<3>		DMI_RXP<2>	P5	
	2 DMI_CPU0_SSB_TX_C_DP<2>		DMI_RXN<2>	P4	
	2 DMI_CPU0_SSB_TX_C_DN<2>		DMI_RXP<1>	T5	
	1 DMI_CPU0_SSB_TX_C_DP<1>		DMI_RXN<1>	T6	
	1 DMI_CPU0_SSB_TX_C_DN<1>		DMI_RXP<0>	U6	
	0 DMI_CPU0_SSB_TX_C_DP<0>		DMI_RXN<0>	U5	
154> 154< IN	DMI_CPU0_SSB_TX_C_DN<3..0>				
	0 DMI_CPU0_SSB_TX_C_DN<0>				
136< OUT	A_DMI_ZCOMP		DMI_ZCOMP	U13	
			DMI_IRCOMP	U12	
	NC_SSB_TP3		TP3	U8	
136< OUT	A_RBIAS_CPY		DMIRBIAS	U9	
177> 147> IN	FM_IBMC_SSB_SCI_LPC_N		GPIO13	AV24	
155> IN	PU_SSB_GPIO33		GPIO33	AT37	
168< OUT	SATA5GP_GPIO49_MGPIO10_R		SATA5GP_GPIO49	H21	
168< IN	SATA4GP_GPIO16_MGPIO9_R		SATA4GP_GPIO16	H22	
168< IN	SATA3GP_GPIO37_R		SATA3GP_GPIO37	C28	
168< IN	SATA2GP_GPIO36_R		SATA2GP_GPIO36	C25	
168< OUT	SATA1GP_GPIO19_R		SATA1GP_GPIO19	A25	
168< IN	SATA0GP_GPIO21_R		SATA0GP_GPIO21	J24	
168< OUT	FM_NMI_EVENT_R_N		GPIO35_NMI_N	B31	
147> OUT	FM_MULTIPLE_PCI_MASTER_N		GPIO32	B24	
168< OUT	PU_USB_OC7_R_N		OC7_N_GPIO14	K38	
168< OUT	PU_USB_OC6_R_N		OC6_N_GPIO10	K30	
168< OUT	FM_USB_OC5_R_N		OC5_N_GPIO9	L39	
168< OUT	FM_USB_OC4_R_N		OC4_N_GPIO43	J30	
168< IN	FM_USB_OC3_R_N		OC3_N_GPIO42	K36	
168< IN	FM_USB_OC2_R_N		OC2_N_GPIO41	M38	
168< IN	FM_USB_OC1_R_N		OC1_N_GPIO40	M37	
168< IN	FM_USB_OC0_R_N		OC0_N_GPIO59	K34	
	NC_SSB_TP12		TP12	F28	
	NC_SSB_TP11		TP11	AL28	
	NC_SSB_TP6		TP6	M32	

2/10

E93039-001

			DMI_TXP<3>	P2	DMI_CPU0_SSB_RX_DP<3>
			DMI_TXN<3>	R1	DMI_CPU0_SSB_RX_DN<3>
			DMI_TXP<2>	R3	DMI_CPU0_SSB_RX_DP<2>
			DMI_TXN<2>	R2	DMI_CPU0_SSB_RX_DN<2>
			DMI_TXP<1>	U2	DMI_CPU0_SSB_RX_DP<1>
			DMI_TXN<1>	U1	DMI_CPU0_SSB_RX_DN<1>
			DMI_TXP<0>	U3	DMI_CPU0_SSB_RX_DP<0>
			DMI_TXN<0>	V2	DMI_CPU0_SSB_RX_DN<0>
			GPIO73	B33	PU_SSB_GP73
			GPIO72	E38	PU_SSB_GP72
			GPIO67	AK15	NC_SSB_GP67
			GPIO66	AL15	PU_SSB_GP66
			GPIO65	AK16	NC_SSB_GP65
			GPIO64	AL16	NC_SSB_GP64
			GPIO57	J27	FM_ME_RCVR_N
			GPIO56	H27	PU_SSB_GP56
			GPIO47	B32	PU_LAN3_DISABLE_N
			GPIO46	D37	PU_LAN2_DISABLE_N
			GPIO45	E25	FM_SSB_LAN1_DISABLE_N
			GPIO44	J25	FM_SSB_LAN0_DISABLE_N
			GPIO31_MGPIO2	K33	IRQ_SML1_PMBUS_ALERT_N
			GPIO28	A33	SSB_GP28_R
			GPIO27	M35	FP_PWR_LED_N
			GPIO34	F25	FM_VIDEO_DISABLE_N
			GPIO26	F31	NC_SSB_GP26
			GPIO25	J38	NC_SSB_GP25
			GPIO24	F34	PU_FM_PBG_DYN_SKU_KEY
			GPIO20_SMI_N	F24	FM_SMI_ACTIVE_N
			GPIO18	B29	NC_SSB_GP18
			GPIO15	E30	GPIO15_R
			LANPHYPC_GPIO12	F39	NC_FM_LOM_DEV_OFF_N
			GPIO8	F38	IRQ_CPU_CATERR_DLY_LVC3_R_N

DMI_CPU0_SSB_RX_DN<3..0> OUT 154<
DMI_CPU0_SSB_RX_DP<3..0> OUT 154<

P3V3_STBY
R2G6 10.0K 1% 1/16W A93548-034 0402LF

P3V3_STBY
R1F34 10.0K 1% 1/16W A93548-034 0402LF

P3V3
R2E42 10.0K 1% 1/16W A93548-034 0402LF

P3V3_STBY
R8U6 10.0K 1% 1/16W A93548-034 0402LF

FM_ME_RCVR_N IN 150>
PU_LAN3_DISABLE_N IN 155>
PU_LAN2_DISABLE_N IN 155>
FM_SSB_LAN1_DISABLE_N OUT 224<
FM_SSB_LAN0_DISABLE_N OUT 219> 219<
IRQ_SML1_PMBUS_ALERT_N IN 169< 176< 188< 231>
SSB_GP28_R OUT 168<
FP_PWR_LED_N OUT 230<
FM_VIDEO_DISABLE_N OUT 176<
PU_FM_PBG_DYN_SKU_KEY IN 147<
FM_SMI_ACTIVE_N OUT 176< 190<
GPIO15_R BI 168<

IRQ_CPU_CATERR_DLY_LVC3_R_N — R1F37 5% 1/16W A93549-001 0402LF — IRQ_CPU_CATERR_DLY_LVC3_N IN 169>

R1F39 5% 1/16W A93549-001 0402LF
IRQ_CATERR_DLY_BUF_N IN 148> 148<

DESIGN NOTE:
THE IRQ_CPU_CATERR_DLY_LVC3_NSIGNAL MUST BE CONDITIONED THROUGH
A 400USEC DELAY CIRCUIT BEFORE IT IS CONNECTED TO
THE PATSBURG SSB GP8 I/O

CAD NOTE: PLACE CLOSE TO PBG
KEEP ROUTING <0.2 OHMS

A_RBIAS_CPY IN 136>
R2F9 1750 1% 1/16W A93548-101 0402LF

CAD NOTE: DMI Z COMP NET SHOULD BE <0.2 OHMS.
COMPI & RCOMPO SHOULD BE SHORTED AT BREAK OUT

P1V1_MAIN_PBG
A93548-045 R2F10 49.9 1% 1/16W 0402LF
A_DMI_ZCOMP IN 136>

ROOM INTEL_SI
ROOM SB

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PATSBURG (2 OF 8)

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		SCALE:	DO NOT SCALE DRAWING	SHEET 136 OF 303	

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U2F1
IC

PBG_EXT_F

168> 168<	IN	JTAG_SSB_TDI		JTAG_TDI	JTAG_TDO	A34	JTAG_SSB_TDO OUT 168<
168> 168<	IN	JTAG_SSB_TCK	E28	JTAG_TCK	RESERVED<20>	F6	NC_SSB_RSVD<20>
168> 168<	IN	JTAG_SSB_TMS	A37	JTAG_TMS	RESERVED<6>	L13	NC_SSB_RSVD<6>
			C39		RESERVED<3>	AB6	NC_SSB_RSVD<3>
175<> 156<>	BI	LPC_LAD<3..0>			RESERVED<39>	Y3	NC_SSB_RSVD<39>
		3 LPC_LAD<3>	AU17	LAD<3>	RESERVED<23>	F12	NC_SSB_RSVD<23>
		2 LPC_LAD<2>	AL36	LAD<2>	RESERVED<9>	K6	NC_SSB_RSVD<9>
		1 LPC_LAD<1>	AV23	LAD<1>			
		0 LPC_LAD<0>	AV15	LAD<0>	RESERVED<1>	AA2	NC_SSB_RSVD<1>
156>	IN	LPC_LDRQ_N	AR37	LDRQ1_N_GPIO23	RESERVED<11>	K12	NC_SSB_RSVD<11>
175>	IN	FM_IBMC_SSB_LDRQ_N	AP19	LDRQ0_N			
175< 156<	OUT	LPC_FRAME_N	AF36	LFRAME_N	RESERVED<17>	H10	NC_SSB_RSVD<17>
		NC_NVRM_ADR<7>	L6	NVRM_ADR<7>	RESERVED<35>	W2	NC_SSB_RSVD<35>
		NC_NVRM_ADR<6>	E3	NVRM_ADR<6>			
		NC_NVRM_ADR<5>	N12	NVRM_ADR<5>	RESERVED<5>	AC6	NC_SSB_RSVD<5>
		NC_NVRM_ADR<4>	L8	NVRM_ADR<4>	DF_TVS	C7	PU_NV_CLE OUT 147<
		NC_NVRM_ADR<3>	F2	NVRM_ADR<3>	RESERVED<4>	AC5	NC_SSB_RSVD<4>
		NC_NVRM_ADR<2>	E2	NVRM_ADR<2>	RESERVED<38>	Y1	NC_SSB_RSVD<38>
		NC_NVRM_ADR<1>	N9	NVRM_ADR<1>			
		NC_NVRM_ADR<0>	K2	NVRM_ADR<0>	RESERVED<15>	J10	NC_SSB_RSVD<15>
					RESERVED<25>	E9	NC_SSB_RSVD<25>
		NC_NVRM_ALE	D3	NVRM_ALE	RESERVED<24>	F10	NC_SSB_RSVD<24>
		NC_NVRM_CS_N	K1	NVRM_CS_N	RESERVED<16>	H9	NC_SSB_RSVD<16>
		NC_NVRM_OE_N	C3	NVRM_OE_N	RESERVED<12>	J4	NC_SSB_RSVD<12>
		NC_NVRM_WE_N	K3	NVRM_WE_N	RESERVED<13>	J13	NC_SSB_RSVD<13>
					RESERVED<21>	F4	NC_SSB_RSVD<21>
		NC_NVRM_D<7>	G1	NVRM_D<7>	RESERVED<26>	E7	NC_SSB_RSVD<26>
		NC_NVRM_D<6>	N11	NVRM_D<6>	RESERVED<8>	K7	NC_SSB_RSVD<8>
		NC_NVRM_D<5>	L9	NVRM_D<5>	RESERVED<14>	J12	NC_SSB_RSVD<14>
		NC_NVRM_D<4>	H2	NVRM_D<4>	RESERVED<18>	F9	NC_SSB_RSVD<18>
		NC_NVRM_D<3>	G3	NVRM_D<3>	RESERVED<10>	K13	NC_SSB_RSVD<10>
		NC_NVRM_D<2>	N8	NVRM_D<2>	RESERVED<7>	L12	NC_SSB_RSVD<7>
		NC_NVRM_D<1>	L5	NVRM_D<1>	RESERVED<22>	F13	NC_SSB_RSVD<22>
		NC_NVRM_D<0>	J2	NVRM_D<0>	RESERVED<2>	AB5	NC_SSB_RSVD<2>
					RESERVED<19>	F7	NC_SSB_RSVD<19>
152<	OUT	SPI_SSB_CLK	B23	SPI_CLK			
		TP_SPI_SSB_CS1_N	J21	SPI_CS_N<1>	PWM<3>	AG36	NC_PWM3
152<	OUT	SPI_SSB_CS0_N	K19	SPI_CS_N<0>	PWM<2>	AR13	NC_PWM2
152>	IN	SPI_SSB_MISO	J22	SPI_MISO	PWM<1>	AV22	NC_PWM1
152<	OUT	SPI_SSB_MOSI	K24	SPI_MOSI	PWM<0>	AW17	NC_PWM0
					SST	J34	NC_SSCTL
137>	IN	PD_SSB_TS_VSS1	E13	TS_VSS1			
137<	OUT	PD_SSB_TS_VSS2	H16	TS_VSS2	TACH7_GPIO71	AM36	PU_TACH7
137>	IN	PD_SSB_TS_VSS3	E12	TS_VSS3	TACH6_GPIO70	AF34	PU_TACH6
137<	OUT	PD_SSB_TS_VSS4	H15	TS_VSS4	TACH5_GPIO69	Y32	PU_TACH5
					TACH4_GPIO68	AG34	PU_TACH4
					TACH3_GPIO7	AJ35	PU_TACH3
					TACH2_GPIO6	Y31	PU_TACH2
					TACH1_GPIO1	AL19	PU_TACH1
					TACH0_GPIO17	AV21	PU_TACH0

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E93039-001

P3V3

R1F3 1/16W 10.0K 1% 0402LF A93548-034
R1F9 1/16W 10.0K 1% 0402LF A93548-034
R1F16 1/16W 10.0K 1% 0402LF A93548-034
R1F8 1/16W 10.0K 1% 0402LF A93548-034
R1F4 1/16W 10.0K 1% 0402LF A93548-034
R1F17 1/16W 10.0K 1% 0402LF A93548-034
R2E40 1/16W 10.0K 1% 0402LF A93548-034
R2E35 1/16W 10.0K 1% 0402LF A93548-034

NOTE: UNUSED TACH INPUTS MUST BE PULLED UP
DEFAULT SET AS GPI

137< OUT PD_SSB_TS_VSS1 — R2G12 1K 1% 1/16W A93548-023 0402LF
137> IN PD_SSB_TS_VSS2 — R2G14 1K 1% 1/16W A93548-023 0402LF
137< OUT PD_SSB_TS_VSS3 — R2G13 1K 1% 1/16W A93548-023 0402LF
137> IN PD_SSB_TS_VSS4 — R2G15 1K 1% 1/16W A93548-023 0402LF

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Wed Oct 27 15:21:40 2010

PATSBURG (3 OF 8)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 137 OF 303

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U2F1
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PBG_EXT_F

174> IN	PE_SSB_IBMC_RX_C_DP	AJ8	PCIE_PERP<8>	PCIE_PETP<8>	AK3	PE_SSB_IBMC_TX_DP	OUT 174<
174> IN	PE_SSB_IBMC_RX_C_DN	AJ9	PCIE_PERN<8>	PCIE_PETN<8>	AL2	PE_SSB_IBMC_TX_DN	OUT 174<
	TP_PCIE_PERP_7	AH9	PCIE_PERP<7>	PCIE_PETP<7>	AJ2	TP_PCIE_PETP_7	
	TP_PCIE_PERN_7	AH8	PCIE_PERN<7>	PCIE_PETN<7>	AK1	TP_PCIE_PETN_7	
	TP_PCIE_PERP_6	AF9	PCIE_PERP<6>	PCIE_PETP<6>	AH3	TP_PCIE_PETP_6	
	TP_PCIE_PERN_6	AF8	PCIE_PERN<6>	PCIE_PETN<6>	AH2	TP_PCIE_PETN_6	
	TP_PCIE_PERP_5	AE9	PCIE_PERP<5>	PCIE_PETP<5>	AG2	TP_PCIE_PETP_5	
	TP_PCIE_PERN_5	AE8	PCIE_PERN<5>	PCIE_PETN<5>	AH1	TP_PCIE_PETN_5	
	TP_PCIE_PERP_4	AJ5	PCIE_PERP<4>	PCIE_PETP<4>	AE3	TP_PCIE_PETP_4	
	TP_PCIE_PERN_4	AJ6	PCIE_PERN<4>	PCIE_PETN<4>	AF2	TP_PCIE_PETN_4	
	TP_PCIE_PERP_3	AH5	PCIE_PERP<3>	PCIE_PETP<3>	AD2	TP_PCIE_PETP_3	
	TP_PCIE_PERN_3	AH6	PCIE_PERN<3>	PCIE_PETN<3>	AE1	TP_PCIE_PETN_3	
	TP_PCIE_PERP_2	AF4	PCIE_PERP<2>	PCIE_PETP<2>	AB3	TP_PCIE_PETP_2	
	TP_PCIE_PERN_2	AF5	PCIE_PERN<2>	PCIE_PETN<2>	AC2	TP_PCIE_PETN_2	
	TP_PCIE_PERP_1	AE5	PCIE_PERP<1>	PCIE_PETP<1>	AB2	TP_PCIE_PETP_1	
	TP_PCIE_PERN_1	AE4	PCIE_PERN<1>	PCIE_PETN<1>	AB1	TP_PCIE_PETN_1	
	NC_PEG0_RXP<3>	AW7	PEG0_RXP<3>	PEG0_TXP<3>	AP7	NC_PEG0_TXP<3>	
	NC_PEG0_RXN<3>	AV8	PEG0_RXN<3>	PEG0_TXN<3>	AR7	NC_PEG0_TXN<3>	
	NC_PEG0_RXP<2>	AV6	PEG0_RXP<2>	PEG0_TXP<2>	AR6	NC_PEG0_TXP<2>	
	NC_PEG0_RXN<2>	AU7	PEG0_RXN<2>	PEG0_TXN<2>	AP6	NC_PEG0_TXN<2>	
	NC_PEG0_RXP<1>	AU5	PEG0_RXP<1>	PEG0_TXP<1>	AN4	NC_PEG0_TXP<1>	
	NC_PEG0_RXN<1>	AV5	PEG0_RXN<1>	PEG0_TXN<1>	AR4	NC_PEG0_TXN<1>	
	NC_PEG0_RXP<0>	AT3	PEG0_RXP<0>	PEG0_TXP<0>	AN3	NC_PEG0_TXP<0>	
	NC_PEG0_RXN<0>	AU3	PEG0_RXN<0>	PEG0_TXN<0>	AP3	NC_PEG0_TXN<0>	
	NC_SSB_TP7	AN2	TP7	GNT_3_N_GPIO55	AF30	FM_BIOS_RCVR_BOOT_N	IN 150>
	NC_SSB_TP8	AT1	TP8	GNT_2_N_GPIO53_GSXDIN	AJ34	SGPIO_GSX_MUX_DIN	IN 147>
	NC_SSB_TP9	AP1	TP9	GNT_1_N_GPIO51_GSXDOUT	AU15	PU_SGPIO_GSX_DOUT	IN 147>
	NC_SSB_TP10	AU1	TP10	GNT_0_N	AN33	TP_PCI_SSB_GNT_0_N	
	NC_PEG0_RBIASN	AL5	PEG0_RBIASN				
	NC_PEG0_RBIASN	AL4	PEG0_RBIASP	REQ3_N_GPIO54_GSXSRESET_N	AK21	PU_SGPIO_GSX_RESET	
				REQ2_N_GPIO52_GSXSLOAD	AK34	SGPIO_GSX_LOAD_R	R8R25 33.2 1% 1/16W 0402LF A93548-001
				REQ1_N_GPIO50_GSXCLK	AR34	SGPIO_GSX_CLK_R	R8R26 33.2 1% 1/16W 0402LF A93548-001
	TP_PCI_AD<31>	AA31	AD<31>				
	TP_PCI_AD<30>	AL30	AD<30>	CXBE_N<3>	AU20	TP_PCI_CXBE3_N	CAD NOTE: PLACE 33OHMS RES WITHIN 1" FROM PBG
	TP_PCI_AD<29>	AG31	AD<29>	CXBE_N<2>	AL33	TP_PCI_CXBE2_N	
	TP_PCI_AD<28>	AR33	AD<28>	CXBE_N<1>	AL18	TP_PCI_CXBE1_N	
	TP_PCI_AD<27>	AL34	AD<27>	CXBE_N<0>	AM31	TP_PCI_CXBE0_N	
	TP_PCI_AD<26>	AD32	AD<26>				
	TP_PCI_AD<25>	AV13	AD<25>	DEVSEL_N	AJ32	PU_PCI_DEVSEL_N	R1F6 A93549-022 1/16W 8.2K 5% 0402LF
	TP_PCI_AD<24>	AM24	AD<24>	FRAME_N	AF31	PU_PCI_FRAME_N	R1F7 A93549-022 1/16W 8.2K 5% 0402LF
	TP_PCI_AD<23>	AK27	AD<23>	IRDY_N	AP18	PU_PCI_IRDY_N	R2E22 A93549-022 1/16W 8.2K 5% 0402LF
	TP_PCI_AD<22>	AL21	AD<22>	PAR	AK28	TP_PCI_PAR	1/16W 8.2K 5% 0402LF
	TP_PCI_AD<21>	AK33	AD<21>	PCIRST_N	E33	TP_PCI_RST_N	
	TP_PCI_AD<20>	AN34	AD<20>	PERR_N	AM19	PU_PCI_PERR_N	R2E39 A93549-022
	TP_PCI_AD<19>	AG32	AD<19>	PLOCK_N	AR15	PU_PCI_PLOCK_N	R2E23 A93549-022 1/16W 8.2K 5% 0402LF
	TP_PCI_AD<18>	AG30	AD<18>	PME_N	C37	TP_PCI_PME_N	1/16W 8.2K 5% 0402LF
	TP_PCI_AD<17>	AU22	AD<17>	REQ0_N	AL27	PU_PCI_REQ0_N	R2E18 A93549-022
	TP_PCI_AD<16>	AM25	AD<16>	SERR_N	AN16	PU_PCI_SERR_N	R2E24 A93549-022 1/16W 8.2K 5% 0402LF
	TP_PCI_AD<15>	AM30	AD<15>	STOP_N	AV19	PU_PCI_STOP_N	1/16W 8.2K 5% 0402LF R2E36 A93549-022
	TP_PCI_AD<14>	AL31	AD<14>	TRDY_N	AR12	PU_PCI_TRDY_N	R2E25 A93549-022 1/16W 8.2K 5% 0402LF
	TP_PCI_AD<13>	AP12	AD<13>				1/16W 8.2K 5% 0402LF
	TP_PCI_AD<12>	AM18	AD<12>	PIRQA_N	AR19	PU_PCI_PIRQA_N	R2E20 A93549-022
	TP_PCI_AD<11>	AW20	AD<11>	PIRQB_N	AJ30	PU_PCI_PIRQB_N	1/16W 8.2K 5% 0402LF R2E31 A93549-022
	TP_PCI_AD<10>	AC32	AD<10>	PIRQC_N	AV18	PU_PCI_PIRQC_N	R2E37 A93549-022 1/16W 8.2K 5% 0402LF
	TP_PCI_AD<9>	AW12	AD<9>	PIRQD_N	AR18	PU_PCI_PIRQD_N	1/16W 8.2K 5% 0402LF R2E21 A93549-022
	TP_PCI_AD<8>	AU25	AD<8>	PIRQE_N_GPIO2	AF32	FM_ERR0_LVC3_N	1/16W 8.2K 5% 0402LF
	TP_PCI_AD<7>	AU12	AD<7>	PIRQF_N_GPIO3	AL22	FM_ERR1_DLY_CO_N	IN 78> BI 129< 147> 169>
	TP_PCI_AD<6>	Y30	AD<6>	PIRQG_N_GPIO4	AA32	FM_IBMC_SSB_SMI_LPC_N	IN 147> 175>
	TP_PCI_AD<5>	AV14	AD<5>	PIRQH_N_GPIO5	AR16	IRQ_IBMC_SSB_NMI	IN 148>
	TP_PCI_AD<4>	AP36	AD<4>	SERIRQ	C22	IRQ_SERIAL	BI 147> 156> 156<> 175<>
	TP_PCI_AD<3>	AR36	AD<3>				
	TP_PCI_AD<2>	AN15	AD<2>				
	TP_PCI_AD<1>	AA30	AD<1>				
	TP_PCI_AD<0>	AW15	AD<0>				

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P3V3

R2E38 8.2K 1/16W 5% 0402LF A93549-022

SGPIO_GSX_LOAD OUT 151<
SGPIO_GSX_CLK OUT 151<

P3V3

NOTE: UNUSED PCI INPUTS MUST BE PULLED UP

DESIGN NOTE:
ERR1# NEEDS A 400US DELAY BEFORE IT IS CONNECTED TO PBG

ROOM INTEL_SI
ROOM SB

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PATSBURG (4 OF 8)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 138 OF 303	

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SAS SCU0: PORTS 0 TO 3
SATA PORTS 0 & 1: G2 @3.0 GBPS

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PBG_EXT_F

NC_SAS_RXP<7>	AR31	SAS_RXP<7>	SAS_TXP<7>	AJ38	NC_SAS_TXP<7>		
NC_SAS_RXN<7>	AP31	SAS_RXN<7>	SAS_TXN<7>	AK39	NC_SAS_TXN<7>		
NC_SAS_RXP<6>	AR30	SAS_RXP<6>	SAS_TXP<6>	AK37	NC_SAS_TXP<6>		
NC_SAS_RXN<6>	AP30	SAS_RXN<6>	SAS_TXN<6>	AL38	NC_SAS_TXN<6>		
NC_SAS_RXP<5>	AR28	SAS_RXP<5>	SAS_TXP<5>	AM38	NC_SAS_TXP<5>		
NC_SAS_RXN<5>	AN28	SAS_RXN<5>	SAS_TXN<5>	AN39	NC_SAS_TXN<5>		
NC_SAS_RXP<4>	AR27	SAS_RXP<4>	SAS_TXP<4>	AN37	NC_SAS_TXP<4>		
NC_SAS_RXN<4>	AN27	SAS_RXN<4>	SAS_TXN<4>	AN38	NC_SAS_TXN<4>		
162< IN SAS_RXP<3>	AR25	SAS_RXP<3>	SAS_TXP<3>	AU33	SAS_TXP<3>	OUT 162<	
162< IN SAS_RXN<3>	AP25	SAS_RXN<3>	SAS_TXN<3>	AV32	SAS_TXN<3>	OUT 162<	
162< IN SAS_RXP<2>	AR24	SAS_RXP<2>	SAS_TXP<2>	AV31	SAS_TXP<2>	OUT 162<	
162< IN SAS_RXN<2>	AP24	SAS_RXN<2>	SAS_TXN<2>	AW30	SAS_TXN<2>	OUT 162<	
162< IN SAS_RXP<1>	AN22	SAS_RXP<1>	SAS_TXP<1>	AU30	SAS_TXP<1>	OUT 162<	
162< IN SAS_RXN<1>	AR22	SAS_RXN<1>	SAS_TXN<1>	AV29	SAS_TXP<0>	OUT 162<	
162< IN SAS_RXP<0>	AN21	SAS_RXP<0>	SAS_TXP<0>	AV28	SAS_TXN<0>	OUT 162<	
162< IN SAS_RXN<0>	AR21	SAS_RXN<0>	SAS_TXN<0>	AW28			
TP_SATA_RXP<5>	F22	SATA_RXP<5>	SATA_TXP<5>	B22	TP_SATA_TXP<5>		
TP_SATA_RXN<5>	E22	SATA_RXN<5>	SATA_TXN<5>	A22	TP_SATA_TXN<5>		
TP_SATA_RXP<4>	F21	SATA_RXP<4>	SATA_TXP<4>	C20	TP_SATA_TXP<4>		
TP_SATA_RXN<4>	E21	SATA_RXN<4>	SATA_TXN<4>	B21	TP_SATA_TXN<4>		
TP_SATA_RXP<3>	F19	SATA_RXP<3>	SATA_TXP<3>	B19	TP_SATA_TXP<3>		
TP_SATA_RXN<3>	E19	SATA_RXN<3>	SATA_TXN<3>	A20	TP_SATA_TXN<3>		
TP_SATA_RXP<2>	F18	SATA_RXP<2>	SATA_TXP<2>	C17	TP_SATA_TXP<2>		
TP_SATA_RXN<2>	E18	SATA_RXN<2>	SATA_TXN<2>	B18	TP_SATA_TXN<2>		
161< IN SATA_RXP<1>	F16	SATA_RXP<1>	SATA_TXP<1>	C12	SATA_TXP<1>	OUT 161<	
161< IN SATA_RXN<1>	E16	SATA_RXN<1>	SATA_TXN<1>	B13	SATA_TXN<1>	OUT 161<	
161< IN SATA_RXP<0>	F15	SATA_RXP<0>	SATA_TXP<0>	B12	SATA_TXP<0>	OUT 161<	
161< IN SATA_RXN<0>	E15	SATA_RXN<0>	SATA_TXN<0>	A12	SATA_TXN<0>	OUT 161<	
SGPIO_SAS1_CLOCK	AL8	SAS_CLOCK1	RBIAS_SATA3	B14	A_RBIAS_SATA3	OUT 139<	
SGPIO_SAS1_LOAD	AN10	SAS_LOAD1	SATA3COMPI	C15	A_SATA3_ZCOMP	OUT 139<	
SGPIO_SAS1_DATAIN	AL9	SAS_DATAIN1	SATA3COMPO	J16			
SGPIO_SAS1_DATAOUT	AV9	SAS_DATAOUT1	TP19	B10	NC_SSB_TP19		
NC_SGPIO_SAS2_CLOCK	AW10	SAS_CLOCK2	SATAICOMPI	K18	A_SATA_ZCOMP	OUT 139<	
NC_SGPIO_SAS2_LOAD	AV10	SAS_LOAD2	SATAICOMPO	J18			
NC_SGPIO_SAS2_DATAIN	AU10	SAS_DATAIN2	TP22	B15	NC_SSB_TP22		
NC_SGPIO_SAS2_DATAOUT	AR10	SAS_DATAOUT2					
230< OUT LED_SAS_ACT_N	AR9	SAS_LED_N	SATALED_N	B27	LED_SATA_ACT_N	OUT 230<	
NC_SSB_TP13	AU37	TP13	SCLOCK_GPIO22	F27	PU_SGPIO_SATA_CLOCK	IN 155>	
NC_SSB_TP15	AV35	TP15	SDATAOUT1_GPIO48	E27	PU_SGPIO_SATA_DATAOUT1	IN 155>	
NC_SSB_TP17	AU35	TP17	SDATAOUT0_GPIO39	K25	PU_SGPIO_SATA_DATAOUT0	IN 155>	
139< OUT A_SAS_RBIASP_0	AV26	SAS_RBIASP<0>	SLOAD_GPIO38	A30	PU_SGPIO_SATA_LOAD	IN 155>	
	AW25	SAS_RBIASN<0>					
NC_SSB_TP14	AU39	TP14	SMBALERT_N_GPIO11	J31	PU_SMB_ALERT_N	IN 147>	
NC_SSB_TP16	AT39	TP16	SMBCLK	G37	SMB_HOST_STBY_LVC3_CLK	BI 32< 177> 188< 190> 202<	
NC_SSB_TP18	AR38	TP18	SMBDATA	H38	SMB_HOST_STBY_LVC3_DATA	BI 32<> 177<> 188<> 190<> 202<>	
NC_A_SAS_RBIASP_1	AL25	SAS_RBIASP<1>	SML0ALERT_N_GPIO60	H34	IRQ_SML0_ALERT_N	OUT 176< 188< 190>	
NC_A_SAS_RBIASN_1	AL24	SAS_RBIASN<1>	SML0CLK	F36	SMB_SMLINK0_STBY_LVC3_CLK	BI 177> 188< 190> 177<> 188<> 190<>	
149> OUT SMB_SAS_SES_CLK	AJ12	SAS_SMBCLK0	SML0DATA	G36	SMB_SMLINK0_STBY_LVC3_DATA	BI	
149<> BI SMB_SAS_SES_DATA	AL11	SAS_SMBDATA0	SML1ALERT_N_PCHHOT_N_GPIO74	J33	FM_SSB_IBMC_THERMTRIP_N	OUT 147> 176<	
PU_SMB_SAS1_CLK	AH13	SAS_SMBCLK1	SML1CLK_GPIO58	K37	SMB_SMLINK1_STBY_LVC3_CLK	BI 188<	
PU_SMB_SAS1_DATA	AH12	SAS_SMBDATA1	SML1DATA_GPIO75	K39	SMB_SMLINK1_STBY_LVC3_DATA	BI 231<	
147> OUT PU_SMB_SAS_BBU_CLK2	AL13	SAS_SMBCLK2					
147> BI PU_SMB_SAS_BBU_DATA2	AM13	SAS_SMBDATA2					

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E93039-001

CAD NOTE: PUT RESISTORS WITHIN 2" OF PATSBURG PINS

149< 147> OUT SGPIO_SAS1_CLOCK — A93548-045 49.9 1% 1/16W 0402LF — R2E43 — SGPIO_SAS1_CLOCK_R
149< 147> OUT SGPIO_SAS1_LOAD — A93548-045 49.9 1% 1/16W 0402LF — R2F4 — SGPIO_SAS1_LOAD_R_R
149< 147> IN SGPIO_SAS1_DATAIN — A93548-045 49.9 1% 1/16W 0402LF — R2F1 — SGPIO_SAS1_DATAIN_R
149< 147> OUT SGPIO_SAS1_DATAOUT — A93548-045 49.9 1% 1/16W 0402LF — R2E6 — SGPIO_SAS1_DATAOUT_R

CAD NOTE:CONNECT RBIASN FROM RBIAS RES PIN2

P3V3

R2E16 4.7K 1% 1/16W A93548-517 0402LF
R2E17 4.7K 1% 1/16W A93548-517 0402LF

CAD NOTE: SATA Z COMP NET SHOULD BE <0.2 OHMS
COMPI & RCOMPO MUST HAVE DIFERENT TRACES FROM RESISTOR CONECTION

P1V1_MAIN_PBG
R8T11 1 2 49.9 A_SATA3_ZCOMP IN 139>
0402LF 1% 1/16W
A93548-045

CAD NOTE: PLACE CLOSE TO PBG
COMPI & RCOMPO SHOULD BE SHORTED UNDER PACKAGE
KEEP ROUTING <0.2 OHMS

P1V1_MAIN_PBG
R8T13 1 2 37.4 A_SATA_ZCOMP IN 139>
0402LF 1% 1/16W
A93548-047

CAD NOTE: PLACE CLOSE TO PBG
KEEP ROUTING <0.2 OHMS

A_RBIAS_SATA3 IN 139>
R2F15 750 1% 1/16W A93548-101 0402LF

CAD NOTE: PLACE CLOSE TO PBG
KEEP ROUTING < 1 OHM

CAD NOTE: CONNECT RBIASN FROM RBIASP RES PIN2
KEEP ROUTING <1 OHM AVOID LAYER CHANGES

A_SAS_RBIASP_0 IN 139>
R8T1 16.04K 1% 1/16W A93548-197 0402LF
C2 1UF 10V 10% A36096-099 0402LF

R8T10 0 5% 1/16W A93549-001 0402LF
R1F30 0 5% 1/16W A93549-001 0402LF

SMB_LAN_STBY_LVC3_DATA BI 177<> 190<> 219<>
SMB_LAN_STBY_LVC3_CLK BI 177> 190> 219<>

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DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 139 OF 303	

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IC

PBG_EXT_F

NC_SSB_RSVD<33>	B5	RESERVED<33>	RESERVED<32>	B6	NC_SSB_RSVD<32>
NC_SSB_RSVD<34>	A7	RESERVED<34>	RESERVED<27>	E6	NC_SSB_RSVD<27>
NC_SSB_RSVD<29>	C5	RESERVED<29>	RESERVED<30>	C10	NC_SSB_RSVD<30>
NC_SSB_RSVD<28>	E10	RESERVED<28>	RESERVED<31>	B8	NC_SSB_RSVD<31>
USB2_13_DP	Y36	USBP<13>	USBRBIASP	U32	A_USB_RBIAS
USB2_13_DN	Y34	USBN<13>	USBRBIASN	V32	
TP_USB2_12_DP	AA36	USBP<12>	TP24	P31	NC_SSB_TP24
TP_USB2_12_DN	AA34	USBN<12>	TP23	P32	NC_SSB_TP23
USB2_11_DP	AC35	USBP<11>			
USB2_11_DN	AC34	USBN<11>	CHIP_DETECT_N	B2	FM_SSB_PRSNT_CO_N
USB2_10_DP	AD35	USBP<10>			
USB2_10_DN	AD34	USBN<10>	NC_4	AV2	NC_SSB_4
USB2_09_DP	V35	USBP<9>	NC_3	AV38	NC_SSB_3
USB2_09_DN	V34	USBN<9>	NC_2	B38	NC_SSB_2
USB2_08_DP	U35	USBP<8>			
USB2_08_DN	U34	USBN<8>			
USB2_07_DP	AF38	USBP<7>			
USB2_07_DN	AE37	USBN<7>			
USB2_06_DP	AE39	USBP<6>			
USB2_06_DN	AD38	USBN<6>			
USB2_05_DP	AC38	USBP<5>			
USB2_05_DN	AB37	USBN<5>			
NC_USB2_04_DP	AB39	USBP<4>			
NC_USB2_04_DN	AB38	USBN<4>			
USB_03_DP	AA38	USBP<3>			
USB_03_DN	Y37	USBN<3>			
USB2_02_DP	V38	USBP<2>			
USB2_02_DN	U37	USBN<2>			
USB2_01_DP	Y39	USBP<1>			
USB2_01_DN	W38	USBN<1>			
USB2_00_DP	U39	USBP<0>			
USB2_00_DN	U38	USBN<0>			

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E93039-001

P3V3_STBY

R2F13
10.0K
1%
1/16W
A93548-034
0402LF

OUT 140<
OUT 140<
OUT 169< 170<

140> IN NC_SSB_RSVD<31>

R2G16
100
1%
1/16W
CHIP
A93548-043
0402LF

CAD NOTE: PLACE CLOSE TO PBG
KEEP ROUTING < 0.2 OHMS
AVOID ROUTING NEXT TO CLOCK PINS OR UNDER STITCHING CAPS
SHORT RBIASP & RBIASN ON PBG VIA FIELD
RBIASP & RBIASN CAN BE SHORTED UNDER PACKAGE

A_USB_RBIAS IN 140>

R8T7
22.6
1%
1/16W
A93548-056
0402LF

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Patsburg USB2 Ports			Potter City	OC#
EHCI #1	UHCI#1	Port 0	Zepher Flash drive	0
		Port 1	Rear Connector 1 (USB 2.0)	2
	UHCI#2	Port 2	User Bay Floppy like (Int Type A USB)	1
		Port 3	iBMC USB 1.1	-
	UHCI#3	Port 4	Not connected	
		Port 5	Rear Connector 1 (USB 2.0)	2
	UHCI#4	Port 6	Rear Connector 2 (USB 2.0)	3
		Port 7	Rear Connector 2 (USB 2.0)	3
EHCI #2	UHCI#5	Port 8	Internal USB 1 to Front Panel	4
		Port 9	Internal USB 1 to Front Panel	4
	UHCI#6	Port 10	Internal USB 2 to Front Panel	5
		Port 11	Internal USB 2 to Front Panel	5
	UHCI#7	Port 12	Not connected	
		Port 13	iBMC USB 2.0	-

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PBG_EXT_F

P1V1_MAIN_PBG

Y16	VCC<30>		VCCASW<18>	V24	
W16	VCC<29>		VCCASW<17>	AC25	
J15	VCC<28>		VCCASW<16>	AC26	
N16	VCC<27>		VCCASW<15>	AC28	
N15	VCC<26>		VCCASW<14>	AD25	
AC16	VCC<25>		VCCASW<13>	AD26	
AC17	VCC<24>		VCCASW<12>	AD28	
AC18	VCC<23>		VCCASW<11>	T22	
AC19	VCC<22>		VCCASW<10>	T23	
AC20	VCC<21>		VCCASW<9>	T24	
AD16	VCC<20>		VCCASW<8>	U22	
AD17	VCC<19>		VCCASW<7>	U23	
AD18	VCC<18>		VCCASW<6>	U24	
AD19	VCC<17>		VCCASW<5>	W22	
AD20	VCC<16>		VCCASW<4>	W23	
T17	VCC<15>		VCCASW<3>	W24	
T18	VCC<14>		VCCASW<2>	Y22	
T19	VCC<13>		VCCASW<1>	Y23	
T20	VCC<12>		VCCASW<0>	Y24	
U17	VCC<11>				
U18	VCC<10>		VCC_IO<44>	T13	
U19	VCC<9>		VCC_IO<43>	T12	
U20	VCC<8>		VCC_IO<7>	AC9	
W17	VCC<7>		VCC_IO<6>	AC8	
W18	VCC<6>		VCC_IO<5>	AC13	
W19	VCC<5>		VCC_IO<4>	AC12	
W20	VCC<4>		VCC_IO<46>	W11	
Y17	VCC<3>		VCC_IO<47>	W12	
Y18	VCC<2>		VCC_IO<48>	W15	
Y19	VCC<1>		VCC_IO<8>	AE11	
Y20	VCC<0>		VCC_IO<3>	AB9	
			VCC_IO<2>	AB8	
AF24	VCC_IO<15>		VCC_IO<49>	Y11	
AE24	VCC_IO<9>		VCC_IO<50>	Y12	
AF25	VCC_IO<16>		VCC_IO<51>	Y15	
AF26	VCC_IO<17>		VCC_IO<55>	Y9	
AF28	VCC_IO<18>		VCC_IO<1>	AB13	
AH25	VCC_IO<22>		VCC_IO<0>	AB12	
AH26	VCC_IO<23>		VCCSCUSW<5>	AC22	
AH28	VCC_IO<24>		VCCSCUSW<4>	AC23	
AJ25	VCC_IO<29>		VCCSCUSW<3>	AC24	
AJ26	VCC_IO<30>		VCCSCUSW<2>	AD22	
AJ28	VCC_IO<31>		VCCSCUSW<1>	AD23	
			VCCSCUSW<0>	AD24	
143> IN P1V1_SSB_VCCSAS0_PLL	AH20	VCCPLLSAS0<1>			
	AJ20	VCCPLLSAS0<0>	VCCXUSW<2>	AE12	
	AF20	VCC_IO<14>	VCCXUSW<1>	AC15	
			VCCXUSW<0>	AD15	
AH23	VCC_IO<21>				
AJ23	VCC_IO<28>		VCC_IO<37>	M24	
143> IN P1V1_SSB_VCCSAS1_PLL	AF23	VCCPLLSAS1	VCC_IO<40>	N23	
			VCC_IO<41>	N24	
AJ22	VCCSAS1_5<2>				
P1V5_MAIN_PBG	AH22	VCCSAS1_5<1>	VCC_IO<35>	L23	
	AF22	VCCSAS1_5<0>			
			VCC_IO<34>	L19	
AR2	VCCXUSW<13>		VCC_IO<36>	M19	
AN9	VCCXUSW<12>				
AF12	VCCXUSW<4>		VCC_IO<54>	Y28	
AF11	VCCXUSW<3>		VCC_IO<53>	Y26	
AF16	VCCXUSW<5>		VCC_IO<52>	Y25	
AF17	VCCXUSW<6>				
AH15	VCCXUSW<7>		DCPSUS<1>	U15	A_VCCA_USBSUS
AH16	VCCXUSW<8>				
AJ15	VCCXUSW<10>		DCPSUS<2>	U16	TP_VCCSUS1
AJ16	VCCXUSW<11>		DCPSUS<0>	N26	TP_VCCSUS0
P3V3_STBY	R22	VCC3_3<6>	VCCSUS3_3<4>	R25	
	N22	VCC3_3<5>	VCCSUS3_3<5>	T25	
AJ18	VCC3_3<3>				
AH18	VCC3_3<2>		VCCDFTERM<0>	L18	
			VCCDFTERM<1>	M18	
W25	VCCSUS3_3<2>		VCCDFTERM<2>	N17	
W26	VCCSUS3_3<1>		VCCDFTERM<3>	N18	
W28	VCCSUS3_3<0>				
AC29	VCC3_3<0>				
AC30	VCC3_3<1>				

P1V1_STBY_PBG
P1V1_MAIN_PBG
P3V3_STBY
P3V3
A_VCCA_USBSUS
TP_VCCSUS1
TP_VCCSUS0

C8T26
1.0UF
6.3V
10%
A36096-027
0402LF

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E93039-001

U2F1
IC

PBG_EXT_F

P1V1_MAIN_PBG
P5V_STBY
P5V

143> IN P1V1_SSB_VCCPE_G3_PLL	AF15	VCCPLLEXPU	V_PROC_IO	L16	P1V05_VTT_CPU0
	AJ13	VCCXUSW<9>	DCPSST	L25	A_VCCSST_CAP
	AD29	VCC5REF	VCC_DMI	L15	
	U28	VCC5REFSUS	VCC_IO<39>	N20	P1V1_MAIN_PBG
144> IN P1V1_SSB_VCCAUPLL	M25	VCCAUPLL	VCC_IO<42>	P12	
144> IN P3V3_SSB_VCCAUBG	U29	VCCAUBG	VCC_IO<45>	T16	
144> IN P3V3_SSB_VCCASATABG	L24	VCC3_3<4>	DCPRTC	M28	A_VCCRTEXT
	L20	VCC_VRM<1>	VCCSUS3_3<3>	T15	
143> IN P1V1_SSB_VCCSATA3_PLL	M20	VCCAPLL_SATA	VCCSPI	N25	P3V3_VBAT
143> IN P1V1_SSB_VCCDMI_PLL	P8	VCCAPLL_EXP	VCCRTC	L28	
143> IN P1V1_SSB_VCCCPY_PLL	Y8	VCCAPLL_DMI2	DCPSUS_BYP	L26	TP_VCCDSW3_3
	L17	VCC_VRM<0>	VCCSUSHDA	U25	
			VCCDSW3_3	N28	
144> IN P3V3_SSB_VCCA3GBG	T8	VCC3_3<7>	VCCASW<19>	T26	
			VCCASW<20>	T28	P1V1_STBY_PBG
			VCCASW<21>	U26	

A_VCCA_SATA3DMI_VRM

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C8T44
0.1UF
10V
10%
A36096-043
0402LF

C8T41
1.0UF
6.3V
10%
A36096-027
0402LF

P1V5_MAIN_PBG
R1F11
1 0 2
1/10W 5% 0603LF
A93552-004

NOTE: THIS RESISTOR SHOULD BE PLACED WHEN INTERNAL PLL VRM IS ENABLED AND REMOVED WHEN EXTERNAL PLL IS USED

P1V1_MAIN_PBG
R1F12
1 0 2
1/10W 5% 0603LF
A93552-004

NOTE: THIS RESISTOR SHOULD BE REMOVED WHEN INTERNAL PLL VRM IS ENABLED AND PLACED WHEN EXTERNAL PLL IS USED

**CAD NOTE: ALL P3V3_STBY BALLS NEED TO TIE TOGETHER IN BOARD AND SUPPLIED THROUGH THE SINGLE SOURCE OF POWER SUPPLY

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IC

PBG_EXT_F

M15	VSS<246>	VSS<182>	AH11
L22	VSS<245>	VSS<181>	AH17
AA1	VSS<244>	VSS<180>	AH19
AA3	VSS<243>	VSS<179>	AH24
AA33	VSS<242>	VSS<178>	AH7
AA37	VSS<241>	VSS<177>	AJ1
AA39	VSS<240>	VSS<176>	AJ11
AB11	VSS<239>	VSS<175>	AJ17
AB15	VSS<238>	VSS<174>	AJ19
AB16	VSS<237>	VSS<173>	AJ24
AB17	VSS<236>	VSS<172>	AJ29
AB18	VSS<235>	VSS<171>	AJ3
AB19	VSS<234>	VSS<170>	AJ33
AB20	VSS<233>	VSS<169>	AJ37
AB22	VSS<232>	VSS<168>	AJ39
AB23	VSS<231>	VSS<167>	AJ7
AB24	VSS<230>	VSS<166>	AL1
AB26	VSS<229>	VSS<165>	AL10
AB28	VSS<228>	VSS<164>	AL3
AB7	VSS<227>	VSS<163>	AL37
AC11	VSS<226>	VSS<162>	AL39
AC33	VSS<225>	VSS<161>	AL6
AC7	VSS<224>	VSS<160>	AM10
AD1	VSS<223>	VSS<159>	AM15
AD3	VSS<222>	VSS<158>	AM16
AD30	VSS<221>	VSS<157>	AM21
AD33	VSS<220>	VSS<156>	AM22
AD37	VSS<219>	VSS<155>	AM27
AD39	VSS<218>	VSS<154>	AM28
AE10	VSS<217>	VSS<153>	AM33
AE15	VSS<216>	VSS<152>	AM34
AE16	VSS<215>	VSS<151>	AM4
AE17	VSS<214>	VSS<150>	AM9
AE18	VSS<213>	VSS<149>	AN12
AE19	VSS<212>	VSS<148>	AN13
AE20	VSS<211>	VSS<147>	AN18
AE22	VSS<210>	VSS<146>	AN19
AE23	VSS<209>	VSS<145>	AN24
AE25	VSS<208>	VSS<144>	AN25
AE26	VSS<207>	VSS<143>	AN30
AE28	VSS<206>	VSS<142>	AN31
A11	VSS<205>	VSS<141>	AN36
A13	VSS<204>	VSS<140>	AN6
A16	VSS<203>	VSS<139>	AN7
A19	VSS<202>	VSS<138>	AP37
A21	VSS<201>	VSS<137>	AP39
A24	VSS<200>	VSS<136>	AR3
A26	VSS<199>	VSS<135>	AU11
A29	VSS<198>	VSS<134>	AU13
A31	VSS<197>	VSS<133>	AU16
A36	VSS<196>	VSS<132>	AU19
A6	VSS<195>	VSS<131>	AU21
A8	VSS<194>	VSS<130>	AU24
AE6	VSS<193>	VSS<129>	AU26
AF1	VSS<192>	VSS<128>	AU29
AF10	VSS<191>	VSS<127>	AU31
AF18	VSS<190>	VSS<126>	AU34
AF19	VSS<189>	VSS<125>	AU6
AF3	VSS<188>	VSS<124>	AU8
AF33	VSS<187>	VSS<123>	AW11
AF37	VSS<186>	VSS<122>	AW13
AF39	VSS<185>	VSS<121>	AW16
AF6	VSS<184>	VSS<120>	AW19
AG33	VSS<183>	VSS<119>	AW21

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U2F1
IC

PBG_EXT_F

AW24	VSS<118>	VSS<55>	M33
AW26	VSS<117>	VSS<54>	N1
AW29	VSS<116>	VSS<53>	N10
AW3	VSS<115>	VSS<52>	A4
AW31	VSS<114>	VSS<51>	A3
AW34	VSS<113>	VSS<50>	N19
AW36	VSS<112>	VSS<49>	N3
AW37	VSS<111>	VSS<48>	N37
AW4	VSS<110>	VSS<47>	N39
AW6	VSS<109>	VSS<46>	N6
AW8	VSS<108>	VSS<45>	P10
C11	VSS<107>	VSS<44>	P30
C13	VSS<106>	VSS<43>	P33
C16	VSS<105>	VSS<42>	P6
C19	VSS<104>	VSS<41>	R15
C21	VSS<103>	VSS<40>	R16
C24	VSS<102>	VSS<39>	R17
C26	VSS<101>	VSS<38>	R18
C29	VSS<100>	VSS<37>	R19
C34	VSS<99>	VSS<36>	R20
C6	VSS<98>	VSS<35>	R23
C8	VSS<97>	VSS<34>	R24
D39	VSS<96>	VSS<33>	R26
F1	VSS<95>	VSS<32>	R28
F3	VSS<94>	VSS<31>	R30
F37	VSS<93>	VSS<30>	R33
G10	VSS<92>	VSS<29>	T1
G12	VSS<91>	VSS<28>	T11
G13	VSS<90>	VSS<27>	T3
G15	VSS<89>	VSS<26>	T37
G16	VSS<88>	VSS<25>	T39
G18	VSS<87>	VSS<24>	T7
G19	VSS<86>	VSS<23>	U11
G21	VSS<85>	VSS<22>	U33
G22	VSS<84>	VSS<21>	U7
G24	VSS<83>	VSS<20>	V15
G25	VSS<82>	VSS<19>	V16
G27	VSS<81>	VSS<18>	V17
G28	VSS<80>	VSS<17>	V18
G30	VSS<79>	VSS<16>	V19
G31	VSS<78>	VSS<15>	V20
G33	VSS<77>	VSS<14>	V22
G34	VSS<76>	VSS<13>	V23
G4	VSS<75>	VSS<12>	V25
G6	VSS<74>	VSS<11>	V26
G7	VSS<73>	VSS<10>	V28
G9	VSS<72>	VSS<9>	V33
H1	VSS<71>	VSS<8>	W1
H3	VSS<70>	VSS<7>	W10
H39	VSS<69>	VSS<6>	W3
L1	VSS<68>	VSS<5>	W37
L11	VSS<67>	VSS<4>	W39
D1	VSS<66>	VSS<3>	W6
C1	VSS<65>	VSS<2>	Y10
L3	VSS<64>	VSS<1>	Y33
L37	VSS<63>	VSS<0>	Y6
L7	VSS<62>		
M16	VSS<61>	VSS<253>	T9
M17	VSS<60>	VSS<255>	M23
M22	VSS<59>	VSS<254>	U30
AB25	VSS<58>		
M26	VSS<57>		
M29	VSS<56>		

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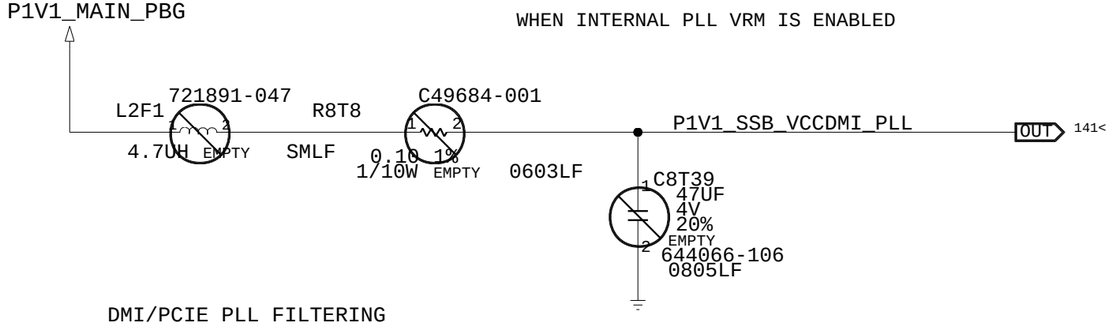
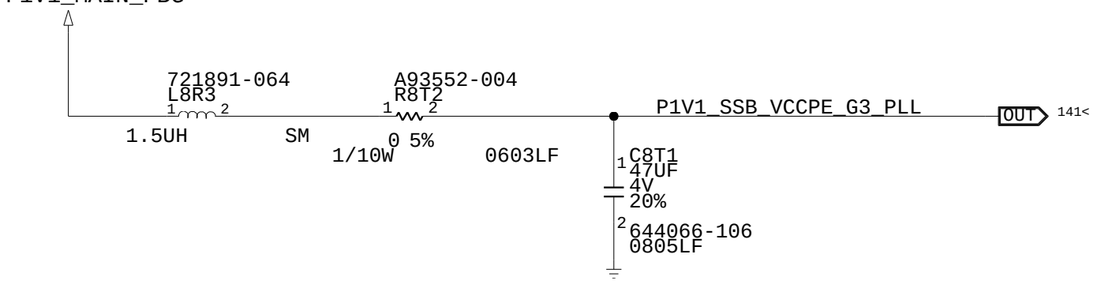
NOTE: THESE COMPONETNS SHOULD BE DNS
WHEN INTERNAL PLL VRM IS ENABLED

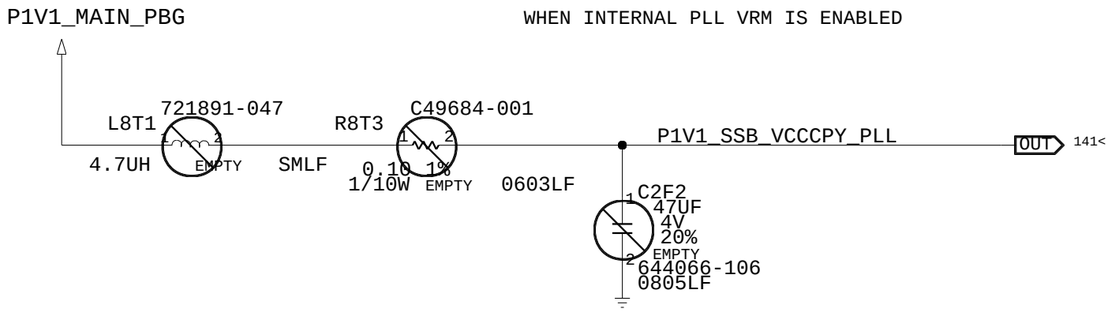


DMI/PCIE PLL FILTERING

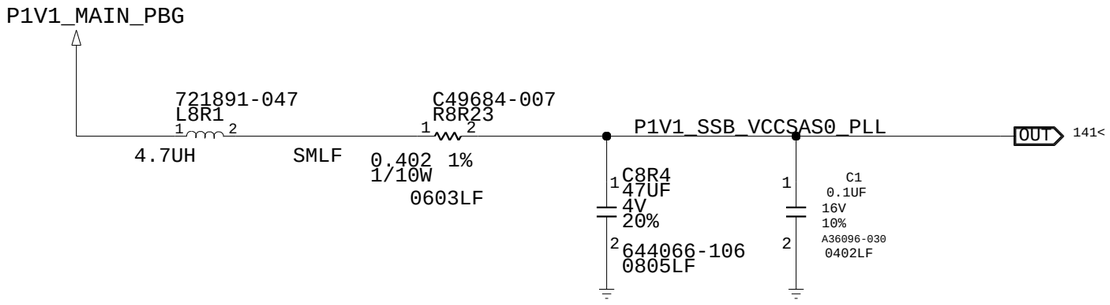


PCIE G3 PLL FILTERING

NOTE: THESE COMPONETNS SHOULD BE DNS
WHEN INTERNAL PLL VRM IS ENABLED

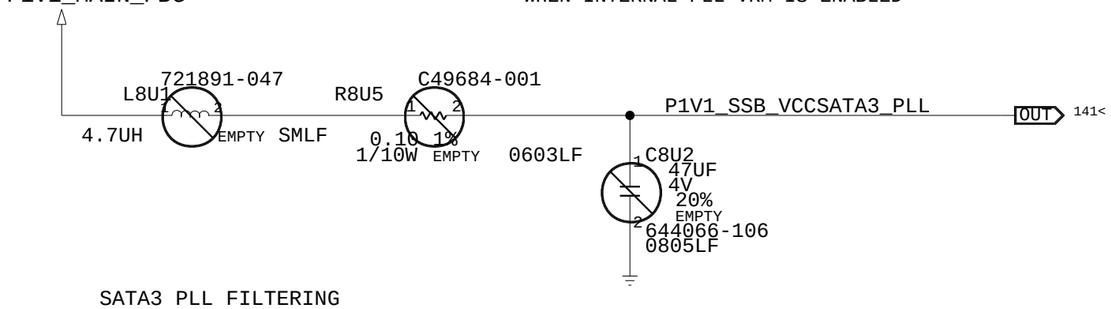


CPY PLL FILTERING

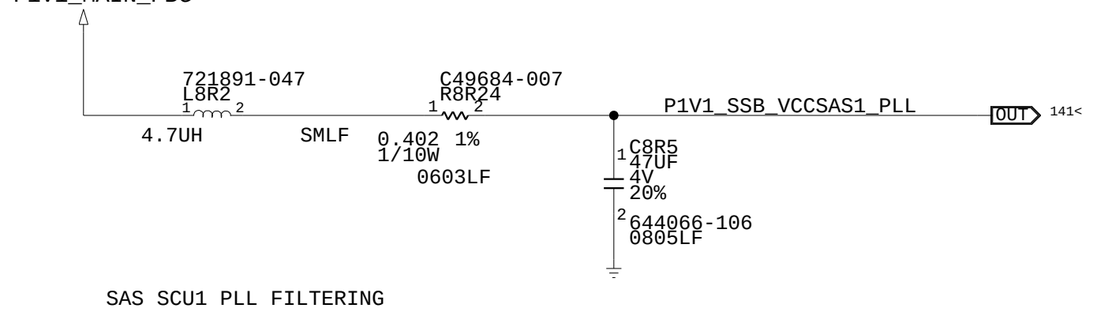


SAS SCU0 PLL FILTERING

NOTE: THESE COMPONETNS SHOULD BE DNS
WHEN INTERNAL PLL VRM IS ENABLED



SATA3 PLL FILTERING



SAS SCU1 PLL FILTERING

ROOM SB

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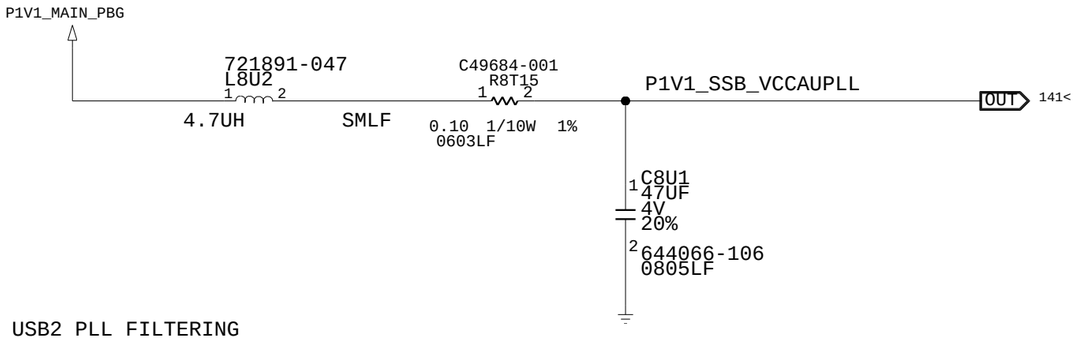
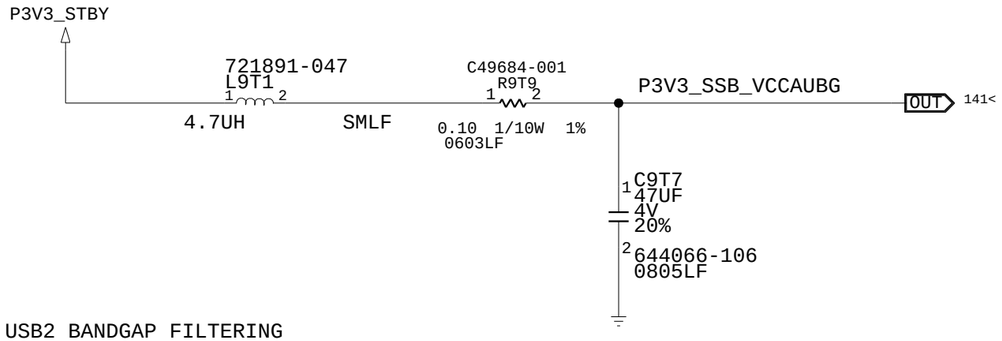
PATSBURG FILTERING 1-2

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 MISSION COLLEGE BLVD. P.O. BOX 58119 SANTA CLARA, CA 95052-8119	B	34649	444359 1.0	
		SCALE:	DO NOT SCALE DRAWING	SHEET 143 OF 303	

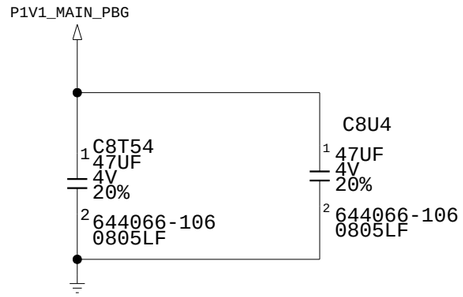
INTEL CONFIDENTIAL



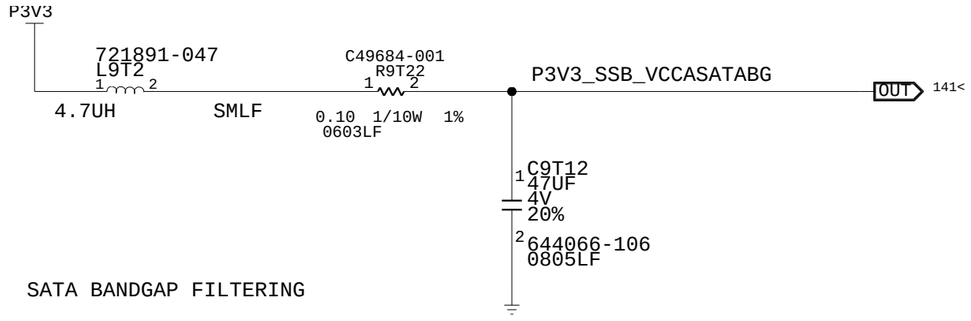
USB2 PLL FILTERING



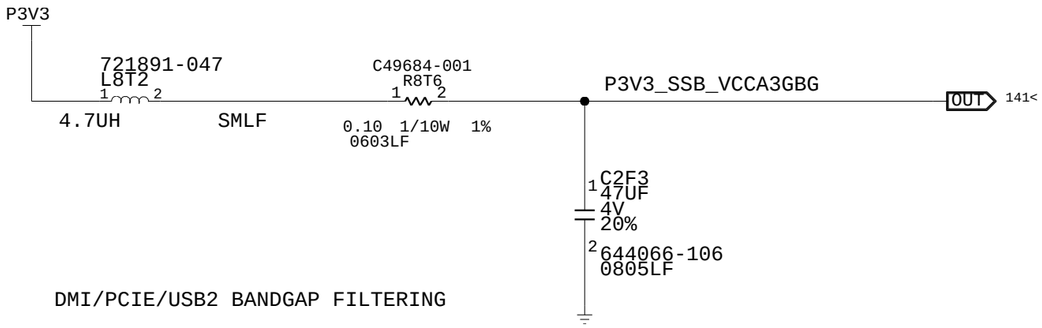
USB2 BANDGAP FILTERING



SATA PLL FILTERING



SATA BANDGAP FILTERING



DMI/PCIE/USB2 BANDGAP FILTERING

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ROOM SB

PATSBURG FILTERING 2-2

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 144 OF 303	

INTEL CONFIDENTIAL

ROOM = SSB_DECOUPLING

P1V1_MAIN_PBG

C8T46 22UF 6.3V 20% — 644066-041 0805LF
C8T19 1.0UF 6.3V 10% — A36096-027 0402LF
C8T25 1.0UF 6.3V 10% — A36096-027 0402LF

CAD NOTE: PLACE 1.0UF CAP UNDERNEATH PACKAGE NEAR PIN Y9
CAD NOTE: PLACE 1.0UF CAP UNDERNEATH PACKAGE NEAR PIN AC9
CAD NOTE: PLACE 22UF CAP AT PACKAGE EDGE NEAR PIN W11

P1V05_VTT_CPU0

C8U8 22UF 6.3V 20% — 644066-041 0805LF

CAD NOTE: PLACE CAP NEAR PIN L15

P1V1_MAIN_PBG

C8T33 1.0UF 6.3V 10% — A36096-027 0402LF
C8T34 1.0UF 6.3V 10% — A36096-027 0402LF

CAD NOTE: PLACE ONE CAP UNDERNEATH PACKAGE NEAR PIN N24
CAD NOTE: PLACE ONE CAP UNDERNEATH PACKAGE NEAR PIN N23

SATA G2

P1V1_MAIN_PBG

C8T38 1.0UF 6.3V 10% — A36096-027 0402LF
C8T43 1.0UF 6.3V 10% — A36096-027 0402LF

CAD NOTE: PLACE ONE CAP UNDERNEATH PACKAGE NEAR PIN M19
CAD NOTE: PLACE ONE CAP UNDERNEATH PACKAGE NEAR PIN L19

SATA G3

PCIE/DMI

P1V1_STBY_PBG

C2G1 47UF 4V 20% — 644066-106 0805LF
C8U3 47UF 4V 20% — 644066-106 0805LF
C8T53 22UF 6.3V 20% — 644066-041 0805LF
C8T21 2.2UF 6.3V 20% — A36096-088 0402LF
C8T28 2.2UF 6.3V 20% — A36096-088 0402LF

CAD NOTE: PLACE 1.0UF CAP UNDERNEATH PACKAGE NEAR PIN AC25
CAD NOTE: PLACE 1.0UF CAP UNDERNEATH PACKAGE NEAR PIN U22
CAD NOTE: PLACE 22UF CAP AT PACKAGE EDGE NEAR PIN T24

ASW

SATA

P1V1_MAIN_PBG

C8T27 2.2UF 6.3V 20% — A36096-088 0402LF
C8T24 2.2UF 6.3V 20% — A36096-088 0402LF

CAD NOTE: PLACE ONE 2.2UF CAP AT PACKAGE EDGE NEAR PIN Y28
CAD NOTE: PLACE ONE 2.2UF CAP AT PACKAGE EDGE NEAR PIN Y26

P5V_STBY

C8T36 1.0UF 6.3V 10% — A36096-027 0402LF

CAD NOTE: PLACE 1.0UF CAP
AT PACKAGE EDGE NEAR PIN U28

P3V3_STBY

C8T23 1.0UF 6.3V 10% — A36096-027 0402LF
C8T45 1.0UF 6.3V 10% — A36096-027 0402LF

CAD NOTE: PLACE ONE 1.0UF CAP UNDERNEATH PACKAGE NEAR PIN W28
CAD NOTE: PLACE ONE 1.0UF CAP AT PACKAGE EDGE NEAR PIN W26

USB

P1V5_MAIN_PBG

C8T3 10UF 6.3V 10% 0805LF 644066-037

CAD NOTE: PLACE CAP AT
PACKAGE EDGE NEAR PIN AJ22

PLL INT VRM

P3V3_STBY

C8T29 1.0UF 6.3V 10% — A36096-027 0402LF
C8T35 1.0UF 6.3V 10% — A36096-027 0402LF

CAD NOTE: PLACE ONE CAP UNDERNEATH PACKAGE NEAR PIN N28
CAD NOTE: PLACE ONE CAP UNDERNEATH PACKAGE NEAR PIN W25

AUDIO/GPIO

P5V

C8T16 1.0UF 6.3V 10% — A36096-027 0402LF

CAD NOTE: PLACE CAP UNDERNEATH
PACKAGE NEAR PIN AD29

P3V3

C8T14 1.0UF 6.3V 10% — A36096-027 0402LF
C8T9 1.0UF 6.3V 10% — A36096-027 0402LF
C8T11 1.0UF 6.3V 10% — A36096-027 0402LF

CAD NOTE: PLACE ONE CAP UNDERNEATH PACKAGE NEAR PIN AC29
CAD NOTE: PLACE ONE CAP UNDERNEATH PACKAGE NEAR PIN AC29
CAD NOTE: PLACE ONE CAP UNDERNEATH PACKAGE NEAR PIN AC30

PCI/GPIIO/LPC

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PATSBURG DECOUPLING 1-2

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 145 OF 303	

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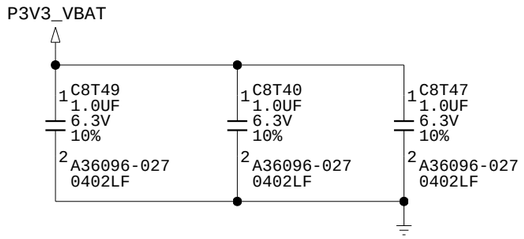
NOTE: PBG DECOUPLING ARE PLACEHOLDERS, EDA TO PROVIDE PBG SPECIFIC INFO AFTER DR 0.6

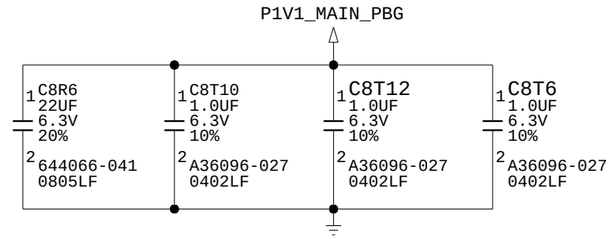
ROOM = SSB_DECOUPLING

RTC



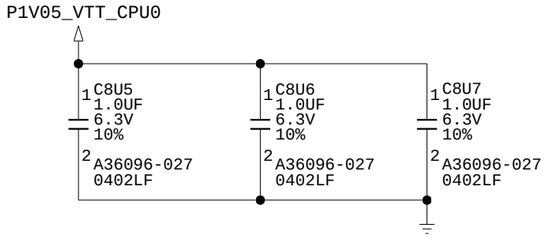
CAD NOTE: PLACE ONE CAP UNDERNEATH PACKAGE NEAR PIN L28
CAD NOTE: PLACE ONE CAP AT PACKAGE EDGE NEAR PIN L28
CAD NOTE: PLACE ONE CAP AT PACKAGE EDGE NEAR PIN L28

PCIE UPLINK



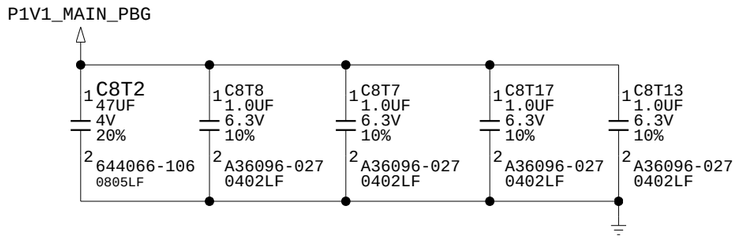
CAD NOTE: PLACE 22UF CAP AT PACKAGE EDGE NEAR PIN AJ15
CAD NOTE: PLACE ONE 1.0UF CAP UNDERNEATH PACKAGE NEAR PIN AJ15
CAD NOTE: PLACE ONE 1.0UF CAP UNDERNEATH PACKAGE NEAR PIN AJ16
CAD NOTE: PLACE ONE 1.0UF CAP UNDERNEATH PACKAGE NEAR PIN AH15

CPU



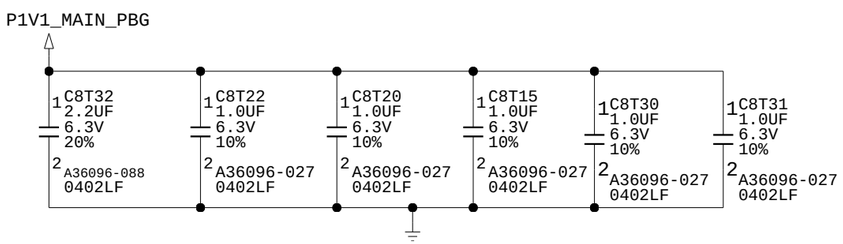
CAD NOTE: PLACE ONE CAP AT PACKAGE EDGE NEAR PIN L16
CAD NOTE: PLACE ONE CAP AT PACKAGE EDGE NEAR PIN L16
CAD NOTE: PLACE ONE CAP AT PACKAGE EDGE NEAR PIN L16

SAS

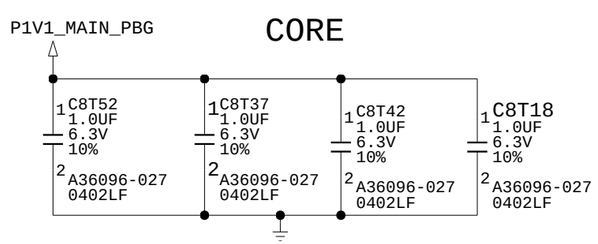


CAD NOTE: PLACE 22UF CAP AT PACKAGE EDGE NEAR PIN AJ25
CAD NOTE: PLACE ONE 1.0UF CAP UNDERNEATH PACKAGE NEAR PIN AJ25
CAD NOTE: PLACE ONE 1.0UF CAP UNDERNEATH PACKAGE NEAR PIN AJ28
CAD NOTE: PLACE ONE 1.0UF CAP UNDERNEATH PACKAGE NEAR PIN AF24
CAD NOTE: PLACE ONE 1.0UF CAP UNDERNEATH PACKAGE NEAR PIN AE24

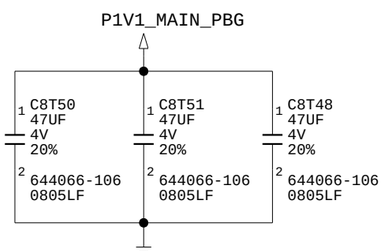
CORE



CAD NOTE: PLACE ONE CAP UNDERNEATH PACKAGE NEAR PIN AD16
CAD NOTE: PLACE ONE CAP UNDERNEATH PACKAGE NEAR PIN Y16
CAD NOTE: PLACE ONE CAP UNDERNEATH PACKAGE NEAR PIN N15
CAD NOTE: PLACE ONE CAP UNDERNEATH PACKAGE NEAR PIN T17
CAD NOTE: PLACE ONE CAP UNDERNEATH PACKAGE NEAR PIN Y20
CAD NOTE: PLACE ONE CAP UNDERNEATH PACKAGE NEAR PIN T20



CAD NOTE: PLACE ONE CAP UNDERNEATH PACKAGE NEAR PIN AC17
CAD NOTE: PLACE ONE CAP UNDERNEATH PACKAGE NEAR PIN N16
CAD NOTE: PLACE ONE CAP UNDERNEATH PACKAGE NEAR PIN J15
CAD NOTE: PLACE ONE CAP AT PACKAGE EDGE NEAR PIN J15



CAD NOTE: PLACE ONE CAP AT PACKAGE EDGE NEAR PIN T19
CAD NOTE: PLACE ONE CAP AT PACKAGE EDGE NEAR PIN T20
CAD NOTE: PLACE ONE CAP AT PACKAGE EDGE NEAR PIN N15

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PATSBURG DECOUPLING 2-2

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 146 OF 303	

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PATSBURG PULL UPS

CAD NOTE: PLACE SGPIO PULL UPS WITHIN 2'' FROM PBG

P3V3

R2E44	2.0K	1%	1/16W	SGPIO_SAS1_CLOCK	OUT	139>	149<
R2F5	2.0K	1%	1/16W	SGPIO_SAS1_LOAD	OUT	139>	149<
R2F2	2.0K	1%	1/16W	SGPIO_SAS1_DATAIN	OUT	139<	149<
R2F7	2.0K	1%	1/16W	SGPIO_SAS1_DATAOUT	OUT	139>	149<

A93548-138 0402LF

P3V3

R2G28	10.0K	1%	1/16W	PU_ROL_MODULE_PRES_N	OUT	168<	
R2G23	10.0K	1%	1/16W	PU_A20GATE	OUT	135<	
R2G21	10.0K	1%	1/16W	PU_SIO_KBRST_N	OUT	135<	
R1H11	10.0K	1%	1/16W	IRQ_SSB_SCI_WHEA_N	OUT	168<	
R2G26	10.0K	1%	1/16W	IRQ_SERIAL	OUT	138<>	156> 156< 175<>
R1F15	10.0K	1%	1/16W	FM_IBMC_SSB_SMI_LPC_N	OUT	138<	175>
R2G29	10.0K	1%	1/16W	PU_SSB_PS_PWROK_LVC3	OUT	168<	
R2G24	10.0K	1%	1/16W	FM_MULTIPLE_PCI_MASTER_N	OUT	136>	
R2E33	4.7K	1%	1/16W	PU_SMB_SAS_BBU_DATA2	OUT	139<>	
R2E41	4.7K	1%	1/16W	PU_SMB_SAS_BBU_CLK2	OUT	139>	
R2E27	10.0K	1%	1/16W	FM_ERR1_DLY_CO_N	OUT	138<	169>

A93548-034 0402LF (R2G28, R2G23, R2G21, R1H11, R2G26, R1F15, R2G29, R2G24)
A93548-517 0402LF (R2E33, R2E41)
A93548-034 0402LF (R2E27)

P3V3_STBY

R1F20	3.01K	1%	1/16W	FM_MFG_MODE_FLSH_SEC_OVRD	OUT	135<	149>

A93548-024 0402LF EMPTY

FLASH DESCRIPTOR SECURITY OVERRIDE WHEN HIGH
NOTE: MANUFACTURING JUMPER ALSO CAN BE USED TO SET THIS STRAP

P3V3_STBY

R2G30	10.0K	1%	1/16W	PU_USB_OC6_N	OUT	168<	
R2G31	10.0K	1%	1/16W	PU_USB_OC7_N	OUT	168<	
R1F31	10.0K	1%	1/16W	PU_RI_N	OUT	135<	
R1F33	10.0K	1%	1/16W	PWRGD_PCH_DRAMPWRGD_CO	OUT	135>	169<
R2F14	2.21K	1%	1/16W	PU_FM_PBG_DYN_SKU_KEY	OUT	136<	
R2G10	10.0K	1%	1/16W	PU_SMB_ALERT_N	OUT	139<	
R2E28	10.0K	1%	1/16W	FM_SSB_IBMC_THERMTRIP_N	OUT	139>	176<
R2E26	10.0K	1%	1/16W	FM_IBMC_SSB_SCI_LPC_N	OUT	136<	177<

A93548-034 0402LF (R2G30, R2G31, R1F31, R1F33, R2F14, R2G10, R2E28, R2E26)

R1F35	10.0K	1%	1/16W	PWRGD_PCH_APWROK_LVC3	OUT	135<	168< 169>
R1F18	10.0K	1%	1/16W	PWRGD_PCH_PWROK_LVC3	OUT	135<	169> 177< 204< 219> 219<
R2G18	10.0K	1%	1/16W	PWRGD_PCH_SYS_PWROK_LVC3	OUT	129<	135< 169>

A93548-034 0402LF (R1F35, R1F18, R2G18)

P3V3_STBY

R2E29	3.01K	1%	1/16W	PU_VRM_VOLTAGE_SELECT	OUT	135<	

A93548-024 0402LF

PLL ODVR INPUT FROM 1.5V WHEN HIGH
EMPTY FOR ODVR INPUT FROM 1.8V

P3V3_STBY

R2G9 1K 1% 1/16W PU_NV_CLE OUT 137>
A93548-023 0402LF

DMI VCC TERMINATED WHEN HIGH, VSS TERMINATED WHEN EMPTY

135< 128< 129< 148< 169< IN RST_PCH_PLTRST_LVC3_N

U2E3
C99406-001
NC7SB3157

R8R20 1K 1% 1/16W PD_DMI_ACMODE
A93548-023 0402LF

151> IN SGPIO_GSX_DIN

P3V3

SMLF

S, B0, B1, VCC, GND, A

A SGPIO_GSX_MUX_DIN OUT 138<

DMI AC MODE WHEN 'B0' INPUT SAMPLED LOW

PATSBURG STRAP SETTINGS

P3V3

R2G22 3.01K 1% 1/16W SPEAKER_SSB OUT 135> 191<
A93548-024 0402LF

REBOOT DISABLE WHEN HIGH

R2G19 1K 1% 1/16W IRQ_INIT3_3V_N OUT 135>
A93548-023 0402LF

CPU INTERFACE BUFFER, STRONGER WHEN LOW

R2E30 1K 1% 1/16W PU_SGPIO_GSX_DOUT OUT 138<
A93548-023 0402LF

R2G32 1K 1% 1/16W FM_BIOS_SPI_WP_N OUT 152< 168<
A93548-023 0402LF

BOOT BIOS STRAPS (BBS)

GNT[1]_GSXDOUT BBS[1]	SATA1GP_GP19 BBS[0]	
0	0	LPC
0	1	NAND
1	0	PCI
1	1	SPI

NOTE: BALLS HAVE AN INTERNAL WEAK PULL-UP DEFAULT DESTINATION IS SPI

P3V3_VBAT

R1F25 390K 5% 1/16W
A93549-100 0402LF

R1F22 390K 5% 1/16W
A93549-100 0402LF

PU_1V1_DSW_ODVR_EN OUT 135<
PU_1V1_SUS_ODVR_EN OUT 135<

PU (DEFAULT)	DSW/SUS INTERNAL VR MODE

R2G25 1K 1% 1/16W PD_SSB_GP28 OUT 155> 168<
A93548-023 0402LF

PLL ON-DIE VR DISABLE WHEN LOW, ENABLE WHEN EMPTY

NOTE: PAGE 2-2 IS IN P157

PATSBURG STRAPS/PULL-UPS 1-2

ROOM = PBG_PU_STRAPS

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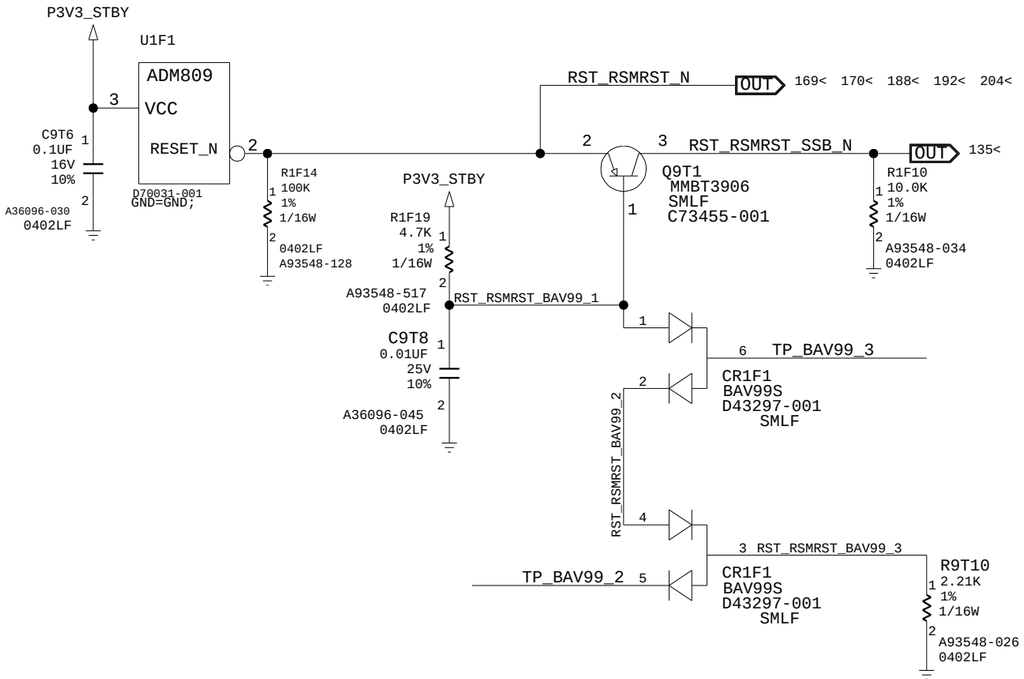
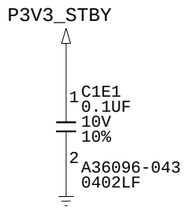
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 147 OF 303	

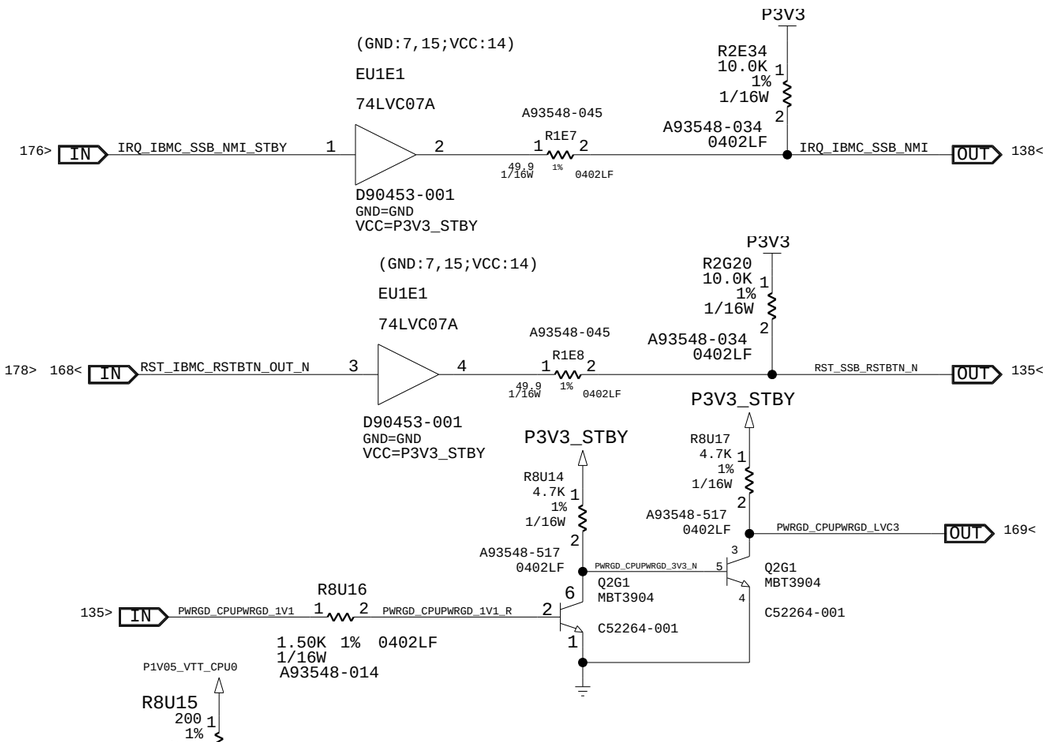
INTEL CONFIDENTIAL

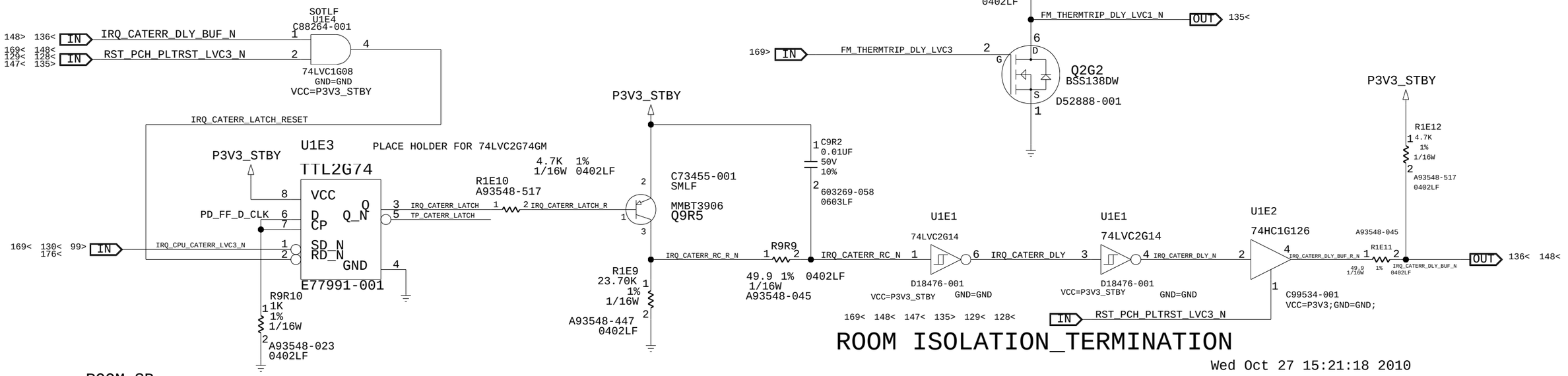
RTC POWER-WELL ISOLATION





**NOTE: PLTRST DELAY HAS BEEN ADDED BY CPLD.
**NOTE: THERMTRIP DELAY HAS BEEN ADDED BY CPLD.





ROOM ISOLATION_TERMINATION

Wed Oct 27 15:21:18 2010

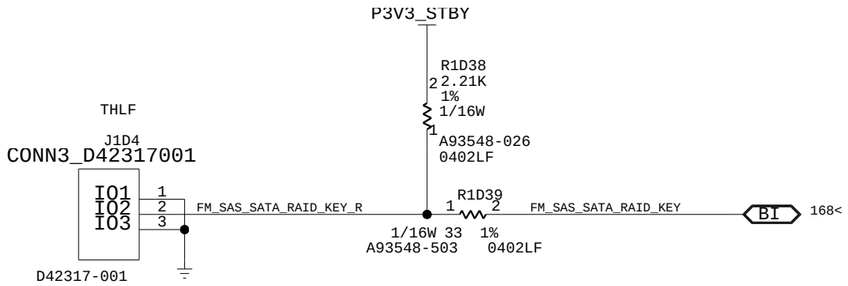
ROOM SB

PATSBURG ISOLATION/TERMINATION

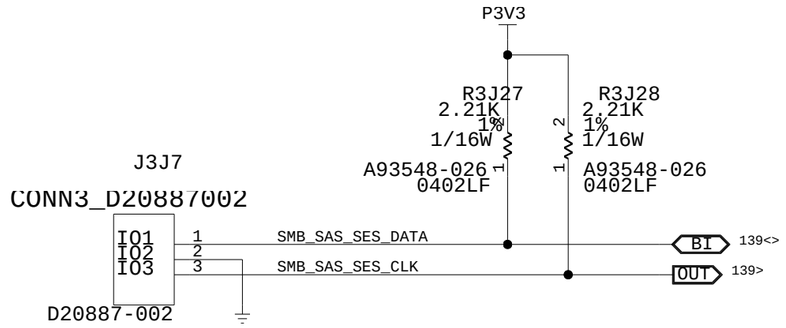
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 148 OF 303	

INTEL CONFIDENTIAL

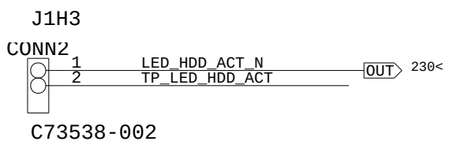
SAS/SATA RAID KEY



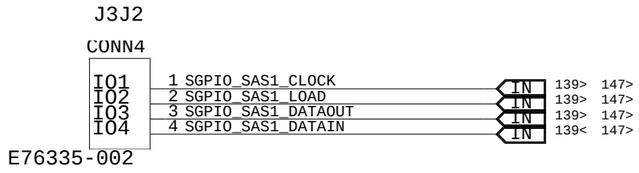
SAS SES



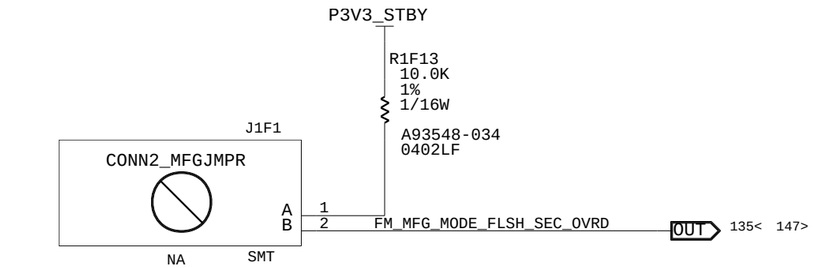
HDD ACTIVITY JUMPER



SAS SGPIO



MANUFACTURING MODE JUMPER



ROOM = PBG_HEADERS

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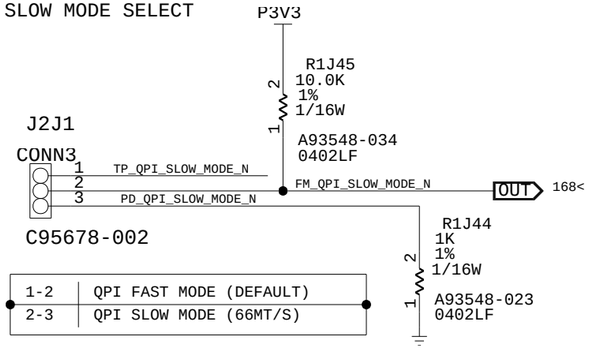
PATSBURG HEADERS 1-2

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 149 OF 303	

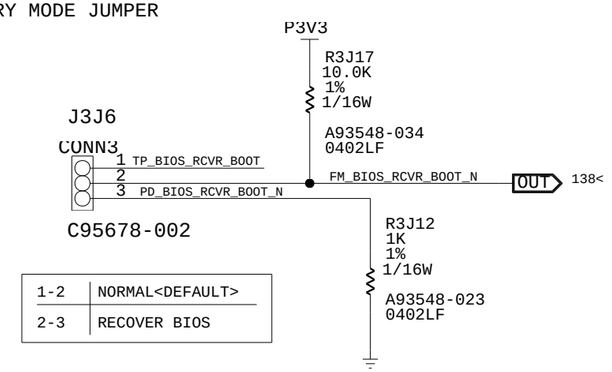
INTEL CONFIDENTIAL

QPI SLOW MODE SELECT



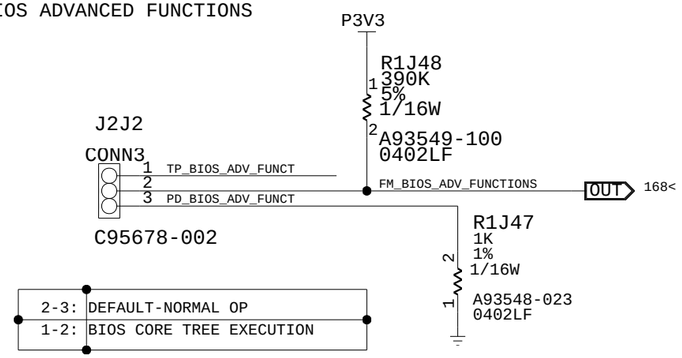
APD DE NOTE: ADD IPN 634479-007 AS JUMPER TO BOM

BIOS RECOVERY MODE JUMPER



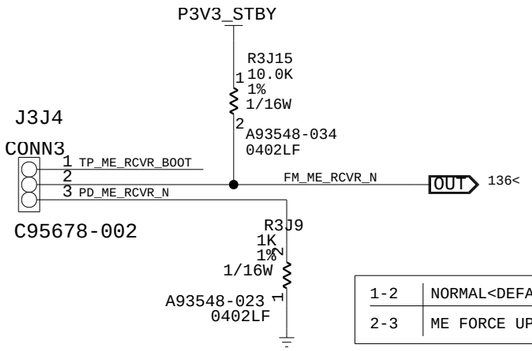
APD DE NOTE: ADD IPN 634479-007 AS JUMPER TO BOM

BIOS ADVANCED FUNCTIONS



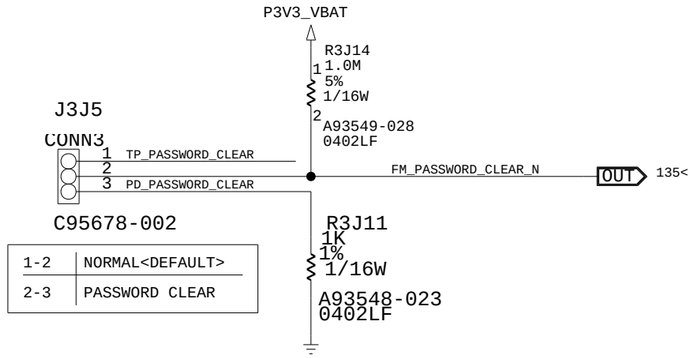
APD DE NOTE: ADD IPN 634479-007 AS JUMPER TO BOM

ME FIRMWARE UPDATE



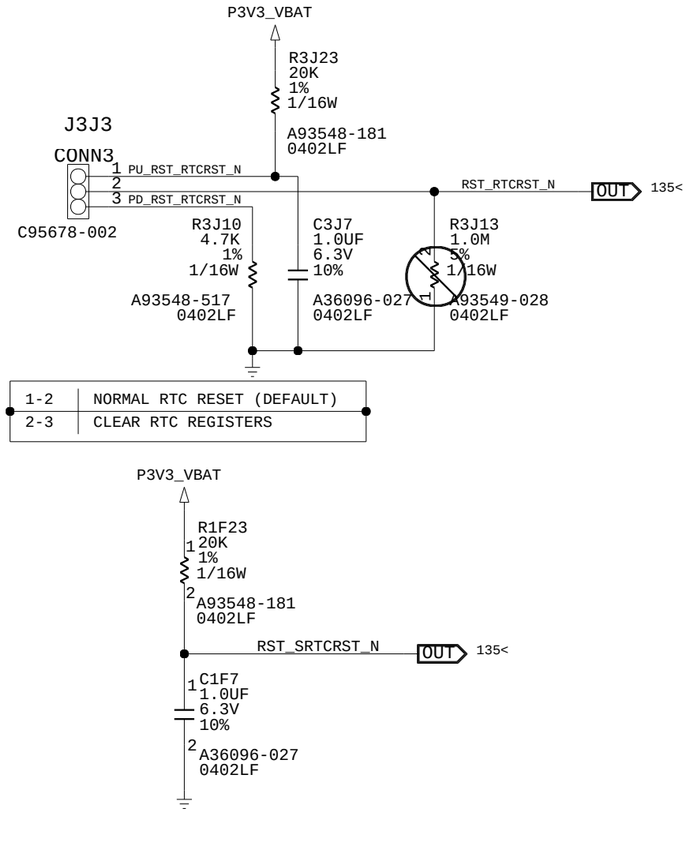
APD DE NOTE: ADD IPN 634479-007 AS JUMPER TO BOM

PASSWORD CLEAR JUMPER



APD DE NOTE: ADD IPN 634479-007 AS JUMPER TO BOM

CMOS CLEAR JUMPER



APD DE NOTE: ADD IPN 634479-007 AS JUMPER TO BOM

ROOM = PBG_HEADERS_BIOS

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PATSBURG HEADERS 2-2

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 150 OF 303	

INTEL CONFIDENTIAL

ROOM = SSB_GSX

P3V3

R1E13 10.0K 1% 1/16W A93548-034 0402LF

R1E14 10.0K 1% 1/16W A93548-034 0402LF

R9R11 1K 1% 1/16W A93548-023 0402LF

PU_EXTERNAL_BMC_CARD_N
PU_BOARD_REV1

GSX EXPANDER 2
EU1E2
74LV165A

TTL165

CAD NOTE: PLACE 33OHMS RES WITHIN 1" FROM 74LV165A

R1E17 33.2 1% 1/16W A93548-001 0402LF

A			
B			
C			
D			
E			
F			
G			
H			
QH	9	SGPIO_GSX_2_QH_R	SGPIO_GSX_2_QH OUT 151<
QH_N	7	TP_SGPIO_GSX_2_QH_N	
SER	10	PD_SGPIO_GSX_2_SER	
SH/LD_N	1	SGPIO_GSX_LOAD	151< 138> IN
CLK	2	SGPIO_GSX_CLK	151< 138> IN
CLK_INH	15	PD_SGPIO_GSX_2_CLK_INH	
TH	17		

R1E15 1K 1% 1/16W A93548-023 0402LF

R1E18 1K 1% 1/16W A93548-023 0402LF

D88985-001
VCC=P3V3; GND=GND;

P3V3

C9R3 1.0UF 6.3V 10% A36096-027 0402LF

C9R4 0.01UF 25V 10% A36096-045 0402LF

P3V3

R2E5 10.0K 1% 1/16W A93548-034 0402LF

R2E15 10.0K 1% 1/16W A93548-034 0402LF

R2E14 10.0K 1% 1/16W A93548-034 0402LF

R2E13 10.0K 1% 1/16W A93548-034 0402LF

R2E12 10.0K 1% 1/16W A93548-034 0402LF

R8R12 1K 1% 1/16W A93548-023 0402LF

R8R14 1K 1% 1/16W A93548-023 0402LF

R8R15 1K 1% 1/16W A93548-023 0402LF

R8R16 1K 1% 1/16W A93548-023 0402LF

R8R17 1K 1% 1/16W A93548-023 0402LF

GSX EXPANDER 1
EU2E2
74LV165A

TTL165

CAD NOTE: PLACE 33OHMS RES WITHIN 1" FROM 74LV165A

R1E16 22.1 1% 1/16W A93548-054 0402LF

A			
B			
C			
D			
E			
F			
G			
H			
QH	9	SGPIO_GSX_DIN_R	SGPIO_GSX_DIN OUT 147<
QH_N	7	TP_SGPIO_GSX_1_QH_N	
SER	10	SGPIO_GSX_2_QH	151> IN
SH/LD_N	1	SGPIO_GSX_LOAD	151< 138> IN
CLK	2	SGPIO_GSX_CLK	151< 138> IN
CLK_INH	15	PD_SGPIO_GSX_1_CLK_INH	
TH	17		

PU_BOARD_REV0
PU_BOARD_ID3
PU_BOARD_ID2
PU_BOARD_ID1
PU_BOARD_ID0
FM_RISER_ID2 172> 171> IN
FM_RISER_ID1 172> 171> IN
FM_RISER_ID0 172> 171> IN

R2E11 1K 1% 1/16W A93548-023 0402LF

D88985-001
VCC=P3V3; GND=GND;

P3V3

C8R3 1.0UF 6.3V 10% A36096-027 0402LF

C8R2 0.01UF 25V 10% A36096-045 0402LF

BOARD ID SETTINGS

PLATFORM	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
POTTER CITY	0	1	0	1

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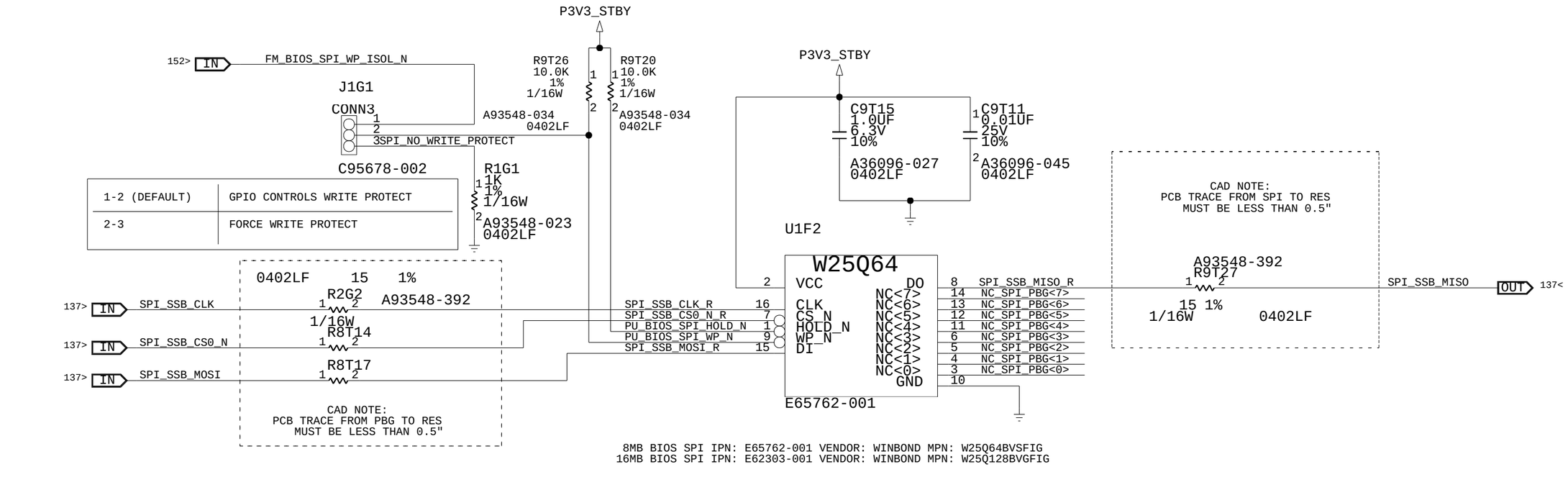
PATSBURG GSX

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 151 OF 303	

INTEL CONFIDENTIAL

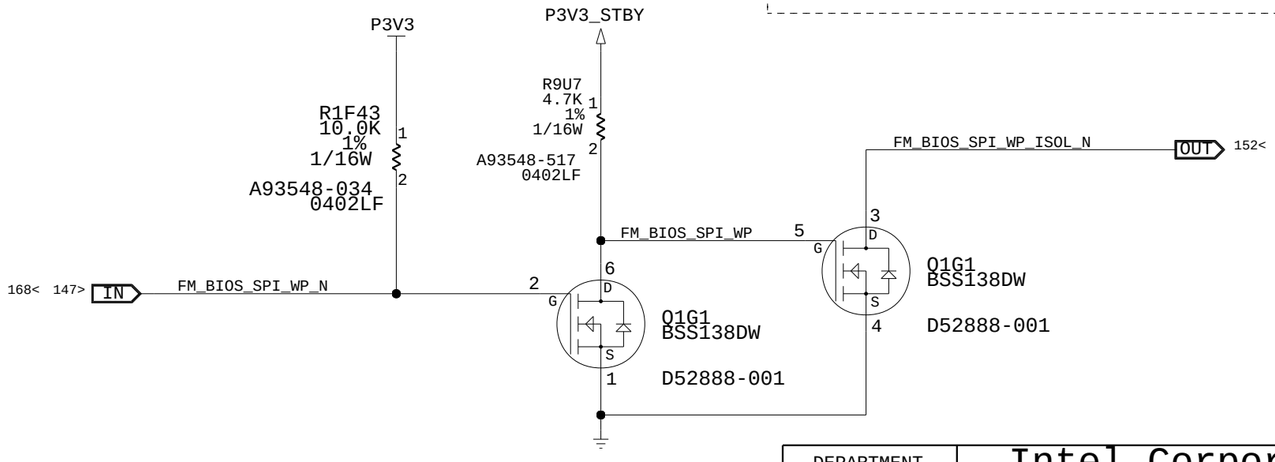
ROOM MIO_BIOS_MEM



8MB BIOS SPI IPN: E65762-001 VENDOR: WINBOND MPN: W25Q64BVSFIG
16MB BIOS SPI IPN: E62303-001 VENDOR: WINBOND MPN: W25Q128BVGFIG

CAD NOTE:
THIS PART WILL BE PLACE WITH SOCKET
USE ALT SYMBOL ASSOCIATED WITH SOCKET FOOTPRINT

BOM NOTE:
SOCKET IS D91187-001



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PATSBURG SPI FLASH

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 152 OF 303	

INTEL CONFIDENTIAL

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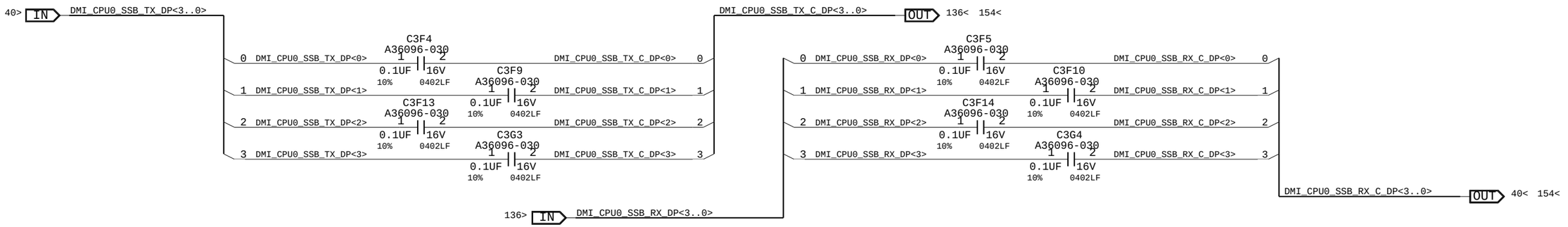
Wed Oct 27 14:54:04 2010

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 153 OF 303	

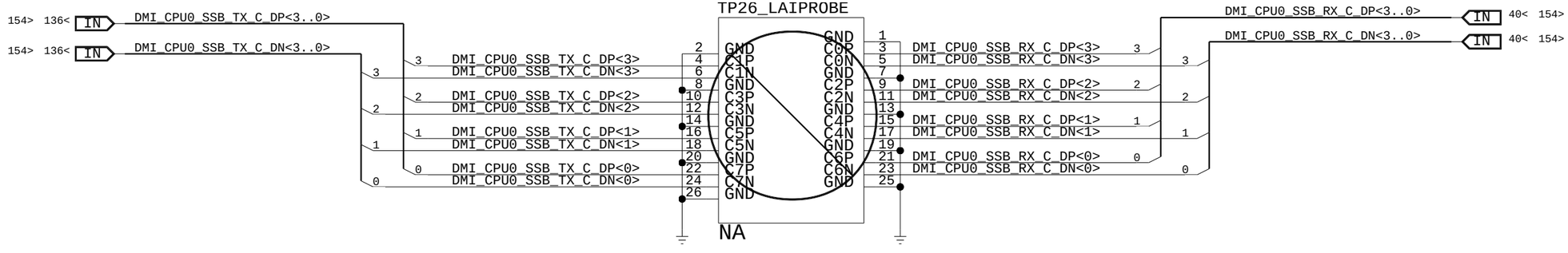
INTEL CONFIDENTIAL

DMI CAPS



TP3G1

TP26_LAIPROBE



NA

NOTE: DMI PORT LANE REVERSED IN MIDBUS SIDE

ROOM: PATSBURG DMI MIDBUS

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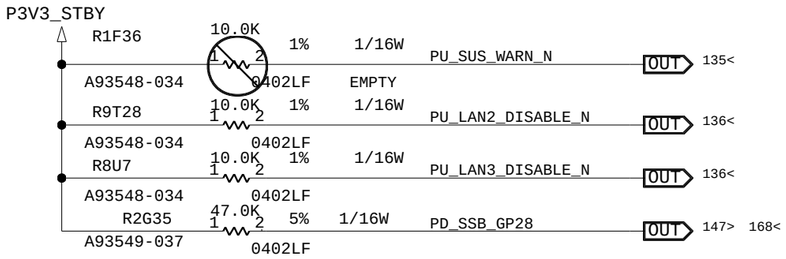
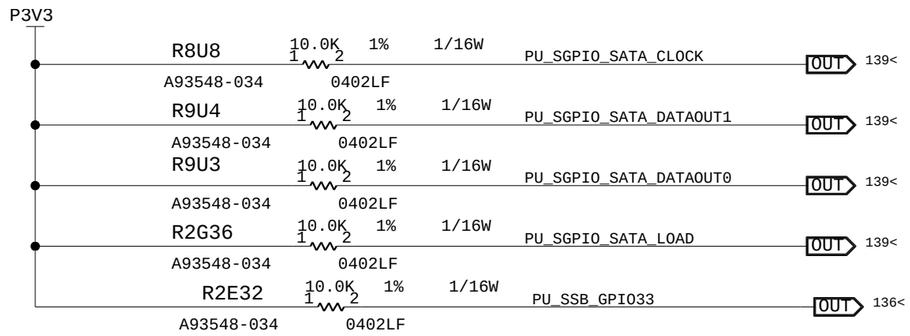
ESI AC BLOCKING & DMI MIDBUS 1-2

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 154 OF 303	

INTEL CONFIDENTIAL





ROOM PBG_PU_STRAPS

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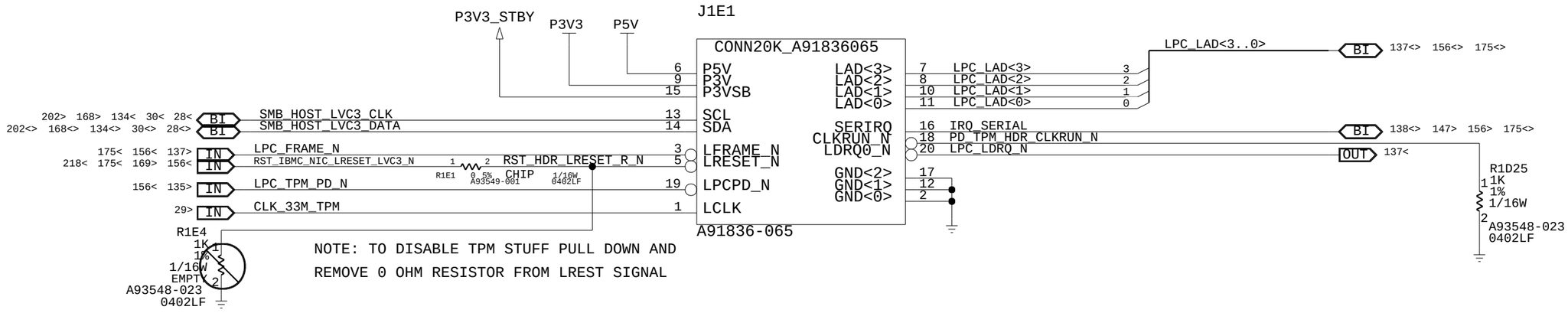
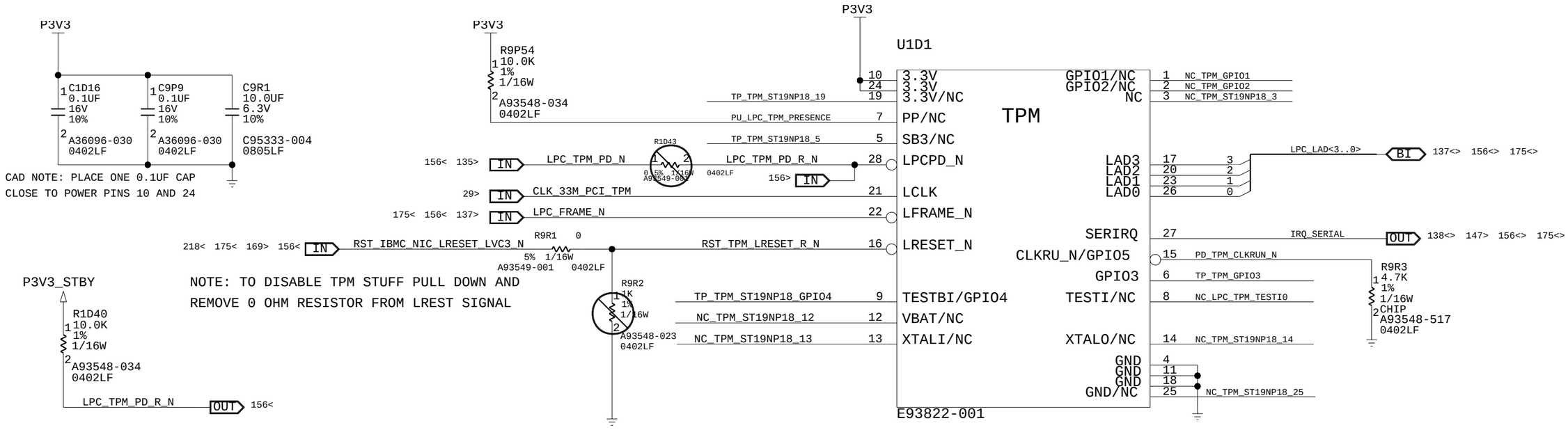
PATSBURG STRAPS/PULL-UPS 2-2

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 155 OF 303	

INTEL CONFIDENTIAL



***NOTE: ONBOARD TPM SUPPORTED: ST19NP18 ONLY



ROOM = MIO_SECURITY

TPM DEVICE/MODULE CONNECTOR

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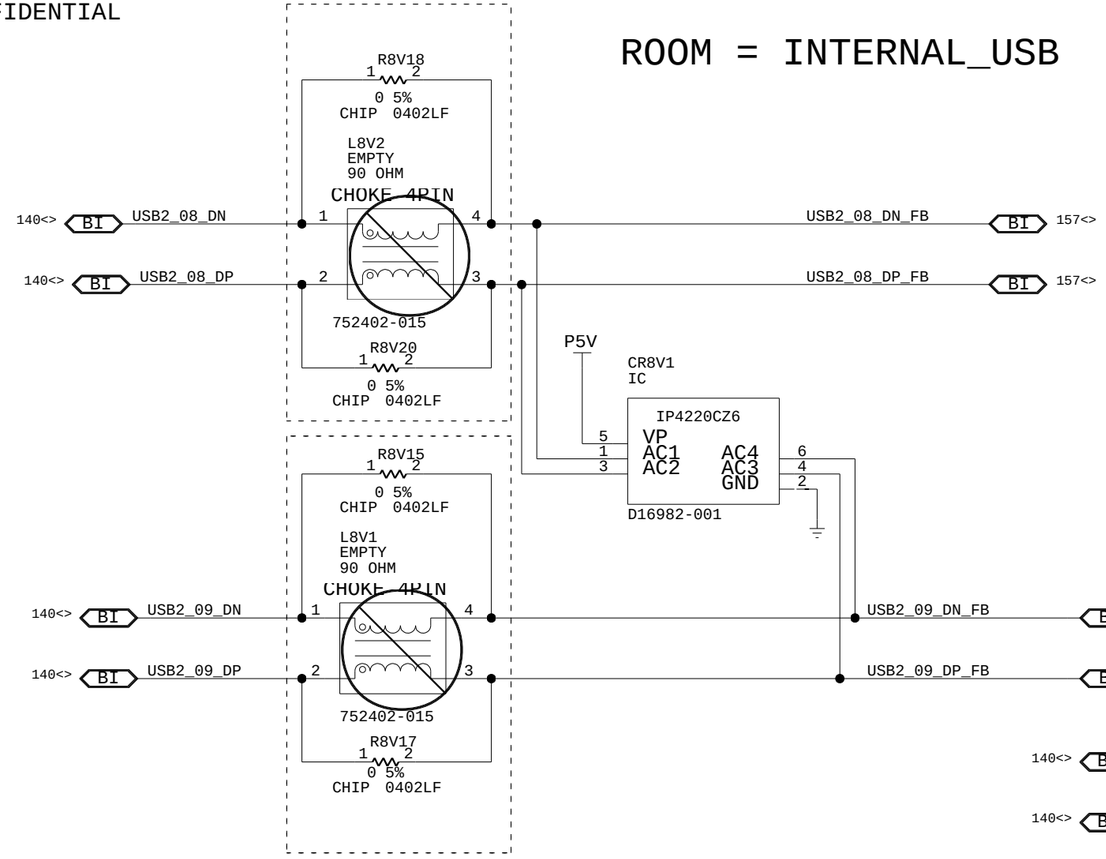
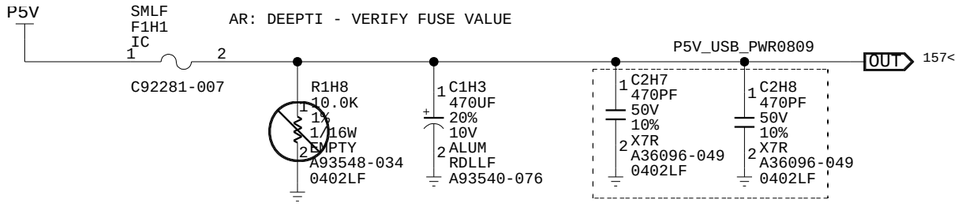
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 156 OF 303	

INTEL CONFIDENTIAL

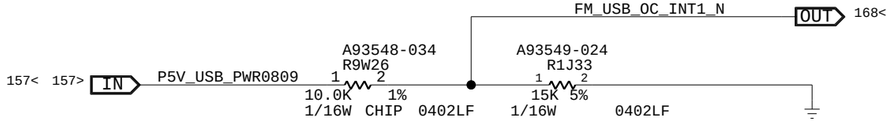
ROOM = INTERNAL_USB



DE NOTE: USE P5V_AUX IF BOARD NEEDS TO SUPPORT USB WAKE FROM S3/S4



CAD NOTE: PLACE AS CLOSE AS POSSIBLE TO USB CONNECTOR



J2H1
CONN10
C91088-002

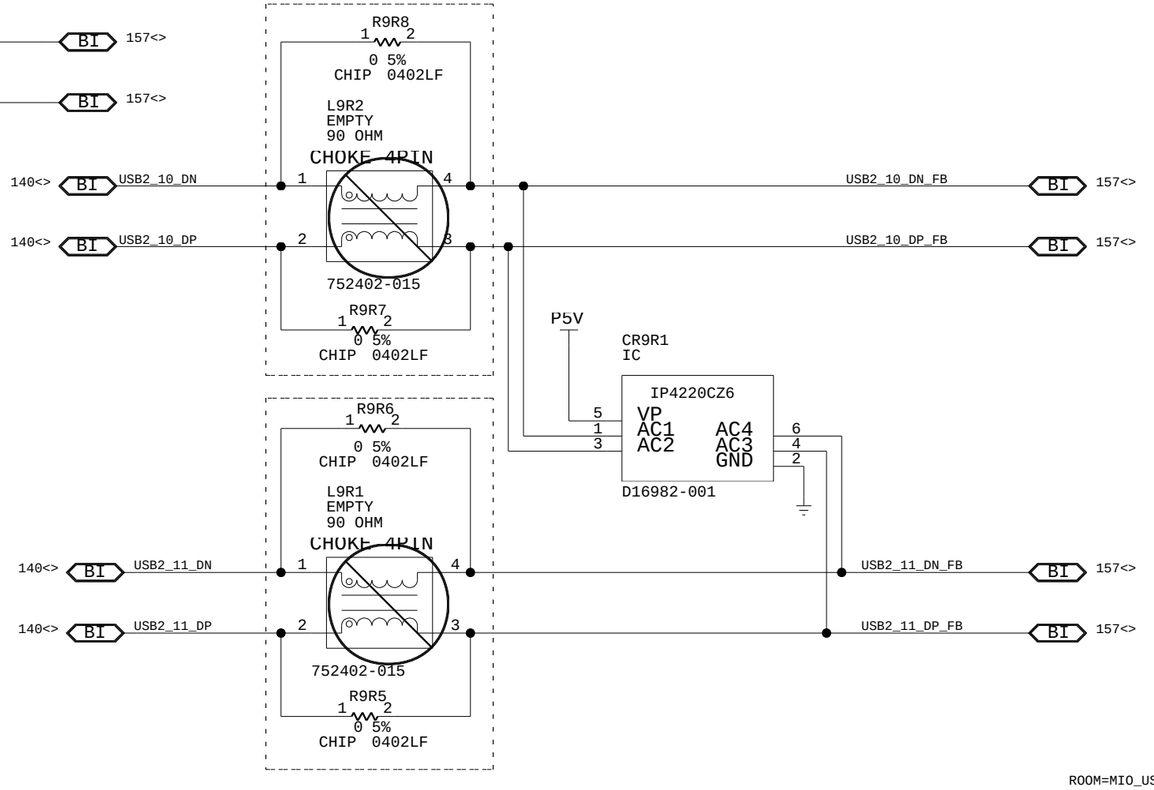
157< 157> IN P5V_USB_PWR0809 — P5V_USB_PWR0809 IN 157> 157<
157<> BI USB2_08_DN_FB — USB2_09_DN_FB BI 157<>
157<> BI USB2_08_DP_FB — USB2_09_DP_FB BI 157<>
TP_USB_ICH_NC

FOR INTERNAL TWO USB PORTS

J1E2
CONN10
C91088-002

158> 158< 157< IN P5V_USB_PWR1011 — P5V_USB_PWR1011 IN 157< 158< 158>
157<> BI USB2_10_DN_FB — USB2_11_DN_FB BI 157<>
157<> BI USB2_10_DP_FB — USB2_11_DP_FB BI 157<>
TP_USB_2_ICH_NC

FOR INTERNAL TWO USB PORTS



DE NOTE: USE P5V_AUX IF BOARD NEEDS TO SUPPORT USB WAKE FROM S3/S4

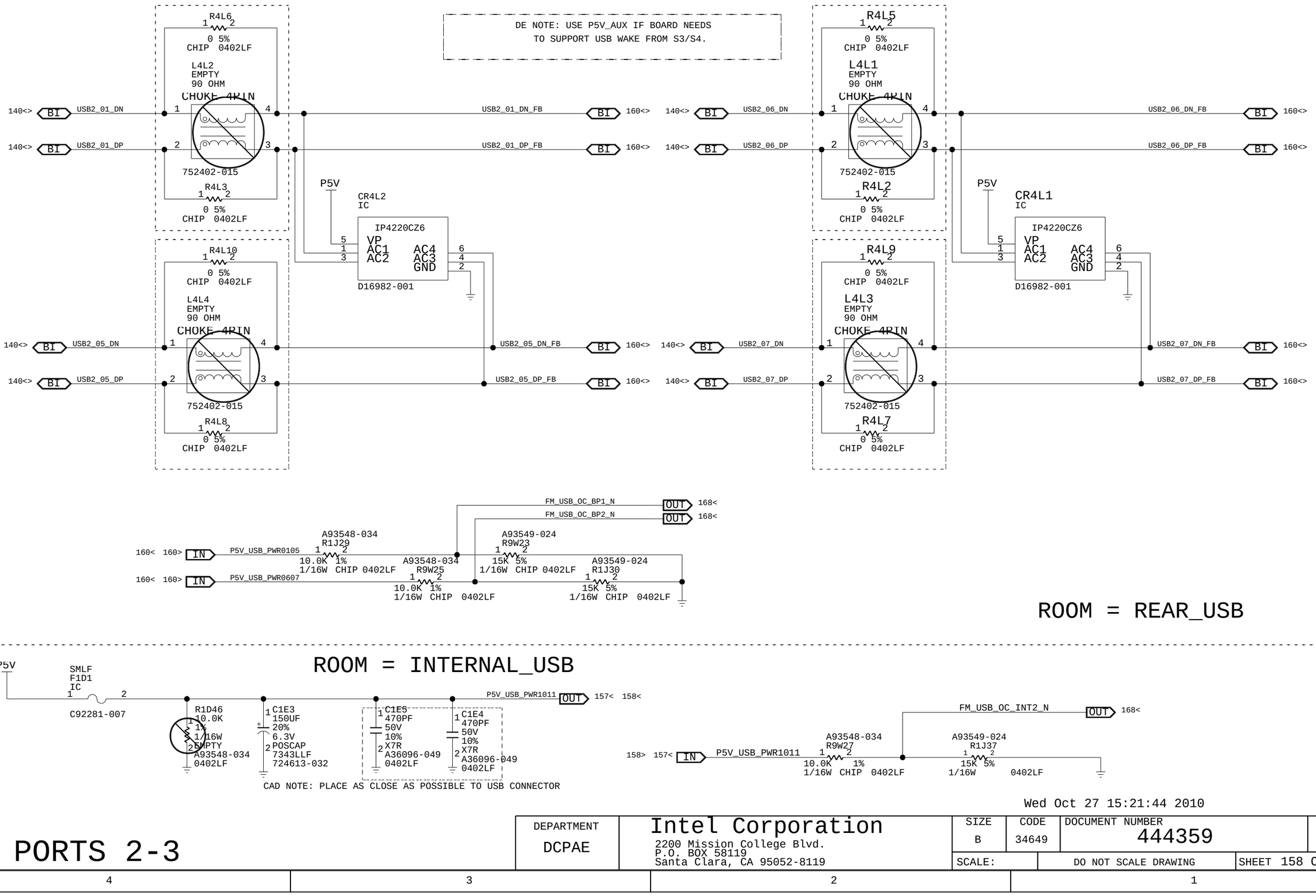
ROOM=MIO_USB

Wed Oct 27 15:21:43 2010

USB PORTS 1-3

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 157 OF 303	

INTEL CONFIDENTIAL



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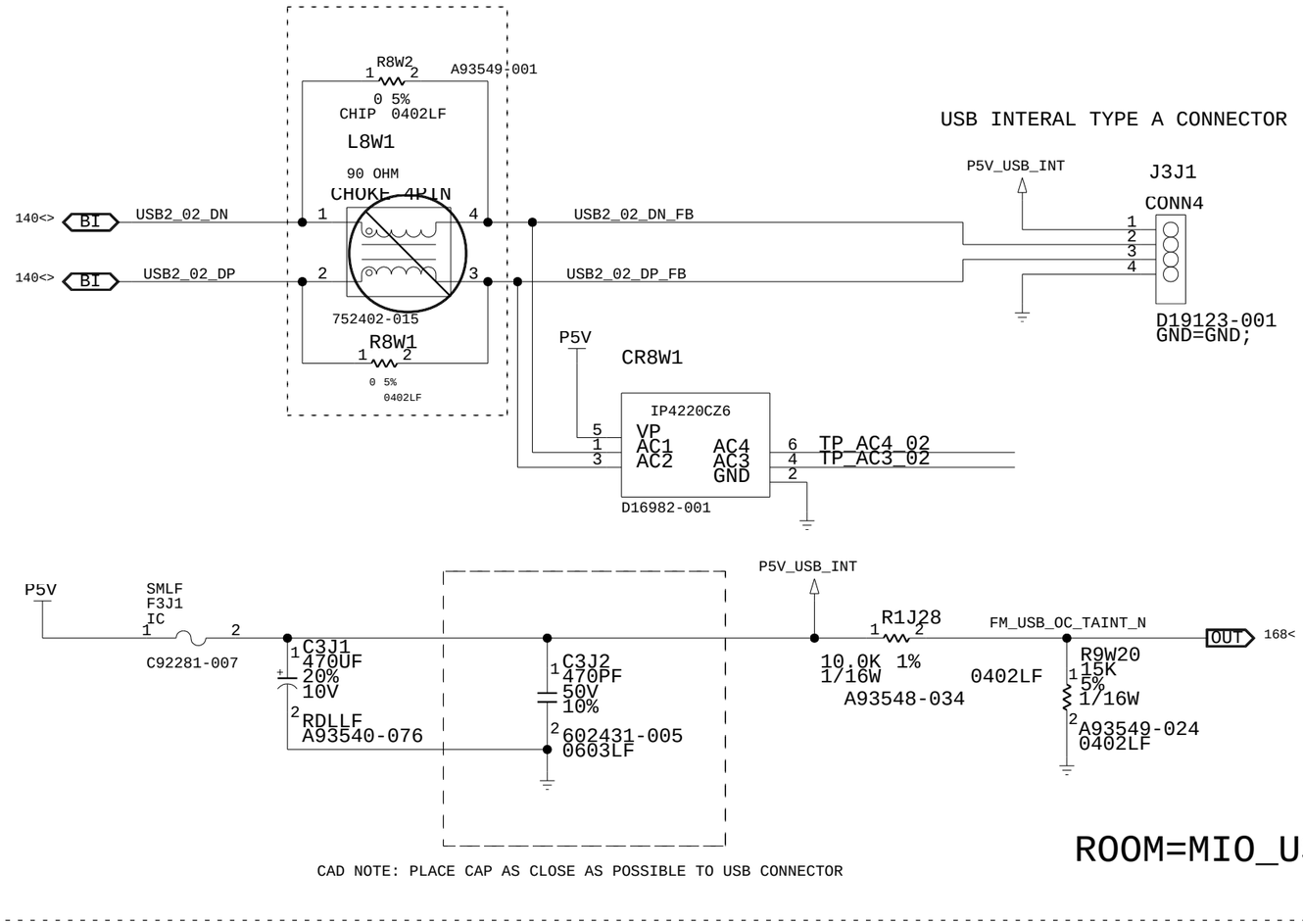
USB PORTS 2-3

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 158 OF 303

INTEL CONFIDENTIAL

TYPE-A INTERNAL USB



USB PORTS 3-3

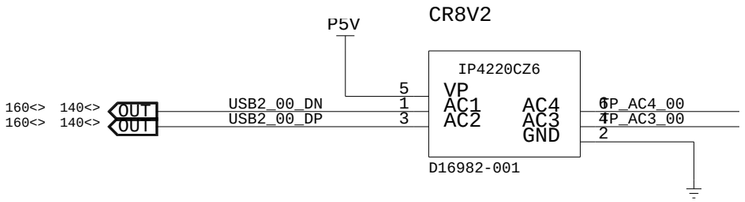
Wed Oct 27 15:21:44 2010

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 159 OF 303	

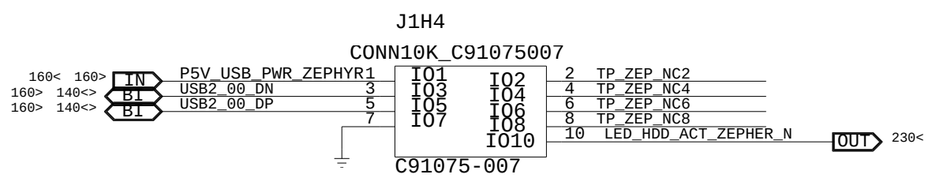
INTEL CONFIDENTIAL

ROOM=MIO_USB

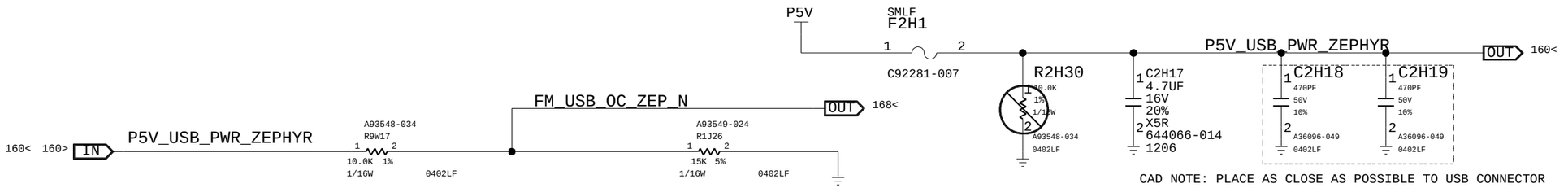
ZEPHER MODULE CONNECTOR:
LOW PROFILE CONNECTOR: C91075-007, 2MM PITCH
STANDARD CONNECTOR: C91088-001, 2.54MM PITCH



CAD NOTE: PLACE ESD CLOSE TO USB CONNECTOR (LESS THAN ONE INCH)

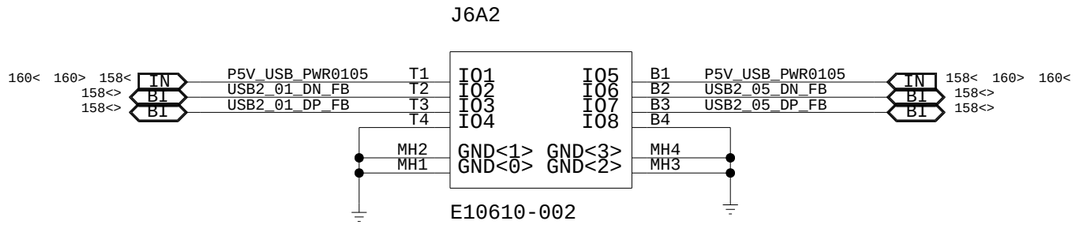


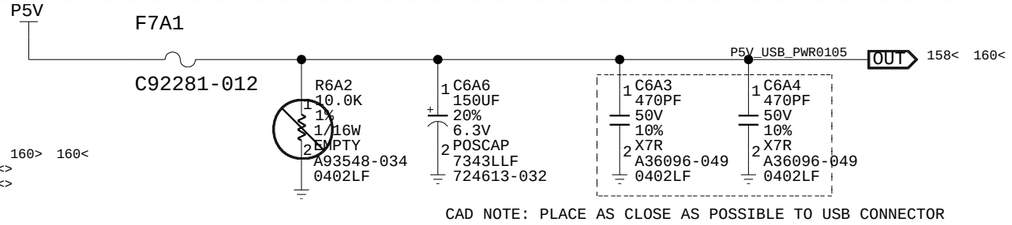
DE NOTE: USE P5V_AUX IF BOARD NEEDS TO SUPPORT USB WAKE FROM S3/S4



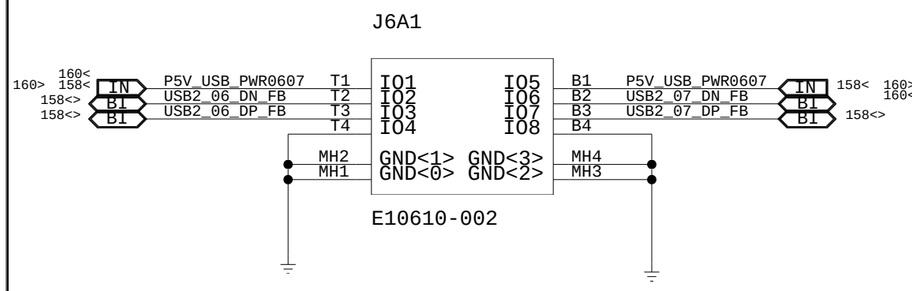
CAD NOTE: PLACE AS CLOSE AS POSSIBLE TO USB CONNECTOR

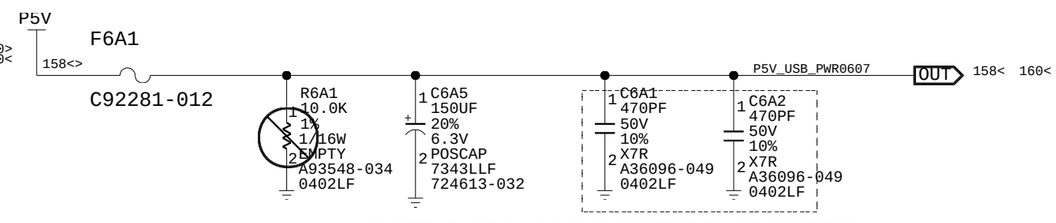
ROOM = REAR_USB





CAD NOTE: PLACE AS CLOSE AS POSSIBLE TO USB CONNECTOR





CAD NOTE: PLACE AS CLOSE AS POSSIBLE TO USB CONNECTOR

Wed Oct 27 15:21:44 2010

REAR USB 2.0 & ZEPHYR CONNECTORS

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 160 OF 303	

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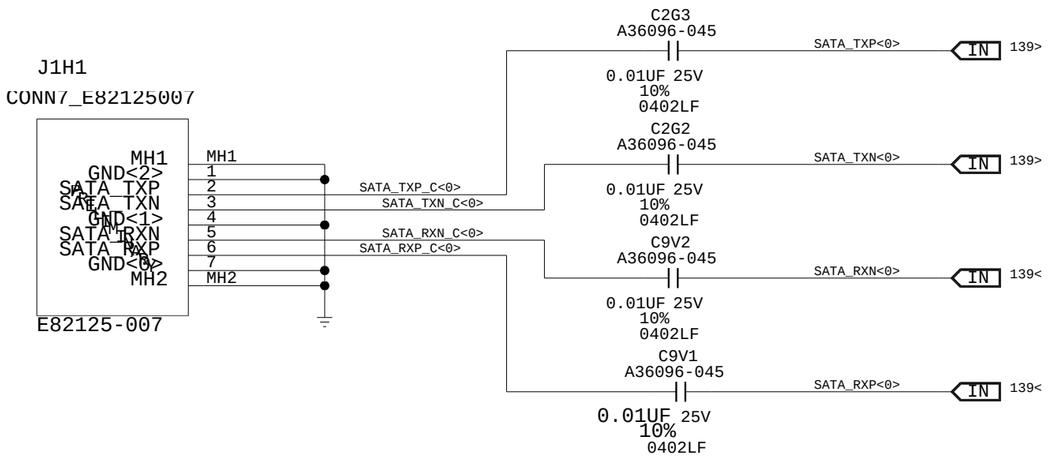
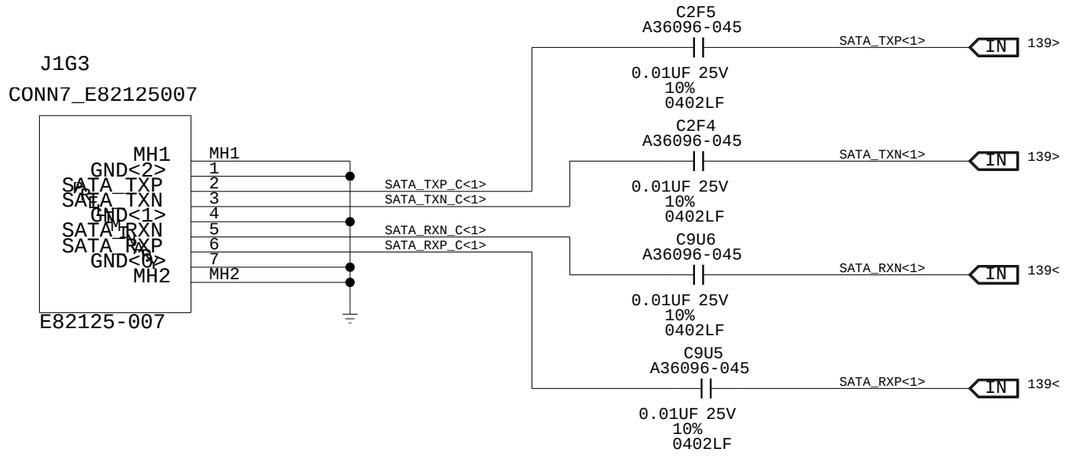
REPLACE SATA CONNECTORS WITH IPN E60833-002





ROOM = SATA

SATA

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DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 161 OF 303	

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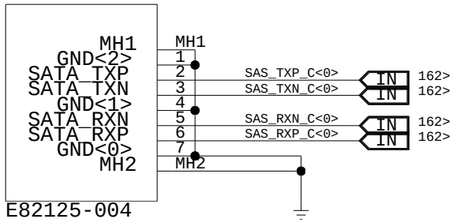
ROOM = SAS

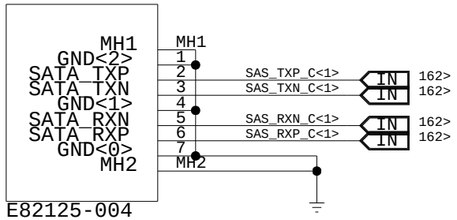
J1E6

CONN7_E82125004



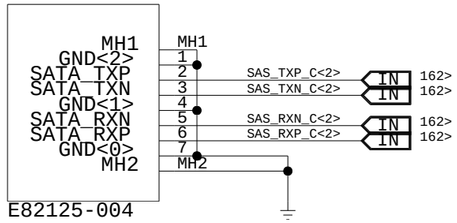
J1F2

CONN7_E82125004



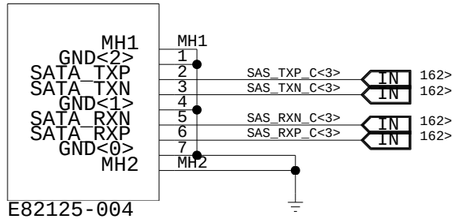
J1F3

CONN7_E82125004



J1G2

CONN7_E82125004



C2E15 A36096-045
139> IN SAS_TXP<0> SAS_TXP_C<0> OUT 162<
0.01UF 25V 10% 0402LF

C2E16 A36096-045
139> IN SAS_TXN<0> SAS_TXN_C<0> OUT 162<
0.01UF 25V 10% 0402LF

C9R5 A36096-045
139< IN SAS_RXP<0> SAS_RXP_C<0> OUT 162<
0.01UF 25V 10% 0402LF

C9R6 A36096-045
139< IN SAS_RXN<0> SAS_RXN_C<0> OUT 162<
0.01UF 25V 10% 0402LF

C2E13 A36096-045
139> IN SAS_TXP<1> SAS_TXP_C<1> OUT 162<
0.01UF 25V 10% 0402LF

C2E14 A36096-045
139> IN SAS_TXN<1> SAS_TXN_C<1> OUT 162<
0.01UF 25V 10% 0402LF

C9T4 A36096-045
139< IN SAS_RXP<1> SAS_RXP_C<1> OUT 162<
0.01UF 25V 10% 0402LF

C9T5 A36096-045
139< IN SAS_RXN<1> SAS_RXN_C<1> OUT 162<
0.01UF 25V 10% 0402LF

C2E11 A36096-045
139> IN SAS_TXP<2> SAS_TXP_C<2> OUT 162<
0.01UF 25V 10% 0402LF

C2E12 A36096-045
139> IN SAS_TXN<2> SAS_TXN_C<2> OUT 162<
0.01UF 25V 10% 0402LF

C9T13 A36096-045
139< IN SAS_RXP<2> SAS_RXP_C<2> OUT 162<
0.01UF 25V 10% 0402LF

C9T14 A36096-045
139< IN SAS_RXN<2> SAS_RXN_C<2> OUT 162<
0.01UF 25V 10% 0402LF

C2E9 A36096-045
139> IN SAS_TXP<3> SAS_TXP_C<3> OUT 162<
0.01UF 25V 10% 0402LF

C2E10 A36096-045
139> IN SAS_TXN<3> SAS_TXN_C<3> OUT 162<
0.01UF 25V 10% 0402LF

C9U1 A36096-045
139< IN SAS_RXP<3> SAS_RXP_C<3> OUT 162<
0.01UF 25V 10% 0402LF

C9U2 A36096-045
139< IN SAS_RXN<3> SAS_RXN_C<3> OUT 162<
0.01UF 25V 10% 0402LF

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SAS

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 162 OF 303

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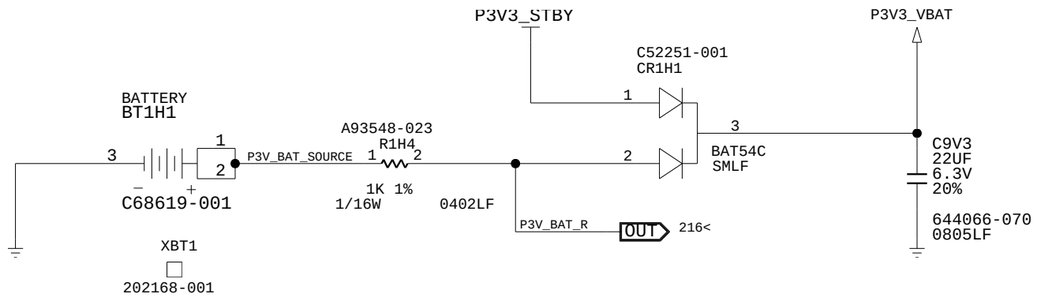
BATTERY



COIN TYPE BATTERY

CAD NOTE:
PLACE 22UF CLOSE TO DIODE
NEAR BATTERY HOLDER

ROOM = BATTERY

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BATTERY CIRCUIT

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 163 OF 303	

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Wed Oct 27 14:54:08 2010

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 164 OF 303	

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Wed Oct 27 14:54:08 2010

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 165 OF 303	

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Wed Oct 27 14:54:09 2010

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 166 OF 303	

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Wed Oct 27 14:54:09 2010

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 167 OF 303	

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CAD NOTE: PLACE 33 OHMS RESISTORS CLOSE TO PATSBURG
CAD NOTE: USE 0 OHMS RESISTORS TO ISOLATE CIRCUITS OTHER THAN XDP CONNECTOR

136< IN FM_USB_OC0_R_N — 1/16W 33 1% R1F42 0402LF A93548-503 — FM_USB_OC0_N OUT 168<
0402LF — R9W4 0 1/16W A93549-001 5% — FM_USB_OC_ZEP_N IN 160>

136< IN FM_USB_OC1_R_N — 1/16W 33 1% R1F21 0402LF A93548-503 — FM_USB_OC1_N OUT 168<
0402LF — R9W7 0 1/16W A93549-001 5% — FM_USB_OC_TAINT_N IN 159>

136< IN FM_USB_OC2_R_N — 1/16W 33 1% R1F24 0402LF A93548-503 — FM_USB_OC2_N OUT 168<
0402LF — R9W10 0 1/16W A93549-001 5% — FM_USB_OC_BP1_N IN 158>

136< IN FM_USB_OC3_R_N — 1/16W 33 1% R9T21 0402LF A93548-503 — FM_USB_OC3_N OUT 168<
0402LF — R9W12 0 1/16W A93549-001 5% — FM_USB_OC_BP2_N IN 158>

136< IN FM_USB_OC4_R_N — 1/16W 33 1% R8U2 0402LF A93548-503 — FM_USB_OC4_N OUT 168<
0402LF — R9W14 0 1/16W A93549-001 5% — FM_USB_OC_INT1_N IN 157>

136< IN FM_USB_OC5_R_N — 1/16W 33 1% R1F26 0402LF A93548-503 — FM_USB_OC5_N OUT 168<
0402LF — R9W16 0 1/16W A93549-001 5% — FM_USB_OC_INT2_N IN 158>

136< IN PU_USB_OC6_R_N — 1/16W 33 1% R8U3 0402LF A93548-503 — PU_USB_OC6_2_N OUT 168<
0402LF — R9W19 0 1/16W A93549-001 5% — PU_USB_OC6_N IN 147>

136> IN PU_USB_OC7_R_N — 1/16W 33 1% R1F27 0402LF A93548-503 — PU_USB_OC7_2_N OUT 168<
0402LF — R9W22 0 1/16W A93549-001 5% — PU_USB_OC7_N IN 147>

136> IN SSB_GP28_R — 1/16W 33 1% R2G33 0402LF A93548-503 — SSB_GP28 OUT 168> 168<
0402LF — R9W5 0 1/16W A93549-001 5% — PD_SSB_GP28 IN 147> 155>

136> IN FM_NMI_EVENT_R_N — 1/16W 33 1% R2G34 0402LF A93548-503 — FM_NMI_EVENT_2_N OUT 168<
0402LF — R9W8 0 1/16W A93549-001 5% — FM_NMI_EVENT_N IN 176< 190>

136< IN SATA0GP_GPIO21_R — 1/16W 33 1% R8U12 0402LF A93548-503 — SATA0GP_GPIO21 OUT 168<
0402LF — R9W11 0 1/16W A93549-001 5% — PU_ROL_MODULE_PRES_N IN 147>

136> IN SATA1GP_GPIO19_R — 1/16W 33 1% R2G5 0402LF A93548-503 — SATA1GP_GPIO19 OUT 168> 168<
0402LF — R9W13 0 1/16W A93549-001 5% — FM_BIOS_SPI_WP_N IN 147> 152<

136< IN SATA2GP_GPIO36_R — 1/16W 33 1% R2G4 0402LF A93548-503 — SATA2GP_GPIO36 OUT 168<
0402LF — R9W15 0 1/16W A93549-001 5% — FM_BIOS_ADV_FUNCTIONS IN 150>

136< IN SATA3GP_GPIO37_R — 1/16W 33 1% R2G3 0402LF A93548-503 — SATA3GP_GPIO37 OUT 168<
0402LF — R9W18 0 1/16W A93549-001 5% — PU_SSB_PS_PWROK_LVC3 IN 147>

136< IN SATA4GP_GPIO16_MGPIO9_R — 1/16W 33 1% R8U11 0402LF A93548-503 — SATA4GP_GPIO16_MGPIO9 OUT 168<
0402LF — R9W21 0 1/16W A93549-001 5% — FM_QPI_SLOW_MODE_N IN 150>

136> IN SATA5GP_GPIO49_MGPIO10_R — 1/16W 33 1% R8U10 0402LF A93548-503 — SATA5GP_GPIO49_MGPIO10 OUT 168<
0402LF — R9W24 0 1/16W A93549-001 5% — FM_BIOS_POST_CMPLT_N IN 176< 188<

136<> IN GPIO15_R — 1/16W 33 1% R8U1 0402LF A93548-503 — XDP_CLK1 OUT 168<
0402LF — R9W2 0 1/16W A93549-001 5% — FM_SAS_SATA_RAID_KEY IN 149<>

135> IN CLK2_R_IRQ_SSB_SCI_WHEA_N — 1/16W 33 1% R2G1 0402LF A93548-503 — CLK2_IRQ_SSB_SCI_WHEA_N OUT 168<
0402LF — R9W3 0 1/16W A93549-001 5% — IRQ_SSB_SCI_WHEA_N IN 147>

PBG XDP

XDP CONNECTOR MUST BE REMOVED FOR PRODUCTION

PATSBURG_XDP

P3V3_STBY — SMLF — P3V3_STBY

J1J1
C21100-002

	TP_XDP_SSB_3	1 3	
	TP_XDP_SSB_5	5 7	
168> IN	FM_USB_OC0_N	9	2 4 XDP_CLK1 IN 168>
			6 CLK2_IRQ_SSB_SCI_WHEA_N IN 168>
168> IN	FM_USB_OC1_N	11	8
		13	10 SSB_GP28 IN 168>
168> IN	FM_USB_OC2_N	15	12 FM_NMI_EVENT_2_N IN 168>
168> IN	FM_USB_OC3_N	17	14
		19	16 SATA0GP_GPIO21 IN 168>
	TP_XDP_SSB_21	21	18 SATA1GP_GPIO19 IN 168>
	TP_XDP_SSB_23	23	20
		25	22 TP_XDP_SSB_22
168> IN	FM_USB_OC4_N	27	24 TP_XDP_SSB_24
168> IN	FM_USB_OC5_N	29	26
		31	28 SATA2GP_GPIO36 IN 168>
168> IN	PU_USB_OC6_2_N	33	30 SATA3GP_GPIO37 IN 168>
168> IN	PU_USB_OC7_2_N	35	32
		37	34 SATA4GP_GPIO16_MGPIO9 IN 168>
169> 147> 135< IN	PWRGD_PCH_APWROK_LVC3 — R1J32 1K 1% 1/16W 0402LF A93548-023 — PWRGD_PCH_APWROK_LVC3_R	39	36 SATA5GP_GPIO49_MGPIO10 IN 168>
302> 169< 134< OUT	PWRGD_XDP_CO	41	38
		43	40 NC_SINAI_JTAG_VREF
	TP_XDP_SSB_45	45	42 TP_XDP_SSB_42
	TP_XDP_SSB_47	47	44
		49	46 RST_IBMC_RSTBTN_OUT_R_N — R1J34 1K 1% 1/16W 0402LF A93548-023 — RST_IBMC_RSTBTN_OUT_N IN 148< 178>
202<> 156<> 134<> 30<> 28<> BI	SMB_HOST_LVC3_DATA	51	48 RST_XDP_CO_N OUT 134> 169< 229< 302>
202> 156<> 134< 30< 28< OUT	SMB_HOST_LVC3_CLK	53	50
	TP_XDP_SSB_55	55	52 JTAG_SSB_TDO IN 137> 168<
168< 137< OUT	JTAG_SSB_TCK	57	54 TP_XDP_SSB_54
		59	56 JTAG_SSB_TDI OUT 137< 168<
			58 JTAG_SSB_TMS OUT 137< 168<
			60

SCONN60 C21100002

NOTE: PWRGD_XDP_CO AND RST_XDP_CO_N ARE OPEN DRAIN SIGNALS
PULL UPS ARE INCLUDED ON PAGES 301 AND 302 RESPECTIVELY

CAD NOTE: PLACE TCK TERMINATION WITHIN 1'' FROM PBG

168> 137< IN JTAG_SSB_TCK — R2G7 51.10 1% 1/16W A93548-072 0402LF

CAD NOTE: PLACE TMS AND TDI TERMINATION WITHIN 1'' FROM PBG
CAD NOTE: PLACE TDO TERMINATION WITHIN 1'' FROM XDP CONN

P3V3_STBY

168> 137< IN JTAG_SSB_TMS — R1F38 150 1% 1/10W A93550-034 0603LF — R2F17 150 1% 1/10W A93550-034 0603LF — R1J40 150 1% 1/10W A93550-034 0603LF
168> 137< IN JTAG_SSB_TDI
168< 137> IN JTAG_SSB_TDO — R1F40 75 1% 1/10W A93550-023 0603LF — R2G8 75 1% 1/10W A93550-023 0603LF — R1J42 75 1% 1/10W A93550-023 0603LF

VTH=1.1V
RTH=50.5 OHMS

P3V3_STBY

168> 168< OUT SSB_GP28 — 1/16W 1% 0402LF — R8U13 4.7K A93548-517

P3V3

168< 168> OUT SATA1GP_GPIO19 — 1/16W 1% 0402LF — R8U18 4.7K A93548-517

ROOM = DEBUG_XDP_PBG

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		SCALE:	DO NOT SCALE DRAWING	SHEET 168 OF 303

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U2D1

EPM570

P3V3_STBY

		9	VCCIO1<3>	VCCIO2<3>	82		
		25	VCCIO1<2>	VCCIO2<2>	100		
		46	VCCIO1<1>	VCCIO2<1>	116		
		64	VCCIO1<0>	VCCIO2<0>	136		
		19	VCCINT<3>	IOB2<57>	73	VR_P1V1_MAIN_CO_EN_N	OUT 276<
		56	VCCINT<2>	IOB2<56>	74	PWRGD_VR_P1V1_MAIN_CO	IN 276>
		90	VCCINT<1>	IOB2<55>	75	VR_P1V5_MAIN_CO_EN	OUT 278<
		126	VCCINT<0>	IOB2<54>	76	PWRGD_VR_P1V5_MAIN_CO	IN 278>
				IOB2<53>	77	VR_P0V65_TWV_CO_EN_N	OUT 286<
				IOB2<52>	78	PWRGD_VR_P0V65_TWV_CO	IN 286>
				IOB2<51>	79	VR_P0V85_TWV_CO_EN_N	OUT 283<
				IOB2<50>	80	PWRGD_VR_P0V85_TWV_CO	IN 283>
				IOB2<49>	81	VR_P1V2_TWV_CO_EN_N	OUT 285<
				IOB2<48>	84	PWRGD_VR_P1V2_TWV_CO	IN 285>
				IOB2<47>	85	VR_P2V6_TWV_CO_EN_N	OUT 282<
				IOB2<46>	86	PWRGD_VR_P2V6_TWV_CO	IN 282>
				IOB2<45>	87	PWRGD_VR_P3V3_STBY_CO	IN 32< 279>
				IOB2<44>	88	VR_P1V5_STBY_CO_EN	OUT 281<
				IOB2<43>	93	PWRGD_VR_P1V5_STBY_CO	IN 281>
				IOB2<42>	94	VR_P0V75_STBY_CO_EN	OUT 278<
				IOB2<41>	95	PWRGD_VR_P0V75_STBY_CO	IN 278>
				IOB2<40>	96	VR_P1V0_STBY_CO_EN	OUT 281<
				IOB2<39>	97	PWRGD_VR_P1V0_STBY_CO	IN 281>
				IOB2<38>	98	VR_P1V1_STBY_CO_EN_N	OUT 273<
				IOB2<37>	101	PWRGD_VR_P1V1_STBY_CO	IN 273>
				IOB2<36>	102	PWRGD_PS_BUF_LVC3	OUT 188< 232<
				IOB2<35>	103	VR_P1V8_STBY_CO_EN	OUT 274<
				IOB2<34>	104	PWRGD_VR_P1V8_STBY_CO	IN 274>
				IOB2<33>	105	FM_NIC_LAN_PWR_GOOD	OUT 219<
				IOB2<32>	106	LED_CPLD_ERR0_LVC3	OUT 301<
				IOB2<31>	107	LED_CPLD_ERR1_LVC3	OUT 301<
				IOB2<30>	108	LED_CPLD_ERR2_LVC3	OUT 301<
				IOB2<29>	109	LED_CPLD_ERR3_LVC3	OUT 301<
				IOB2<28>	110	FM_CPLD_PSON_R_LVC3_N	IN 177>
				IOB2<27>	111	FM_IBMC_PS_PWROK_LVC3	OUT 176<
				IOB2<26>	112	FM_PS_EN_LVC3	OUT 303<
				IOB2<25>	113	PWRGD_PS_PWROK_LVC3_N	IN 303>
				IOB2<24>	114	FM_SLPA_LVC3_N	IN 135>
				IOB2<23>	117	FM_SLPS3_LVC3_N	IN 129< 135> 177<
				IOB2<22>	118	FM_SLPS4_LVC3_N	IN 129< 135> 177< 230<
				IOB2<21>	119	FP_PWR_BTN_CO_N	OUT 178< 229>
				IOB2<20>	120	FM_PERST_SRC_LVC3	IN 302>
				IOB2<19>	121	FM_CPU_CLKEN_CO_N	OUT 30<
				IOB2<18>	122	FM_CK420_CLK_EN_CO_N	OUT 28< 130<
				IOB2<17>	123	PWRGD_XDP_CO	IN 134> 168> 302>
				IOB2<16>	124	RST_XDP_CO_N	IN 134> 168> 229< 302>
				IOB2<15>	125	FM_XDP_PWRCYCLE_MODE_CO	IN 302>
				IOB2<14>	127	FM_CPLD_VCCP_PWRGD_LVC3	IN 170>
				IOB2<13>	129	FM_CPLD_CPU_PWREN_LVC3	OUT 170<
				IOB2<12>	130	FM_CPLD_CPU_PWRGD_LVC3	IN 170>
				IOB2<11>	131	FM_CPLD_CPU_PWRFLT_LVC3	IN 170>
				IOB2<10>	132	FM_CPLD_MEM_PWREN_LVC3	OUT 170<
				IOB2<9>	133	FM_CPLD_MEM_PWRGD_LVC3	IN 170>
				IOB2<8>	134	FM_CPLD_MEM_PWRFLT_LVC3	IN 170>
				IOB2<7>	137	NC_CPLDSOUTH_137	
				IOB2<6>	138	NC_CPLDSOUTH_138	
				IOB2<5>	139	FM_CPLD_CHANNEL5_LVC3	BI 170<>
				IOB2<4>	140	FM_CPLD_CHANNEL4_LVC3	BI 170<>
				IOB2<3>	141	FM_CPLD_CHANNEL3_LVC3	BI 170<>
				IOB2<2>	142	FM_CPLD_CHANNEL2_LVC3	BI 170<>
				IOB2<1>	143	FM_CPLD_CHANNEL1_LVC3	BI 170<>
				IOB2<0>	144	FM_CPLD_CHANNEL0_LVC3	BI 170<>

100>	IN	FM_THERMTRIP_LVC3_N	1	IOB1<51>		
148<	OUT	FM_THERMTRIP_DLY_LVC3	2	IOB1<50>		
231> 188< 176<	IN	IRQ_SML1_PMBUS_ALERT_N	3	IOB1<49>		
212<	OUT	IRQ_FAN_12V_GATE_LVC3	4	IOB1<48>		
129< 78>	IN	FM_ERR1_LVC3_N	5	IOB1<47>		
147> 138<	OUT	FM_ERR1_DLY_CO_N	6	IOB1<46>		
135> 135<	IN	FM_THROTTLE_LVC3_N	7	IOB1<45>		
124<	OUT	FM_SYS_THROTTLE_LVC3	8	IOB1<44>		
176< 148< 130< 99>	IN	IRQ_CPU_CATERR_LVC3_N	11	IOB1<43>		
136<	OUT	IRQ_CPU_CATERR_DLY_LVC3_N	12	IOB1<42>		
30<	OUT	FM_DB1900_CLK_EN_CO	13	IOB1<41>		
208<	OUT	RST_DLY_CPURST_LVC3	14	IOB1<40>		
148>	IN	PWRGD_CPUPWRGD_LVC3	15	IOB1<39>		
148< 147< 135< 129<	IN	RST_PCH_PLTRST_LVC3_N	16	IOB1<38>		
147>	IN	PWRGD_PCH_DRAMPWRGD_CO	21	IOB1<37>		
125>	IN	RST_CPU_EAR_LVC3_N	22	IOB1<36>		
168< 147> 135<	OUT	PWRGD_PCH_APWROK_LVC3	23	IOB1<35>		
219< 219> 204< 177< 147> 135<	OUT	PWRGD_PCH_PWROK_LVC3	24	IOB1<34>		
147> 135< 129<	OUT	PWRGD_PCH_SYS_PWROK_LVC3	27	IOB1<33>		
77<	OUT	RST_CPU0_RESET_LVC3_N	28	IOB1<32>		
		NC_CPLDSOUTH_29	29	IOB1<31>		
207< 206>	OUT	SGPIO_IBMC_LD_GATE_LVC3_N	30	IOB1<30>		
77<	OUT	RST_CPU3_RESET_LVC3_N	31	IOB1<29>		
77<	OUT	PWRGD_CPU0_PWRGOOD_LVC3	32	IOB1<28>		
		NC_CPLDSOUTH_37	37	IOB1<27>		
		NC_CPLDSOUTH_38	38	IOB1<26>		
77<	OUT	PWRGD_CPU3_PWRGOOD_LVC3	39	IOB1<25>		
77<	OUT	PWRGD_CPU0_DRAMPWRGD_LVC3	40	IOB1<24>		
		NC_CPLDSOUTH_41	41	IOB1<23>		
		NC_CPLDSOUTH_42	42	IOB1<22>		
77<	OUT	PWRGD_CPU3_DRAMPWRGD_LVC3	43	IOB1<21>		
218< 175< 156<	OUT	RST_IBMC_NIC_LRESET_LVC3_N	44	IOB1<20>		
171<	OUT	RST_PERST_LVC3_N	45	IOB1<19>		
		NC_CPLDSOUTH_48	48	IOB1<18>		
		NC_CPLDSOUTH_49	49	IOB1<17>		
		NC_CPLDSOUTH_50	50	IOB1<16>		
		NC_CPLDSOUTH_51	51	IOB1<15>		
206< 170< 129< 102> 54>	IN	FM_CPU3_SKTOCC_CO_N	52	IOB1<14>		
206< 170< 129< 79> 54>	IN	FM_CPU2_SKTOCC_CO_N	53	IOB1<13>		
207< 170< 133< 129< 56> 54>	IN	FM_CPU1_SKTOCC_CO_N	55	IOB1<12>		
207< 170< 129< 54> 33>	IN	FM_CPU0_SKTOCC_CO_N	57	IOB1<11>		
170< 140>	IN	FM_SSB_PRSNT_CO_N	58	IOB1<10>		
301>	IN	FM_CPLD_DBGMODE_LVC3_N	59	IOB1<9>		
301<>	BI	FM_CPLD_DEBUG0_LVC3	62	IOB1<8>		
301<>	BI	FM_CPLD_DEBUG1_LVC3	63	IOB1<7>		
301<>	BI	FM_CPLD_DEBUG2_LVC3	66	IOB1<6>		
301<>	BI	FM_CPLD_DEBUG3_LVC3	67	IOB1<5>		
301<>	BI	FM_CPLD_DEBUG4_LVC3	68	IOB1<4>		
301<>	BI	FM_CPLD_DEBUG5_LVC3	69	IOB1<3>		
301<>	BI	FM_CPLD_DEBUG6_LVC3	70	IOB1<2>		
301<>	BI	FM_CPLD_DEBUG7_LVC3	71	IOB1<1>		
170>	IN	FM_CPUVALIDCFG_LVC3	72	IOB1<0>		
206<	OUT	SGPIO_CPLD_DATOUT_LVC3	61	IO_DEV_CLR_N		
		NC_CPLDSOUTH_60	60	IO_DEV_OE		
204< 192< 188< 170< 148>	IN	RST_RSMRST_N	91	IO_GCLK<3>		
		CLK_33K_SOUTHCPLD_LVC3	89	IO_GCLK<2>		
207< 206> 206<	IN	SGPIO_IBMC_CLK_BUF_LVC3	20	IO_GCLK<1>		
207< 206> 206<	IN	SGPIO_IBMC_LD_BUF_LVC3_N	18	IO_GCLK<0>		
169>	IN	JTAG_CPLD_TDI_LVC3	34	TDI	TDO	36 JTAG_SOUTHCPLD_TDO_LVC3 OUT 170<
170< 169>	IN	JTAG_CPLD_TMS_LVC3	33	TMS		
170< 169>	IN	JTAG_CPLD_TCK_LVC3	35	TCK		
			17	GNDINT<3>	GNDIO<7>	10
			54	GNDINT<2>	GNDIO<6>	26
			92	GNDINT<1>	GNDIO<5>	47
			128	GNDINT<0>	GNDIO<4>	65
					GNDIO<3>	83
					GNDIO<2>	99
					GNDIO<1>	115
					GNDIO<0>	135

E74324-001

R1C11 0402LF
1 — 2 CLK_33K_SUSCLK_PLD IN 32> 170<
8.20 5% 1/16W
A93549-064

CAD NOTE:
PLACE TERMINATION RESISTOR WITHIN 1'' FROM CK_MNG_133

DECOUPLING CAPS FOR SOUTH CPLD

PLACE ONE 0.1UF CAP FOR EACH VCC/GND PAIR OF THE CPLD
PLACE CLOSE TO PINS

P3V3_STBY

19	56	90	126
C9P4 0.1UF 16V 10%	C8N7 0.1UF 16V 10%	C8P1 0.1UF 16V 10%	C9N21 0.1UF 16V 10%
A36096-030 0402LF	A36096-030 0402LF	A36096-030 0402LF	A36096-030 0402LF
17	54	92	128
9	25	46	64
C8P9 0.1UF 16V 10%	C8P2 0.1UF 16V 10%	C8P8 0.1UF 16V 10%	C8P5 0.1UF 16V 10%
A36096-030 0402LF	A36096-030 0402LF	A36096-030 0402LF	A36096-030 0402LF
10	26	47	65
82	100	116	136
C9P7 0.1UF 16V 10%	C9P1 0.1UF 16V 10%	C9P3 0.1UF 16V 10%	C8N6 0.1UF 16V 10%
A36096-030 0402LF	A36096-030 0402LF	A36096-030 0402LF	A36096-030 0402LF
83	99	115	135

ALTERA IN SYSTEM PROGRAMMING HEADER

P3V3_STBY P3V3_STBY

R9P33 1/16W 1% 10.0K 0402LF A93548-034

J8F1 CONN10

170< 169<	OUT	JTAG_CPLD_TCK_LVC3	1 — 2
170>	IN	JTAG_CPLD_TDO_LVC3	3 — 4
170< 169<	OUT	JTAG_CPLD_TMS_LVC3	5 — 6 NC_CPLD_ISPH_PIN6
		NC_CPLD_ISPH_PIN7	7 — 8 NC_CPLD_ISPH_PIN8
169<	OUT	JTAG_CPLD_TDI_LVC3	9 — 10

C73564-005

R9P32 1/16W 1% 1K 0402LF A93548-023

C9F2 10UF 6.3V 20% 602433-075 0603LF
C9F1 0.1UF 16V 10% A36096-030 0402LF

CAD NOTE:
PLACE THESE CAPS CLOSE TO ISPH HEADER OF CPLD.

ROOM=CPLD_SOUTH

Wed Oct 27 15:21:45 2010

SOUTH CPLD

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 169 OF 303	

INTEL CONFIDENTIAL

ROOM=CPLD_NORTH

U9F1

P3V3_STBY

EPM240

E7	VCCINT<1>		
F4	VCCINT<0>		
G6	VCCIO1<2>	TDO	J2
G4	VCCIO1<1>		
E4	VCCIO1<0>		
D4	VCCIO2<2>	GCLK1_IO<37>	E1
D6	VCCIO2<1>	IO<36>	D9
F7	VCCIO2<0>	IO<35>	D8
		IO<34>	D3
		IO<33>	D2
K8	IO<79>	IO<32>	D10
K7	IO<78>	IO<31>	D1
K6	IO<77>	IO<30>	C9
K5	IO<76>	IO<29>	C8
K4	IO<75>	IO<28>	C7
K3	IO<74>	IO<27>	C6
K2	IO<73>	IO<26>	C5
K10	IO<72>	IO<25>	C4
K1	IO<71>	IO<24>	C3
J9	IO<70>	IO<23>	C2
J8	IO<69>	IO<22>	C10
J7	DEV_OE_IO<68>	IO<21>	C1
J6	IO<67>	IO<20>	B9
J5	IO<66>	IO<19>	B8
J4	IO<65>	IO<18>	B7
J3	IO<64>	IO<17>	B6
J10	IO<63>	IO<16>	B5
H9	IO<62>	IO<15>	B4
H8	IO<61>	IO<14>	B3
H7	IO<60>	IO<13>	B2
H6	IO<59>	IO<12>	B10
H5	IO<58>	IO<11>	B1
H4	IO<57>	IO<10>	A9
H10	IO<56>	IO<9>	A8
H1	IO<55>	IO<8>	A7
G9	IO<54>	IO<7>	A6
G8	IO<53>	IO<6>	A5
G3	IO<52>	IO<5>	A4
G2	IO<51>	IO<4>	A3
G10	IO<50>	IO<3>	A2
G1	IO<49>	IO<2>	A10
F9	IO<48>	IO<1>	A1
F8	GCLK2_IO<47>		K9
F3	IO<46> DEV_CLR_N_IO<0>		
F2	IO<45>		
F10	IO<44>	GNDINT<1>	F5
F1	IO<43>	GNDINT<0>	E6
E9	IO<42>	GNDIO<5>	D5
E8	IO<41>	GNDIO<4>	D7
E3	IO<40>	GNDIO<3>	F6
E2	GCLK0_IO<39>	GNDIO<2>	G7
E10	GCLK3_IO<38>	GNDIO<1>	G5
J1	TMS	GNDIO<0>	E5
H3	TCK		
H2	TDI		

E58496-001

238>	IN	PWRGD_VR_VCCP_CPU1_CO	K8	
238>	IN	PWRGD_VR_VSA_CPU1_CO	K7	
269<	OUT	VR_PV_VTT_CPU0_CO_EN	K6	
269>	IN	PWRGD_VR_VTT_CPU0_CO	K5	
253>	IN	PWRGD_VR_VDDQ_CPU0_CO	K4	
233<	OUT	VR_PV_VCCP_VSA_CPU0_CO_EN	K3	
253<	OUT	VR_PV_VDDQ_CPU0_CO_EN	K2	
238<	OUT	VR_PV_VCCP_VSA_CPU1_CO_EN	K10	
255<	OUT	VR_PV_VTT_DDR3_CPU0_CO_EN	K1	
258<	OUT	VR_PV_VTT_DDR3_CPU1_CO_EN	J9	
256<	OUT	VR_PV_VDDQ_CPU1_CO_EN	J8	
		NC_CPLDNORTH_J7	J7	
270<	OUT	VR_PV_VTT_CPU1_CO_EN	J6	
255>	IN	PWRGD_VR_VTT_DDR3_CPU0_CO	J5	
233>	IN	PWRGD_VR_VSA_CPU0_CO	J4	
271<	OUT	VR_PV_VTT_CPU2_CO_EN	J3	
256>	IN	PWRGD_VR_VDDQ_CPU1_CO	J10	
266>	IN	PWRGD_VR_PLL_CPU1_CO	H9	
265<	OUT	VR_PLL_CPU0_CO_EN	H8	
271>	IN	PWRGD_VR_VTT_CPU2_CO	H7	
270>	IN	PWRGD_VR_VTT_CPU1_CO	H6	
265>	IN	PWRGD_VR_PLL_CPU0_CO	H5	
233>	IN	PWRGD_VR_VCCP_CPU0_CO	H4	
258>	IN	PWRGD_VR_VTT_DDR3_CPU1_CO	H10	
272<	OUT	VR_PV_VTT_CPU3_CO_EN	H1	
77<	OUT	RST_CPU1_RESET_LVC3_N	G9	
266<	OUT	VR_PLL_CPU1_CO_EN	G8	
265< 206< 125>	IN	FM_CPU0_IVT_ID_LVC3_N	G3	
266< 206< 125>	IN	FM_CPU1_IVT_ID_LVC3_N	G2	
267< 206< 125>	IN	FM_CPU2_IVT_ID_LVC3_N	G10	
272>	IN	PWRGD_VR_VTT_CPU3_CO	G1	
77<	OUT	RST_CPU2_RESET_LVC3_N	F9	
		NC_CPLDNORTH_F8	F8	
		NC_CPLDNORTH_F3	F3	
169<>	BI	FM_CPLD_CHANNEL0_LVC3	F2	
77<	OUT	PWRGD_CPU1_PWRGOOD_LVC3	F10	
169<>	BI	FM_CPLD_CHANNEL1_LVC3	F1	
259>	IN	PWRGD_VR_VDDQ_CPU2_CO	E9	
77<	OUT	PWRGD_CPU2_PWRGOOD_LVC3	E8	
169<>	BI	FM_CPLD_CHANNEL2_LVC3	E3	
204< 192< 188< 169< 148>	IN	RST_RSMRST_N	E2	
		NC_CPLDNORTH_E10	E10	
169< 169>	IN	JTAG_CPLD_TMS_LVC3	J1	
169< 169>	IN	JTAG_CPLD_TCK_LVC3	H3	
169>	IN	JTAG_SOUTHCPLD_TDO_LVC3	H2	

J2	JTAG_CPLD_TDO_LVC3	OUT	169<
E1	CLK_33K_NORTHCPLD_LVC3	IN	32> 169<
D9	VR_PV_VTT_DDR3_CPU2_CO_EN	OUT	261<
D8	PWRGD_VR_VCCP_CPU2_CO	IN	243>
D3	FM_CPUVALIDCFG_LVC3	OUT	169<
D2	FM_CPLD_CHANNEL3_LVC3	BI	169<>
D10	PWRGD_CPU2_DRAMPWRGD_LVC3	OUT	77<
D1	FM_CPU1_SKTOCC_CO_N	IN	54> 56> 129< 133<
C9	PWRGD_VR_VSA_CPU2_CO	IN	169< 207< 243>
C8	VR_PV_VDDQ_CPU2_CO_EN	OUT	259<
C7	VR_PV_VCCP_VSA_CPU3_CO_EN	OUT	248<
C6	PWRGD_VR_VTT_DDR3_CPU2_CO	IN	261>
C5	FM_CPU3_SKTOCC_CO_N	IN	54> 102> 129< 169< 206<
C4	FM_CPLD_CPU_PWRGD_LVC3	OUT	169<
C3	FM_CPU3_IVT_ID_LVC3_N	IN	126> 206< 268<
C2	FM_CPU0_SKTOCC_CO_N	IN	33> 54> 129< 169< 207<
C10	VR_PV_VCCP_VSA_CPU2_CO_EN	OUT	243<
C1	FM_CPLD_CHANNEL4_LVC3	BI	169<>
B9	VR_PLL_CPU2_CO_EN	OUT	267<
B8	VR_PV_VTT_DDR3_CPU3_CO_EN	OUT	264<
B7	PWRGD_VR_PLL_CPU2_CO	IN	267>
B6	VR_PLL_CPU3_CO_EN	OUT	268<
B5	PWRGD_VR_VTT_DDR3_CPU3_CO	IN	264>
B4	FM_CPLD_VCCP_PWRGD_LVC3	OUT	169<
B3	PWRGD_CPU1_DRAMPWRGD_LVC3	OUT	77<
B2	FM_CPLD_CHANNEL5_LVC3	BI	169<>
B10	PWRGD_VR_VCCP_CPU3_CO	IN	248>
B1	FM_CPLD_MEM_PWRFLT_LVC3	OUT	169<
A9	PWRGD_VR_VSA_CPU3_CO	IN	248>
A8	VR_PV_VDDQ_CPU3_CO_EN	OUT	262<
A7	FM_SSB_PRSNT_CO_N	IN	140> 169<
A6	PWRGD_VR_PLL_CPU3_CO	IN	268>
A5	FM_CPU2_SKTOCC_CO_N	IN	54> 79> 129< 169< 206<
A4	FM_CPLD_CPU_PWREN_LVC3	IN	169>
A3	FM_CPLD_CPU_PWRFLT_LVC3	OUT	169<
A2	FM_CPLD_MEM_PWREN_LVC3	IN	169>
A10	PWRGD_VR_VDDQ_CPU3_CO	IN	262>
A1	FM_CPLD_MEM_PWRGD_LVC3	OUT	169<
K9	NC_CPLDNORTH_K9		

R1C12
1 — 2 CLK_33K_SUSCLK_PLD
8.20 5% 1/16W 0402LF
A93549-064

CAD NOTE:
PLACE TERMINATION RESISTOR WITHIN 1'' FROM CK_MNG_133

DECOUPLING CAPS FOR NORTH CPLD

PLACE ONE 0.1UF CAP FOR EACH VCC/GND PAIR OF THE CPLD; PLACE THEM CLOSE TO PINS

P3V3_STBY

E7	F4	G6	G4	E4	D4	D6	F7	
C1T8	C1T7	C1T4	C1T2	C1T6	C1T9	C1T5	C1T3	1
0.1UF	0.1UF	0.1UF	0.1UF	0.1UF	0.1UF	0.1UF	0.1UF	
16V	16V	16V	16V	16V	16V	16V	16V	
10%	10%	10%	10%	10%	10%	10%	10%	
A36096-030 0402LF	A36096-030 0402LF	A36096-030 0402LF	A36096-030 0402LF	A36096-030 0402LF	A36096-030 0402LF	A36096-030 0402LF	A36096-030 0402LF	2
F5	E6	D5	D7	F6	G7	G5	E5	

Wed Oct 27 15:21:45 2010

NORTH CPLD

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 170 OF 303	

INTEL CONFIDENTIAL

NO LANE REVERSAL

POLARITY INVERSION ON NETS: TX_PE1A <2:0>, RX_PE3B<3:0>

P3E_CPU0_RCONN_TX_PE1A_C_DN<3..0>
P3E_CPU0_RCONN_TX_PE1A_C_DP<3..0>
P3E_CPU0_RCONN_TX_PE1B_C_DN<3..0>
P3E_CPU0_RCONN_TX_PE1B_C_DP<3..0>
P3E_CPU0_RCONN_TX_PE3A_C_DN<3..0>
P3E_CPU0_RCONN_TX_PE3A_C_DP<3..0>
P3E_CPU0_RCONN_TX_PE3B_C_DN<3..0>
P3E_CPU0_RCONN_TX_PE3B_C_DP<3..0>
P3E_CPU0_RCONN_TX_PE3C_C_DN<3..0>
P3E_CPU0_RCONN_TX_PE3C_C_DP<3..0>
P3E_CPU0_RCONN_TX_PE3D_C_DN<3..0>
P3E_CPU0_RCONN_TX_PE3D_C_DP<3..0>
FM_RISER_ID0
TP_FM_RISER_ID
RST_PERST_LVC3_N
FM_PXPME_N

P3V3 3.3 P3V3_STBY 3.3 N12V -12

J3E1CONN280 CONN

P3V3 3.3
P12V 12
P5V 5

IRQ_SSB_WAKE_LVC3_N
NC_CHASSIS_INTRUSION_CO
PD_J11_PIN_A31
R3D8 0 5% A93549-001
1/16W CHIP 0402LF SUPERSLOT

P3E_CPU0_RCONN_RX_PE3D_DP<3..0>
P3E_CPU0_RCONN_RX_PE3D_DN<3..0>
P3E_CPU0_RCONN_RX_PE3C_DP<3..0>
P3E_CPU0_RCONN_RX_PE3C_DN<3..0>
P3E_CPU0_RCONN_RX_PE3B_DP<3..0>
P3E_CPU0_RCONN_RX_PE3B_DN<3..0>
P3E_CPU0_RCONN_RX_PE3A_DP<3..0>
P3E_CPU0_RCONN_RX_PE3A_DN<3..0>
P3E_CPU0_RCONN_RX_PE1B_DP<3..0>
P3E_CPU0_RCONN_RX_PE1B_DN<3..0>
P3E_CPU0_RCONN_RX_PE1A_DP<3..0>
P3E_CPU0_RCONN_RX_PE1A_DN<3..0>

CLK_100M_SLOT4_DP
CLK_100M_SLOT4_DN
CLK_100M_SLOT6_DP
CLK_100M_SLOT6_DN
CLK_100M_SLOT8_DP
CLK_100M_SLOT8_DN
CLK_100M_SLOT10_DP
CLK_100M_SLOT10_DN
FM_RISER_ID2
CLK_100M_SLOT5_DP
CLK_100M_SLOT5_DN
CLK_100M_SLOT7_DP
CLK_100M_SLOT7_DN
CLK_100M_SLOT9_DP
CLK_100M_SLOT9_DN
FM_RISER_ID1

C35295-006

DECOUPLING CAPS CAD NOTE: PLACE CAPS CLOSE TO RISER CONNECTOR

P3V3 3.3: C3E4 22UF 6.3V 20% X5R 644066-070 0805LF SUPERSLOT; C3E5 22UF 6.3V 20% X5R 644066-070 0805LF SUPERSLOT

P5V 5: C3D3 22UF 6.3V 20% X5R 644066-070 0805LF SUPERSLOT; C3D4 22UF 6.3V 20% X5R 644066-070 0805LF SUPERSLOT

P12V 12: C3D9 22UF 16V 20% X5R 644066-032 1210LF SUPERSLOT; C3D8 22UF 16V 20% X5R 644066-032 1210LF SUPERSLOT

P3V3_STBY 3.3: C3D10 22UF 6.3V 20% X5R 644066-070 0805LF SUPERSLOT; C3D11 22UF 6.3V 20% X5R 644066-070 0805LF SUPERSLOT

N12V -12: C3D6 22UF 16V 20% X5R 644066-032 1210LF SUPERSLOT; C3D5 22UF 16V 20% X5R 644066-032 1210LF SUPERSLOT

NOTE: PE WIDTH STRAPPING
ON ROMLEY, THE SANDY BRIDGE-EX AND IVY BRIDGE-EXB INTEGRATED IOM
DO NOT HAVE SUPPORT FOR THIS FEATURE

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ROOM: SUPERSLOT

RISER CONNECTOR (1 OF 2)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 171 OF 303	

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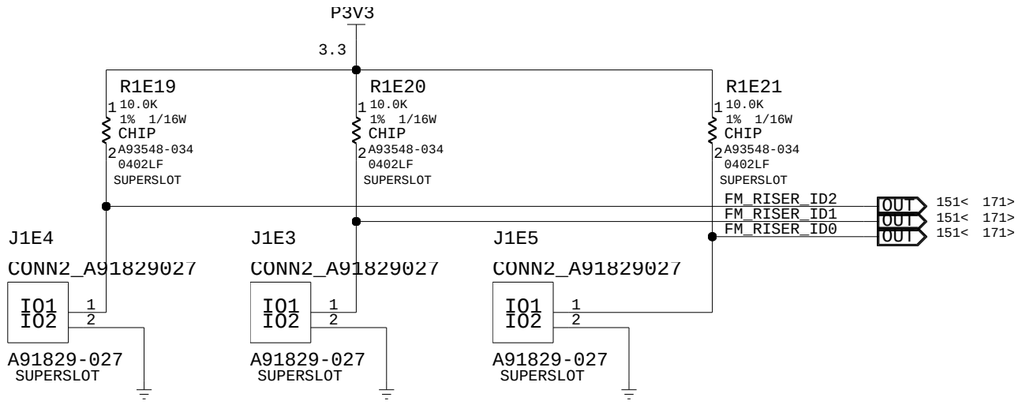
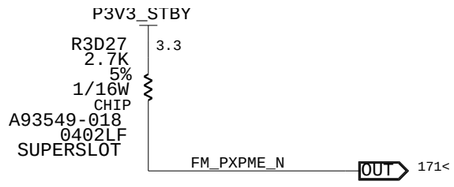
BOARD ID SETTINGS			
URBANNA CARDS PINS	RISER_TYPE3	RISER_TYPE2	RISER_TYPE1
POTTER CITY NAME	RISER_ID2	RISER_ID1	RISER_ID0
1U PCI-E RISER	1	0	0
2U PCI-E RISER	0	1	1

THE RISER_ID IS PULLED UP TO 3.3V ON THE BASEBOARD AND GROUNDED IF NECESSARY BY THE RISER, A RISER_ID GROUNDED BY THE RISER IS REPRESENTED BY A 0 IN THE TABLE ABOVE.





ROOM: SUPERSLOT

RISER CONNECTOR (2 OF 2)

Wed Oct 27 15:21:46 2010

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 172 OF 303	

INTEL CONFIDENTIAL

FROM ROMLEY PDG:
DECOUPLING CAP VALUE FOR PCIE GEN3 = 180NF TO 265NF

38> IN P3E_CPU0_RCONN_TX_PE1A_DP<3..0>

C6L12 A36096-028 — 0.220UF 6.3V 10% X5R 0402LF
C6L14 A36096-028 — 0.220UF 6.3V 10% X5R 0402LF
C6M1 A36096-028 — 0.220UF 6.3V 10% X5R 0402LF
C6M5 A36096-028 — 0.220UF 6.3V 10% X5R 0402LF

0	P3E_CPU0_RCONN_TX_PE1A_DP<0>	P3E_CPU0_RCONN_TX_PE1A_C_DP<0> 0
1	P3E_CPU0_RCONN_TX_PE1A_DP<1>	P3E_CPU0_RCONN_TX_PE1A_C_DP<1> 1
2	P3E_CPU0_RCONN_TX_PE1A_DP<2>	P3E_CPU0_RCONN_TX_PE1A_C_DP<2> 2
3	P3E_CPU0_RCONN_TX_PE1A_DP<3>	P3E_CPU0_RCONN_TX_PE1A_C_DP<3> 3

P3E_CPU0_RCONN_TX_PE1A_C_DP<3..0> OUT 171<

38> IN P3E_CPU0_RCONN_TX_PE1A_DN<3..0>

C6L13 A36096-028 — 0.220UF 6.3V 10% X5R 0402LF
C6L17 A36096-028 — 0.220UF 6.3V 10% X5R 0402LF
C6M2 A36096-028 — 0.220UF 6.3V 10% X5R 0402LF
C6M4 A36096-028 — 0.220UF 6.3V 10% X5R 0402LF

0	P3E_CPU0_RCONN_TX_PE1A_DN<0>	P3E_CPU0_RCONN_TX_PE1A_C_DN<0> 0
1	P3E_CPU0_RCONN_TX_PE1A_DN<1>	P3E_CPU0_RCONN_TX_PE1A_C_DN<1> 1
2	P3E_CPU0_RCONN_TX_PE1A_DN<2>	P3E_CPU0_RCONN_TX_PE1A_C_DN<2> 2
3	P3E_CPU0_RCONN_TX_PE1A_DN<3>	P3E_CPU0_RCONN_TX_PE1A_C_DN<3> 3

P3E_CPU0_RCONN_TX_PE1A_C_DN<3..0> OUT 171<

38> IN P3E_CPU0_RCONN_TX_PE1B_DP<3..0>

C7M20 A36096-028 — 0.220UF 6.3V 10% X5R 0402LF
C7M25 A36096-028 — 0.220UF 6.3V 10% X5R 0402LF
C7M29 A36096-028 — 0.220UF 6.3V 10% X5R 0402LF
C7M41 A36096-028 — 0.220UF 6.3V 10% X5R 0402LF

0	P3E_CPU0_RCONN_TX_PE1B_DP<0>	P3E_CPU0_RCONN_TX_PE1B_C_DP<0> 0
1	P3E_CPU0_RCONN_TX_PE1B_DP<1>	P3E_CPU0_RCONN_TX_PE1B_C_DP<1> 1
2	P3E_CPU0_RCONN_TX_PE1B_DP<2>	P3E_CPU0_RCONN_TX_PE1B_C_DP<2> 2
3	P3E_CPU0_RCONN_TX_PE1B_DP<3>	P3E_CPU0_RCONN_TX_PE1B_C_DP<3> 3

P3E_CPU0_RCONN_TX_PE1B_C_DP<3..0> OUT 171<

38> IN P3E_CPU0_RCONN_TX_PE1B_DN<3..0>

C7M19 A36096-028 — 0.220UF 6.3V 10% X5R 0402LF
C7M24 A36096-028 — 0.220UF 6.3V 10% X5R 0402LF
C7M28 A36096-028 — 0.220UF 6.3V 10% X5R 0402LF
C7M33 A36096-028 — 0.220UF 6.3V 10% X5R 0402LF

0	P3E_CPU0_RCONN_TX_PE1B_DN<0>	P3E_CPU0_RCONN_TX_PE1B_C_DN<0> 0
1	P3E_CPU0_RCONN_TX_PE1B_DN<1>	P3E_CPU0_RCONN_TX_PE1B_C_DN<1> 1
2	P3E_CPU0_RCONN_TX_PE1B_DN<2>	P3E_CPU0_RCONN_TX_PE1B_C_DN<2> 2
3	P3E_CPU0_RCONN_TX_PE1B_DN<3>	P3E_CPU0_RCONN_TX_PE1B_C_DN<3> 3

P3E_CPU0_RCONN_TX_PE1B_C_DN<3..0> OUT 171<

ROOM: CPU0 IOU0 RCONN

SUPERSLOT AC COUPLING

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DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 173 OF 303	

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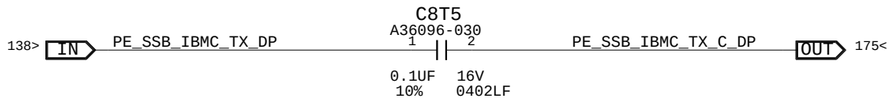
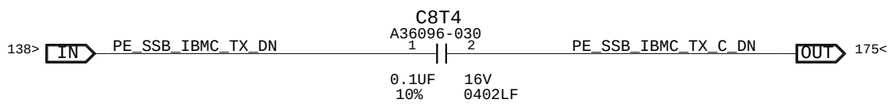
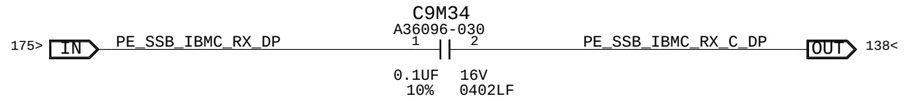
CAD NOTE: PLACE NEAR PATSBURG

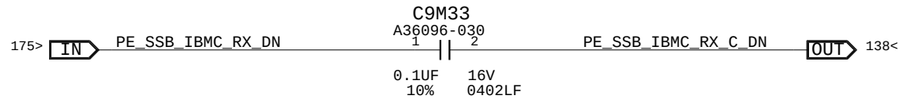




ROOM=PBG_IBMC_PCIE

CAD NOTE: PLACE NEAR IBMC





ROOM=IBMC_PBG_PCIE

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IBMC AND ASMI AC BLOCKING

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 174 OF 303

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ROOM=IBMC

U1A1

PILOT_III_D

31> IN	CLK_100M_IBMC_DP	AF9	PCIE_CLKP	PCIE_RTRIM	AG8	PD_IBMC_PCIE_RTRIM	R1B14 1.50K 1% 1/16W A93548-014 0402LF
31> IN	CLK_100M_IBMC_DN	AG9	PCIE_CLKN	PCIE_RTRIMN	AD10	PD_IBMC_PCIE_RTRIM_N	
174> IN	PE_SSB_IBMC_TX_C_DP	AF11	PCIE_RXP	PCIE_TXP	AG13	PE_SSB_IBMC_RX_DP	OUT 174<
174> IN	PE_SSB_IBMC_TX_C_DN	AG11	PCIE_RXN	PCIE_TXN	AF13	PE_SSB_IBMC_RX_DN	OUT 174<
218< 169> 156< IN	RST_IBMC_NIC_LRESET_LVC3_N — R2B10 75 A93548-003 1% 1/16W 0402LF — RST_IBMC_LVC3_N	AG15	SIO_LRESET_N	SIO_LAD_3	AF16	LPC_LAD<3>	LPC_LAD<3..0> BI 137<> 156<>
29> IN	CLK_33M_IBMC	AF15	SIO_LCLK	SIO_LAD_2	AD16	LPC_LAD<2>	
156< 137> IN	LPC_FRAME_N	AG16	SIO_LFRAME_N	SIO_LAD_1	AE16	LPC_LAD<1>	
				SIO_LAD_0	AG17	LPC_LAD<0>	
				SIO_SERIRQ	AE14	IRQ_SERIAL	BI 138<> 147> 156> 156<>
				SIO_SCI_N	AE15	FM_IBMC_SSB_LDRQ_N	OUT 137<
				SIO_SMI_N	AD15	FM_IBMC_SSB_SMI_LPC_N	OUT 138< 147>
184> BI	V_M_IBMC_DDR3_DQ<15..0>			DDR_DQS_P_1	U1	V_M_IBMC_DDR3_DQS1_P	BI 184<>
				DDR_DQS_N_1	V1	V_M_IBMC_DDR3_DQS1_N	BI 184<>
				DDR_DQS_P_0	N1	V_M_IBMC_DDR3_DQS0_P	BI 184<>
				DDR_DQS_N_0	P1	V_M_IBMC_DDR3_DQS0_N	BI 184<>
				DDR_BNK_2	F1	V_M_IBMC_DDR3_BA2	OUT 184<
				DDR_BNK_1	L4	V_M_IBMC_DDR3_BA1	OUT 184<
				DDR_BNK_0	F3	V_M_IBMC_DDR3_BA0	OUT 184<
				DDR_DM_1	AA1	V_M_IBMC_DDR3_DM1	OUT 184<
				DDR_DM_0	T4	V_M_IBMC_DDR3_DM0	OUT 184<
				DDR_RST_N	J4	V_M_IBMC_DDR3_RST_N	OUT 184<
15	V_M_IBMC_DDR3_DQ<15>	W3	DDR_DQ_15	DDR_MA_15	M1	V_M_IBMC_DDR3_MA<15>	15 V_M_IBMC_DDR3_MA<15..0> OUT 184< 185<
14	V_M_IBMC_DDR3_DQ<14>	W2	DDR_DQ_14	DDR_MA_14	F4	V_M_IBMC_DDR3_MA<14>	14
13	V_M_IBMC_DDR3_DQ<13>	W1	DDR_DQ_13	DDR_MA_13	K3	V_M_IBMC_DDR3_MA<13>	13
12	V_M_IBMC_DDR3_DQ<12>	V3	DDR_DQ_12	DDR_MA_12	L1	V_M_IBMC_DDR3_MA<12>	12
11	V_M_IBMC_DDR3_DQ<11>	Y1	DDR_DQ_11	DDR_MA_11	G4	V_M_IBMC_DDR3_MA<11>	11
10	V_M_IBMC_DDR3_DQ<10>	U4	DDR_DQ_10	DDR_MA_10	M3	V_M_IBMC_DDR3_MA<10>	10
9	V_M_IBMC_DDR3_DQ<9>	V4	DDR_DQ_9	DDR_MA_9	K1	V_M_IBMC_DDR3_MA<9>	9
8	V_M_IBMC_DDR3_DQ<8>	V2	DDR_DQ_8	DDR_MA_8	G3	V_M_IBMC_DDR3_MA<8>	8
7	V_M_IBMC_DDR3_DQ<7>	R4	DDR_DQ_7	DDR_MA_7	M4	V_M_IBMC_DDR3_MA<7>	7
6	V_M_IBMC_DDR3_DQ<6>	R1	DDR_DQ_6	DDR_MA_6	J3	V_M_IBMC_DDR3_MA<6>	6
5	V_M_IBMC_DDR3_DQ<5>	P4	DDR_DQ_5	DDR_MA_5	K2	V_M_IBMC_DDR3_MA<5>	5
4	V_M_IBMC_DDR3_DQ<4>	P2	DDR_DQ_4	DDR_MA_4	J2	V_M_IBMC_DDR3_MA<4>	4
3	V_M_IBMC_DDR3_DQ<3>	R2	DDR_DQ_3	DDR_MA_3	G2	V_M_IBMC_DDR3_MA<3>	3
2	V_M_IBMC_DDR3_DQ<2>	T1	DDR_DQ_2	DDR_MA_2	J1	V_M_IBMC_DDR3_MA<2>	2
1	V_M_IBMC_DDR3_DQ<1>	T2	DDR_DQ_1	DDR_MA_1	K4	V_M_IBMC_DDR3_MA<1>	1
0	V_M_IBMC_DDR3_DQ<0>	R3	DDR_DQ_0	DDR_MA_0	G1	V_M_IBMC_DDR3_MA<0>	0
		T3	DDR_VREF	DDR_RAS_N	C1	V_M_IBMC_DDR3_RAS_N	OUT 184<
		H1	DDR_ADR_VREF	DDR_CS_N	F2	V_M_IBMC_DDR3_CS_N	OUT 184<
				DDR_CAS_N	E2	V_M_IBMC_DDR3_CAS_N	OUT 184<
				DDR_WE_N	H4	V_M_IBMC_DDR3_WE_N	OUT 184<
				DDR_CKE	M2	V_M_IBMC_DDR3_CKE	OUT 184<
				DDR_CLKP	N4	V_M_IBMC_DDR3_CLK_DP	OUT 184<
				DDR_CLKN	N3	V_M_IBMC_DDR3_CLK_DN	OUT 184<
	PU_IBMC_DDR_BZ_DRV_TRIM0	D1	DDR_BZ_DRV_TRIM0				
	PD_IBMC_DDR_BZ_DRV_TRIM1	E3	DDR_BZ_DRV_TRIM1				
	PU_IBMC_DDR_BZ_ODT_TRIM	E4	DDR_BZ_ODT_TRIM				
184< OUT	V_M_IBMC_DDR3_ODT	E1	DDR_ODT				
32> IN	CLK_50M_IBMCA	B16	MAC0_REF_CLK	MAC_MDC	C15	RMII_IBMC_MAC_MDC	R9L22 A93548-054 1% 1/16W 0402LF 22.1 RMII_IBMC_MAC_R_MDC OUT 197<
				MAC_MD_IO	A17	RMII_IBMC_MAC_MDIO	R8L56 22.1 RMII_IBMC_MAC_R_MDIO BI 197<>
197> IN	RMII_IBMC_RMM3_RX_DV	B17	MAC0_RX_DV	MAC0_TX_EN	D17	RMII_IBMC_RMM3_TX_EN	R8L48 0 5% 1/16W 0402LF A93549-001 RMII_IBMC_RMM3_TX_R_EN OUT 197<
197> IN	RMII_IBMC_RMM3_RX_ER	A15	MAC0_RX_ER	MAC0_TXD_3	D13	TP_IBMC_MAC0_TXD_3	
	TP_IBMC_MAC0_RXD_3	D14	MAC0_RXD_3	MAC0_TXD_2	B15	TP_IBMC_MAC0_TXD_2	
	TP_IBMC_MAC0_RXD_2	A16	MAC0_RXD_2	MAC0_TXD_1	C16	RMII_IBMC_RMM3_TXD<1>	R8L49 39.0 RMII_IBMC_RMM3_R_TXD<1> OUT 197<
197> IN	RMII_IBMC_RMM3_RXD<1>	D16	MAC0_RXD_1	MAC0_TXD_0	D15	RMII_IBMC_RMM3_TXD<0>	R8L50 39.0 RMII_IBMC_RMM3_R_TXD<0> OUT 197<
197> IN	RMII_IBMC_RMM3_RXD<0>	C17	MAC0_RXD_0				5% 1/16W 0402LF A93549-075 IN 183>
	PU_IBMC_GFX_VREF	AB24	GFX_VREF	GFX_HSYNC	AE24	V_IBMC_GFX_HSYN	OUT 182<
	PD_IBMC_GFX_RSET	AD25	GFX_RSET	GFX_VSYNC	AD23	V_IBMC_GFX_VSYN	OUT 182<
		AD26	IORET_CUR_R	GFX_RED	AC24	V_IBMC_GFX_RED	OUT 182<
		AE27	IORET_CUR_G	GFX_GREEN	AC25	V_IBMC_GFX_GRN	OUT 182<
		AC26	IORET_CUR_B	GFX_BLUE	AD27	V_IBMC_GFX_BLU	OUT 182<
				GFX_DDC_SDA	AG25	V_IBMC_DDC_SDA	BI 189<>
				GFX_DDC_SDC	AE23	V_IBMC_DDC_SCL	OUT 189<

P0V75_STBY_IBMC_DDR_VREF

C9L45 0.1UF 16V 10% 0402LF — A36096-030 — C9L37 0.1UF 16V 10% 0402LF

C9L32 0.01UF 25V 10% 0402LF — A36096-045

R9L21 44.2 1% 1/16W 0402 — A93548-497

P1V5_STBY_IBMC

R9L24 294 1% 1/16W 0402LF — A93548-158

R9L23 44.2 1% 1/16W 0402 — A93548-497

P3V3_STBY

A93548-023 R8M33 1K 1/16W 0402LF 1%

U2B3 — LM385 D11618-001

C8M37 0.1UF 16V 10% 0402LF — A36096-030

R2B33 2.0K 1% 1/16W 0402LF — A93548-138

CAD NOTE:
TIE PINS TOGETHER
AND THEN TO GND

1/6

E68397-001

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IBMC (PAGE 1 OF 6)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 175 OF 303	

INTEL CONFIDENTIAL

ROOM=IBMC

U1A1

PILOT_III_D

		TP_IBMC_GPIO_15	D10	GPIO_15			
169>	IN	FM_IBMC_PS_PWROK_LVC3	A10	GPIO_14	GPIO_14_4	C5	TP_IBMC_GPIO_14_4
186<	OUT	FM_IBMC_FLASH_WP_N	A9	GPIO_13	GPIO_14_3	A3	PU_IBMC_GPIO_14_3
197>	IN	FM_RMM3_PRSNT_N	C11	GPIO_12	GPIO_14_2	A4	PU_IBMC_GPIO_14_2
		NC_IBMC_GPIO_11	B10	GPIO_11	GPIO_14_1	D5	PU_IBMC_GPIO_14_1
		FM_BMC_LAN1_DISABLE_N	B11	GPIO_10	GPIO_14_0	B5	PU_IBMC_GPIO_14_0
224<	OUT	TP_ID_BTN_CO_N	D11	GPIO_9	GPIO_31	D6	CLK_50M_IBMCB
		FP_NMI_BTN_CO_N	C12	GPIO_8	GPIO_30	D7	PD_RMII_IBMC_LAN_RX_ER
229>	IN	FM_VIDEO_DISABLE_N	D12	GPIO_7	GPIO_29	B4	RMII_NIC_IBMC_CRS_DV
136>	IN	SPEAKER_IBMC	A12	GPIO_6	GPIO_28	B6	RMII_NIC_IBMC_RXD<0>
191<	OUT	FM_BIOS_POST_CMPLT_N	A11	GPIO_5	GPIO_27	C6	RMII_NIC_IBMC_RXD<1>
188< 168<	IN	IRQ_SML0_ALERT_N	C13	GPIO_4	GPIO_26	C7	RMII_IBMC_NIC_TXD<0>
190> 188< 139>	IN	FM_SMI_ACTIVE_N	B12	GPIO_3	GPIO_25	A5	RMII_IBMC_NIC_TXD<1>
190> 136>	IN	TP_ID_LED_N	A13	GPIO_2	GPIO_24	B7	RMII_IBMC_NIC_TX_EN
		FM_FORCE_IBMC_UPDATE_N	B13	GPIO_1	GPIO_23	D8	FAN_IBMC_TACH11
180>	IN	FM_NMI_EVENT_N	A14	GPIO_0	GPIO_22	A8	FAN_IBMC_TACH10
190> 168<	IN				GPIO_21	A6	FAN_IBMC_TACH9
					GPIO_20	C9	FAN_IBMC_TACH8
					GPIO_19	A7	PD_FAN_IBMC_PWM7
					GPIO_18	B9	PD_FAN_IBMC_PWM6
					GPIO_17	D9	FAN_IBMC_PWM5
					GPIO_16	C10	FAN_IBMC_PWM4

1% 1/16W A93548-054

R1A43 1 2 22.1 RMII_IBMC_NIC_R_TXD<0>

R8M9 1 2 22.1 RMII_IBMC_NIC_R_TXD<1>

R1A44 1 2 22.1 RMII_IBMC_NIC_TX_R_EN

216>	IN	A_PV_VCCP_CPU3_SENSOR	AA25	AVIN_14			
216>	IN	A_P1V1_STBY_PBG_SENSOR	W24	AVIN_13			
216>	IN	A_P1V8_STBY_IBMC_SENSOR	AA26	AVIN_12			
216>	IN	A_P1V5_DDR3_CPU3_SENSOR	W25	AVIN_11			
216>	IN	A_P1V5_DDR3_CPU2_SENSOR	AA27	AVIN_10			
216>	IN	A_P1V5_DDR3_CPU1_SENSOR	V24	AVIN_9			
216>	IN	A_P1V5_DDR3_CPU0_SENSOR	Y27	AVIN_8			
216>	IN	A_PV_VCCP_CPU1_SENSOR	W26	AVIN_7			
216>	IN	A_PV_VCCP_CPU0_SENSOR	U24	AVIN_6			
216>	IN	A_PV_VCCP_CPU2_SENSOR	V26	AVIN_5			
216>	IN	A_P3V3_STBY_SCALED	V27	AVIN_4			
216>	IN	A_P5V_STBY_SCALED	U25	AVIN_3			
216>	IN	A_P3V3_SCALED	U26	AVIN_2			
216>	IN	A_P5V_SCALED	T24	AVIN_1			
216>	IN	A_P12V_SCALED	U27	AVIN_0			
216>	IN	A_P3V_BAT	AB27	AVIN_BAT_15			
28>	IN	CLK_48M_USB_IBMC	AE5	USB_CLK			
191<>	BI	USB_03_R_DP	AG3	USB0_DP	USB0_DISCON	AG4	USB_IBMC_DISCON
191<>	BI	USB_03_R_DN	AF3	USB0_DN			
140<>	BI	USB2_13_DP	AG7	USB1_DP			
140<>	BI	USB2_13_DN	AF7	USB1_DN			
191>	IN	USB_IBMC_REXT	AD8	USB1_REXT			
		TP_IBMC_NAND_RB_N	R26	NAND_RB_N	NAND_ALE	L25	FM_IBMC_NAND_ALE
188>	IN	FM_IBMC_DEBUG_CARD_PRES_N	R27	NAND_DQ_7_GPIO_PORT20_7	NAND_CE_2	L27	TP_IBMC_NAND_CE_2
147> 139>	IN	FM_SSB_IBMC_THERMTRIP_N	P27	NAND_DQ_6_GPIO_PORT20_6	NAND_CE_1	L26	TP_IBMC_NAND_CE_1
169< 148< 130< 99>	IN	IRQ_CPU_CATERR_LVC3_N	N27	NAND_DQ_5_GPIO_PORT20_5	NAND_CE_0	L24	TP_IBMC_NAND_CE_0
129< 78>	IN	FM_ERR2_LVC3_N	N24	NAND_DQ_4_GPIO_PORT20_4			
148<	OUT	IRQ_IBMC_SSB_NMI_STBY	N26	NAND_DQ_3_GPIO_PORT20_3	NAND_CLE	M25	PD_IBMC_NAND_CLE
231> 188< 169< 136<	IN	IRQ_SML1_PMBUS_ALERT_N	N25	NAND_DQ_2_GPIO_PORT20_2	NAND_CLK	M26	PD_IBMC_NAND_CLK
		TP_NAND_DQ_1	M27	NAND_DQ_1_GPIO_PORT20_1			
		TP_NAND_DQ_0	M24	NAND_DQ_0_GPIO_PORT20_0			
		TP_IBMC_NAND_DQS	P24	NAND_DQS	NAND_WP_N	R25	PD_IBMC_NAND_WP_N
					NAND_WR_N	R24	PD_IBMC_NAND_WR_N
		TP_IBMC_SD_DATA_3	C24	SD_DATA_3	SD_CLK	D25	SPI_IBMC_RMM3_CLK
		TP_IBMC_SD_DATA_2	C25	SD_DATA_2	SD_CMD	C27	SPI_IBMC_RMM3_DO
197> IN	SPI_IBMC_RMM3_DI		B25	SD_DATA_1	SD_CD	E25	TP_IBMC_SD_CD
197< OUT	SPI_IBMC_RMM3_CS_R_N		C26	SD_DATA_0	SD_WP	D22	TP_IBMC_SD_WP

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	IN	190>					
	IN	190>					
	IN	190>					
	IN	190>					
	IN	32>					
	IN	190>					
	IN	219>	224>				
	IN	219>	224>				
	IN	219>	224>				
	OUT	219<	224>				
	OUT	219<	224>				
	OUT	219<	224>				
	IN	211>					
	IN	211>					
	IN	211>					
	IN	211>					
	IN	189>					
	IN	189>					
	OUT	189>	193<				
	OUT	189>	193<				

P3V3_STBY

R9M19 15K 1% 1/16W A93548-132 0402LF

Q1B1 MMBT3906 SMLF C73455-001

USB_IBMC_DISC_B

R1B19 1.50K 1% 1/16W A93548-014 0402LF

USB_IBMC_DISC_C

R9M20 1K 1% 1/16W A93548-023 0402LF

USB_03_DP BI 140<> 191<>

R2A50 33 1% 1/16W A93548-503 0402LF

A93548-503 0402LF

R8L54 1 2 33 SPI_IBMC_RMM3_CLK_R OUT 197<

R8L52 1 2 33 SPI_IBMC_RMM3_DO_R OUT 197<

1% 1/16W

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ROOM=IBMC

U1A1

PILOT_III_D

P3V3_STBY

R8M35 150 1% 1/16W A93548-293 0402LF

CAD NOTE: TO BE CLEAR FOR FUTURE PRODUCT REFERENCE

P2V5_IBMC_AVREF

C8M38 0.1UF 16V 10% X36096-030 0402LF

U8M1 LM4040 D11613-001

ADC_AVREEP T26
ADC_AVREFN T25

SDA_7	F26	SMB_PMBUS_IBMC_STBY_LVC3_DATA	BI	190<> 231<>
SDC_7	D26	SMB_PMBUS_IBMC_STBY_LVC3_CLK	OUT	190> 231<
SDA_6	G26	SMB_GS_STBY_LVC3_DATA	BI	190<>
SDC_6	D27	SMB_GS_STBY_LVC3_CLK	OUT	190>
SDA_5	F27	SMB_LAN_STBY_LVC3_DATA	BI	139<> 190<> 219<>
SDC_5	F24	SMB_LAN_STBY_LVC3_CLK	OUT	139<> 190> 219<>
SDA_4	G27	SMB_SMLINK0_STBY_LVC3_DATA	BI	139<> 188<> 190<>
SDC_4	F25	SMB_SMLINK0_STBY_LVC3_CLK	OUT	139<> 188< 190>
SDA_3	H24	SMB_HOST_STBY_LVC3_DATA	BI	32<> 139<> 188<> 190<> 202<>
SDC_3	E26	SMB_HOST_STBY_LVC3_CLK	OUT	32< 139<> 188< 190> 202<
SDA_2	H27	SMB_PCI_STBY_LVC3_DATA	BI	190<>
SDC_2	E27	SMB_PCI_STBY_LVC3_CLK	OUT	190>
SDA_1	J24	SMB_SENSOR_STBY_LVC3_DATA	BI	190<> 202<> 217<> 229<>
SDC_1	G24	SMB_SENSOR_STBY_LVC3_CLK	OUT	190> 202< 217< 229<
SDA_0	J26	SMB_IPMB_STBY_LVC3_DATA	BI	190<> 203<>
SDC_0	G25	SMB_IPMB_STBY_LVC3_CLK	OUT	190> 203<>
			IN	183> 187>

207> IN SGPIO_IBMC_DIN_LVC3 — R8M23 33 1% 1/16W A93548-503 0402LF — SGPIO_IBMC_DIN_R_LVC3 AE19 — SGPIO_DIN

SGPIO_CLK
SGPIO_DOUT
SGPIO_LD

AF21	SGPIO_IBMC_CLK_LVC3	R2B24 33	SGPIO_IBMC_CLK_R_LVC3	OUT 204< 206<
AG21	SGPIO_IBMC_DATOUT_LVC3	R2B23 33	SGPIO_IBMC_DATOUT_R_LVC3	OUT 204<
AF19	SGPIO_IBMC_LD_LVC3_N	R2B25 33	SGPIO_IBMC_LD_R_LVC3_N	OUT 204< 206<
				IN 183>

186> IN SPI_IBMC_BT_DI_R W4 — BMC_BOOT_SPI_DI

BMC_BOOT_SPI_CLK
BMC_BOOT_SPI_CS2_N
BMC_BOOT_SPI_CS1_N
BMC_BOOT_SPI_CS0_N
BMC_BOOT_SPI_DO

AA2	SPI_IBMC_BT_CLK	R1B9 33	SPI_IBMC_BT_CLK_R	OUT 186<
AA4	NC_IBMC_BOOT_SPI_CS2_N			
AA3	NC_IBMC_BOOT_SPI_CS1_N			
AB2	SPI_IBMC_BT_CS_N	R9M16 33	SPI_IBMC_BT_CS_R_N	OUT 186<
Y4	SPI_IBMC_BT_DO	R9M9 33	SPI_IBMC_BT_DO_R	OUT 186<
				IN 183>

DEFAULT GPIO INPUT & INTERNAL PULL-UP

TP_IBMC_HOST_SPI_DI AC1 — SIO_HOST_SPI_DI

SIO_HOST_SPI_CLK
SIO_HOST_SPI_CS_N
SIO_HOST_SPI_DO

AB3	PD_IBMC_HOST_SPI_CLK		IN 183>
AC3	TP_IBMC_HOST_SPI_CS_N		
AC2	TP_IBMC_HOST_SPI_DO	DEFAULT GPIO INPUT & INTERNAL PULL-UP	

192> 178< IN RST_RSMRST_BUF_R_N AC27 — VSBPWR_GD

219< 219> 204< 169> 147> 135< IN PWRGD_PCH_PWROK_LVC3 AE7 — VDDPWR_GD

169< 135> 129< IN FM_SLPS3_LVC3_N AF17 — SIO_SLPS3_N

230< 169< 135> 129< IN FM_SLPS4_LVC3_N AE17 — SIO_SLPS5_N

178> IN FM_IBMC_PWR_BTN_N AF18 — SIO_PWRBTIN_N

230> IN FM_INTRUDER_HDR_CO_N AB25 — CHASI_N

32> IN CLK_25M_IBMC_XTAL_SE AD7 — XT1_1

NC_IBMC_XT2_1 AF6 — XT2_1

SIO_PWRREQ_N
SIO_ONCTL_N
SIO_PWRBTOUT_N

AG18	FM_IBMC_SSB_SCI_LPC_N			OUT 136< 147>
AD18	FM_CPLD_PSON_LVC3_N	R2B26 33	FM_CPLD_PSON_R_LVC3_N	OUT 169<
AD17	FM_IBMC_PWRBTN_OUT_N			OUT 135<

ICMB_TX_EN

T27	TP_IBMC_ICBM_TX_EN	

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ROOM=IBMC

U1A1

PILOT_III_D

211> IN	FAN_IBMC_TACH3	J27	BMC_FAN_TACH_3						
211> IN	FAN_IBMC_TACH2	K26	BMC_FAN_TACH_2						
211> IN	FAN_IBMC_TACH1	K24	BMC_FAN_TACH_1						
211> IN	FAN_IBMC_TACH0	K27	BMC_FAN_TACH_0						
				BMC_PWM_1	J25	FAN_IBMC_PWM1	OUT	189>	192<
				BMC_PWM_0	K25	FAN_IBMC_PWM0	OUT	189>	192<
194> IN	SPA_CTS_N	D23	UART0_CTS_N						
194> IN	SPA_DCD_N	A24	UART0_DCD_N						
194> IN	SPA_DSR_N	B24	UART0_DSR_N						
194> IN	SPA_RI_N	A25	UART0_RI_N						
194> IN	SPA_SIN	C23	UART0_RXD						
				UART0_DTR_N	C22	SPA_DTR_N	OUT	183>	194<
				UART0_RTS_N	A23	SPA_RTS_N	OUT	183>	194<
				UART0_TXD	D20	SPA_SOUT	OUT	194<	
195> IN	SPB_CTS_N	B23	UART1_CTS_N						
195> IN	SPB_DCD_N	B21	UART1_DCD_N						
195> IN	SPB_DSR_N	D21	UART1_DSR_N						
190> IN	PU_SPB_RI_N	B22	UART1_RI_N						
195> IN	SPB_SIN	C21	UART1_RXD						
				UART1_DTR_N	D19	SPB_DTR_N	OUT	183>	195<
				UART1_RTS_N	A20	SPB_RTS_N	OUT	183>	195<
				UART1_TXD	B19	SPB_SOUT	OUT	183>	195<
211> IN	FAN_IBMC_TACH4	C18	UART2_CTS_N						
211> IN	FAN_IBMC_TACH5	B18	UART2_DCD_N						
211> IN	FAN_IBMC_TACH6	C19	UART2_DSR_N						
211> IN	FAN_IBMC_TACH7	A19	UART2_RI_N						
187> IN	FM_IBMC_UART2_RXD	A18	UART2_RXD						
				UART2_DTR_N	A22	FAN_IBMC_PWM2	OUT	189>	192<
				UART2_RTS_N	D18	FAN_IBMC_PWM3	OUT	189>	192<
				UART2_TXD	A21	FM_IBMC_UART2_TXD	OUT	183>	187<
	TP_IBMC_SIO_WATCHDOG	AE18	UART3_RXD						
				UART3_TXD	AG19	PD_IBMC_UART3_TXD	IN	183>	
190> IN	PU_IBMC_PASSTHRUIN2	AE22	PASSTHRUIN2						
229> 169> IN	FP_PWR_BTN_CO_N	AF22	PASSTHRUIN1						
229> IN	FP_RST_BTN_CO_N	AE21	PASSTHRUIN0						
				PASSTHRUOUT2	AD21	NC_IBMC_PASSTHRUOUT2			
				PASSTHRUOUT1	AG22	FM_IBMC_PWR_BTN_N	OUT	177<	
				PASSTHRUOUT0	AD20	RST_IBMC_RSTBTN_OUT_N	OUT	148<	168<
	TP_IBMC_MFG_IDDT	AD6	MFG_IDDT						
	TP_IBMC_MFG_PROCMON	AD3	MFG_PROCMON						
	TP_IBMC_MFG_SCAN_ENABLE	AG5	MFG_SCAN_ENABLE						
	TP_IBMC_MFG_TN	AF5	MFG_TN						
187> IN	JTAG_IBMC_TCK	AE1	MFG_CW_TAP_TCK						
187> IN	JTAG_IBMC_TDI	AC4	MFG_CW_TAP_TDI						
187> IN	JTAG_IBMC_TMS	AD1	MFG_CW_TAP_TMS						
192> 177< IN	RST_RSMRST_BUF_R_N	AB4	MFG_CW_TAP_TRSTN						
IN	TP_IBMC_MFG_CW_TAP	AF1	MFG_CW_TAP						
				MFG_CW_TAP_TDO	AE2	JTAG_IBMC_TDO	R9M18 1% 1/16W A93548-503 0402LF 33 JTAG_IBMC_TDO_R	OUT	187<
				PECI_VTT	AG23				
				PECI	AF23	PECI_IBMC_LVC1	BI	196<>	
190> IN	PD_IBMC_TEST_BUS_EN	AD19	TEST_BUS_EN						
190> IN	PU_IBMC_RSVD0	AG20	RSVD0						

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P1V05_VTT_CPU0

C9L33 1.0UF 10% 6.3V A36096-027 0402LF

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DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
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U1A1

PILOT_III_D

P1V0_STBY_IBMC

P1V5_STBY_IBMC

P3V3_STBY

P3V3_VBAT

L12	VDD<22>	VDDIO_DDR<11>	D2		
L14	VDD<21>	VDDIO_DDR<10>	G5		
L16	VDD<20>	VDDIO_DDR<9>	H3		
M11	VDD<19>	VDDIO_DDR<8>	H5		
M13	VDD<18>	VDDIO_DDR<7>	L3		
M15	VDD<17>	VDDIO_DDR<6>	N5		
M17	VDD<16>	VDDIO_DDR<5>	P3		
N12	VDD<15>	VDDIO_DDR<4>	P5		
N14	VDD<14>	VDDIO_DDR<3>	U3		
N16	VDD<13>	VDDIO_DDR<2>	Y3		
P11	VDD<12>	VDDIO_DDR<1>	Y5		
P13	VDD<11>	VDDIO_DDR<0>	AA5		
P15	VDD<10>				
P17	VDD<9>	USB1_VDD33	AD9	P3V3_USB_VDD33	IN 179>
R12	VDD<8>	USB0_VDD33	AF4		
R14	VDD<7>				
R16	VDD<6>				
T11	VDD<5>	PECL_VDDIO	AE9	P1V0_PECLVDDIO	IN 179>
T13	VDD<4>	PCIE_TXVTERM2	AD14	P1V8_PCIE_TXVTERM	IN 179>
T15	VDD<3>	PCIE_TXVTERM1	AE11		IN 179>
T17	VDD<2>	PCIE_TXVCOVDD	AE13	P1V8_PCIE_TXVCOVDD	IN 179>
U12	VDD<1>				
U16	VDD<0>	PIX_PLL_VDD	E24	P1V8_PIX_PLL_VDD	IN 179>
AC15	VDDIO33_1<30>				
AC20	VDDIO33_1<29>				
AC23	VDDIO33_1<28>	PCIE_AVDD<3>	AD13	P1V0_AVDD	IN 179>
AC5	VDDIO33_1<27>	PCIE_AVDD<2>	AD11		
AC8	VDDIO33_1<26>	PCIE_AVDD<1>	AC14		
AD2	VDDIO33_1<25>	PCIE_AVDD<0>	AC11		
AE20	VDDIO33_1<24>				
AE25	VDDIO33_1<23>	DAC_AVDD<1>	Y23	P3V3_DAC_AVDD	IN 179>
AE3	VDDIO33_1<22>	DAC_AVDD<0>	W23		
AE4	VDDIO33_1<21>				
AE8	VDDIO33_1<20>	ADC_AVDD	W27	P3V3_ADC_AVDD	IN 179>
AF14	VDDIO33_1<19>				
C14	VDDIO33_1<18>	BAT_VDD	AA24		
C20	VDDIO33_1<17>				
C8	VDDIO33_1<15>	SYS_PLL_VDD	E9	P1V8_SYS_PLL_VDD	IN 179>
E13	VDDIO33_1<14>				
E20	VDDIO33_1<13>	DDR_PLL_VDD	E6	P1V8_DDR_PLL_VDD	IN 179>
E21	VDDIO33_1<12>				
E23	VDDIO33_1<11>				
E5	VDDIO33_1<10>				
E7	VDDIO33_1<9>				
E8	VDDIO33_1<8>				
H23	VDDIO33_1<7>				
H25	VDDIO33_1<6>				
J23	VDDIO33_1<5>				
N23	VDDIO33_1<4>				
P25	VDDIO33_1<3>				
AF24	VDDIO33_1<2>				
Y25	VDDIO33_1<0>				

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P1V0_STBY_IBMC

179< OUT P1V0_AVDD

693286-021 FB2B9 30 SMLF

C2B10 22UF 6.3V 20% 0603LF (602433-081)
C1B3 0.1UF 16V 10% 0402LF (A36096-030)
C1B2 0.1UF 16V 10% 0402LF (A36096-030)
C1B4 0.01UF 25V 10% 0402LF (A36096-045)

179< OUT P1V0_PECLVDDIO

693286-021 FB9M3 30 SMLF

C9M32 22UF 6.3V 20% 0603LF (602433-081)
C9M35 0.1UF 16V 10% 0402LF (A36096-030)

P1V8_STBY_IBMC

179< OUT P1V8_SYS_PLL_VDD

693286-021 FB9L1 30 SMLF

C9L23 22UF 6.3V 20% 0603LF (602433-081)
C9L20 0.1UF 16V 10% 0402LF (A36096-030)
C9L19 0.1UF 16V 10% 0402LF (A36096-030)
C9L21 0.1UF 16V 10% 0402LF (A36096-030)

179< OUT P1V8_PIX_PLL_VDD

693286-021 FB1A1 30 SMLF

C1A5 22UF 6.3V 20% 0603LF (602433-081)
C1A8 0.1UF 16V 10% 0402LF (A36096-030)
C1A6 0.1UF 16V 10% 0402LF (A36096-030)
C8L56 0.1UF 16V 10% 0402LF (A36096-030)

179< OUT P1V8_PCIE_TXVCOVDD

693286-021 FB9M2 30 SMLF

C9M11 22UF 6.3V 20% 0603LF (602433-081)
C9M20 0.1UF 16V 10% 0402LF (A36096-030)

179< OUT P1V8_PCIE_TXVTERM

693286-021 FB9M1 30 SMLF

C9M16 22UF 6.3V 20% 0603LF (602433-081)
C9M14 0.1UF 16V 10% 0402LF (A36096-030)

179< OUT P1V8_DDR_PLL_VDD

693286-021 FB9L2 30 SMLF

C9L24 22UF 6.3V 20% 0603LF (602433-081)
C9L22 0.1UF 16V 10% 0402LF (A36096-030)

P3V3_STBY

179< OUT P3V3_ADC_AVDD

693286-021 FB2B7 30 SMLF

C2B6 22UF 6.3V 20% 0603LF (602433-081)
C2B2 0.1UF 16V 10% 0402LF (A36096-030)

179< OUT P3V3_USB_VDD33

693286-021 FB2B6 30 SMLF

C8M21 22UF 6.3V 20% 0603LF (602433-081)
C9M19 0.1UF 16V 10% 0402LF (A36096-030)
C9M22 0.1UF 16V 10% 0402LF (A36096-030)

179< OUT P3V3_DAC_AVDD

693286-021 FB2B5 30 SMLF

C2B5 22UF 6.3V 20% 0603LF (602433-081)
C8M9 0.1UF 16V 10% 0402LF (A36096-030)
C8M8 0.1UF 16V 10% 0402LF (A36096-030)
C8M5 0.1UF 16V 10% 0402LF (A36096-030)

ROOM=IBMC

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ROOM=IBMC

U1A1

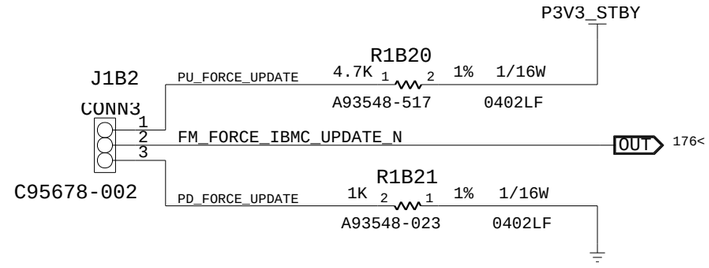
PILOT_III_D

N2	VSS<91>	VSS<40>	R23
A2	VSS<90>	VSS<39>	R5
A26	VSS<89>	VSS<38>	T12
B1	VSS<88>	VSS<37>	T14
B14	VSS<87>	VSS<36>	T16
B2	VSS<86>	VSS<35>	U11
B20	VSS<85>	VSS<34>	U15
B26	VSS<84>	VSS<33>	U17
B27	VSS<83>	VSS<32>	U2
B3	VSS<82>	VSS<31>	W5
B8	VSS<81>	VSS<30>	Y2
C2	VSS<80>	VSS<29>	Y26
C3	VSS<79>	VSS<28>	AA23
C4	VSS<78>	VSS<27>	AB23
D24	VSS<77>	VSS<26>	AB26
D3	VSS<76>	VSS<25>	AB5
D4	VSS<75>	VSS<24>	AC19
E14	VSS<74>	VSS<23>	AC21
E15	VSS<73>	VSS<22>	AC22
E19	VSS<72>	VSS<21>	AC6
E22	VSS<71>	VSS<20>	AC7
AD24	VSS<70>	VSS<19>	AC9
AD5	VSS<69>	VSS<18>	AD22
F23	VSS<68>	VSS<17>	AD4
F5	VSS<67>	VSS<16>	AE10
G23	VSS<66>	VSS<15>	AE6
H2	VSS<65>	VSS<14>	AF10
H26	VSS<64>	VSS<13>	AF12
J5	VSS<63>	VSS<12>	AF2
L11	VSS<62>	VSS<11>	AF20
L13	VSS<61>	VSS<10>	AF25
L15	VSS<60>	VSS<9>	AF26
L17	VSS<59>	VSS<8>	AF27
L2	VSS<58>	VSS<7>	AF8
M12	VSS<57>	VSS<6>	AG10
M14	VSS<56>	VSS<5>	AG12
M16	VSS<55>	VSS<4>	AG14
N11	VSS<54>	VSS<3>	AG2
N13	VSS<53>	VSS<2>	AG24
N15	VSS<52>	VSS<1>	AG26
N17	VSS<51>	VSS<0>	AG6
P12	VSS<50>	ADC_AGND	V25
P14	VSS<49>		
P16	VSS<48>		
AB1	VSS<47>		
P23	VSS<46>	BAT_GND	Y24
P26	VSS<45>		
R11	VSS<44>		
R13	VSS<43>		
R15	VSS<42>	DAC_AGND	AE26
R17	VSS<41>		

6/6

E68397-001

FORCE IBMC UPDATE JUMPER			
JUMPER POSITION	SIGNAL STATE	OPERATION MODE	
1-2	PULLED HIGH	NORMAL	<- DEFAULT
2-3	PULLED DOWN	UPDATE	



IBMC CONFIGURATION

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IBMC (PAGE 6 OF 6)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 180 OF 303	

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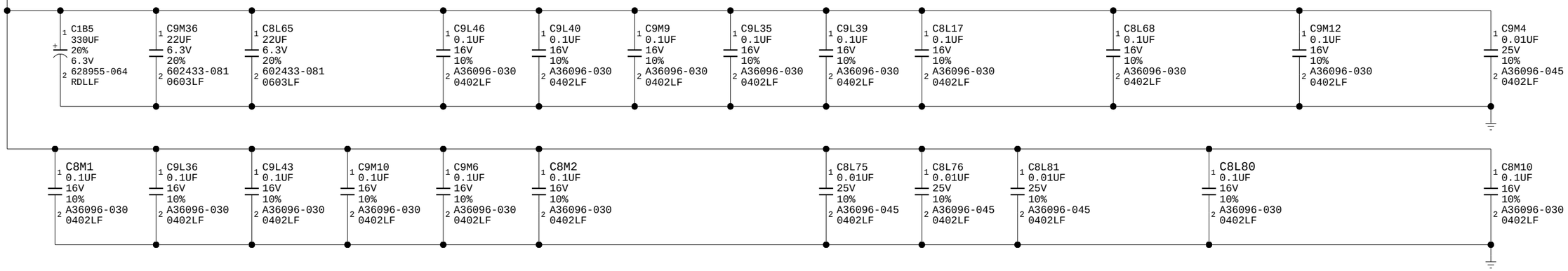
ROOM=IBMC_1V0

P1V0_STBY_IBMC

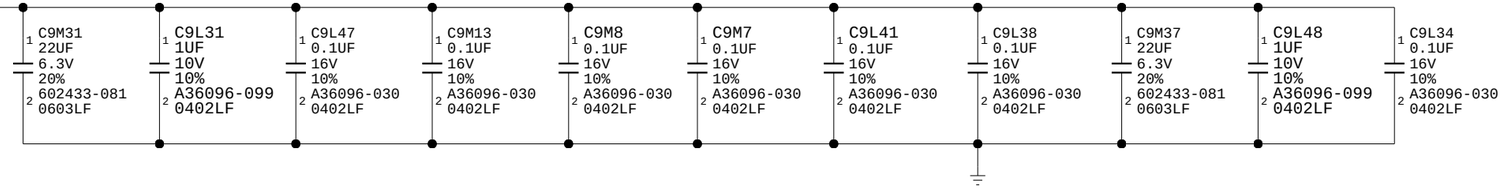
IBMC 1.0V BYPASS



ROOM=IBMC_1V5

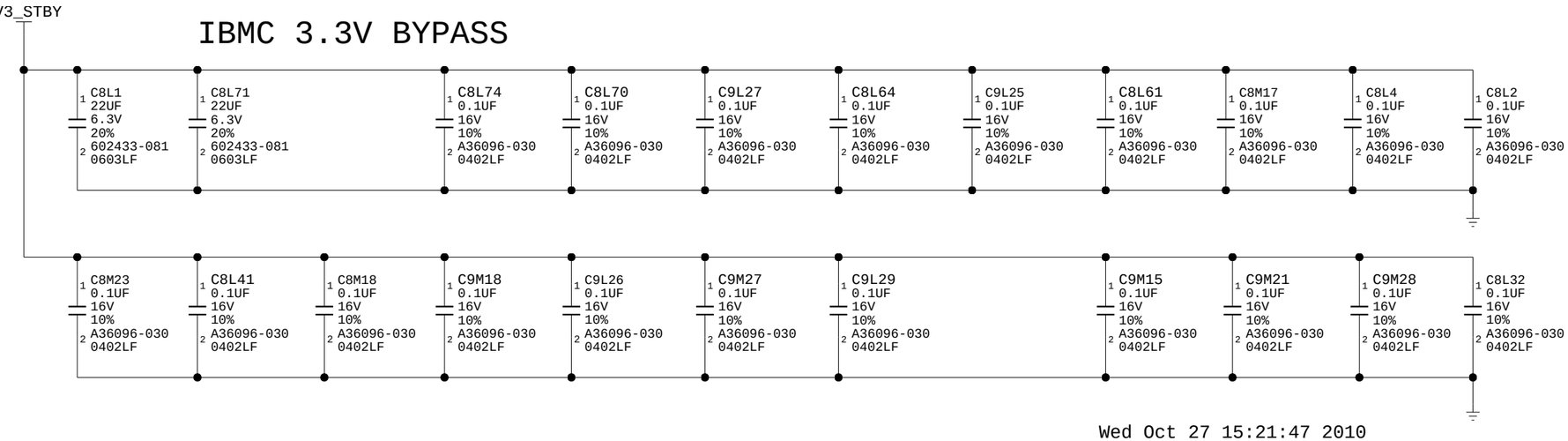
P1V5_STBY_IBMC

IBMC 1.5V BYPASS



P3V3_STBY

IBMC 3.3V BYPASS



ROOM=IBMC_3V3

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IBMC BYPASS CAPS

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 181 OF 303	

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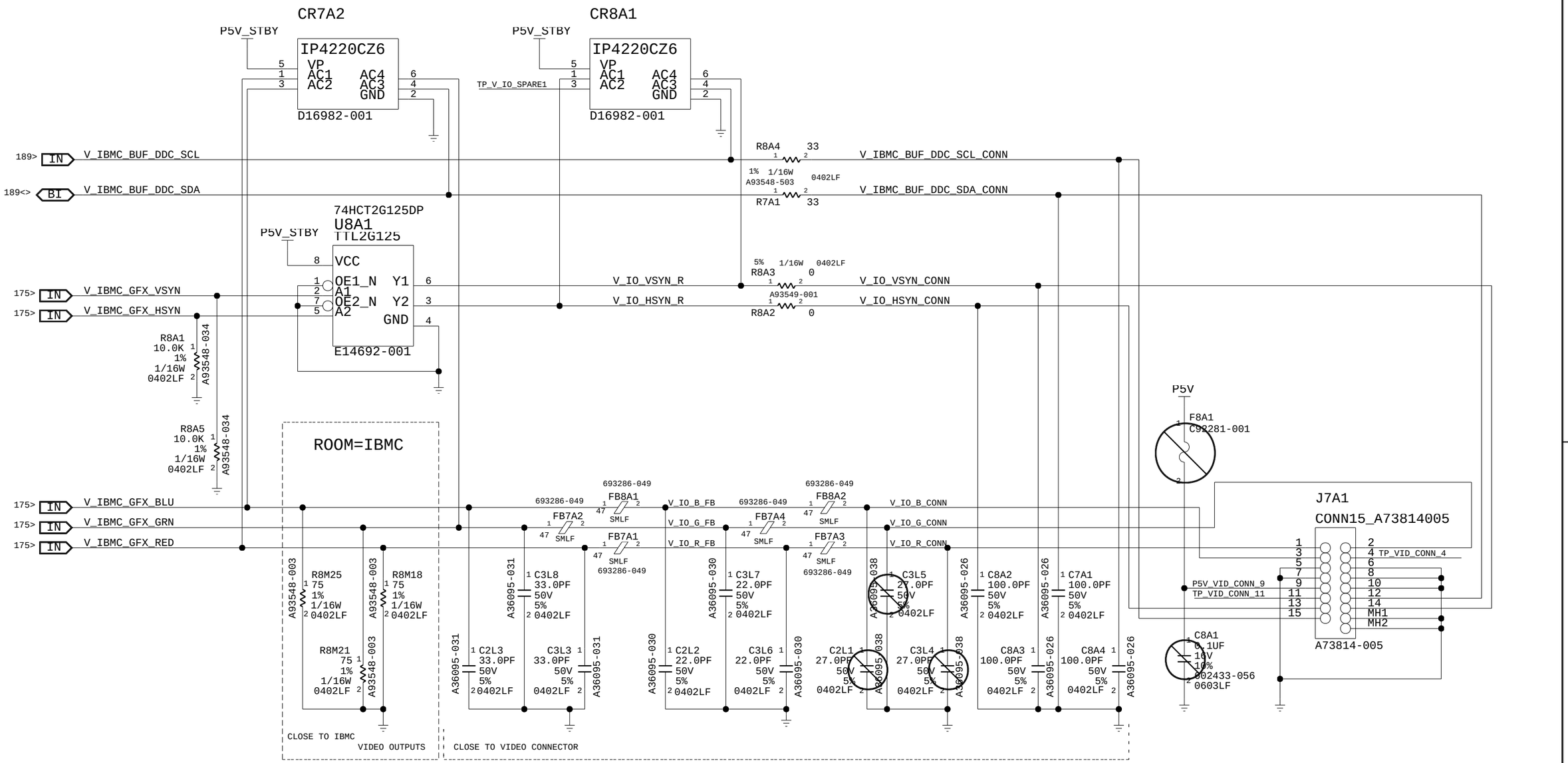

IBMC VIDEO CONNECTOR

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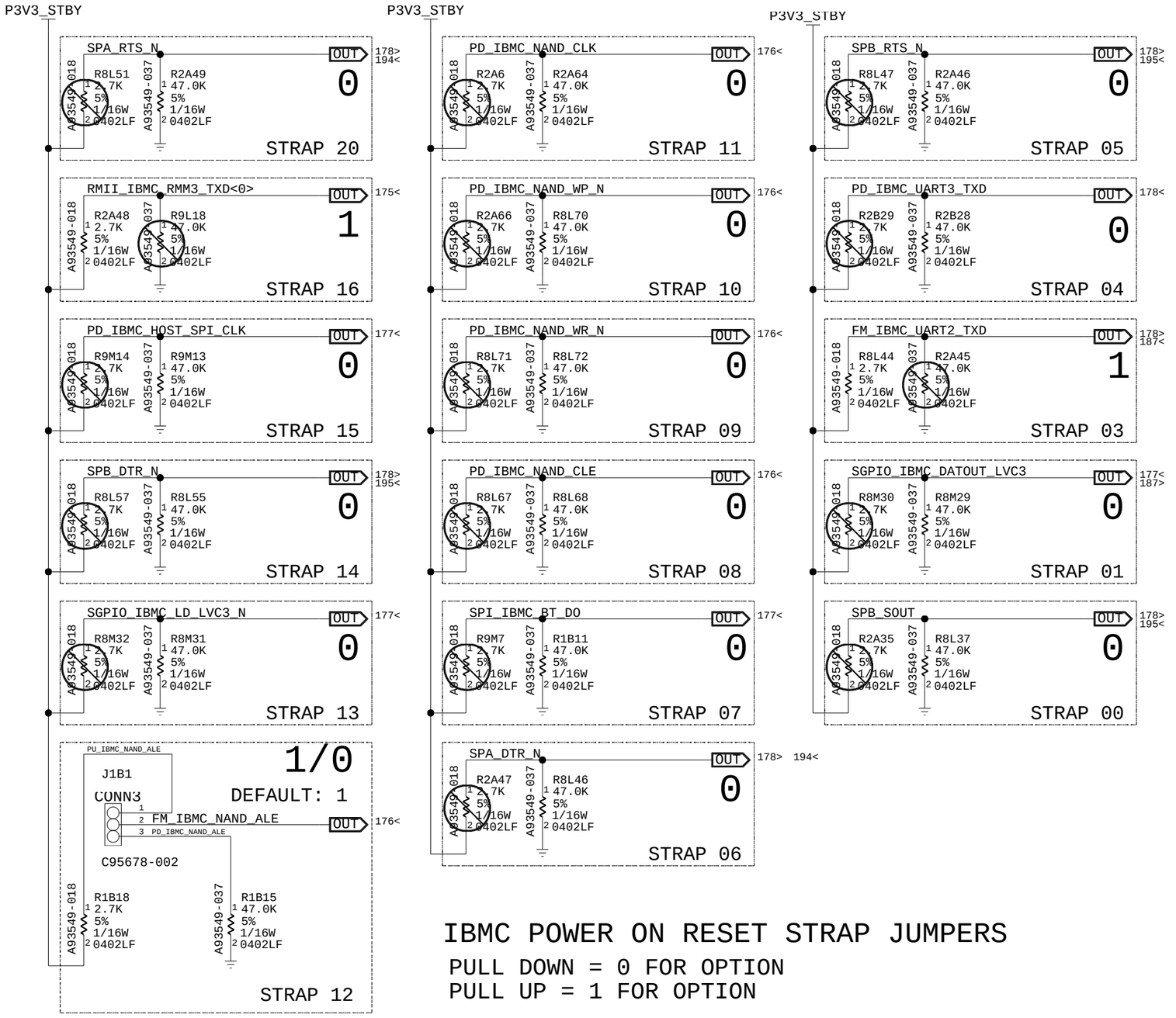
DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 182 OF 303	

INTEL CONFIDENTIAL

IBMC STRAP OPTIONS TABLE (DEFAULT -> @)

STRAP NUM	BALL NUM	BALL NAME	STRAP NAME FUNCTIONAL DESCRIPTION
20	A23	UART0_RTS_N	RGMII_1_MODE_STRAP @ 0: ETHERNET PORT B IS RMII 1: ETHERNET PORT B IS RGMII
19	AC2	SIO_HOST_SPI_DO	RESERVED
18	D17	MAC0_TX_EN	RESERVED
17	C16	MAC0_TXD_1	RESERVED
16 15	D15 AB3	MAC0_TXD_0 SIO_HOST_SPI_CLK	(16)HSPI_SWAP_SIZE_STRAP_1 & (15)HSPI_SWAP_SIZE_STRAP_0 DETERMINE SIZE OF SPI MEMORY ON SPI HOST PORT 00: MEM SIZE 2 MBYTES 01: MEM SIZE 4 MBYTES @ 10: MEM SIZE 8 MBYTES 11: MEM SIZE 16 MBYTES
14	D19	UART1_DTR_N	HSPI_SWAP_EN_STRAP @ 0:USE DEFAULT SYSTEM BIOS IMAGE 1:USE ALTERNATE SYSTEM BIOS IMAGE
13	AF19	SGPIO_LD	HSPI_EN_STRAP @ 0: SIO_HOST_SPI PINS USED AS GPIOS 1: SIO_HOST_SPI INTERFACE SELECTED
12	L25	NAND_ALE	BAR_STRAP 0: LPC HOST INTERFACE ADDRESS 2EH-2FH @ 1: LPC HOST INTERFACE ADDRESS 4EH-4FH
11	M26	NAND_CLK	INT_ACPI_STRAP @ 0: EXTERNAL ACPI CTLR 1: INTERNAL ACPI CTLR
10	R25	NAND_WP_N	EEPROM_STRAP @ 0: OPTION ROM DISABLED 1: OPTION ROM ENABLED
09	R24	NAND_WR_N	RSTBYP_STRAP THIS IS AN INTERNAL OPTION USED DURING MANUFACTURING TEST AND SHOULD BE STRAPPED WITH A PULL- DOWN RESISTOR
08	M25	NAND_CLE	SSPJTAG_STRAP @ 0: JTAG INTERFACE CONNECTED TO ONLY ARM PROCESSOR 1: COMBINES INTERNAL JTAG CHAIN FOR MANUFACTURING TEST
07	Y4	BMC_BOOT_SPI_DO	UART4_STRAP @ 0: SDA_0 & SDC_0 ARE PORT I2C_0 1: SDA_0 & SDC_0 ARE PORT UART4
06	C22	UART0_DTR_N	SDCARD_STRAP @ 0: SD/MMC CARD INTERFACE NOT USED. THE PINS ARE GPIO 1: SD/MMC CARD INTERFACE ENABLED
05	A20	UART1_RTS_N	EXT_BUS_STRAP @ 0: NAND/EXTERNAL BUS INTERFACE NOT USED, PINS ARE GPIO 1: NAND/EXTERNAL BUS INTERFACE IS USED
04	AG19	UART3_TXD	RGMII_0_MODE_STRAP @ 0: ETHERNET PORT A IS RMII 1: ETHERNET PORT A IS RGMII
03	A21	UART2_TXD	MAC1_STRAP CONFIGURE THE ETHERNET PORT B AS GPIO[31:24] PINS 0: THESE PINS ARE USED AS GPIO[31:24] PINS @ 1: ETHERNET PORT B INTERFACE CONFIGURED FOR RMII RGMII_1_MODE_STRAP, MAC1_STRAP 0 0 PINS USED AS GPIOS 0 1 PINS USED AS RMII AND THE ADDITIONAL PINS ARE GPIOS 1 0 ALL MAC1 PINS AND ADDITIONAL PINS ARE USED AS RGMII 1 1 ALL MAC1 PINS AND ADDITIONAL PINS ARE USED AS RGMII
02	D20	UART0_TXD	RESERVED
01	AG21	SGPIO_DOUT	ROM_BOOT_STRAP @ 0: BOOT FROM BMC BOOT SPI INTERFACE 1: BOOT FROM INTERNAL ROM (SCRATCHPAD REGISTERS)
00	B19	UART1_TXD	DDR2_STRAP @ 0: DDR3 DEVICE CONNECTED TO DDR PINS 1: DDR2 DEVICE CONNECTED TO DDR PINS



IBMC POWER ON RESET STRAP JUMPERS

PULL DOWN = 0 FOR OPTION
PULL UP = 1 FOR OPTION

ROOM=IBMC_STRAPS

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IBMC STRAPS

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
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		SCALE:	DO NOT SCALE DRAWING		SHEET 183 OF 303

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IBMC DDR3 MEMORY

U1B1

K4B1G16

P1V5_STBY_IBMC

P0V75_STBY_IBMC

P0V75_STBY_IBMC_DDR_VREF

CAD NOTE: PLACE 49.9 RESISTORS CLOSE TO DDR3 MEMORY

R9M8 49.9 1% 1/16W 0402LF (A93548-045)
R9M10 49.9 1% 1/16W 0402LF (A93548-045)
R1B8 49.9 1% 1/16W 0402LF (A93548-045)
R9M2 49.9 1% 1/16W 0402LF (A93548-045)
R1A50 49.9 1% 1/16W 0402LF (A93548-045)
R9M12 49.9 1% 1/16W 0402LF (A93548-045)
R1B12 49.9 1% 1/16W 0402LF (A93548-045)
R9M15 49.9 1% 1/16W 0402LF (A93548-045)
R1B6 49.9 1% 1/16W 0402LF (A93548-045)

R9M6 1K 1% 1/16W 0402LF (A93548-023)
R1B10 1K 1% 1/16W 0402LF (A93548-023)
R1A53 1K 1% 1/16W 0402LF (A93548-023)
R9M3 240 1% 1/16W 0402 (A93548-504)

C9L44 0.01UF 25V 10% 0402LF (A36096-045)
C9M2 0.1UF 16V 10% 0402LF (A36096-030)

K4B1G16 pin	Net	Connector pin
R9	VDD<8>	
R1	VDD<7>	
N9	VDD<6>	
N1	VDD<5>	
K8	VDD<4>	
K2	VDD<3>	
G7	VDD<2>	
D9	VDD<1>	
B2	VDD<0>	
H9	VDDQ<8>	
H2	VDDQ<7>	
F1	VDDQ<6>	
E9	VDDQ<5>	
D2	VDDQ<4>	
C9	VDDQ<3>	
C1	VDDQ<2>	
A8	VDDQ<1>	
A1	VDDQ<0>	
L9	ZQ1_NC<3>	NC_V_M_ZQ1
L1	CS1_N_NC<2>	NC_V_M_CS1_N
J9	CE1_NC<1>	NC_V_M_CE1
J1	ODT_1NC<0>	NC_V_M_ODT_1
A3	DQU7	V_M_IBMC_DDR3_DQ<15> 15
B8	DQU6	V_M_IBMC_DDR3_DQ<14> 14
A2	DQU5	V_M_IBMC_DDR3_DQ<13> 13
A7	DQU4	V_M_IBMC_DDR3_DQ<12> 12
C2	DQU3	V_M_IBMC_DDR3_DQ<11> 11
C8	DQU2	V_M_IBMC_DDR3_DQ<10> 10
C3	DQU1	V_M_IBMC_DDR3_DQ<9> 9
D7	DQU0	V_M_IBMC_DDR3_DQ<8> 8
B7	DQSU_N	V_M_IBMC_DDR3_DQS1_N
C7	DQSU	V_M_IBMC_DDR3_DQS1_P
G3	DQSL_N	V_M_IBMC_DDR3_DQS0_N
F3	DQSL	V_M_IBMC_DDR3_DQS0_P
H7	DQL7	V_M_IBMC_DDR3_DQ<7> 7
G2	DQL6	V_M_IBMC_DDR3_DQ<6> 6
H8	DQL5	V_M_IBMC_DDR3_DQ<5> 5
H3	DQL4	V_M_IBMC_DDR3_DQ<4> 4
F8	DQL3	V_M_IBMC_DDR3_DQ<3> 3
F2	DQL2	V_M_IBMC_DDR3_DQ<2> 2
F7	DQL1	V_M_IBMC_DDR3_DQ<1> 1
E3	DQL0	V_M_IBMC_DDR3_DQ<0> 0
H1	VREFDQ	
M8	VREFCA	
M7	A15_BA3	V_M_IBMC_DDR3_MA<15> 15
T7	A14	V_M_IBMC_DDR3_MA<14> 14
T3	A13	V_M_IBMC_DDR3_MA<13> 13
N7	A12	V_M_IBMC_DDR3_MA<12> 12
R7	A11	V_M_IBMC_DDR3_MA<11> 11
L7	A10_AP	V_M_IBMC_DDR3_MA<10> 10
R3	A9	V_M_IBMC_DDR3_MA<9> 9
T8	A8	V_M_IBMC_DDR3_MA<8> 8
R2	A7	V_M_IBMC_DDR3_MA<7> 7
R8	A6	V_M_IBMC_DDR3_MA<6> 6
P2	A5	V_M_IBMC_DDR3_MA<5> 5
P8	A4	V_M_IBMC_DDR3_MA<4> 4
N2	A3	V_M_IBMC_DDR3_MA<3> 3
P3	A2	V_M_IBMC_DDR3_MA<2> 2
P7	A1	V_M_IBMC_DDR3_MA<1> 1
N3	A0	V_M_IBMC_DDR3_MA<0> 0
G9	VSSQ<8>	
G1	VSSQ<7>	
F9	VSSQ<6>	
E8	VSSQ<5>	
E2	VSSQ<4>	
D8	VSSQ<3>	
D1	VSSQ<2>	
B9	VSSQ<1>	
B1	VSSQ<0>	
T9	VSS<11>	
T1	VSS<10>	
P9	VSS<9>	
P1	VSS<8>	
M9	VSS<7>	
M1	VSS<6>	
J8	VSS<5>	
J2	VSS<4>	
G8	VSS<3>	
E1	VSS<2>	
B3	VSS<1>	
A9	VSS<0>	
L3	WE_N	V_M_IBMC_DDR3_WE_N
T2	RESET_N	V_M_IBMC_DDR3_RST_N
J3	RAS_N	V_M_IBMC_DDR3_RAS_N
K1	ODT_ODT0	V_M_IBMC_DDR3_ODT
D3	DMU_	V_M_IBMC_DDR3_DM1
E7	DML_	V_M_IBMC_DDR3_DM0
L2	CS_N_CS0_N	V_M_IBMC_DDR3_CS_N
K9	CKE_CKE0	V_M_IBMC_DDR3_CKE
K7	CK_N	V_M_IBMC_DDR3_CLK_DN
J7	CK	V_M_IBMC_DDR3_CLK_DP
K3	CAS_N	V_M_IBMC_DDR3_CAS_N
M3	BA2	V_M_IBMC_DDR3_BA2
N8	BA1	V_M_IBMC_DDR3_BA1
M2	BA0	V_M_IBMC_DDR3_BA0
L8	ZQ_ZQ0	V_M_IBMC_DDR3_ZQ

V_M_IBMC_DDR3_DQ<15..0> BI 175<>

V_M_IBMC_DDR3_MA<15..0> 185< 175> IN

E66291-001

ROOM=IBMC_MEMORY

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IBMC DDR3 MEMORY (1 OF 2)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 184 OF 303	

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RTAD

184< 175> IN V_M_IBMC_DDR3_MA<15:0>

15	V_M_IBMC_DDR3_MA<15>	R1A51	49.9 1% 1/16W A93548-045 0402LF
14	V_M_IBMC_DDR3_MA<14>	R9L28	49.9 1% 1/16W A93548-045 0402LF
13	V_M_IBMC_DDR3_MA<13>	R1A22	49.9 1% 1/16W A93548-045 0402LF
12	V_M_IBMC_DDR3_MA<12>	R9L25	49.9 1% 1/16W A93548-045 0402LF
11	V_M_IBMC_DDR3_MA<11>	R9L27	49.9 1% 1/16W A93548-045 0402LF
10	V_M_IBMC_DDR3_MA<10>	R1A34	49.9 1% 1/16W A93548-045 0402LF
9	V_M_IBMC_DDR3_MA<9>	R1A54	49.9 1% 1/16W A93548-045 0402LF
8	V_M_IBMC_DDR3_MA<8>	R9L29	49.9 1% 1/16W A93548-045 0402LF
7	V_M_IBMC_DDR3_MA<7>	R1A55	49.9 1% 1/16W A93548-045 0402LF
6	V_M_IBMC_DDR3_MA<6>	R9L30	49.9 1% 1/16W A93548-045 0402LF
5	V_M_IBMC_DDR3_MA<5>	R1B4	49.9 1% 1/16W A93548-045 0402LF
4	V_M_IBMC_DDR3_MA<4>	R9M1	49.9 1% 1/16W A93548-045 0402LF
3	V_M_IBMC_DDR3_MA<3>	R1B7	49.9 1% 1/16W A93548-045 0402LF
2	V_M_IBMC_DDR3_MA<2>	R1A52	49.9 1% 1/16W A93548-045 0402LF
1	V_M_IBMC_DDR3_MA<1>	R9L26	49.9 1% 1/16W A93548-045 0402LF
0	V_M_IBMC_DDR3_MA<0>	R1A33	49.9 1% 1/16W A93548-045 0402LF

CAD NOTE:
PLACE RTAD RESISTORS CLOSE
TO DDR3 MEMORY, BETWEEN
100MILS AND 500MILS

ROOM=IBMC_MEMORY

P0V75_STBY_IBMC

C9L15 0.1UF 16V 10% A36096-030 0402LF
C9M25 0.1UF 16V 10% A36096-030 0402LF
C1A10 0.1UF 16V 10% A36096-030 0402LF
C1A11 0.1UF 16V 10% A36096-030 0402LF

DDR3 VTT 0.75V MEMORY DECOUPLING

IBMC DDR3 TERMINATORS

P1V5_STBY_IBMC

C9M23 0.1UF 16V 10% A36096-030 0402LF
C9M30 0.1UF 16V 10% A36096-030 0402LF
C9M17 0.1UF 16V 10% A36096-030 0402LF
C9M1 0.1UF 16V 10% A36096-030 0402LF
C9M24 0.1UF 16V 10% A36096-030 0402LF
C9L42 22UF 6.3V 20% 602433-081 0603LF
C9M29 0.1UF 16V 10% A36096-030 0402LF
C9M26 0.1UF 16V 10% A36096-030 0402LF
C9M5 0.1UF 16V 10% A36096-030 0402LF
C1B1 0.1UF 16V 10% A36096-030 0402LF
C9M3 0.1UF 16V 10% A36096-030 0402LF
C9M38 22UF 6.3V 20% 602433-081 0603LF

DDR3 1.5V MEMORY DECOUPLING

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IBMC DDR3 MEMORY (2 OF 2)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 185 OF 303

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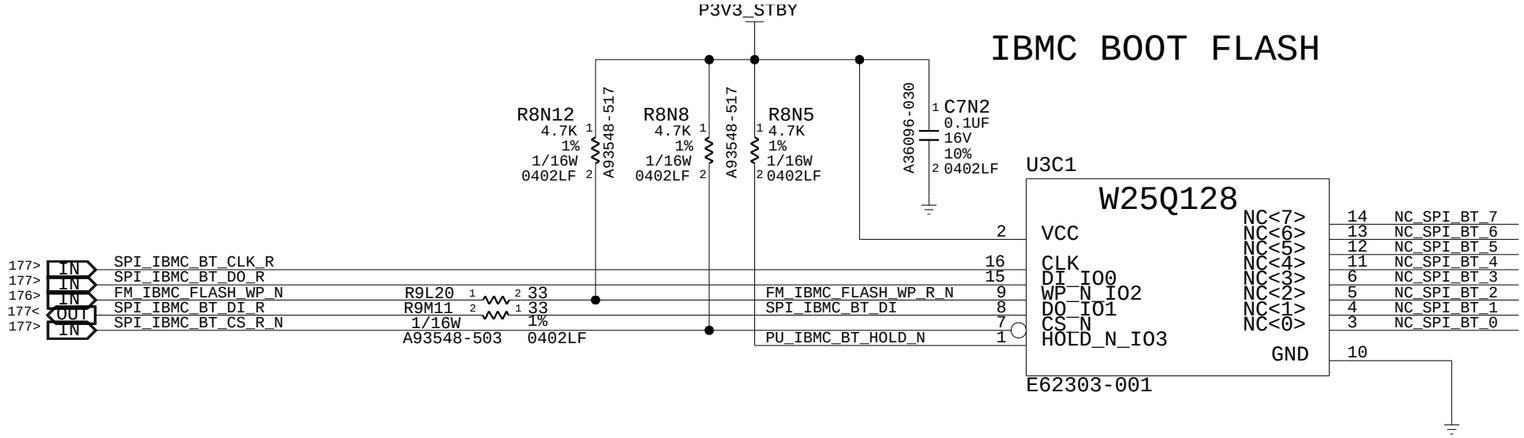
IBMC BOOT FLASH



CAD NOTE:
THIS PART WILL BE IN SOCKET
USE ALT SYMBOL ASSOCIATED WITH PART FOOTPRINT
BOM NOTE: SOCKET IS D91187-001

ROOM=IBMC_BOOT_FLASH

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IBMC SERIAL BOOT FLASH

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 186 OF 303	

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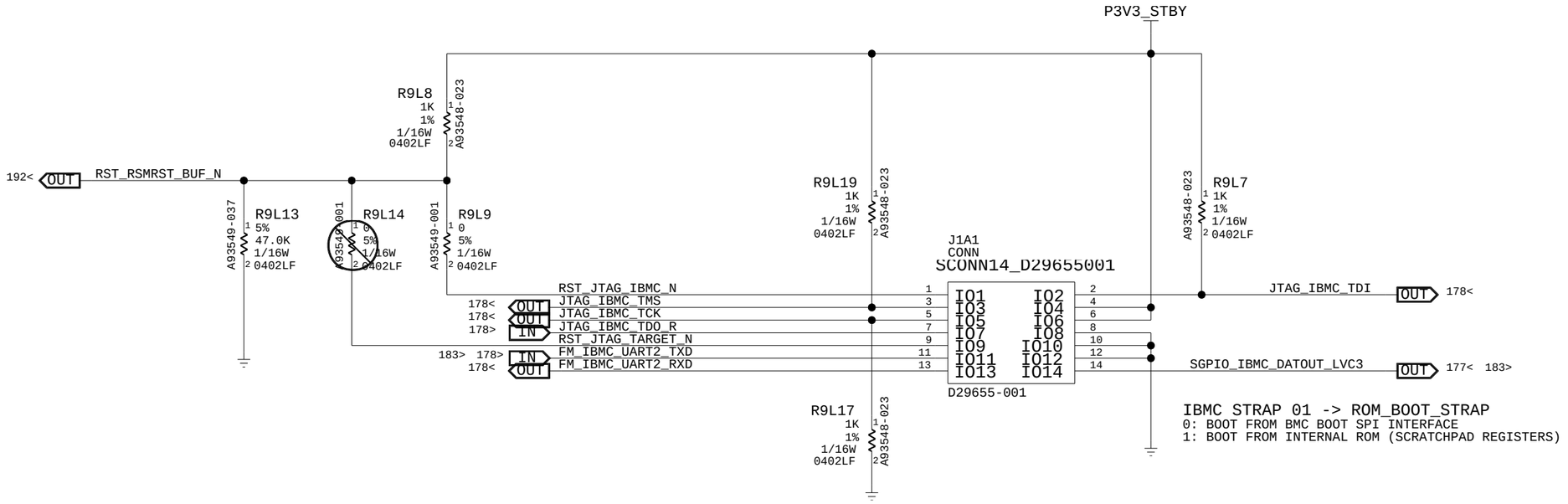

ROOM=IBMC_DEBUG_HEADER

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IBMC DEBUG HEADER

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 187 OF 303	

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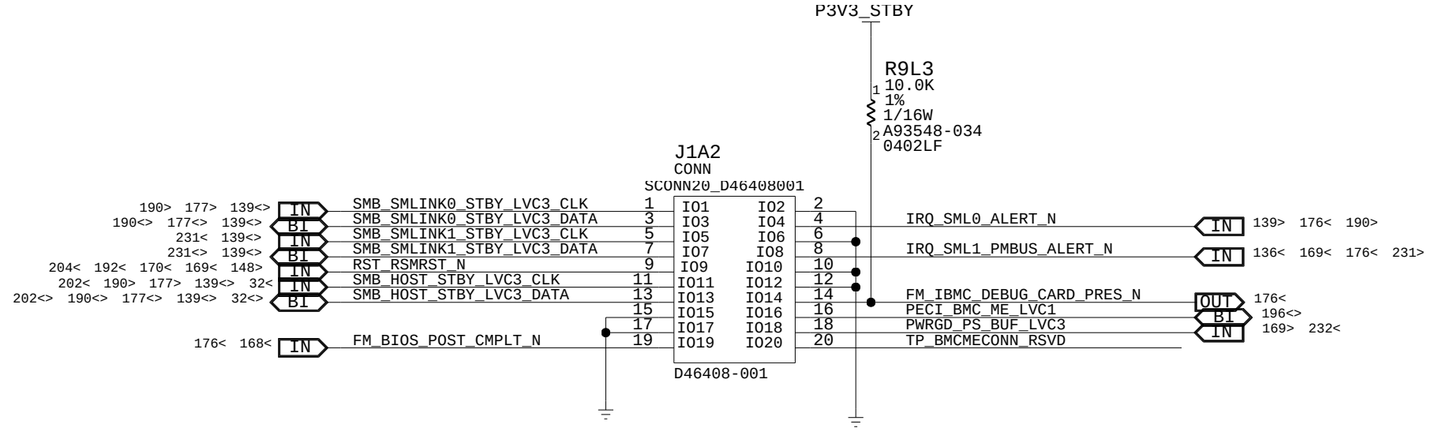

ROOM=BMC-ME_CONN

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BMC-ME CONNECTOR

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 188 OF 303	

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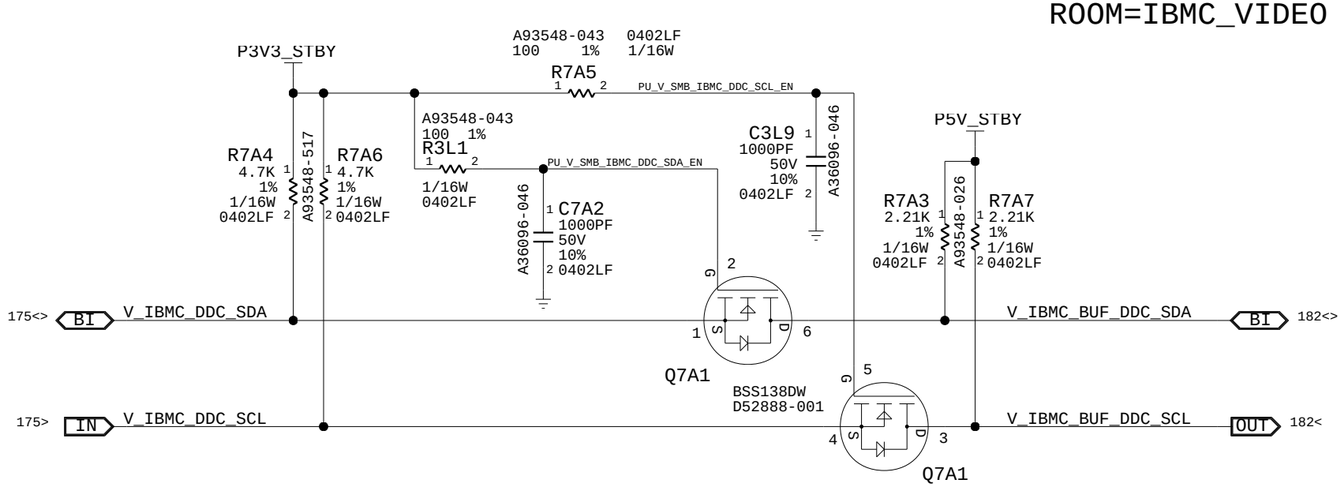
ROOM=IBMC_VIDEO



DDC SMBUS ISOLATORS

P3V3_STBY

R9L12 10.0K 1% 1/16W A93548-034 0402LF	FAN_IBMC_PWM5	OUT	176>	193<
R1A28 10.0K 1% 1/16W A93548-034 0402LF	FAN_IBMC_PWM4	OUT	176>	193<
R8L45 10.0K 1% 1/16W A93548-034 0402LF	FAN_IBMC_PWM3	OUT	178>	192<
R2A43 10.0K 1% 1/16W A93548-034 0402LF	FAN_IBMC_PWM2	OUT	178>	192<
R8L65 10.0K 1% 1/16W A93548-034 0402LF	FAN_IBMC_PWM1	OUT	178>	192<
R3C3 10.0K 1% 1/16W A93548-034 0402LF	FAN_IBMC_PWM0	OUT	178>	192<

R1A41 10.0K 1% 1/16W A93548-034 0402LF	PD_FAN_IBMC_PWM7	OUT	176<	
R1A45 10.0K 1% 1/16W A93548-034 0402LF	PD_FAN_IBMC_PWM6	OUT	176<	

P3V3_STBY

R9P37 4.7K 1% 1/16W A93548-517 0402LF	FM_SKT0_DIMM_A1_EVENT_N	OUT	46>	100<	207<
R9P38 4.7K 1% 1/16W A93548-517 0402LF	FM_SKT0_DIMM_B1_EVENT_N	OUT	47>	100<	207<
R9P52 4.7K 1% 1/16W A93548-517 0402LF	FM_SKT0_DIMM_C1_EVENT_N	OUT	48>	100<	207<
R9P53 4.7K 1% 1/16W A93548-517 0402LF	FM_SKT0_DIMM_D1_EVENT_N	OUT	49>	100<	207<
R9P31 4.7K 1% 1/16W A93548-517 0402LF	FM_SKT1_DIMM_E1_EVENT_N	OUT	69>	100<	207<
R9P50 4.7K 1% 1/16W A93548-517 0402LF	FM_SKT1_DIMM_F1_EVENT_N	OUT	70>	100<	207<
R9P48 4.7K 1% 1/16W A93548-517 0402LF	FM_SKT1_DIMM_G1_EVENT_N	OUT	71>	100<	207<
R9P49 4.7K 1% 1/16W A93548-517 0402LF	FM_SKT1_DIMM_H1_EVENT_N	OUT	72>	100<	207<
R1D44 4.7K 1% 1/16W A93548-517 0402LF	FM_SKT2_DIMM_J1_EVENT_N	OUT	92>	100<	206<
R1D47 4.7K 1% 1/16W A93548-517 0402LF	FM_SKT2_DIMM_K1_EVENT_N	OUT	93>	100<	206<
R1D45 4.7K 1% 1/16W A93548-517 0402LF	FM_SKT2_DIMM_L1_EVENT_N	OUT	94>	100<	206<
R1D42 4.7K 1% 1/16W A93548-517 0402LF	FM_SKT2_DIMM_M1_EVENT_N	OUT	95>	100<	206<
R1D27 4.7K 1% 1/16W A93548-517 0402LF	FM_SKT3_DIMM_N1_EVENT_N	OUT	100<	115>	206<
R1D28 4.7K 1% 1/16W A93548-517 0402LF	FM_SKT3_DIMM_P1_EVENT_N	OUT	100<	116>	206<
R1D31 4.7K 1% 1/16W A93548-517 0402LF	FM_SKT3_DIMM_R1_EVENT_N	OUT	100<	117>	206<
R1D32 4.7K 1% 1/16W A93548-517 0402LF	FM_SKT3_DIMM_T1_EVENT_N	OUT	100<	118>	206<

ROOM=IBMC_MISC

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IBMC MISCELLANEOUS (1 OF 5)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 189 OF 303	

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IMPORTANT: WHEN R1J49 AND R1J50 (PAGE 231) ARE UNSTUFFED,
IT IS MANDATORY TO STUFF R8L59 AND R8L58.

WHEN R8T10 AND R1F30 (PAGE 139) ARE UNSTUFFED,
IT IS MANDATORYTO STUFF R2B18 AND R8M19.

P3V3_STBY

R9L6 — PU_IBMC_GPIO_14_3 — OUT 176<
10.0K 1% 1/16W A93548-034 0402LF

R9L10 — PU_IBMC_GPIO_14_2 — OUT 176<
10.0K 1% 1/16W A93548-034 0402LF

R9L11 — PU_IBMC_GPIO_14_1 — OUT 176<
10.0K 1% 1/16W A93548-034 0402LF

R9L5 — PU_IBMC_GPIO_14_0 — OUT 176<
10.0K 1% 1/16W A93548-034 0402LF

R8M27 — PU_IBMC_PASSTHRUIN2 — OUT 178<
10.0K 1% 1/16W A93548-034 0402LF

R1A42 — FM_SMI_ACTIVE_N — OUT 136> 176<
4.7K 1% 1/16W A93548-517 0402LF

R9L15 — FM_NMI_EVENT_N — OUT 168< 176<
4.7K 1% 1/16W A93548-517 0402LF

I134

R8M26 — PU_IBMC_RSVD0 — OUT 178<
10.0K 1% 1/16W A93548-034 0402LF

R2A44 — PU_SPB_RI_N — OUT 178<
10.0K 1% 1/16W A93548-034 0402LF

R9L16 — IRQ_SML0_ALERT_N — OUT 139> 176< 188<
10.0K 1% 1/16W A93548-034 0402LF

R9L4 — PD_RMII_IBMC_LAN_RX_ER — OUT 176<
4.7K 1% 1/16W A93548-517 0402LF

R8M28 — PD_IBMC_TEST_BUS_EN — OUT 178<
10.0K 1% 1/16W A93548-034 0402LF

P3V3_STBY

R8L59 — SMB_PMBUS_IBMC_STBY_LVC3_DATA — BI 177<> 231<>
4.7K 1% 1/16W A93548-517 0402LF

R8L58 — SMB_PMBUS_IBMC_STBY_LVC3_CLK — OUT 177> 231<
4.7K 1% 1/16W A93548-517 0402LF

R2A56 — SMB_GS_STBY_LVC3_DATA — BI 177<>
4.7K 1% 1/16W A93548-517 0402LF

R2A51 — SMB_GS_STBY_LVC3_CLK — OUT 177>
4.7K 1% 1/16W A93548-517 0402LF

R2B18 — SMB_LAN_STBY_LVC3_DATA — BI 139<> 177<> 219<>
4.7K 1% 1/16W A93548-517 0402LF

R8M19 — SMB_LAN_STBY_LVC3_CLK — OUT 139<> 177> 219<>
4.7K 1% 1/16W A93548-517 0402LF

R1F32 — SMB_SMLINK0_STBY_LVC3_DATA — BI 139<> 177<> 188<>
2.21K 1% 1/16W A93548-026 0402LF

R1F29 — SMB_SMLINK0_STBY_LVC3_CLK — OUT 139<> 177> 188<
2.21K 1% 1/16W A93548-026 0402LF

R1G3 — SMB_HOST_STBY_LVC3_DATA — BI 32<> 139<> 177<> 188<> 202<>
4.7K 1% 1/16W A93548-517 0402LF

R1G12 — SMB_HOST_STBY_LVC3_CLK — OUT 32< 139<> 177> 188< 202<
4.7K 1% 1/16W A93548-517 0402LF

R8L53 — SMB_PCI_STBY_LVC3_DATA — BI 177<>
4.7K 1% 1/16W A93548-517 0402LF

R2A52 — SMB_PCI_STBY_LVC3_CLK — OUT 177>
4.7K 1% 1/16W A93548-517 0402LF

R1G6 — SMB_SENSOR_STBY_LVC3_DATA — BI 177<> 202<> 217<> 229<>
4.7K 1% 1/16W A93548-517 0402LF

R1G15 — SMB_SENSOR_STBY_LVC3_CLK — OUT 177> 202< 217< 229<
4.7K 1% 1/16W A93548-517 0402LF

R1C32 — SMB_IPMB_STBY_LVC3_DATA — BI 177<> 203<>
4.7K 1% 1/16W A93548-517 0402LF

R1C42 — SMB_IPMB_STBY_LVC3_CLK — OUT 177> 203<>
4.7K 1% 1/16W A93548-517 0402LF

P3V3_STBY

R9P6 — FM_CPU0_THERMTRIP_LVC3_N — OUT 100> 100< 128< 207<
1.21K 1% 1/16W A93548-107 0402LF

R1C34 — FM_CPU1_THERMTRIP_LVC3_N — OUT 100> 100< 128< 207<
1.21K 1% 1/16W A93548-107 0402LF

R1D22 — FM_CPU2_THERMTRIP_LVC3_N — OUT 100> 100< 128< 206<
1.21K 1% 1/16W A93548-107 0402LF

R1D21 — FM_CPU3_THERMTRIP_LVC3_N — OUT 100> 100< 128< 206<
1.21K 1% 1/16W A93548-107 0402LF

R9P18 — FM_CPU0_PROCHOT_LVC3_N — OUT 122> 130< 207<
1.21K 1% 1/16W A93548-107 0402LF

R9P17 — FM_CPU1_PROCHOT_LVC3_N — OUT 122> 130< 207<
1.21K 1% 1/16W A93548-107 0402LF

R1C38 — FM_CPU2_PROCHOT_LVC3_N — OUT 122> 130< 206<
1.21K 1% 1/16W A93548-107 0402LF

R1C39 — FM_CPU3_PROCHOT_LVC3_N — OUT 122> 130< 206<
1.21K 1% 1/16W A93548-107 0402LF

R9P5 — FM_CPU0_MEMAB_HOT_LVC3_N — OUT 123> 207<
1.21K 1% 1/16W A93548-107 0402LF

R9P4 — FM_CPU0_MEMCD_HOT_LVC3_N — OUT 123> 207<
1.21K 1% 1/16W A93548-107 0402LF

R9P3 — FM_CPU1_MEMEF_HOT_LVC3_N — OUT 123> 207<
1.21K 1% 1/16W A93548-107 0402LF

R9P2 — FM_CPU1_MEMGH_HOT_LVC3_N — OUT 123> 207<
1.21K 1% 1/16W A93548-107 0402LF

R1C35 — FM_CPU2_MEMJK_HOT_LVC3_N — OUT 123> 206<
1.21K 1% 1/16W A93548-107 0402LF

R1C31 — FM_CPU2_MEMLM_HOT_LVC3_N — OUT 123> 206<
1.21K 1% 1/16W A93548-107 0402LF

R1C30 — FM_CPU3_MEMNP_HOT_LVC3_N — OUT 123> 206<
1.21K 1% 1/16W A93548-107 0402LF

R1C28 — FM_CPU3_MEMRT_HOT_LVC3_N — OUT 123> 206<
1.21K 1% 1/16W A93548-107 0402LF

ROOM=IBMC_MISC

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IBMC MISCELLANEOUS (2 OF 5)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 190 OF 303	

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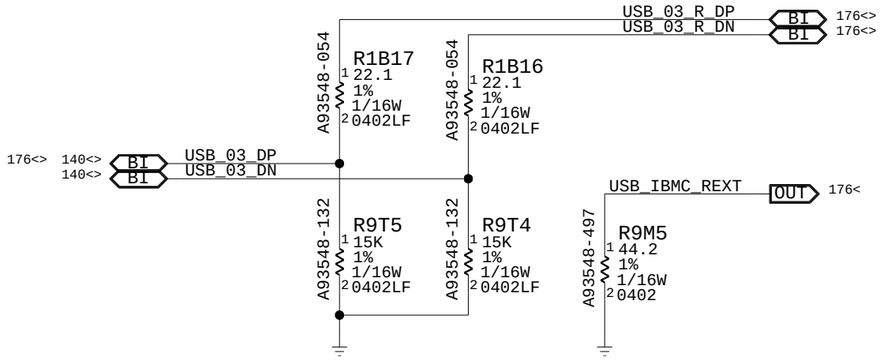
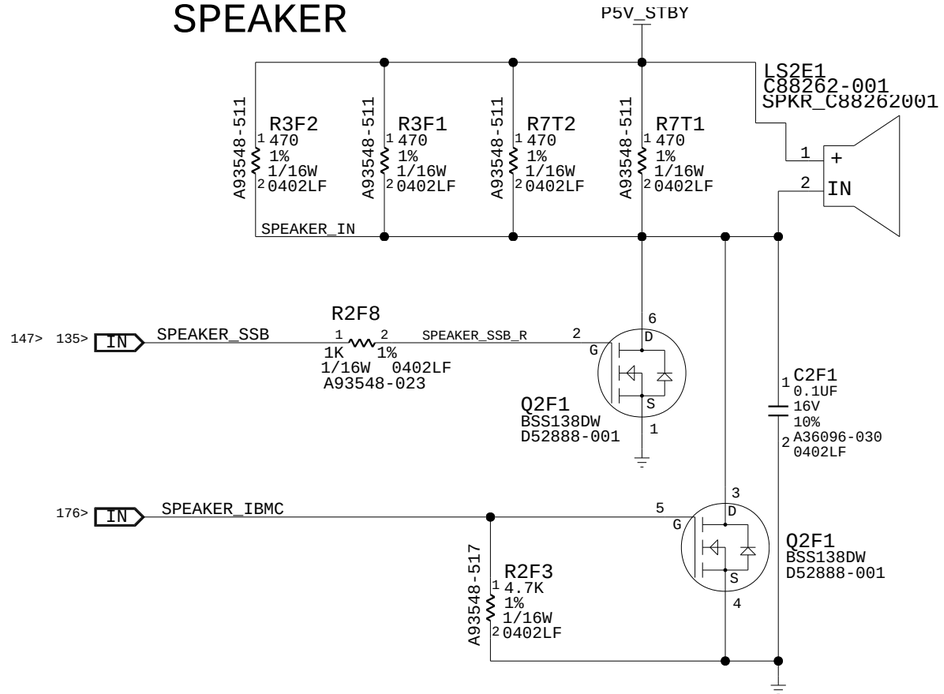
ROOM=IBMC_PBG_USB

USB TERMINATIONS

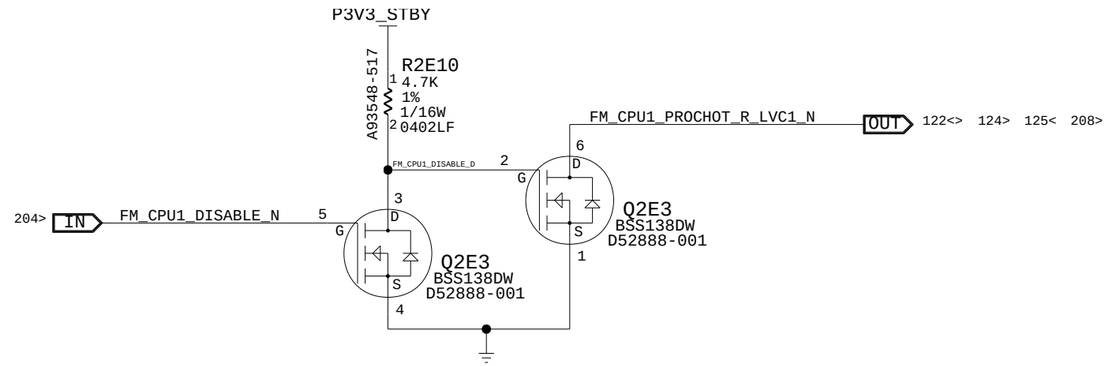


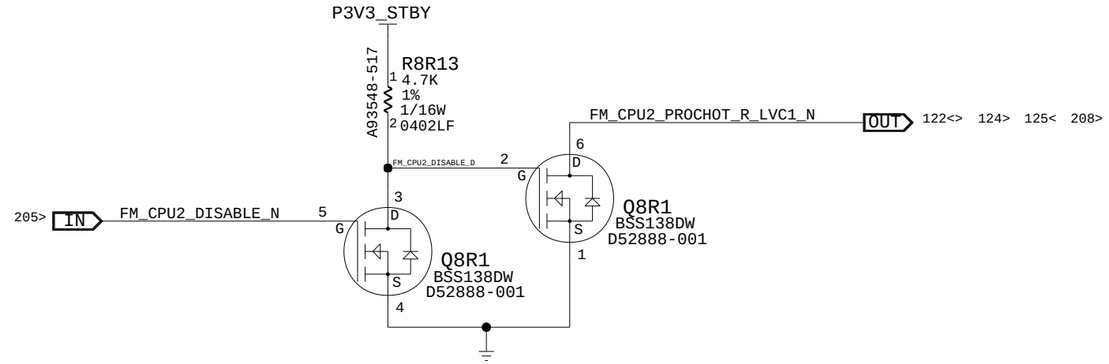
SPEAKER

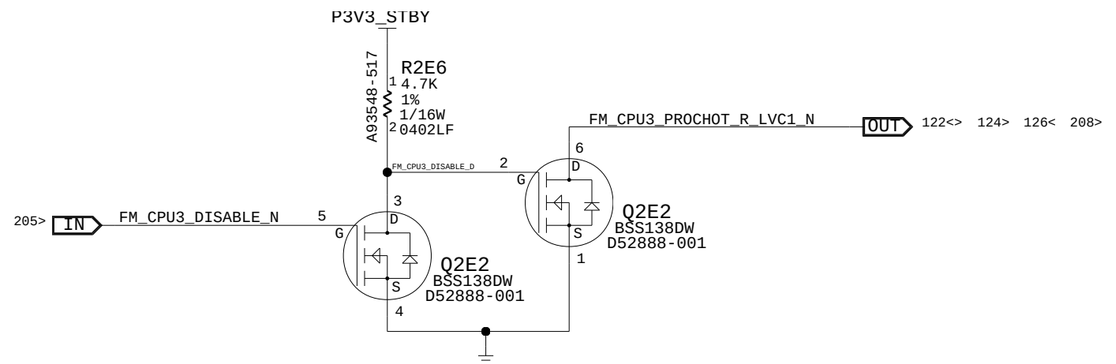


ROOM=IBMC_SPEAKER

ROOM=IBMC_CPUX_DISABLE







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IBMC MISCELLANEOUS (3 OF 5)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
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EU2E3
74LVC07A

204> IN FP_LED_STATUS_GREEN_N 3 — 4 FP_LED_STATUS_GREEN_BUF_CO_N OUT 229<

D90453-001
VCC=P3V3_STBY; GND=GND; TH=GND;

EU2E3
74LVC07A

204> IN FP_LED_STATUS_AMBER_N 5 — 6 FP_LED_STATUS_AMBER_BUF_CO_N OUT 229<

D90453-001
VCC=P3V3_STBY; GND=GND; TH=GND;

EU2E3
74LVC07A

204< 188< 170< 169< 148> IN RST_RSMRST_N 1 — 2 R2E7 1 2 RST_RSMRST_BUF_R_N OUT 177< 178<

0 5% 1/16W 0402LF
A93549-001

RST_RSMRST_BUF_N IN 187>

D90453-001
VCC=P3V3_STBY; GND=GND; TH=GND;

P5V

R2C3 4.7K 1% 1/16W A93548-517 0402LF

FAN_IBMC_PWM0_N OUT 193<

189> 178> IN FAN_IBMC_PWM0 5 — G D S 3 4

Q3C2
BSS138DW
D52888-001

A93548-392
R3B13
15 1% 1/16W 0402LF

FAN_IBMC_OC_PWM0 1 — 2 FAN_PWM_OUT_CF0 OUT 213<

2 G D S 6 1

Q3C2
BSS138DW
D52888-001

P5V

R2C2 4.7K 1% 1/16W A93548-517 0402LF

FAN_IBMC_PWM1_N OUT 193<

189> 178> IN FAN_IBMC_PWM1 5 — G D S 3 4

Q2C1
BSS138DW
D52888-001

A93548-392
R2C1
15 1% 1/16W 0402LF

FAN_IBMC_OC_PWM1 1 — 2 FAN_PWM_OUT_CF3 OUT 213<

2 G D S 6 1

Q2C1
BSS138DW
D52888-001

P5V

R8N3 4.7K 1% 1/16W A93548-517 0402LF

FAN_IBMC_PWM2_N OUT 193<

189> 178> IN FAN_IBMC_PWM2 5 — G D S 3 4

Q7N3
BSS138DW
D52888-001

A93548-392
R8N1
15 1% 1/16W 0402LF

FAN_IBMC_OC_PWM2 1 — 2 FAN_PWM_OUT_SF9_10 OUT 214<

2 G D S 6 1

Q7N3
BSS138DW
D52888-001

P5V

R3C2 4.7K 1% 1/16W A93548-517 0402LF

FAN_IBMC_PWM3_N OUT 193<

189> 178> IN FAN_IBMC_PWM3 5 — G D S 3 4

Q3C1
BSS138DW
D52888-001

A93548-392
R7N1
15 1% 1/16W 0402LF

FAN_IBMC_OC_PWM3 1 — 2 FAN_PWM_OUT_SF7_8_11 OUT 214<

2 G D S 6 1

Q3C1
BSS138DW
D52888-001

ROOM=IBMC_LED_FAN

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IBMC MISCELLANEOUS (4 OF 5)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 192 OF 303

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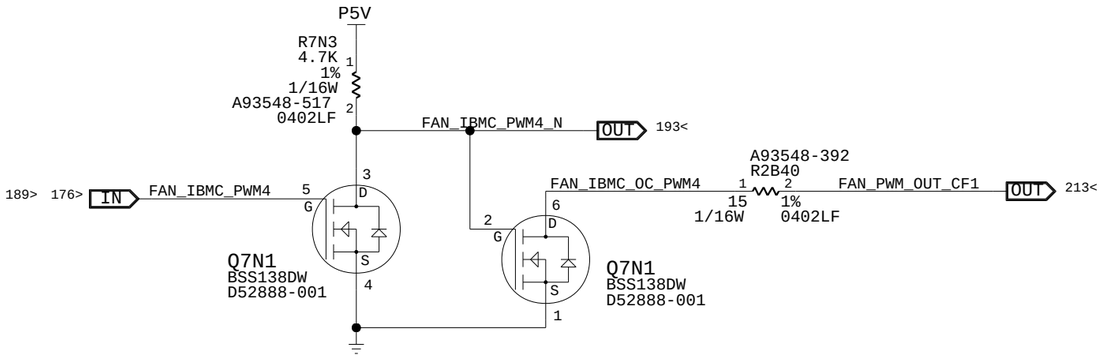
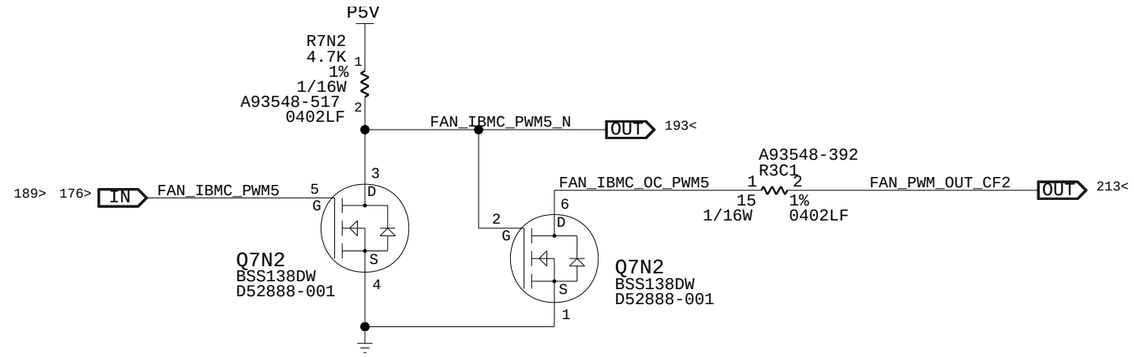
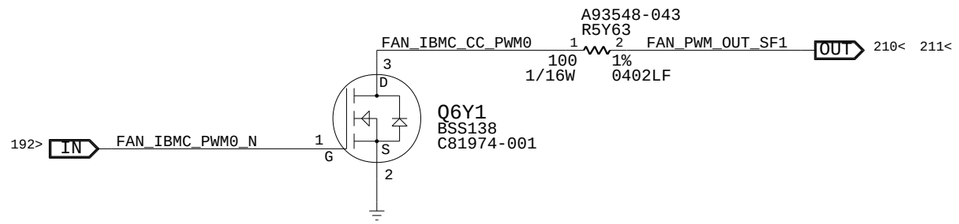
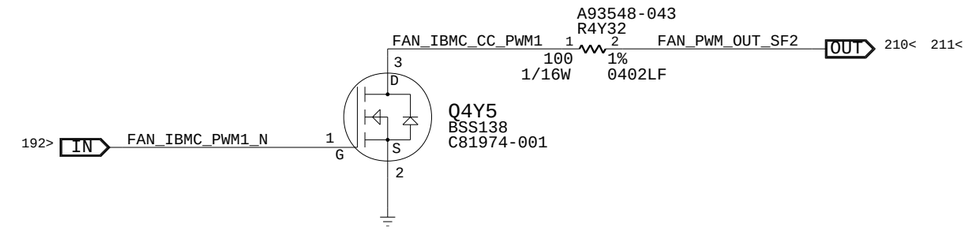
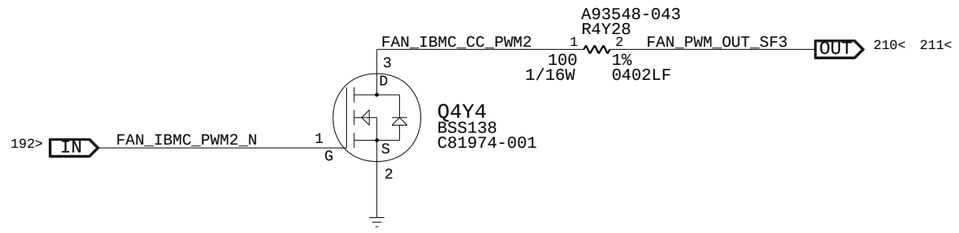
ROOM=IBMC_LED_FAN

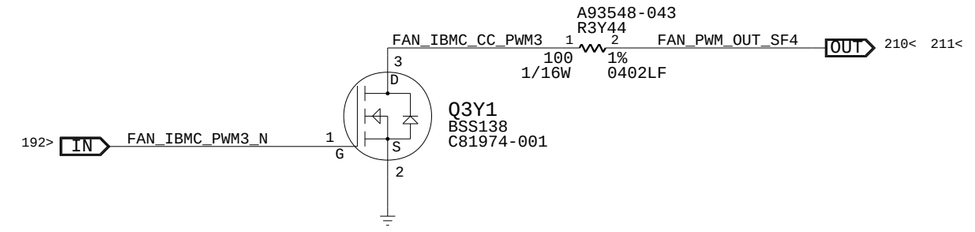


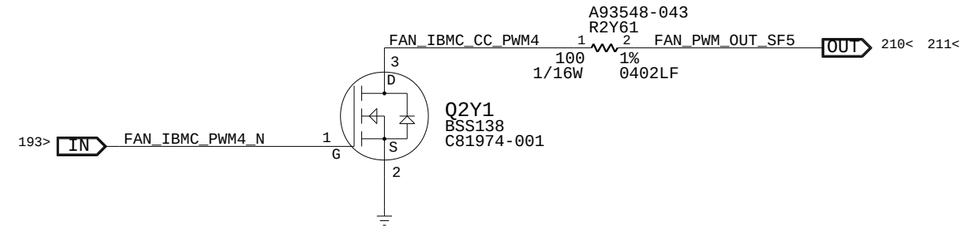


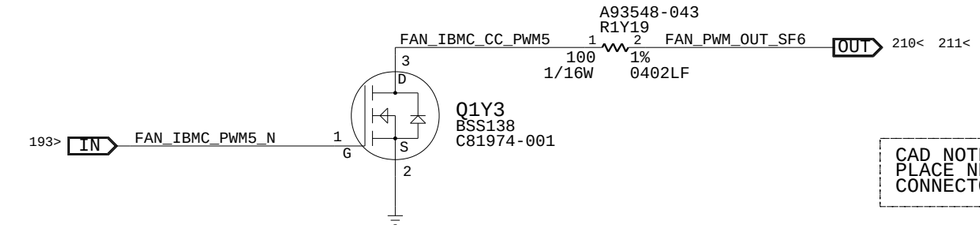












CAD NOTE:
PLACE NEAR FRONT
CONNECTOR(S)

ROOM=IBMC_FAN_CLOSE_CHASSIS

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IBMC MISCELLANEOUS (5 OF 5)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 193 OF 303

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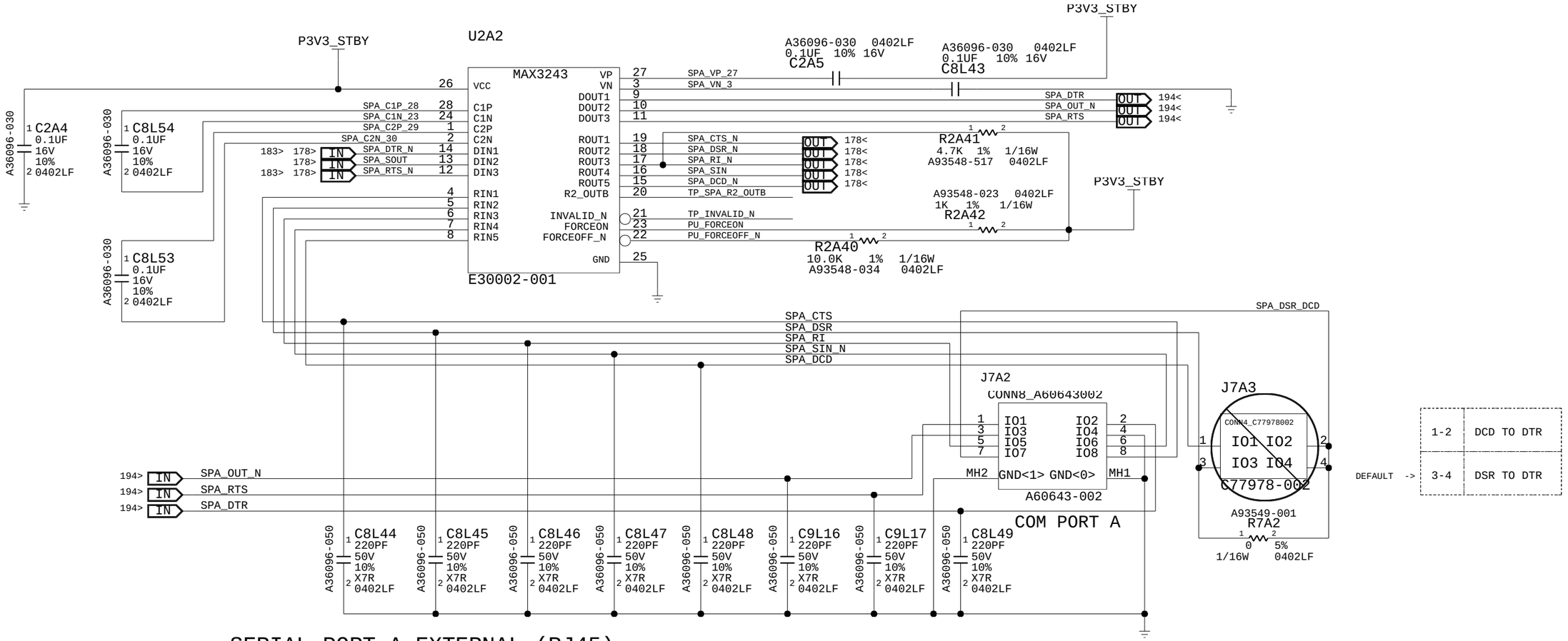

SERIAL PORT A EXTERNAL (RJ45)

ROOM=IBMC_SPA

IBMC SERIAL PORT (1 OF 2)

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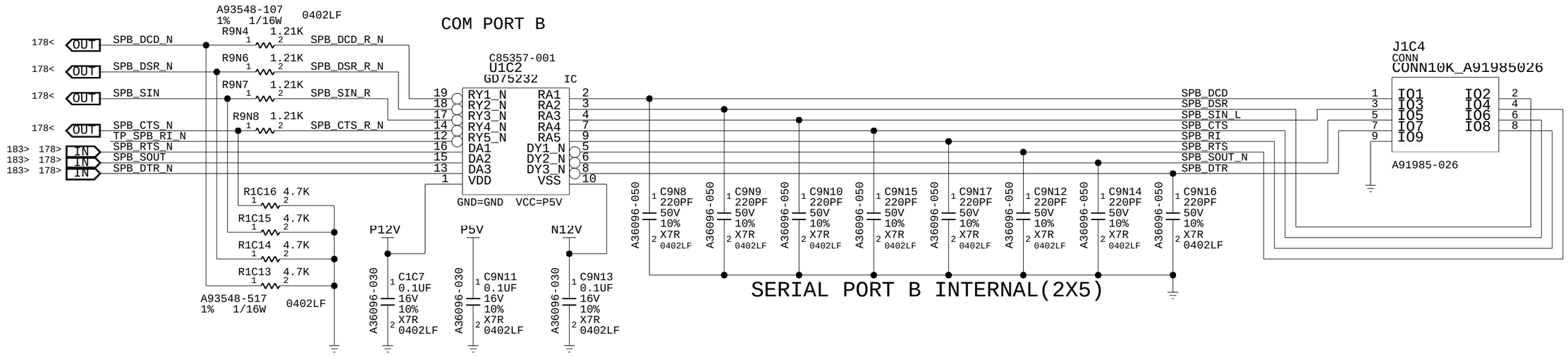
DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 194 OF 303	

INTEL CONFIDENTIAL



ROOM=IBMC_SPB

IBMC SERIAL PORT (2 OF 2)

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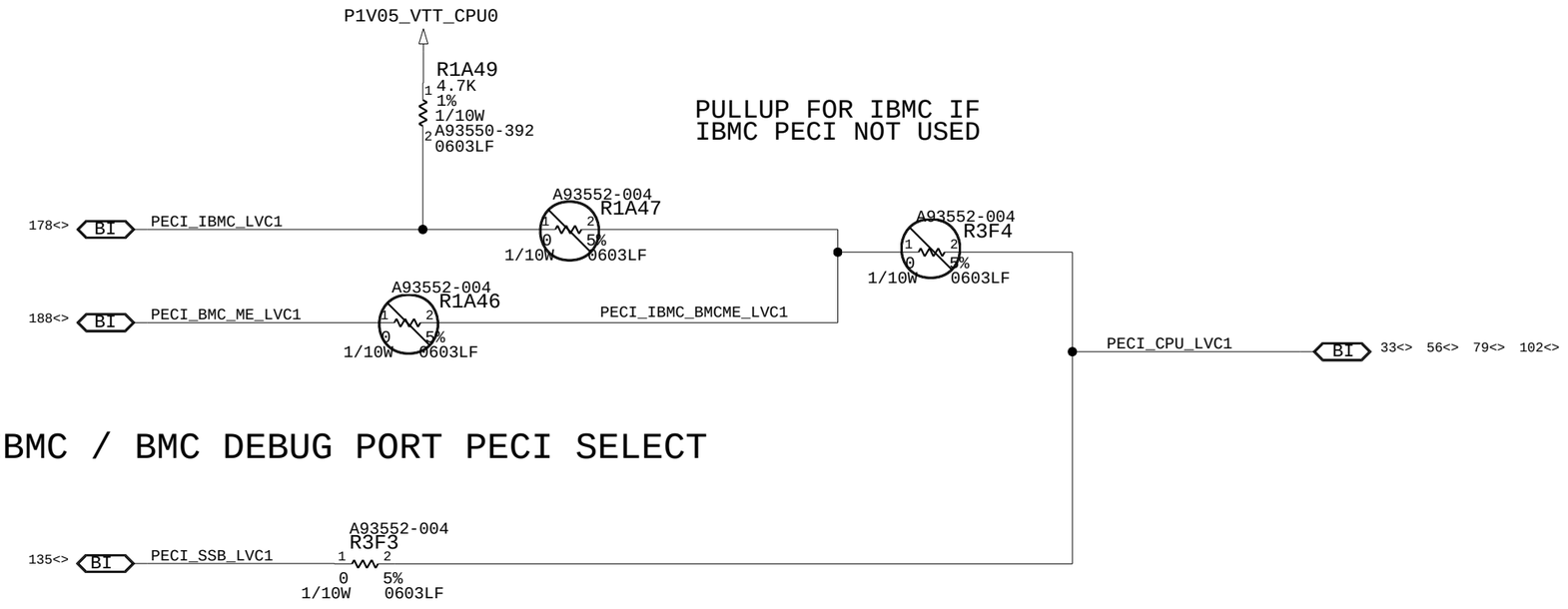
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 195 OF 303	

INTEL CONFIDENTIAL



CAD NOTE: PLACE THE R1A46 AND R1A47 RESISTORS AS CLOSE AS POSSIBLE TO THE COMMON NODE, SO THAT THE PECI BUS STUB IS AS SHORT AS POSSIBLE WHEN ANY OF THEM IS UNSTUFFED.AS WELL, THE SAME FOR R3F3 AND R3F4; ALSO, INDICATE WHICH ONE IS FOR IBMC, BMC DEBUG, AND SSB

ROOM=IBMC_PECI

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PECI

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 196 OF 303	

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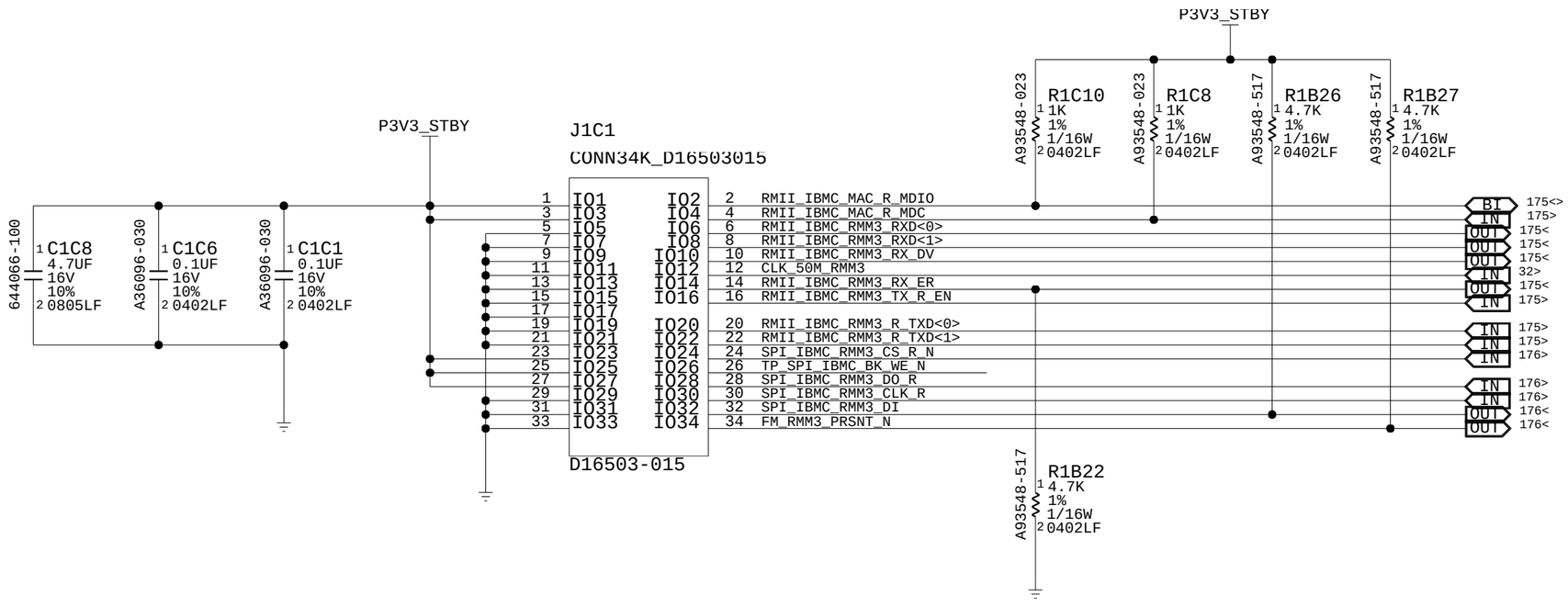
RMM3 CONNECTOR



ROOM=IBMC_RMM3_CONN

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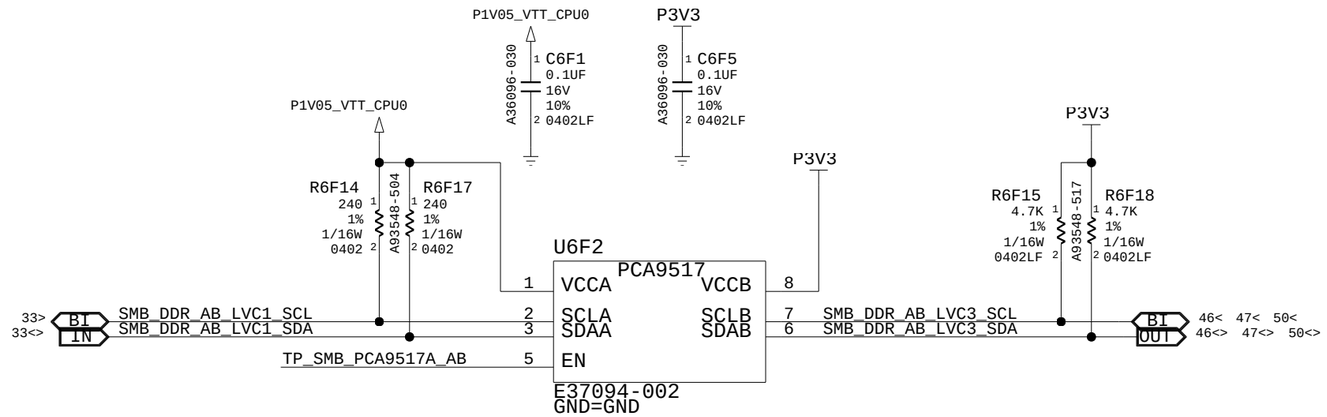
RMII

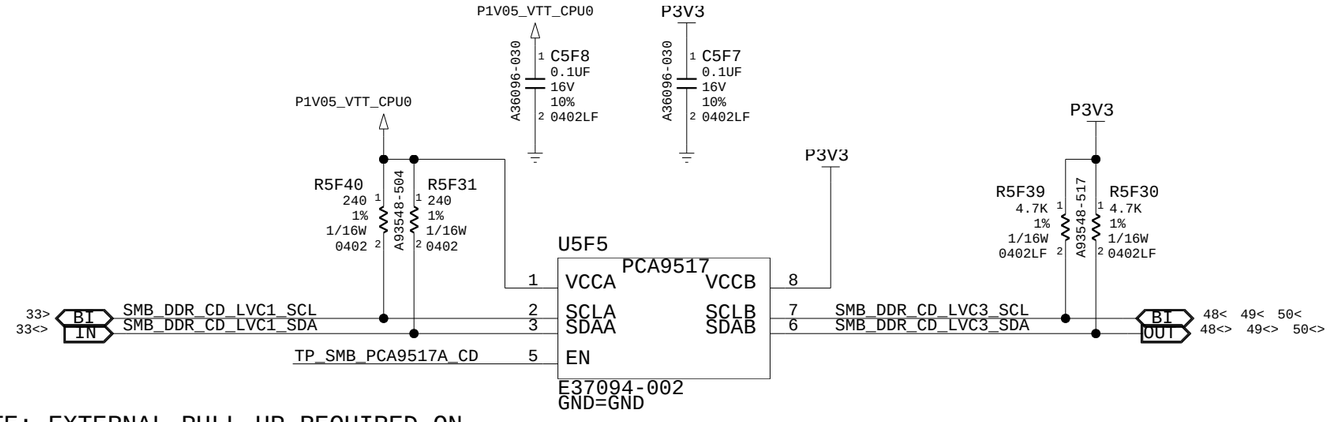
DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 197 OF 303	

INTEL CONFIDENTIAL

ROOM=SMBUS_SOCKET0



NOTE: EXTERNAL PULL UP REQUIRED ON
SIDE "A" FOR IVB-EXB COMPATIBILITY



NOTE: EXTERNAL PULL UP REQUIRED ON
SIDE "A" FOR IVB-EXB COMPATIBILITY

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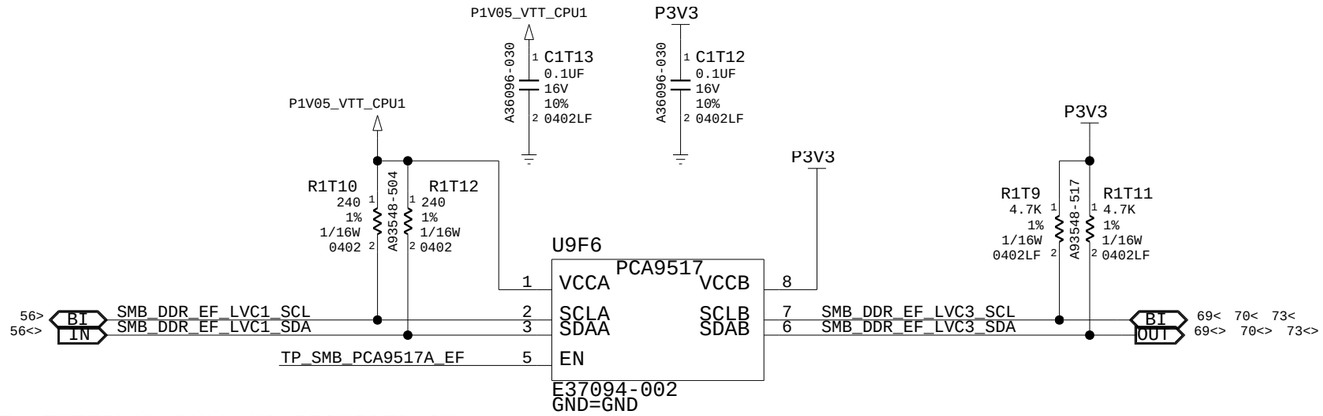
SMBUS (1 OF 6)

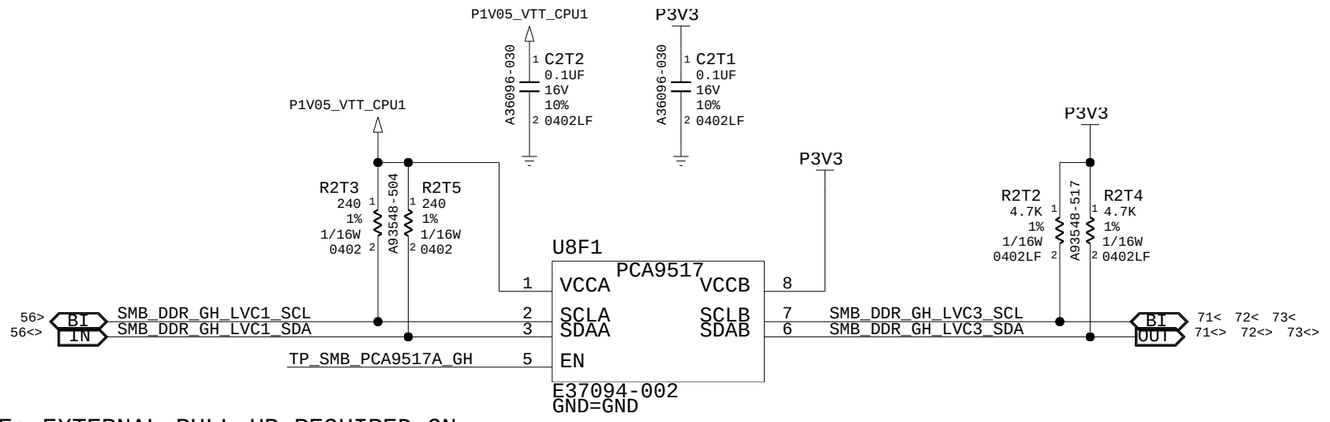
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 198 OF 303	

INTEL CONFIDENTIAL

ROOM=SMBUS_SOCKET1



NOTE: EXTERNAL PULL UP REQUIRED ON
SIDE "A" FOR IVB-EXB COMPATIBILITY



NOTE: EXTERNAL PULL UP REQUIRED ON
SIDE "A" FOR IVB-EXB COMPATIBILITY

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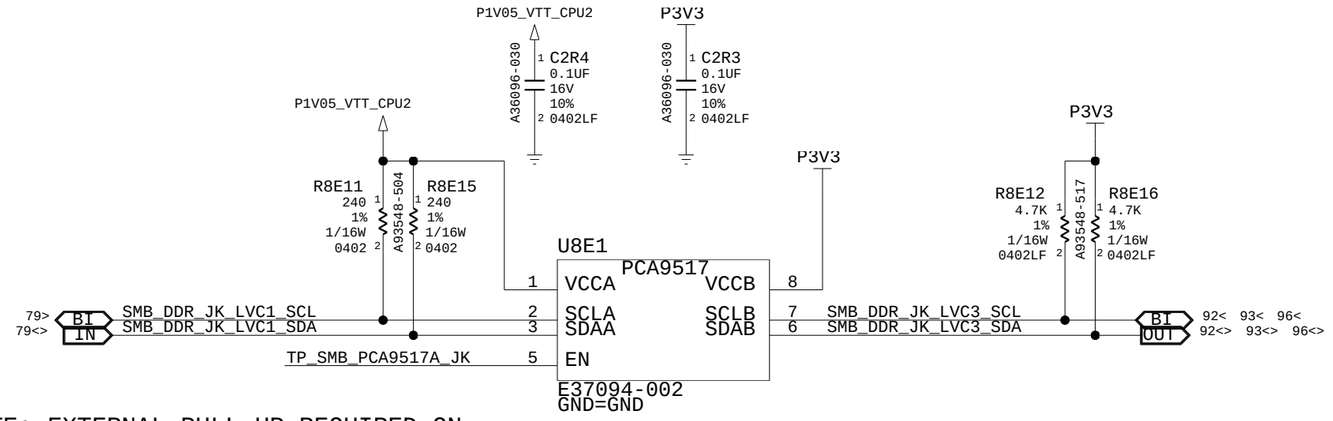
SMBUS (2 OF 6)

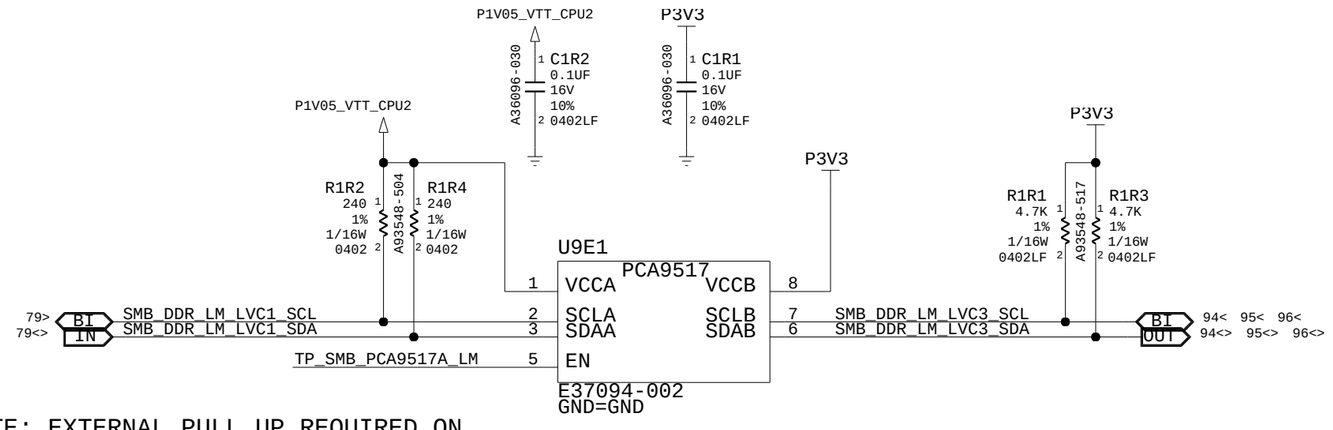
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 199 OF 303	

INTEL CONFIDENTIAL

ROOM=SMBUS_SOCKET2



NOTE: EXTERNAL PULL UP REQUIRED ON
SIDE "A" FOR IVB-EXB COMPATIBILITY



NOTE: EXTERNAL PULL UP REQUIRED ON
SIDE "A" FOR IVB-EXB COMPATIBILITY

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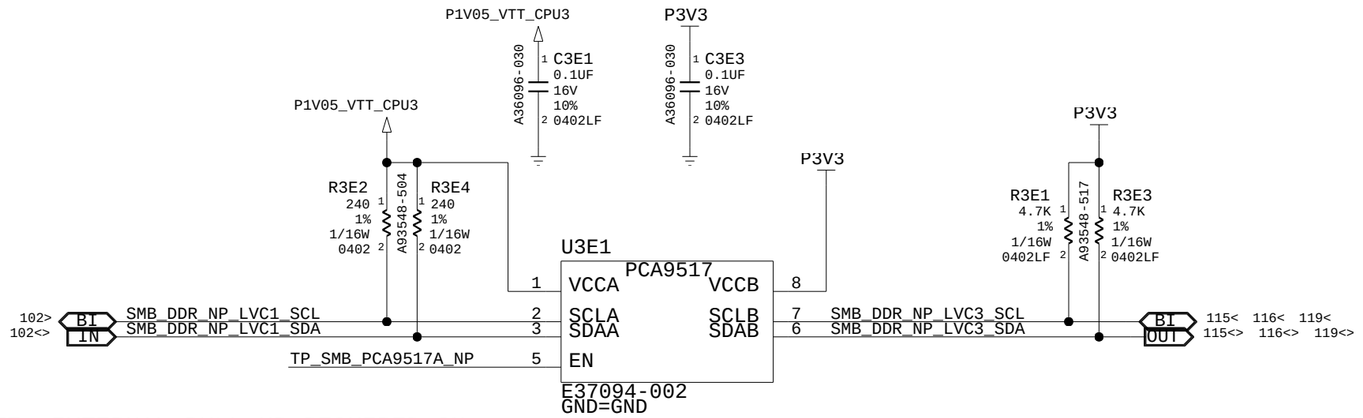
SMBUS (3 OF 6)

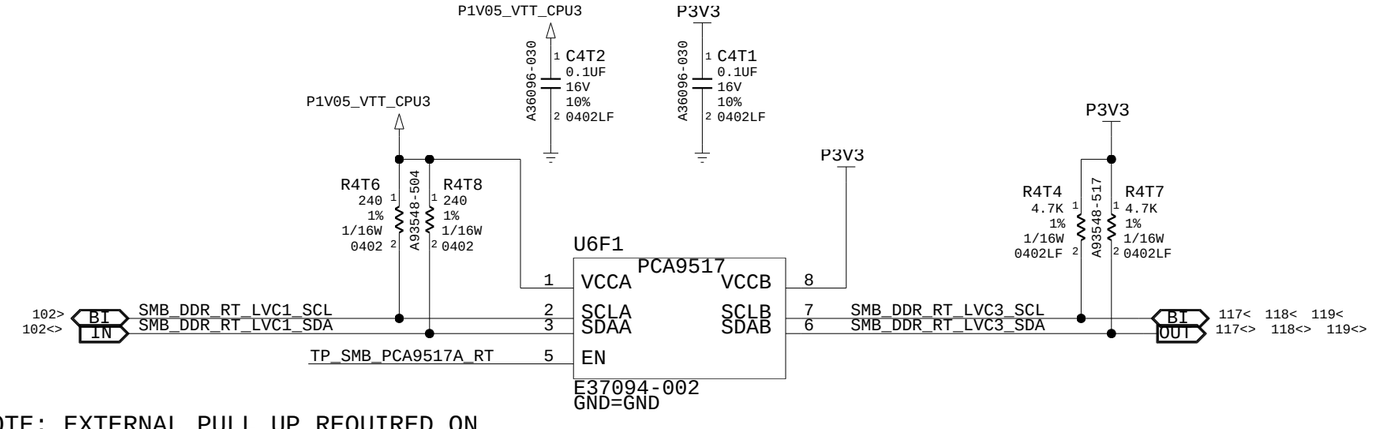
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 200 OF 303	

INTEL CONFIDENTIAL

ROOM=SMBUS_SOCKET3



NOTE: EXTERNAL PULL UP REQUIRED ON
SIDE "A" FOR IVB-EXB COMPATIBILITY



NOTE: EXTERNAL PULL UP REQUIRED ON
SIDE "A" FOR IVB-EXB COMPATIBILITY

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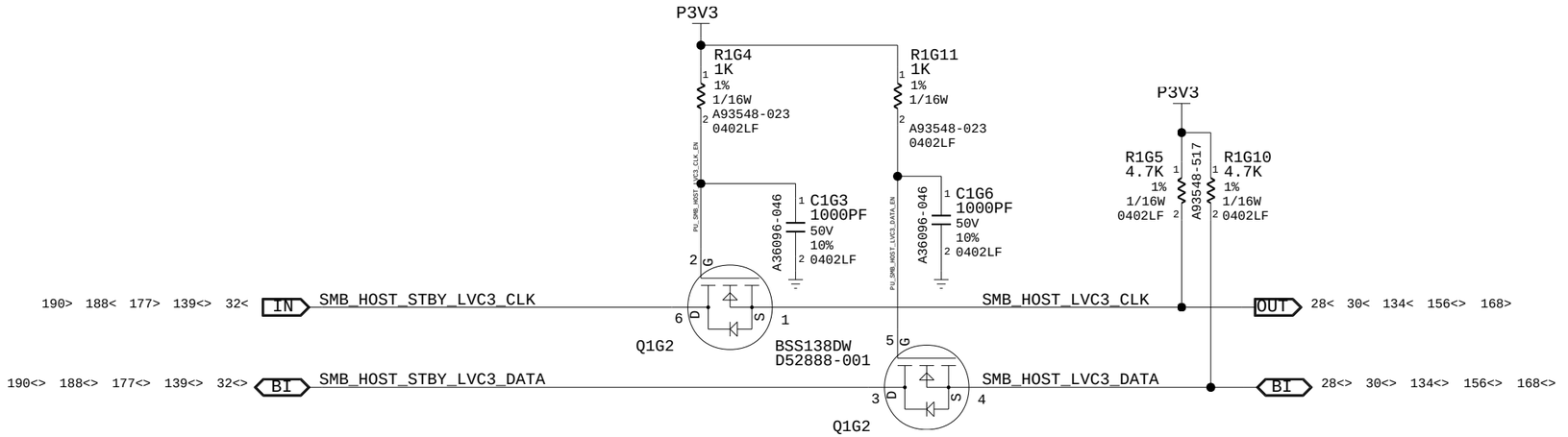
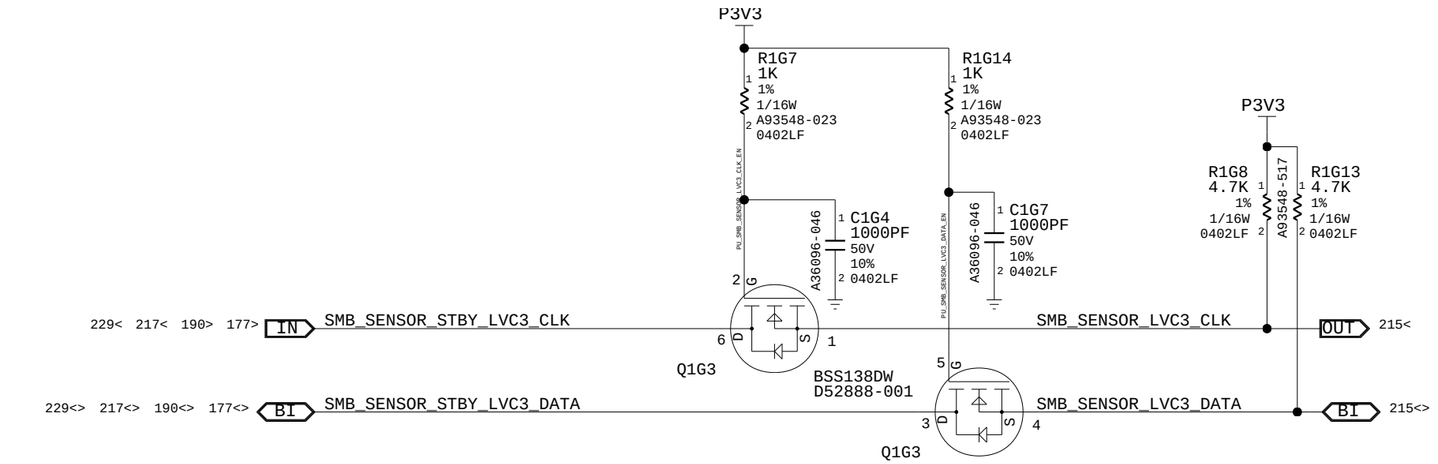
SMBUS (4 OF 6)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 201 OF 303	

INTEL CONFIDENTIAL





ROOM=IBMC_SMBUS

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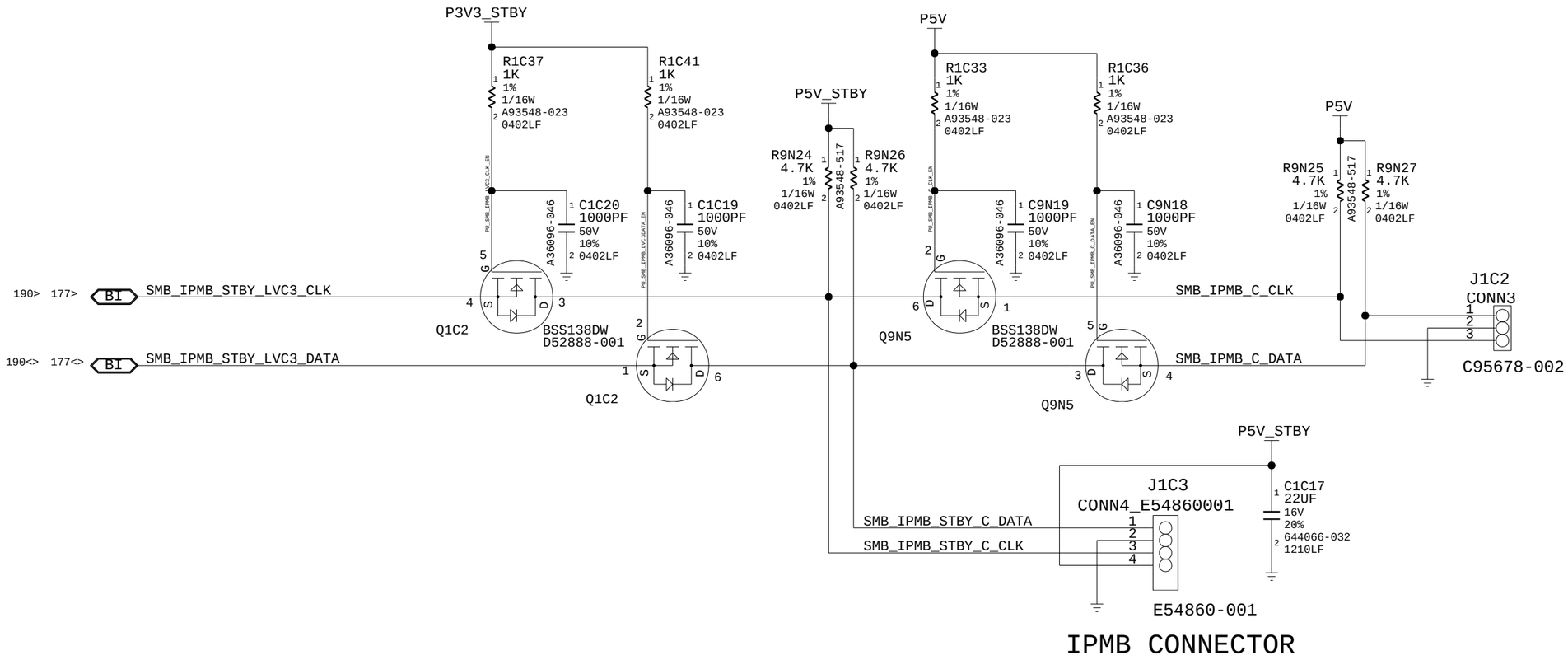
SMBUS (5 OF 6)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 202 OF 303	

INTEL CONFIDENTIAL



IPMB CONNECTOR

ROOM=IBMC_SMBUS

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SMBUS (6 OF 6)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 203 OF 303	

INTEL CONFIDENTIAL

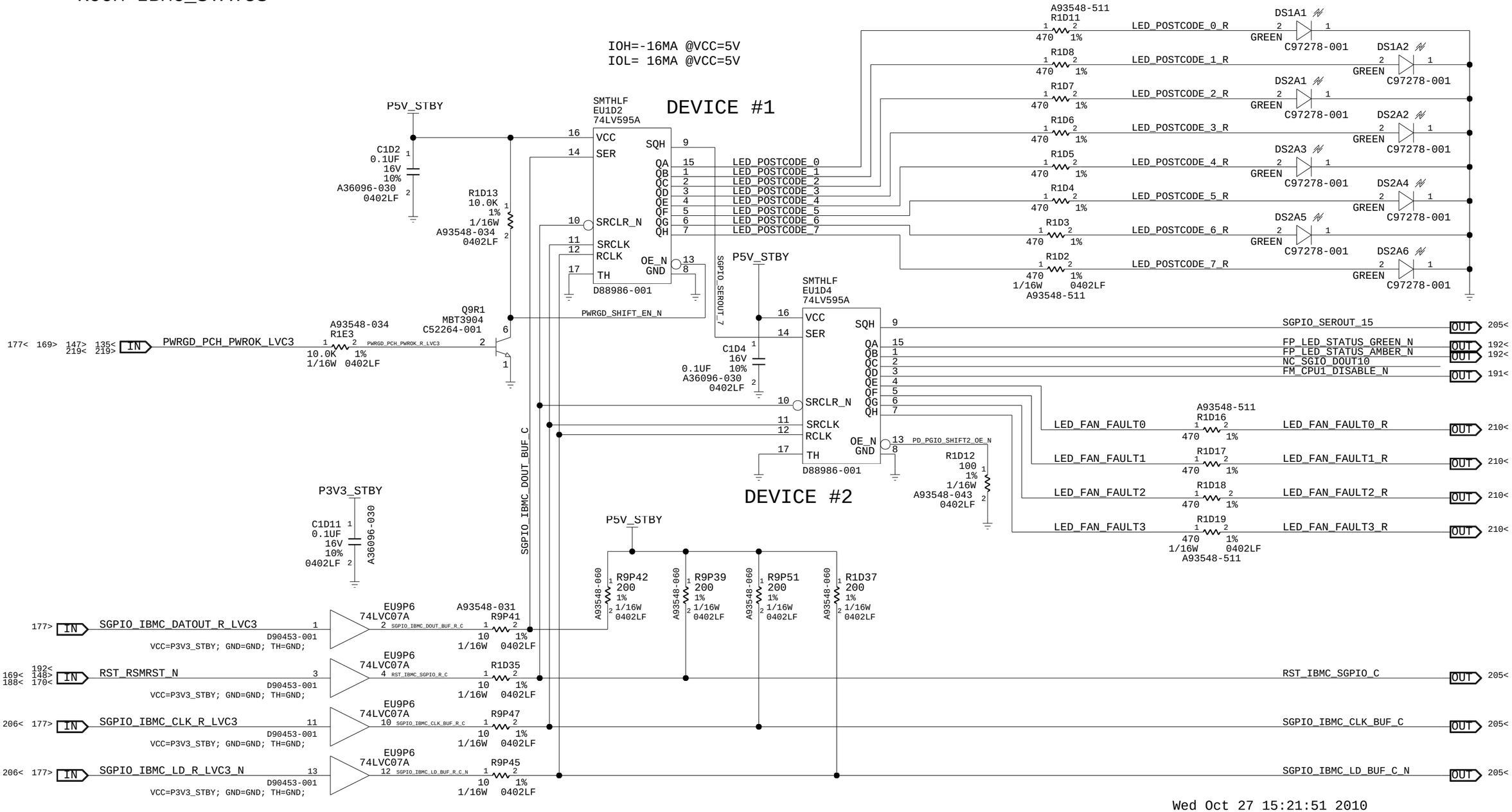
ROOM=IBMC_STATUS

LED_POSTCODE_0 = LSB
LED_POSTCODE_7 = MSB
ADD SPACE BETWEEN LED_POSTCODE_3 AND LED_POSTCODE_4

IOH=-16MA @VCC=5V
IOL= 16MA @VCC=5V

DEVICE #1

DEVICE #2



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LEDS & STATUS (1 OF 6)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 204 OF 303	

INTEL CONFIDENTIAL

DEVICE #3

P5V_STBY
A36096-030 C9P2 0.1UF 16V 10% 0402LF
SMTHLF EU9P1 74LV595A D88986-001
VCC SER SRCLR_N SRCLK RCLK TH SQH GND OE_N
SQA SQB SQC SQD SQE SQF SQG SQH

204> IN SGPIO_SEROUT_15
204> IN RST_IBMC_SGPIO_C
204> IN SGPIO_IBMC_CLK_BUF_C
204> IN SGPIO_IBMC_LD_BUF_C_N

LED_FAN_FAULT4
LED_FAN_FAULT5
TP_LED_FAN_FAULT6
TP_LED_FAN_FAULT7
LED_SKT0_DIMM_A1_FAULT_R
LED_SKT0_DIMM_B1_FAULT_R
LED_SKT0_DIMM_C1_FAULT_R
LED_SKT0_DIMM_D1_FAULT_R

IOH=-16MA @VCC=5V
IOL= 16MA @VCC=5V

PD_SGPIO_SHIFT3_OE_N
SGPIO_SEROUT_23

DEVICE #4

P5V_STBY
A36096-030 C9P8 0.1UF 16V 10% 0402LF
SMTHLF EU9P5 74LV595A D88986-001
R9P20 100 1% 1/16W A93548-043 0402LF

LED_SKT1_DIMM_E1_FAULT_R
LED_SKT1_DIMM_F1_FAULT_R
LED_SKT1_DIMM_G1_FAULT_R
LED_SKT1_DIMM_H1_FAULT_R
LED_SKT2_DIMM_J1_FAULT_R
LED_SKT2_DIMM_K1_FAULT_R
LED_SKT2_DIMM_L1_FAULT_R
LED_SKT2_DIMM_M1_FAULT_R

IOH=-16MA @VCC=5V
IOL= 16MA @VCC=5V

PD_SGPIO_SHIFT4_OE_N
R9P35 100 1% 1/16W A93548-043 0402LF

DEVICE #5

P5V_STBY
A36096-030 C1D9 0.1UF 16V 10% 0402LF
SGPIO_SEROUT_31
SMTHLF EU1D6 74LV595A D88986-001

TP_SGPIO_SEROUT_39_SH
LED_SKT3_DIMM_N1_FAULT_R
LED_SKT3_DIMM_P1_FAULT_R
LED_SKT3_DIMM_R1_FAULT_R
LED_SKT3_DIMM_T1_FAULT_R

IOH=-16MA @VCC=5V
IOL= 16MA @VCC=5V

PD_SGPIO_SHIFT5_OE_N
R1D29 100 1% 1/16W 0402LF A93548-043

R9P19 R9P8 R9P7 R9P9 R9P10 R9P11 — 470 1% 0402LF A93548-511 — OUT 210<
LED_FAN_FAULT4_R
LED_FAN_FAULT5_R
LED_SKT0_DIMM_A1_FAULT
LED_SKT0_DIMM_B1_FAULT
LED_SKT0_DIMM_C1_FAULT
LED_SKT0_DIMM_D1_FAULT

R9P36 R9P29 R9P28 R9P27 R9P26 R9P25 R9P24 R9P30 — 470 1% 0402LF A93548-511
LED_SKT1_DIMM_E1_FAULT
LED_SKT1_DIMM_F1_FAULT
LED_SKT1_DIMM_G1_FAULT
LED_SKT1_DIMM_H1_FAULT
LED_SKT2_DIMM_J1_FAULT
LED_SKT2_DIMM_K1_FAULT
LED_SKT2_DIMM_L1_FAULT
LED_SKT2_DIMM_M1_FAULT

R1D30 R1D26 R1D24 R1D23 — 470 1% 0402LF A93548-511
LED_SKT3_DIMM_N1_FAULT
LED_SKT3_DIMM_P1_FAULT
LED_SKT3_DIMM_R1_FAULT
LED_SKT3_DIMM_T1_FAULT

DS1H4 DS1H3 DS1H1 DS1H2 DS1H8 DS1H7 DS1H5 DS1H6 DS1G15 DS1G16 DS1G18 DS1G17 DS1G11 DS1G12 DS1G14 DS1G13 — C97278-002 AMBER

CAD NOTE:
PLACE LEDS NEAR
THE CORRESPONDING
CHANNEL/DIMM SLOT

FM_CPU2_DISABLE_N — OUT 191<
FM_CPU3_DISABLE_N — OUT 191<
TP_SGPIO_SEROUT_38
TP_SGPIO_SEROUT_39

ROOM=IBMC_STATUS

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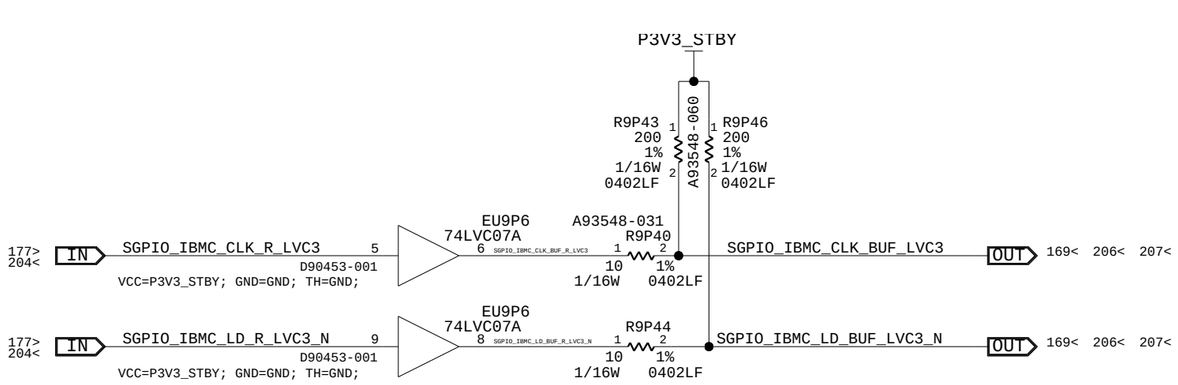
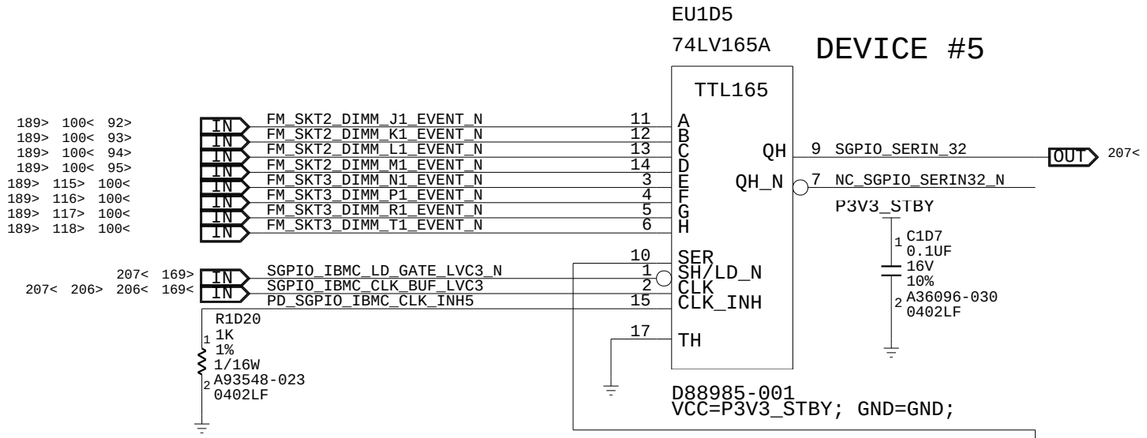
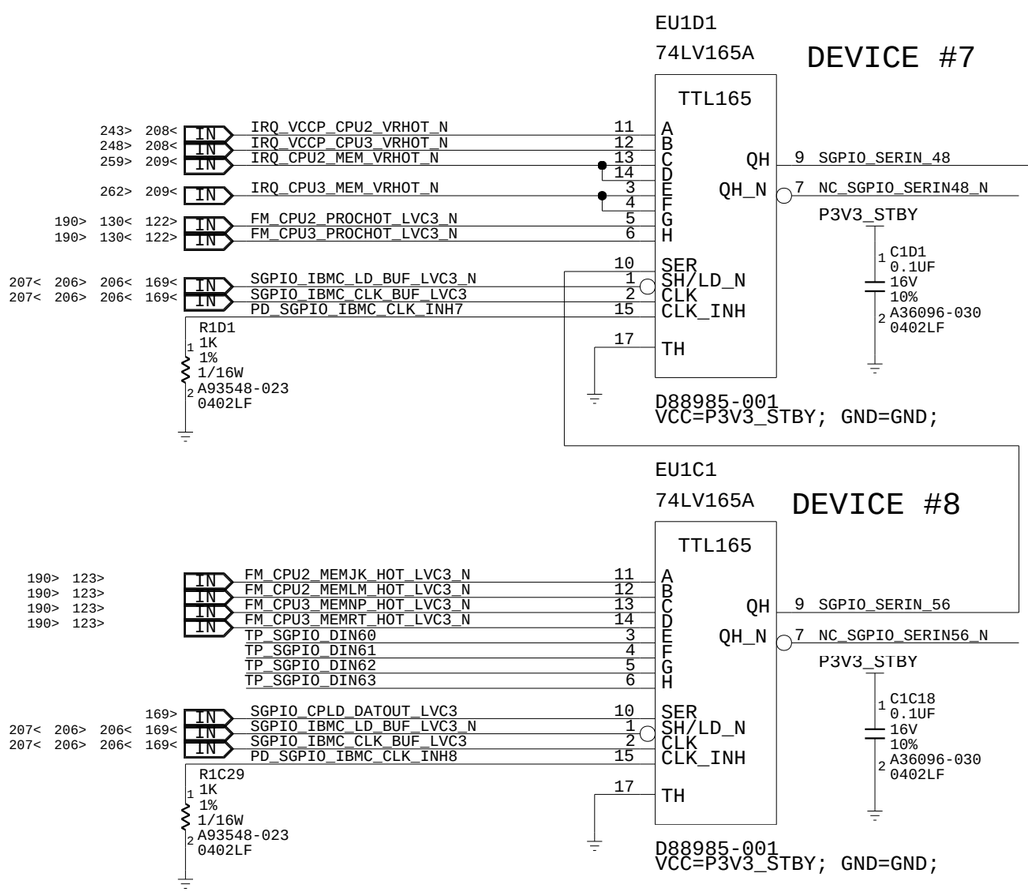
LEDS & STATUS (2 OF 6)

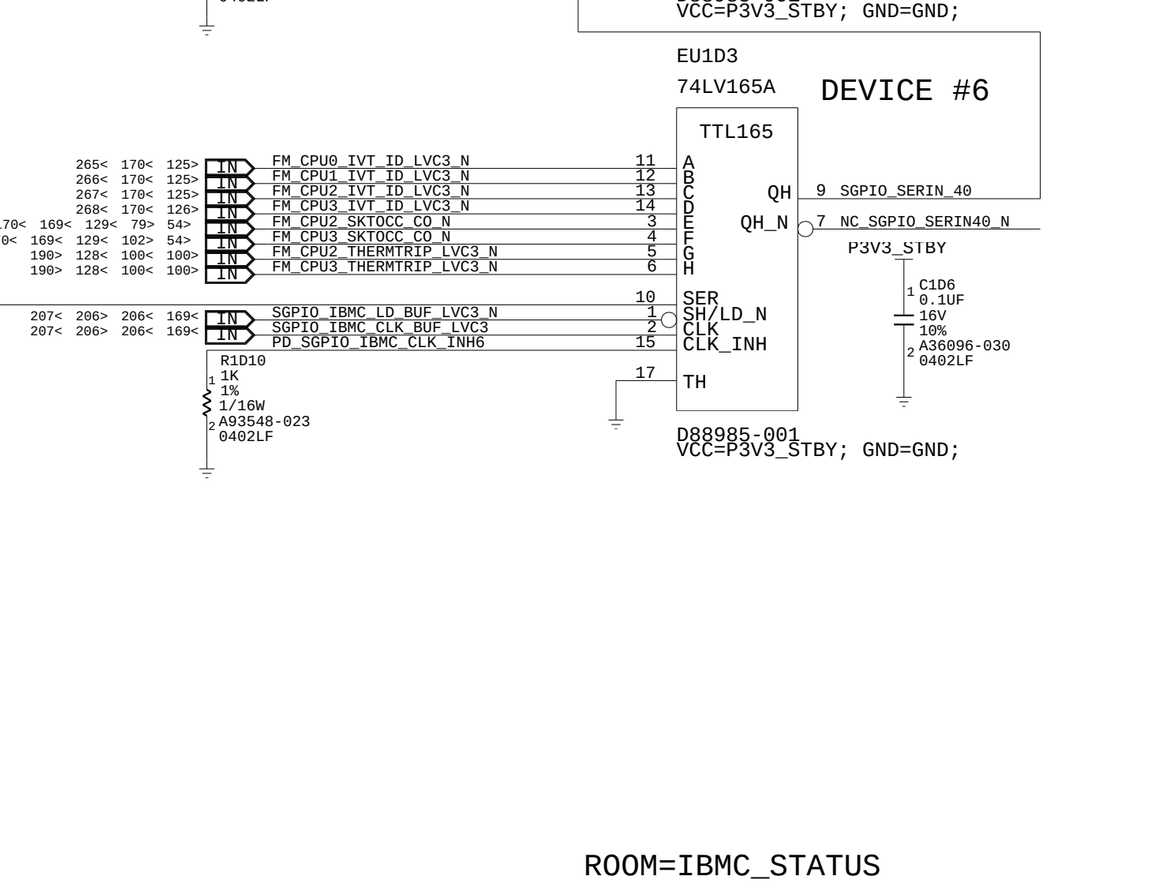
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 205 OF 303	

INTEL CONFIDENTIAL









ROOM=IBMC_STATUS

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LEDS & STATUS (3 OF 6)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 206 OF 303	

INTEL CONFIDENTIAL

EU9N1
74LV165A
DEVICE #1

TTL165

170< 169< 129< 54> 33> FM_CPU0_SKTOCC_CO_N 11 A
170< 169< 133< 129< 56> 54> FM_CPU1_SKTOCC_CO_N 12 B
190> 128< 100< 100> FM_CPU0_THERMTRIP_LVC3_N 13 C
190> 128< 100< 100> FM_CPU1_THERMTRIP_LVC3_N 14 D
233> 208< IRQ_VCCP_CPU0_VRHOT_N 3 E
238> 208< IRQ_VCCP_CPU1_VRHOT_N 4 F
253> 209< IRQ_CPU0_MEM_VRHOT_N 5 G
6 H

QH 9 SGPIO_IBMC_DIN_LVC3 OUT 177<
QH_N 7 NC_SGPIO_SERIN0_N
P3V3_STBY
C9N20 0.1UF 16V 10% A36096-030 0402LF

207< 206> 206< 169< SGPIO_IBMC_LD_BUF_LVC3_N 1 SH/LD_N
207< 206> 206< 169< SGPIO_IBMC_CLK_BUF_LVC3 2 CLK
PD_SGPIO_IBMC_CLK_INH1 15 CLK_INH
10 SER
17 TH

R9P1 1K 1% 1/16W A93548-023 0402LF

D88985-001
VCC=P3V3_STBY; GND=GND;

EU9P2
74LV165A
DEVICE #2

TTL165

256> 209< IRQ_CPU1_MEM_VRHOT_N 11 A
190> 130< 122> FM_CPU0_PROCHOT_LVC3_N 13 C
190> 130< 122> FM_CPU1_PROCHOT_LVC3_N 14 D
190> 123> FM_CPU0_MEMAB_HOT_LVC3_N 3 E
190> 123> FM_CPU0_MEMCD_HOT_LVC3_N 4 F
190> 123> FM_CPU1_MEMEF_HOT_LVC3_N 5 G
190> 123> FM_CPU1_MEMGH_HOT_LVC3_N 6 H

QH 9 SGPIO_SERIN_8
QH_N 7 NC_SGPIO_SERIN8_N
P3V3_STBY
C1D3 0.1UF 16V 10% A36096-030 0402LF

207< 206> 206< 169< SGPIO_IBMC_LD_BUF_LVC3_N 1 SH/LD_N
207< 206> 206< 169< SGPIO_IBMC_CLK_BUF_LVC3 2 CLK
PD_SGPIO_IBMC_CLK_INH2 15 CLK_INH
10 SER
17 TH

R9P16 1K 1% 1/16W A93548-023 0402LF

D88985-001
VCC=P3V3_STBY; GND=GND;

EU9P3
74LV165A
DEVICE #3

TTL165

210> FM_SYS_FAN_PRSNT_0_N 11 A
210> FM_SYS_FAN_PRSNT_1_N 12 B
210> FM_SYS_FAN_PRSNT_2_N 13 C
210> FM_SYS_FAN_PRSNT_3_N 14 D
210> FM_SYS_FAN_PRSNT_4_N 3 E
210> FM_SYS_FAN_PRSNT_5_N 4 F
TP_SYS_FAN_PRSNT_6_N 5 G
TP_SYS_FAN_PRSNT_7_N 6 H

QH 9 SGPIO_SERIN_16
QH_N 7 NC_SGPIO_SERIN16_N
P3V3_STBY
C9P6 0.1UF 16V 10% A36096-030 0402LF

207< 206> 206< 169< SGPIO_IBMC_LD_BUF_LVC3_N 1 SH/LD_N
207< 206> 206< 169< SGPIO_IBMC_CLK_BUF_LVC3 2 CLK
PD_SGPIO_IBMC_CLK_INH3 15 CLK_INH
10 SER
17 TH

R9P21 1K 1% 1/16W A93548-023 0402LF

D88985-001
VCC=P3V3_STBY; GND=GND;

EU9P4
74LV165A
DEVICE #4

TTL165

189> 100< 46> FM_SKT0_DIMM_A1_EVENT_N 11 A
189> 100< 47> FM_SKT0_DIMM_B1_EVENT_N 12 B
189> 100< 48> FM_SKT0_DIMM_C1_EVENT_N 13 C
189> 100< 49> FM_SKT0_DIMM_D1_EVENT_N 14 D
189> 100< 69> FM_SKT1_DIMM_E1_EVENT_N 3 E
189> 100< 70> FM_SKT1_DIMM_F1_EVENT_N 4 F
189> 100< 71> FM_SKT1_DIMM_G1_EVENT_N 5 G
189> 100< 72> FM_SKT1_DIMM_H1_EVENT_N 6 H

QH 9 SGPIO_SERIN_24
QH_N 7 NC_SGPIO_SERIN24_N
P3V3_STBY
C1D10 0.1UF 16V 10% A36096-030 0402LF

206> SGPIO_SERIN_32 10 SER
206< 169> SGPIO_IBMC_LD_GATE_LVC3_N 1 SH/LD_N
207< 206> 206< 169< SGPIO_IBMC_CLK_BUF_LVC3 2 CLK
PD_SGPIO_IBMC_CLK_INH4 15 CLK_INH
17 TH

R9P34 1K 1% 1/16W A93548-023 0402LF

D88985-001
VCC=P3V3_STBY; GND=GND;

ROOM=IBMC_STATUS

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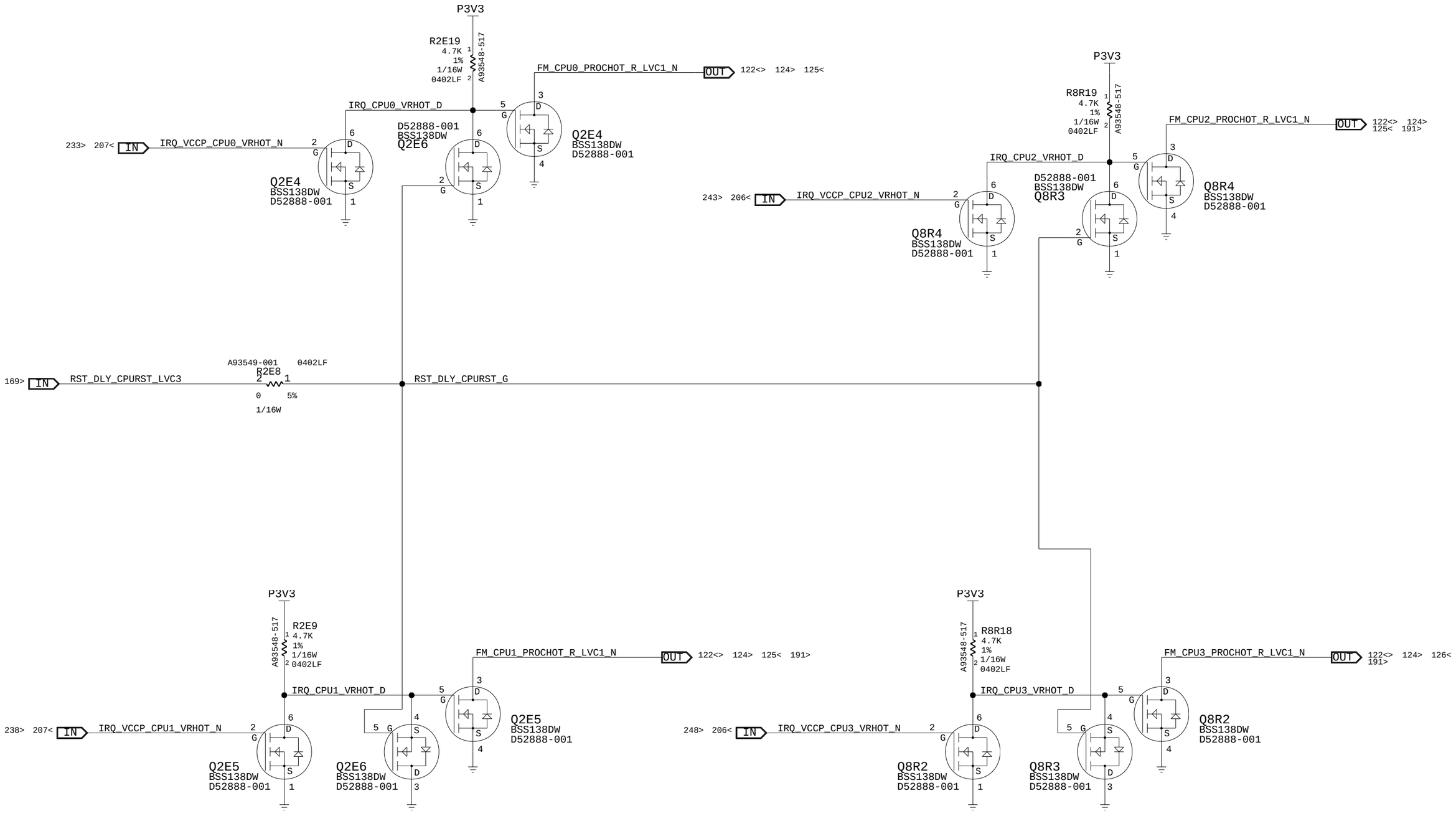
LEDS & STATUS (4 OF 6)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 207 OF 303	

INTEL CONFIDENTIAL



ROOM=IBMC_STATUS

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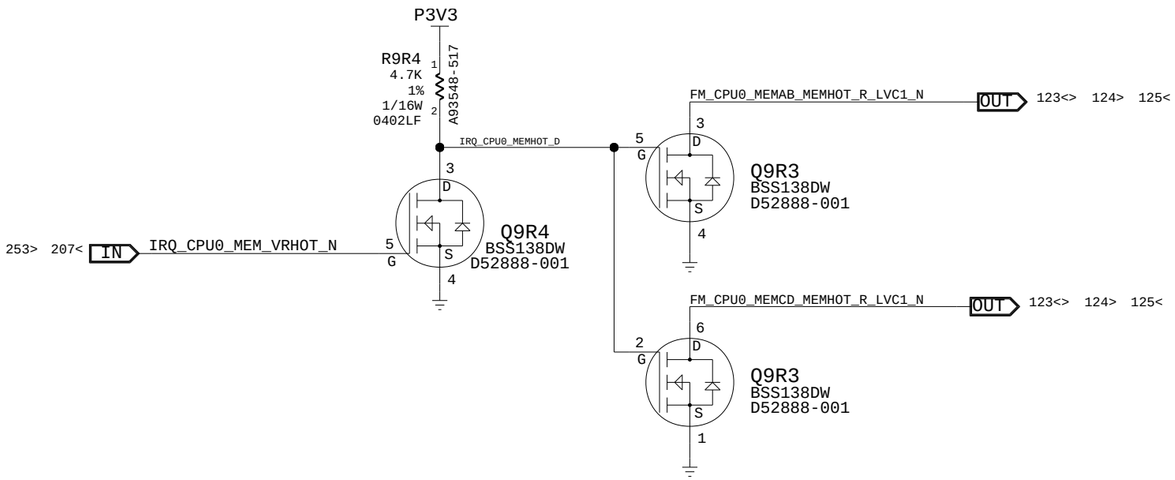
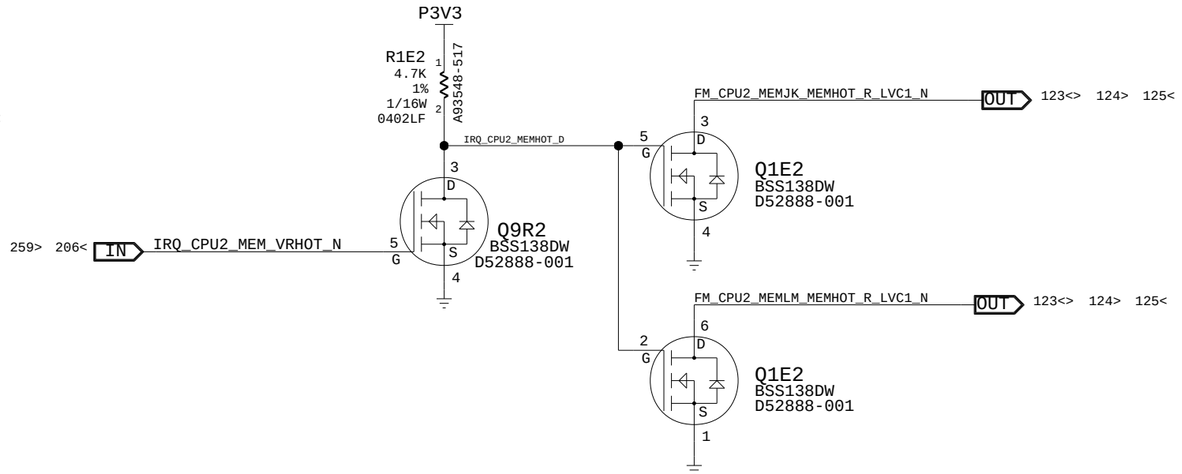
LEDS & STATUS (5 OF 6)

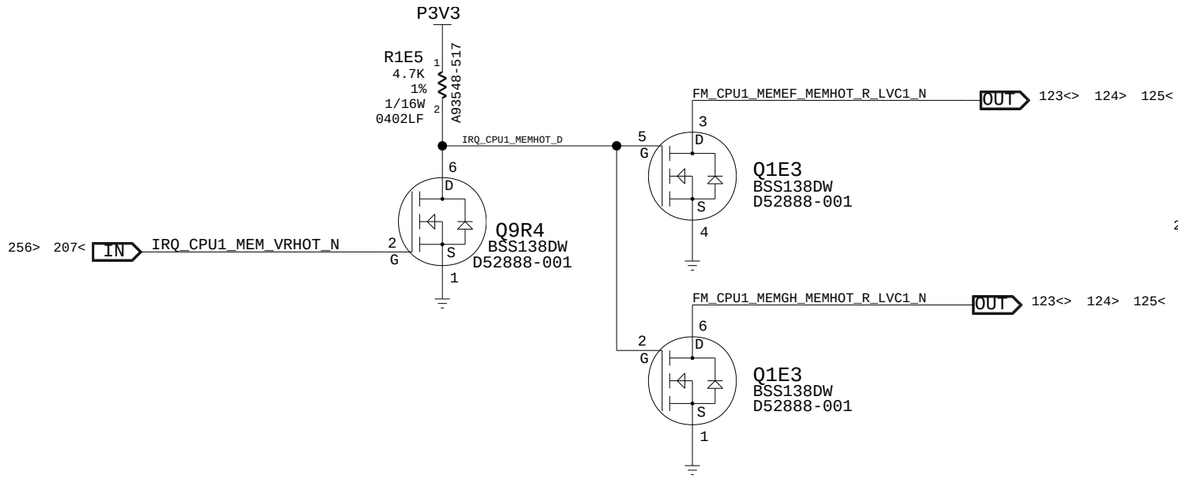
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 208 OF 303	

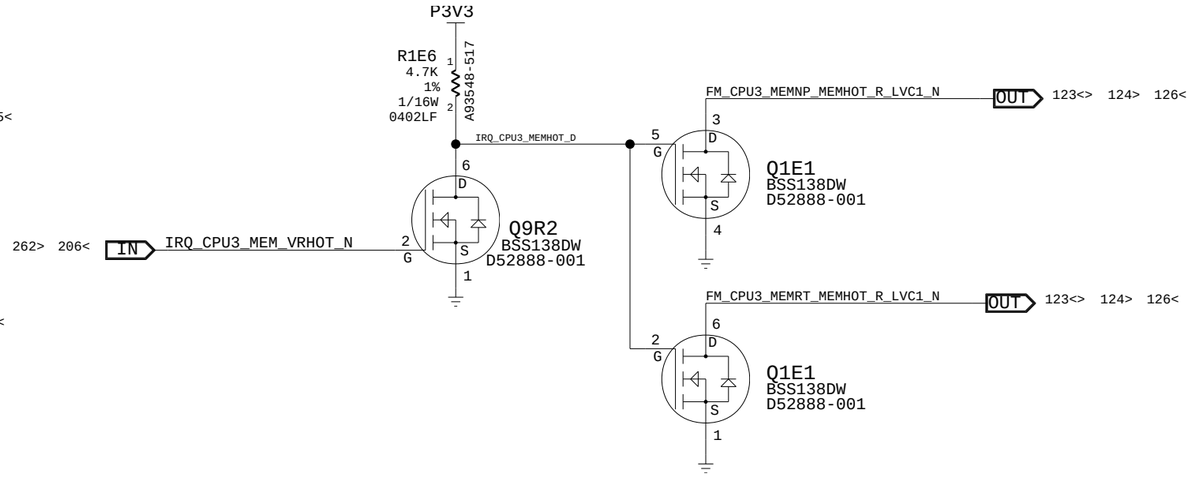
INTEL CONFIDENTIAL

ROOM=IBMC_STATUS









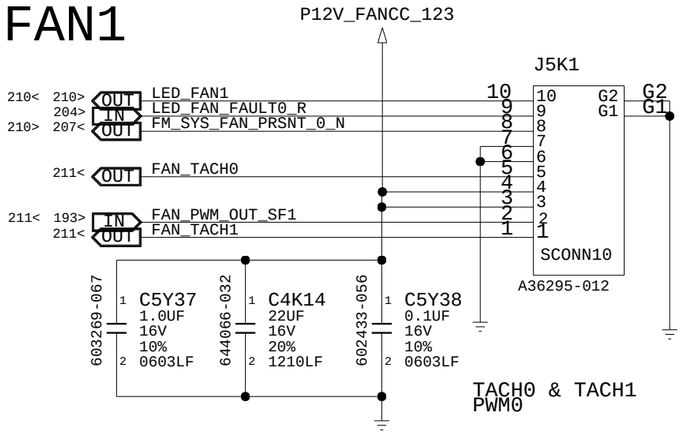
Wed Oct 27 15:21:52 2010

LEDS & STATUS (6 OF 6)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 209 OF 303	

INTEL CONFIDENTIAL

FAN1



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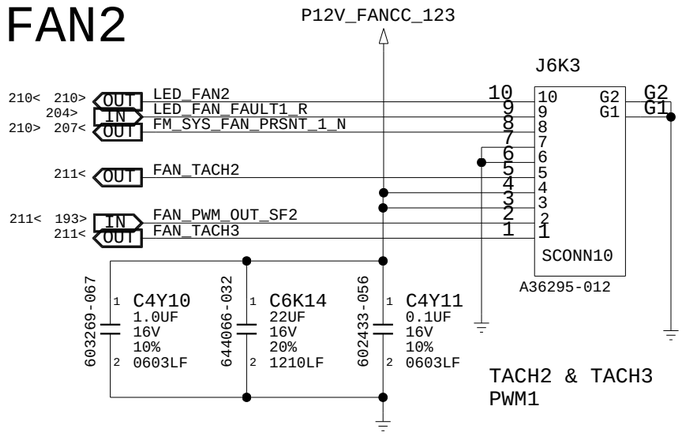

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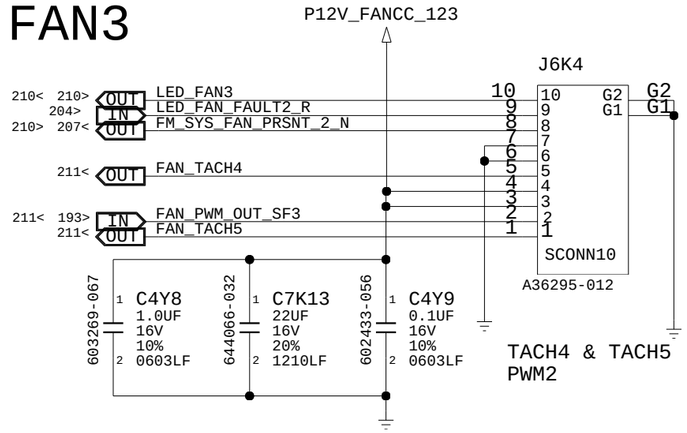

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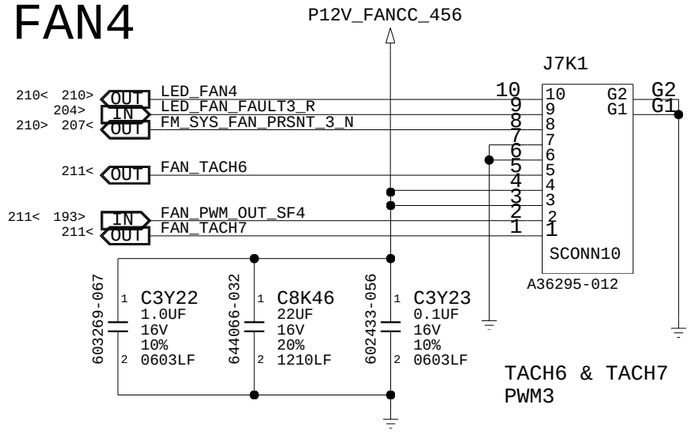

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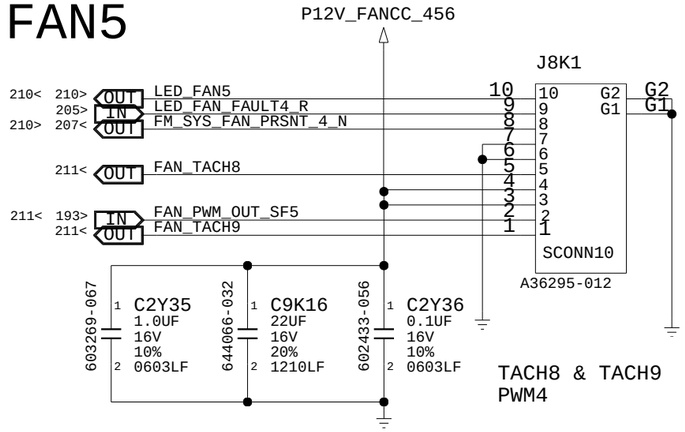

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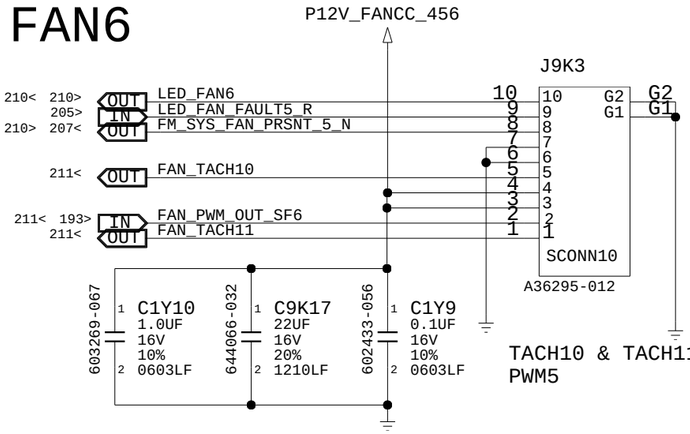

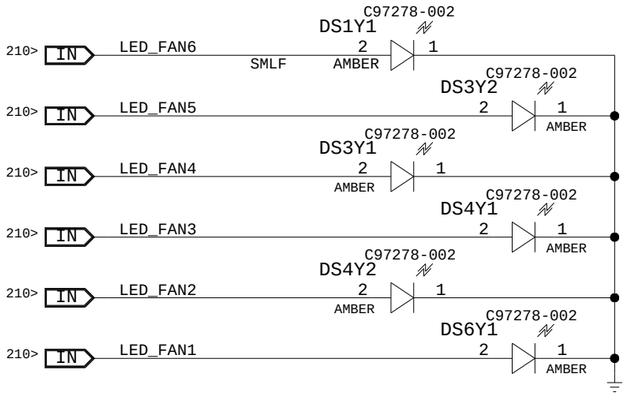

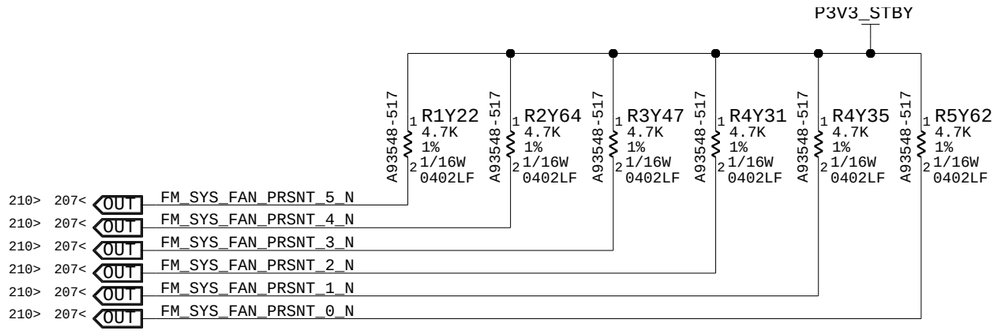

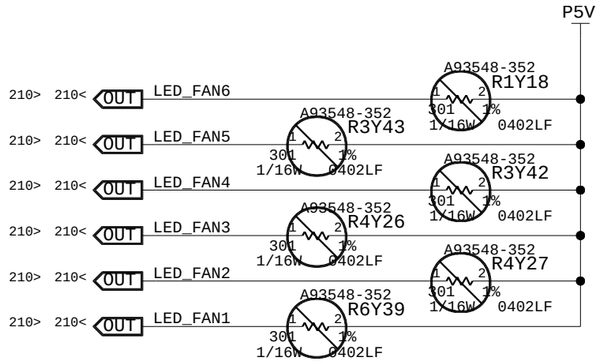

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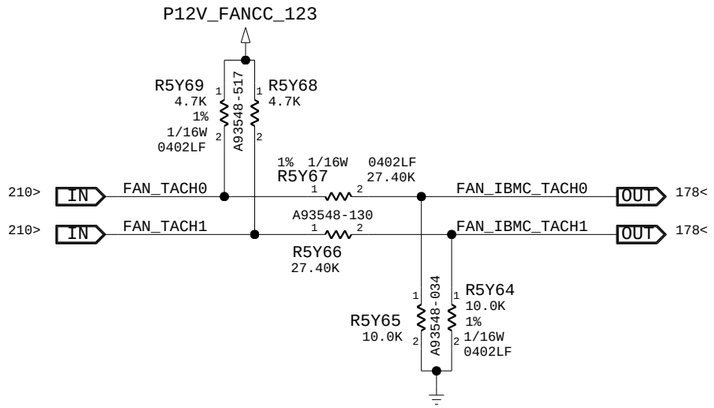
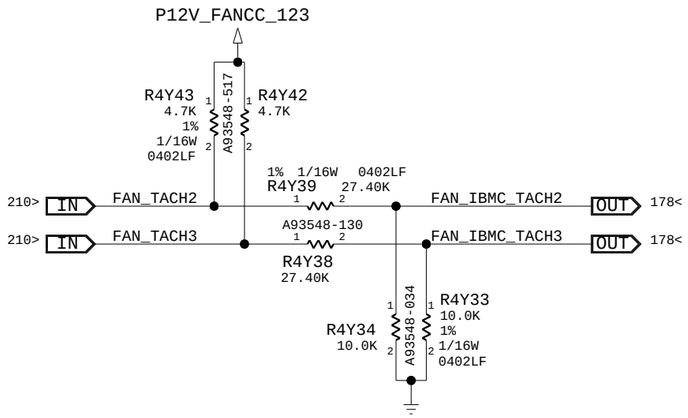
Wed Oct 27 15:21:52 2010

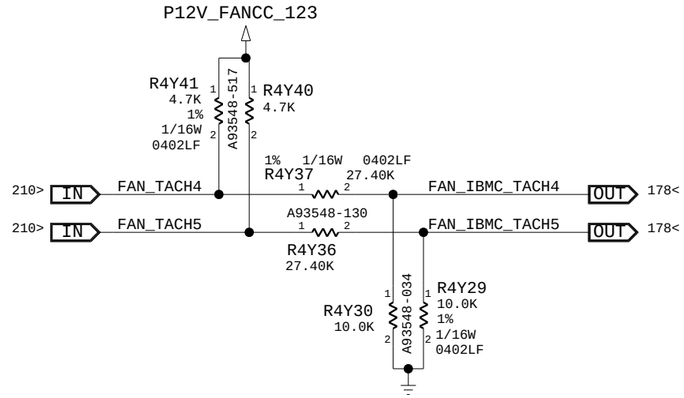
CLOSED CHASSIS FANS (1 OF 3)

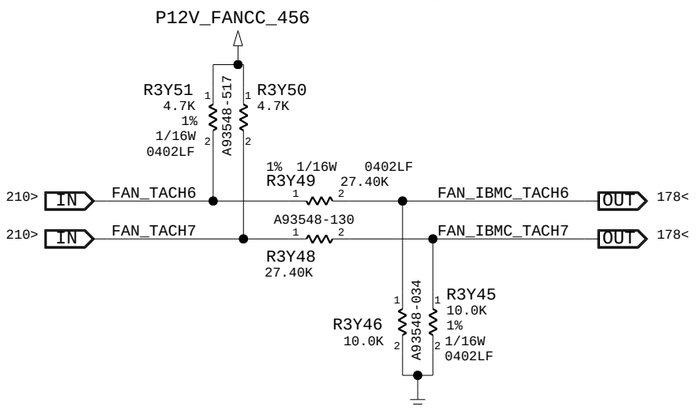
DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 210 OF 303

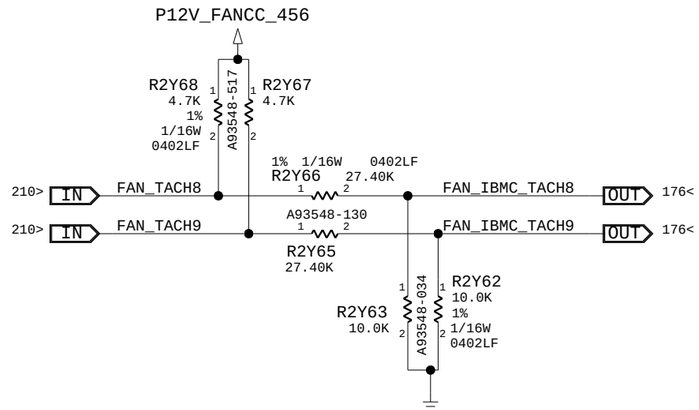
INTEL CONFIDENTIAL

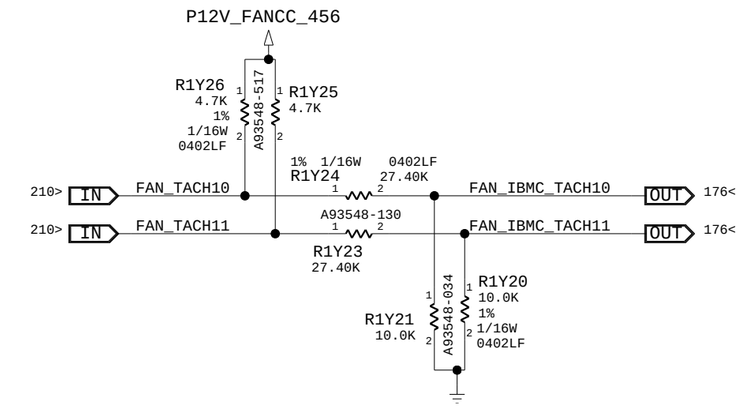


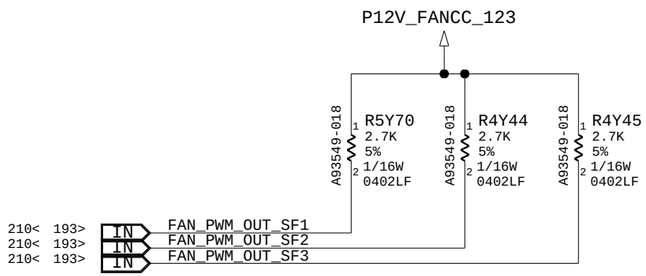


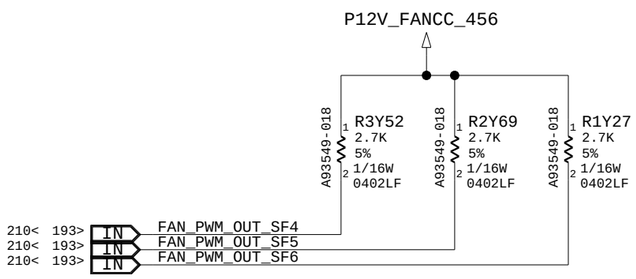












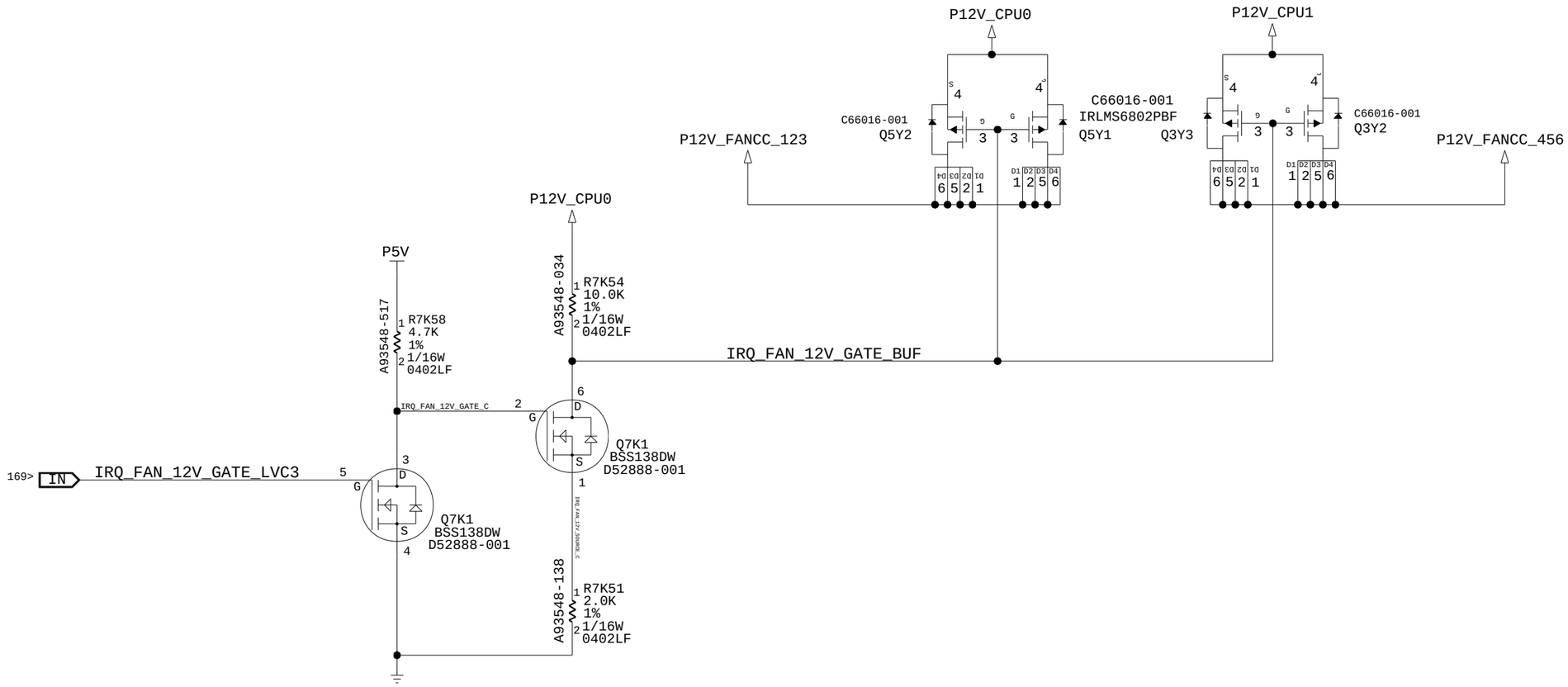
ROOM=IBMC_FAN_CLOSE_CHASSIS

Wed Oct 27 15:21:53 2010

CLOSED CHASSIS FANS (2 OF 3)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 211 OF 303	

INTEL CONFIDENTIAL



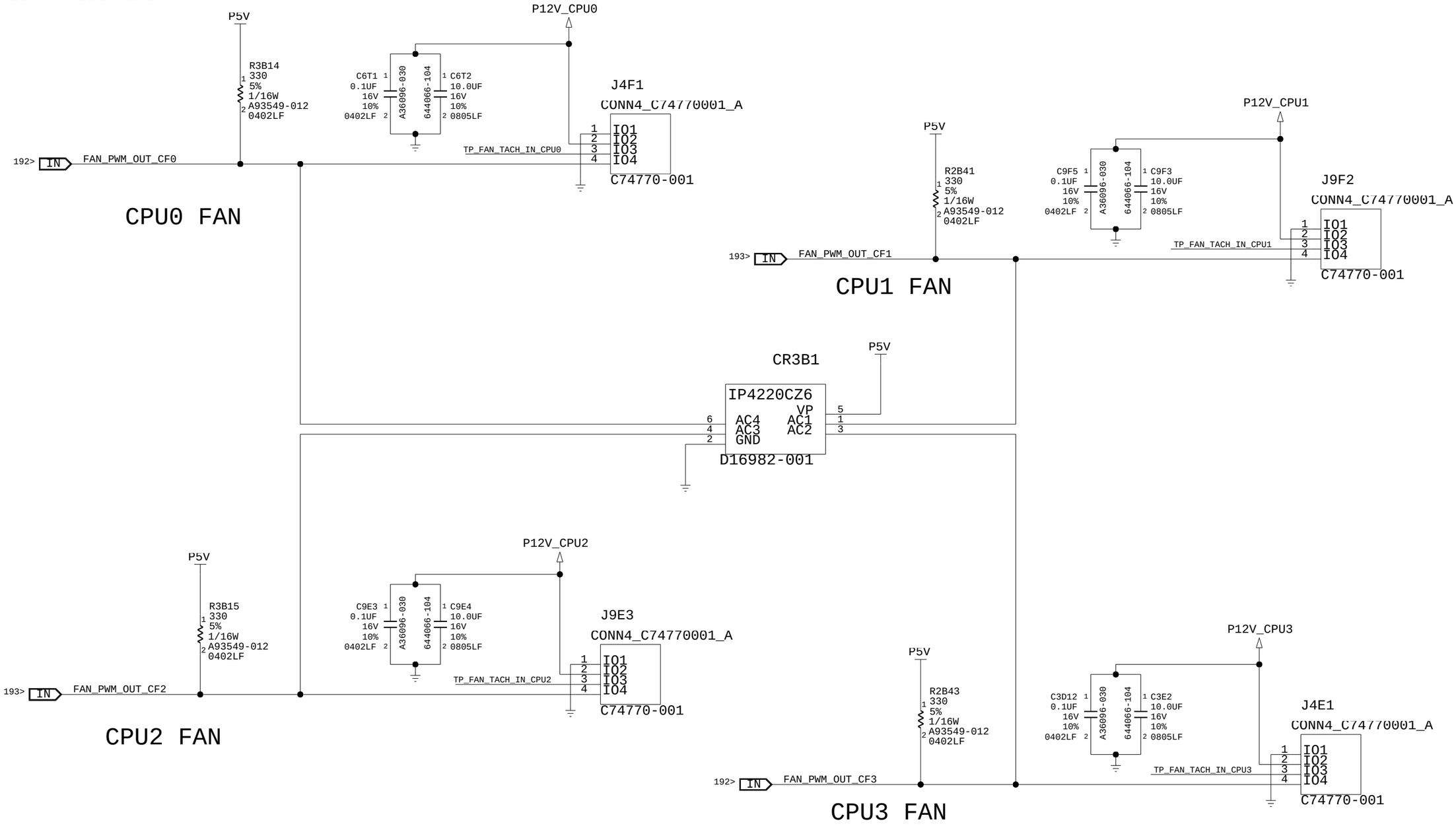
ROOM=IBMC_FAN_CLOSE_CHASSIS

Wed Oct 27 15:21:53 2010

CLOSED CHASSIS FANS (3 OF 3)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 212 OF 303

INTEL CONFIDENTIAL



ROOM=IBMC_FAN_CPU_HS

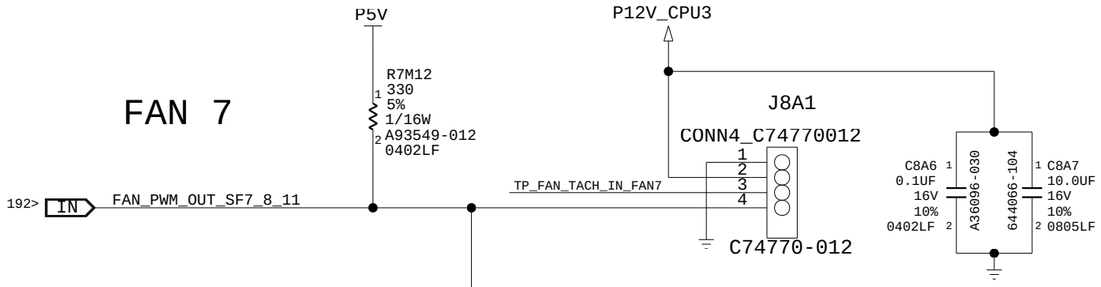
Wed Oct 27 15:21:53 2010

OPEN CHASSIS FANS (1 OF 2)

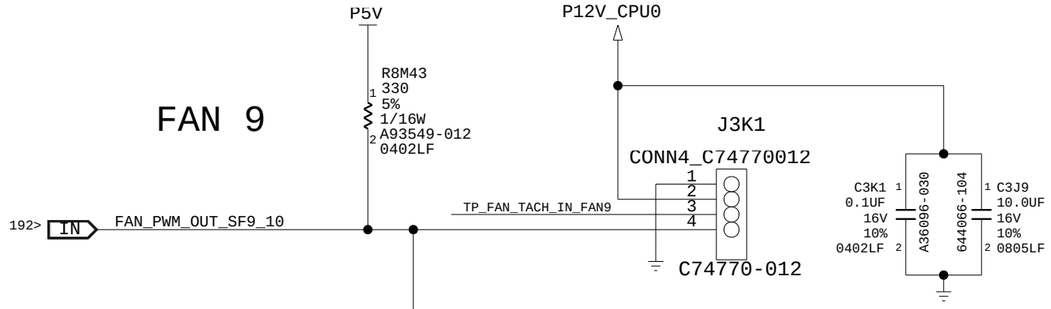
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 213 OF 303	

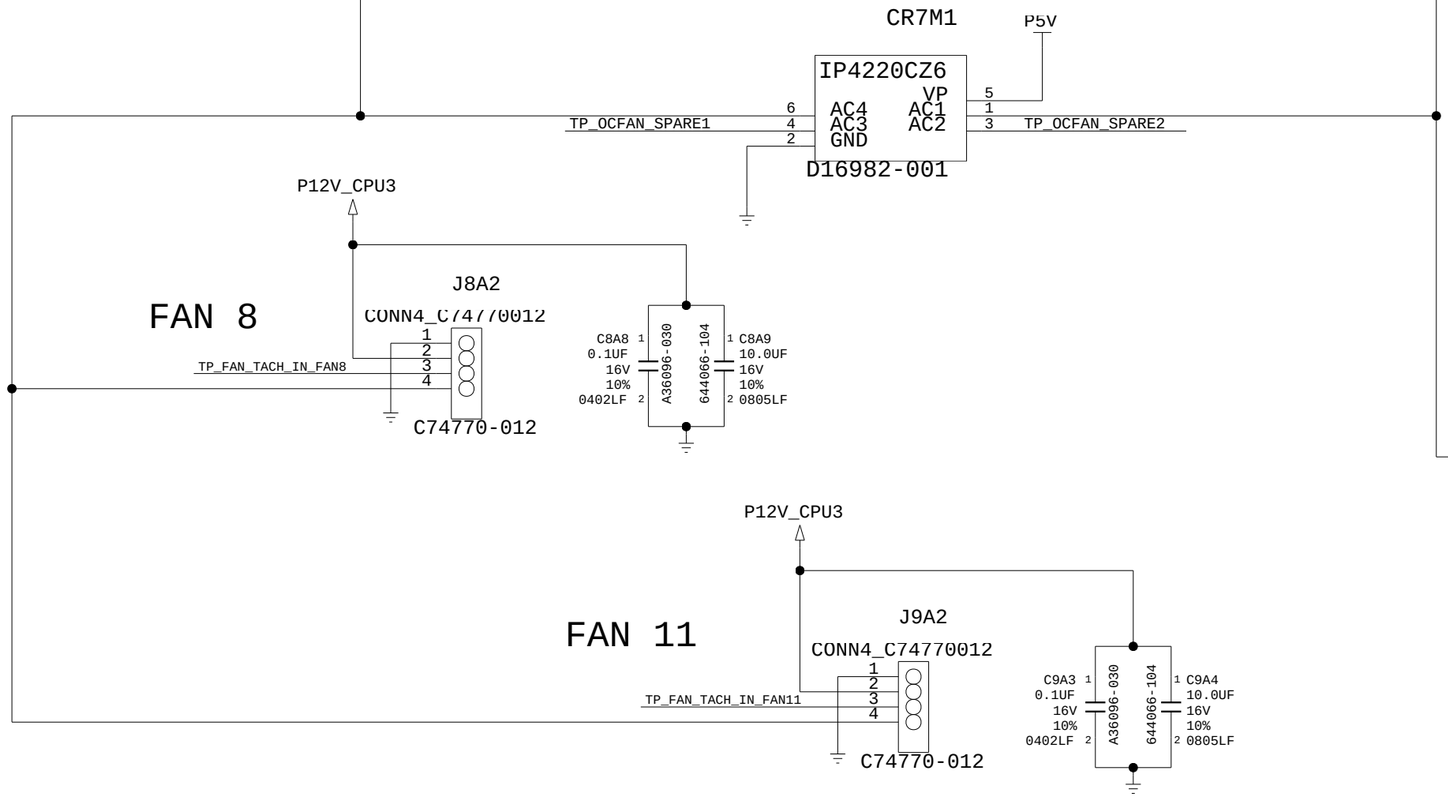
INTEL CONFIDENTIAL

FAN 7



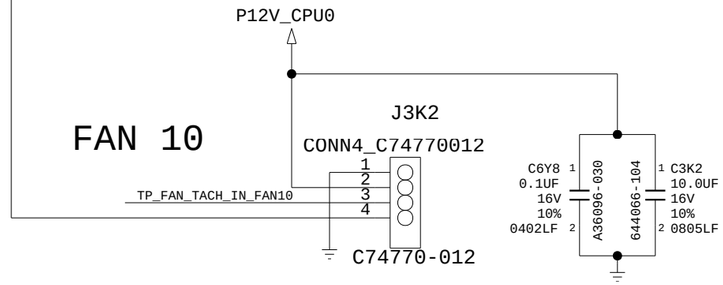
FAN 9





FAN 8

FAN 11



FAN 10

ROOM=IBMC_FAN_OPEN_CHASSIS

Wed Oct 27 15:21:53 2010

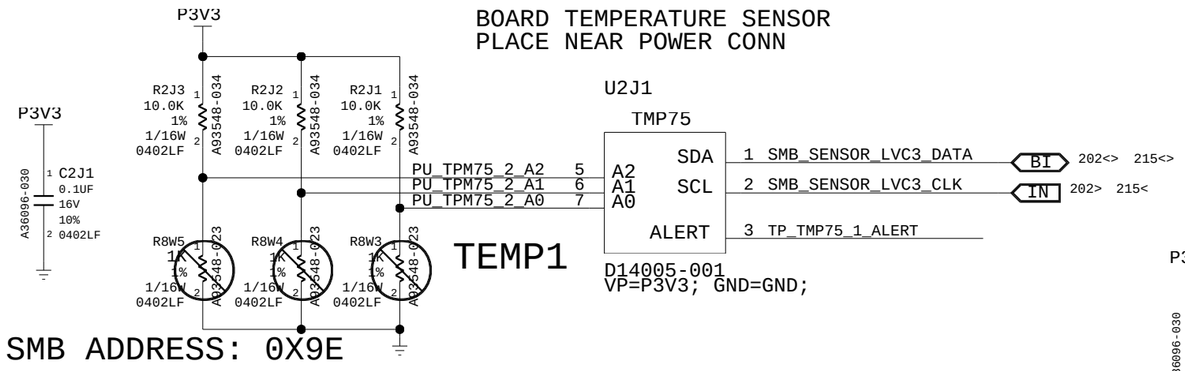
OPEN CHASSIS FANS (2 OF 2)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 214 OF 303	

INTEL CONFIDENTIAL

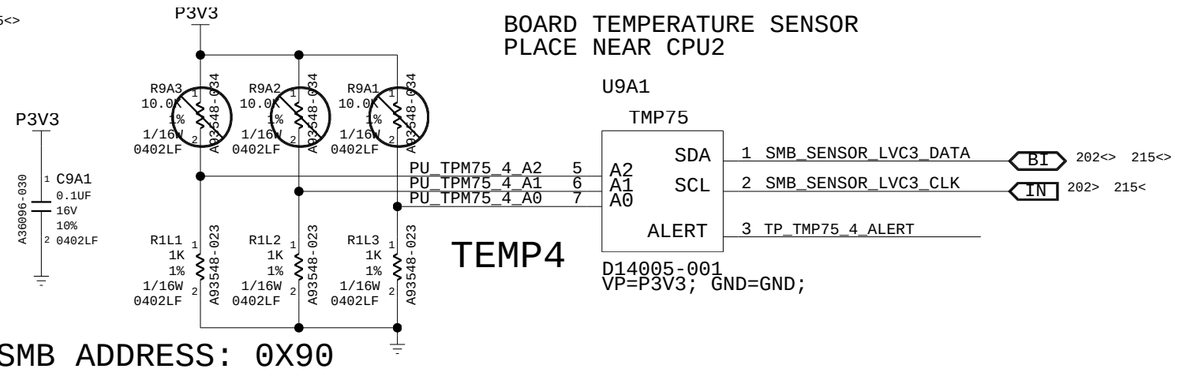
CAD NOTE: PLACE CAPACITORS NEAR THE CORRESPONDING CHIP

BOARD TEMPERATURE SENSOR PLACE NEAR POWER CONN



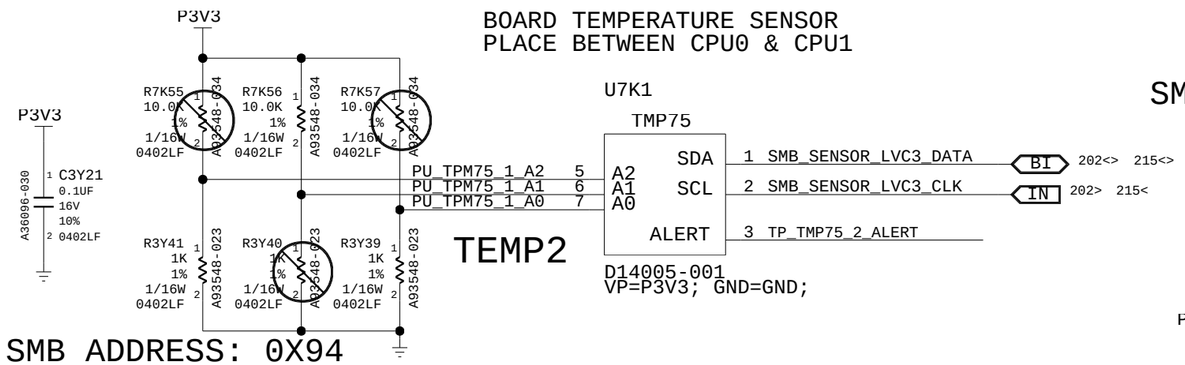
SMB ADDRESS: 0X9E

BOARD TEMPERATURE SENSOR PLACE NEAR CPU2



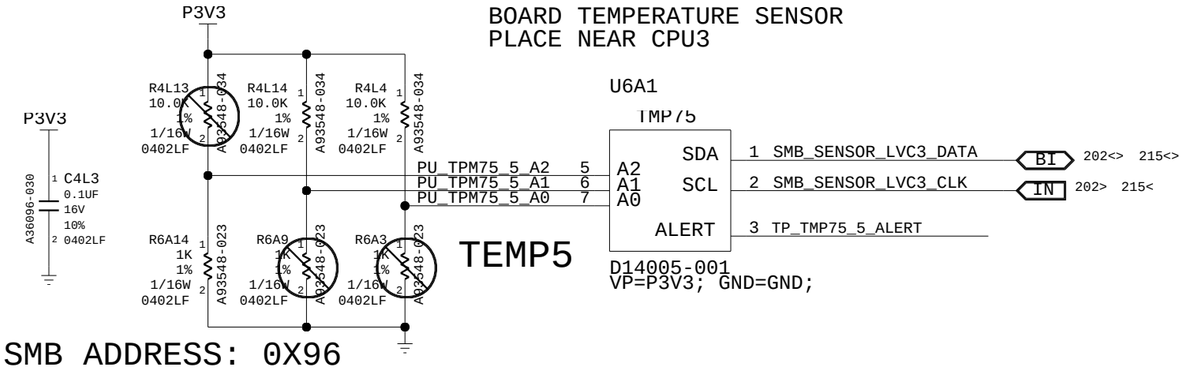
SMB ADDRESS: 0X90

BOARD TEMPERATURE SENSOR PLACE BETWEEN CPU0 & CPU1



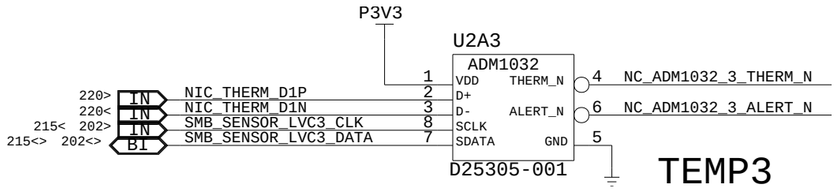
SMB ADDRESS: 0X94

BOARD TEMPERATURE SENSOR PLACE NEAR CPU3



SMB ADDRESS: 0X96

BOARD TEMPERATURE SENSOR PLACE NEAR IBMC/TWINVILLE



SMB ADDRESS: 0X98

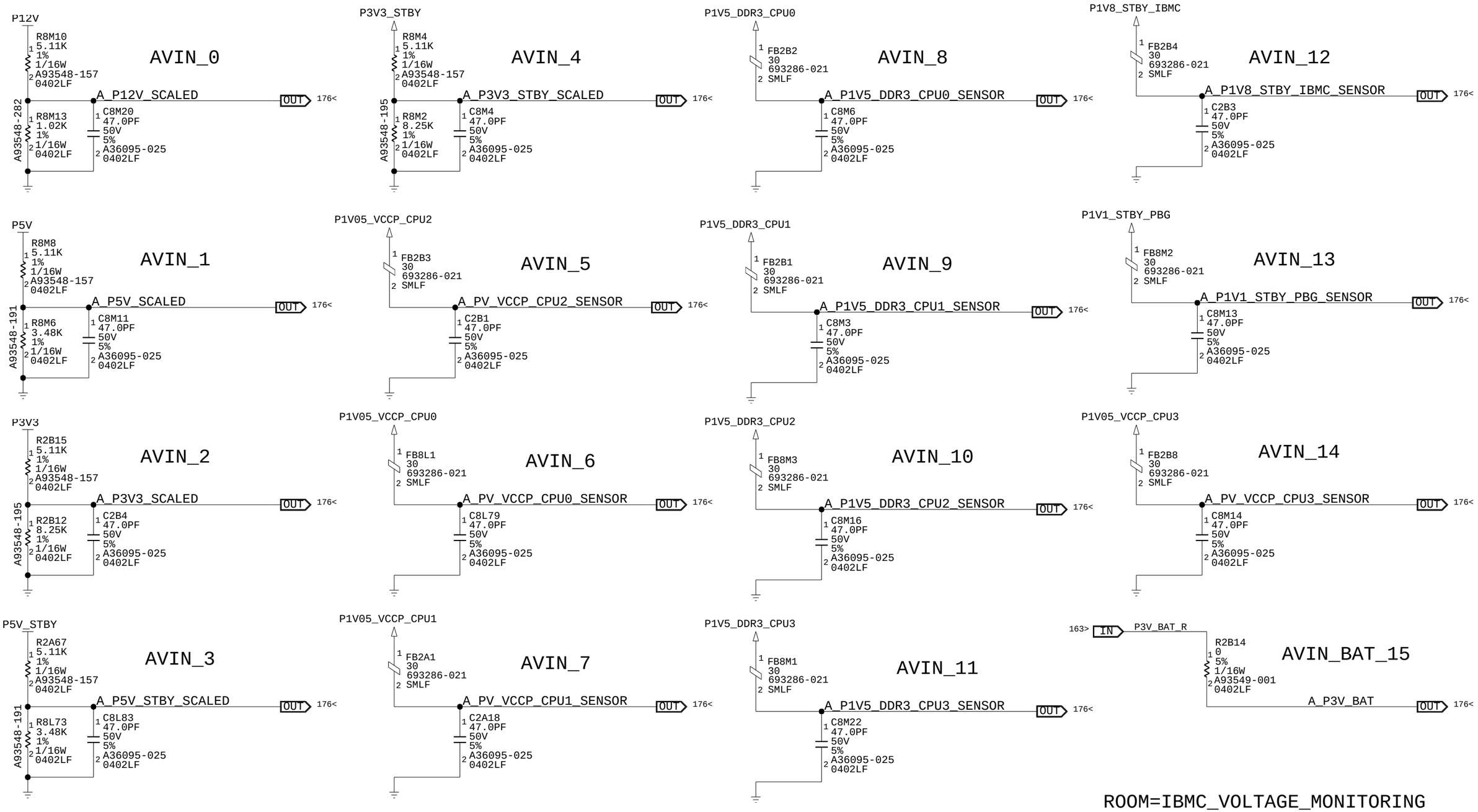
ROOM=IBMC_TEMP_SENSORS

Wed Oct 27 15:21:53 2010

TEMPERATURE SENSORS

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 215 OF 303	

INTEL CONFIDENTIAL



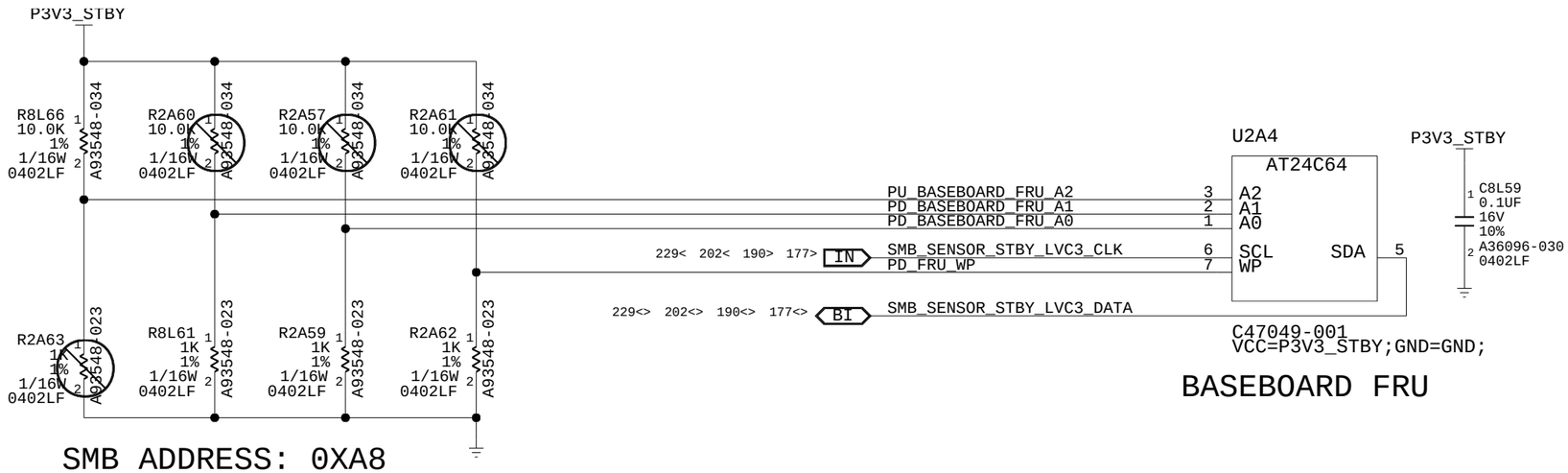
ROOM=IBMC_VOLTAGE_MONITORING

Wed Oct 27 15:21:53 2010

VOLTAGE MONITORING

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 216 OF 303	

INTEL CONFIDENTIAL



ROOM=IBMC_BB_FRU_MEM

BASEBOARD FRU MEMORY

Wed Oct 27 15:21:54 2010

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 217 OF 303	

INTEL CONFIDENTIAL

U3B1
IC

TWINVILLE_EXT_B

226<> BI	NIC_A_MDI_DP<4>	A11	MDI0_4P	LED0_3	K4	NIC0_LED03_1G_LVT2	OUT 226<
226<> BI	NIC_A_MDI_DN<4>	B11	MDI0_4N	LED0_2	J4	NIC0_LED02_ACT_LVT2	OUT 226< 226<> 230<
	NIC_A_MDI_DP<3>	A9	MDI0_3P	LED0_1	J3	NIC0_LED01_10G_LVT2	OUT 226<
	NIC_A_MDI_DN<3>	B9	MDI0_3N	LED0_0	H4	NIC0_LED00_LINKUP_LVT2	OUT 226< 230<
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	NIC_B_MDI_DN<0>	B22	MDI1_0N				
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228< 225> IN	P2E_CPU0_TWV_TX_PE2C_C_DN<3..0>	AC12	PER_3N	PET_3N	AD10	P2E_CPU0_TWV_RX_PE2C_DN<3>	3
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31> IN	CLK_100M_LAN_DN	Y1	PE_CLKN				
	NIC_PE_RBIAS_1	V2	PE_RBIAS1				
	NIC_PE_RBIAS_0	V1	PE_RBIAS0				
175< 169< 156< IN	RST_IBMC_NIC_LRESET_LVC3_N	W2	PE_RST_N	PE_WAKE_N	W1	IRQ_SSB_WAKE_LVC3_N	OUT 135< 171>

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E87345-001

R2B27 3.3K 5% 1/16W CHIP A93549-019 0402LF — R3B9 3.3K 5% 1/16W CHIP A93549-019 0402LF

POPULATE THESE RESISTORS
R & R
IF TWINVILLE IS BEING USED

UNPOPULATE
IF I350 IS BEING USED

P2E_CPU0_TWV_RX_PE2D_DP<3..0> OUT 225<
P2E_CPU0_TWV_RX_PE2D_DN<3..0> OUT 225<

P2E_CPU0_TWV_RX_PE2C_DP<3..0> OUT 225<
P2E_CPU0_TWV_RX_PE2C_DN<3..0> OUT 225<

A93548-014 R8M36 1.50K 1% 1/16W EMPTY 0402LF

POPULATE THIS RESISTOR
IF I350 IS BEING USED

UNPOPULATE IF
TWINVILLE IS BEING USED

R2B31 3.01K 1% 1/16W CHIP A93548-024 0402LF

R2B32 3.01K 1% 1/16W CHIP A93548-024 0402LF

POPULATE THESE RESISTORS
R2B31 & R2B32
IF TWINVILLE IS BEING USED

UNPOPULATE
IF I350 IS BEING USED

CAD NOTE:
PLACE CLOSE TO SILICON. TOTAL
PE_RBIAS0, PE_RBAIS1
TRACE LENGTH SHOULD BE
LESS THAN 1 INCH.

ROOM=NIC

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TWINVILLE (1 OF 7)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 218 OF 303	

INTEL CONFIDENTIAL

U3B1
IC

TWINVILLE_EXT_B

224> 176>	IN	RMII_IBMC_NIC_R_TXD<1>	G3	NCSI_TXD1	NCSI_RXD1	G1	RMII_NIC_IBMC_RXD<0>	OUT	176< 224>
224> 176>	IN	RMII_IBMC_NIC_R_TXD<0>	H2	NCSI_TXD0	NCSI_RXD0	H3	RMII_NIC_IBMC_RXD<1>	OUT	176< 224>
224> 176>	IN	RMII_IBMC_NIC_TX_R_EN	G4	NCSI_TX_EN	NCSI_RX_DV	H1	RMII_NIC_IBMC_CRS_DV	OUT	176< 224>
224> 32>	IN	CLK_50M_TWN	G2	NCSI_CLK_IN					
		NC_I350_RSVDF1	F1	NCSI_ARB_IN	NCSI_ARB_OUT	F2	NC_I350_RSVDF2		
224>	IN	SPI_NIC_EE_R_SO	K1	FLSH_SO	FLSH_SI	K2	SPI_NIC_EE_SI	OUT	224<
219<	BI	NIC_BG_REXT	D12	BG_REXT	FLSH_SCK	J1	SPI_NIC_EE_CLK	OUT	224<
219<	BI	NIC_TM_REXT	C12	TM_REXT	FLSH_CE_N	J2	SPI_NIC_EE_CE_N	OUT	224<
219>	IN	NIC_SEC_EN	M1	SEC_EN					
219>	IN	NIC_LAN_PWR_GOOD	L24	LAN_PWR_GOOD	SMBD	L1	SMB_LAN_STBY_LVC3_DATA	BI	139<> 177<> 190<>
219>	IN	NIC_AUX_PWR	P2	AUX_PWR	SMBCLK	L2	SMB_LAN_STBY_LVC3_CLK	BI	139<> 177> 190>
219> 204< 177< 169> 147>	IN	PWRGD_PCH_PWROK_LVC3	R2	MAIN_PWR_OK	SMBALRT_N	M2	SMB_LAN_STBY_LVC3_ALRT_N		
219>	IN	NIC_BYPASS_POR	H23	BYPASS_POR					
224> 219>	IN	NIC_LAN1_DIS_N	K24	LAN1_DIS_N					
219> 136>	IN	FM_SSB_LAN0_DISABLE_N	K23	LAN0_DIS_N					
219>	IN	JTAG_NIC_TDI	W22	TDI	TDO	V22	JTAG_NIC_TDO	OUT	219<
219>	IN	JTAG_NIC_TRST_LVC2_N	W23	TRST_N					
219>	IN	JTAG_NIC_TCK	Y22	TCK					
219>	IN	JTAG_NIC_TMS	W21	TMS					
219>	IN	XTAL_I_50M_NIC	D23	XTAL_I	XTAL_O	D24	XTAL_O_50M_NIC	OUT	219<

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E87345-001

CAD NOTE: RBIAS RESISTORS FOR BOTH PORTS 0 AND 1 SHOULD BE PLACED LESS THAN 1 INCH AWAY FROM LAN SILICON.

P2V6_TVL_P3V3_BHPC_AUX

R7L19
140 1% 1/16W CHIP
A93548-579 0402

NIC_TM_REXT BI 219<>

R7L20
2.0K 1/16W 1% CHIP
A93548-138 0402LF

NIC_BG_REXT BI 219<>

FOR I350 REMOVE THIS RESISTOR

FOR I350 CHANGE THIS RESISTOR TO A 3.01 KOHMS 1% IPN: A93548-024

FOR TVL CHANGE A 2.0 KOHMS 1% IPN: A93548-138

P3V3_STBY

R2B19
10.0K 1% 1/16W CHIP
A93548-034 0402LF

IF SM_BUS IS NOT USED SMB_CLK AND SMB_DAT ADJUSTED BY SYSTEM STILL NEED TO BE BE PULLED UP TO 3.3V

PULL UPS FOR DATA AND CLK WERE MOVED TO PAGE 190

P2V6_TVL_P3V3_BHPC_AUX

R3A7
3.3K 5% 1/16W CHIP
A93549-019 0402LF

J3A2
CONN
CONN3

219< OUT NIC_BYPASS_POR_PU 1
NIC_BYPASS_POR 2
NIC_BYPASS_POR_PD 3

C95678-002

R7M4
10.0K 1% 1/16W CHIP
A93548-034 0402LF

P2V6_TVL_P3V3_BHPC_AUX

R3A3
10.0K 1% A93548-034 0402LF

J3A1
CONN
CONN3

219< OUT NIC_LAN_PWR_GOOD_PU 3
169> IN NIC_LAN_PWR_GOOD 2
FM_NIC_LAN_PWR_GOOD 1

C95678-002

P2V6_TVL_P3V3_BHPC_AUX

R3B8
3.3K 5% 1/16W CHIP
A93549-019 0402LF

R3B10
10.0K 1%

R3B6
10.0K 1% 1/16W CHIP
A93548-034 0402LF

J2B3
CONN
CONN5_D31236001

219< OUT JTAG_NIC_TDI 1 IO1
219< OUT JTAG_NIC_TRST_LVC2_N 2 IO2
219< OUT JTAG_NIC_TCK 3 IO3
219< OUT JTAG_NIC_TMS 4 IO4
219> IN JTAG_NIC_TDO 5 IO5

R3B11
470 1%

R3B7
470 1% 1/16W CHIP
A93548-511 0402LF

D31236-001

CRYSTAL:
TVL = 50MHZ (C13728-030)
I350 = 25MHZ (C13728-008)

CAPS:
TVL = 18PF (A36095-042)
I350 = 33PF (A36095-031)

C13728-030
Y3A1
50.000MHZ
IC

C3A14
18PF 50V 5% C0G
A36095-042 0402LF

C3A15
18PF 50V 5% C0G
A36095-042 0402LF

CAD NOTE: TRACE LENGTHS SHOULD BE LESS THAN 0.75 IN

XTAL_I_50M_NIC OUT 219<

XTAL_O_50M_R_NIC — R1 A93549-001 0 1/16W 5% CHIP 0402LF — XTAL_O_50M_NIC IN 219>

FOR TVL USE R4A19 0 OHM 5% 0402LF IPN: A93549-001

FOR I350 REPLACE R4A19 WITH CAP: 10.0 PF 5% 0402LF IPN: A36094-025

CAD NOTE1: LOAD CAPS C3A14 & C3A15 NEED TO BE AS CLOSE TO THE CRYSTAL(Y3A1) SOLDER PADS, C5A1 & C5A2 SHOULD BE NO MORE THAN 90 MILS AWAY FROM CRYSTAL PADS

CAD NOTE2: C3A14, C3A15, Y3A1 & U3B1 MUST BE ON SAME SIDE OF BOARD, MAXIMUM OF ONE VIA TO GROUND LOAD CAPS(C5A1, C5A2) ON XTAL_O_50M_NIC & XTAL_I_50M_NIC

P2V6_TVL_P3V3_BHPC_AUX

P3V3_STBY

R2B21 10.0K 1%
R2B20 10.0K 1%
R8M22 10.0K 1%
R7M7 10.0K 1%
R8M24 10.0K 1% 1/16W EMPTY A93548-034 0402LF

219< OUT NIC_SEC_EN
224> 219< OUT NIC_LAN1_DIS_N
219< OUT NIC_AUX_PWR
219< 136> OUT FM_SSB_LAN0_DISABLE_N
219< 204< 177< 169> 147> 135< OUT PWRGD_PCH_PWROK_LVC3

ROOM=NIC

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TWINVILLE (2 OF 7)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 219 OF 303	

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P2V6_TVL_P3V3_BHPC_AUX

POPULATE R3A11 WHEN IT IS USED A0 TVL

R3A11 1
10.0K
1%
CHIP 2

PU_DFTCAP_RSVDK3 OUT 220<

R2 1
10.0K
1%
EMPTY 2

POPULATE R3A13 WHEN IT IS USED B0 TVL.

P2V6_TVL_P3V3_BHPC_AUX

R3 1
3.3K 5%
1/16W CHIP
A93549-019 2
0402LF

220> IN PU_DFTCAP_RSVDK3
220> IN NIC_RSVD_VSS<15>

NIC_RSVD_VSS_M23_PU

P2V6_TVL_P3V3_BHPC_AUX

R8M34 1
3.3K 5%
1/16W CHIP
A93549-019 2
0402LF

NIC_RSVD_VCC2P5_T2_PU T2

NIC_RSVD_VSS<15> OUT 220<

R3A13 1
3.3K
5%
CHIP 2

U3B1
IC

TWINVILLE_EXT_B

J23	RSVD_VSS<25>	RSVD_NC<59>	G21	NIC_THERM_D1P	OUT	215<	
AD24	RSVD_VSS<24>	RSVD_NC<58>	G22	NIC_THERM_D1N	IN	215<	
A24	RSVD_VSS<23>	RSVD_NC<57>	F4	NC_I350_TSENSP			
H22	RSVD_VSS<22>	RSVD_NC<56>	F3	NC_I350_TSENSZ			
G23	RSVD_VSS<21>	RSVD_NC<55>	A1	NC_I350_RSVDA1			
D14	RSVD_VSS<20>	RSVD_NC<54>	C11	NC_I350_RSVDC11			
J24	RSVD_VSS<19>	RSVD_NC<53>	C13	NC_I350_RSVDC13			
P23	RSVD_VSS<18>	RSVD_NC<52>	D1	NC_I350_RSVDD1			
V21	RSVD_VSS<17>	RSVD_NC<51>	AA8	NC_I350_RSVDAA8			
K3	RSVD_VSS<16>	RSVD_NC<50>	D11	NC_I350_RSVDD11			
G24	RSVD_VSS<15>	RSVD_NC<49>	D13	NC_I350_RSVDD13			
H24	RSVD_VSS<14>	RSVD_NC<48>	E1	NC_I350_RSVDE1			
W4	RSVD_VSS<13>	RSVD_NC<47>	E24	NC_I350_RSVDE24			
Y21	RSVD_VSS<12>	RSVD_NC<46>	C1	NC_I350_RSVDC1			
M23	RSVD_VSS<11>	RSVD_NC<45>	F24	NC_I350_RSVDF24			
M24	RSVD_VSS<10>	RSVD_NC<44>	E23	NC_I350_RSVDE23			
N23	RSVD_VSS<9>	RSVD_NC<43>	G11	NC_I350_RSVDG11			
N24	RSVD_VSS<8>	RSVD_NC<42>	L21	NC_I350_RSVDL21			
P24	RSVD_VSS<7>	RSVD_NC<41>	L22	NC_I350_RSVDL22			
Y4	RSVD_VSS<6>	RSVD_NC<40>	L3	NC_I350_NCSI_CLKOUT			
T23	RSVD_VSS<5>	RSVD_NC<39>	L4	NC_I350_RSVDL4			
T24	RSVD_VSS<4>	RSVD_NC<38>	M21	NC_I350_RSVDM21			
W24	RSVD_VSS<3>	RSVD_NC<37>	L23	NC_I350_RSVDL23			
AA24	RSVD_VSS<2>	RSVD_NC<36>	M12	NC_I350_RSVDM12			
AD1	RSVD_VSS<1>	RSVD_NC<35>	N2	SPI_NIC_I350_EE_SCK	OUT	224<	
H21	RSVD_VSS<0>	RSVD_NC<34>	N3	SPI_NIC_I350_EE_CS_N	OUT	224<	
		RSVD_NC<33>	N4	NC_I350_RSVDN4			
		RSVD_NC<32>	N13	NC_I350_RSVDN13			
		RSVD_NC<31>	N21	NC_I350_RSVDN21			
		RSVD_NC<30>	N22	NC_I350_RSVDN22			
		RSVD_NC<29>	M22	NC_I350_RSVDM22			
		RSVD_NC<28>	M4	NC_I350_RSVDM4			
		RSVD_NC<27>	P4	NC_I350_RSVDP4			
		RSVD_NC<26>	P21	NC_I350_RSVDP21			
		RSVD_NC<25>	P22	NC_I350_RSVDP22			
		RSVD_NC<24>	M3	NC_I350_RSVDM3			
		RSVD_NC<23>	R1	SPI_NIC_I350_EE_DI	OUT	224<	
		RSVD_NC<22>	N1	NC_I350_RSVDN1			
		RSVD_NC<21>	P1	NC_I350_RSVDP1			
		RSVD_NC<20>	R23	NC_I350_RSVDR23			
		RSVD_NC<19>	R21	NC_I350_RSVDR21			
		RSVD_NC<18>	R22	NC_I350_RSVDR22			
		RSVD_NC<17>	T1	SPI_NIC_I350_EE_DO	IN	224>	
		RSVD_NC<16>	V24	NIC_I350_DEV_OFF_LVC3_N	IN	224>	
		RSVD_NC<15>	Y20	NC_I350_RSVDY20			
		RSVD_NC<14>	R24	NC_I350_RSVDR24			
RSVD_VCC2P5		RSVD_NC<13>	U4	NC_I350_RSVDU4			
		RSVD_NC<12>	U1	NC_I350_RSVDU1			
		RSVD_NC<11>	U2	NC_I350_RSVDU2			
		RSVD_NC<10>	U3	NC_I350_RSVDU3			
		RSVD_NC<9>	Y5	NC_I350_RSVDY5			
		RSVD_NC<8>	U23	NIC_I350_LAN2_DIS_LVC3_N	IN	224>	
		RSVD_NC<7>	U24	NIC_I350_LAN3_DIS_LVC3_N	IN	224>	
		RSVD_NC<6>	V3	NC_I350_RSVDTP8			
		RSVD_NC<5>	V4	NC_I350_RSVDV4			
		RSVD_NC<4>	AA18	NC_I350_RSVDAA18			
		RSVD_NC<3>	AA6	NC_I350_RSVDAA6			
		RSVD_NC<2>	AA10	NC_I350_RSVDAA10			
		RSVD_NC<1>	AA14	NC_I350_RSVDAA14			
		RSVD_NC<0>	AA16	NC_I350_RSVDAA16			

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E87345-001

ROOM=NIC

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TWINVILLE (3 OF 7)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 220 OF 303

INTEL CONFIDENTIAL

P0V85_TVL_P1V0_BHPC_AUX

P0V65_TVL_P1V0_BHPC_AUX

U3B1
IC

TWINVILLE_EXT_B

G13	VCC0P8<42>	VCC0P65<40>	G7
G15	VCC0P8<41>	VCC0P65<39>	G9
G17	VCC0P8<40>	VCC0P65<38>	G5
G19	VCC0P8<39>	VCC0P65<37>	H8
H14	VCC0P8<38>	VCC0P65<36>	H10
H16	VCC0P8<37>	VCC0P65<35>	J7
H18	VCC0P8<36>	VCC0P65<34>	J9
H20	VCC0P8<35>	VCC0P65<33>	J11
J15	VCC0P8<34>	VCC0P65<32>	K6
J17	VCC0P8<33>	VCC0P65<31>	K8
J19	VCC0P8<32>	VCC0P65<30>	K10
K14	VCC0P8<31>	VCC0P65<29>	K12
K16	VCC0P8<30>	VCC0P65<28>	H12
K18	VCC0P8<29>	VCC0P65<27>	L7
K20	VCC0P8<28>	VCC0P65<26>	L9
L13	VCC0P8<27>	VCC0P65<25>	L11
L15	VCC0P8<26>	VCC0P65<24>	H6
L17	VCC0P8<25>	VCC0P65<23>	M8
L19	VCC0P8<24>	VCC0P65<22>	M10
M14	VCC0P8<23>	VCC0P65<21>	J5
M16	VCC0P8<22>	VCC0P65<20>	N7
M18	VCC0P8<21>	VCC0P65<19>	N9
N15	VCC0P8<20>	VCC0P65<18>	N11
N17	VCC0P8<19>	VCC0P65<17>	P10
J13	VCC0P8<18>	VCC0P65<16>	P8
P14	VCC0P8<17>	VCC0P65<15>	P12
P16	VCC0P8<16>	VCC0P65<14>	R7
P18	VCC0P8<15>	VCC0P65<13>	R9
R13	VCC0P8<14>	VCC0P65<12>	R11
R15	VCC0P8<13>	VCC0P65<11>	T8
R17	VCC0P8<12>	VCC0P65<10>	T10
T14	VCC0P8<11>	VCC0P65<9>	T12
T16	VCC0P8<10>	VCC0P65<8>	U7
T18	VCC0P8<9>	VCC0P65<7>	U9
U13	VCC0P8<8>	VCC0P65<6>	U11
U15	VCC0P8<7>	VCC0P65<5>	V8
U17	VCC0P8<6>	VCC0P65<4>	V10
V14	VCC0P8<5>	VCC0P65<3>	V12
V16	VCC0P8<4>	VCC0P65<2>	W7
V18	VCC0P8<3>	VCC0P65<1>	W9
W13	VCC0P8<2>	VCC0P65<0>	W11
W15	VCC0P8<1>		
W17	VCC0P8<0>		

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P0V85_TVL_P1V0_BHPC_AUX

ROOM=P0V85_TVL

C2B20 22UF 6.3V 20% X5R 644066-041 0805LF	C8M53 22UF 6.3V 20% X5R 644066-041 0805LF	C3B2 22UF 6.3V 20% X5R 644066-041 0805LF	C3B3 22UF 6.3V 20% X5R 644066-041 0805LF	C3B4 22UF 6.3V 20% X5R 644066-041 0805LF	C8M52 22UF 6.3V 20% X5R 644066-041 0805LF	C2B25 22UF 6.3V 20% X5R 644066-041 0805LF	C7M15 1.0UF 6.3V 10% X5R A36096-027 0402LF	C7M36 1.0UF 6.3V 10% X5R A36096-027 0402LF
C7M35 1.0UF 6.3V 10% X5R A36096-027 0402LF	C7M38 1.0UF 6.3V 10% X5R A36096-027 0402LF	C7M4 1.0UF 6.3V 10% X5R A36096-027 0402LF	C2B24 1.0UF 6.3V 10% X5R A36096-027 0402LF	C7M8 1.0UF 6.3V 10% X5R A36096-027 0402LF	C3B5 1.0UF 6.3V 10% X5R A36096-027 0402LF	C7M12 1.0UF 6.3V 10% X5R A36096-027 0402LF	C7M16 1.0UF 6.3V 10% X5R A36096-027 0402LF	C7M40 1.0UF 6.3V 10% X5R A36096-027 0402LF
C7M42 1.0UF 6.3V 10% X5R A36096-027 0402LF	C7M43 1.0UF 6.3V 10% X5R A36096-027 0402LF	C7M37 1.0UF 6.3V 10% X5R A36096-027 0402LF	C7M34 1.0UF 6.3V 10% X5R A36096-027 0402LF	C7M39 1.0UF 6.3V 10% X5R A36096-027 0402LF	C7M6 1.0UF 6.3V 10% X5R A36096-027 0402LF	C7M14 1.0UF 6.3V 10% X5R A36096-027 0402LF	C7M17 1.0UF 6.3V 10% X5R A36096-027 0402LF	C7M11 1.0UF 6.3V 10% X5R A36096-027 0402LF

P0V65_TVL_P1V0_BHPC_AUX

ROOM=P0V65_TVL

C2B17 22UF 6.3V 20% X5R 644066-041 0805LF	C2B18 22UF 6.3V 20% X5R 644066-041 0805LF	C2B19 22UF 6.3V 20% X5R 644066-041 0805LF	C2B11 22UF 6.3V 20% X5R 644066-041 0805LF	C2B12 22UF 6.3V 20% X5R 644066-041 0805LF	C2B13 22UF 6.3V 20% X5R 644066-041 0805LF	C2B15 22UF 6.3V 20% X5R 644066-041 0805LF	C8M26 1.0UF 6.3V 10% X5R A36096-027 0402LF	C2B21 1.0UF 6.3V 10% X5R A36096-027 0402LF
C7M26 1.0UF 6.3V 10% X5R A36096-027 0402LF	C8M49 1.0UF 6.3V 10% X5R A36096-027 0402LF	C7M23 1.0UF 6.3V 10% X5R A36096-027 0402LF	C8M36 1.0UF 6.3V 10% X5R A36096-027 0402LF	C7M21 1.0UF 6.3V 10% X5R A36096-027 0402LF	C7M22 1.0UF 6.3V 10% X5R A36096-027 0402LF	C8M51 1.0UF 6.3V 10% X5R A36096-027 0402LF	C8M25 1.0UF 6.3V 10% X5R A36096-027 0402LF	C2B22 1.0UF 6.3V 10% X5R A36096-027 0402LF
C8M47 1.0UF 6.3V 10% X5R A36096-027 0402LF	C8M50 1.0UF 6.3V 10% X5R A36096-027 0402LF	C8M48 1.0UF 6.3V 10% X5R A36096-027 0402LF	C8M39 1.0UF 6.3V 10% X5R A36096-027 0402LF	C8M42 1.0UF 6.3V 10% X5R A36096-027 0402LF	C8M44 1.0UF 6.3V 10% X5R A36096-027 0402LF	C8M27 1.0UF 6.3V 10% X5R A36096-027 0402LF	C8M24 1.0UF 6.3V 10% X5R A36096-027 0402LF	C2B23 1.0UF 6.3V 10% X5R A36096-027 0402LF

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ROOM=NIC

TWINVILLE (4 OF 7)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 221 OF 303

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P1V2_TVL_P1V8_BHPC_AUX

U3B1
IC

TWINVILLE_EXT_B

	D4	VCC1P2<23>	VCC2P5<44>	AB5	
	D6	VCC1P2<22>	VCC2P5<43>	AB8	
	D8	VCC1P2<21>	VCC2P5<42>	A2	
	D10	VCC1P2<20>	VCC2P5<41>	A4	
	D16	VCC1P2<19>	VCC2P5<40>	A6	
	D18	VCC1P2<18>	VCC2P5<39>	A8	
	D20	VCC1P2<17>	VCC2P5<38>	A10	
222> IN NIC_P1V2_AUX_TVL_E3	E3	VCC1P2<16>	VCC2P5<37>	A12	
	E5	VCC1P2<15>	VCC2P5<36>	A13	
	E7	VCC1P2<14>	VCC2P5<35>	A15	
	E9	VCC1P2<13>	VCC2P5<34>	A17	
	E11	VCC1P2<12>	VCC2P5<33>	A19	
	E13	VCC1P2<11>	VCC2P5<32>	A21	
	E15	VCC1P2<10>	VCC2P5<31>	A23	
	E17	VCC1P2<9>	VCC2P5<30>	C2	
	E19	VCC1P2<8>	VCC2P5<29>	C4	
222> IN NIC_P1V2_AUX_TVL_E21	E21	VCC1P2<7>	VCC2P5<28>	C6	
	Y6	VCC1P2<6>	VCC2P5<27>	C8	
	Y8	VCC1P2<5>	VCC2P5<26>	C10	
	Y10	VCC1P2<4>	VCC2P5<25>	C15	
	Y12	VCC1P2<3>	VCC2P5<24>	C17	
	Y14	VCC1P2<2>	VCC2P5<23>	C19	
	Y16	VCC1P2<1>	VCC2P5<22>	C21	
	Y18	VCC1P2<0>	VCC2P5<21>	C23	
			VCC2P5<20>	C24	NIC_P2V6_AUX_TVL_C24 IN 222>
P3V3_STBY	N5	VCC3P3<2>	VCC2P5<19>	P6	
	M6	VCC3P3<1>	VCC2P5<18>	P20	
	L5	VCC3P3<0>	VCC2P5<17>	R5	
			VCC2P5<16>	R19	
			VCC2P5<15>	T6	
			VCC2P5<14>	T20	
			VCC2P5<13>	U5	
			VCC2P5<12>	U19	
			VCC2P5<11>	V6	
			VCC2P5<10>	W5	
			VCC2P5<9>	W19	
			VCC2P5<8>	M20	
			VCC2P5<7>	N19	
			VCC2P5<6>	V20	
			VCC2P5<5>	AB11	
			VCC2P5<4>	AB14	
			VCC2P5<3>	AB17	
			VCC2P5<2>	AB20	
			VCC2P5<1>	AB22	
			VCC2P5<0>	AB3	

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E87345-001

P3V3_STBY

ROOM=P3V3_AUX_TVL

C8M30 1.0UF 6.3V 10% X5R A36096-027 0402LF
C8M29 1.0UF 6.3V 10% X5R A36096-027 0402LF
C8M28 1.0UF 6.3V 10% X5R A36096-027 0402LF
C2B7 22UF 6.3V 20% X5R 644066-041 0805LF

P2V6_TVL_P3V3_BHPC_AUX

ROOM=P2V6_TVL

C3A10 1.0UF 6.3V 10% X5R A36096-027 0402LF
C7L15 1.0UF 6.3V 10% X5R A36096-027 0402LF
C3A11 1.0UF 6.3V 10% X5R A36096-027 0402LF

P2V6_TVL_P3V3_BHPC_AUX

C7M30 22UF 6.3V 20% X5R 644066-041 0805LF
C3A19 22UF 6.3V 20% X5R 644066-041 0805LF
C3A6 22UF 6.3V 20% X5R 644066-041 0805LF
C3A5 22UF 6.3V 20% X5R 644066-041 0805LF
C3A4 22UF 6.3V 20% X5R 644066-041 0805LF
C3A13 22UF 6.3V 20% X5R 644066-041 0805LF
C3A7 22UF 6.3V 20% X5R 644066-041 0805LF
C8M7 1.0UF 6.3V 10% X5R A36096-027 0402LF

ROOM=P2V6_TVL

C7L19 1.0UF 6.3V 10% X5R A36096-027 0402LF
C7M13 1.0UF 6.3V 10% X5R A36096-027 0402LF
C8L78 1.0UF 6.3V 10% X5R A36096-027 0402LF
C7L10 1.0UF 6.3V 10% X5R A36096-027 0402LF
C7L20 1.0UF 6.3V 10% X5R A36096-027 0402LF
C7L12 1.0UF 6.3V 10% X5R A36096-027 0402LF
C7L14 1.0UF 6.3V 10% X5R A36096-027 0402LF
C7L18 1.0UF 6.3V 10% X5R A36096-027 0402LF

C8L73 1.0UF 6.3V 10% X5R A36096-027 0402LF
C7M32 1.0UF 6.3V 10% X5R A36096-027 0402LF
C7L9 1.0UF 6.3V 10% X5R A36096-027 0402LF
C7L17 1.0UF 6.3V 10% X5R A36096-027 0402LF
C7M31 1.0UF 6.3V 10% X5R A36096-027 0402LF
C7L13 1.0UF 6.3V 10% X5R A36096-027 0402LF
C7L11 1.0UF 6.3V 10% X5R A36096-027 0402LF
C8L77 1.0UF 6.3V 10% X5R A36096-027 0402LF

P1V2_TVL_P1V8_BHPC_AUX

C8L63 22UF 6.3V 20% X5R 644066-041 0805LF
C2A8 22UF 6.3V 20% X5R 644066-041 0805LF
C2A7 22UF 6.3V 20% X5R 644066-041 0805LF
C2A12 22UF 6.3V 20% X5R 644066-041 0805LF
C7M27 1.0UF 6.3V 10% X5R A36096-027 0402LF
C8L72 1.0UF 6.3V 10% X5R A36096-027 0402LF
C2A13 1.0UF 6.3V 10% X5R A36096-027 0402LF

ROOM=P1V2_TVL

C8L62 1.0UF 6.3V 10% X5R A36096-027 0402LF
C8L57 1.0UF 6.3V 10% X5R A36096-027 0402LF
C8L60 1.0UF 6.3V 10% X5R A36096-027 0402LF
C7M1 1.0UF 6.3V 10% X5R A36096-027 0402LF
C8L58 1.0UF 6.3V 10% X5R A36096-027 0402LF
C8L69 1.0UF 6.3V 10% X5R A36096-027 0402LF
C8L66 1.0UF 6.3V 10% X5R A36096-027 0402LF

ROOM=NIC

P1V2_TVL_P1V8_BHPC_AUX

656554-026
FB2
1 2
100 FB SMLF

NIC_P1V2_AUX_TVL_E3 OUT 222<

C2A16 1.0UF 6.3V 10% X5R A36096-027 0402LF
C2A17 1.0UF 6.3V 10% X5R A36096-027 0402LF

656554-026
FB3
1 2
100 FB SMLF

NIC_P1V2_AUX_TVL_E21 OUT 222<

C3A17 1.0UF 6.3V 10% X5R A36096-027 0402LF
C3A18 1.0UF 6.3V 10% X5R A36096-027 0402LF

FOR TVL USE FERRITE
100 0805LF
IPN: 656554-026

FOR I350 REPLACE
FERRITE WITH RES:
0 OHM 5% 0805LF
IPN: A93552-002

P2V6_TVL_P3V3_BHPC_AUX

P2V6_TVL
656554-026
FB1
1 2
100 FB SMLF

NIC_P2V6_AUX_TVL_C24 OUT 222<

C3A9 1.0UF 6.3V 10% X5R A36096-027 0402LF
C7L16 1.0UF 6.3V 10% X5R A36096-027 0402LF

FOR TVL USE FERRITE
100 0805LF
IPN: 656554-026

FOR I350 REPLACE
FERRITE WITH RES:
0 OHM 5% 0805LF
IPN: A93552-002

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TWINVILLE (5 OF 7)

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		SCALE:	DO NOT SCALE DRAWING		SHEET 222 OF 303

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U3B1
IC

TWINVILLE_EXT_B

AA12	VSS<224>	VSS<168>	F16
B1	VSS<223>	VSS<167>	F17
B2	VSS<222>	VSS<166>	F18
B4	VSS<221>	VSS<165>	F19
B6	VSS<220>	VSS<164>	F20
B8	VSS<219>	VSS<163>	G6
B10	VSS<218>	VSS<162>	G8
B12	VSS<217>	VSS<161>	G10
D7	VSS<216>	VSS<160>	G12
D3	VSS<215>	VSS<159>	G14
B13	VSS<214>	VSS<158>	G16
B15	VSS<213>	VSS<157>	G18
B17	VSS<212>	VSS<156>	G20
B19	VSS<211>	VSS<155>	H5
B21	VSS<210>	VSS<154>	H7
B23	VSS<209>	VSS<153>	H9
B24	VSS<208>	VSS<152>	H11
C3	VSS<207>	VSS<151>	H13
C5	VSS<206>	VSS<150>	H15
C7	VSS<205>	VSS<149>	H17
C9	VSS<204>	VSS<148>	H19
C14	VSS<203>	VSS<147>	J6
C16	VSS<202>	VSS<146>	J8
C18	VSS<201>	VSS<145>	J10
C20	VSS<200>	VSS<144>	J12
C22	VSS<199>	VSS<143>	J14
D5	VSS<198>	VSS<142>	J16
D19	VSS<197>	VSS<141>	J18
E20	VSS<196>	VSS<140>	J20
D21	VSS<195>	VSS<139>	K11
D22	VSS<194>	VSS<138>	K13
E22	VSS<193>	VSS<137>	K15
F22	VSS<192>	VSS<136>	K17
E4	VSS<191>	VSS<135>	K19
E6	VSS<190>	VSS<134>	K5
E8	VSS<189>	VSS<133>	K7
D9	VSS<188>	VSS<132>	K9
E10	VSS<187>	VSS<131>	L6
E12	VSS<186>	VSS<130>	L8
E14	VSS<185>	VSS<129>	L10
D15	VSS<184>	VSS<128>	L12
E16	VSS<183>	VSS<127>	L14
D17	VSS<182>	VSS<126>	L16
E18	VSS<181>	VSS<125>	L18
F21	VSS<180>	VSS<124>	L20
F5	VSS<179>	VSS<123>	M5
F6	VSS<178>	VSS<122>	M7
F7	VSS<177>	VSS<121>	M9
F8	VSS<176>	VSS<120>	M11
F9	VSS<175>	VSS<119>	M13
F10	VSS<174>	VSS<118>	M15
F11	VSS<173>	VSS<117>	M17
F12	VSS<172>	VSS<116>	M19
F13	VSS<171>	VSS<115>	N6
F14	VSS<170>	VSS<114>	N8
F15	VSS<169>	VSS<113>	N10
		VSS<112>	N12

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U3B1
IC

TWINVILLE_EXT_B

N14	VSS<111>	VSS<55>	Y11
N16	VSS<110>	VSS<54>	Y13
N18	VSS<109>	VSS<53>	Y15
N20	VSS<108>	VSS<52>	Y17
P5	VSS<107>	VSS<51>	Y19
P7	VSS<106>	VSS<50>	Y23
P9	VSS<105>	VSS<49>	Y24
P11	VSS<104>	VSS<48>	Y3
P13	VSS<103>	VSS<47>	AA1
P15	VSS<102>	VSS<46>	AA2
P17	VSS<101>	VSS<45>	AA3
P19	VSS<100>	VSS<44>	AA4
R6	VSS<99>	VSS<43>	AA5
R8	VSS<98>	VSS<42>	AA7
R10	VSS<97>	VSS<41>	AA9
R12	VSS<96>	VSS<40>	AA11
R14	VSS<95>	VSS<39>	AA13
R16	VSS<94>	VSS<38>	AA15
R18	VSS<93>	VSS<37>	AA17
R20	VSS<92>	VSS<36>	AA19
T5	VSS<91>	VSS<35>	AA20
T7	VSS<90>	VSS<34>	AA21
T9	VSS<89>	VSS<33>	AA22
T11	VSS<88>	VSS<32>	AA23
T13	VSS<87>	VSS<31>	AB9
T15	VSS<86>	VSS<30>	AB4
T17	VSS<85>	VSS<29>	D2
T19	VSS<84>	VSS<28>	AB6
F23	VSS<83>	VSS<27>	E2
U6	VSS<82>	VSS<26>	AB10
U8	VSS<81>	VSS<25>	AB12
U10	VSS<80>	VSS<24>	AB13
U12	VSS<79>	VSS<23>	AB16
U14	VSS<78>	VSS<22>	AB18
U16	VSS<77>	VSS<21>	AB19
U18	VSS<76>	VSS<20>	AB15
U20	VSS<75>	VSS<19>	AB21
V5	VSS<74>	VSS<18>	AB7
V7	VSS<73>	VSS<17>	AC1
V9	VSS<72>	VSS<16>	AC2
V11	VSS<71>	VSS<15>	AC5
V13	VSS<70>	VSS<14>	AC8
V15	VSS<69>	VSS<13>	AC11
V17	VSS<68>	VSS<12>	AC14
V19	VSS<67>	VSS<11>	AC17
W20	VSS<66>	VSS<10>	AC20
W10	VSS<65>	VSS<9>	AC23
W12	VSS<64>	VSS<8>	AC24
W14	VSS<63>	VSS<7>	AD2
W16	VSS<62>	VSS<6>	AD5
W18	VSS<61>	VSS<5>	AD8
W3	VSS<60>	VSS<4>	AD11
W6	VSS<59>	VSS<3>	AD14
W8	VSS<58>	VSS<2>	AD17
Y7	VSS<57>	VSS<1>	AD20
Y9	VSS<56>	VSS<0>	AD23

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ROOM=NIC

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TWINVILLE (6 OF 7)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 223 OF 303	

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P3V3_STBY

R8M16 10.0K 1% 1/16W CHIP A93548-034 0402LF
R2B13 10.0K 1% 1/16W CHIP A93548-034 0402LF
R8M11 10.0K 1% 1/16W CHIP A93548-034 0402LF
R2B16 10.0K 1% 1/16W CHIP A93548-034 0402LF

RMII_NIC_IBMC_RXD<0> OUT 176< 219>
RMII_NIC_IBMC_RXD<1> OUT 176< 219>
RMII_IBMC_NIC_R_TXD<1> OUT 176> 219<
RMII_IBMC_NIC_R_TXD<0> OUT 176> 219<
RMII_IBMC_NIC_TX_R_EN OUT 176> 219<
RMII_NIC_IBMC_CRS_DV OUT 176< 219>
CLK_50M_TWN OUT 32> 219<

R2B17 100 1% 1/16W CHIP A93548-043 0402LF
R8M14 100 1% 1/16W CHIP A93548-043 0402LF
R2B11 10.0K 1% 1/16W CHIP A93548-034 0402LF

P3V3_STBY

R7M10 10.0K 1% 1/16W EMPTY A93548-034 0402LF
TVL - NOT POPULATE
I350 - POPULATE

NIC_I350_DEV_OFF_LVC3_N OUT 220<
NIC_I350_LAN2_DIS_LVC3_N OUT 220<
NIC_I350_LAN3_DIS_LVC3_N OUT 220<

R7M9 10.0K 1% 1/16W EMPTY A93548-034 0402LF
R7M8 10.0K 1% 1/16W EMPTY A93548-034 0402LF

TWINVILLE FLASH

P2V6_TVL_P3V3_BHPC_AUX

CHIP R8M5 3.3K 5%
R8L74 3.3K 5% CHIP
R8M1 3.3K 5% CHIP
C8L82 0.1UF 16V 10% X7R 602433-056 0603LF

U2A5
IC
W25Q16
E87440-001

SPI_NIC_EE_CE_N IN 219>
SPI_NIC_EE_SI IN 219>
SPI_NIC_EE_CLK IN 219>
SPI_NIC_EE_WP_N
SPI_NIC_EE_HOLD_N

VCC
CS_N
WP_N IO2
DI_IO0
CLK
HOLD_N_IO3
DO_IO1
GND

SPI_NIC_EE_SO
R8M3 0 5% CHIP 1/16W 0402LF A93549-001
SPI_NIC_EE_R_SO OUT 219<

I350 EEPROM

P3V3_STBY

R8M17 3.3K 5% 1/16W EMPTY A93549-019 0402LF
R8M15 3.3K 5% EMPTY
R8M20 3.3K 5% EMPTY
R8M12 3.3K 5% EMPTY
C8M19 0.1UF 16V 10% EMPTY 602433-056 0603LF

U2B1
AT25256 EMPTY

SPI_NIC_I350_EE_CS_N IN 220>
SPI_NIC_I350_EE_DI IN 220>
SPI_NIC_I350_EE_SCK IN 220>
NIC_I350_EE_WP_N
NIC_I350_EE_HOLD_N

CS_N
WP_N
SI
SCK
HOLD_N
SO

SPI_NIC_I350_EE_DO OUT 220<

C98131-001
VCC=P3V3_STBY
GND=GND

P3V3_STBY

R3B2 10.0K 1% 1/16W CHIP A93548-034 0402LF

EU7M1
IC
74LVC07A
D90453-001
VCC=P3V3_STBY; GND=GND; TH=GND;

FM_SSB_LAN1_DISABLE_N IN 136>
NIC_LAN1_DIS_N OUT 219> 219<

R7L21 0 5% 1/16W CHIP A93549-001 0402LF

EU7M1
IC
74LVC07A
D90453-001
VCC=P3V3_STBY; GND=GND; TH=GND;

FM_BMC_LAN1_DISABLE_N IN 176>
R7M6 0 5% CHIP 1/16W 0402LF A93549-001
FM_BMC_LAN1_DISABLE_R_N

ROOM=NIC

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		SCALE:	DO NOT SCALE DRAWING	SHEET 224 OF 303	

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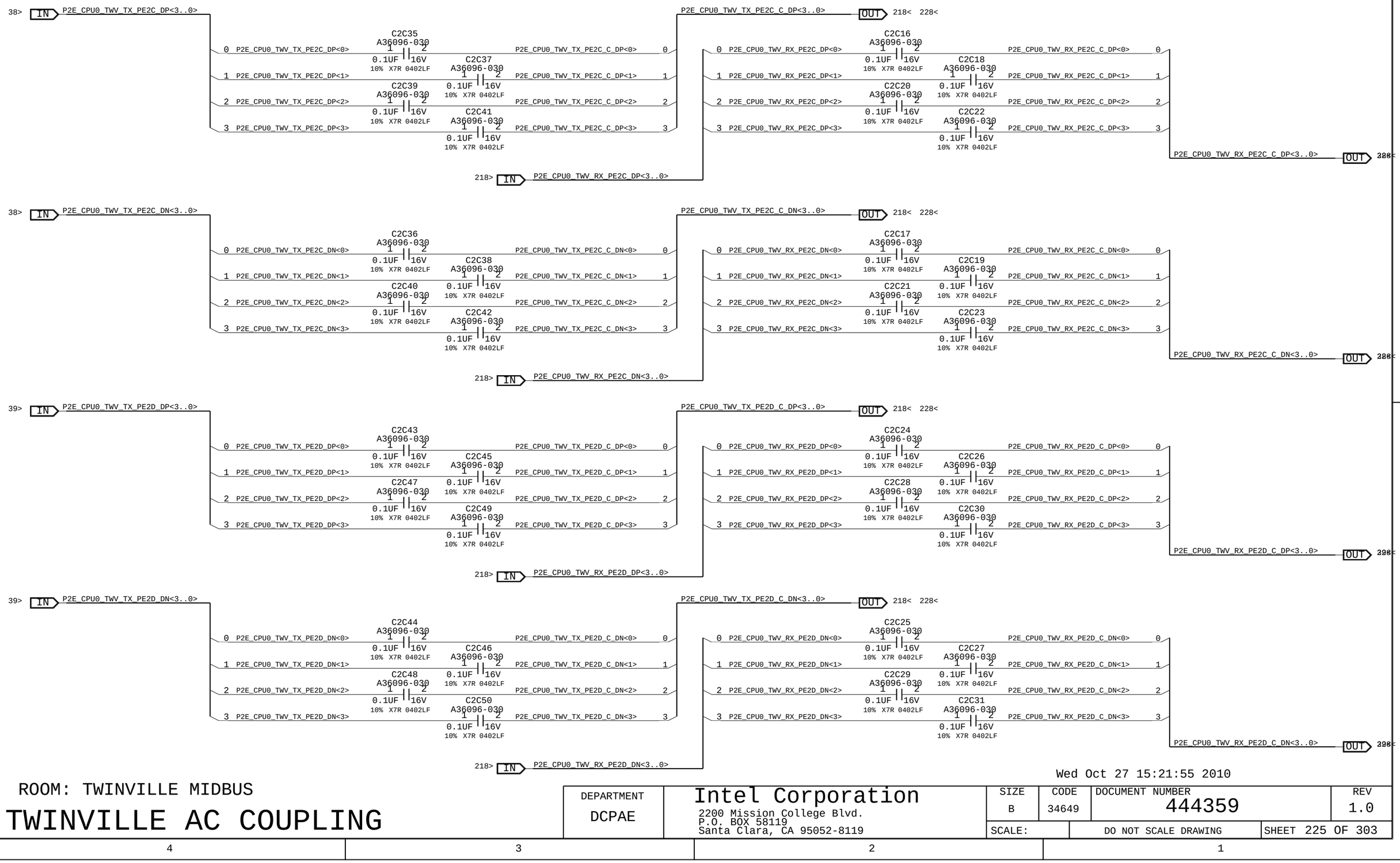

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ROOM: TWINVILLE MIDBUS

TWINVILLE AC COUPLING

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 225 OF 303	

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P2V6_TVL_P3V3_BHPC_AUX

CAD NOTE:
PLACE THESE COMPONENTS TOGETHER AND NEAR THE MAGNETICS

C4A1 4.7UF 10% 16V 0805LF EMPTY 644066-100

CHIP R4A1 0 1% 1/2W C44950-002 1206LF

NOTE:
TVL:
PLACE RESISTOR R4A1
REMOVE CAP C4A1

I350:
REMOVE RESISTOR R4A1
PLACE CAP C4A1

U4A1
IC

XFMR_D82329007

P2V55_AUX_NIC_A_R_TWINVILLE

218<>	BI	NIC_A_MDI_DP<0>	1	TRDCT1	TRPCT1	30	NIC_A_MCT1
218<>	BI	NIC_A_MDI_DN<0>	2	TRD1P	TRP1P	29	
			3	TRD1N	TRP1N	28	
218<>	BI	NIC_A_MDI_DP<1>	4	TRDCT2	TRPCT2	27	NIC_A_MCT2
218<>	BI	NIC_A_MDI_DN<1>	5	TRD2P	TRP2P	26	
			6	TRD2N	TRP2N	25	
218<>	BI	NIC_A_MDI_DP<2>	7	TRDCT3	TRPCT3	24	NIC_A_MCT3
218<>	BI	NIC_A_MDI_DN<2>	8	TRD3P	TRP3P	23	
			9	TRD3N	TRP3N	22	
218<>	BI	NIC_A_MDI_DP<3>	10	TRDCT4	TRPCT4	21	NIC_A_MCT4
218<>	BI	NIC_A_MDI_DN<3>	11	TRD4P	TRP4P	20	
			12	TRD4N	TRP4N	19	
226<>	BI	NIC_A_MDI_FIL_DP<4>	13	CMSDCT	CMSPCT	A93549-001 18	
226<>	BI	NIC_A_MDI_FIL_DN<4>	14	CMSDP	CMSPP	17	
			15	CMSDN	CMSPN	16	NIC_A_MDI_MAG_DN<4>

D82329-007

75 1.0% R6L5 1/8W 0805 A93556-030
75 1.0% R6L4
75 1.0% R6L3
300 5.0% R6L2
R6L1 0 5% 1/16W 0402LF CHIP

FOR TVL USE
300 OHM 5% 0805LF
IPN: A93555-036

FOR I350 USE
75 OHM 1% 0805LF
IPN: A93556-030

FOR TVL POPULATE
0 OHM 5% 0402LF
IPN: A93549-001

FOR I350 DEPOPULATE

C6L1 1000PF 3000V 10% X7R 662367-009 1808

GND_CHASSIS_TVL

C6L3 4.7UF 16V 10% X5R 644066-100 0805LF
C6L6 4.7UF 16V 10% X5R
C6L5 4.7UF 16V 10% X5R
C6L4 4.7UF 16V 10% X5R
C6L2 4.7UF 16V 10% X5R

JA4A1
CONN

CONN12_E79836002

AP					
AM					
BP	NIC_A_MDI_MAG_DP<0>	1			
BM	NIC_A_MDI_MAG_DN<0>	2			
CP	NIC_A_MDI_MAG_DP<1>	3	LED2P	9	NIC0_LED00_LINKUP_R_LVT2 IN 226>
CM	NIC_A_MDI_MAG_DN<1>	6	LED2N	10	NIC0_LED02_ACT_LVT2 IN 218> 226<> 230<
DP	NIC_A_MDI_MAG_DP<2>	4	LED1N_G	11	NIC0_LED01_10G_BUFF_LVT3 IN 226>
DM	NIC_A_MDI_MAG_DN<2>	5	LED1N_O	12	NIC0_LED03_1G_BUFF_LVT3 IN 226>
	NIC_A_MDI_MAG_DP<3>	7	MH1	MH1	
	NIC_A_MDI_MAG_DN<3>	8	MH2	MH2	

E79836-002

COLOR:
AMBER:1 GB
GREEN:10 GB

GND_CHASSIS_TVL

230< 218> IN NIC0_LED00_LINKUP_LVT2 — R2B22 330 1/16W 5% 0402LF CHIP A93549-012 — NIC0_LED00_LINKUP_R_LVT2 OUT 226<

230< 226< 218> IN NIC0_LED02_ACT_LVT2 OUT

C2B9 470PF 50V 10% X7R A36096-049 0402LF

C8M31 470PF 50V 10% X7R A36096-049 0402LF

THE FILTER SHOULD BE PLACED/ROUTED AS BALANCED DIFFERENTIALLY AS POSSIBLE AND SHOULD BE LOCATED CLOSE TO THE TWINVILLE PACKAGE

218<> BI NIC_A_MDI_DP<4> — L2A5 33NH IND SM A47303-108 — NIC_A_MDI_L_DP<4> — L2A3 33NH IND SM A47303-108 — NIC_A_MDI_FIL_DP<4> BI 226<>

C2A15 3.3PF 50V 0.25PF COG A36094-026 0402LF
C2A11 6.8PF 50V 5% COG A36094-050 0402
C2A9 3.3PF 50V 0.25PF COG A36094-026 0402LF

218<> BI NIC_A_MDI_DN<4> — L2A4 33NH IND SM A47303-108 — NIC_A_MDI_L_DN<4> — L2A2 33NH IND SM A47303-108 — NIC_A_MDI_FIL_DN<4> BI 226<>

FOR I350 THIS FILTER SHOULD BE REMOVED COMPLETELY

P3V3_STBY

R7M5 220 5% CHIP 1/16W A93549-011 0402LF

218> IN NIC0_LED01_10G_LVT2 — EU7M2 74LVC07A D90453-001 (5 → 6) — NIC0_LED01_10G_BUFF_LVT3 OUT 226<

VCC=P3V3_STBY; GND=GND; TH=GND;

C7M5 470PF 10% X7R 50V A36096-049 0402LF

P3V3_STBY

R3B1 220 5% CHIP 1/16W A93549-011 0402LF

218> IN NIC0_LED03_1G_LVT2 — EU7M2 74LVC07A D90453-001 (9 → 8) — NIC0_LED03_1G_BUFF_LVT3 OUT 226<

VCC=P3V3_STBY; GND=GND; TH=GND;

C7M3 470PF 10% X7R 50V A36096-049 0402LF

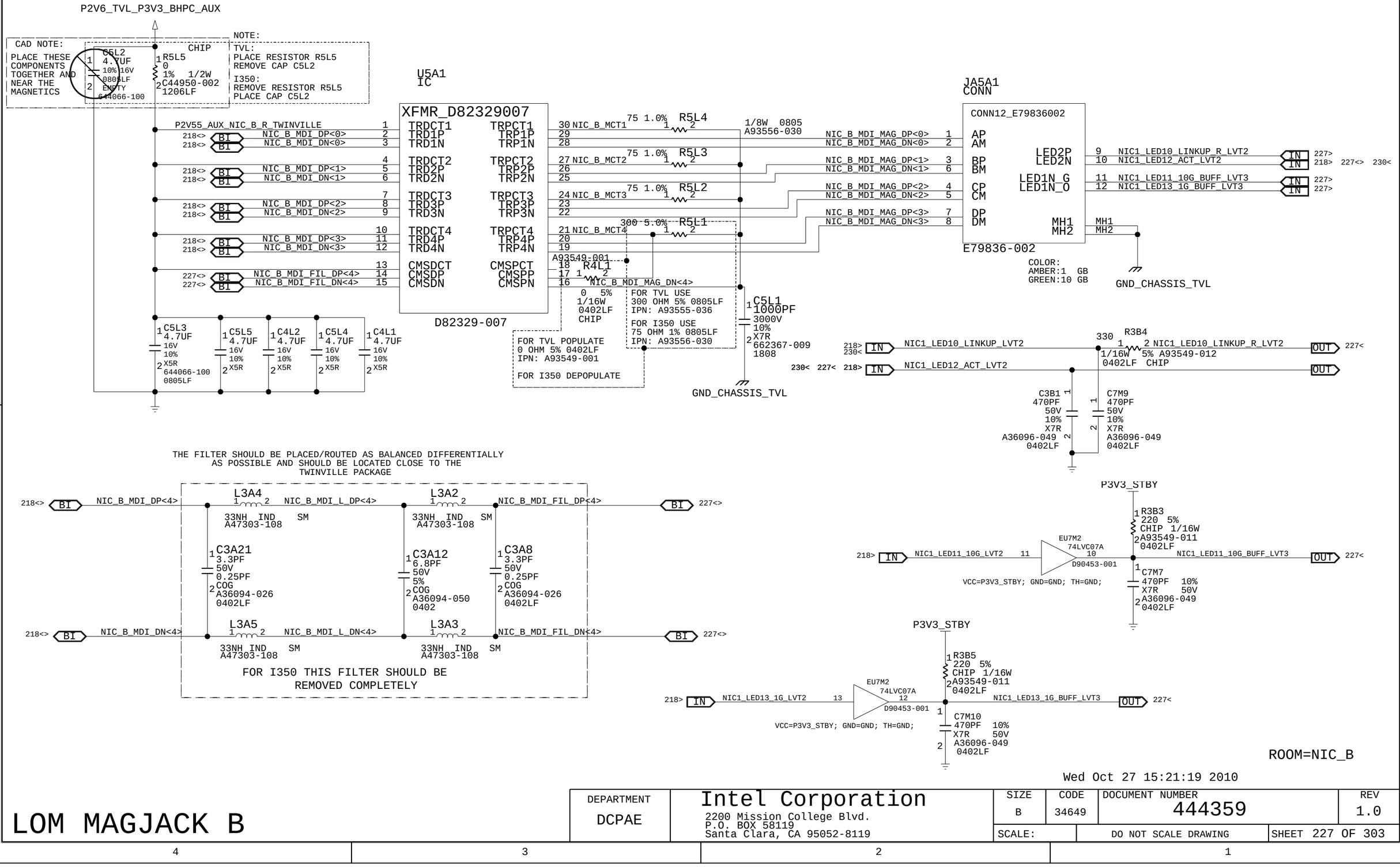
ROOM=NIC_A

Wed Oct 27 15:21:18 2010

LOM MAGJACK A

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 226 OF 303

INTEL CONFIDENTIAL



ROOM=NIC_B

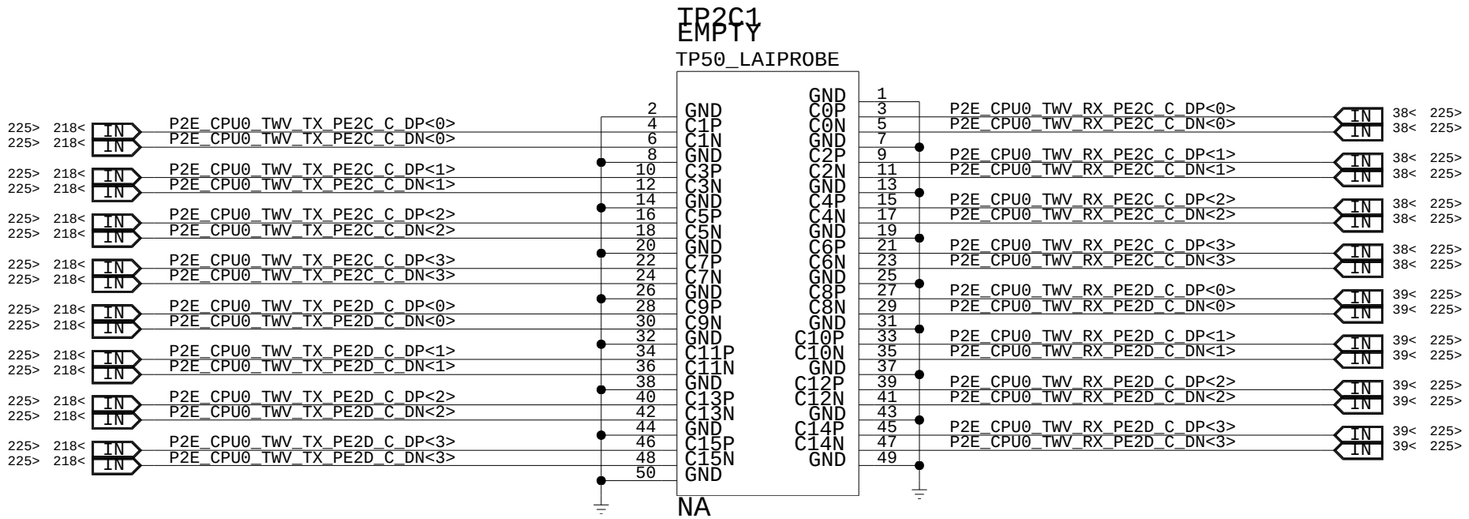
Wed Oct 27 15:21:19 2010

LOM MAGJACK B

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 227 OF 303

INTEL CONFIDENTIAL

ROOM: TWINVILLE MIDBUS



Wed Oct 27 15:21:55 2010

TWINVILLE MIDBUS

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 228 OF 303	

INTEL CONFIDENTIAL

ON-BOARD POWER & RESET BUTTONS

S1J2
1 2
D90553-001
SWITCH_D90553001

S1J1
1 2
D90553-001
SWITCH_D90553001

ON-BOARD STATUS LEDS

P3V3_STBY

DS2A7
IC
C97900-001
1
3 GREEN
2 YELLOW

192> IN FP_LED_STATUS_GREEN_BUF_CO_N
R9V14 330 5% 1/16W 0402LF A93549-012
FP_LED_STATUS_GREEN_R1_CO_N

192> IN FP_LED_STATUS_AMBER_BUF_CO_N
R9V15 330 5% 1/16W 0402LF A93549-012
FP_LED_STATUS_AMBER_R1_CO_N

U9W1
74LVC1G07
169< 134> 168> 302> IN RST_XDP_CO_N 2 4
VCC=P3V3_STBY; GND=GND;
C88419-001

P3V3_STBY

R9V17 10.0K 1% 0402LF 1/16W A93548-034
R9W6 10.0K 1% 0402LF 1/16W A93548-034
R1J43 10.0K 1% 0402LF 1/16W A93548-034

P3V3_STBY

R1J35 10.0K 1% 0402LF 1/16W A93548-034

P3V3_STBY

J1H2
CONN24_C85892002
C85892-002

1	2		
4	TP_ID_LED_ANODE		
6	TP_ID_LED_CATHODE		
5	7	8	FP_LED_STATUS_GREEN_R_CO_N
9	10	FP_LED_STATUS_AMBER_R_CO_N	
11	12	FP_NIC0_LED_LINKUP_LVT3_R	
13	14	FP_NIC0_LED_ACT_LVT3_R	
15	16		
17	18		
TP_ID_BTN	19	20	
NC_SIO_TEMP_SENSOR_LVC3	21	22	FP_NIC1_LED_LINKUP_LVT3_R
FP_NMI_BTN_R_CO_N	23	24	FP_NIC1_LED_ACT_LVT3_R

100 R9V13 1% 1/16W A93548-043 0402LF
100 R9V16 1% 1/16W A93548-043 0402LF
100 R1J27 1% 1/16W A93548-043 0402LF
100 R1H12 1% 1/16W A93548-043 0402LF
100 R1J39 1% 1/16W A93548-043 0402LF
100 R1J31 1% 1/16W A93548-043 0402LF

230> IN FP_PWR_LED_BUF_LVC3_N
R1H9 A93548-043 0402LF 100 1/16W 1%
FP_PWR_LED_BUF_LVC3_R_N

230> IN FP_LED_HDD_ACT_LVT3_N
100 R1H10 1% 0402LF 1/16W A93548-043
FP_HDD_ACT_LED_LVT3_R_N

169> 178< OUT FP_PWR_BTN_CO_N
330 0402LF 5% 1/16W A93549-012 R9W1
FP_PWR_BTN_R_CO_N

178< OUT FP_RST_BTN_CO_N
330 0402LF 5% 1/16W A93549-012 R9W9
FP_RST_BTN_R_CO_N

176< OUT FP_NMI_BTN_CO_N
330 0402LF 5% 1/16W A93549-012 R1J41
FP_NMI_BTN_R_CO_N

FP_NIC0_LED_LINKUP_LVT3 IN 230> 217<>
FP_NIC0_LED_ACT_LVT3 IN 230> 202<>
SMB_SENSOR_STBY_LVC3_DATA BI 217< 190<>
SMB_SENSOR_STBY_LVC3_CLK IN 177> 177<>
FM_CHASSIS_INTRUSION_CO OUT 230< 202<
FP_NIC1_LED_LINKUP_LVT3 IN 230>
FP_NIC1_LED_ACT_LVT3 IN 230>

C1J15
16V 10% 0.1UF
0402LF A36096-030

C9W1
0.1UF 10% 16V
0402LF A36096-030

C9W2
0.1UF 10% 16V
0402LF A36096-030

IBMC NEEDS TO ENABLE ITS INTERNAL PU RESISTORS AND DEBOUNCERS FOR THE FP BUTTONS.

RC CIRCUIT IN FPB BUTTONS ARE REQUIRED TO PREVENT OVERVOLTAGE UNDERVOLTAGE CONDITIONS WHEN THE FPB DOES NOT INCLUDE THEM.

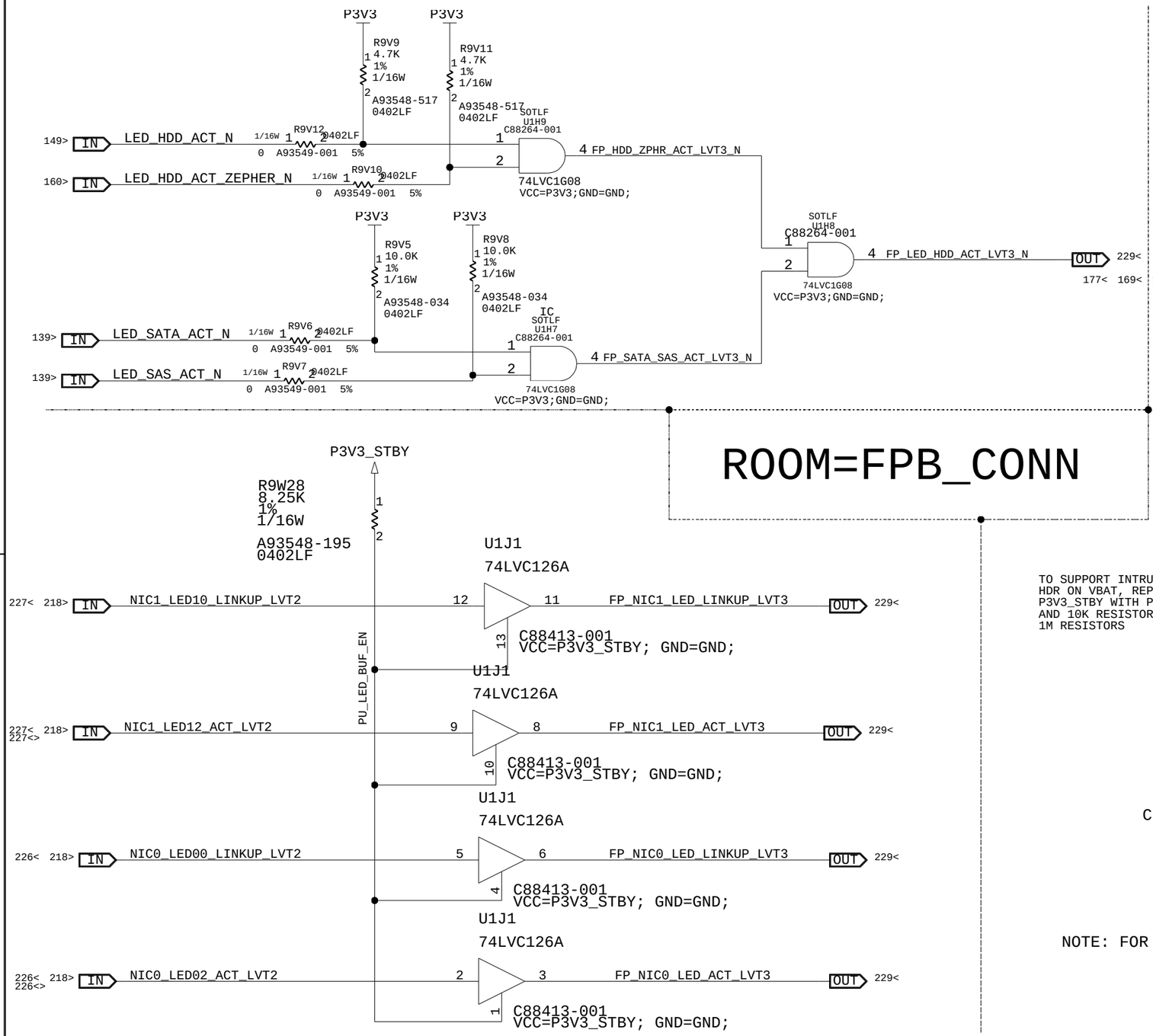
ROOM=FPB_CONN

Wed Oct 27 15:21:56 2010

FRONT PANEL SIGNALS (1 OF 2)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 229 OF 303	

INTEL CONFIDENTIAL



NOTE: FOR OPEN CHASSIS DEBUG A JUMPER MUST BE POPULATED

1-2 CLOSED	CHASSIS COVER IS CLOSED
1-2 OPEN	CHASSIS COVER IS REMOVED

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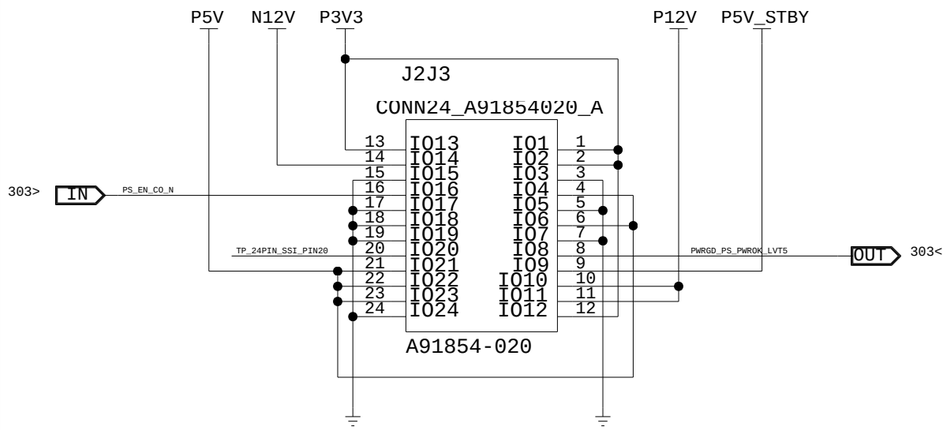
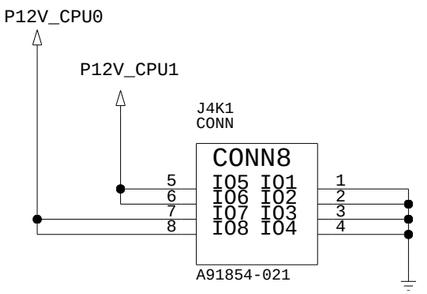
FRONT PANEL SIGNALS (2 OF 2)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 230 OF 303	

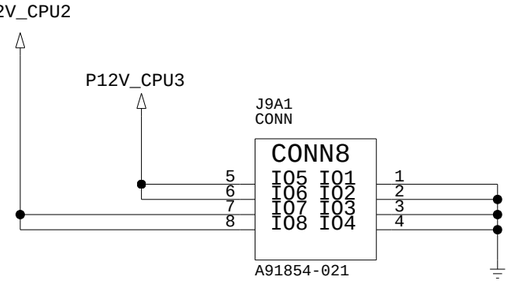
INTEL CONFIDENTIAL



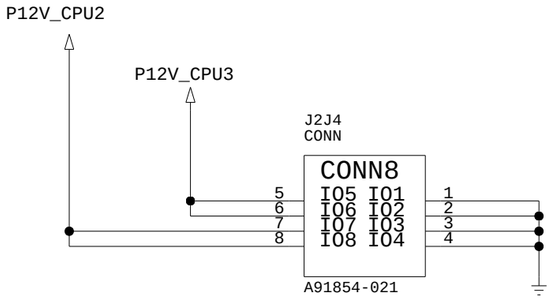
NOTE: REPLACE 2X12 WITH IPN A91854-020
ADD BULK AND DECOUPLING CAPS!!



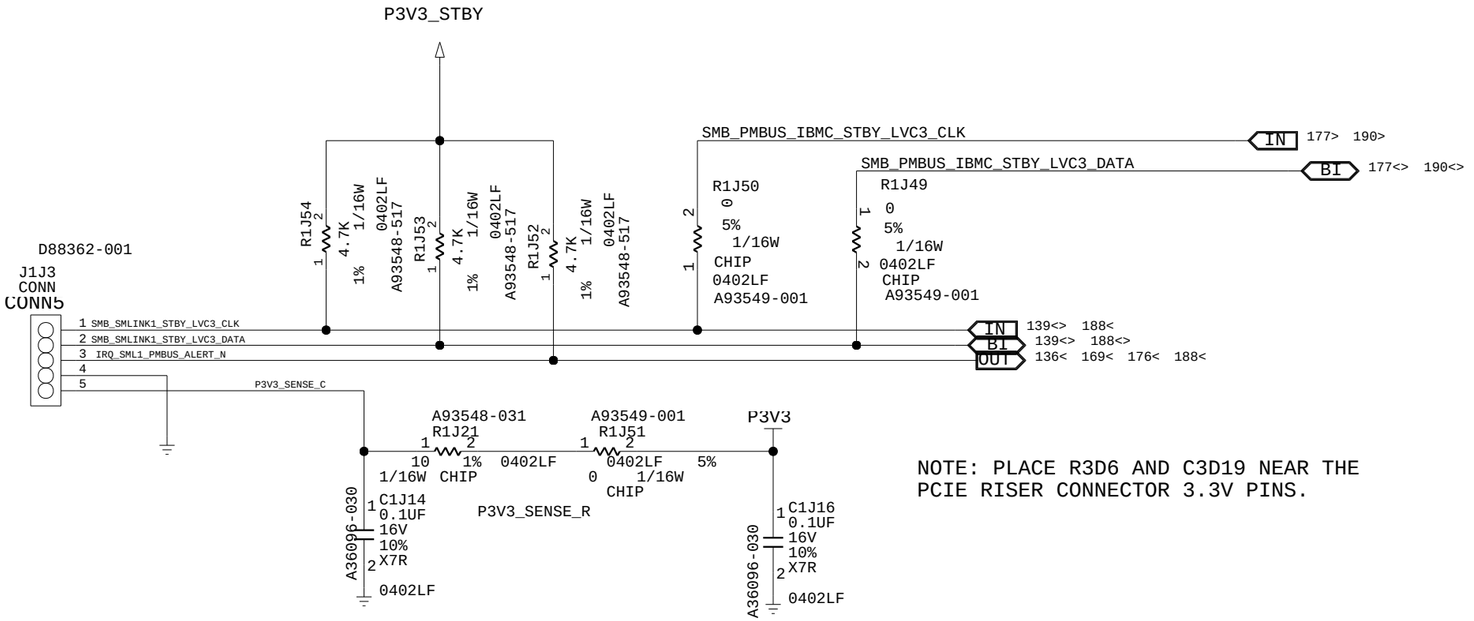
FOR BOTH 95W & 130W PROCESSORS



FOR 130W PROCESSORS (OPEN-CHASSIS)



FOR 95W PROCESSORS (CLOSED-CHASSIS)



NOTE: PLACE R3D6 AND C3D19 NEAR THE
PCIE RISER CONNECTOR 3.3V PINS.

Wed Oct 27 15:21:56 2010

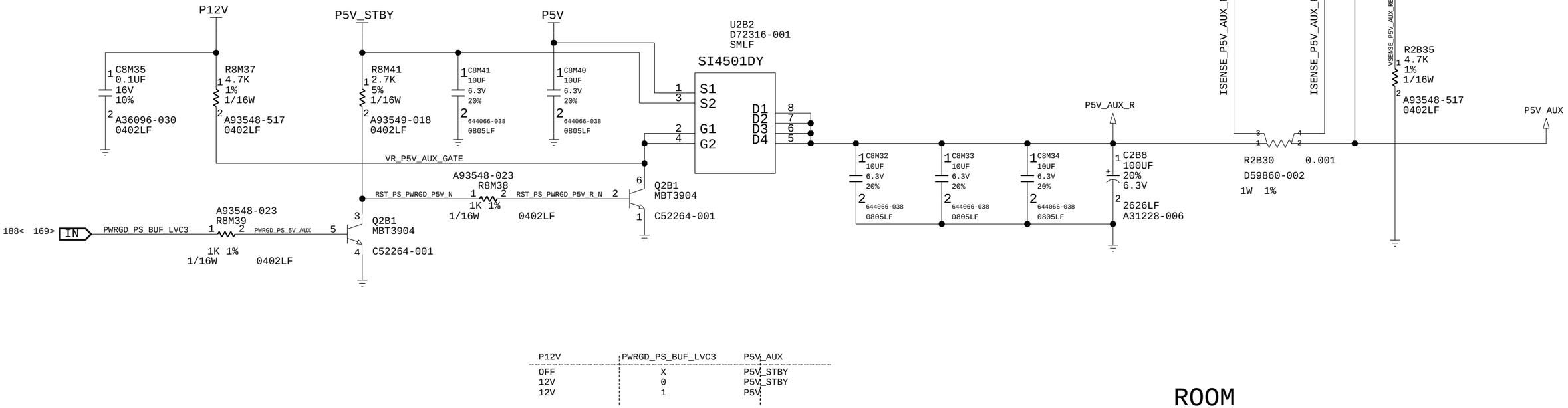
POWER CONNECTORS

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 231 OF 303	

INTEL CONFIDENTIAL

5V AUX SWITCH (3.5A)

S0,S1 3.05A / S4,S5 0.32A



SPECIFICATION

1 MV/A
DESIRED FULL SCALE CURRENT = 3.5 A
KELVIN RESISTOR MAX CURRENT=30 A

P12V	PWRGD_PS_BUF_LVC3	P5V_AUX
OFF	X	P5V_STBY
12V	0	P5V_STBY
12V	1	P5V

ROOM

P5V_AUX

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5VAUX SWITCH

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 232 OF 303	

INTEL CONFIDENTIAL

VR SPECIFICATION
VOUT=SVID, +/-15MV
LOAD LINE = 0.8MOHMS
RIPPLE = +/-10MV
IOUT = 165A PEAK
IOUT = 135A TDC
IOUT STEP = 106A
IOUT DI/DT=200A/US
FREQ=489KHZ
MINIMUM AIR FLOW=551LFM

CAD NOTE:
PLACE NEAR CONTROLLER

VBOOTA=0.9V (R=45.3K)

VBOOT=0V (R=10K)

CAD NOTE: ROUTE DIO LINE BETWEEN ALERT AND CLOCK 20 MILS SPACING. 30 MILS SPACING TO OTHER LINES IMPEDANCE 50 OHM CLK, DIO LENGHT MATCHED TO LESS THAN 250 MILS GROUND-REFERENCED

ROOM CPU0_CORE_VR

VCCP CPU0 VR (PAGE 1 OF 4)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. Box 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 233 OF 303

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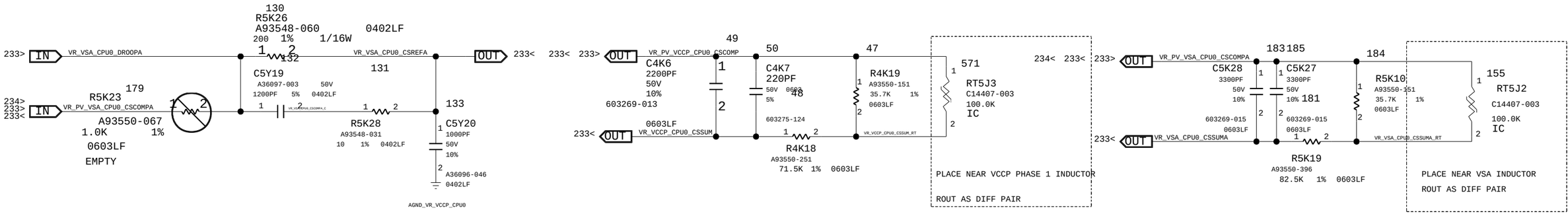
INTEL CONFIDENTIAL

ROOM CPU0_CORE_VR

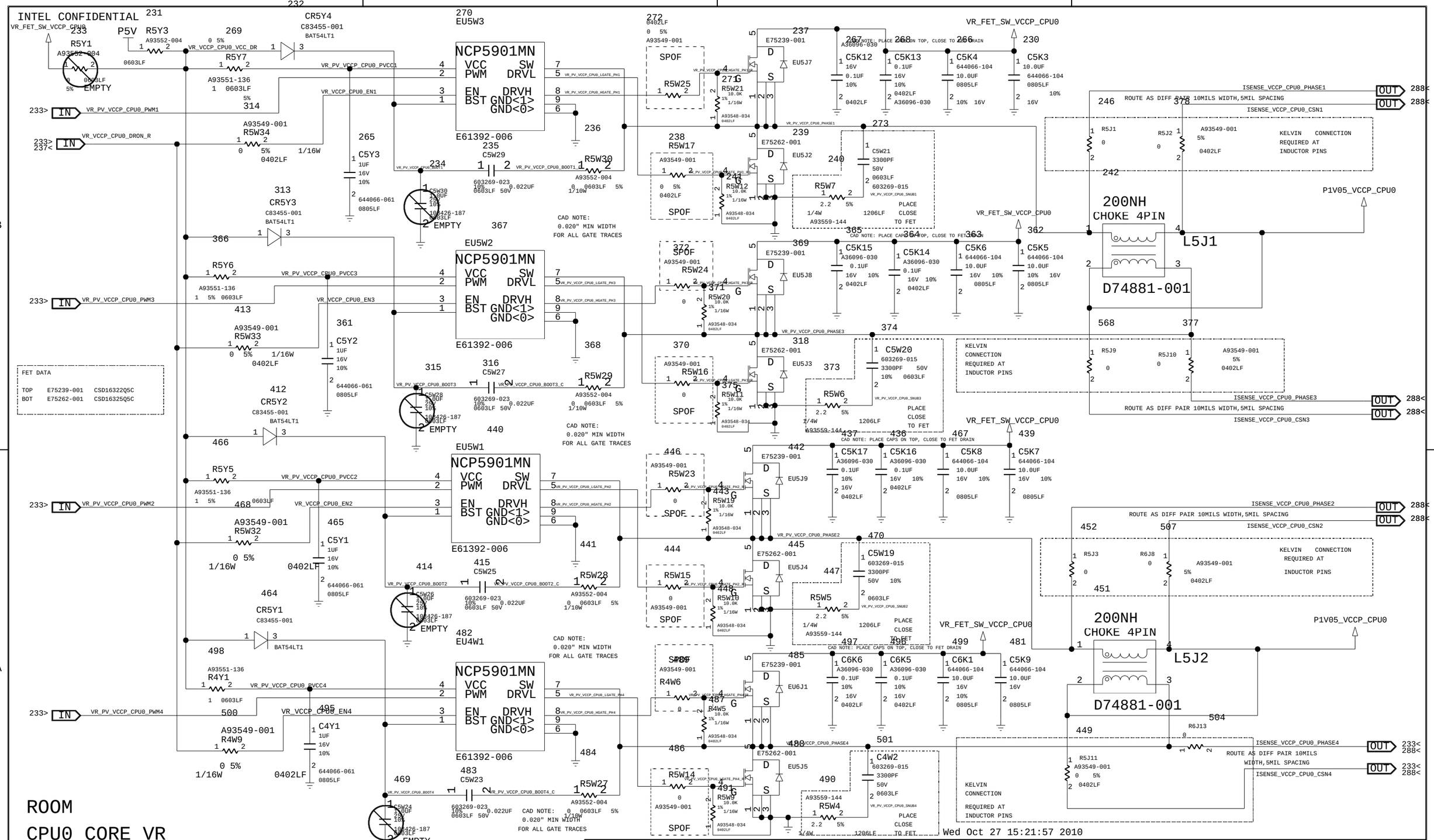


Wed Oct 27 15:21:57 2010

VCCP CPU0 VR (PAGE 2 OF 4)

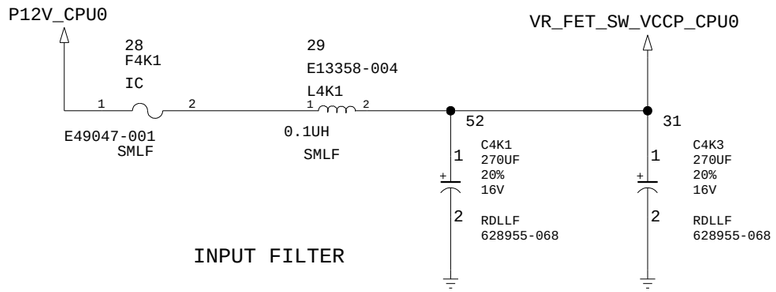
DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 234 OF 303

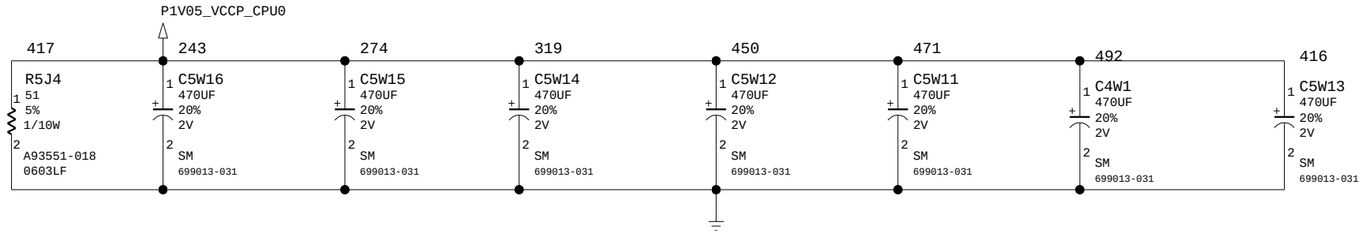
INTEL CONFIDENTIAL

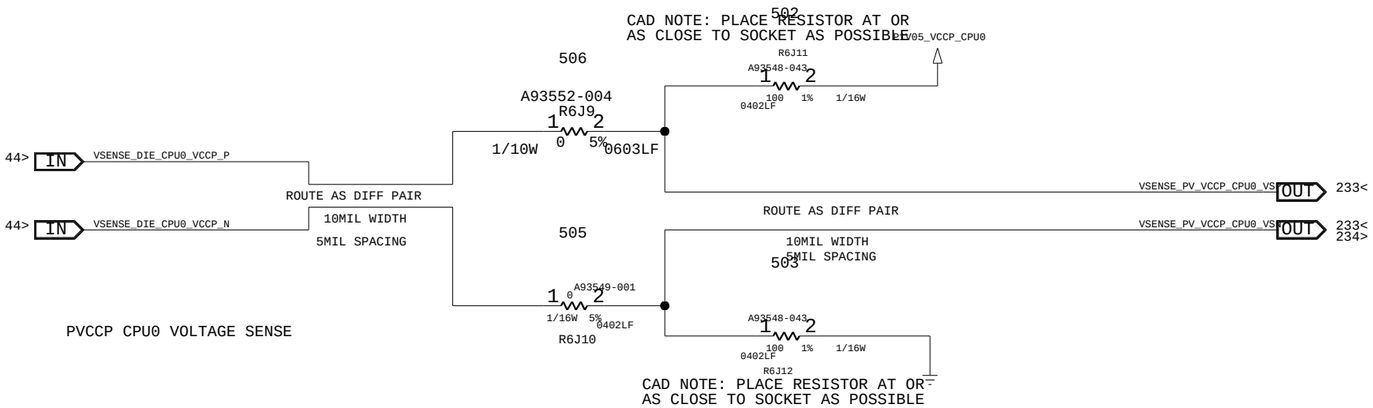


DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 235 OF 303	

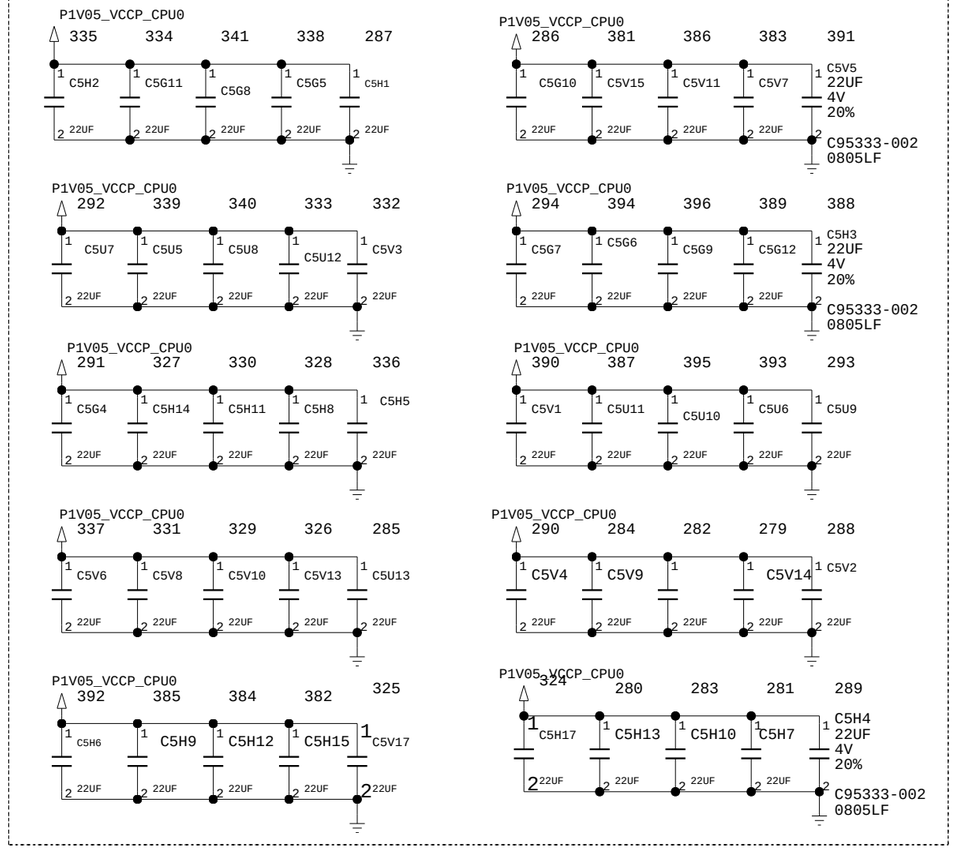
INTEL CONFIDENTIAL

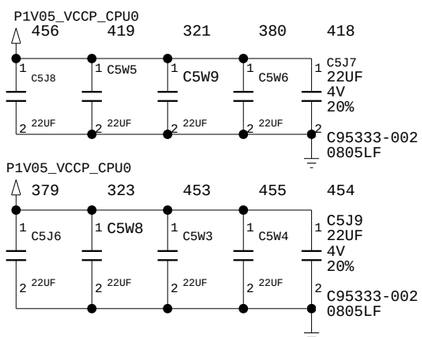


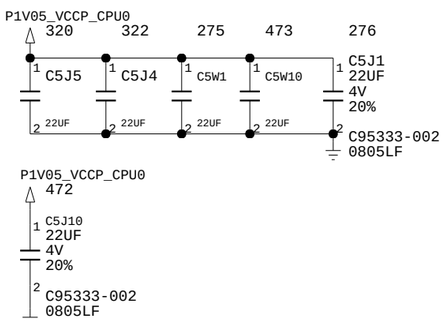




CAVITY CAPS (48X HIGH TEMP X6S)







ROOM
CPU0_CORE_VR

VCCP CPU0 VR (PAGE 4 OF 4)

Wed Oct 27 15:21:57 2010

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 236 OF 303

INTEL CONFIDENTIAL

ROOM

CPU0_VSA_VR

FET DATA

TOP	E75239-001	CSD16322Q5C
BOT	E75262-001	CSD16325Q5C

VR_FET_SW_VCCP_CPU0

192 C5K10 0.1UF 16V 10% 0402LF

191 C5K11 0.1UF 16V 10% 0402LF A36096-030

143 C5K1 10.0UF 16V 0805LF

194 C5K2 10.0UF 16V 0805LF 644066-104

CPU0_VSA_VR

P5V

142 A93552-004 R5Y4 0 5% 1/10W 0603LF

100 CR5Y5 C83455-001 BAT54LT1

147 VR_FET_SW_VCCP_CPU0

193 VR_VSA_CPU0_BOOT_VIN

VR_PV_VSA_CPU0_BOOT

A93552-004 R5X2 0 5% 1/10W EMPTY 0603LF

R5Y8 A93551-136 1 5% 0603LF

VR_PV_VSA_CPU0_BVCC

145 EU5W4

NCP5901MN

VCC SW

PWM DRVL

EN DRVH

BST GND<1>

GND<0>

E61392-006

VR_PV_VSA_CPU0_LGATE_PH

VR_PV_VSA_CPU0_HGATE_PH

233> IN VR_PV_VSA_CPU0_PWM5

195

235< 233> IN VR_VCCP_CPU0_DRON_R

R5W35 A93549-001 0 5% 0402LF

VR_VSA_CPU0_DRON

190 C5Y4 1UF 16V 10% 644066-061 0805LF

105 C6W3 470UF 20% 2V EMPTY 100426-187 SM 699013-031

144 C6W2 603269-023 100 0.022UF 0603LF 50V

VR_PV_VSA_CPU0_BOOT_C

146

149

152 R5W26 A93549-001 0 5% 0402LF

150 R5W22 10.0K 1% 1/16W A93548-034 0402LF

148 E75239-001 EU5J6

151 E75262-001 EU5J1

154 R5W13 10.0K 1% 1/16W A93548-034 0402LF

R5W18 A93549-001 0 5% 0402LF

R5W31 A93552-004 0 0603LF 5% 1/10W

VR_PV_VSA_CPU0_PHASE

196

153 C5W22 3300PF 50V 10% 0603LF 603269-015

R5W8 2.2 5% 1/4W A93559-144 1206LF

VR_PV_VSA_CPU0_SNUB

PLACE CLOSE TO FET

156 D43477-003 L5J3 0.4UH 5MLF

P0V85_VSA_CPU0

160 R5J8 0

161 R5J7 A93549-001 0 5% 0402LF

159 R5J6 0

158 R5J5 0

KELVIN CONNECTION REQUIRED AT INDUCTOR PINS

ISENSE_VSA_CPU0_CSNA

ROUTE AS DIFF PAIR 10MILS WIDTH,5MIL SPACING

OUT 233<

ISENSE_VSA_CPU0_PHASE

OUT 233<

ISENSE_VSA_CPU0_VO_PMON

ROUTE AS DIFF PAIR 10MILS WIDTH,5MIL SPACING

OUT 289<

ISENSE_VSA_CPU0_VCS_PMON

OUT 289<

P0V85_VSA_CPU0

108 C6W1 470UF 20% 2V EMPTY SM 699013-031

157 C5W18 470UF 20% 2V SM 699013-031

197 C5W17 470UF 20% 2V SM 699013-031

245 C5W7 47UF

277 C5V21 47UF

278 C5V20 47UF

244 C5J3 47UF 20% 644066-106 0805LF

162 C5J2 47UF EMPTY 644066-106

163 C5W2 47UF EMPTY 644066-106

79 R6W1 51 5% 1/10W A93551-018 0603LF

CAD NOTE: PLACE RESISTOR AT OR AS CLOSE TO SOCKET AS POSSIBLE

P0V85_VSA_CPU0

111 R4J10 A93548-043 100 1% 1/16W 0402LF

A93552-004 R4J5 0 5% 1/10W 0603LF

44> IN VSENSE_DIE_VSA0_P

44> IN VSENSE_DIE_VSA0_N

ROUTE AS DIFF PAIR 10MIL WIDTH 5MIL SPACING

VSENSE_PV_VSA_CPU0_VSPA OUT 233<

112 ROUTE AS DIFF PAIR 10MIL WIDTH 5MIL SPACING

VSENSE_PV_VSA_CPU0_VSNA OUT 233< 234>

109 A93549-001 0 1/16W 5% 0402LF R4J4

A93548-043 100 1% 1/16W 0402LF R4J8

PVSA VOLTAGE SENSE

CAD NOTE: PLACE RESISTOR AT OR AS CLOSE TO SOCKET AS POSSIBLE

VR SPECIFICATION
VOUT = SVID,+/-5MV
RIPPLE = +/-15MV
AC TOL. = +/-32MV
IOUT = 24A PEAK
IOUT = 20A TDC
IOUT STEP = 7.5A
IOUT DI/DT = 4A/US
FREQ = 484 KHZ
MINIMUM AIR FLOW=551LFM

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CPU0 VSA

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 237 OF 303	

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VR SPECIFICATION
VOUT=SVID, +/-15MV
LOAD LINE = 0.8MOHMS
RIPPLE = +/-10MV
IOUT = 165A PEAK
IOUT = 135A TDC
IOUT STEP = 106A
IOUT DI/DT=200A/US
FREQ=489KHZ
MINIMUM AIR FLOW=551LFM

R7K12 A93549-001 0402LF 0 5%
VR_VCCP_CPU1_DRON_R → VR_VCCP_CPU1_DRON
C3Y7 603269-059 1200PF 10% 50V 0603LF
R3Y12 A93550-345 1.02K 1% 1/10W 0603LF
R7K21 A93550-084 2.0K 1% 1/10W 0603LF
VR_PV_VCCP_CPU1_CSCOMP
R7K17 A93548-254 4.02K 1% 1/16W 0402LF
VR_VCCP_CPU1_CSREF
C3Y5 A36096-046 1000PF 10% 50V 0402LF
R7K18 A93548-031 10 1% 0402LF
VR_VCCP_CPU1_CSREF_R
C3Y6 A36096-046 1000PF 10% 50V 0402LF
AGND_VR_VCCP_CPU1
R2Y17 A93550-116 10.0K 1% 0603LF
R8K3 A93548-031 10 1% 0402LF
C2Y5 A36096-055 47.0NF 10V 10% 0402LF
ISENSE_VSA_CPU1_PHASE
VR_VSA_CPU1_CSREFA
ISENSE_VSA_CPU1_CSNA
ISENSE_VCCP_CPU1_PHASE1
ISENSE_VCCP_CPU1_PHASE3
ISENSE_VCCP_CPU1_PHASE2
ISENSE_VCCP_CPU1_PHASE4
R8K14 20.0K 1% 0603LF A93550-136
R7K7 R7K6 R7K8 R7K9 25.5K 1% 1/10W A93550-142 0603LF
VR_VCCP_CPU1_CSSUM
R3Y8 A93550-116 10.0K 1% 0603LF
C3Y4 A36096-055 47.0NF 10V 10% 0402LF
R7K15 A93550-116 10.0K 1% 0603LF
C7K5 A36096-055 47.0NF 10V 10% 0402LF
R3Y10 A93550-116 10.0K 1% 0603LF
C3Y3 A36096-055 47.0NF 10V 10% 0402LF
R7K16 A93550-116 10.0K 1% 0603LF
C7K4 A36096-055 47.0NF 10V 10% 0402LF
ISENSE_VCCP_CPU1_CSN1
ISENSE_VCCP_CPU1_CSN3
ISENSE_VCCP_CPU1_CSN2
ISENSE_VCCP_CPU1_CSN4
R3Y2 R3Y3 R3Y4 R3Y5 10 1% 0402LF A93548-031
VR_VCCP_CPU1_CSREF

VR_FET_SW_VCCP_CPU1
R2Y58 10.0K 1% 0402LF A93548-034
R3Y11 22.60K 1% 1/16W 0402LF A93548-212
VR_VCCP_CPU1_ILIM
VR_VCCP_CPU1_DROOP
VR_PV_VCCP_CPU1_CSCOMP
VR_PV_VCCP_CPU1_COMP
VR_VCCP_CPU1_TRBST
VR_PV_VCCP_CPU1_FB
VR_PV_VCCP_CPU1_TSENSE
VR_PV_VCCP_CPU1_CO_EN
R7J13 1.0K 1% A93550-067
VR_VCCP_CPU1_VRMP
VR_VSA_CPU1_CSPA
VSENSE_PV_VCCP_CPU1_VSP
VSENSE_PV_VSA_CPU1_VSPA
VSENSE_PV_VCCP_CPU1_VSN
VSENSE_PV_VSA_CPU1_VSNA
VR_PV_VCCP_CPU1_TSENSEA
VR_VSA_CPU1_VBOOTA
VR_VCCP_CPU1_CSP1
VR_VCCP_CPU1_CSP3
VR_VCCP_CPU1_CSP2
VR_VCCP_CPU1_CSP4
CPU1_CORE_VR

R8K42 8.25K 1% 0603LF A93550-111
R7K10 45.3K 1% 1/10W 0603LF A93550-157
C8K41 0.01UF 50V 0603LF 603269-058
R2Y60 21K 1% 1/10W 0603LF A93550-137
C3Y11 1000PF 50V 0402LF A36096-046
C8K34 A36096-046 1000PF 50V 0402LF
C7K10 A36096-046 1000PF 50V 0402LF
C2Y31 1000PF A36096-046 50V 0402LF
AGND_VR_VCCP_CPU1
R8K53 10.0K 1% 1/16W 0402LF A93548-034

CAD NOTE:
PLACE NEAR CONTROLLER

VBOOTA=0.9V (R=45.3K)

P5V
R2Y49 0 5% 0603LF A93552-004
P3V3
R7K37 5.11K 1% 0402LF A93548-157
R7K50 10.0K 1% 0402LF
R2Y54 10.0K 1% 0402LF A93548-034
VR_PV_VCCP_CPU1_VCC
C7K9 1UF 10V 10%
R3Y1 100K 5% 0402LF A93549-027
R3Y7 100K
R2Y10 100K
C8K39 1000PF 50V 10% 0402LF
A36096-046
C3Y19 A36096-046 1000PF 10% 50V 0402LF
R3Y6 100K
SWITCHING A36096-099 NCP6151A 0402LF EU7K1
R3Y9 1K 1% 1/16W 0402LF A93548-023
AGND_VR_VCCP_CPU1

NCP6151_C

VCC	11	CSREF	43
DRON	33		
DROOP	46	DROOPA	21
ILIM	47	ILIMA	20
COMP	48	COMPA	19
TRBST	49	TRBSTA	18
FB	50	FBA	17
TSENSE	2		
ENABLE	9		
VRMP	12		
	25	VR_RDY	7
CSNA	26	VR_RDYA	8
CSPA	1	CSCOMP	45
VSP	14	CSCOMPA	22
VSPA	52	IOUT	42
VSN	15	IOUTA	24
VSNA	44	DIFFOUT	51
CSSUM	23	DIFFOUTA	16
CSSUMA	13	PWM4	29
TSENSEA	27	PWM3_IMAX	31
VBOOTA	34	PWM2_VBOOT	30
CSP1	35	PWM1_ADDR	32
CSN1	36	PWMA_IMAXA	28
CSP3	37	SDIO	4
CSN3	38	SCLK	5
CSP2	39	ALERT_N	6
CSN2	40	ROSC	10
CSP4	41	VR_HOT_N	3
CSN4		TH_PAD	53

E59559-005
MAIN ADDR:00H
AUX ADDR:01H

VR_VCCP_CPU1_SVID_DIO
VR_VCCP_CPU1_SVID_CLK
VR_VCCP_CPU1_SVID_ALERT
VR_PV_VCCP_CPU1_FS
R7K4 7.50K 1% 1/16W 0402LF A93548-194
R7K5 15.8K 1% 1/10W 0603LF A93550-296
R7K14 133K 1% 1/16W 0402LF A93548-153
R7K3 10.0K 1% 1/16W 0402LF A93548-034
R8K41 4.7K 1% 0603LF A93550-392
R7K32 0 0603LF A93552-004
R8K2 0 0603LF A93552-004
AGND_VR_VCCP_CPU1

R8K26 8.45K 0.10%
VR_VSA_CPU1_DROOPA
VR_VSA_CPU1_ILIMA
A93553-081 0603LF
VR_PV_VSA_CPU1_CSCOMPA
VR_PV_VSA_CPU1_COMPA
VR_VSA_CPU1_TRBSTA
VR_PV_VSA_CPU1_FBA
VR_VCCP_CPU1_CSREF
PWRGD_VR_VCCP_CPU1_CO
PWRGD_VR_VSA_CPU1_CO
VR_PV_VCCP_CPU1_CSCOMP
VR_PV_VSA_CPU1_CSCOMPA
VR_VCCP_CPU1_IMON
VR_VSA_CPU1_IMONA
VR_VCCP_CPU1_DIFFOUT
VR_VSA_CPU1_DIFFOUTA
VR_PV_VCCP_CPU1_PWM4
VR_PV_VCCP_CPU1_PWM3
VR_PV_VCCP_CPU1_PWM2
VR_PV_VCCP_CPU1_PWM1
VR_PV_VSA_CPU1_PWM5
IRQ_VCCP_CPU1_VRHOT_N
VBOOT=0V (R=10K)

P1V05_VTT_CPU1
R7K43 100 1% 1/16W 0402LF A93548-043
R7K45 56.0 1% 1/16W 0402LF A93549-076
R7K46 5610 1% 0402LF EMPTY 5% 1/16W
C3Y1 22UF 20% 6.3V 0805LF 644066-041
AGND_VR_VCCP_CPU1
R3Y30 A93552-004
R7K30 A93552-004 0 5% 1/10W 0603LF
SVID_ALERT_CPU1 BI 55< 256<>
R3Y26 A93552-004 NOTE: VCCP TERMINATES BUS
R7K28 A93552-004 0 5% 1/10W 0603LF
SVID_DIO_CPU1 BI 256<>
R7K29 A93550-124 150 1% 1/10W 0603LF
R3Y31 A93552-004
SVID_CLK_CPU1 BI 256<>
C3Y15 1000PF EMPTY
C3Y17 1000PF EMPTY
C3Y16 1000PF 10% EMPTY 0402LF A36096-046
AGND_VR_VCCP_CPU1

CAD NOTE: ROUTE DIO LINE BETWEEN ALERT AND CLOCK 20 MILS SPACING. 30 MILS SPACING TO OTHER LINES
IMPEDANCE 50 OHM
CLK, DIO LENGHT MATCHED TO LESS THAN 250 MILS
GROUND-REFERENCED

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ROOM CPU1_CORE_VR

VCCP CPU1 VR (PAGE 1 OF 4)

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ROOM
CPU1_CORE_VR

R8K25
A93548-060 0402LF
200 1% 1/16W

238> IN VR_VSA_CPU1_DROOPA

239>
238<
238> IN VR_PV_VSA_CPU1_CSCOMPA

R8K22
A93550-067
1.0K 1%
0603LF
EMPTY

C2Y19
A36097-003 50V
1200PF 5% 0402LF

R8K27
A93548-031
10 1% 0402LF

C2Y20
1000PF
50V
10%
A36096-046
0402LF

VR_VSA_CPU1_CSREFA

OUT 238<

AGND_VR_VCCP_CPU1

238< 238> OUT VR_PV_VCCP_CPU1_CSCOMP

C7K6
2200PF
50V
10%
603269-013
0603LF

C7K7
220PF
50V 0603
5%
603275-124

R7K20
A93550-151
35.7K 1%
0603LF

238< OUT VR_VCCP_CPU1_CSSUM

R7K19
A93550-251
71.5K 1% 0603LF

239< 238< 238<

RT8J2
C14407-003
100.0K
IC

238<

PLACE NEAR VCCP PHASE 1 INDUCTOR
ROUT AS DIFF PAIR

OUT VR_PV_VSA_CPU1_CSCOMPA

C8K28
3300PF
50V
10%
603269-015
0603LF

C8K27
3300PF
50V
10%
603269-015
0603LF

R8K9
A93550-151
35.7K 1%
0603LF

RT7J1
C14407-003
100.0K
IC

OUT VR_VSA_CPU1_CSSUMA

R8K18
A93550-396
82.5K 1% 0603LF

PLACE NEAR VSA INDUCTOR
ROUT AS DIFF PAIR

R7K38
A93550-011
30.1 1%
0603LF

C3Y14
A36096-049
470PF 50V
0402LF
10%

C3Y10
603275-174
68PF 50V
0603LF 5%

238> IN VR_VCCP_CPU1_DIFFOUT

VR_PV_VCCP_CPU1_COMP OUT 238<

R7K31
A93550-067
1.0K 1% 0603LF

R7K25
A93550-096
3.4K 1%
0603LF

C3Y9
A36096-066
4700PF 50V
10% 0402LF

CR7K1
C89383-001
MMSD914
SMLF

238< IN VR_VCCP_CPU1_TRBST_A

R3Y14
0 0402LF
1/16W 5%
A93549-001

VR_VCCP_CPU1_TRBST_D

C3Y8
3300PF
50V
10%
603269-015
0603LF

R7K24
A93548-195
8.25K 1%
0402LF
1/16W

R3Y13
100 1%
A93550-026
0603LF 1/10W

VR_VCCP_CPU1_TRBST_C

VR_VCCP_CPU1_TRBST_R

R3Y22
A93548-138
2.0K
0402LF 1% 1/16W

C3Y12
A36096-075
2200PF 50V
0402LF 10%

AGND_VR_VCCP_CPU1

VR_PV_VCCP_CPU1_FB OUT 238<

C2Y34
603269-059
1200PF 50V
0603LF 10%

C2Y29
603275-162
22PF 50V
0603LF 5%

238> IN VR_VSA_CPU1_DIFFOUTA

A93550-220
R8K50
453 1% 1/10W
0603

VR_PV_VSA_CPU1_COMPA OUT 238<

R8K51
A93550-067
1.0K 1% 0603LF

R8K40
A93550-301
3.65K 1%
0603LF

C8K32
602433-008
5600PF 50V
10% 0603LF

CR8K2
C89383-001
MMSD914
SMLF

238< IN VR_VSA_CPU1_TRBSTA_A

EMPTY
R2Y37
0
0402LF 5%
1/16W
A93549-001

VR_VSA_CPU1_TRBSTA_D

R2Y36
EMPTY
A93548-034
10.0K 1%
0402LF

C2Y24
3300PF
EMPTY
50V 10%
603269-015
0603LF

R8K47
EMPTY
A93548-460
255K 1%
1/16W
0402LF

VR_VSA_CPU1_TRBSTA_R

VR_VSA_CPU1_TRBSTA_C

R2Y44
A93550-026
100 1%
0603LF
1/10W
EMPTY

R2Y48
A93549-001
0 5%
0402LF
EMPTY

C2Y28
A36096-075
2200PF 50V
0402LF 10%
EMPTY

AGND_VR_VCCP_CPU1

VR_PV_VSA_CPU1_FBA OUT 238<

VR_VCCP_CPU1_IMON OUT 238>

R7K13
A93548-212
22.60K 1%
0402LF

C3Y2
0.1UF
16V 10%
0402LF
A36096-030

VSENSE_PV_VCCP_CPU1_VSN_R

R3Y15
0 5%
1/16W
0402LF
A93549-001

R3Y18
0 5%
1/16W
0402LF
A93549-001

AGND_VR_VCCP_CPU1

VSENSE_PV_VCCP_CPU1_VSN OUT 238< 241>

VR_VSA_CPU1_IMONA OUT 238>

R8K1
29.40K
1%
1/16W
A93548-251
0402LF

C2Y6
0.1UF
16V 10%
0402LF
A36096-030

VSENSE_PV_VSA_CPU1_VSNA_R

R2Y14
0 5%
1/16W
0402LF
A93549-001

R8K5
0 5%
1/16W
0402LF
A93549-001

AGND_VR_VCCP_CPU1

VSENSE_PV_VSA_CPU1_VSNA OUT 238< 242>

VR_PV_VCCP_CPU1_TSENSEA OUT 238<

RT7J3
100.0K
C14407-003
SMLF

C2Y30
0.1UF
50V
10%
602433-061
0603LF

AGND_VR_VCCP_CPU1

PLACE NEAR VSA FETS

R7K35
A93552-004
0 0603LF
5%

VR_PV_VCCP_CPU1_TSENSE_R

RT8J3
100.0K
IC
C14407-003
SMLF

R3Y23
A93550-111
8.25K 1%
0603LF

VR_PV_VCCP_CPU1_TSENSE OUT 238<

C3Y13
603269-058
0.01UF
0603LF
50V
X7R

AGND_VR_VCCP_CPU1

PLACE NEAR VCCP PHASE 1 FETS

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VCCP CPU1 VR (PAGE 2 OF 4)

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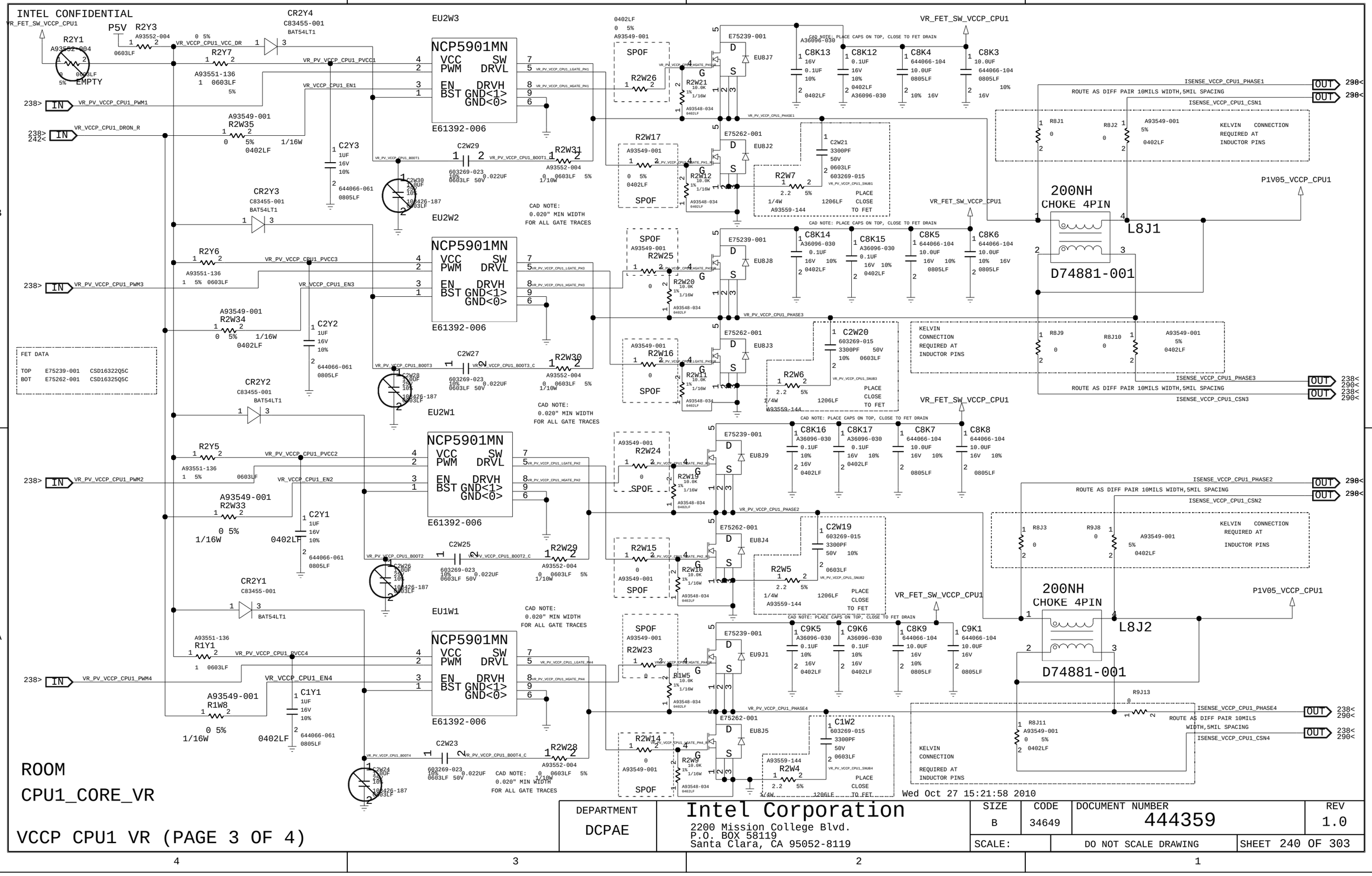

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		SCALE:	DO NOT SCALE DRAWING		SHEET 240 OF 303

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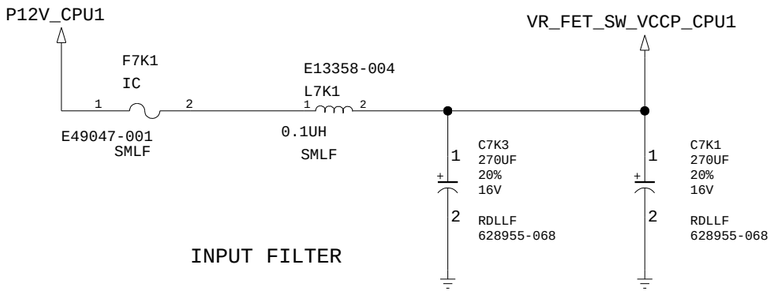

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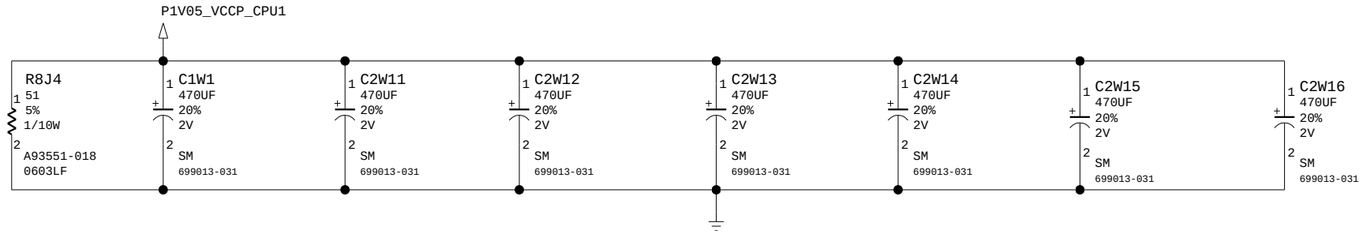
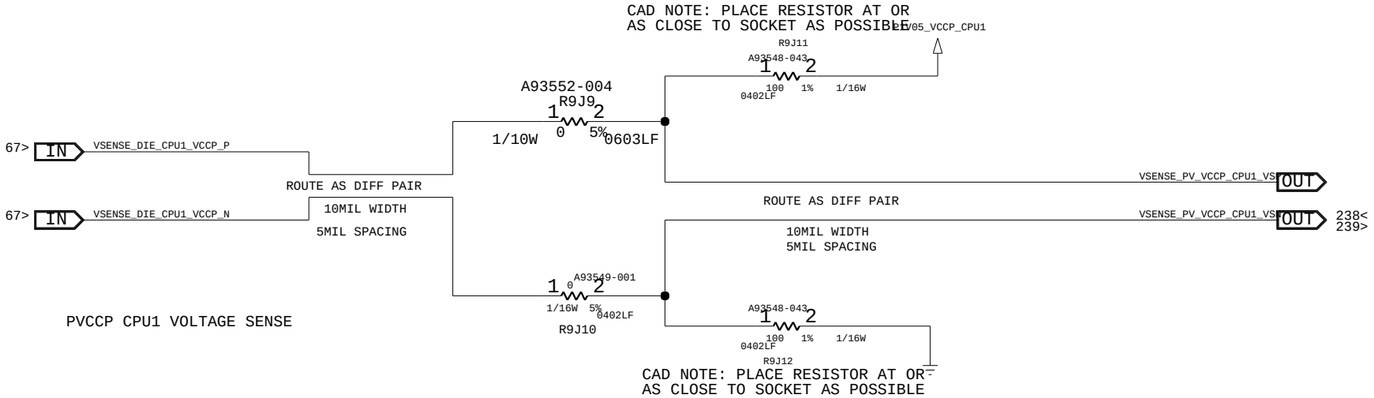
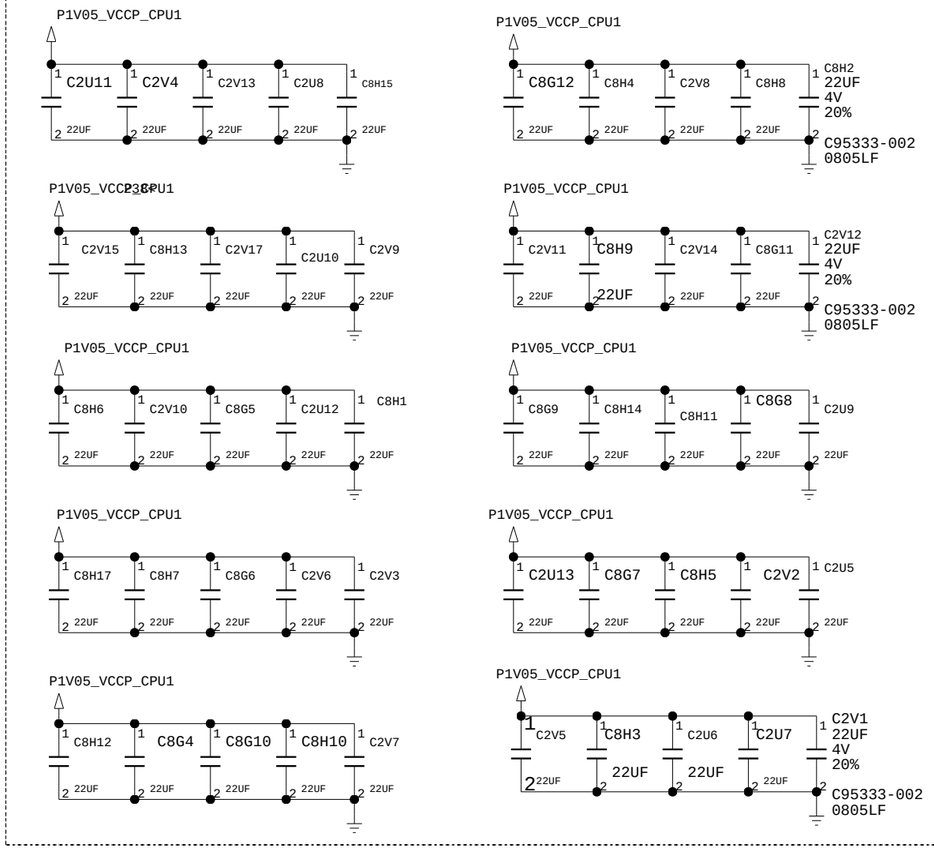
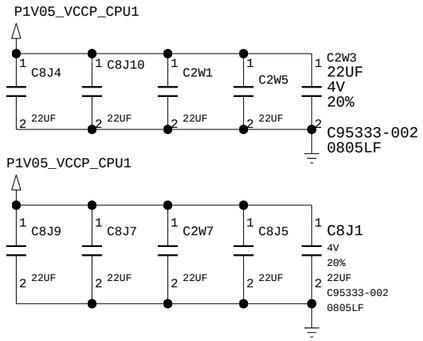


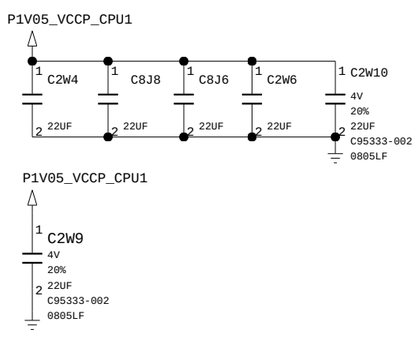


PVCCP CPU1 VOLTAGE SENSE

CAVITY CAPS (48X HIGH TEMP X6S)







ROOM
CPU1_CORE_VR

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VCCP CPU1 VR (PAGE 4 OF 4)

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ROOM

CPU1_VSA_VR

FET DATA

TOP	E75239-001	CSD16322Q5C
BOT	E75262-001	CSD16325Q5C

VR_FET_SW_VCCP_CPU1

P5V

A93552-004 R2Y4 0 5% 1/10W 0603LF

A93552-004 R2Y2 0 5% 1/10W 0603LF

CR3Y1 C83455-001 BAT54LT1

A93551-136 R2Y8 1 5% 1/10W 0603LF

VR_VSA_CPU1_BOOT_VIN

VR_PV_VSA_CPU1_BOOT

VR_PV_VSA_CPU1_PVCC

EU2W4

NCP5901MN

VCC SW

PWM DRVL

EN DRVH

BST GND<1>

GND<0>

E61392-006

238> IN VR_PV_VSA_CPU1_PWM5

238> 240< IN VR_VCCP_CPU1_DRON_R

R2W36 A93549-001 0 5% 0402LF

VR_VSA_CPU1_DRON

C2Y4 1UF 16V 10% 644066-061 0805LF

C3W2 603269-023 10% 0603LF 50V 0.022UF

R2W32 A93552-004 0 0603LF 5% 1/10W

C3W3 470UF 20% 2V EMPTY 108426-187 6003LF

VR_PV_VSA_CPU1_LGATE_PH

VR_PV_VSA_CPU1_HGATE_PH

R2W27 A93549-001 0 5% 0402LF

R2W22 10.0K 1% 1/16W A93548-034 0402LF

R2W18 A93549-001 0 5% 0402LF

R2W13 10.0K 1% 1/16W A93548-034 0402LF

E75239-001 EU8J6

E75262-001 EU8J1

VR_PV_VSA_CPU1_PHASE

C2W22 3300PF 50V 10% 603269-015

VR_PV_VSA_CPU1_SNUB

PLACE CLOSE TO FET

R2W8 2.2 5% 1/4W 120LF A93559-144

VR_FET_SW_VCCP_CPU1

C8K11 0.1UF 16V 10% 0402LF

C8K10 0.1UF 16V 10% 0402LF A36096-030

C8K1 10.0UF 16V 0805LF

C8K2 10.0UF 16V 0805LF 644066-104

CPU1_VSA_VR

D43477-003 L8J3 0.4UH SMLF

P0V85_VSA_CPU1

R8J8 R8J7 A93549-001 0 5% 0402LF R8J6 R8J5

KELVIN CONNECTION REQUIRED AT INDUCTOR PINS

ISENSE_VSA_CPU1_CSNA

ROUTE AS DIFF PAIR 10MILS WIDTH,5MIL SPACING

ISENSE_VSA_CPU1_PHASE

ISENSE_VSA_CPU1_VO_PMON

ROUTE AS DIFF PAIR 10MILS WIDTH,5MIL SPACING

ISENSE_VSA_CPU1_VCS_PMON

OUT 238<

OUT 238<

OUT 291<

OUT 291<

P0V85_VSA_CPU1

C3W1 470UF 20% 2V EMPTY SM 699013-031

C2W17 470UF 20% 2V SM 699013-031

C2W18 470UF 20% 2V SM 699013-031

C8J3 47UF

C2W8 47UF

C2V21 47UF

C2V20 47UF 4V 20% 644066-106 0805LF

C2W2 47UF EMPTY

C8J2 47UF EMPTY

R3W1 51 5% 1/10W A93551-018 0603LF

CAD NOTE: PLACE RESISTOR AT OR AS CLOSE TO SOCKET AS POSSIBLE

P0V85_VSA_CPU1

R7J10 A93548-043 100 1% 1/16W 0402LF

A93552-004 R7J5 0 5% 1/10W 0603LF

67> IN VSENSE_DIE_VSA1_P

67> IN VSENSE_DIE_VSA1_N

ROUTE AS DIFF PAIR 10MIL WIDTH 5MIL SPACING

VSENSE_PV_VSA_CPU1_VSPA OUT 238<

VSENSE_PV_VSA_CPU1_VSNA OUT 238< 239>

ROUTE AS DIFF PAIR 10MIL WIDTH 5MIL SPACING

A93549-001 0 1/16W 5% 0402LF R7J4

A93548-043 100 1% 1/16W 0402LF R7J8

PVSA VOLTAGE SENSE

CAD NOTE: PLACE RESISTOR AT OR AS CLOSE TO SOCKET AS POSSIBLE

VR SPECIFICATION
VOUT = SVID,+/-5MV
RIPPLE = +/-15MV
AC TOL. = +/-32MV
IOUT = 24A PEAK
IOUT = 20A TDC
IOUT STEP = 7.5A
IOUT DI/DT = 4A/US
FREQ = 484 KHZ
MINIMUM AIR FLOW=551LFM

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CPU1 VSA

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 242 OF 303	

INTEL CONFIDENTIAL

VR SPECIFICATION
VOUT=SVID, +/-15MV
LOAD LINE = 0.8MOHMS
RIPPLE = +/-10MV
IOUT = 165A PEAK
IOUT = 135A TDC
IOUT STEP = 106A
IOUT DI/DT=200A/US
FREQ=489 KHZ
MINIMUM AIR FLOW=551LFM

CAD NOTE:
PLACE NEAR CONTROLLER

VBOOTA=0.9V (R=45.3K)

CAD NOTE: ROUTE DIO LINE BETWEEN ALERT AND CLOCK 20 MILS SPACING. 30 MILS SPACING TO OTHER LINES IMPEDANCE 50 OHM CLK, DIO LENGHT MATCHED TO LESS THAN 250 MILS GROUND-REFERENCED

VBOOT=0V (R=10K)

ROOM CPU2_CORE_VR

VCCP CPU2 VR (PAGE 1 OF 4)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 243 OF 303	

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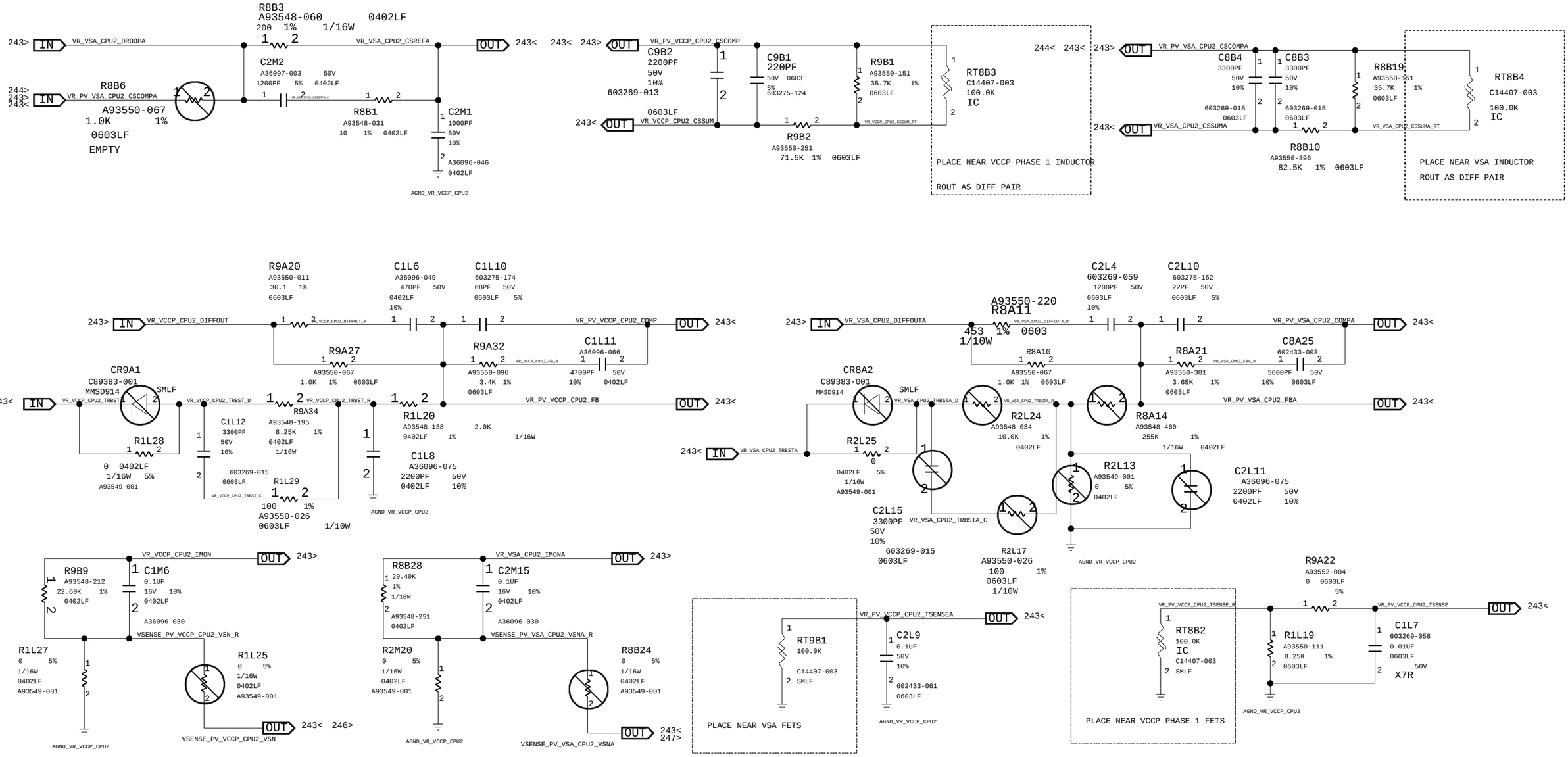
INTEL CONFIDENTIAL

ROOM
CPU2_CORE_VR

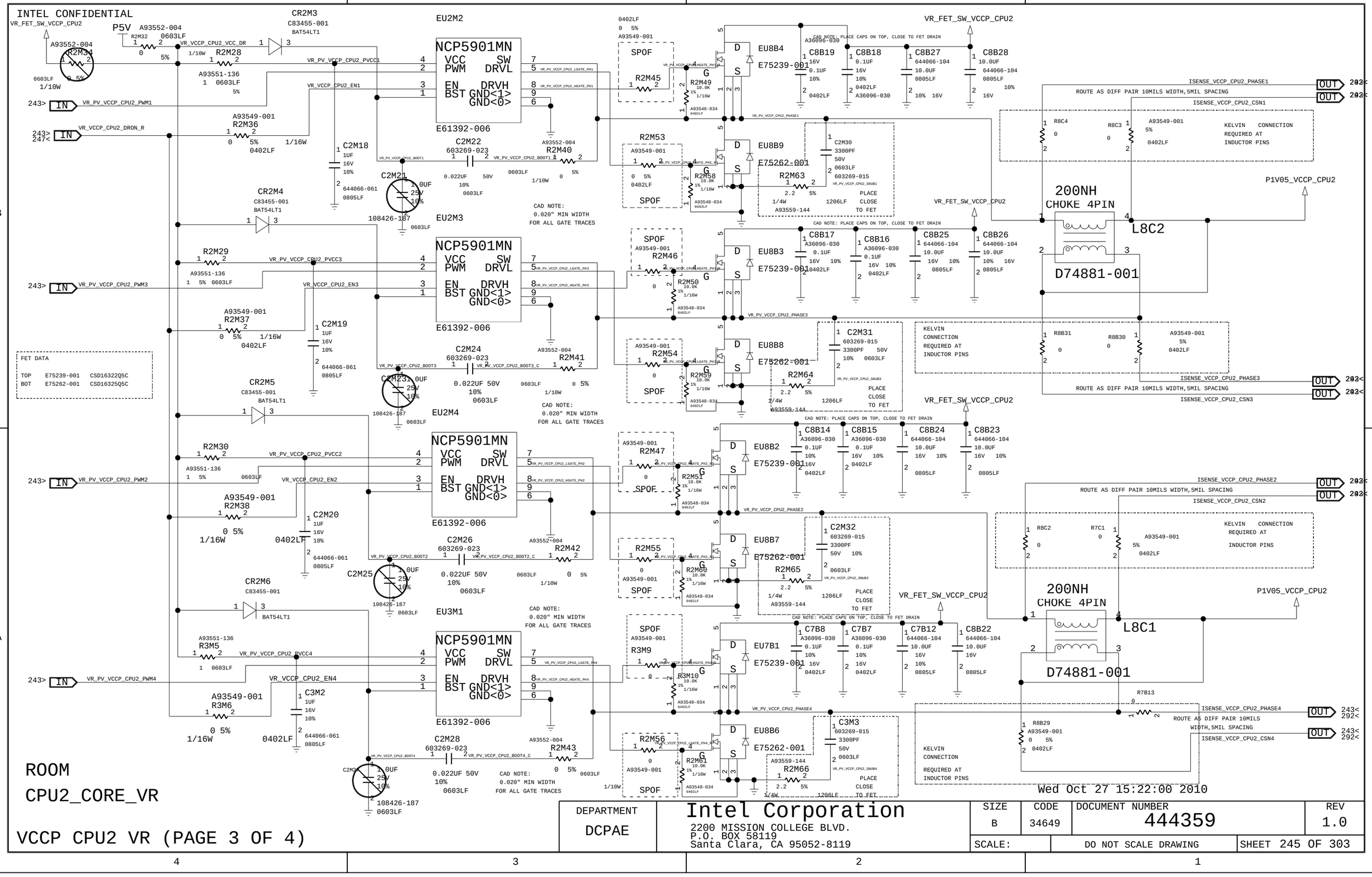


Wed Oct 27 15:21:59 2010

VCCP CPU2 VR (PAGE 2 OF 4)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 244 OF 303

INTEL CONFIDENTIAL



ROOM

CPU2_CORE_VR

VCCP CPU2 VR (PAGE 3 OF 4)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 MISSION COLLEGE BLVD. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 245 OF 303	

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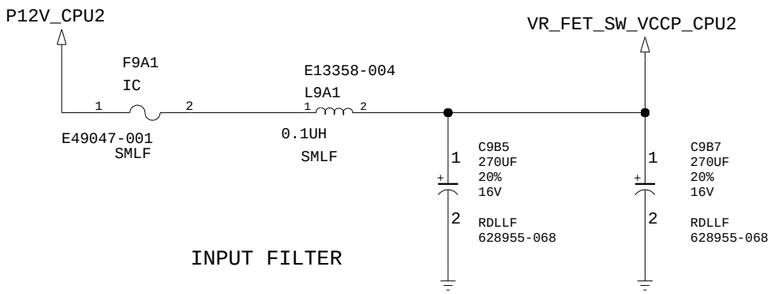
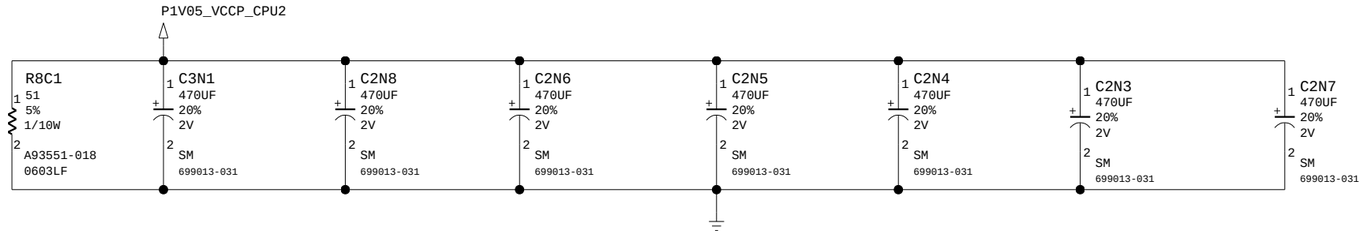
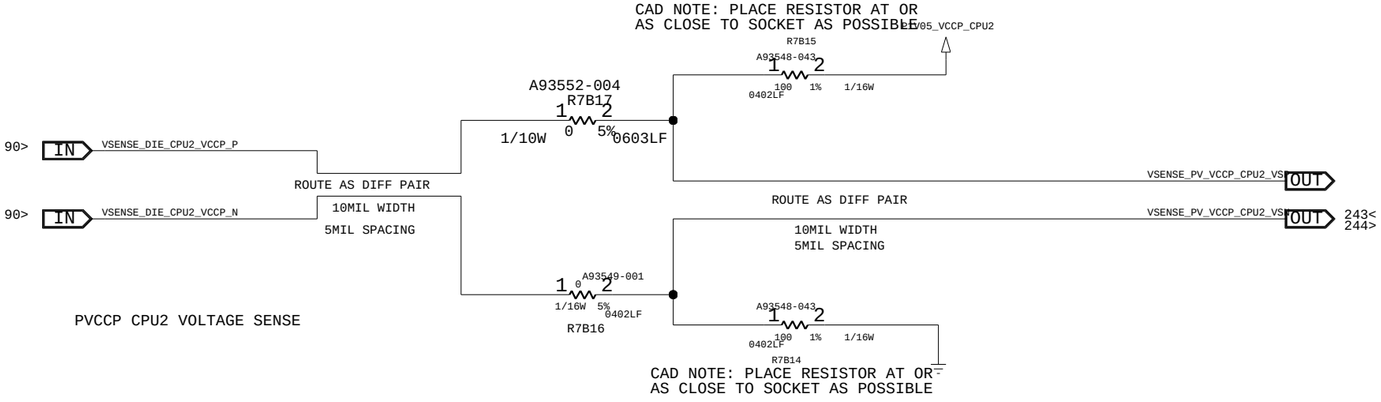
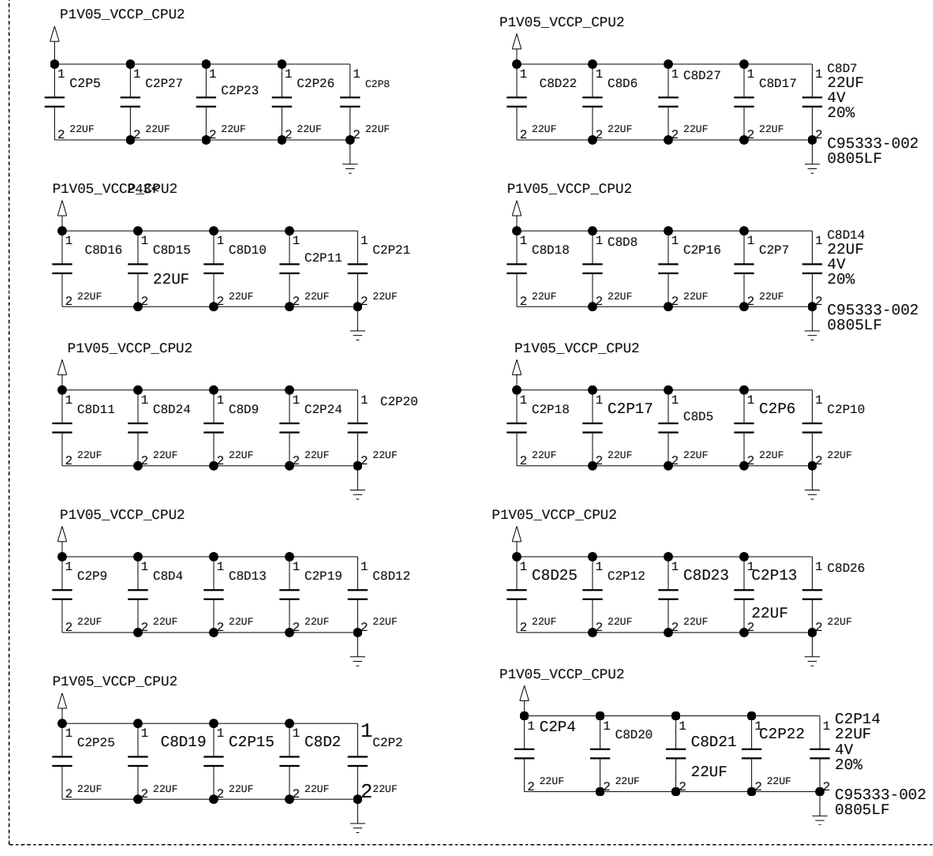
INTEL CONFIDENTIAL

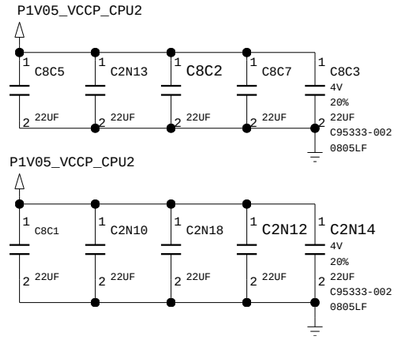


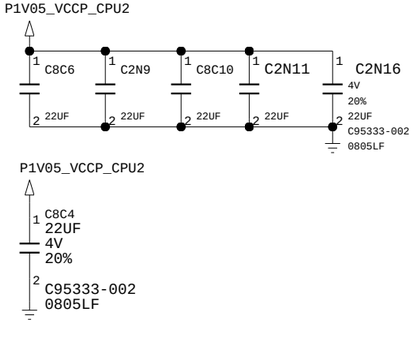




CAVITY CAPS (48X HIGH TEMP X6S)







ROOM
CPU2_CORE_VR

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VCCP CPU2 VR (PAGE 4 OF 4)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 246 OF 303	

INTEL CONFIDENTIAL

ROOM

CPU2_VSA_VR

FET DATA

TOP	E75239-001	CSD16322Q5C
BOT	E75262-001	CSD16325Q5C

VR_FET_SW_VCCP_CPU2

P5V

0603LF A93552-004 R2M31 0 5% 1/10W

CR2M2 C83455-001 BAT54LT1

VR_VSA_CPU2_BOOT_VIN

VR_PV_VSA_CPU2_BOOT

A93552-004 R2M33 0 5% 0603LF 1/10W

R2M27 A93551-136 1 5% 0603LF

VR_PV_VSA_CPU2_PVCC

EU2M1

NCP5901MN

VCC SW

PWM DRVL

EN DRVH

BST GND<1>

GND<0>

E61392-006

VR_PV_VSA_CPU2_LGATE_PH

VR_PV_VSA_CPU2_HGATE_PH

243> IN VR_PV_VSA_CPU2_PWM5

245< 243> IN VR_VCCP_CPU2_DRON_R

R2M35 A93549-001 0 5% 0402LF

VR_VSA_CPU2_DRON

C2M17 1UF 16V 10% 644066-061 0805LF

C1M8 1.0UF 25V 10% EMPTY 108426-187 0603LF

C1M9 603269-023 0.022UF 50V 10% 0603LF

VR_PV_VSA_CPU2_BOOT_C

A93552-004 R2M39 0 5% 0603LF 1/10W

R2M44 A93549-001 0 5% 0402LF

VR_PV_VSA_CPU2_HGATE_PH_R

R2M48 10.0K 1% 1/16W A93548-034 0402LF

EU8B5 E75239-001

VR_PV_VSA_CPU2_PHASE

R2M52 A93549-001 0 5% 0402LF

VR_PV_VSA_CPU2_LGATE_PH_R

R2M57 10.0K 1% 1/16W A93548-034 0402LF

EU8B10 E75262-001

C2M29 3300PF 50V 10% 0603LF 603269-015

VR_PV_VSA_CPU2_SNUB

PLACE CLOSE TO FET

R2M62 2.2 5% 1/4W A93559-144 1206LF

C8B21 0.1UF 16V 10% 0402LF

C8B20 0.1UF 16V 10% 0402LF A36096-030

C8B29 10.0UF 16V 0805LF

C8B30 10.0UF 16V 0805LF 644066-104

P0V85_VSA_CPU2

D43477-003 L8B1 0.4UH SMLF

R8B32 R8B33 A93549-001 0 5% 0402LF R8B34 R8B35

KELVIN CONNECTION REQUIRED AT INDUCTOR PINS

ISENSE_VSA_CPU2_CSNA OUT 243<

ROUTE AS DIFF PAIR 10MILS WIDTH,5MIL SPACING

ISENSE_VSA_CPU2_PHASE OUT 243<

ISENSE_VSA_CPU2_VO_PMON OUT 293<

ROUTE AS DIFF PAIR 10MILS WIDTH,5MIL SPACING

ISENSE_VSA_CPU2_VCS_PMON OUT 293<

P0V85_VSA_CPU2

C1N1 470UF 20% 2V EMPTY SM 699013-031

C2N1 470UF 20% 2V SM 699013-031

C2N2 470UF 20% 2V SM 699013-031

C2N15 47UF

C8C8 47UF

C2N20 47UF

C2N21 47UF 20% 644066-106 0805LF

C2N17 47UF

C8C9 47UF

R1M11 51 5% 1/10W A93551-018 0603LF

VR SPECIFICATION
VOUT = SVID,+/-5MV
RIPPLE = +/-15MV
AC TOL. = +/-32MV
IOUT = 24A PEAK
IOUT = 20A TDC
IOUT STEP = 7.5A
IOUT DI/DT = 4A/US
FREQ = 484 KHZ
MINIMUM AIR FLOW=551LFM

CAD NOTE: PLACE RESISTOR AT OR AS CLOSE TO SOCKET AS POSSIBLE

P0V85_VSA_CPU2

R9B24 A93548-043 100 1% 1/16W 0402LF

A93552-004 R9C4 0 5% 1/10W 0603LF

90> IN VSENSE_DIE_VSA2_P

90> IN VSENSE_DIE_VSA2_N

ROUTE AS DIFF PAIR 10MIL WIDTH 5MIL SPACING

VSENSE_PV_VSA_CPU2_VSPA OUT 243<

ROUTE AS DIFF PAIR 10MIL WIDTH 5MIL SPACING

VSENSE_PV_VSA_CPU2_VSNA OUT 243< 244>

A93549-001 R9C5 0 1/16W 5% 0402LF

A93548-043 100 1% 1/16W 0402LF R9C1

PVSA VOLTAGE SENSE

CAD NOTE: PLACE RESISTOR AT OR AS CLOSE TO SOCKET AS POSSIBLE

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CPU2 VSA

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 247 OF 303

INTEL CONFIDENTIAL

VR SPECIFICATION
VOUT=SVID, +/-15MV
LOAD LINE = 0.8MOHMS
RIPPLE = +/-10MV
IOUT = 165A PEAK
IOUT = 135A TDC
IOUT STEP = 106A
IOUT DI/DT=200A/US
FREQ=489KHZ
MINIMUM AIR FLOW=551LFM

CAD NOTE:
PLACE NEAR CONTROLLER

VBOOTA=0.9V (R=45.3K)

VBOOT=0V (R=10K)

CAD NOTE: ROUTE DIO LINE BETWEEN ALERT AND CLOCK 20 MILS SPACING. 30 MILS SPACING TO OTHER LINES IMPEDANCE 50 OHM CLK, DIO LENGHT MATCHED TO LESS THAN 250 MILS GROUND-REFERENCED

ROOM CPU3_CORE_VR

VCCP CPU3 VR (PAGE 1 OF 4)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 248 OF 303	

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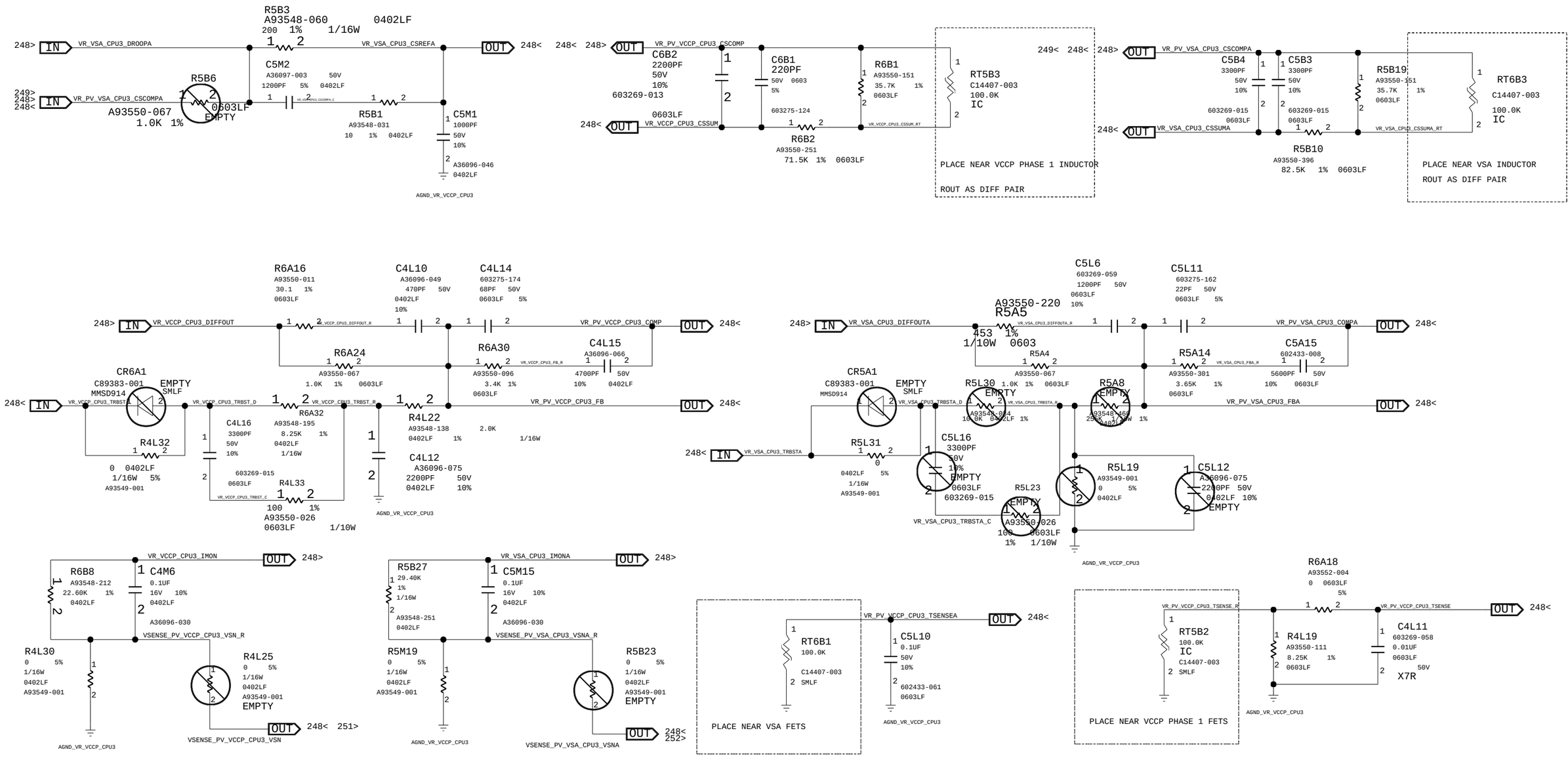
INTEL CONFIDENTIAL

ROOM
CPU3_CORE_VR

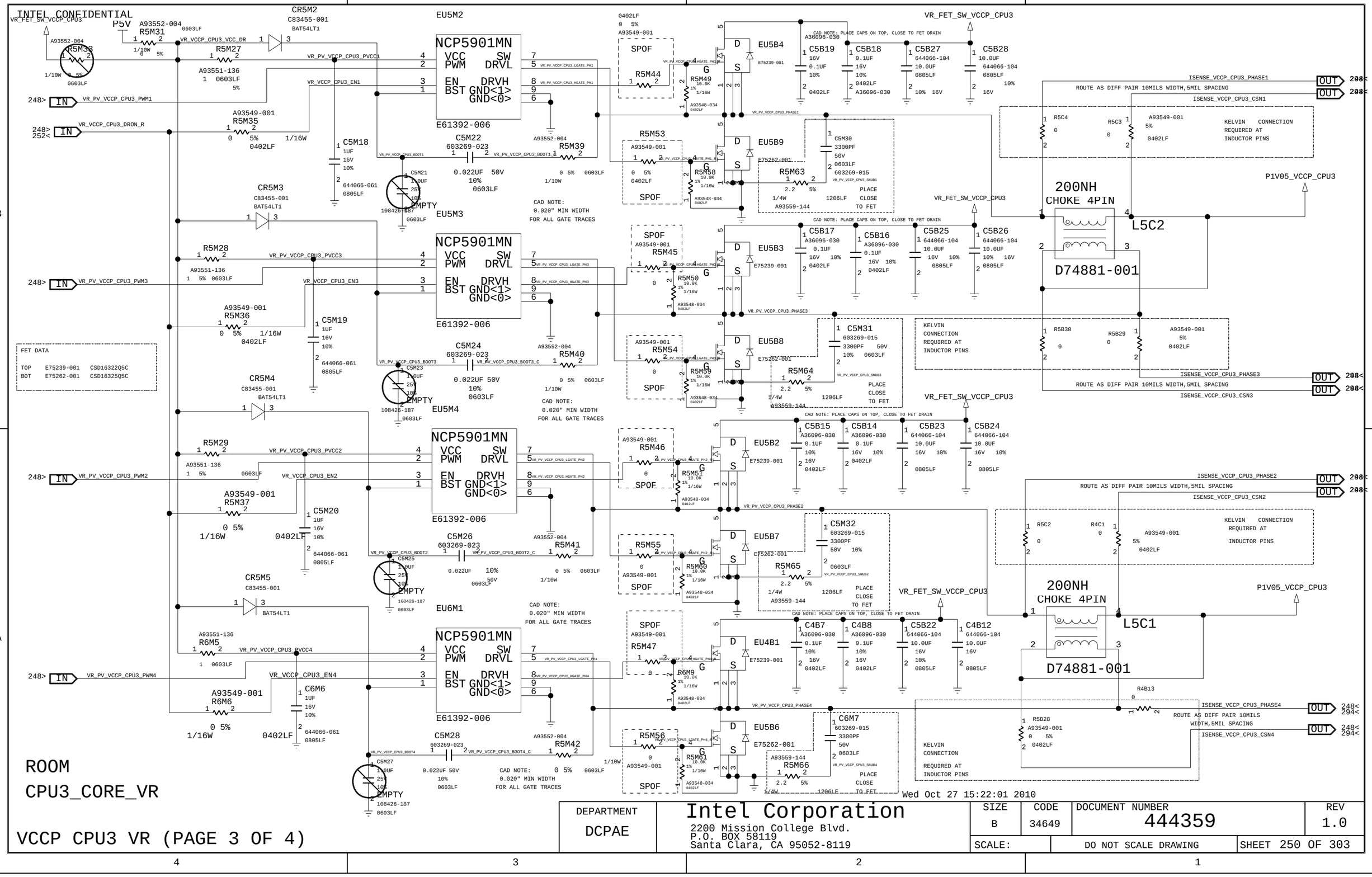


Wed Oct 27 15:22:01 2010

VCCP CPU3 VR (PAGE 2 OF 4)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 249 OF 303

INTEL CONFIDENTIAL



ROOM
CPU3_CORE_VR

VCCP CPU3 VR (PAGE 3 OF 4)

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DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 250 OF 303	

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P12V_CPU3

F6A2
IC
E49047-001
SMLF

E13358-004
L6A1
0.1UH
SMLF

VR_FET_SW_VCCP_CPU3

C6B5
270UF
20%
16V
RDLLF
628955-068

C6B7
270UF
20%
16V
RDLLF
628955-068

INPUT FILTER

P1V05_VCCP_CPU3

R5C1
51
5%
1/10W
A93551-018
0603LF

C5N8 C6N1 C5N3 C5N4 C5N5 C5N7 C5N6
470UF
20%
2V
SM
699013-031

CAD NOTE: PLACE RESISTOR AT OR
AS CLOSE TO SOCKET AS POSSIBLE

P1V05_VCCP_CPU3

R4B15
A93548-043
100 1% 1/16W
0402LF

A93552-004
R4B17
0 5%
1/10W 0603LF

113> IN VSENSE_DIE_CPU3_VCCP_P
ROUTE AS DIFF PAIR
VSENSE_PV_VCCP_CPU3_VSP OUT

113> IN VSENSE_DIE_CPU3_VCCP_N
10MIL WIDTH
5MIL SPACING
ROUTE AS DIFF PAIR
10MIL WIDTH
5MIL SPACING
VSENSE_PV_VCCP_CPU3_VSN OUT 248< 249>

A93549-001
0
1/16W 5% 0402LF
R4B16

A93548-043
100 1% 1/16W
0402LF
R4B14

PVCCP CPU3 VOLTAGE SENSE

CAD NOTE: PLACE RESISTOR AT OR
AS CLOSE TO SOCKET AS POSSIBLE

CAVITY CAPS (48X HIGH TEMP X6S)

P1V05_VCCP_CPU3

C5P11 C5P15 C5P25 C5N18 C5P12
C5N10 C5D22 C5N16 C5D9 C5N11
C5P16 C5N14 C5C5 C5P21 C5C7
C5D23 C5P13 C5N15 C5D27 C5D26
C5P7 C5D25 C5D8 C5P18 C5P5
C5D14 C5N12 C5D4 C5D5 C5D24
C5D15 C5N13 C5C10 C5P27 C5P6
C5P23 C5D11 C5P3 C5D7
C5P22 C5C4 C5D13 C5P9 C5D16
C5P24 C5C2 C5D18 C5P17 C5P19

22UF

C95333-002
0805LF

P1V05_VCCP_CPU3

C5P4 C5D6 C5P14 C5P26 C5D2
C5D21 C5D20 C5C3 C5P20 C5P8

22UF
4V
20%
C95333-002
0805LF

P1V05_VCCP_CPU3

C5C6 C5D19 C5P10 C5D10 C5D17
22UF
4V
20%
C95333-002
0805LF

P1V05_VCCP_CPU3

C5C1
22UF
4V
20%
C95333-002
0805LF

ROOM
CPU3_CORE_VR

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VCCP CPU3 VR (PAGE 4 OF 4)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 251 OF 303	

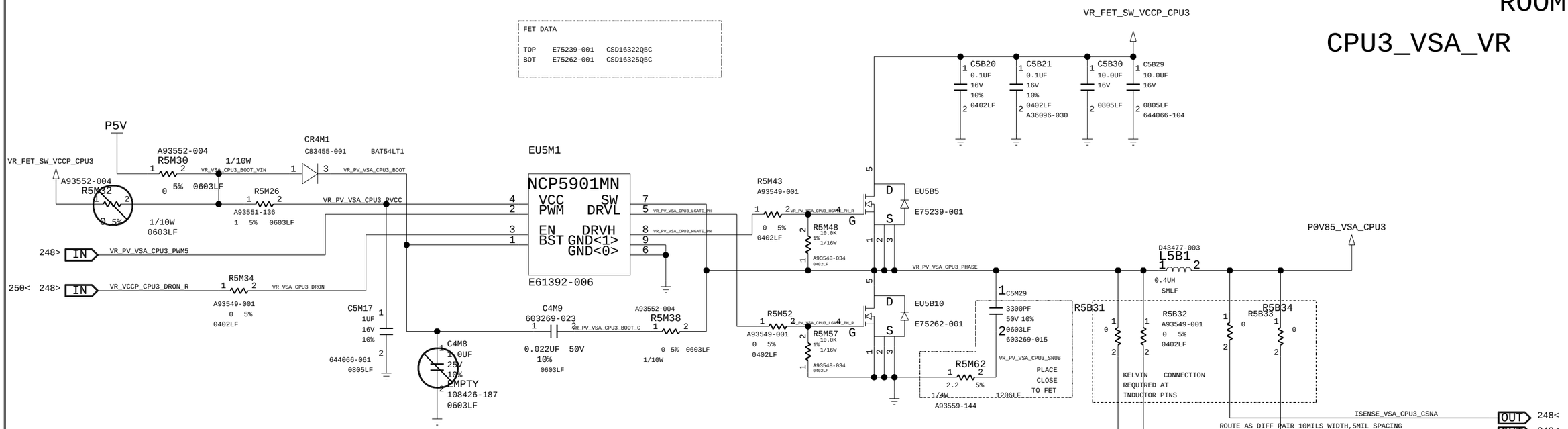
INTEL CONFIDENTIAL

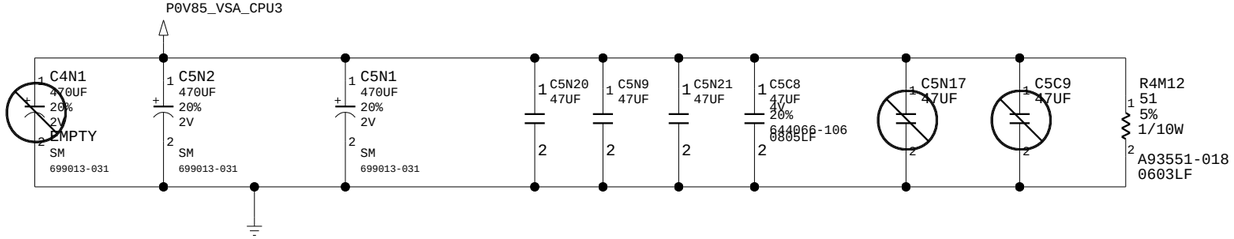
ROOM

CPU3_VSA_VR

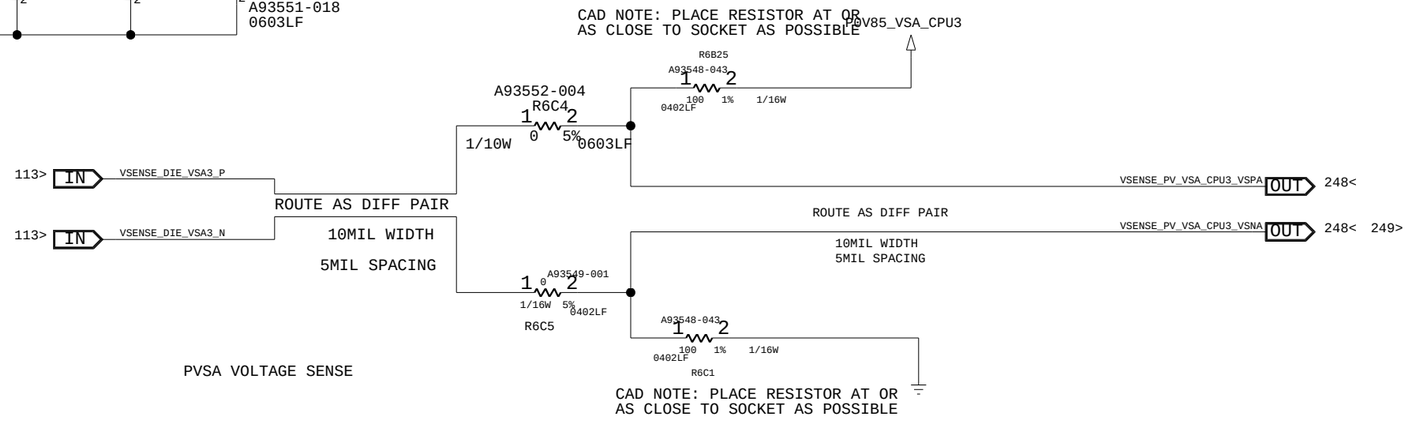
FET DATA

TOP	E75239-001	CSD16322Q5C
BOT	E75262-001	CSD16325Q5C





VR SPECIFICATION
VOUT = SVID,+/-5MV
RIPPLE = +/-15MV
AC TOL. = +/-32MV
IOUT = 24A PEAK
IOUT = 20A TDC
IOUT STEP = 7.5A
IOUT DI/DT = 4A/US
FREQ = 484 KHZ
MINIMUM AIR FLOW=551LFM



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CPU3 VSA

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 252 OF 303	

INTEL CONFIDENTIAL

ROOM = DDR3_CPU0_VDDQ_VR

NCP6151_C

SWITCHING NCP6151A EU5K4

VCC, CSREF, DRON, DROOP, ILIM, COMP, TRBST, FB, TSENSE, ENABLE, VRMP, CSNA, CSPA, VSP, VSPA, VSN, VSNA, CSSUM, CSSUMA, TSENSEA, VBOOTA, CSP1, CSN1, CSP3, CSN3, CSP2, CSN2, CSP4, CSN4, DROOPA, IMONA, COMPA, TRBSTA, FBA, VR_RDY, VR_RDYA, CSCOMP, CSCOMPA, IOUT, IOUTA, DIFFOUT, DIFFOUTA, PWM4, PWM3_IMAX, PWM2_VBOOT, PWM1_ADDR, PWMA_IMAXA, SDIO, SCLK, ALERT_N, ROSC, VR_HOT_N, TH_PAD

E59559-005

MAIN ADDR: 02H

AUX ADDR: N/A

VR SPECIFICATION
VOUT = 1.5V OR 1.35V, +/-0.5%
RIPPLE = +/-0.5%
AC TOL. = +/-2.5%
IOUT = 74A PEAK
IOUT = 56A TDC
IOUT STEP = 47.4A
IOUT DI/DT = 10.8A/US
FREQ = 600KHZ
MINIMUM AIR FLOW=551LFM

VBOOT = 1.5V(R=165K)

PLACE NEAR INDUCTOR ROUT AS DIFF PAIR

PLACE NEAR FETS

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CPU0 DDR3 VDDQ VR (PAGE 1 OF 2)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 253 OF 303

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CPU0 DDR3 VDDQ VR (PAGE 2 OF 2)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 254 OF 303	

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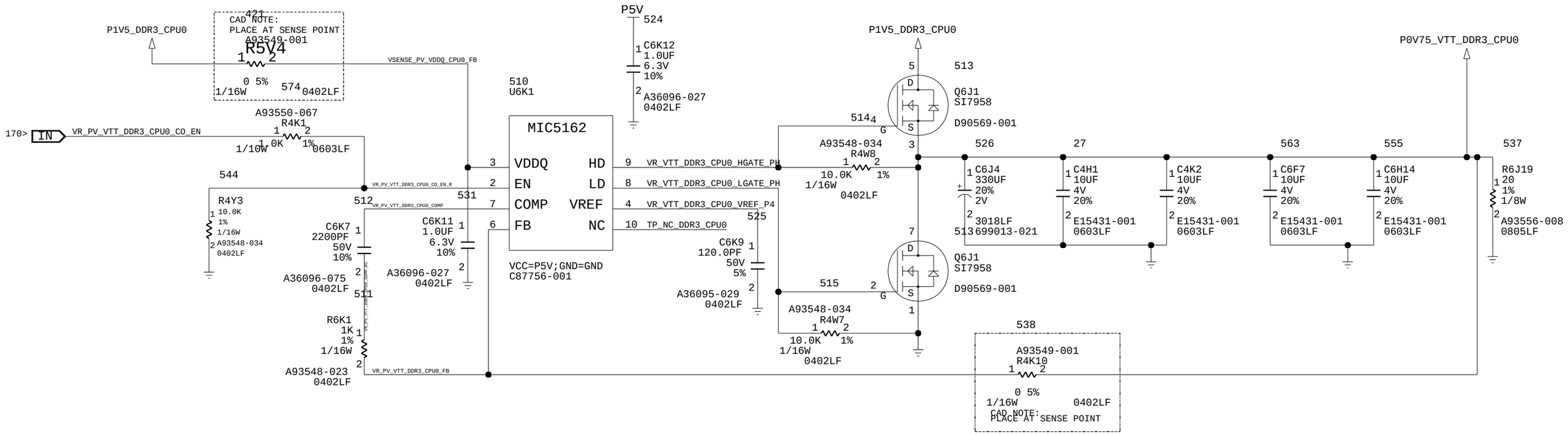
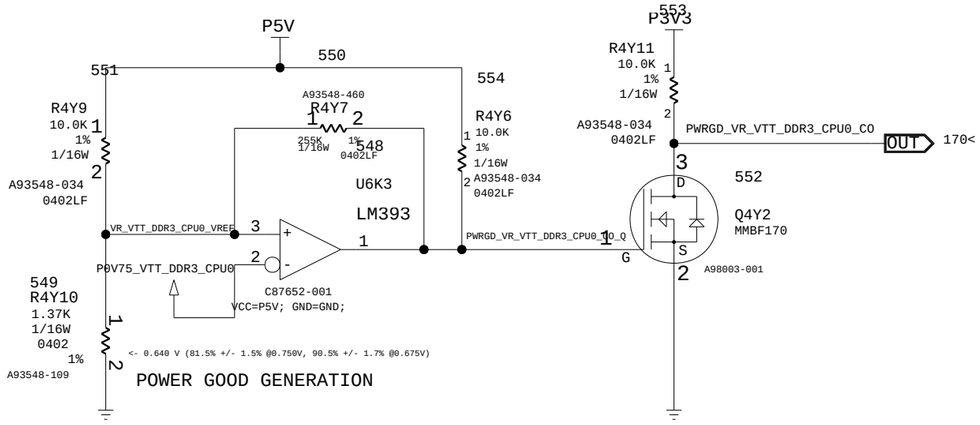
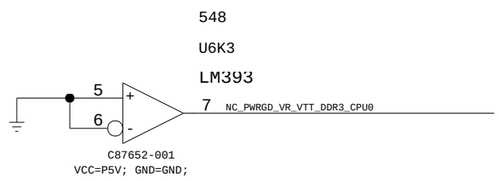
INTEL CONFIDENTIAL

ROOM

VTT_DDR3_CPU0_VR







VR SPECIFICATION
VOUT=1/2 VDDQ
DC & AC TOL. = 1/2VDDQ +/- 39MV
"IOUT=+/-2.9A PEAK
IOUT=+/-2.5A TDC
IOUT STEP=0.8A
STEP DI/DT=1A/US
MINIMUM AIR FLOW=551LFM

Wed Oct 27 15:22:02 2010

CPU0 DDR3 VTT

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 255 OF 303	

INTEL CONFIDENTIAL

ROOM = DDR3_CPU1_VDDQ_VR

NCP6151_C

SWITCHING
NCP6151A
EU8K4

11	VCC	CSREF	43
33	DRON		
46	DROOP	DROOPA	21
47	ILIM	ILIMA	20
48	COMP	COMPA	19
49	TRBST	TRBSTA	18
50	FB	FBA	17
2	TSENSE		
9	ENABLE	VR_RDY	7
12	VRMP	VR_RDYA	8
		CSCOMP	45
25	CSNA	CSCOMPA	22
26	CSPA	IOUT	42
1	VSP	IOUTA	24
14	VSPA	DIFFOUT	51
52	VSN	DIFFOUTA	16
15	VSNA	PWM4	29
44	CSSUM	PWM3_IMAX	31
23	CSSUMA	PWM2_VBOOT	30
13	TSENSEA	PWM1_ADDR	32
27	VBOOTA	PWMA_IMAXA	28
34	CSP1	SDIO	4
35	CSN1	SCLK	5
36	CSP3	ALERT_N	6
37	CSN3	ROSC	10
38	CSP2		
39	CSN2	VR_HOT_N	3
40	CSP4	TH_PAD	53
41	CSN4		

E59559-005

MAIN ADDR: 02H
AUX ADDR: N/A

VR SPECIFICATION
VOUT = 1.5V OR 1.35V, +/-0.5%
RIPPLE = +/-0.5%
AC TOL. = +/-2.5%
IOUT = 74A PEAK
IOUT = 56A TDC
IOUT STEP = 47.4A
IOUT DI/DT = 10.8A/US
FREQ = 600KHZ
MINIMUM AIR FLOW=551LFM

PLACE NEAR FETS

PLACE NEAR INDUCTOR ROUT AS DIFF PAIR

VBOOT = 1.5V(R=165K)

Wed Oct 27 15:22:03 2010

CPU1 DDR3 VDDQ VR (PAGE 1 OF 2)

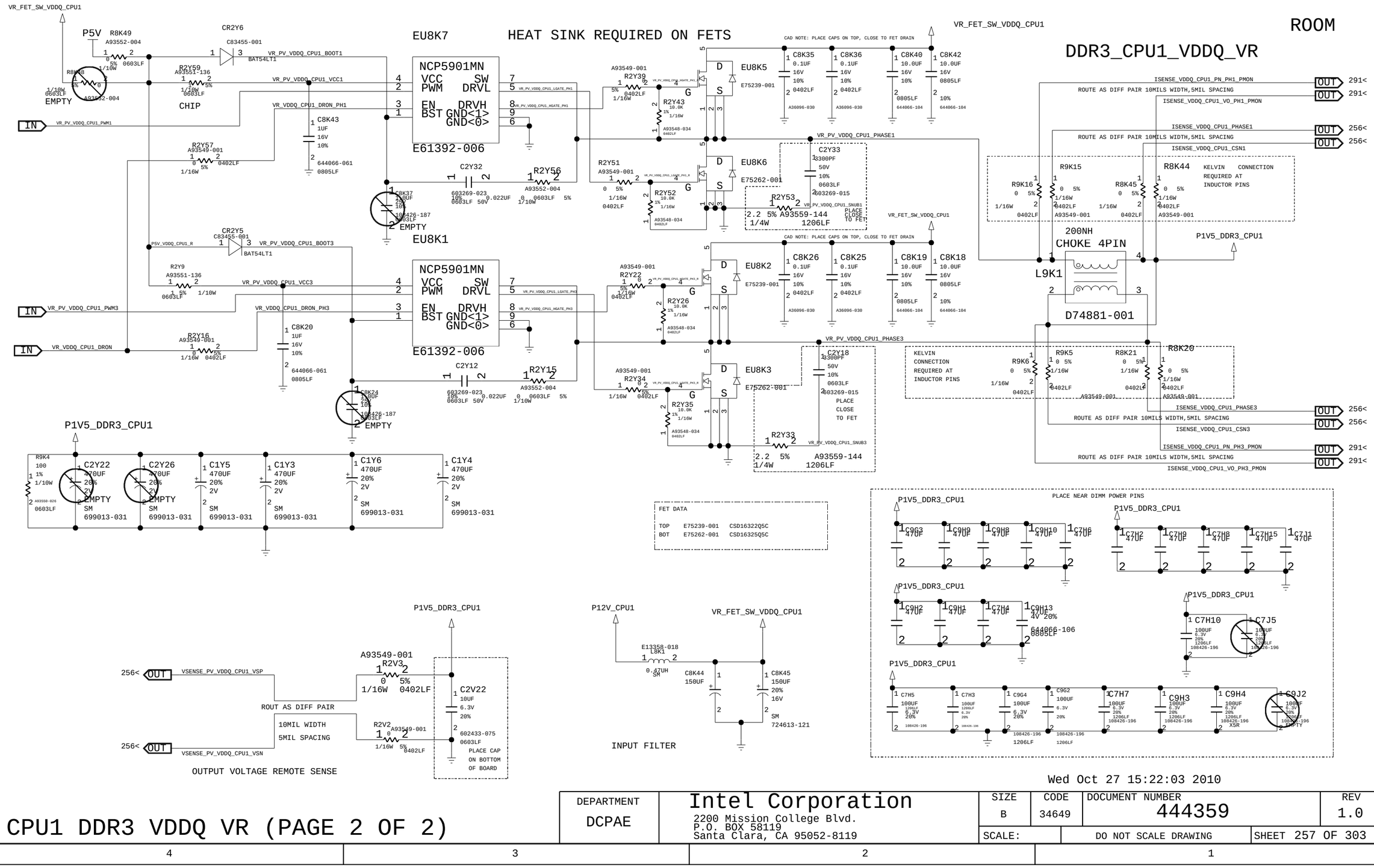
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 MISSION COLLEGE BLVD. P.O. BOX 58119 SANTA CLARA, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 256 OF 303	

INTEL CONFIDENTIAL

CPU1 DDR3 VDDQ VR (PAGE 2 OF 2)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 257 OF 303

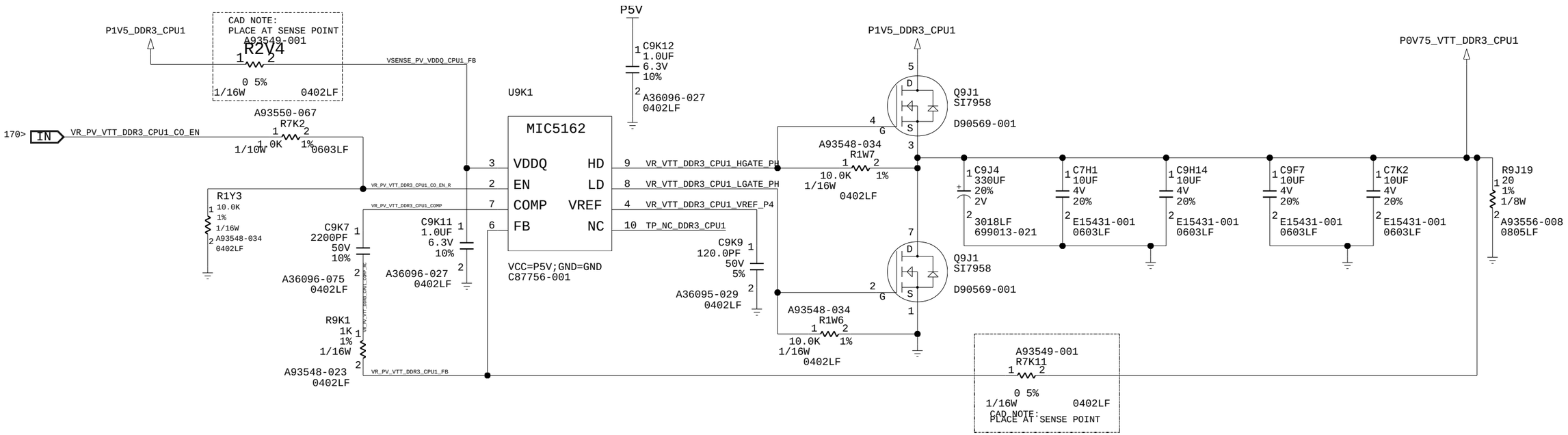
Wed Oct 27 15:22:03 2010

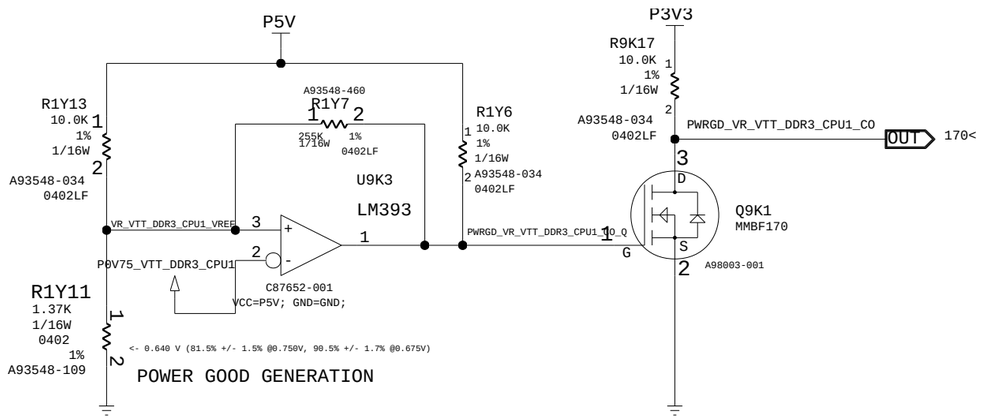


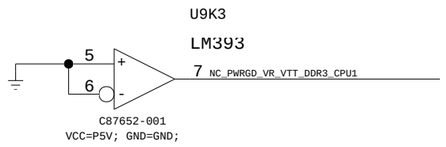
INTEL CONFIDENTIAL

ROOM

VTT_DDR3_CPU1_VR







VR SPECIFICATION
VOUT=1/2 VDDQ
DC & AC TOL. = 1/2VDDQ +/- 39MV
IOUT=+/-2.9A PEAK
IOUT=+/-2.5A TDC
IOUT STEP=0.8A
STEP DI/DT=1A/US
MINIMUM AIR FLOW=551LFM

Wed Oct 27 15:22:03 2010

CPU1 DDR3 VTT

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 258 OF 303

INTEL CONFIDENTIAL

ROOM = DDR3_CPU2_VDDQ_VR

NCP6151_C

SWITCHING
NCP6151A
EU8A4

11	VCC	CSREF	43
33	DRON		
46	DROOP	DROOPA	21
47	ILIM	ILIMA	20
48	COMP	COMPA	19
49	TRBST	TRBSTA	18
50	FB	FBA	17
2	TSENSE		
9	ENABLE	VR_RDY	7
12	VRMP	VR_RDYA	8
		CSCOMP	45
25	CSNA	CSCOMPA	22
26	CSPA	IOUT	42
1	VSP	IOUTA	24
14	VSPA	DIFFOUT	51
52	VSN	DIFFOUTA	16
15	VSNA	PWM4	29
44	CSSUM	PWM3 IMAX	31
23	CSSUMA	PWM2 VBOOT	30
13	TSENSEA	PWM1 ADDR	32
27	VBOOTA	PWMA_IMAXA	28
34	CSP1	SDIO	4
35	CSN1	SCLK	5
36	CSP3	ALERT_N	6
37	CSN3	ROSC	10
38	CSP2		
39	CSN2	VR_HOT_N	3
40	CSP4		
41	CSN4	TH_PAD	53

E59559-005

MAIN ADDR: 02H
AUX ADDR: N/A

VR SPECIFICATION
VOUT = 1.5V OR 1.35V, +/-0.5%
RIPPLE = +/-0.5%
AC TOL. = +/-2.5%
IOUT = 74A PEAK
IOUT = 56A TDC
IOUT STEP = 47.4A
IOUT DI/DT = 10.8A/US
FREQ = 600KHZ
MINIMUM AIR FLOW=551LFM

VBOOT = 1.5V(R=165K)

PLACE NEAR FETS

PLACE NEAR INDUCTOR ROUT AS DIFF PAIR

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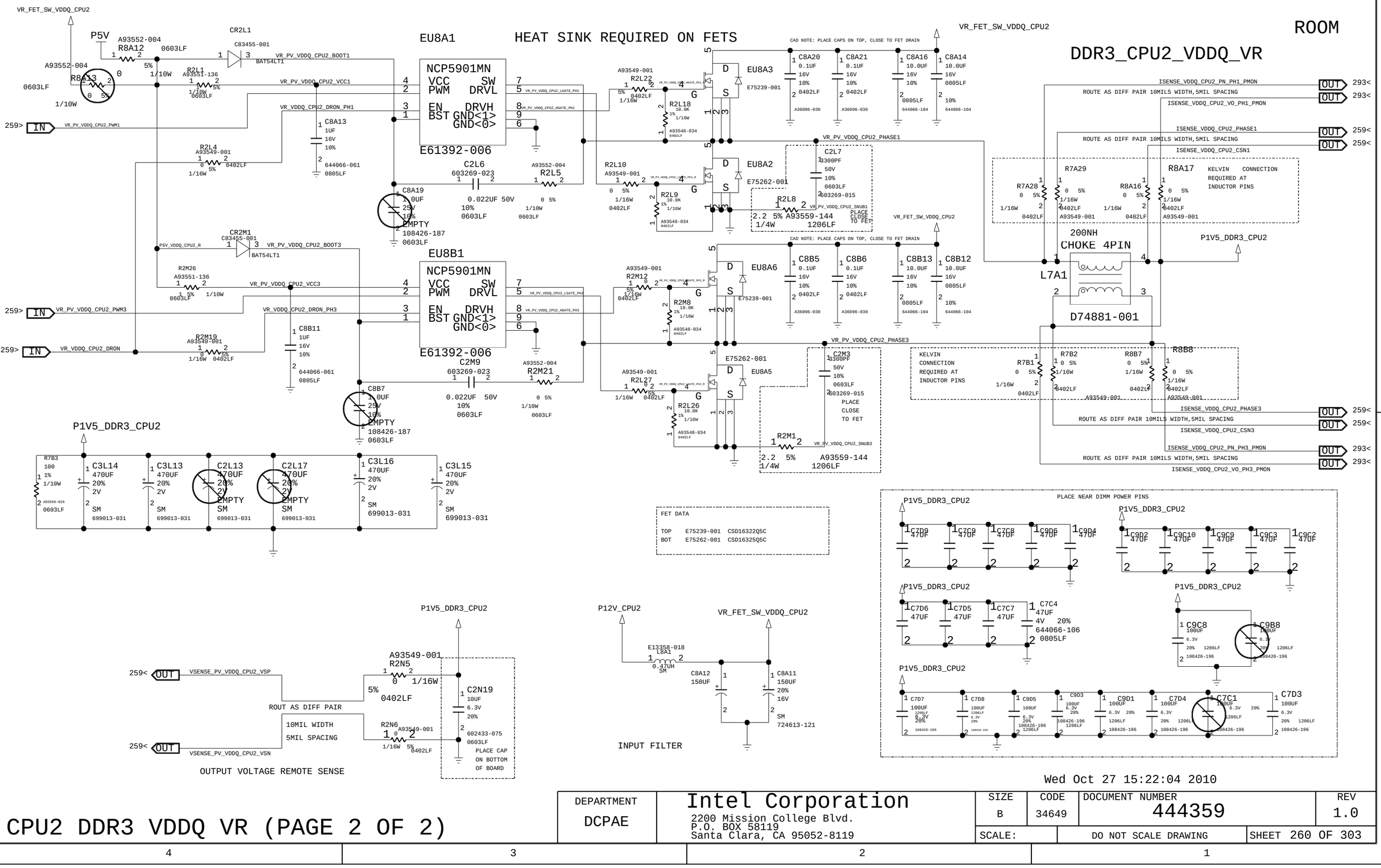
CPU2 DDR3 VDDQ VR (PAGE 1 OF 2)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 MISSION COLLEGE BLVD. P.O. BOX 58119 SANTA CLARA, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 259 OF 303	

INTEL CONFIDENTIAL

CPU2 DDR3 VDDQ VR (PAGE 2 OF 2)



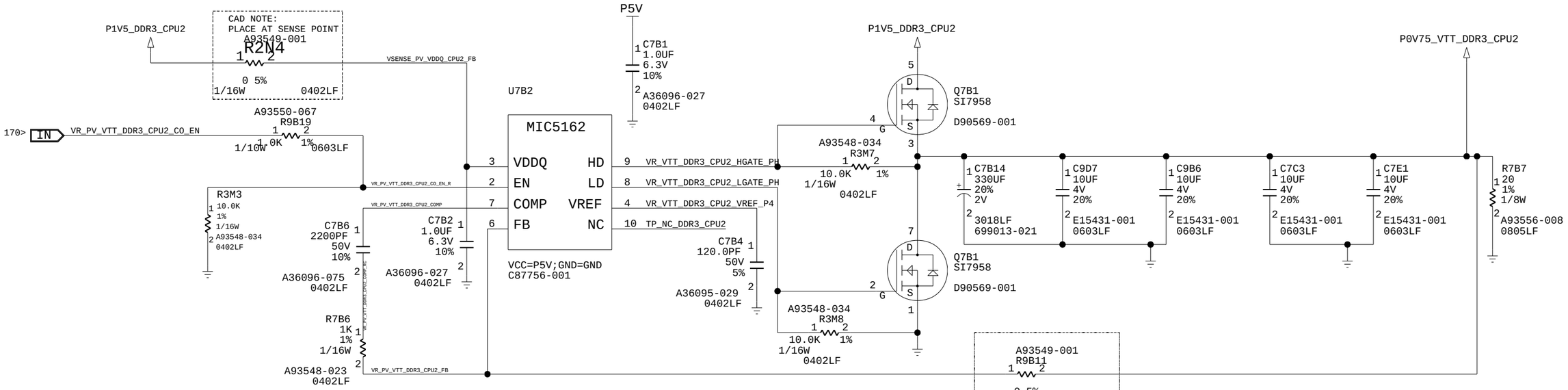
Wed Oct 27 15:22:04 2010

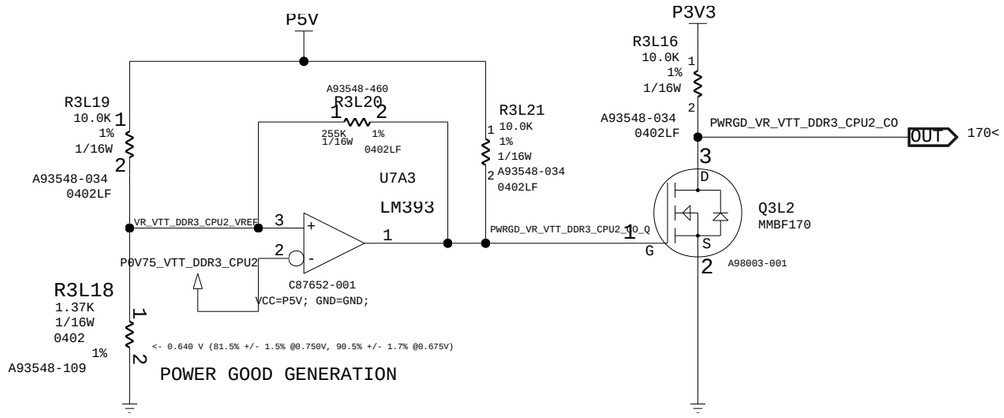
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 260 OF 303	

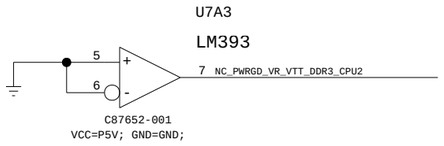
INTEL CONFIDENTIAL

ROOM

VTT_DDR3_CPU2_VR







VR SPECIFICATION
VOUT=1/2 VDDQ
DC & AC TOL. = 1/2VDDQ +/- 39MV
IOUT=+/-2.9A PEAK
IOUT=+/-2.5A TDC
IOUT STEP=0.8A
STEP DI/DT=1A/US
MINIMUM AIR FLOW=551LFM

Wed Oct 27 15:22:04 2010

CPU2 DDR3 VTT

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 261 OF 303	

INTEL CONFIDENTIAL

ROOM = DDR3_CPU3_VDDQ_VR

NCP6151_C

SWITCHING
NCP6151A
EU5A4

11	VCC	CSREF	43
33	DRON		
46	DROOP	DROOPA	21
47	ILIM	ILIMA	20
48	COMP	COMPA	19
49	TRBST	TRBSTA	18
50	FB	FBA	17
2	TSENSE		
9	ENABLE	VR_RDY	7
12	VRMP	VR_RDYA	8
		CSCOMP	45
25	CSNA	CSCOMPA	22
26	CSPA	IOUT	42
1	VSP	IOUTA	24
14	VSPA	DIFFOUT	51
52	VSN	DIFFOUTA	16
15	VSNA	PWM4	29
44	CSSUM	PWM3_IMAX	31
23	CSSUMA	PWM2_VBOOT	30
13	TSENSEA	PWM1_ADDR	32
27	VBOOTA	PWMA_IMAXA	28
34	CSP1	SDIO	4
35	CSN1	SCLK	5
36	CSP3	ALERT_N	6
37	CSN3	ROSC	10
38	CSP2		
39	CSN2	VR_HOT_N	3
40	CSP4	TH_PAD	53
41	CSN4		

E59559-005

MAIN ADDR: 02H
AUX ADDR: N/A

VR SPECIFICATION
VOUT = 1.5V OR 1.35V, +/-0.5%
RIPPLE = +/-0.5%
AC TOL. = +/-2.5%
IOUT = 74A PEAK
IOUT = 56A TDC
IOUT STEP = 47.4A
IOUT DI/DT = 10.8A/US
FREQ = 600KHZ
MINIMUM AIR FLOW=551LFM

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CPU3 DDR3 VDDQ VR (PAGE 1 OF 2)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 MISSION COLLEGE BLVD. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 262 OF 303	

INTEL CONFIDENTIAL

CPU3 DDR3 VDDQ VR (PAGE 2 OF 2)

EU5A1 NCP5901MN VCC SW PWM DRVL EN DRVH BST GND<1> GND<0> E61392-006

EU5B1 NCP5901MN VCC SW PWM DRVL EN DRVH BST GND<1> GND<0> E61392-006

HEAT SINK REQUIRED ON FETS

CAD NOTE: PLACE CAPS ON TOP, CLOSE TO FET DRAIN

FET DATA

TOP	E75239-001	CSD16322Q5C
BOT	E75262-001	CSD16325Q5C

ROOM DDR3_CPU3_VDDQ_VR

KELVIN CONNECTION REQUIRED AT INDUCTOR PINS

200NH CHOKE 4PIN D74881-001 L4A1

PLACE NEAR DIMM POWER PINS

OUTPUT VOLTAGE REMOTE SENSE

INPUT FILTER

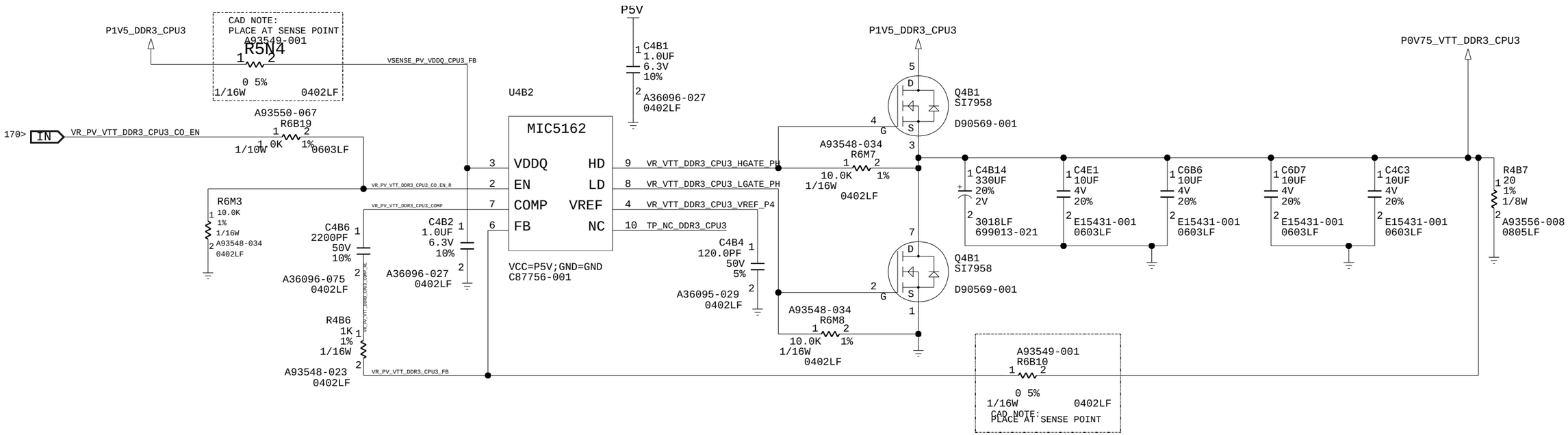
Wed Oct 27 15:22:04 2010

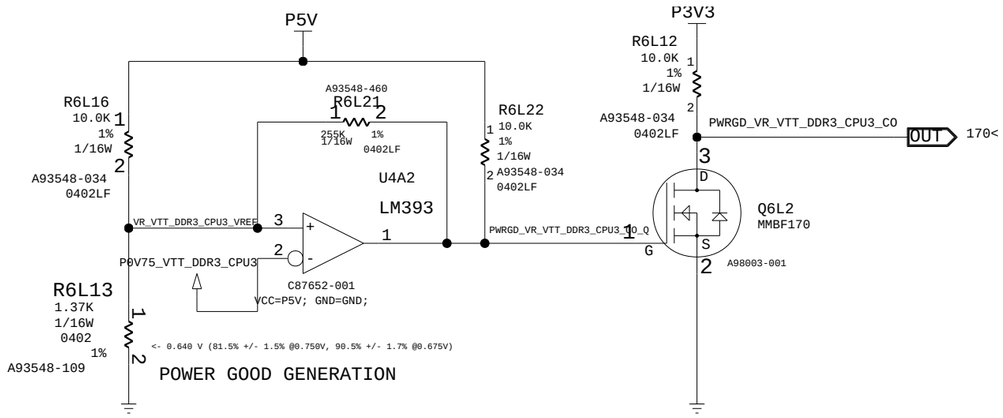
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 263 OF 303	

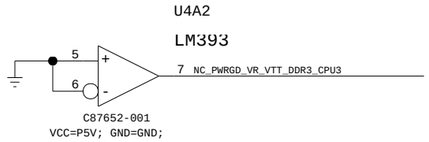
INTEL CONFIDENTIAL

ROOM

VTT_DDR3_CPU3_VR







VR SPECIFICATION
VOUT=1/2 VDDQ
DC & AC TOL. = 1/2VDDQ +/- 39MV
IOUT=+/-2.9A PEAK
IOUT=+/-2.5A TDC
IOUT STEP=0.8A
STEP DI/DT=1A/US
MINIMUM AIR FLOW=551LFM

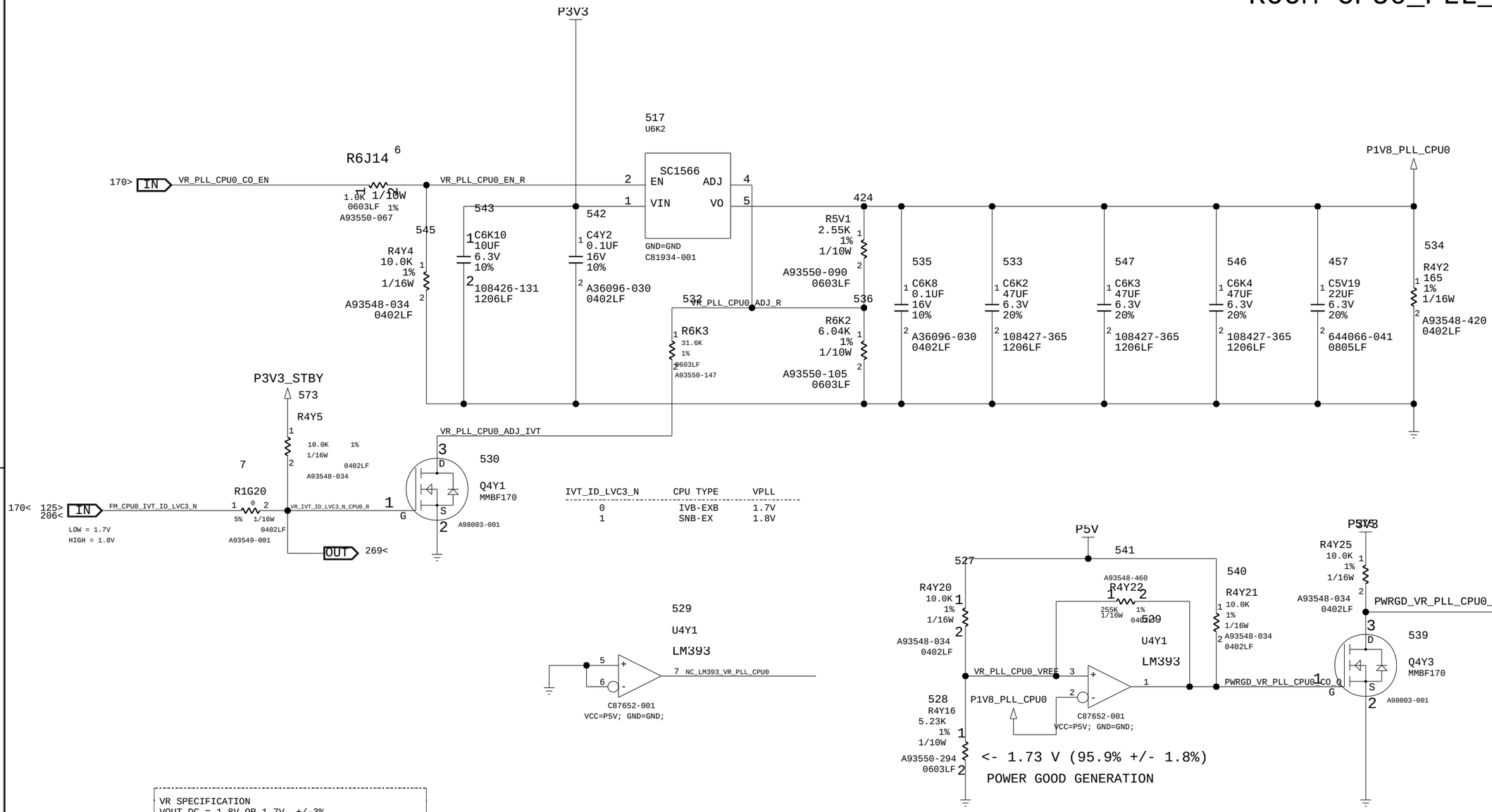
Wed Oct 27 15:22:04 2010

CPU3 DDR3 VTT

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 264 OF 303	

INTEL CONFIDENTIAL

ROOM CPU0_PLL_VR



VR SPECIFICATION
VOUT DC = 1.8V OR 1.7V, +/-3%
VOUT AC = 1.8V OR 1.7V, +/-1.5%
IOUT = 2A PEAK
IOUT = 2A TDC
IOUT STEP SIZE = 100MA
IOUT DI/DT = 100MA/US
MINIMUM AIR FLOW = 551 LFM

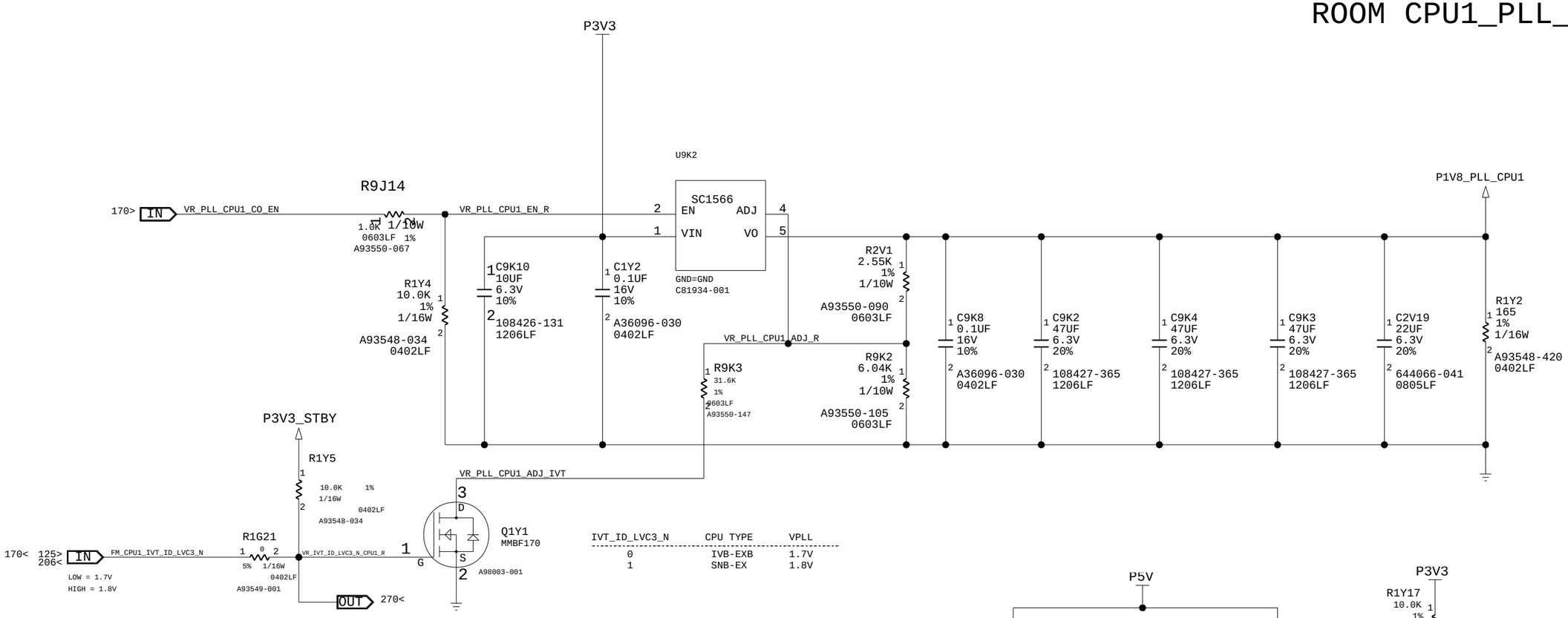
Wed Oct 27 15:22:05 2010

1.8V CPU0 PLL

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359 15	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 265 OF 303	

INTEL CONFIDENTIAL

ROOM CPU1_PLL_VR



VR SPECIFICATION
VOUT DC = 1.8V OR 1.7V, +/-3%
VOUT AC = 1.8V OR 1.7V, +/-1.5%
IOUT = 2A PEAK
IOUT = 2A TDC
IOUT STEP SIZE = 100MA
IOUT DI/DT = 100MA/US
MINIMUM AIR FLOW = 551 LFM

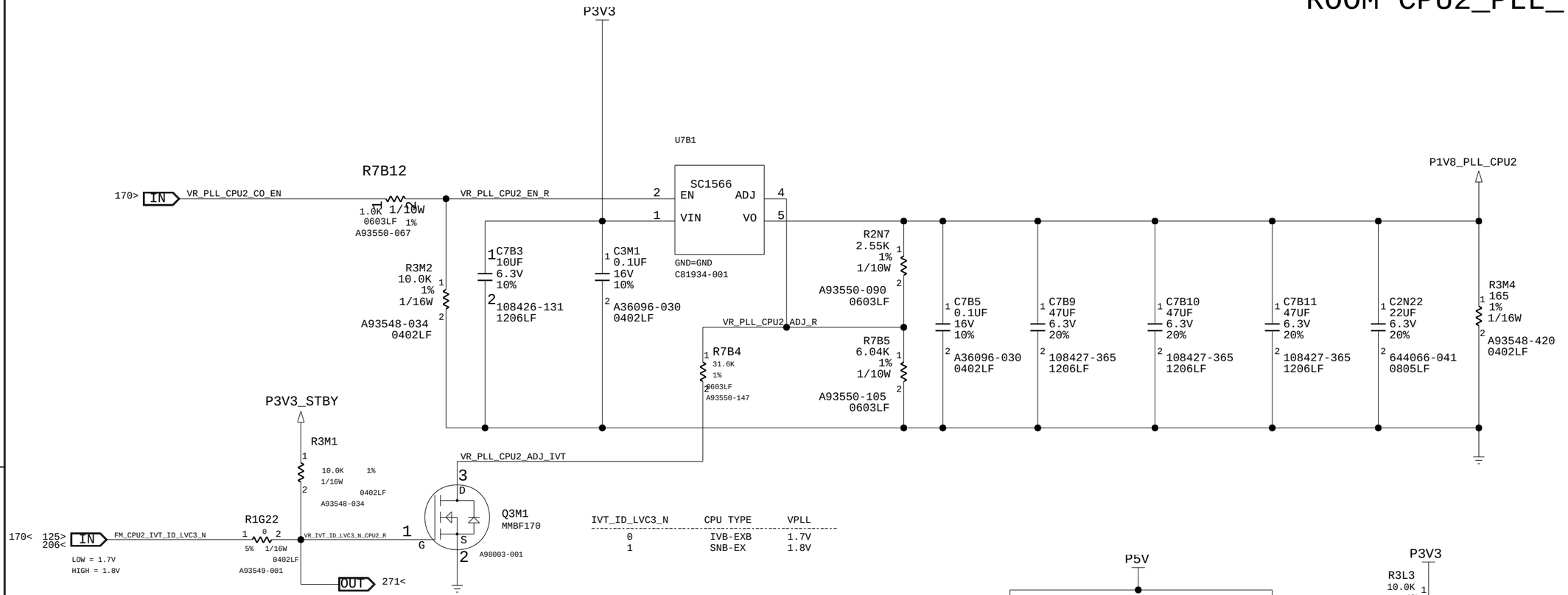
Wed Oct 27 15:22:05 2010

1.8V CPU1 PLL

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 266 OF 303

INTEL CONFIDENTIAL

ROOM CPU2_PLL_VR



VR SPECIFICATION
VOUT DC = 1.8V OR 1.7V, +/-3%
VOUT AC = 1.8V OR 1.7V, +/-1.5%
IOUT = 2A PEAK
IOUT = 2A TDC
IOUT STEP SIZE = 100MA
IOUT DI/DT = 100MA/US
MINIMUM AIR FLOW = 551 LFM

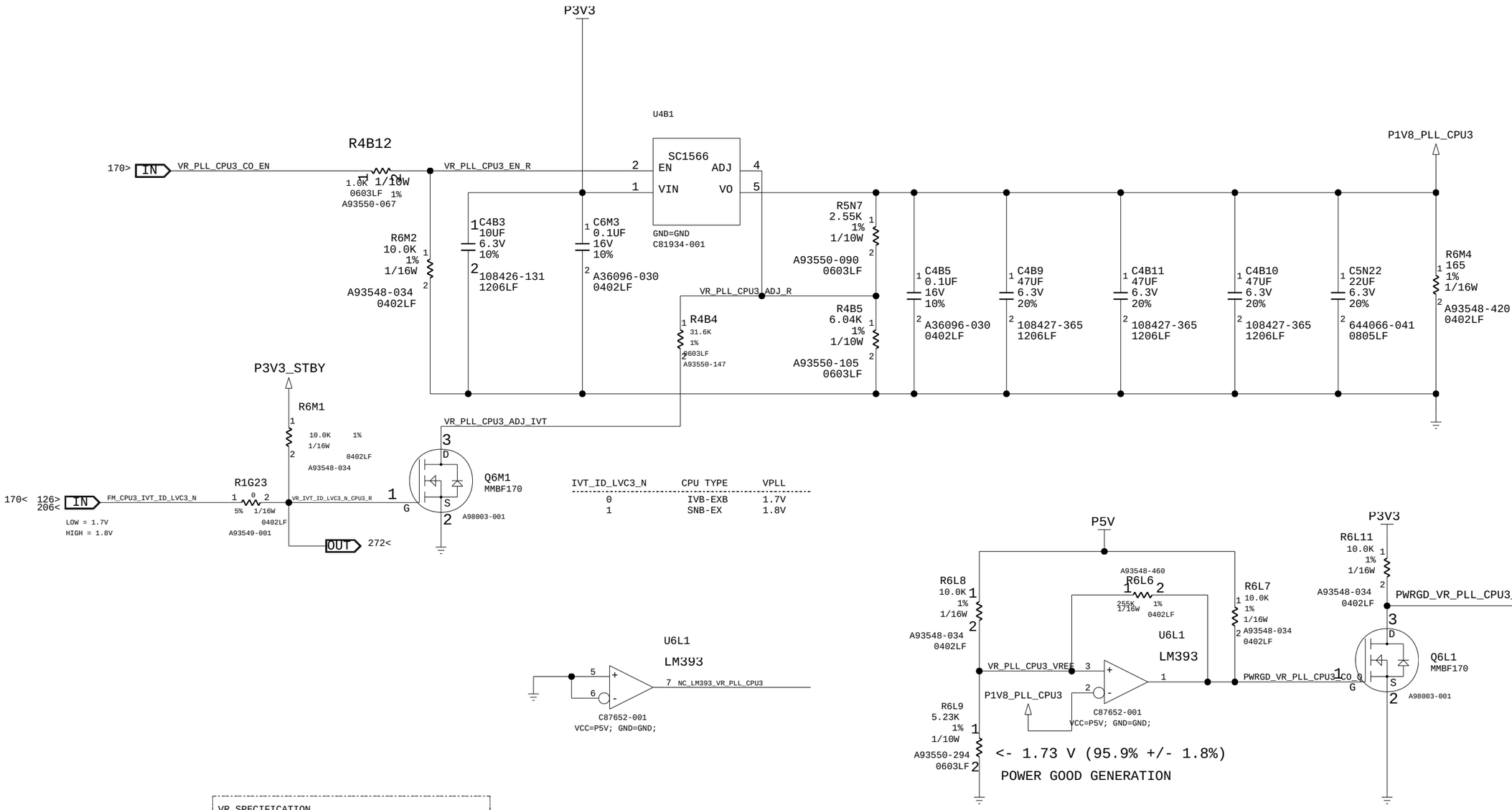
Wed Oct 27 15:22:05 2010

1.8V CPU2 PLL

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 267 OF 303	

INTEL CONFIDENTIAL

ROOM CPU3_PLL_VR



VR SPECIFICATION
VOUT DC = 1.8V OR 1.7V, +/-3%
VOUT AC = 1.8V OR 1.7V, +/-1.5%
IOUT = 2A PEAK
IOUT = 2A TDC
IOUT STEP SIZE = 100MA
IOUT DI/DT = 100MA/US
MINIMUM AIR FLOW = 551 LFM

Wed Oct 27 15:22:05 2010

1.8V CPU3 PLL

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 268 OF 303	

INTEL CONFIDENTIAL

CPU0 VTT

ISL6314

VR SPECIFICATION
VOUT DC = 1.05V OR 1.0V, +/-0.6%
VOUT AC = +/-3.2%
RIPPLE = +/-0.5%
IOUT = 24A PEAK
IOUT = 20A TDC
IOUT STEP = 14A
IOUT DI/DT = 20A/US
FREQ = 700 KHZ
LOAD LINE = 0 MILLIOHMS
MINIMUM AIR FLOW = 157.5 LFM

IVT_ID_LVC3_N	CPU TYPE	VTT
0	IVB-EXB	1.00V (1X010110)
1	SNB-EX	1.05V (1X010100)

FET DATA			GATE DRIVE VOLTAGE
TOP	E75239-001	CSD16322Q5C	5V
BOT	E75262-001	CSD16325Q5C	5V

ROOM CPU0_VTT_VR

Wed Oct 27 15:22:05 2010

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 269 OF 303	

INTEL CONFIDENTIAL

CPU1 VTT

ROOM CPU1_VTT_VR

ISL6314

VCC	19	PVCC	
PGOOD	1	LGATE	21
QFS	5	BOOT	22
SS	2	UGATE	23
FS	3	PHASE	24
VID7	32	VSEN	12
VID6	25	VDIFF	10
VID5	26	COMP	7
VID4	27	RCOMP	8
VID3	28	FB	9
VID2	29	APA	6
VID1	30	NC	20
VID0	31		
REF	4		
EN	17	RGND	11
ISENN	15	TH	33
ISENP	16	OCSET	13
		ISENO	14

VR SPECIFICATION
VOUT DC = 1.05V OR 1.0V, +/-0.6%
VOUT AC = +/-3.2%
RIPPLE = +/-0.5%
IOUT = 24A PEAK
IOUT = 20A TDC
IOUT STEP = 8.6A
IOUT DI/DT = 8.2A/US
FREQ = 500 KHZ
LOAD LINE = 0 MILLIOHMS
MINIMUM AIR FLOW = 157.5 LFM

IVT_ID_LVC3_N	CPU TYPE	VTT
0	IVB-EXB	1.00V (1X010110)
1	SNB-EX	1.05V (1X010100)

FET DATA / GATE DRIVE VOLTAGE

TOP	E75239-001	CSD16322Q5C	5V
BOT	E75262-001	CSD16325Q5C	5V

CAD INSTRUCTION FOR ALL DIFFERENTIAL PAIR ROUTING IN THIS PAGE:
ROUTE AS DIFF PAIR 10MILS WIDTH,5MIL SPACING

CAD NOTE: PLACE IN A ROW

CAD NOTE:PLACE RESISTORS AT INDUCTOR PADS

CAD NOTE:PLACE NEAR CONTROLLER

CAD NOTE:PLACE NEAR PROCESSOR SOCKET

Wed Oct 27 15:22:06 2010

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 270 OF 303	

INTEL CONFIDENTIAL

CPU2 VTT

ISL6314

VR SPECIFICATION
VOUT DC = 1.05V OR 1.0V, +/-0.6%
VOUT AC = +/-3.2%
RIPPLE = +/-0.5%
IOUT = 24A PEAK
IOUT = 20A TDC
IOUT STEP = 8.6A
IOUT DI/DT = 8.2A/US
FREQ = 500 KHZ
LOAD LINE = 0 MILLIOHMS
MINIMUM AIR FLOW = 157.5 LFM

IVT_ID_LVC3_N	CPU TYPE	VTT
0	IVB-EXB	1.00V (1X010110)
1	SNB-EX	1.05V (1X010100)

FET DATA		GATE DRIVE VOLTAGE
TOP	E75239-001	CSD16322Q5C 5V
BOT	E75262-001	CSD16325Q5C 5V

CAD INSTRUCTION FOR ALL DIFFERENTIAL PAIR ROUTING IN THIS PAGE:
ROUTE AS DIFF PAIR 10MILS WIDTH,5MIL SPACING

CAD NOTE: PLACE IN A ROW

CAD NOTE:PLACE NEAR CONTROLLER

CAD NOTE:PLACE RESISTORS AT INDUCTOR PADS

CAD NOTE:PLACE NEAR PROCESSOR SOCKET

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INTEL CONFIDENTIAL

CPU3 VTT

ISL6314

VR SPECIFICATION
VOUT DC = 1.05V OR 1.0V, +/-0.6%
VOUT AC = +/-3.2%
RIPPLE = +/-0.5%
IOUT = 24A PEAK
IOUT = 20A TDC
IOUT STEP = 8.6A
IOUT DI/DT = 8.2A/US
FREQ = 500 KHZ
LOAD LINE = 0 MILLIOHMS
MINIMUM AIR FLOW = 157.5 LFM

IVT_ID_LVC3_N	CPU TYPE	VTT
0	IVB-EXB	1.00V (1X010110)
1	SNB-EX	1.05V (1X010100)

FET DATA			GATE DRIVE VOLTAGE
TOP	E75239-001	CSD16322Q5C	5V
BOT	E75262-001	CSD16325Q5C	5V

CAD INSTRUCTION FOR ALL DIFFERENTIAL PAIR ROUTING IN THIS PAGE:
ROUTE AS DIFF PAIR 10MILS WIDTH,5MIL SPACING

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VR SPECIFICATION
VOUT DC = 1.1V, +/-2%
VOUT AC = 1.1V, +/-2%
RIPPLE = +/-1%
IOUT = 2.7A PEAK
IOUT = 2A TDC
IOUT STEP SIZE = 0.7A
IOUT DI/DT = 13A/US
FREQ = 500KHZ
MINIMUM AIR FLOW = 157.5 LFM

P5V_STBY

R8U34 2.20 5% 1/16W A93549-051 0402LF

SPOF CR2G1 BAT54LT1 C83455-001 SOT23LF

C2G17 644066-032 22UF 20% 16V 1210LF

C2G13 644066-032 22UF 20% 16V 1210LF

VR_P1V1_STBY_VCC

VR_P1V1_STBY_SS_BAT_C

C92211-001 U2G1 SC2612 VCC COMP FB DL SS_EN DH BST GND

SPOF C2G8 0.1UF 16V 10% 602433-056 0603LF

EU2G2

FET DATA E58781-001 IRFH7911TRPBF

R8V4 A93548-034 10.0K 1% 1/16W 0402LF

Q2H1 MMBT3904 SMLF C52245-001

VR_P1V1_STBY_CO_EN_N 169> IN A93552-004 R2H2 0 5% 1/10W 0603LF

VR_P1V1_STBY_SS

C8U12 1.0UF 6.3V 10% A36096-027 0402LF

C2G18 1.0UF 10% 16V 603269-067 0603LF

AGND_P1V1_STBY

VR_P1V1_STBY_LGATE_PH

VR_P1V1_STBY_HGATE_PH

A93549-001 R8U30 0 5% 1/16W 0402LF VR_P1V1_STBY_HGATE_PH_R

R8U32 10.0K 1% 1/16W A93548-034 0402LF

VR_P1V1_STBY_PHASE

A93549-001 R8U31 0 5% 1/16W 0402LF VR_P1V1_STBY_LGATE_PH_R

R8U33 10.0K 1% 1/16W A93548-034 0402LF

E58781-001

E19636-002 L2G1 SMLF 2.20UH

R2G49 2.2 5% 1/8W A93555-133 0805LF

VR_P1V1_STBY_SWN

P1V1_STBY_PBG

C8U10 699013-021 330UF 20% 2V 3018LF

C2G7 644066-041 22UF 20% 6.3V 0805LF

R8U28 A93555-033 220 5% 1/8W 0805LF

VR_P1V1_STBY_FB

VR_P1V1_STBY_COMP

A36096-019 C2G21 0.033UF 10% 16V 0402LF

VR_P1V1_STBY_COMP_RC

A93548-132 R2G48 15K 1% 1/16W 0402LF

A36094-026 C2G22 3.3PF 50V 0402LF 0.25PF

A36096-075 C2H1 2200PF 50V 10% 0402LF

VR_P1V1_STBY_FB_RC

A93548-503 R2G50 33 1% 1/16W 0402LF

C2G19 1000PF 50V 10% A36096-046 0402LF

A93549-001 R1G9 0 5% 1/16W 0402LF

A93550-090 R2H1 2.55K 1% 1/10W 0603LF

VR_P1V1_STBY_FB_R2

A93550-001 10 1% 0603LF R1G2

SPOF CAD NOTE: PLACE AT LOAD

R8U35 6.81K 1% 1/16W A93548-451 0402LF

A93552-004 R8U36 0 5% 1/10W 0603LF

AGND_P1V1_STBY

P3V3_STBY

C8V1 644066-041 22UF 20% 6.3V 0805LF

P5V_STBY

R8V5 10.0K 1% 1/16W A93548-034 0402LF

A93548-460 R8V2 255K 1% 1/16W 0402LF

R8V1 10.0K 1% 1/16W A93548-034 0402LF

R8V3 10.0K 1% 1/16W A93548-034 0402LF

U2H1 LM393

VR_P1V1_STBY_VREF

P1V1_STBY_PBG

C87652-001 VCC=P5V_STBY; GND=GND;

R8V6 2.61K 1% 1/10W A93550-091 0603LF

<- 1.05 V (95.1% +/- 1.8%)

POWER GOOD GENERATION

PWRGD_VR_P1V1_STBY_CO

PWRGD_VR_P1V1_STBY_CO_Q

169< OUT

Q2G3 MMBF170 A98003-001

CAD NOTE: PLACE NEAR PIN 8 OF LM393

P5V_STBY C2G20 0.1UF 16V 10% A36096-030 0402LF

PATSBURG 1.1V STBY VR

ROOM = PBG_P1V1_STBY_VR

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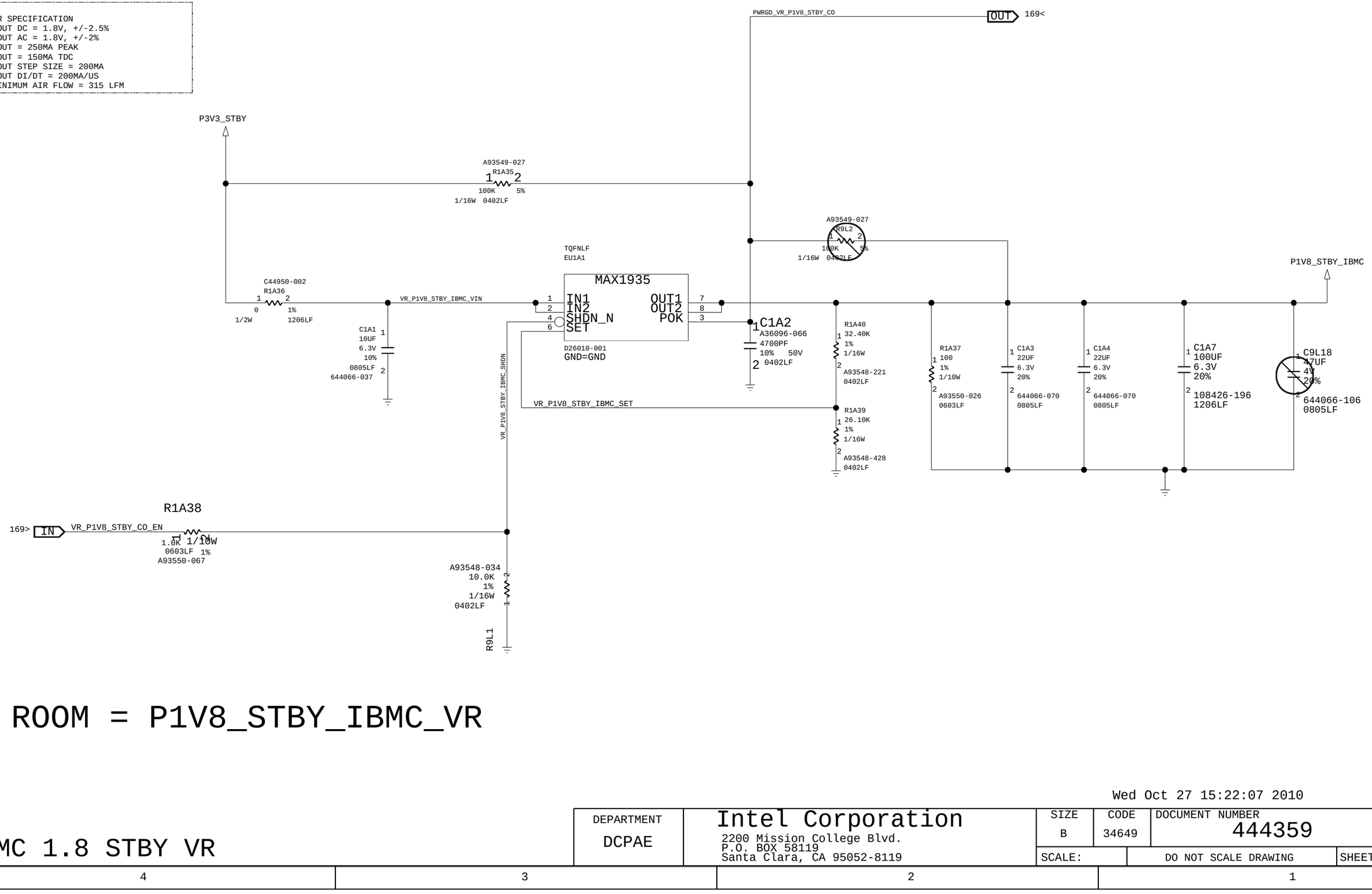
VR SPECIFICATION
VOUT DC = 1.8V, +/-2.5%
VOUT AC = 1.8V, +/-2%
IOUT = 250MA PEAK
IOUT = 150MA TDC
IOUT STEP SIZE = 200MA
IOUT DI/DT = 200MA/US
MINIMUM AIR FLOW = 315 LFM



ROOM = P1V8_STBY_IBMC_VR

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IBMC 1.8 STBY VR

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
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		SCALE:	DO NOT SCALE DRAWING	SHEET 275 OF 303	

INTEL CONFIDENTIAL

VR SPECIFICATION
VOUT DC = 1.1V, +/-1.2%
VOUT AC = 1.1V, +/-2.8%
RIPPLE = +/-0.5%
IOUT = 8.3A PEAK
IOUT = 5A TDC
IOUT STEP SIZE = 8A
IOUT DI/DT = 20A/US
FREQ = 500KHZ
MINIMUM AIR FLOW = 157.5LFM

P5V

R9U21 2.20 5% 1/16W A93549-051 0402LF

SPOF CR1G1 BAT54LT1 C83455-001 SOT23LF

C1G8 644066-032 22UF 20% 16V 1210LF

C1G9 644066-032 22UF 20% 16V 1210LF

C1G10 644066-032 22UF 20% 16V 1210LF

VR_P1V1_MAIN_VCC

VR_P1V1_MAIN_SS_BST_C

C92211-001 U1G1

SC2612
VCC COMP
FB DL
SS_EN DH
BST GND

SPOF C1G5 0.1UF 16V 10% 602433-056 0603LF

P3V3_STBY

R9U25 A93548-034 10.0K 1% 1/16W 0402LF

VR_P1V1_MAIN_CO_EN_N 169> IN A93552-004 R1H5 0 5% 1/10W 0603LF

Q1G4 MMBT3904 SMLF C52245-001

VR_P1V1_MAIN_SS

C9U4 1.0UF 6.3V 10% A36096-027 0402LF

C1G11 1.0UF 16V 10% 603269-067 0603LF

AGND_P1V1_MAIN

VR_P1V1_MAIN_LGATE_PH

VR_P1V1_MAIN_HGATE_PH

A93549-001 R9U17 0 5% 1/16W 0402LF

VR_P1V1_MAIN_HGATE_PH_R

R9U19 10.0K 1% 1/16W A93548-034 0402LF

EU1G1

D G S

E58781-001

FET DATA
E58781-001 IRFH7911TRPBF

VR_P1V1_MAIN_PHASE

A93549-001 R9U18 0 5% 1/16W 0402LF

VR_P1V1_MAIN_LGATE_PH_R

R9U20 10.0K 1% 1/16W A93548-034 0402LF

NC

E13358-003 L1G1 1.00UH SM

R1G17 2.2 5% 1/8W A93555-133 0805LF

VR_P1V1_MAIN_SNUBBER

C1G12 1000PF 50V 10% A36096-046 0402LF

P1V1_MAIN_PBG

C1G1 699013-021 330UF 20% 2V 3018LF

C1G2 699013-021 330UF 20% 2V 3018LF

R9U16 A93555-033 220 5% 1/8W 0805LF

C9U3 644066-041 22UF 20% 6.3V 0805LF

VR_P1V1_MAIN_FB

VR_P1V1_MAIN_COMP

A36096-045 C1G13 0.01UF 25V 10% 0402LF

VR_P1V1_MAIN_COMP_RC

A93548-181 R1G16 20K 1% 1/16W 0402LF

A36094-026 C1G14 3.3PF 0.25PF 50V 0402LF

A36096-075 C1G15 2200PF 50V 10% 0402LF

VR_P1V1_MAIN_FB_RC

A93548-503 R1G18 33 1% 1/16W 0402LF

A93553-090 R1G19 3.32K .1% 1/16W 0603LF

VR_P1V1_MAIN_FB_R2

A93549-001 R2G43 0 5% 1/16W 0402LF

A93550-001 10 1% 0603LF R2G42

SPOF
CAD NOTE: PLACE AT LOAD

A93552-004 R9U24 0 5% 1/10W 0603LF

AGND_P1V1_MAIN

R9U22 8.66K 1% 1/10W A93550-112 0603LF

AGND_P1V1_MAIN

P5V_STBY

P3V3

R8V10 10.0K 1% 1/16W A93548-034 0402LF

A93548-460 R8V9 255K 1% 1/16W 0402LF

R8V8 10.0K 1% 1/16W A93548-034 0402LF

U2H1 LM393

VR_P1V1_MAIN_VREF

P1V1_MAIN_PBG

C87652-001
VCC=P5V_STBY; GND=GND;

R8V12 2.61K 1% 1/10W A93550-091 0603LF

<- 1.05 V (95.1% +/- 1.8%)

POWER GOOD GENERATION

R9U23 10.0K 1% 1/16W

A93548-034 0402LF

PWRGD_VR_P1V1_MAIN_CO

OUT 169<

PWRGD_VR_P1V1_MAIN_CO_Q

Q2H2 MMBF170 A98003-001

ROOM = PBG_P1V1_MAIN_VR

PATSBURG 1.1V MAIN VR

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PATSBURG VR BLANK PAGE

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		SCALE:	DO NOT SCALE DRAWING	SHEET 277 OF 303	

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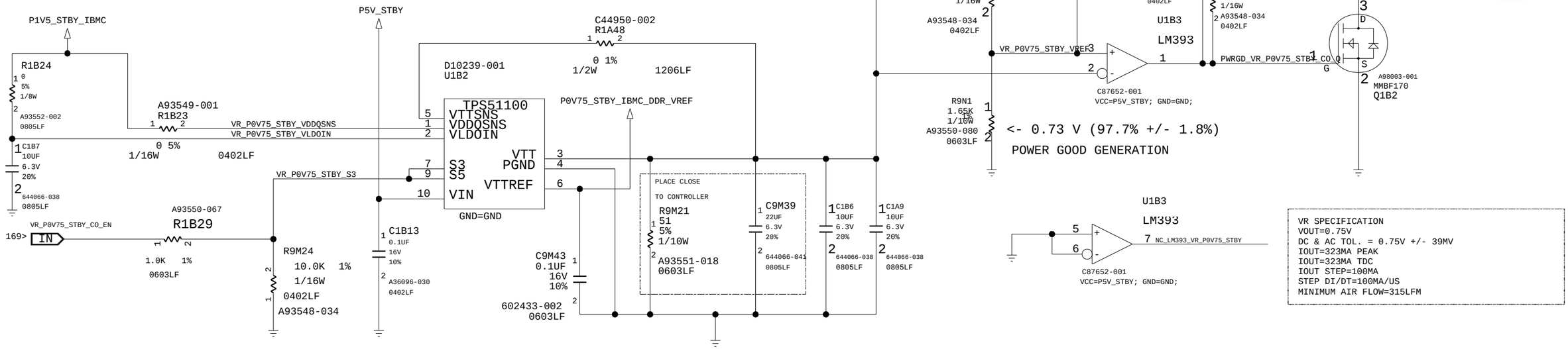
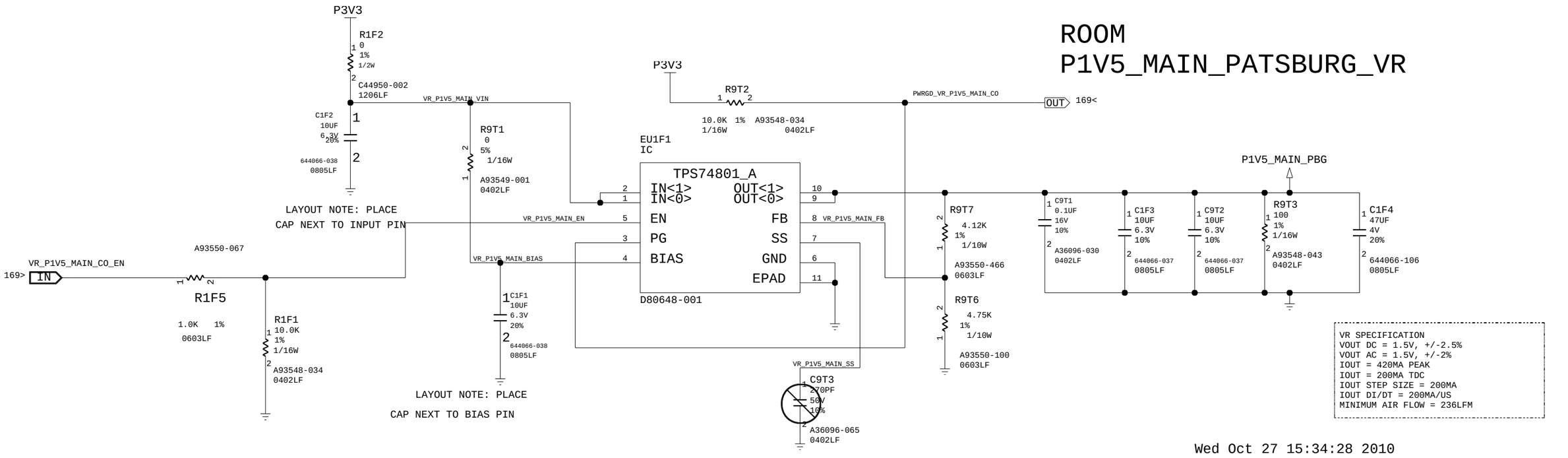
ROOM
P0V75_STBY_IBMC_VR



ROOM
P1V5_MAIN_PATSBURG_VR



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IBMC 0V75 AND PBG 1V5 VR

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ROOM = P3V3_STBY_VR

VR SPECIFICATION
VOUT DC = 3.3V, +/-2%
VOUT AC = 3.3V, +/-1.5%
RIPPLE = +/-1%
IOUT = 4A PEAK
IOUT = 3.5A TDC
IOUT STEP SIZE = 1A
IOUT DI/DT = 1A/US
FREQ = 500KHZ
MINIMUM AIR FLOW = 236LFM

P5V_STBY

C2E2 644066-032 22UF 20% 16V 1210LF

C2E1 644066-032 22UF 20% 16V 1210LF

P3V3_STBY

C1D13 470UF 20% 6.3V EMPTY RDLLF 628955-070

R8R4 2.20 5% 1/16W A93549-051 0402LF

SPOF CR2D1 BAT54LT1 C83455-001 SOT23LF

VR_P3V3_STBY_VCC

C92211-001 U2E1 SC2612 VCC COMP FB DL SS_EN DH BST GND

SPOF C2D9 0.1UF 16V 10% 602433-056 0603LF

VR_P3V3_STBY_SS_BST_C

VR_P3V3_STBY_SS

C2E3 1.0UF 16V 10% 603269-067 0603LF

C8R1 1.0UF 6.3V 10% A36096-027 0402LF

AGND_P3V3_STBY

VR_P3V3_STBY_LGATE_PH

VR_P3V3_STBY_HGATE_PH

A93549-001 R8P24 0 5% 1/16W 0402LF

VR_P3V3_STBY_HGATE_PH_R

R8R2 10.0K 1% 1/16W A93548-034 0402LF

VR_P3V3_STBY_PHASE

EU2E1 E58781-001

FET DATA E58781-001 IRFH7911TRPBF

NC

E19636-002 L2D1 SMLF 2.20UH

R2E2 2.2 5% 1/8W A93555-133 0805LF

VR_P3V3_STBY_SW

C2E4 1000PF 50V 10% A36096-046 0402LF

C8P15 47UF 6.3V 20% 108427-365 1206LF

C8P13 47UF 6.3V 20% 108427-365 1206LF

P3V3_STBY

R8P23 A93555-045 680 5% 1/8W 0805LF

C8P16 644066-041 22UF 20% 6.3V 0805LF

C8P14 47UF 6.3V 20% 108427-365 1206LF

C2D8 47UF 6.3V 20% 108427-365 1206LF

A93549-001 R8R1 0 5% 1/16W 0402LF

VR_P3V3_STBY_LGATE_PH_R

R8R3 10.0K 1% 1/16W A93548-034 0402LF

VR_P3V3_STBY_FB

VR_P3V3_STBY_COMP

A36096-028 C2E6 0.220UF 6.3V 10% 0402LF

VR_P3V3_STBY_COMP_RC

A93548-197 R2E1 6.04K 1% 1/16W 0402LF

A93552-004 R8R6 0 5% 1/10W 0603LF

A36095-045 C2E7 220PF 5% 50V 0402LF

603269-019 C2E8 8200PF 50V 10% 0603LF

VR_P3V3_STBY_FB_RC

A93548-136 R2E4 21 1% 1/16W 0402LF

A93548-014 R2E3 1.50K 1% 1/16W 0402LF

VR_P3V3_STBY_FB_R2

R8R5 475 1% 1/16W A93548-059 0402LF

A93549-001 R2B38 0 5% 1/16W 0402LF

A93550-001 10 1% 0603LF R2B39

SPOF
CAD NOTE: PLACE AT LOAD

CAD NOTE: PLACE NEAR PIN 8 OF LM393

P5V_STBY

C2E5 0.1UF 16V 10% A36096-030 0402LF

U2E2 LM393

NC_LM393_VR_P3V3_STBY

C87652-001
VCC=P5V_STBY; GND=GND;

P5V_STBY

R8R10 10.0K 1% 1/16W A93548-034 0402LF

A93548-460 R8R8 255K 1% 1/16W 0402LF

R8R7 10.0K 1% 1/16W A93548-034 0402LF

U2E2 LM393

VR_P3V3_STBY_VREF

P3V3_STBY

C87652-001
VCC=P5V_STBY; GND=GND;

R8R11 17.4K 1% 1/10W A93550-133 0603LF

<- 3.16 V (95.7% +/- 1.8%)

POWER GOOD GENERATION

P3V3_STBY

R8R9 10.0K 1% 1/16W A93548-034 0402LF

PWRGD_VR_P3V3_STBY_CO

OUT 32< 169<

Q2E1 MMBF170 A98003-001

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3.3V STBY VR

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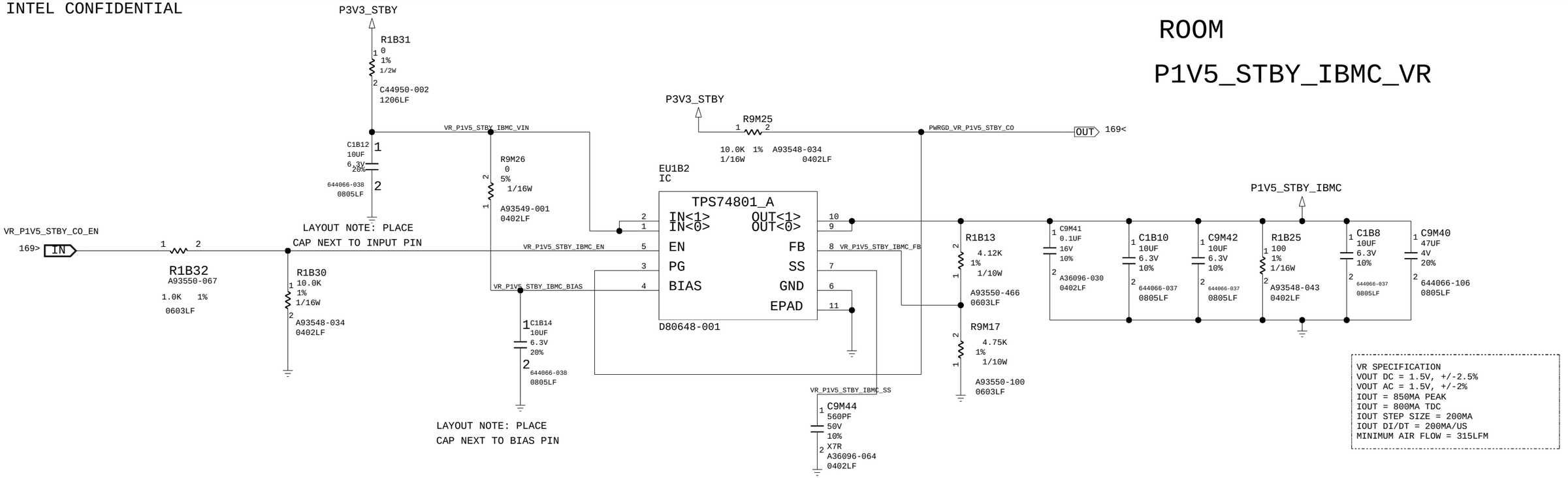
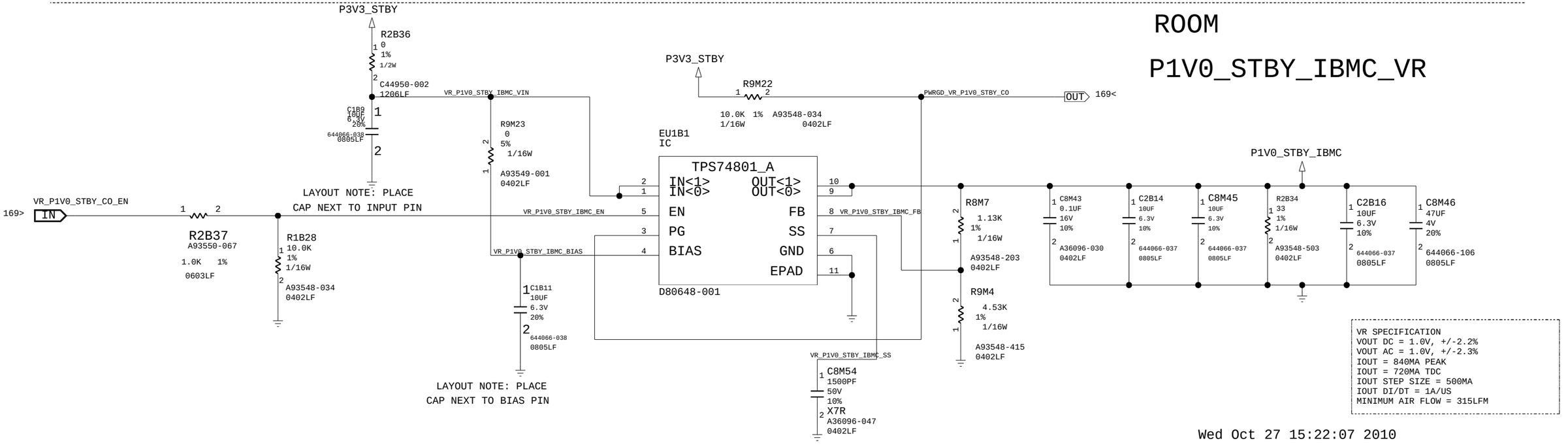
ROOM P1V5_STBY_IBMC_VR



ROOM P1V0_STBY_IBMC_VR



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IBMC 1V5 AND 1V0 STBY VR

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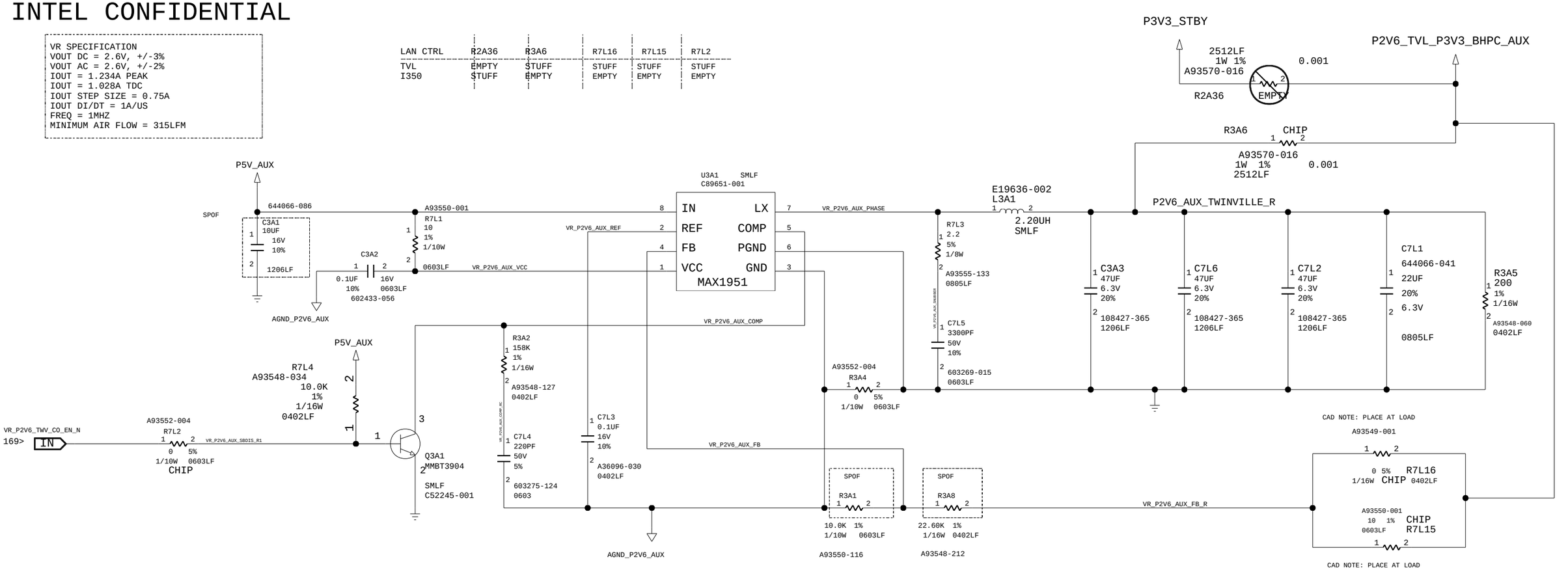
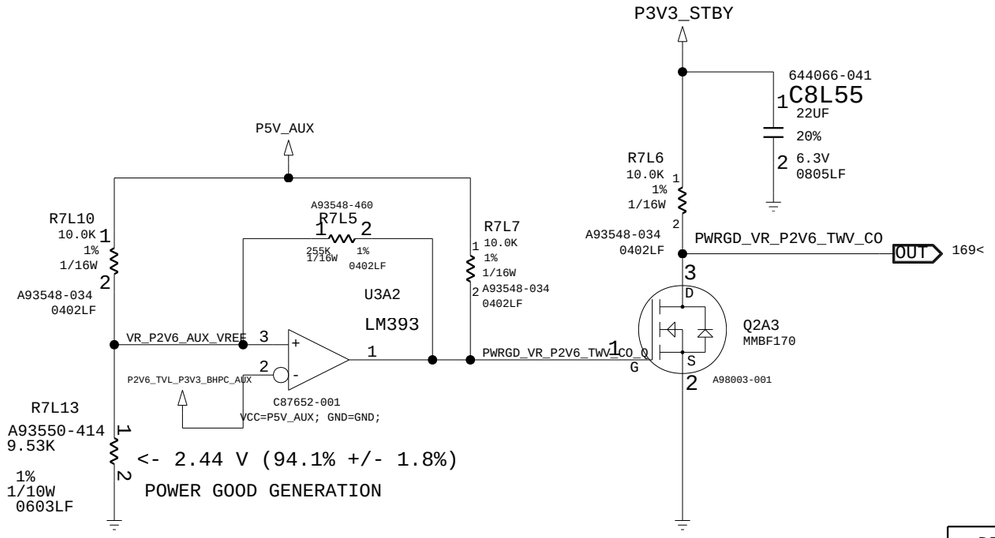
VR SPECIFICATION
VOUT DC = 2.6V, +/-3%
VOUT AC = 2.6V, +/-2%
IOUT = 1.234A PEAK
IOUT = 1.028A TDC
IOUT STEP SIZE = 0.75A
IOUT DI/DT = 1A/US
FREQ = 1MHZ
MINIMUM AIR FLOW = 315LFM

LAN CTRL	R2A36	R3A6	R7L16	R7L15	R7L2
TVL	EMPTY	STUFF	STUFF	STUFF	STUFF
I350	STUFF	EMPTY	EMPTY	EMPTY	EMPTY





ROOM = TWINVILLE_P2V6_AUX_VR

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TWINVILLE 2.6V AUX VR

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
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INTEL CONFIDENTIAL

P5V_AUX

CAD NOTE: PLACE 22UF (3) NEAR VIN PINS

C2C4 644066-032 22UF 20% 16V 1210LF

C2C13 644066-032 22UF 20% 16V 1210LF

C2C6 644066-032 22UF 20% 16V 1210LF

P3V3_STBY

R2C6 A93548-034 10.0K 1% 1/16W 0402LF

PWRGD_VR_P0V85_TWV_CO → OUT 169<

VR SPECIFICATION
VOUT DC = 0.85V, +/-2%
VOUT AC = 0.85V, +/-3%
IOUT = 7.054A PEAK
IOUT = 4.702A TDC
IOUT STEP SIZE = 4A
IOUT DI/DT = 1A/US
FREQ = 400KHZ
MINIMUM AIR FLOW = 315LFM

LAN CTRL	R2C4	R2B42	R3B12	R7M11	R2C11
TVL	EMPTY	STUFF	STUFF	STUFF	STUFF
I350	STUFF	EMPTY	EMPTY	EMPTY	EMPTY

P5V_AUX

C2C5 1.0UF 20% 6.3V 0603LF EMPTY 602433-052

R2C7 A93550-447 90.9K 1% 1/10W 0603LF

R2C9 A93548-031 10 1% 1/16W 0402LF

EU2C1

SC417

VIN<4> 35		VOUT	5
VIN<3> 11		VLDO	7 NC_VR_P0V85_AUX_VLDO
VIN<2> 10		PGOOD	26
VIN<1> 9		NC<1>	14 NC_VR_P0V85_AUX_DH
VIN<0> 6		NC<0>	12 NC_VR_P0V85_AUX_DL
V5V 3	← VR_P0V85_AUX_V5V		
TON 31	← VR_P0V85_AUX_TON	AGND<2>	34
FBL 2	← NC_VR_P0V85_AUX_FBL	AGND<1>	30
FB 1	← VR_P0V85_AUX_FB	AGND<0>	4
ENL 32			
EN_PSV 29	← VR_P0V85_AUX_EN_PSV	PGND<7>	22
BST 8	← VR_P0V85_AUX_BST	PGND<6>	21
ILIM 27	← VR_P0V85_AUX_ILIM	PGND<5>	20
		PGND<4>	19
LX<5> 33		PGND<3>	18
LX<4> 28		PGND<2>	17
LX<3> 25		PGND<1>	16
LX<2> 24		PGND<0>	15
LX<1> 23			
LX<0> 13			

E36480-001

CAD NOTE: PLACE 1000PF CLOSE TO VOUT PIN

C2C9 602431-026 1000PF 10% 50V 0603LF

P0V65_TVL_P1V0_BHPC_AUX

A93570-016 2512LF 1W 1% 0.001 R2C4 EMPTY

P0V85_TVL_P1V0_BHPC_AUX

R2B42 CHIP

A93570-016 1W 1% 0.001 2512LF

P0V85_AUX_TWINVILLE_R

AGND_P0V85_AUX

C2B27 699013-031 470UF 20% 2V SM

C2B26 699013-031 470UF 20% 2V SM

C2B28 699013-031 470UF 20% 2V SM

C8N2 644066-041 22UF 20% 6.3V 0805LF

C8N3 602433-052 1.0UF 20% 6.3V 0603LF

R8N4 A93555-027 120 5% 1/8W 0805LF

CAD NOTE: PLACE AT LOAD

A93550-001 10 1% 0603LF CHIP R3B12

VSENSE_P0V85_AUX

R2C8 10.0K 1% 1/16W 0402LF A93548-034

C2C11 560PF 50V 10% A36096-064 0402LF

A93552-004 R7M11 5% 0 0603LF CHIP 1/10W

CAD NOTE: PLACE AT LOAD

C2C8 1.0UF 6.3V 20% 602433-052 0603LF

C2C7 0.1UF 16V 10% A36096-030 0402LF

P5V_AUX

644066-041 C2C15 22UF 20% 6.3V 0805LF

R2C10 A93548-034 10.0K 1% 1/16W 0402LF

AGND_P0V85_AUX

R2C5 7.5K 1% 1/10W 0603LF A93550-230

E13358-018 L2C1 0.47UH 5M

C2C3 1UF 16V 10% 644066-061 0805LF

R8N2 A93549-001 0 5% 1/16W 0402LF

C8N1 A36096-073 0.022UF 10% 16V 0402LF EMPTY

R8N6 0 5% 1/16W 0402LF A93549-001

TWINVILLE_P0V85_AUX_VR

C2C10 0.1UF 16V 10% A36096-030 0402LF EMPTY

169> IN VR_P0V85_TWV_CO_EN_N

A93552-004 5% 0 1/10W 0603LF R2C11 CHIP

Q2C2 MMBT3904 SMLF C52245-001

P5V_AUX

AGND_P0V85_AUX

A93552-004 R8N10 0 5% 1/10W 0603LF

AGND_P0V85_AUX

CAD NOTE: PLACE CLOSE TO CONTROLLER

R8N11 14.3K 1% 1/10W 0603LF A93550-128

AGND_P0V85_AUX

CAD NOTE: PLACE EMPTY 0 OHM, 0.022UF CLOSE TO 0.47UH, BACKSIDE OK
CAD NOTE: PLACE EMPTY 0.1UF CLOSE TO FB PIN
CAD NOTE: TRACE WIDTH 25 MIL MIN.

ROOM = TWINVILLE_P0V85_AUX_VR

Wed Oct 27 15:22:08 2010

TWINVILLE 0.85V AUX VR

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 283 OF 303	

INTEL CONFIDENTIAL

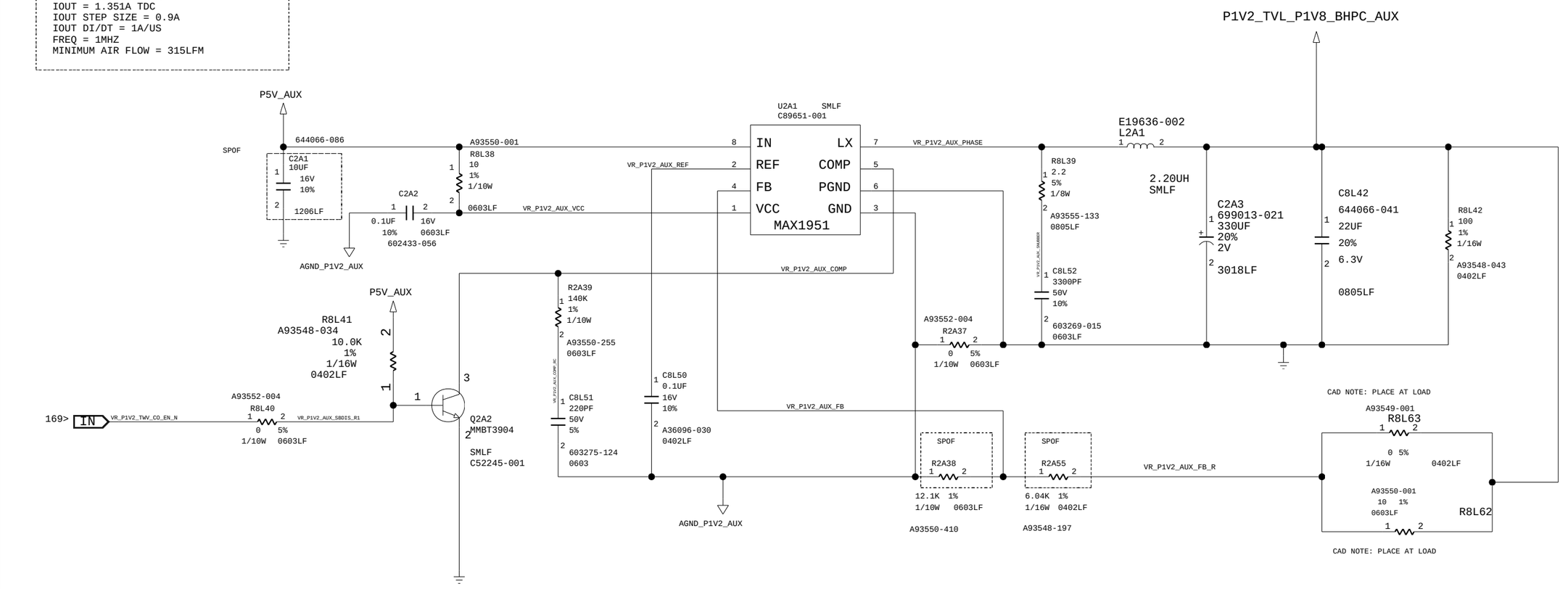
TWINVILLE VR BLANK PAGE

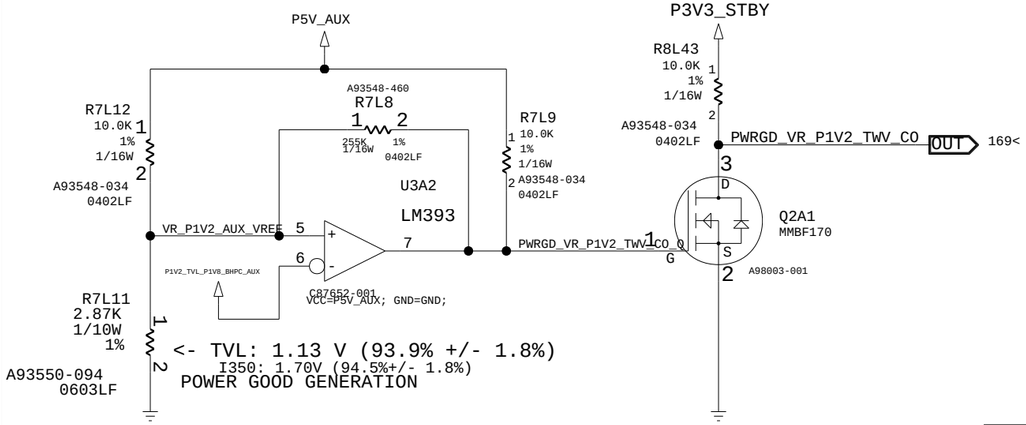
Wed Oct 27 14:54:46 2010

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 284 OF 303	

INTEL CONFIDENTIAL

VR SPECIFICATION
VOUT DC = 1.2V, +/-3%
VOUT AC = 1.2V, +/-2%
IOUT = 1.631A PEAK
IOUT = 1.351A TDC
IOUT STEP SIZE = 0.9A
IOUT DI/DT = 1A/US
FREQ = 1MHZ
MINIMUM AIR FLOW = 315LFM





LAN CTRL	R2A38	R2A55	R7L11
TVL	A93550-410	A93548-197	A93550-094
I350	A93550-116	A93548-064	A93550-214

ROOM = TWINVILLE_P1V2_AUX_VR

Wed Oct 27 15:22:08 2010

TWINVILLE 1.2V AUX VR

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 285 OF 303	

INTEL CONFIDENTIAL

VR SPECIFICATION
VOUT DC = 0.65V, +/-2%
VOUT AC = 0.65V, +/-3%
IOUT = 3.733A PEAK
IOUT = 2.871A TDC
IOUT STEP SIZE = 2.4A
IOUT DI/DT = 1A/US
FREQ = 400KHZ
MINIMUM AIR FLOW = 315LFM

P5V_AUX

CAD NOTE: PLACE 22UF (3) NEAR VIN PINS

C2C14 644066-032 22UF 20% 16V 1210LF
C2C34 644066-032 22UF 20% 16V 1210LF
C2C32 644066-032 22UF 20% 16V 1210LF

P3V3_STBY

R1C19 A93548-034 10.0K 1% 1/16W 0402LF

PWRGD_VR_P0V65_TWV_CO → OUT 169<

C1C9 1.0UF 20% 6.3V 0603LF EMPTY 602433-052

R1C23 A93548-128 100K 1% 1/16W 0402LF

R2C12 A93548-031 10 1% 1/16W 0402LF

EU2C2

SC417

VIN<4>	35	VOUT	5
VIN<3>	11	VLDO	7 NC_VR_P0V65_AUX_VLDO
VIN<2>	10	PGOOD	26
VIN<1>	9		
VIN<0>	6	NC<1>	14 NC_VR_P0V65_AUX_DH
		NC<0>	12 NC_VR_P0V65_AUX_DL
V5V	3		
TON	31	AGND<2>	34
FBL	2	AGND<1>	30
FB	1	AGND<0>	4
ENL	32		
EN_PSV	29	PGND<7>	22
BST	8	PGND<6>	21
ILIM	27	PGND<5>	20
		PGND<4>	19
LX<5>	33	PGND<3>	18
LX<4>	28	PGND<2>	17
LX<3>	25	PGND<1>	16
LX<2>	24	PGND<0>	15
LX<1>	23		
LX<0>	13		

E36480-001

VR_P0V65_AUX_V5V
VR_P0V65_AUX_TON
NC_VR_P0V65_AUX_FBL
VR_P0V65_AUX_FB
VR_P0V65_AUX_EN_PSV
VR_P0V65_AUX_BST
VR_P0V65_AUX_ILIM

CAD NOTE: PLACE 1000PF CLOSE TO VOUT PIN

C2C33 602431-026 1000PF 10% 50V 0603LF

P0V65_TVL_P1V0_BHPC_AUX

AGND_P0V65_AUX

C1C11 1.0UF 6.3V 20% 602433-052 0603LF
C1C10 0.1UF 16V 10% A36096-030 0402LF

C2C1 699013-021 330UF 20% 2V 3018LF
C2C2 699013-021 330UF 20% 2V 3018LF
C8N4 644066-041 22UF 20% 6.3V 0805LF
C8N5 602433-052 1.0UF 20% 6.3V 0603LF
R8N7 A93555-027 120 5% 1/8W 0805LF

644066-041 C1C16 22UF 20% 6.3V 0805LF

R1C27 A93548-034 10.0K 1% 1/16W 0402LF

R1C17 4.7K 1% 1/16W 0402LF A93548-517

ISENSE_P0V65_AUX_ILIM

L1C1 E13358-008 SM 0.68UH

CAD NOTE: PLACE AT LOAD
R8M42 0 5% 1/10W 0603LF A93552-004

VSENSE_P0V65_AUX

LAN CTRL	R9N19	R1C17
TVL	A93548-026	A93548-517
I350	A93548-034	A93548-024

169> IN VR_P0V65_TWV_CO_EN_N

Q1C1 MMBT3904 SMLF C52245-001

R2C13 A93552-004 0 5% 1/10W 0603LF

C2C12 1UF 16V 10% 644066-061 0805LF

R9N5 A93549-001 0 5% 1/16W 0402LF EMPTY

C9N7 A36096-073 EMPTY 0.022UF 10% 16V 0402LF

R8N9 0 5% 1/16W 0402LF A93549-001

A93550-001 0603LF 10 1% R8M40

CAD NOTE: PLACE AT LOAD

C1C12 0.1UF 16V 10% EMPTY A36096-030 0402LF

R1C24 10.0K 1% 1/16W 0402LF A93548-034

C1C13 68.0PF 50V 5% A36095-041 0402LF

AGND_P0V65_AUX

A93552-004 R8N13 0 5% 1/10W 0603LF

R9N19 33K 5% 1/16W 0402LF A93549-026

CAD NOTE: PLACE CLOSE TO CONTROLLER

CAD NOTE: PLACE EMPTY 0 OHM, 0.022UF CLOSE TO 0.68UH, BACKSIDE OK
CAD NOTE: PLACE EMPTY 0.1UF CLOSE TO FB PIN
CAD NOTE: TRACE WIDTH 25 MIL MIN.

ROOM = TWINVILLE_P0V65_AUX_VR

Wed Oct 27 15:22:08 2010

TWINVILLE 0.65V AUX VR

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 286 OF 303	

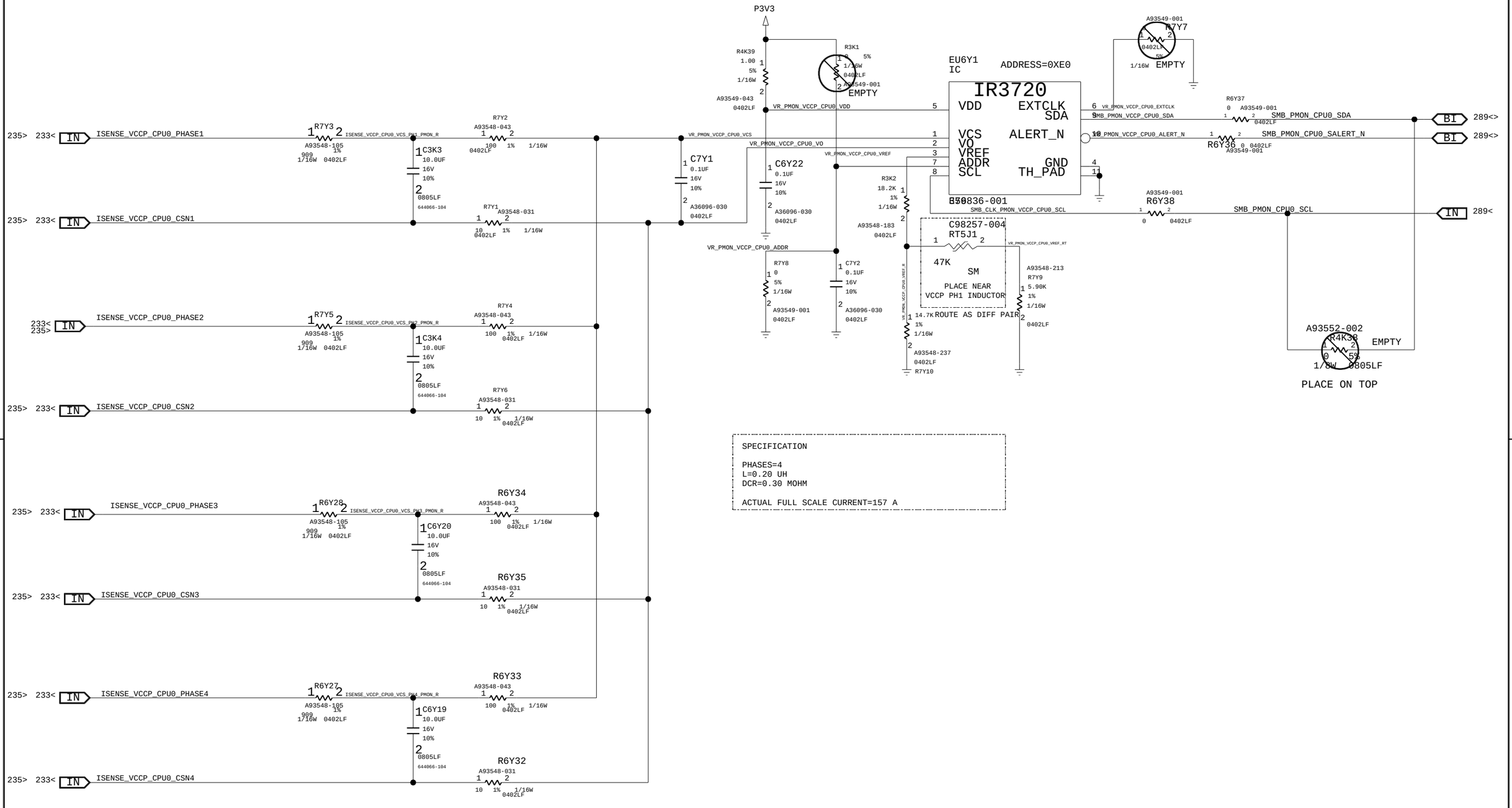
INTEL CONFIDENTIAL

TWINVILLE VR BLANK PAGE

Wed Oct 27 14:54:47 2010

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 287 OF 303	

INTEL CONFIDENTIAL



SPECIFICATION

PHASES=4
L=0.20 UH
DCR=0.30 MOHM

ACTUAL FULL SCALE CURRENT=157 A

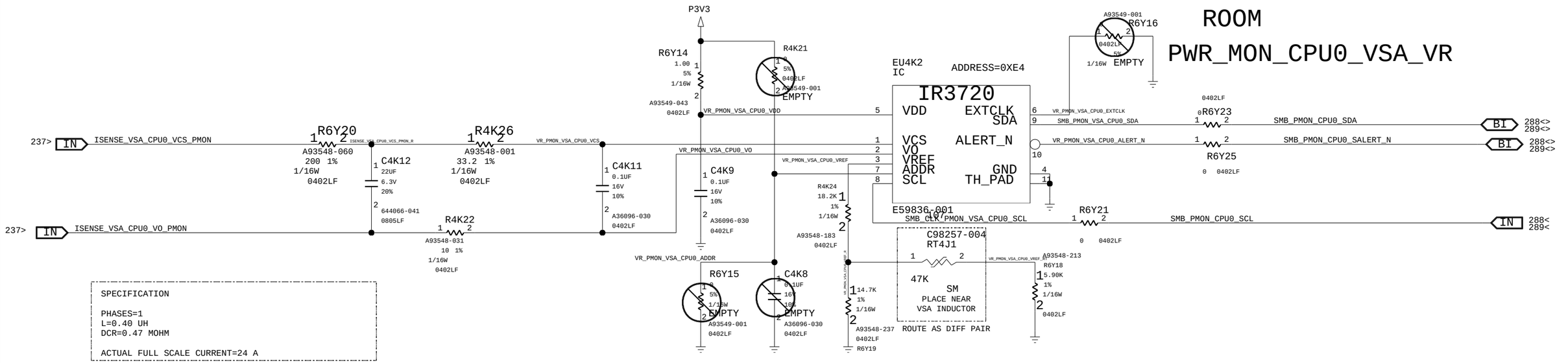
Wed Oct 27 15:22:08 2010

CPU0 VR MONITOR (1/2)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 288 OF 303	

INTEL CONFIDENTIAL

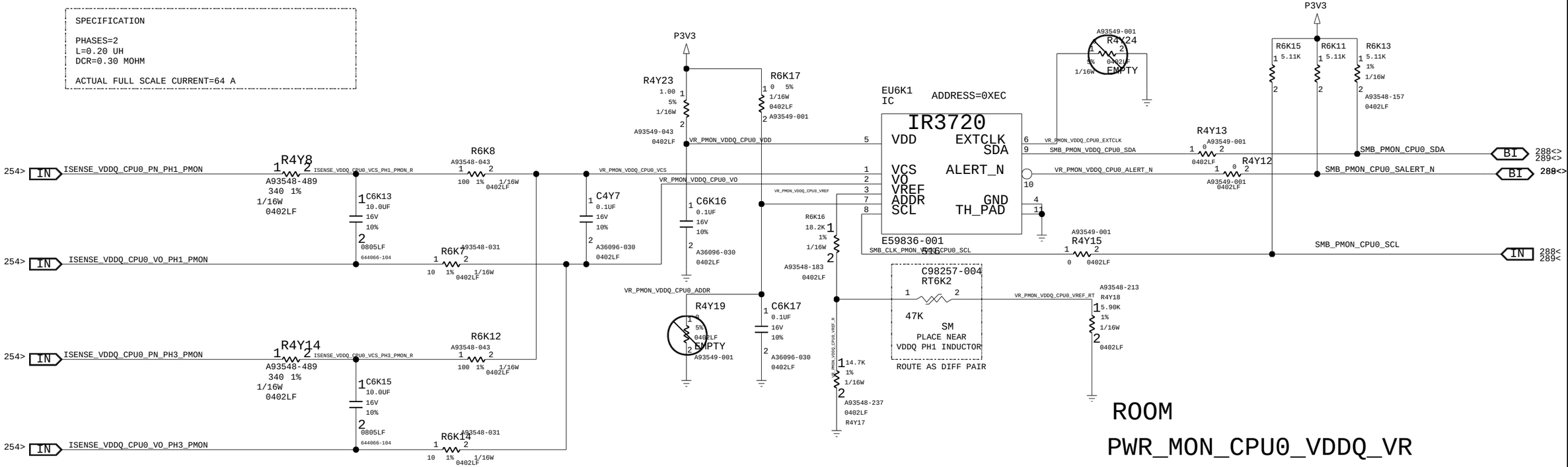
ROOM PWR_MON_CPU0_VSA_VR



SPECIFICATION

PHASES=1
L=0.40 UH
DCR=0.47 MOHM

ACTUAL FULL SCALE CURRENT=24 A



SPECIFICATION

PHASES=2
L=0.20 UH
DCR=0.30 MOHM

ACTUAL FULL SCALE CURRENT=64 A

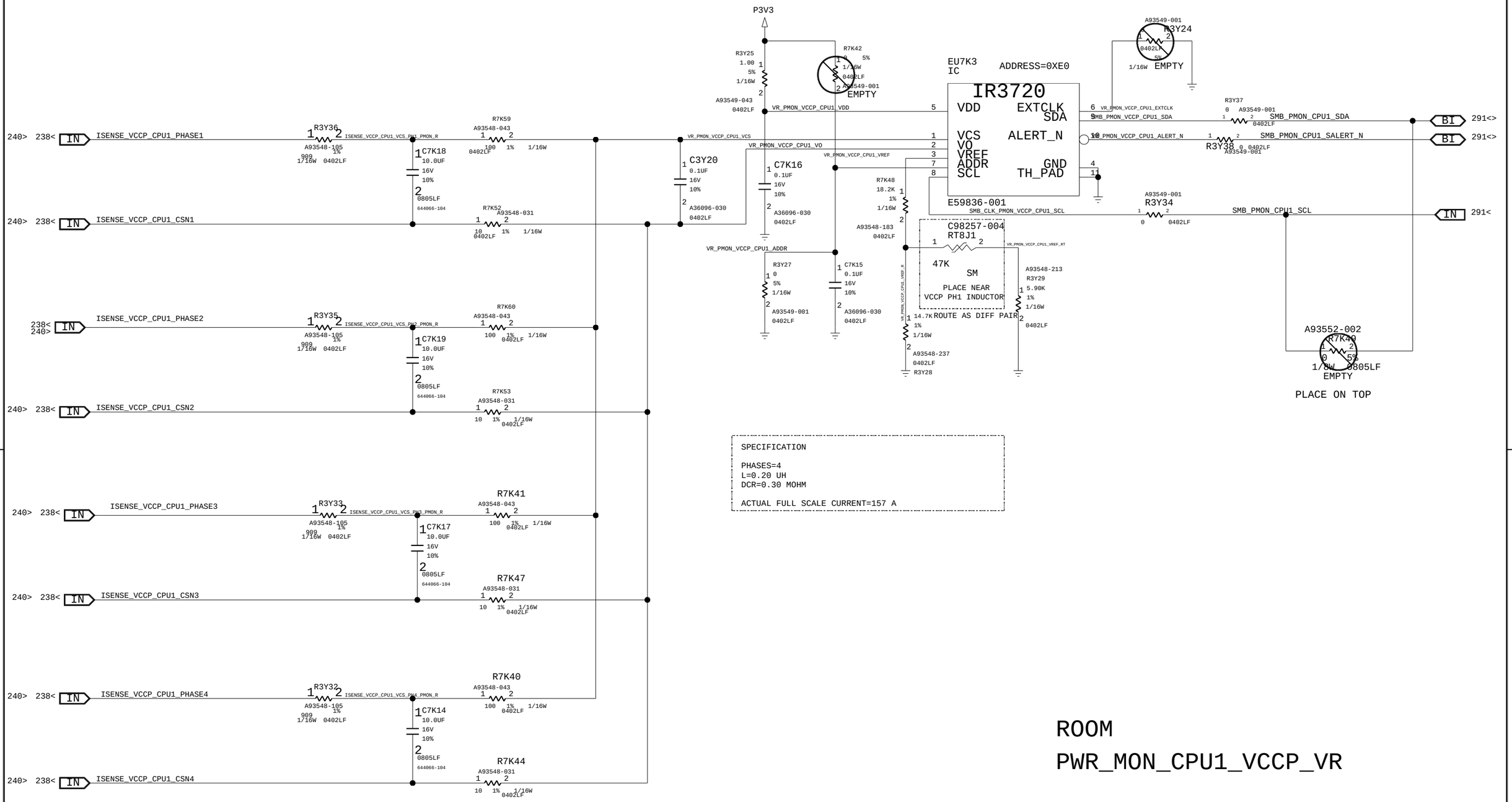
ROOM PWR_MON_CPU0_VDDQ_VR

Wed Oct 27 15:22:09 2010

CPU0 VR MONITOR (2/2)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 289 OF 303	

INTEL CONFIDENTIAL



SPECIFICATION

PHASES=4
L=0.20 UH
DCR=0.30 MOHM

ACTUAL FULL SCALE CURRENT=157 A

PLACE ON TOP

ROOM
PWR_MON_CPU1_VCCP_VR

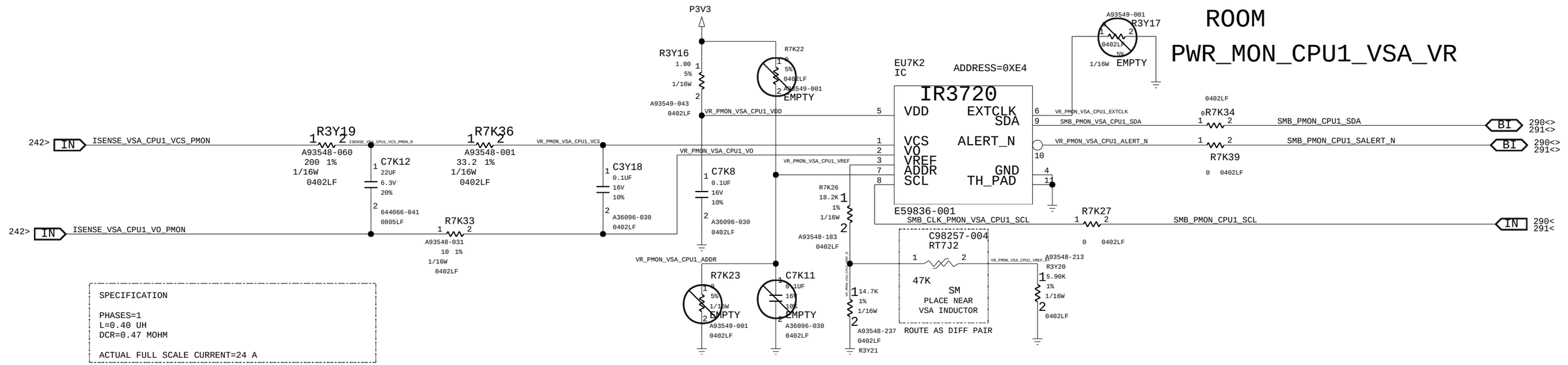
Wed Oct 27 15:22:09 2010

CPU1 VR MONITOR (1/2)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 290 OF 303	

INTEL CONFIDENTIAL

ROOM
PWR_MON_CPU1_VSA_VR



SPECIFICATION

PHASES=1
L=0.40 UH
DCR=0.47 MOHM

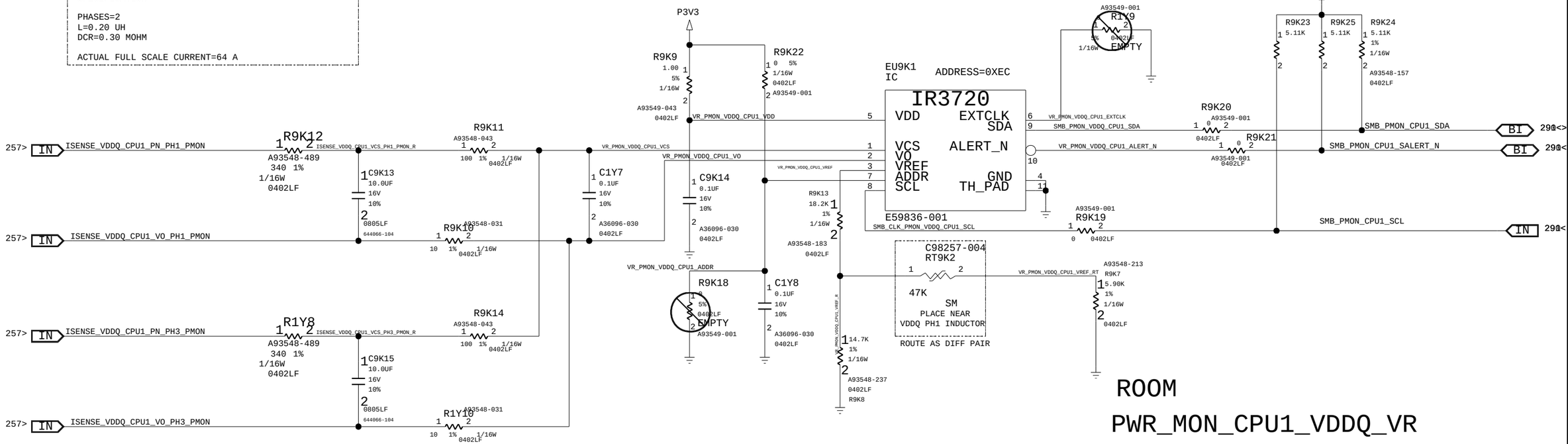
ACTUAL FULL SCALE CURRENT=24 A

SPECIFICATION

PHASES=2
L=0.20 UH
DCR=0.30 MOHM

ACTUAL FULL SCALE CURRENT=64 A

ROOM
PWR_MON_CPU1_VDDQ_VR

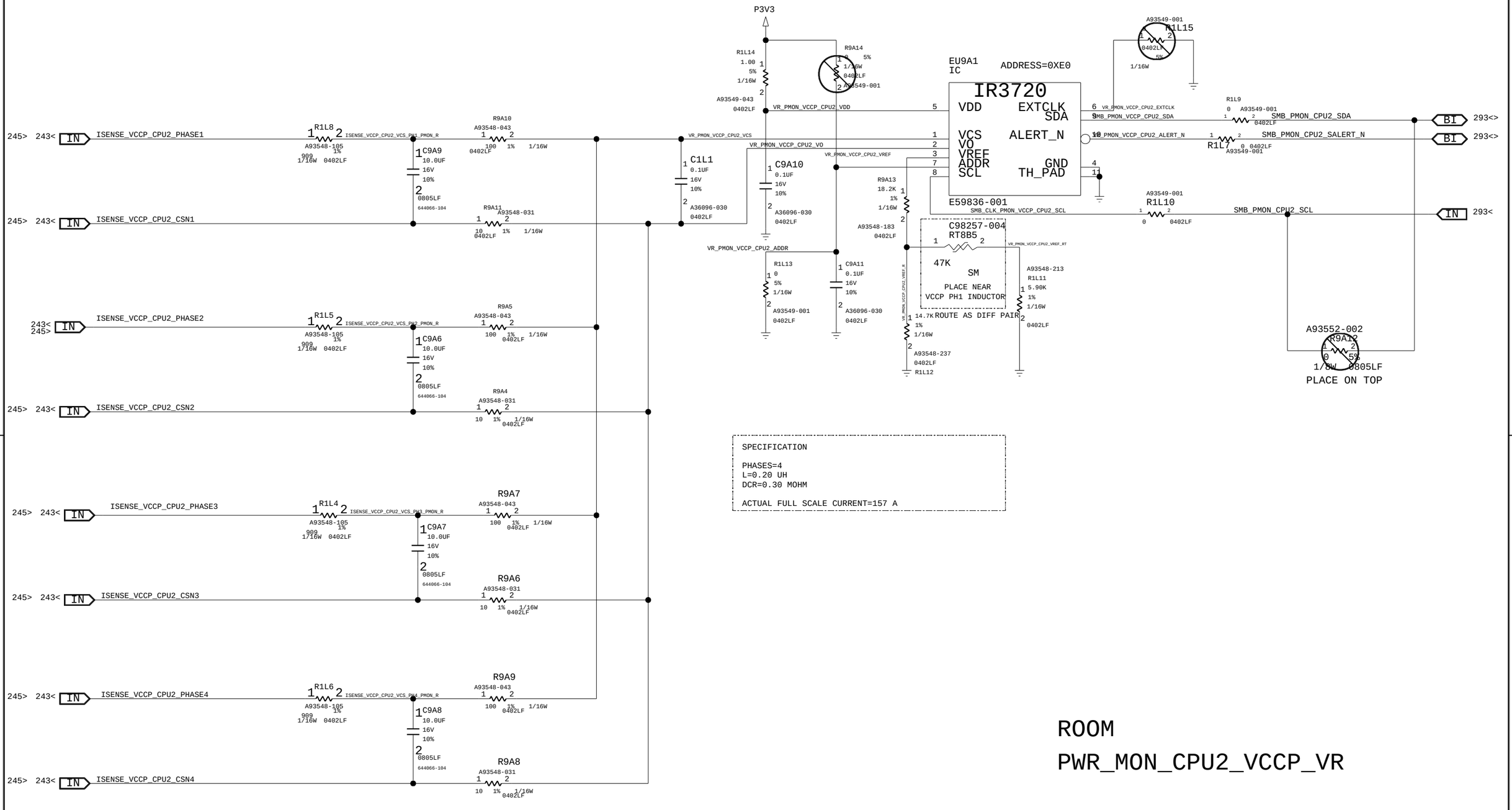


Wed Oct 27 15:22:09 2010

CPU1 VR MONITOR (2/2)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 291 OF 303	

INTEL CONFIDENTIAL



ROOM
PWR_MON_CPU2_VCCP_VR

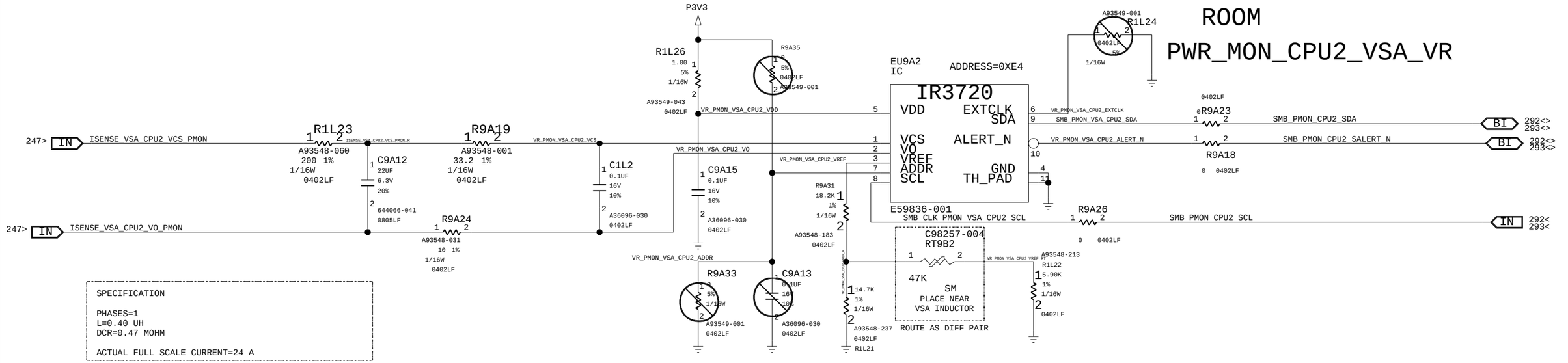
Wed Oct 27 15:22:09 2010

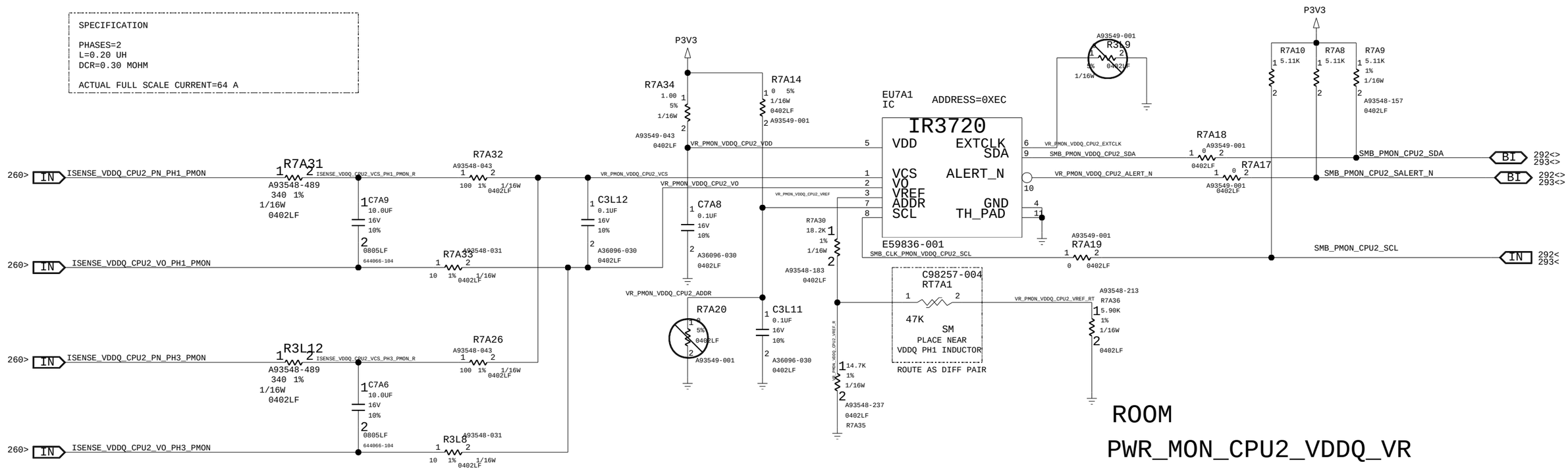
CPU2 VR MONITOR (1/2)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 292 OF 303	

INTEL CONFIDENTIAL

ROOM PWR_MON_CPU2_VSA_VR





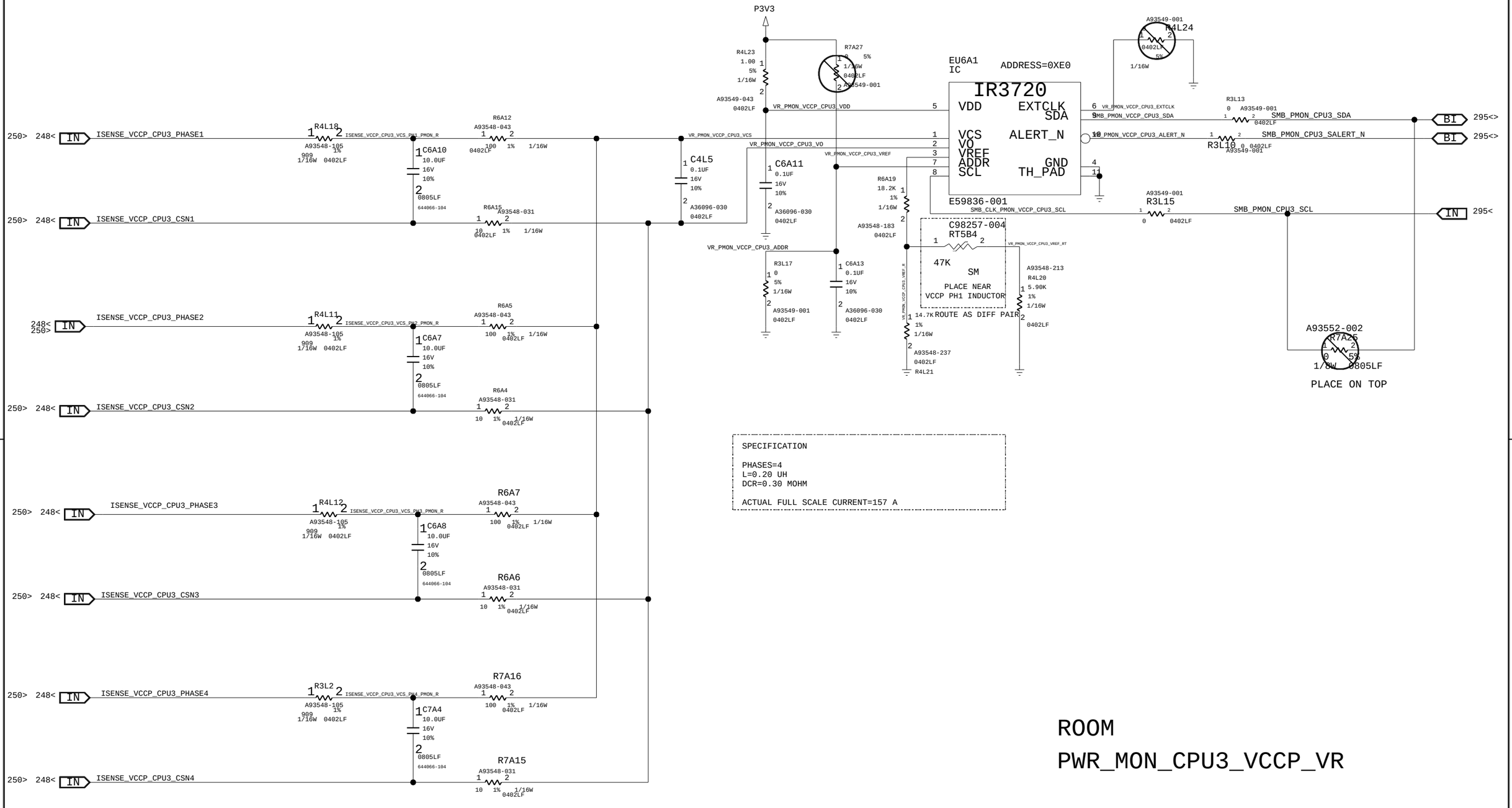
ROOM PWR_MON_CPU2_VDDQ_VR

Wed Oct 27 15:22:09 2010

CPU2 VR MONITOR (2/2)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 293 OF 303	

INTEL CONFIDENTIAL



SPECIFICATION

PHASES=4
L=0.20 UH
DCR=0.30 MOHM

ACTUAL FULL SCALE CURRENT=157 A

ROOM
PWR_MON_CPU3_VCCP_VR

Wed Oct 27 15:22:10 2010

CPU3 VR MONITOR (1/2)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 294 OF 303	

INTEL CONFIDENTIAL

ROOM PWR_MON_CPU3_VSA_VR

SPECIFICATION

PHASES=1
L=0.40 UH
DCR=0.47 MOHM

ACTUAL FULL SCALE CURRENT=24 A

252> IN ISENSE_VSA_CPU3_VCS_PMON
252> IN ISENSE_VSA_CPU3_VO_PMON
R4L26 A93548-060 200 1% 1/16W 0402LF
R6A21 A93548-001 33.2 1% 1/16W 0402LF
R6A28 A93548-031 10 1% 1/16W 0402LF
C6A12 22UF 6.3V 20% 644066-041 0805LF
C4L6 0.1UF 16V 10% A36096-030 0402LF
C6A17 0.1UF 16V 10% A36096-030 0402LF
P3V3
R4L31 1.00 5% 1/16W A93549-043 0402LF
R6A34 0 5% 0402LF A93549-001
VR_PMON_VSA_CPU3_VDD
VR_PMON_VSA_CPU3_VCS
VR_PMON_VSA_CPU3_VO
VR_PMON_VSA_CPU3_VREF
VR_PMON_VSA_CPU3_ADDR
R6A33 A93549-001 0402LF
C6A16 0.1UF 16V 10% A36096-030 0402LF
EU6A2 IC ADDRESS=0XE4
IR3720
VDD EXTCLK SDA VCS ALERT_N VO VREF ADDR GND SCL TH_PAD
E59836-001
R6A31 18.2K 1% 1/16W A93548-183 0402LF
R4L27 14.7K 1% 1/16W A93548-237 0402LF
C98257-004 RT6B2 47K SM PLACE NEAR VSA INDUCTOR
ROUTE AS DIFF PAIR
A93549-001 R4L29 0402LF 5% 1/16W
R6A23 0 0402LF
R6A20 0 0402LF
R6A29 0 0402LF
A93548-213 R4L28 5.90K 1% 1/16W 0402LF
VR_PMON_VSA_CPU3_EXTCLK
SMB_PMON_VSA_CPU3_SDA
VR_PMON_VSA_CPU3_ALERT_N
SMB_CLK_PMON_VSA_CPU3_SCL
SMB_PMON_CPU3_SDA
SMB_PMON_CPU3_SALERT_N
SMB_PMON_CPU3_SCL
BI 294<> 295<>
IN 294< 295<

SPECIFICATION

PHASES=2
L=0.20 UH
DCR=0.30 MOHM

ACTUAL FULL SCALE CURRENT=64 A

263> IN ISENSE_VDDQ_CPU3_PN_PH1_PMON
263> IN ISENSE_VDDQ_CPU3_VO_PH1_PMON
263> IN ISENSE_VDDQ_CPU3_PN_PH3_PMON
263> IN ISENSE_VDDQ_CPU3_VO_PH3_PMON
R4A12 A93548-489 340 1% 1/16W 0402LF
R4A10 A93548-043 100 1% 1/16W 0402LF
R4A9 A93548-031 10 1% 1/16W 0402LF
R6L19 A93548-489 340 1% 1/16W 0402LF
R4A11 A93548-043 100 1% 1/16W 0402LF
R6L20 A93548-031 10 1% 1/16W 0402LF
C4A3 10.0UF 16V 10% 644066-104 0805LF
C4A4 10.0UF 16V 10% 644066-104 0805LF
C6L9 0.1UF 16V 10% A36096-030 0402LF
C4A2 0.1UF 16V 10% A36096-030 0402LF
C6L7 0.1UF 16V 10% A36096-030 0402LF
P3V3
R4A4 1.00 5% 1/16W A93549-043 0402LF
R6L10 0 5% 1/16W 0402LF A93549-001
VR_PMON_VDDQ_CPU3_VDD
VR_PMON_VDDQ_CPU3_VCS
VR_PMON_VDDQ_CPU3_VO
VR_PMON_VDDQ_CPU3_VREF
VR_PMON_VDDQ_CPU3_ADDR
R4A2 A93549-001 0402LF
EU4A1 IC ADDRESS=0XEC
IR3720
VDD EXTCLK SDA VCS ALERT_N VO VREF ADDR GND SCL TH_PAD
E59836-001
R4A5 18.2K 1% 1/16W A93548-183 0402LF
R4A6 14.7K 1% 1/16W A93548-237 0402LF
C98257-004 RT4A1 47K SM PLACE NEAR VDDQ PH1 INDUCTOR
ROUTE AS DIFF PAIR
A93549-001 R6L14 0402LF 5% 1/16W
R6L17 A93549-001 0402LF
R6L18 A93549-001 0402LF
R6L15 0 0402LF
A93548-213 R4A3 5.90K 1% 1/16W 0402LF
R7L14 5.11K
R7L18 5.11K
R7L17 5.11K 1% 1/16W
A93548-157 0402LF
VR_PMON_VDDQ_CPU3_EXTCLK
SMB_PMON_VDDQ_CPU3_SDA
VR_PMON_VDDQ_CPU3_ALERT_N
SMB_PMON_CPU3_SDA
SMB_PMON_CPU3_SALERT_N
SMB_PMON_CPU3_SCL
BI 294<> 295<>
IN 294< 295<

ROOM PWR_MON_CPU3_VDDQ_VR

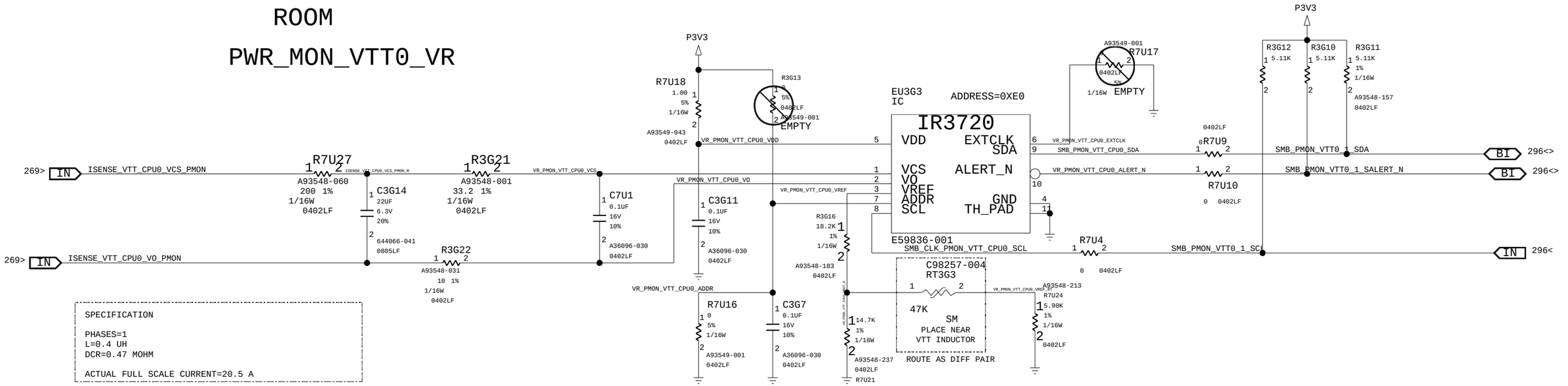
Wed Oct 27 15:22:10 2010

CPU3 VR MONITOR (2/2)

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 295 OF 303	

INTEL CONFIDENTIAL

ROOM PWR_MON_VTT0_VR

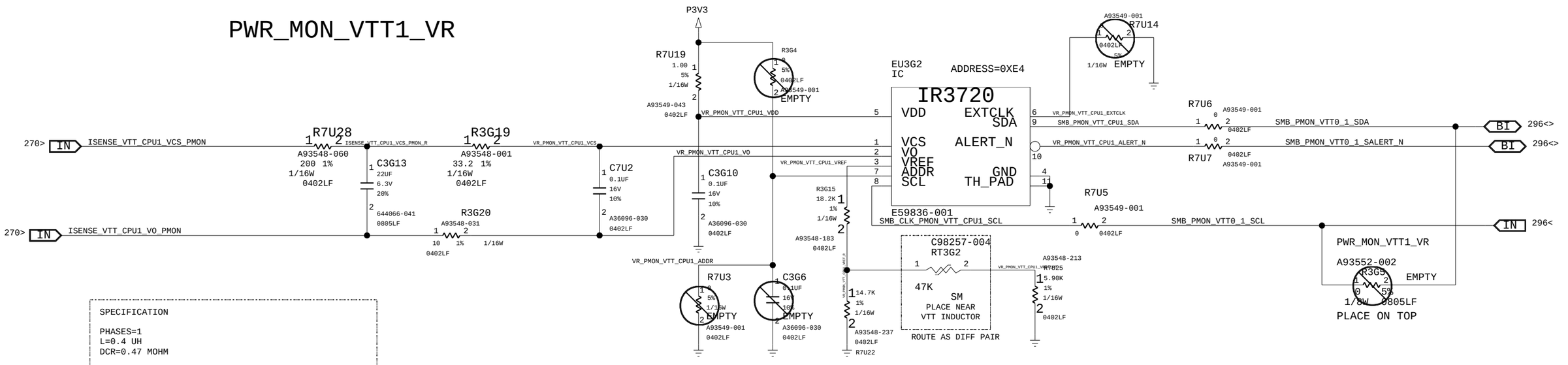


SPECIFICATION

PHASES=1
L=0.4 UH
DCR=0.47 MOHM

ACTUAL FULL SCALE CURRENT=20.5 A

ROOM PWR_MON_VTT1_VR



SPECIFICATION

PHASES=1
L=0.4 UH
DCR=0.47 MOHM

ACTUAL FULL SCALE CURRENT=20.5 A

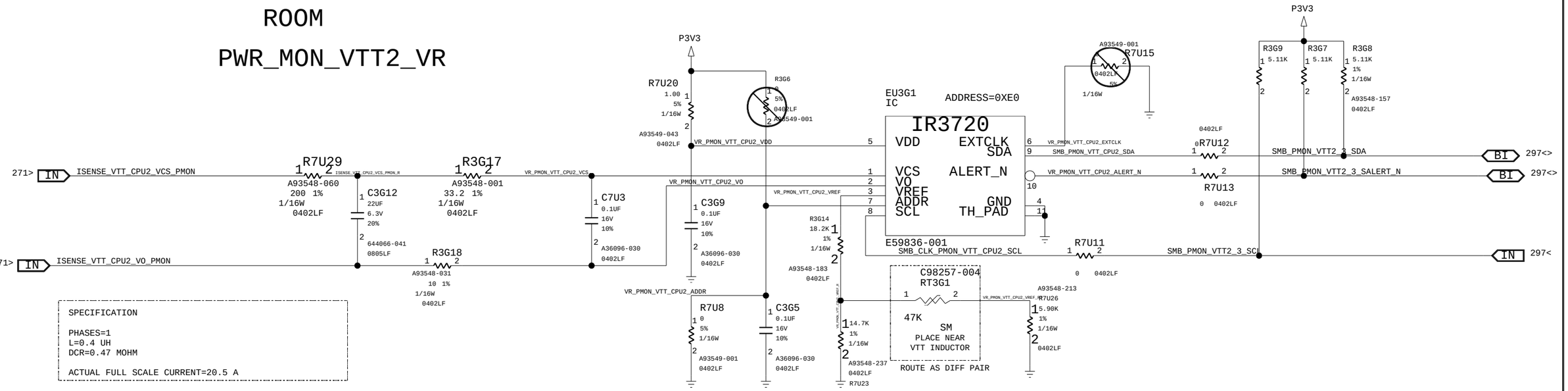
Wed Oct 27 15:22:10 2010

VTT0 AND VTT1 MONITOR

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 296 OF 303	

INTEL CONFIDENTIAL

ROOM
PWR_MON_VTT2_VR



SPECIFICATION

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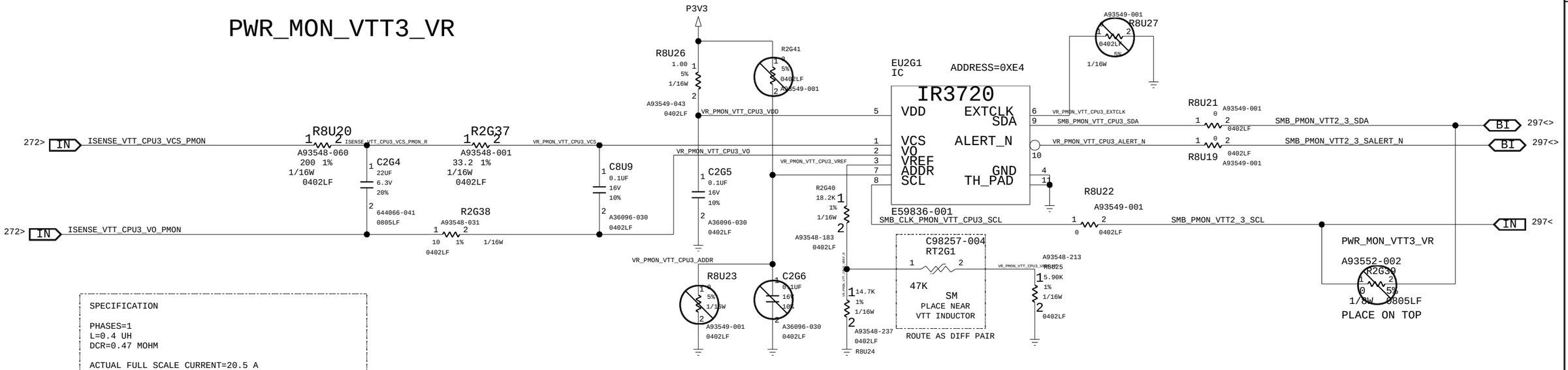
L=0.4 UH
DCR=0.47 MOHM

ACTUAL FULL SCALE CURRENT=20.5 A

ROOM
PWR_MON_VTT3_VR



SPECIFICATION

PHASES=1
L=0.4 UH
DCR=0.47 MOHM

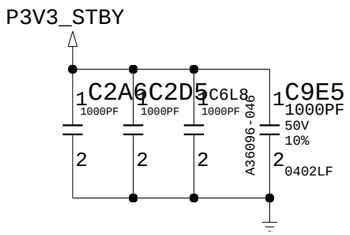
ACTUAL FULL SCALE CURRENT=20.5 A

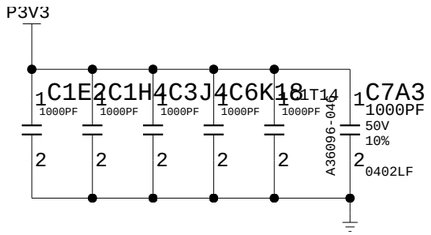
Wed Oct 27 15:22:10 2010

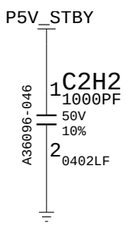
VTT2 AND VTT3 MONITOR

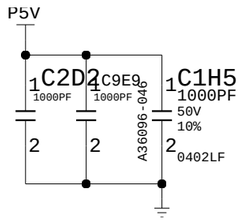
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 297 OF 303	

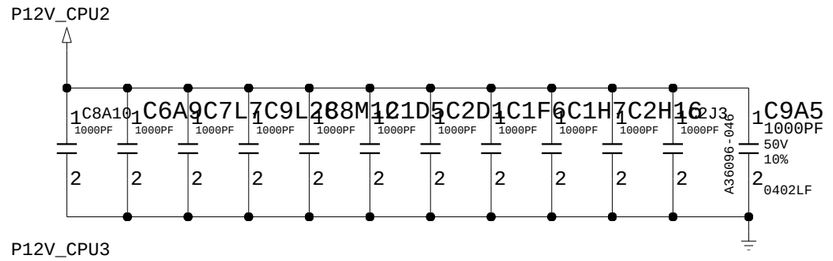
INTEL CONFIDENTIAL

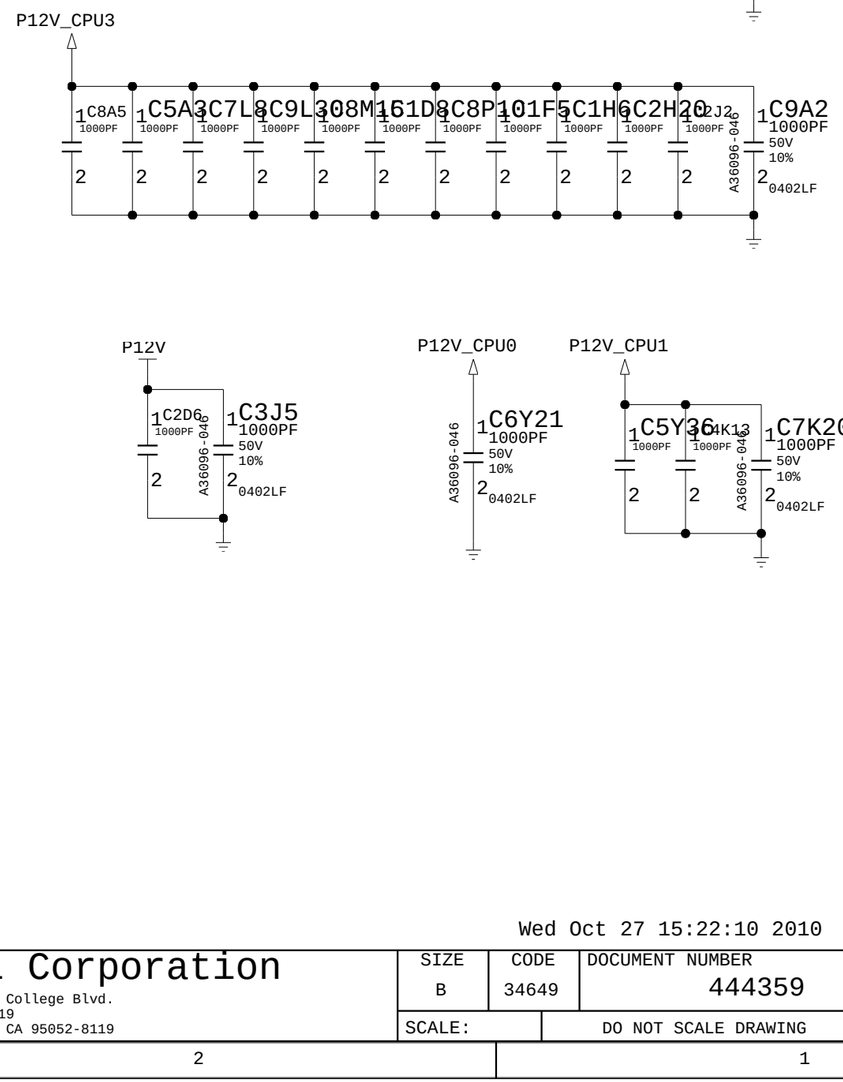












CAD NOTE: SPREAD CAPS OVER THE
ENTIRE COPPER FILL AREA TO REDUCE
NOISE CAUSED BY VR AND OTHER CIRCUITRY

CAPS FOR NOISE PREVENTION

ROOM
MISC_POWER

Wed Oct 27 15:22:10 2010

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 298 OF 303	

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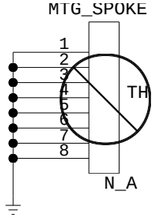
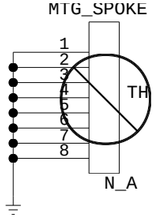
MH9A1 MTG_SPOKE



MH9K1 MTG_SPOKE



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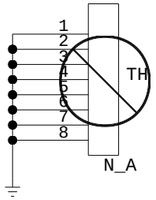
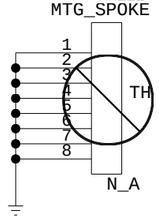


MH1E1 MTG_SPOKE



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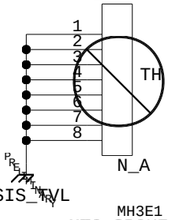
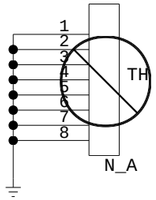


GND_CHASSIS_TVL

MH1J1 MTG_SPOKE



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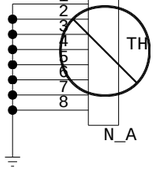

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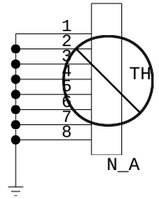

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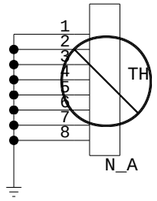

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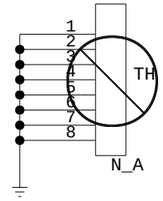
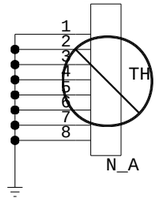
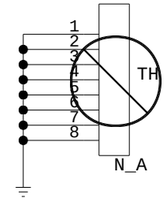


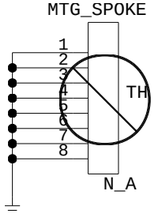
MH6F1 MTG_SPOKE



MH1A1 MTG_SPOKE



MH7F1 MTG_SPOKE



REGULATORY MARKINGS

LB6F1 LOGOLABEL_A

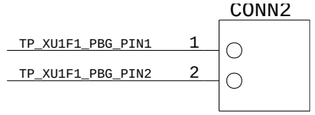
LB3E1 PB_FREE_A

LB3D1 BLANKLABEL_A

LB3F1 SNLABEL_A

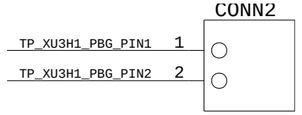
TWINVILLE AND PATSBURG HEATSINK ANCHORS

XU1E1 CONN2



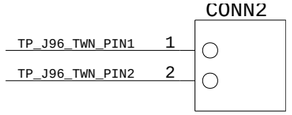
A13494-008

XU2G1 CONN2



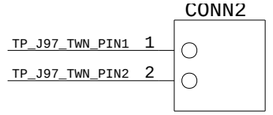
A13494-008

J2A1 CONN2



A13494-008

J3B1 CONN2



A13494-008

Wed Oct 27 15:22:11 2010

MOUNTING HOLES/LABELS/COMPLIANCE COUPONS(1 OF 2)

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 299 OF 303

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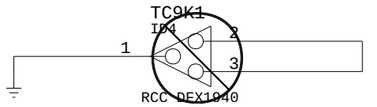
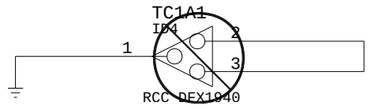
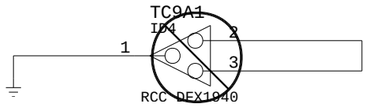
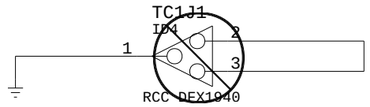
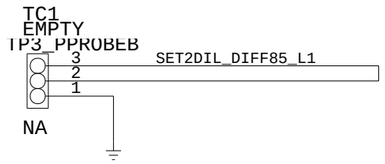
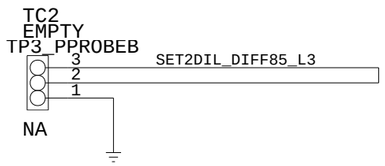


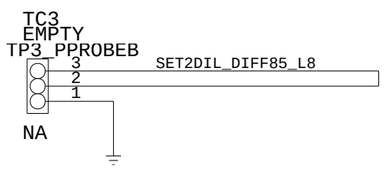


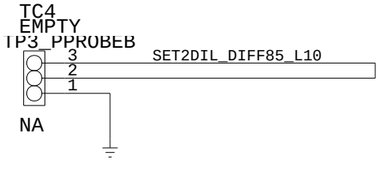




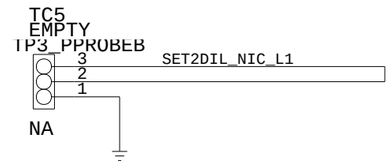


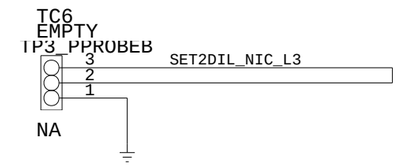


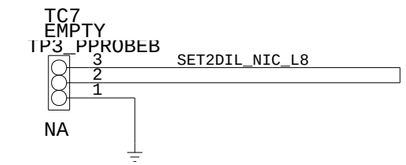




CAD NOTES:
KEEP THE ROUTING AS NIC_ MDI TRACES ARE.







CAD NOTES:
1. DIFF85 ROUTING
2. LOOP BACK TOTAL 8 INCHES (NOT INCLUDED SMALL LOOP SEGMENT)
   * IF SERPENTINING NEEDED, PLEASE FOLLOWING THE SPACING RULES:
     20XH (U-STRIP)
     10XH (STRIPLINE)
3. 5 DEGREE ANGLE ROUTING
4. VOID ANTI-PAD BETWEEN VIAS PAIR ON THE INNER LAYER
5. PLACE PROBE ON TOP FOR L1/L8 TO MINIMIZE VIA STUB
6. PLACE PROBE ON BOT FOR L3/L10 TO MINIMIZE VIA STUB
7. ADDING MEANINGFUL SILKSCREEN (EG: L3, Z85) RIGHT NEXT TO THE LAUNCH SITES
   (AND ON THE APPROPRIATE SIDE PRIMARY OR SECONDARY)

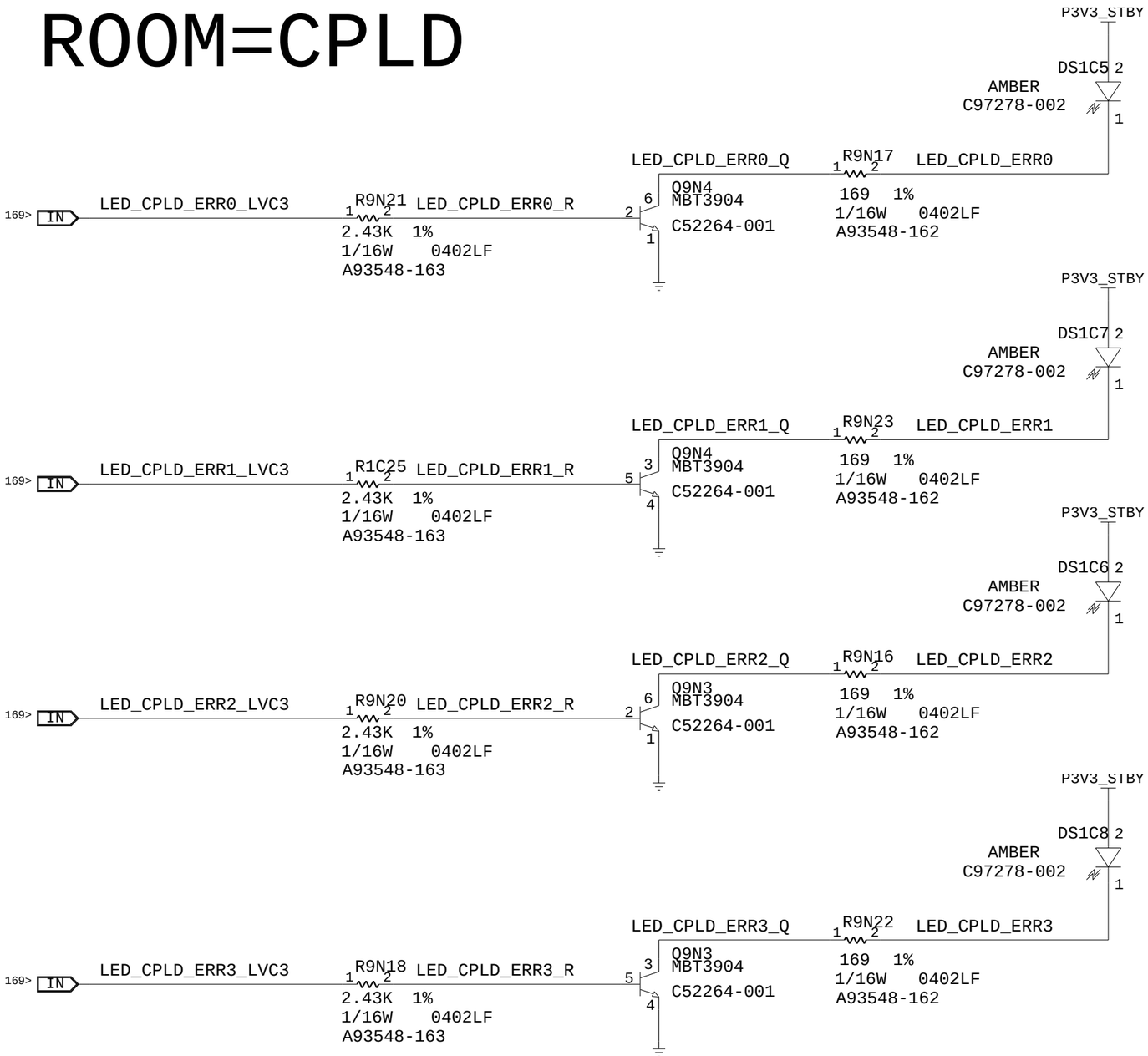
Wed Oct 27 15:21:19 2010

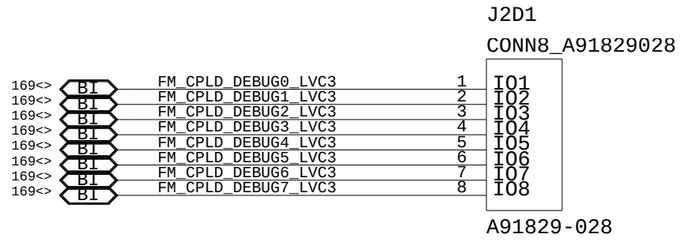
MOUNTING HOLES/LABELS/COMPLIANCE COUPONS(2 OF 2)

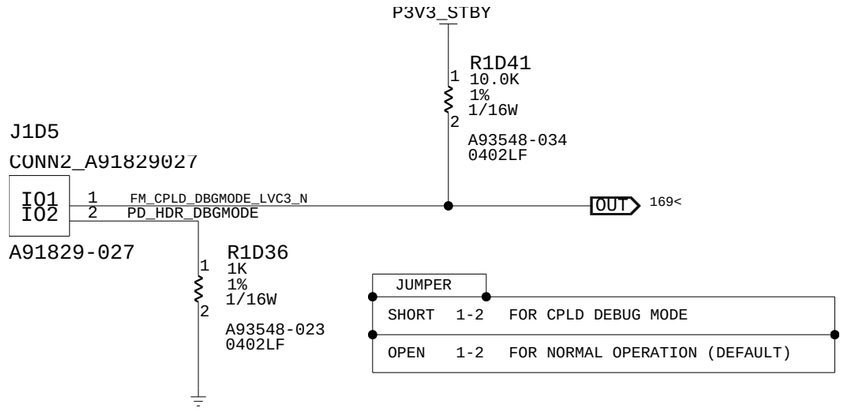
DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 300 OF 303	

INTEL CONFIDENTIAL

ROOM=CPLD







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CPLD DEBUG HOOKS

DEPARTMENT	Intel Corporation	SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 301 OF 303	

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P3V3_STBY

R1J36
1K
1%
1/16W
A93548-023
0402LF

PWRGD_XDP_CO — OUT — 134> 168> 169<

XDP POWER CYCLE MODE.

P3V3_STBY

R1D33
10.0K
1%
1/16W
A93548-034
0402LF

J1D3
CONN2_A91829027
IO1
IO2
1 FM_XDP_PWRCYCLE_MODE_CO — OUT 169<
2 PD_HDR_PWRCYCLE
A91829-027

R1D34
1K
1%
1/16W
A93548-023
0402LF

JUMPER		
SHORT	1-2	LOGIC ONLY PWR CYCLE
OPEN	1-2	FULL PWR CYCLE (DEFAULT)

P3V3_STBY

R1J38
1K
1%
1/16W
A93548-023
0402LF

RST_XDP_CO_N — OUT — 134> 168> 169< 229<

X24 PCIE RESET SOURCE

P3V3_STBY

R1D9
10.0K
1%
1/16W
A93548-034
0402LF

J1D1
CONN2_A91829027
IO1
IO2
1 FM_PERST_SRC_LVC3 — OUT 169<
2 PD_HDR_PERST_SRC
A91829-027

R1D15
1K
1%
1/16W
A93548-023
0402LF

JUMPER		
SHORT	1-2	SELECT PLATFORM RESET
OPEN	1-2	SELECT PWRGD RST (DEFAULT)

ROOM=PWRRST_SEQ

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SYSTEM PWR/RESET SEQUENCE

DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 302 OF 303	

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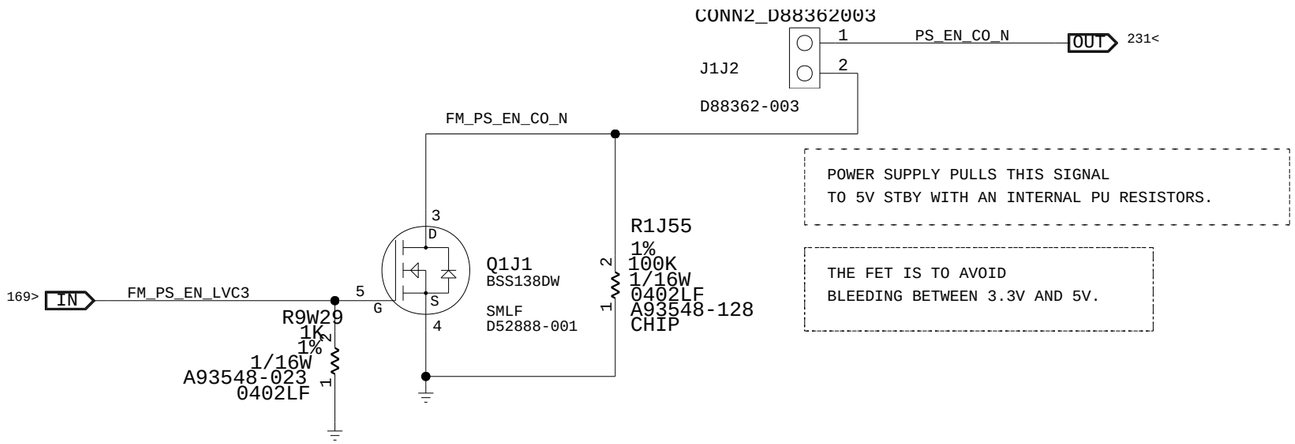
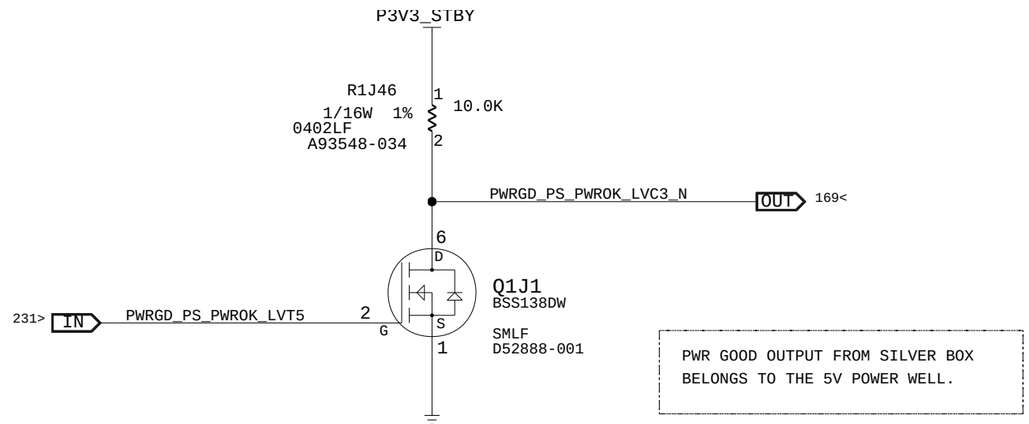
EMERGENCY/KILL POWER HEADER





ROOM=PWRSUPPLY

POWER-SUPPLY POWER-ON SEQUENCE

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DEPARTMENT		SIZE	CODE	DOCUMENT NUMBER	REV
DCPAE	Intel Corporation 2200 Mission College Blvd. P.O. BOX 58119 Santa Clara, CA 95052-8119	B	34649	444359	1.0
		SCALE:	DO NOT SCALE DRAWING	SHEET 303 OF 303	