



Comet Lake S UDIMM(3200) CMP-H Reference Validation Platform

Customer Reference Board Schematics

Revision 0.7

October 2019

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Revision History

Document Number	Revision Number	Description	Revision Date
615704	0.7	Initial Schematics	October 2019

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MODULE REV DETAILS

MODULE NAME	REV	DATE

CML-S UDIMM(3200) CMP-H RVP
 REV 0.7

BPAGE DRAWING

udimm.sch_1.1
Tue Sep 24 13:43:59 2019

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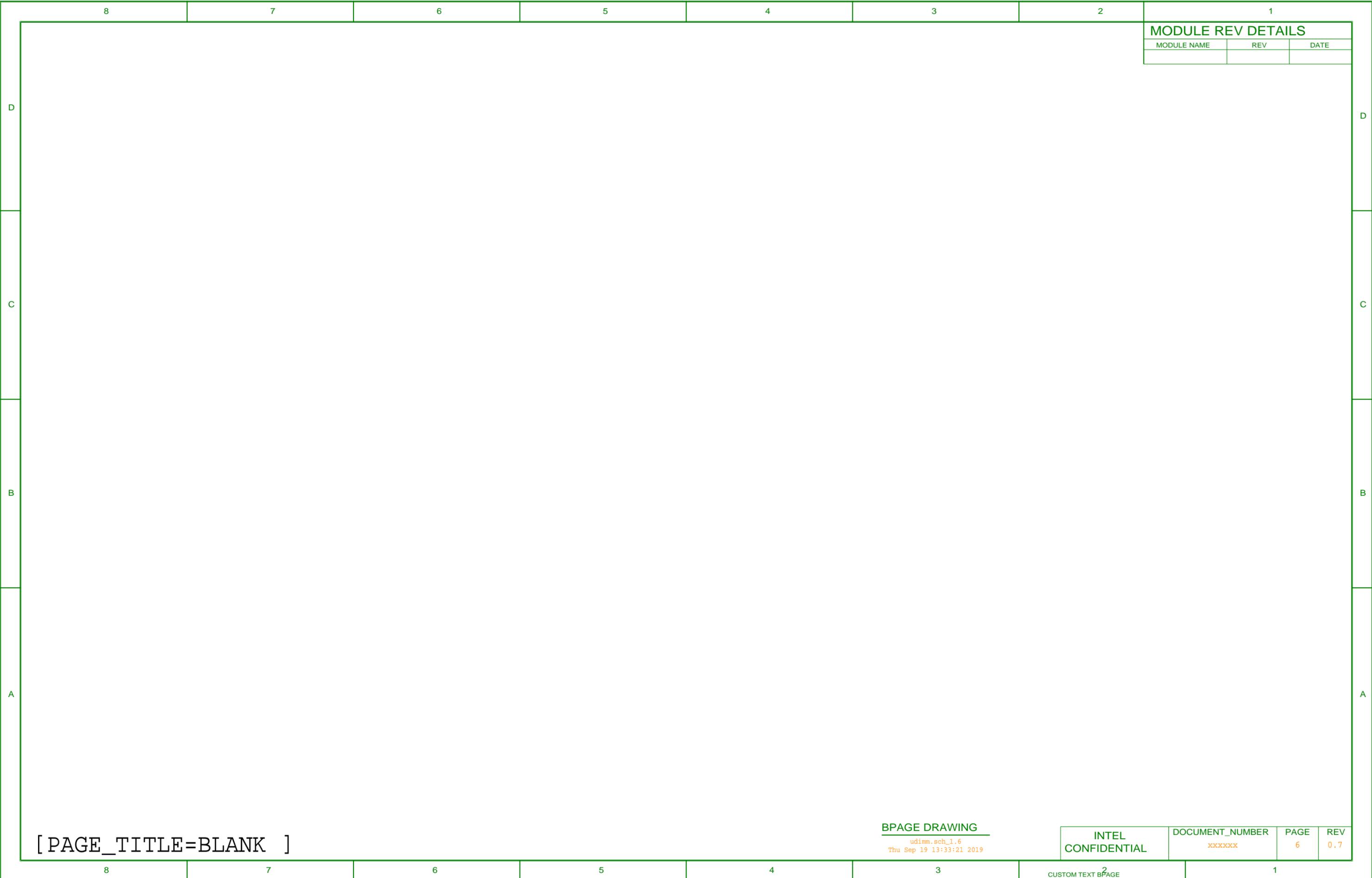
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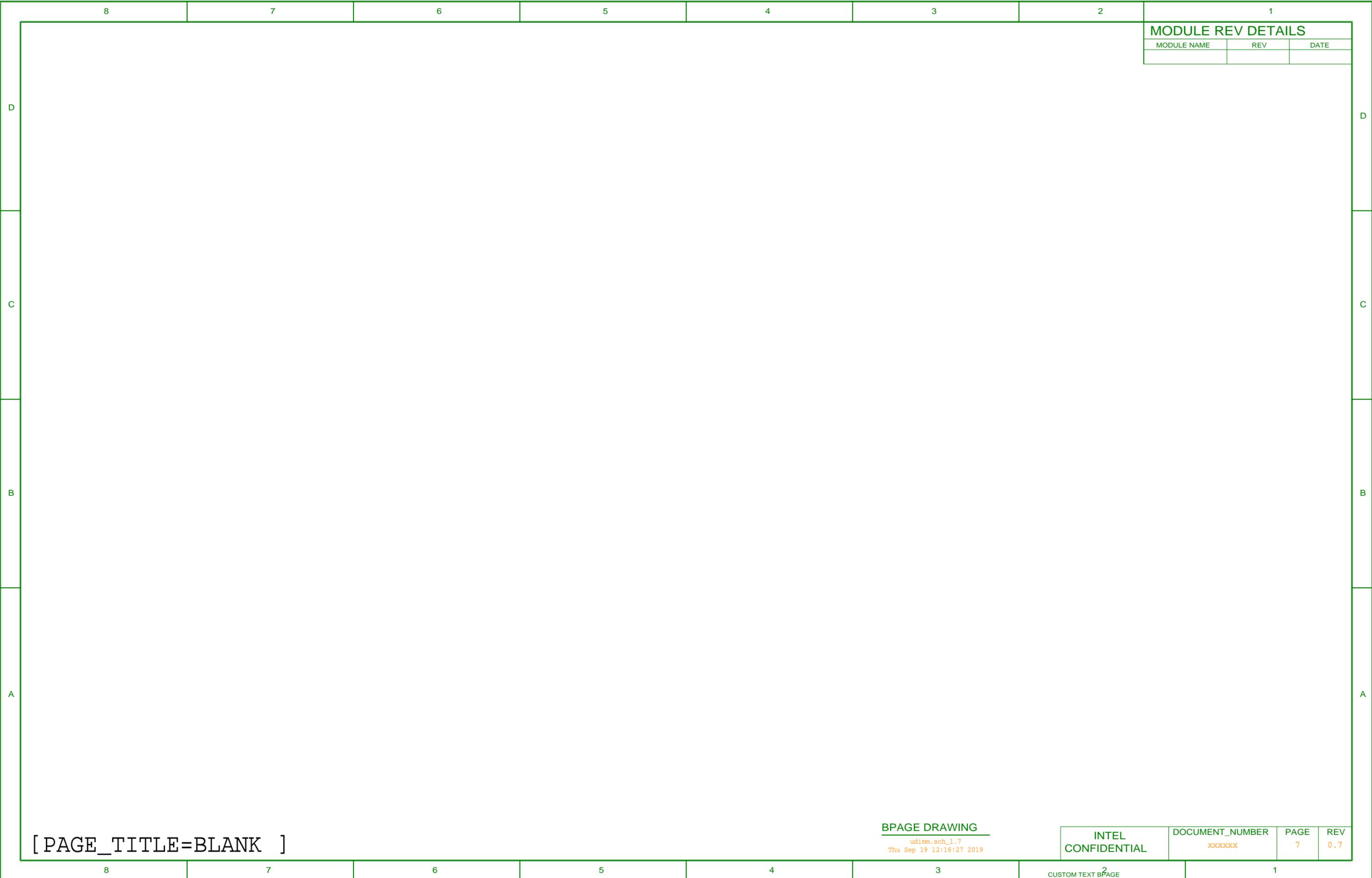
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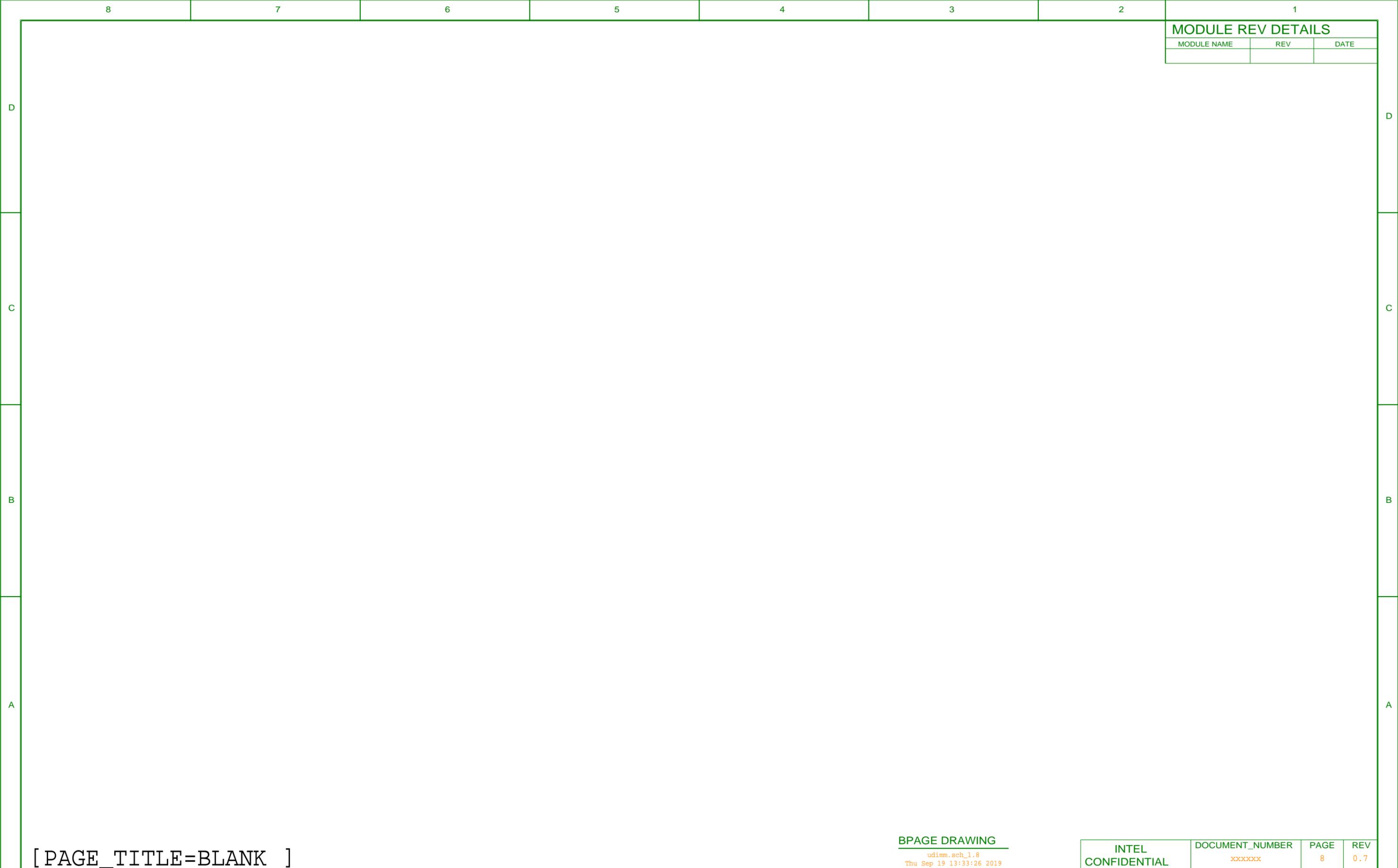
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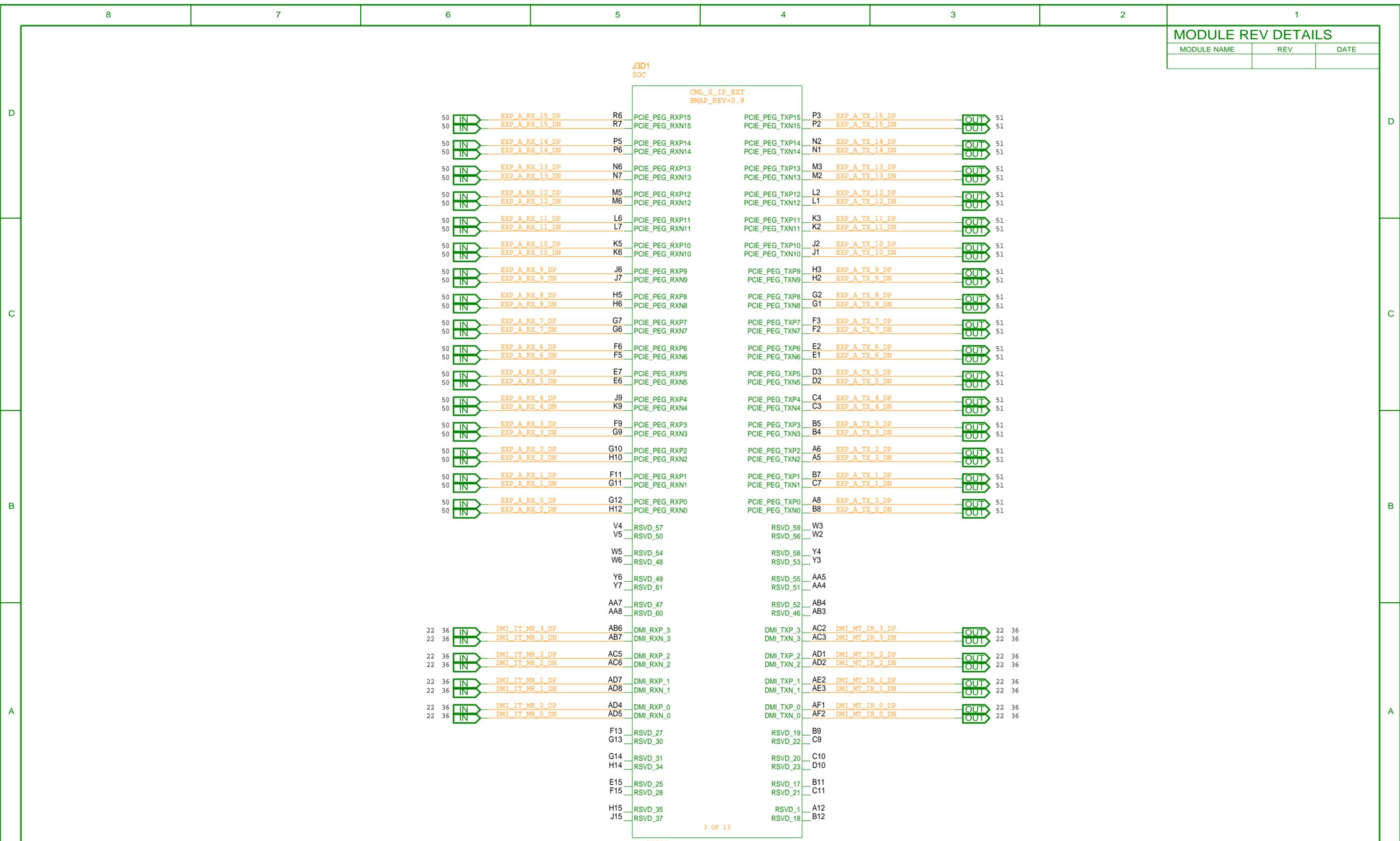
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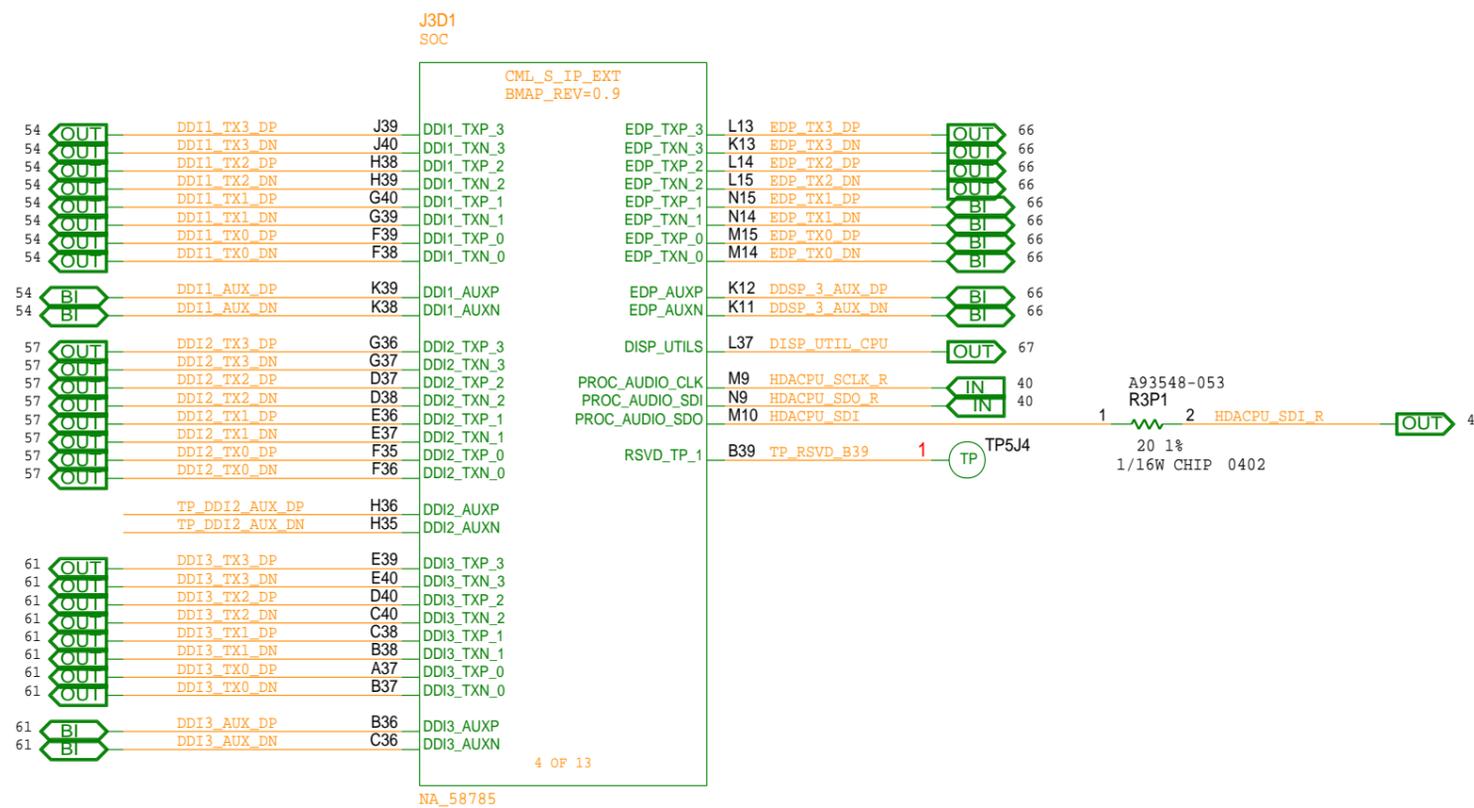
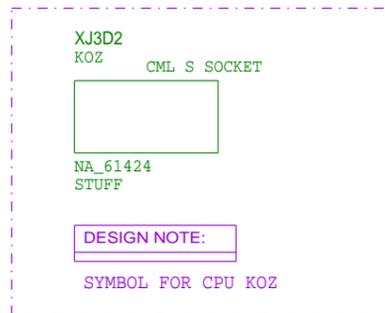
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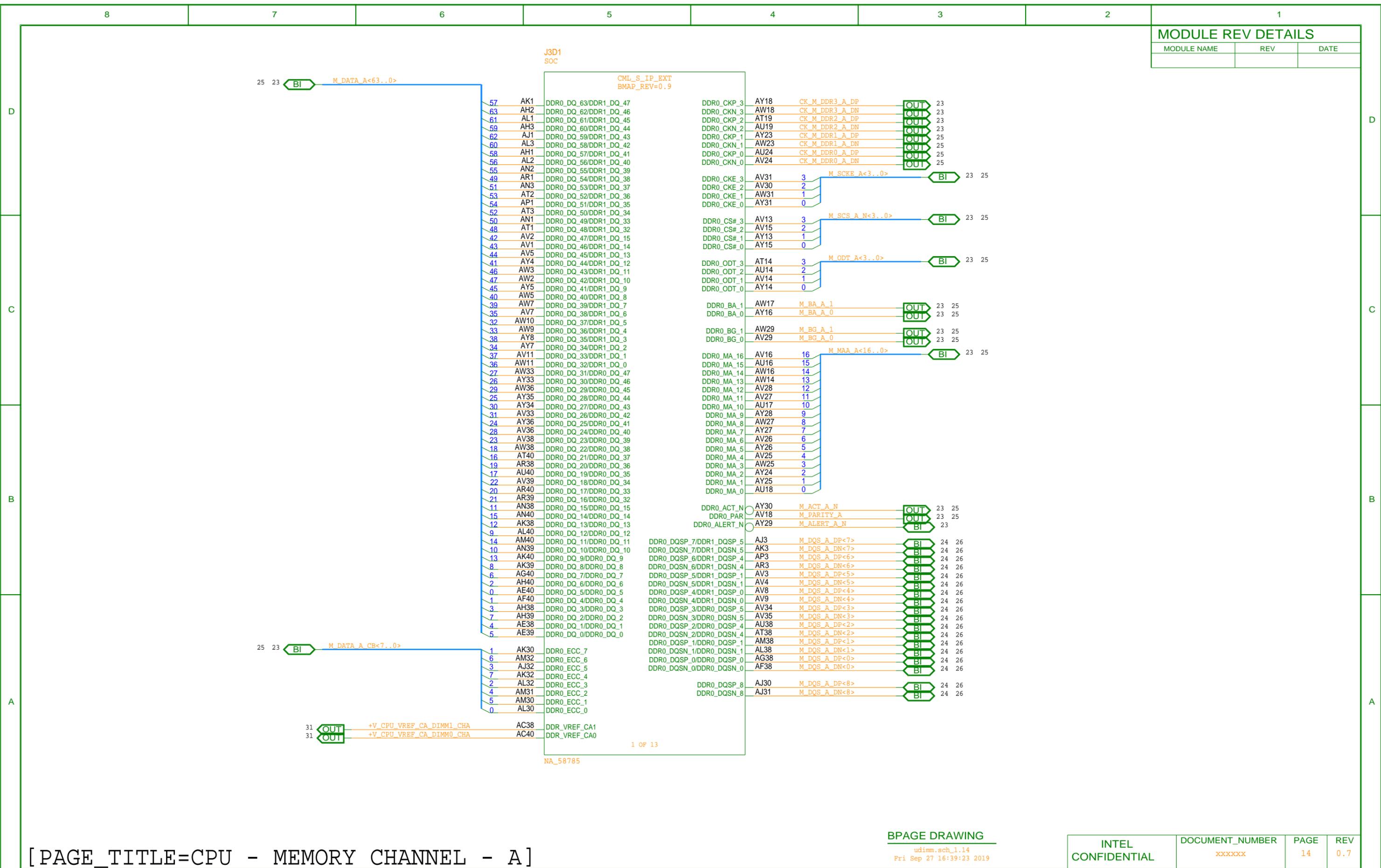


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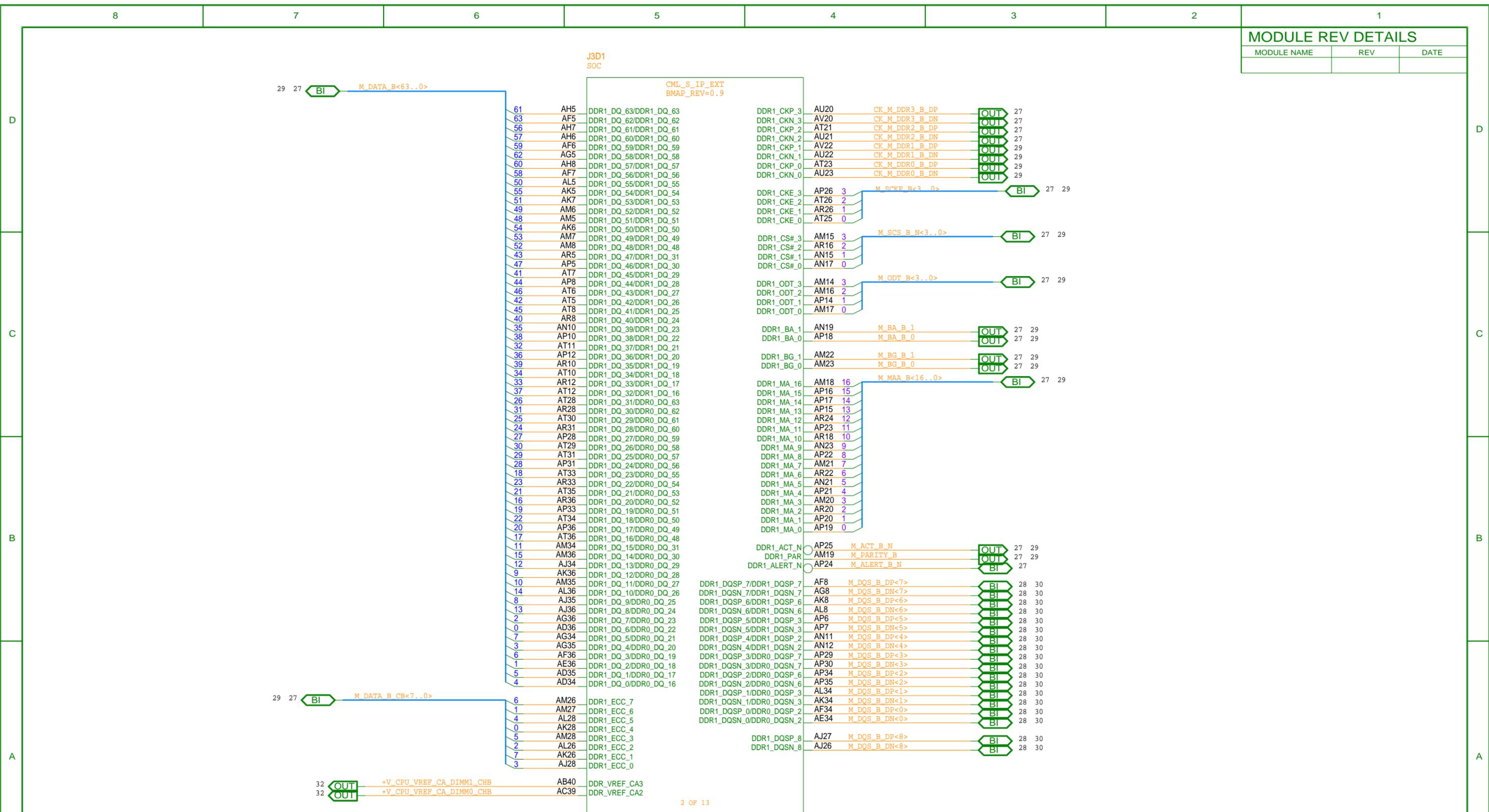
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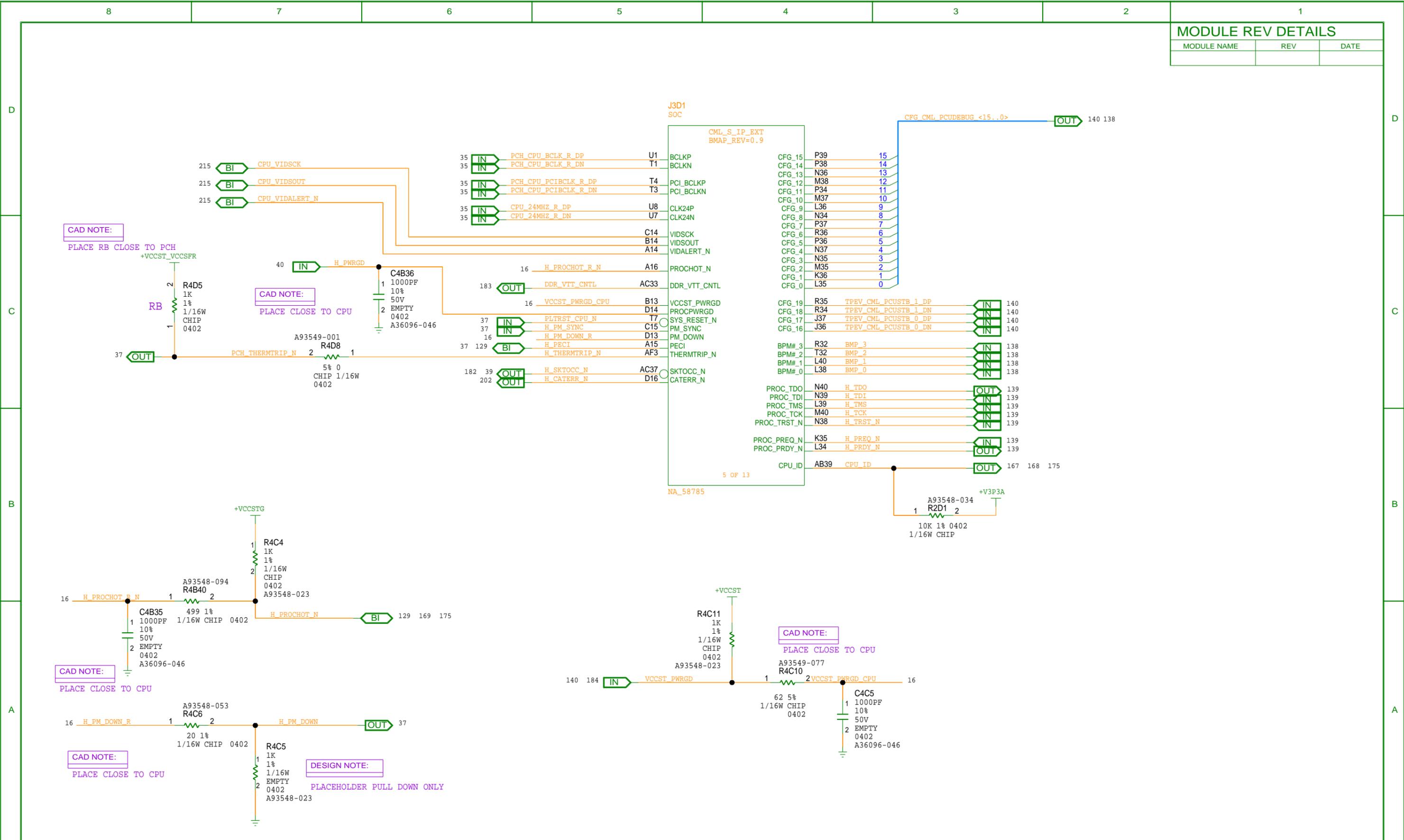
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[PAGE_TITLE=CPU - MEMORY CHANNEL - B]

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CAD NOTE:

PLACE RB CLOSE TO PCH

CAD NOTE:

PLACE CLOSE TO CPU

CAD NOTE:

PLACE CLOSE TO CPU

CAD NOTE:

PLACE CLOSE TO CPU

DESIGN NOTE:

PLACEHOLDER PULL DOWN ONLY

CAD NOTE:

PLACE CLOSE TO CPU

[PAGE_TITLE=CPU - PM , CFG , JTAG, CLK]

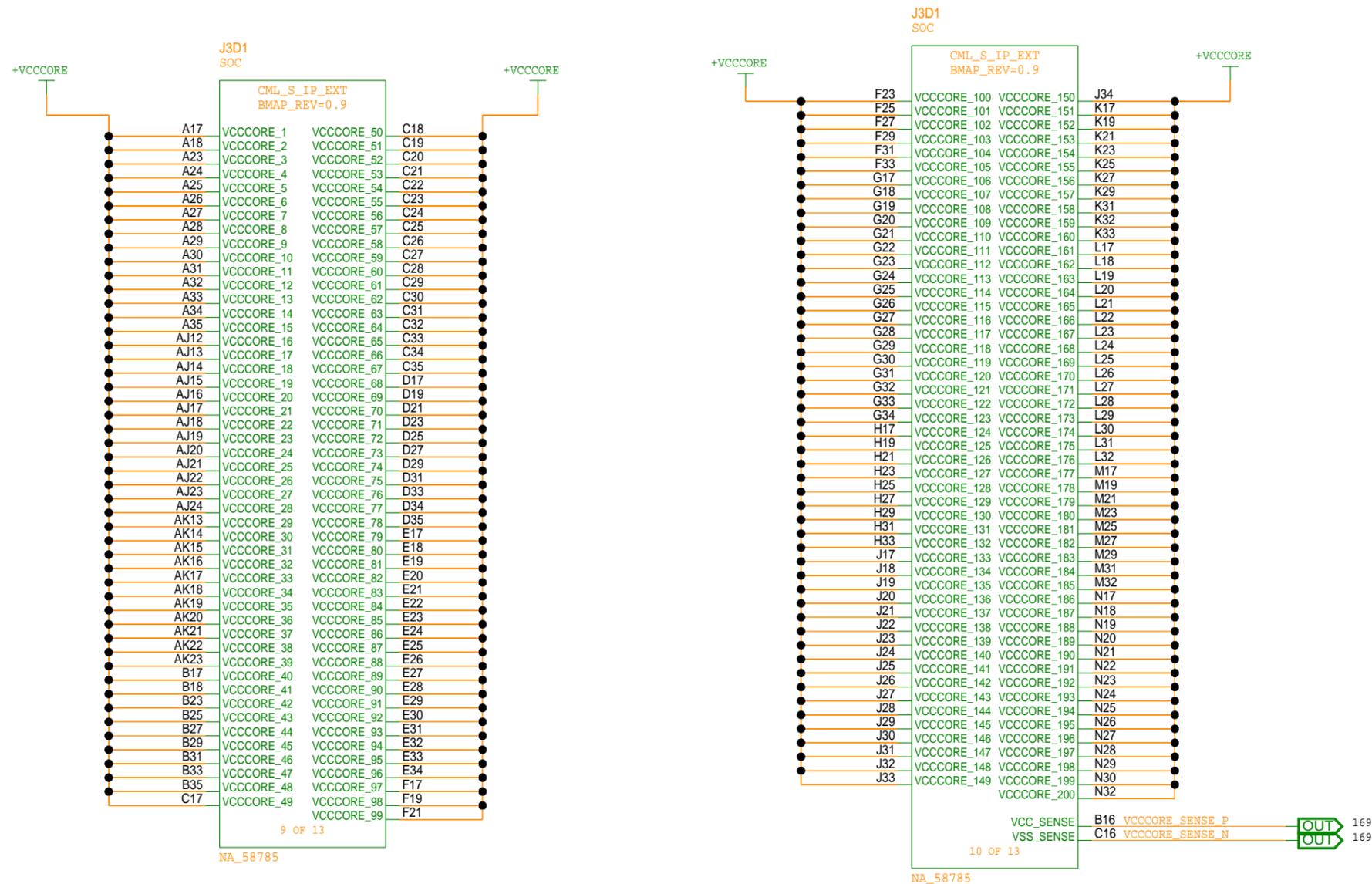
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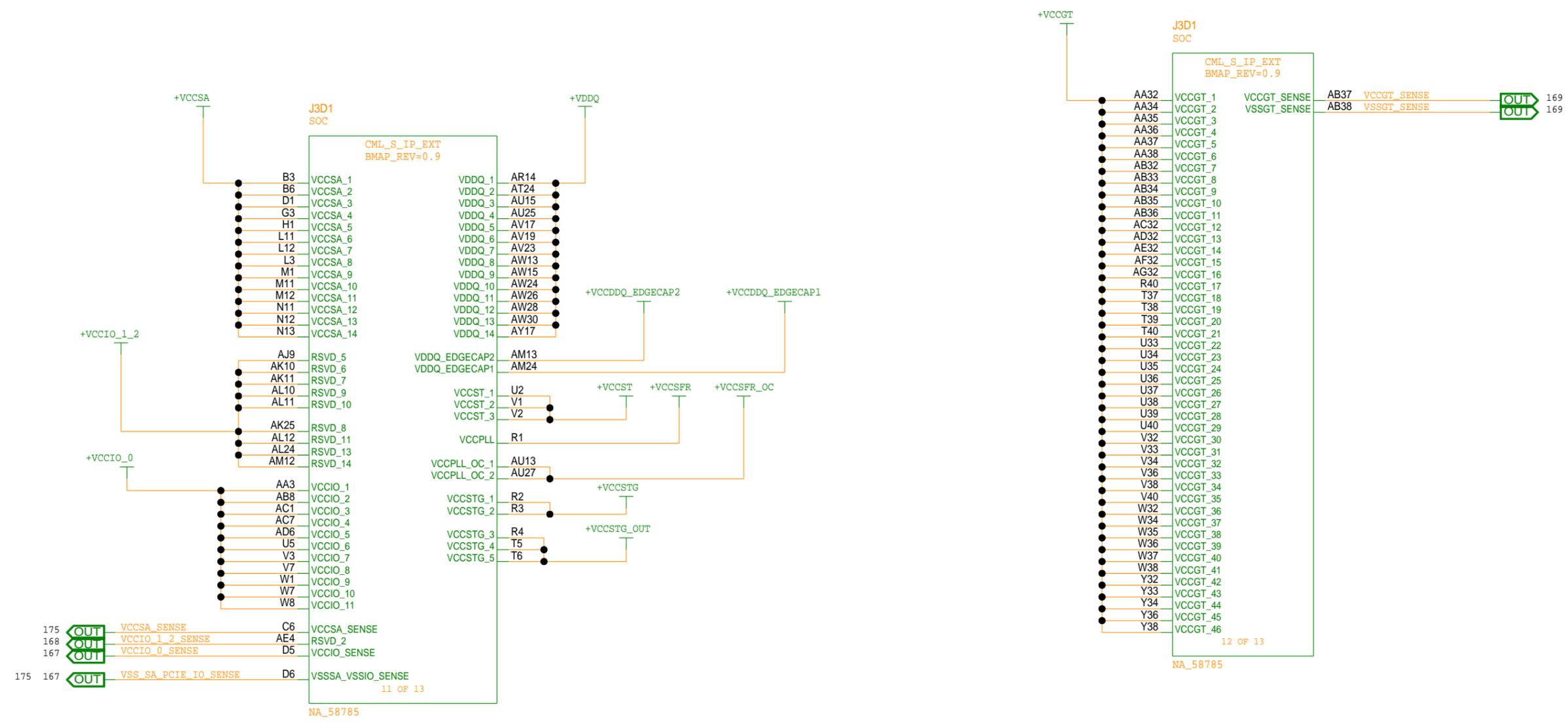
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MODULE REV DETAILS

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NOTE:+VCCIO_1_2 IS REQUIRED TO SUPPORT FORWARD COMPATIBILITY WITH 2021 NEXT GEN S-SERIES CPU ON CML-S BASED BOARDS.
 +VCCIO_1_2 IS NOT REQUIRED IF BOARD IS DESIGNED TO SUPPORT CML-S CPU ONLY.

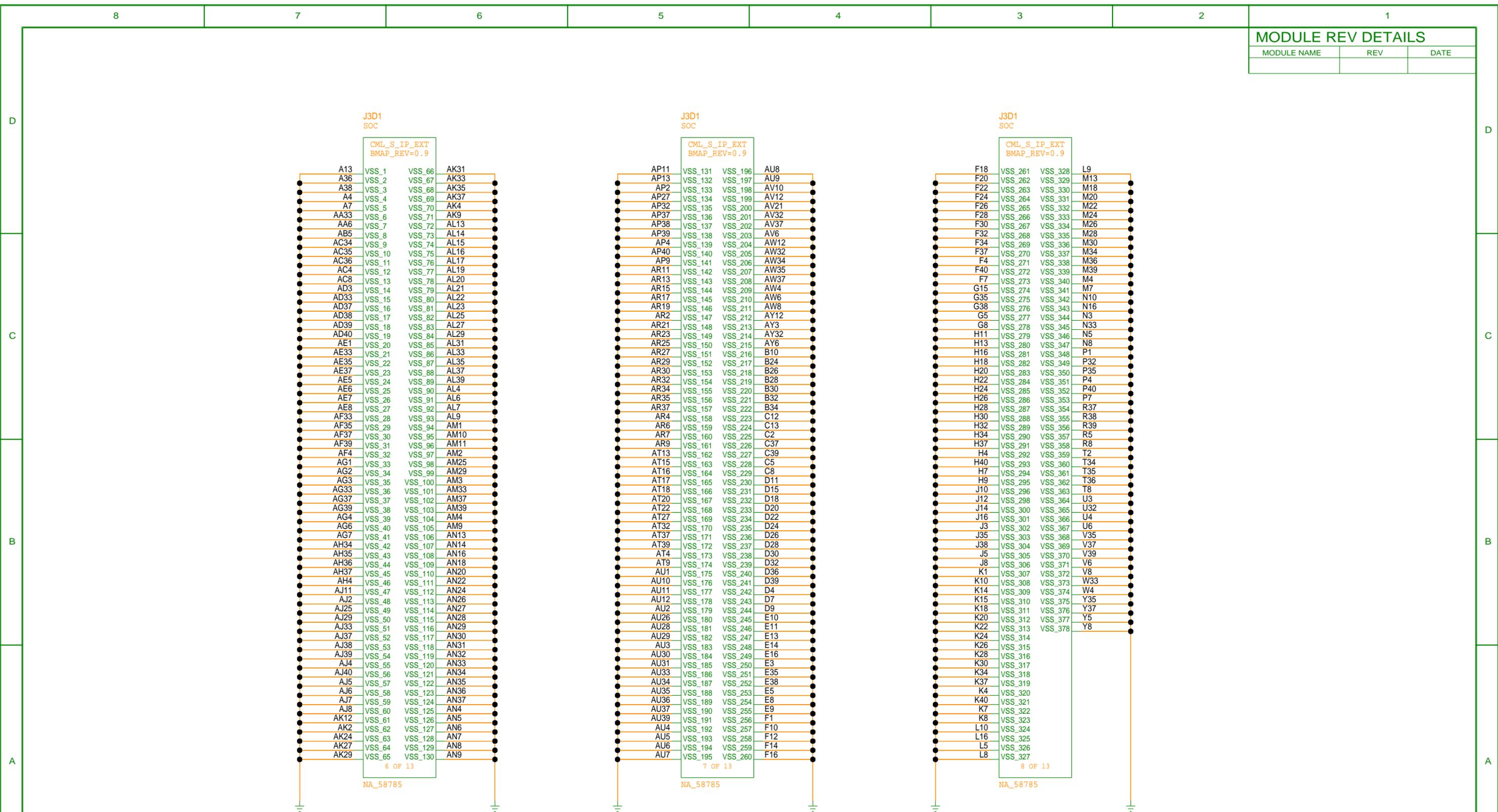
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[PAGE_TITLE=CPU - POWER , VSS]

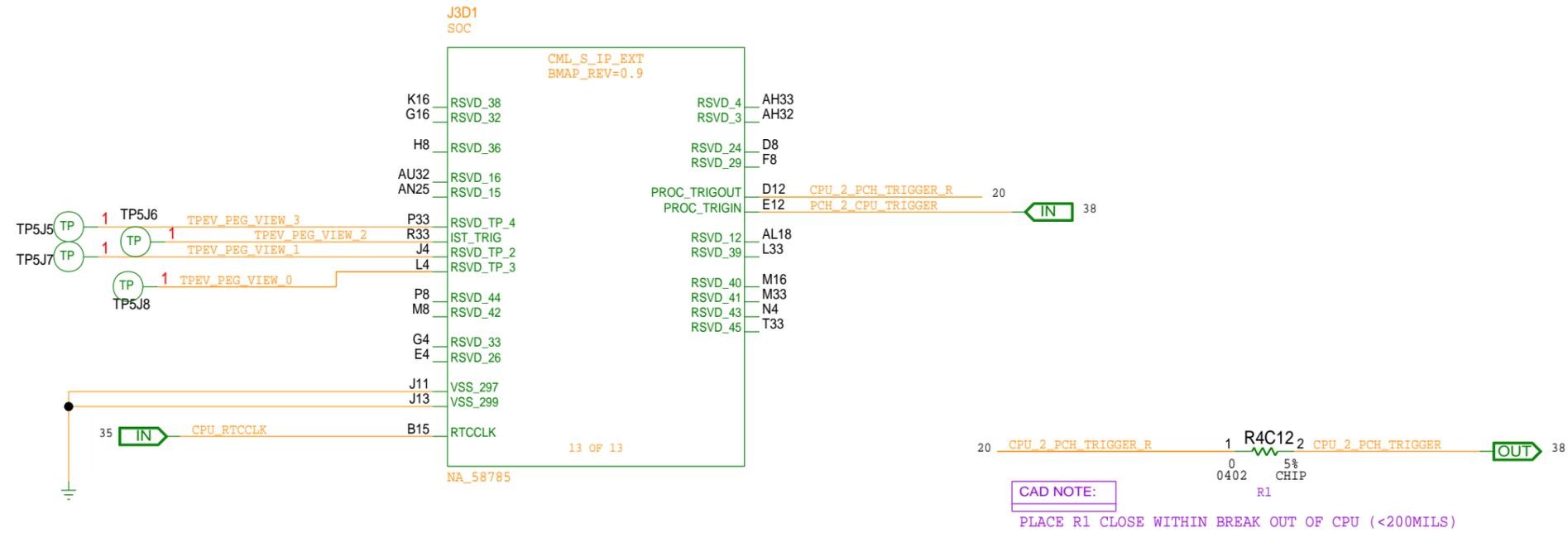
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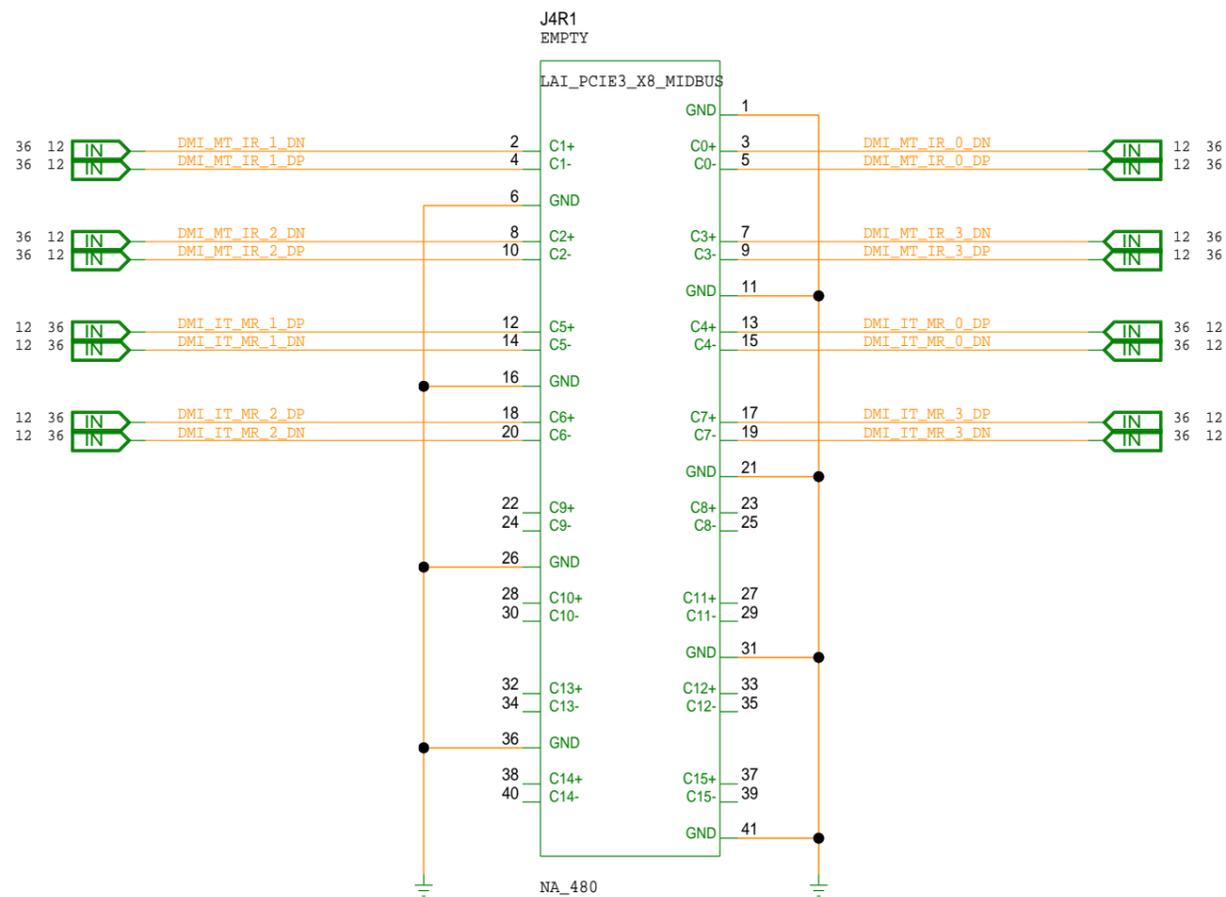
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CAD NOTE:

REMOVE THIS FOOTPRINT FROM THE SECONDARY SOLDERPASTE LAYER

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CUSTOM TEXT BPAGE

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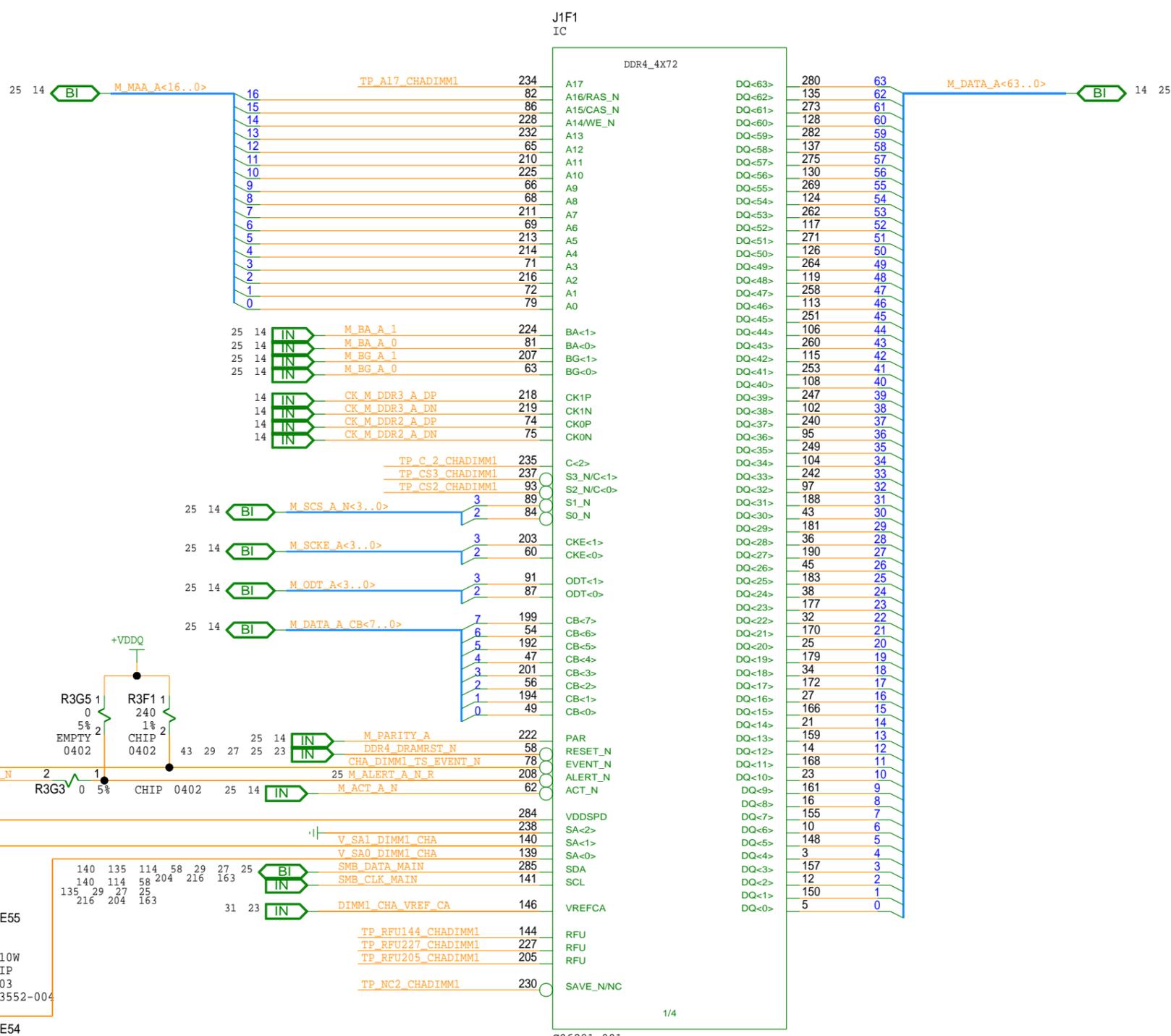
MODULE NAME	REV	DATE

DESIGN NOTE:

SPD ADDRESS FOR CHANNEL-A DIMM1 :
 WRITE ADDRESS: 0XA2
 READ ADDRESS: 0XA3
 SA0 =1; SA1 = 0

DDR4 POR OPERATING SPEED: XX00 MT/S

'EVENT_N': INDICATES THERMAL EVENT ON DIMM.



CAD NOTE:

PLACE THE CAP WITHIN 200 MILS FROM THE DIMM -1

CAD NOTE:

PLACE THE CAP CLOSE TO DIMM

CAD NOTE:

TRIPAD

CAD NOTE:

USE 3 PAD

CAD NOTE:

USE 3 PAD

BPAGE DRAWING

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MODULE REV DETAILS

MODULE NAME	REV	DATE

DESIGN NOTE:

SPD ADDRESS FOR CHANNEL-0 :
 WRITE ADDRESS: 0XA0
 READ ADDRESS: 0XA1
 SA0 = 0; SA1 = 0
 DDR4 POR OPERATING SPEED: XX00 MT/S
 'EVENT_N': INDICATES THERMAL EVENT ON DIMM.

CAD NOTE:

PLACE THE CAP WITHIN 200 MILS FROM THE DIMM -1

CAD NOTE:

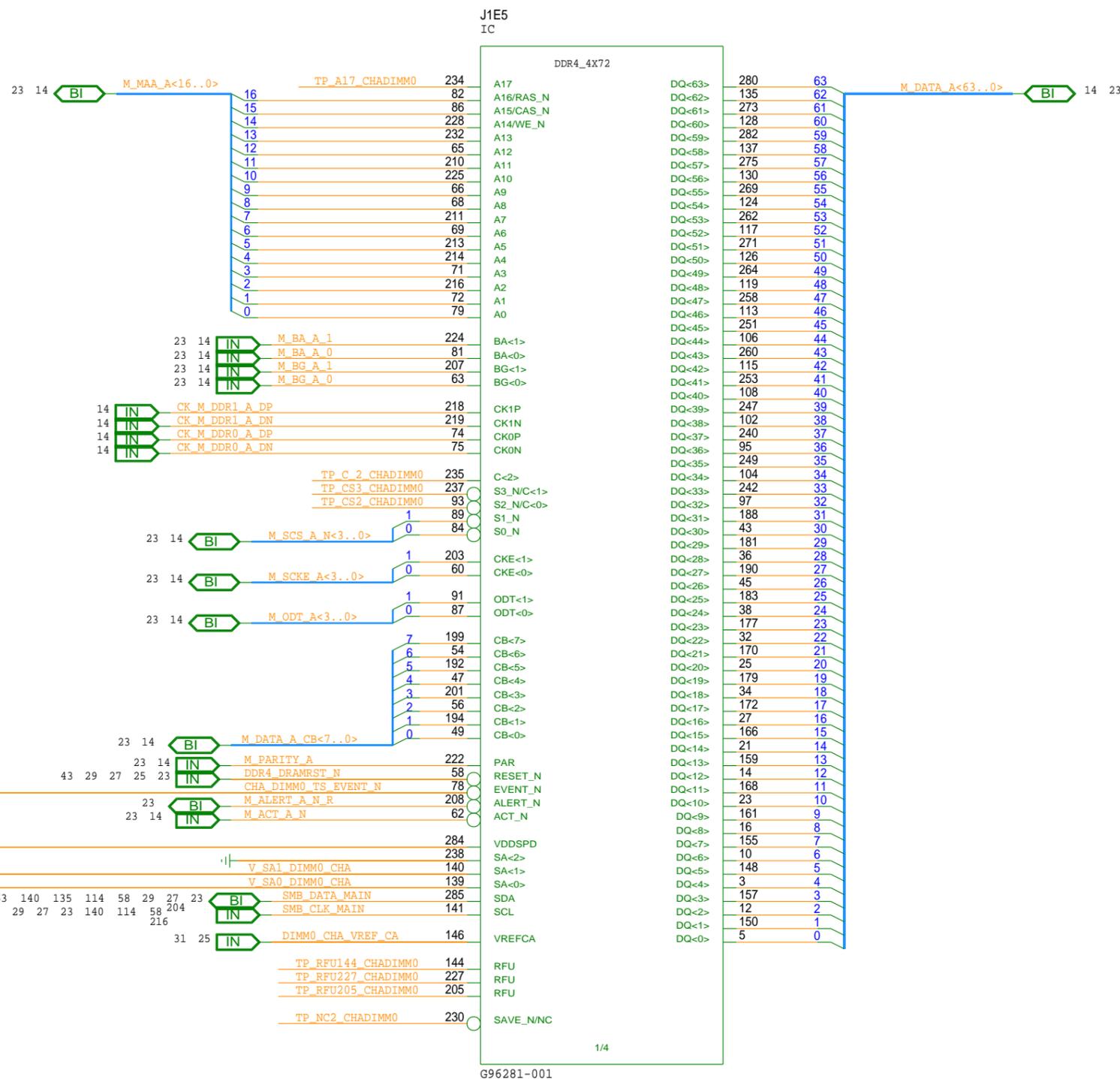
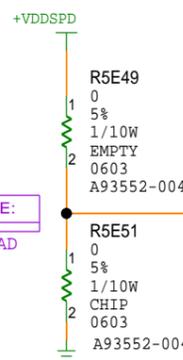
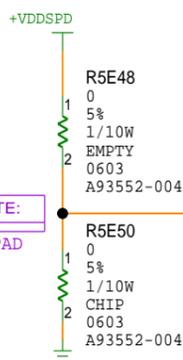
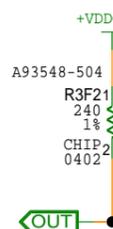
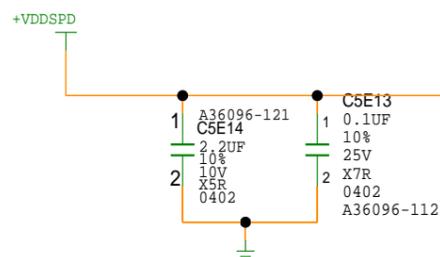
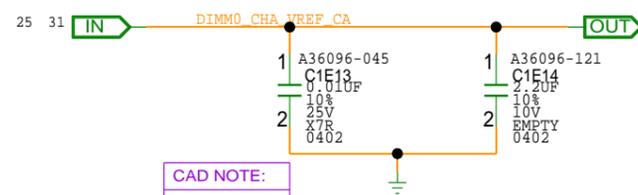
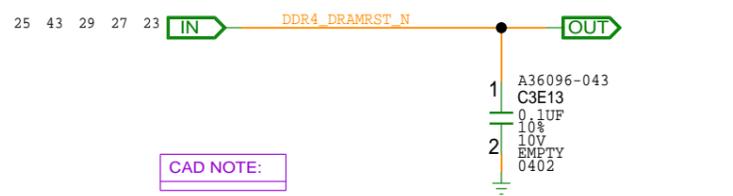
PLACE THE CAP CLOSE TO DIMM

CAD NOTE:

USE 3 PAD

CAD NOTE:

USE 3 PAD



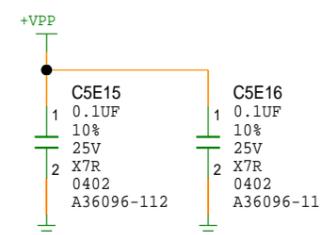
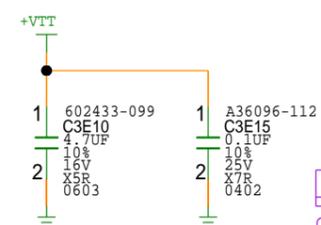
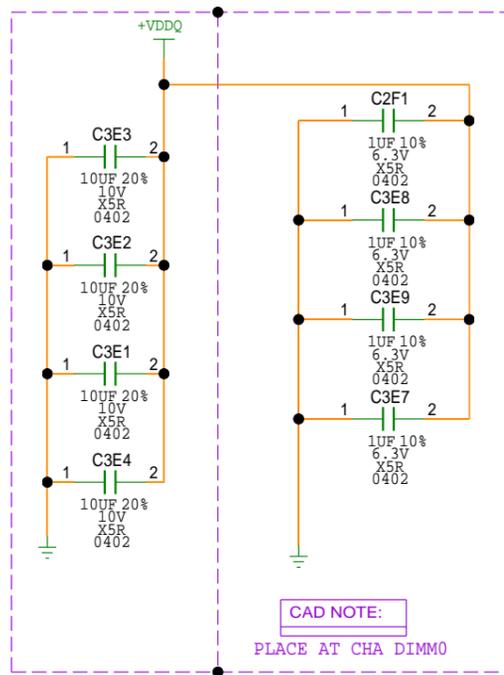
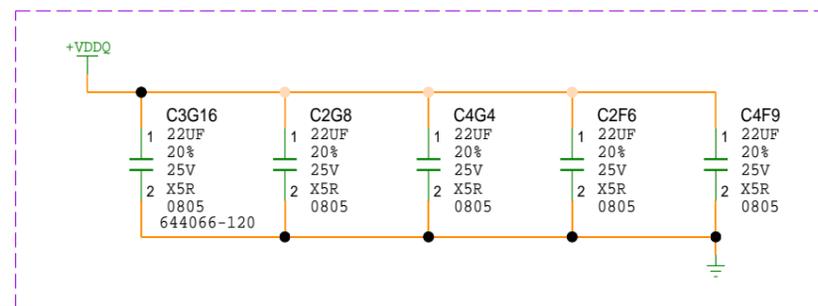
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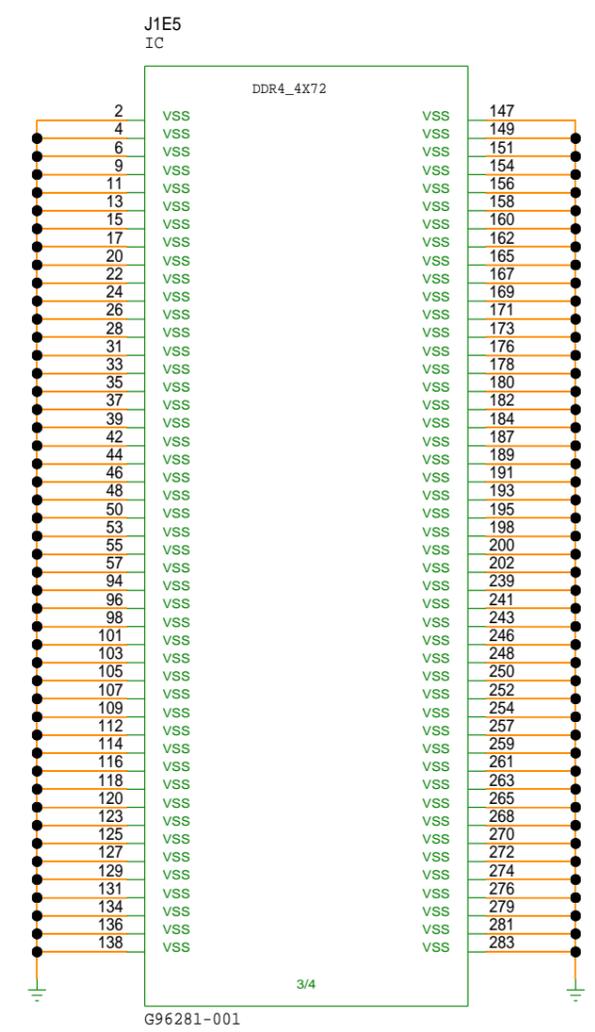
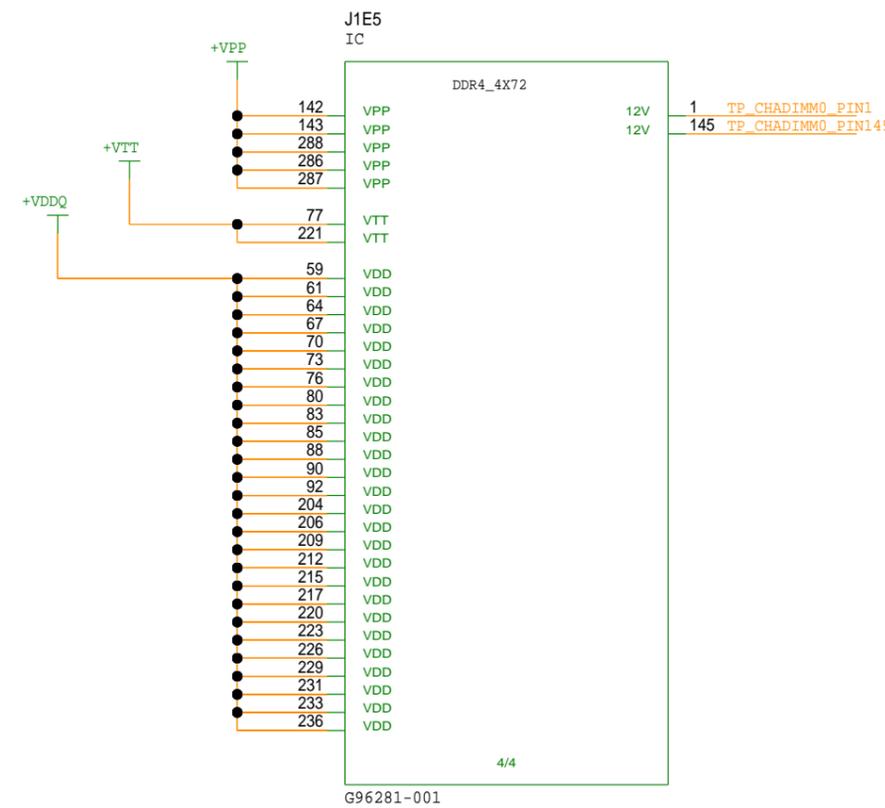
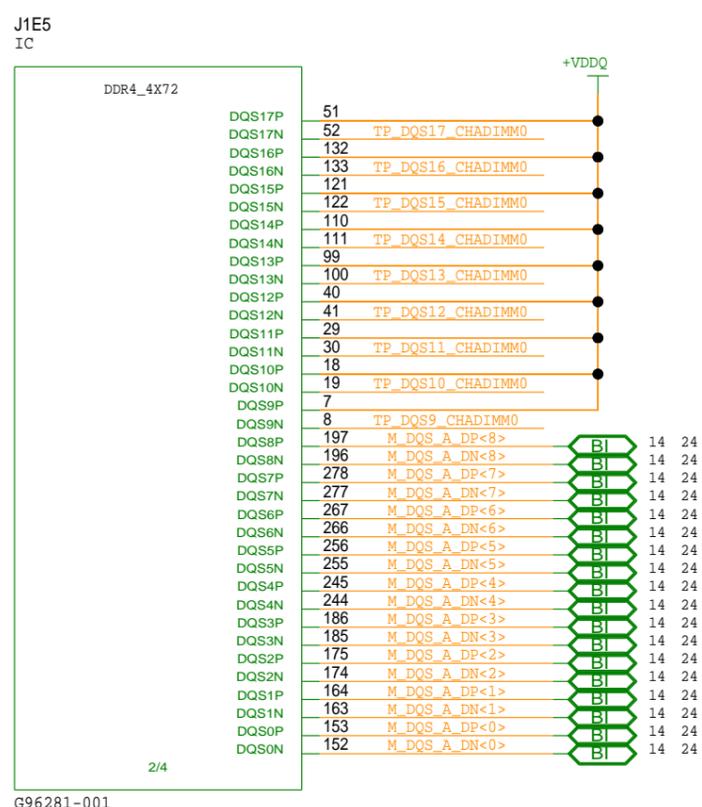
MODULE REV DETAILS

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DESIGN NOTE:
CH A VDDQ_VTT DECOUPLING CAPS

CAD NOTE:
PLACE AT CHA DIMMO



MODULE REV DETAILS

MODULE NAME	REV	DATE

DESIGN NOTE:

SPD ADDRESS FOR CHANNEL-0 :
 WRITE ADDRESS: 0XA6
 READ ADDRESS: 0XA7
 SA0 =1; SA1 = 1.
 DDR4 POR OPERATING SPEED: XX00 MT/S
 'EVENT_N': INDICATES THERMAL EVENT ON DIMM.

CAD NOTE:

PLACE THE CAP WITHIN 200 MILS FROM THE DIMM - 1

CAD NOTE:

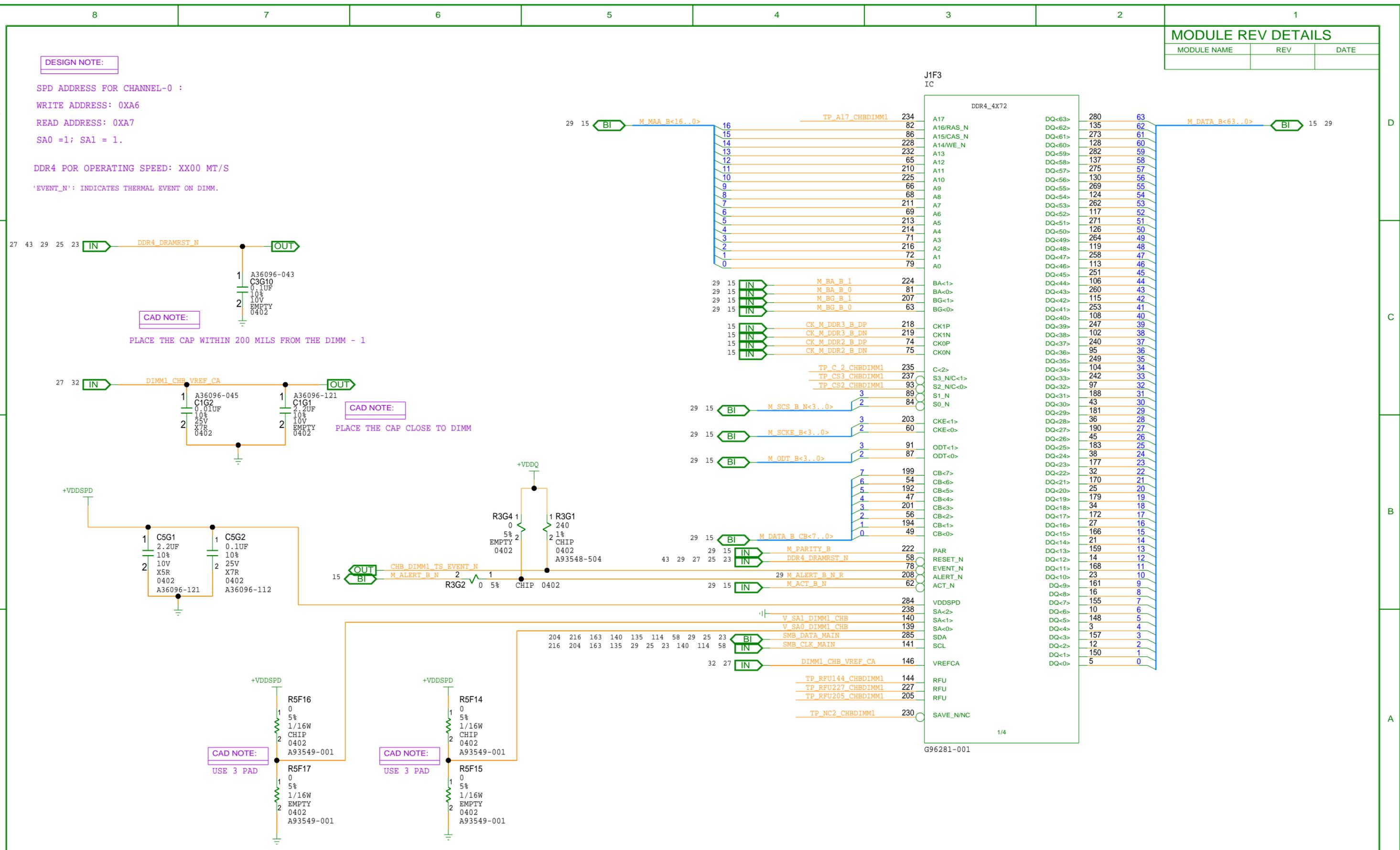
PLACE THE CAP CLOSE TO DIMM

CAD NOTE:

USE 3 PAD

CAD NOTE:

USE 3 PAD



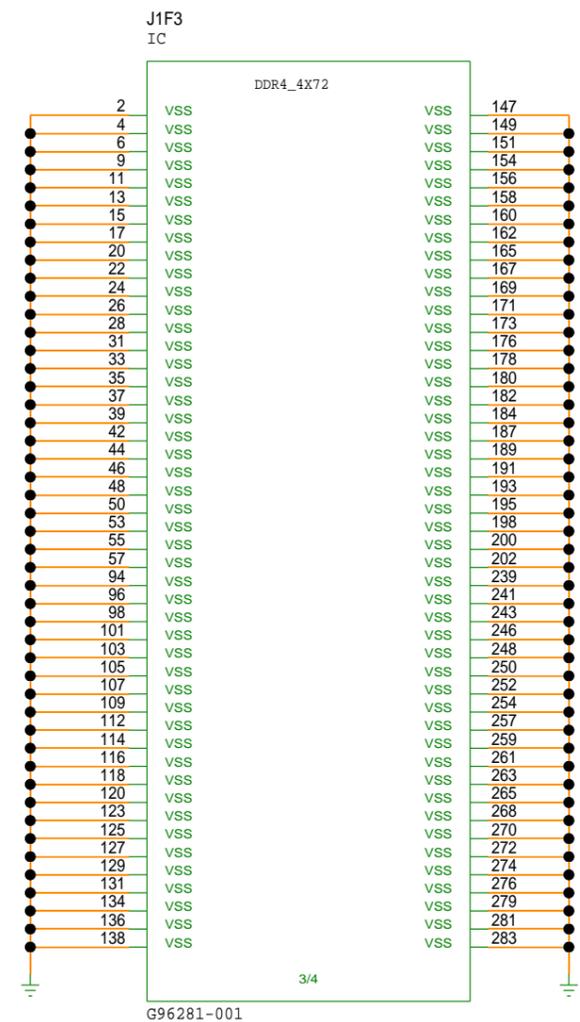
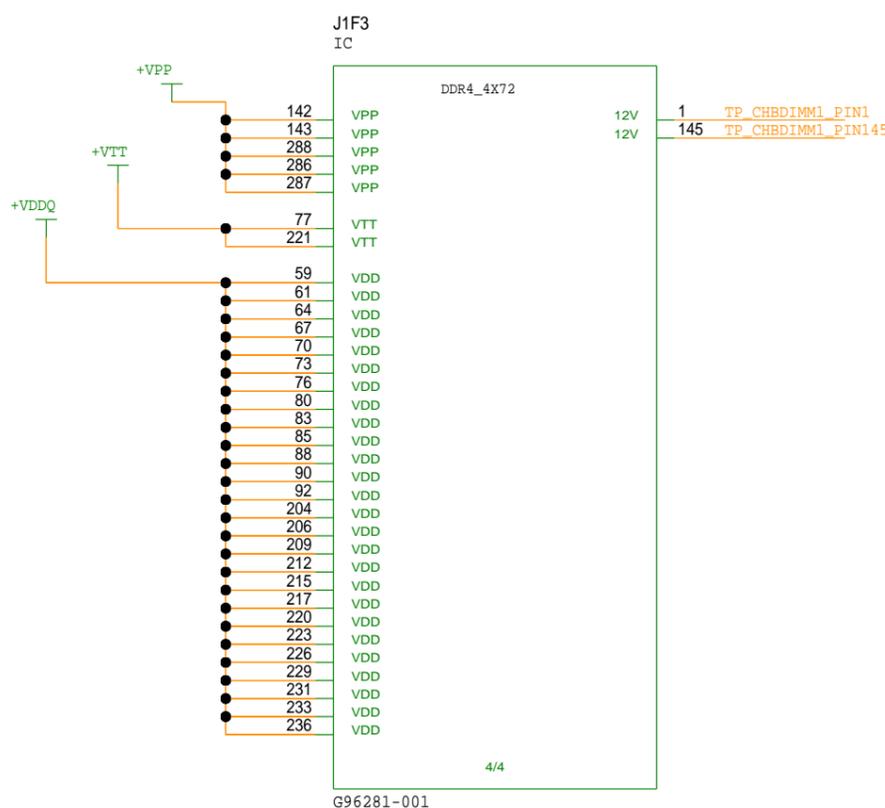
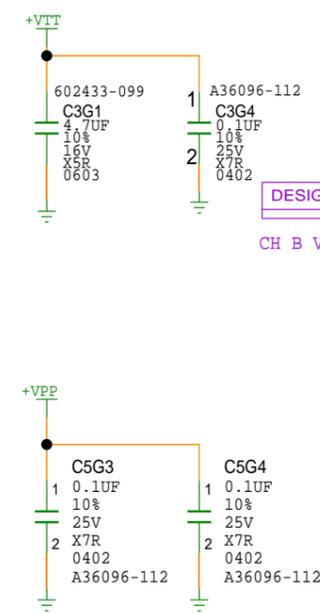
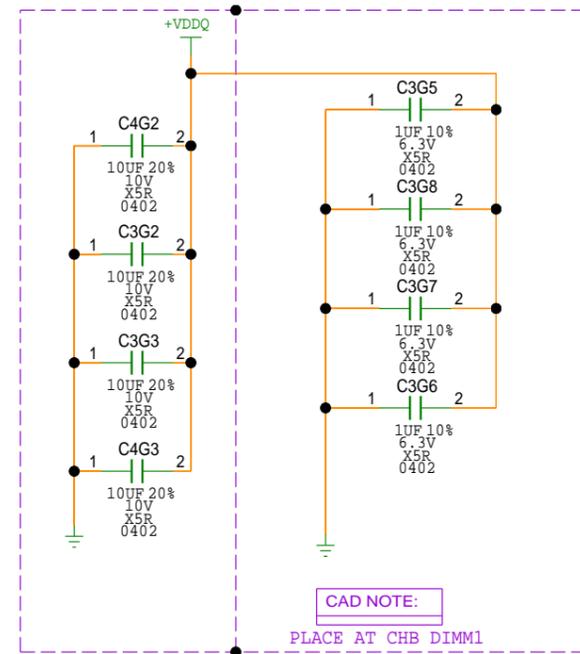
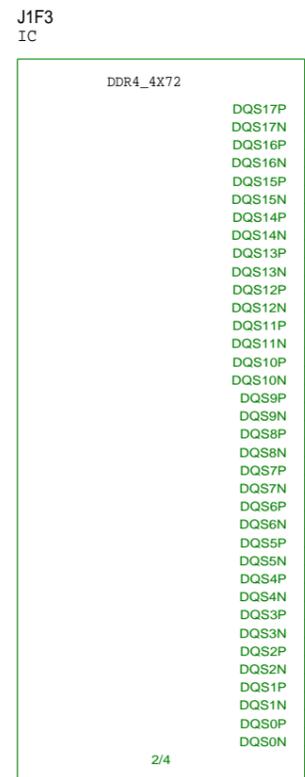
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MODULE REV DETAILS

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DESIGN NOTE:

SPD ADDRESS FOR CHANNEL-0 :
 WRITE ADDRESS: 0XA4
 READ ADDRESS: 0XA5
 SA0 = 0; SA1 = 1

 DDR4 POR OPERATING SPEED: XX00 MT/S
 'EVENT_N': INDICATES THERMAL EVENT ON DIMM.

CAD NOTE:

PLACE THE CAP WITHIN 200 MILS FROM THE DIMM - 0

CAD NOTE:

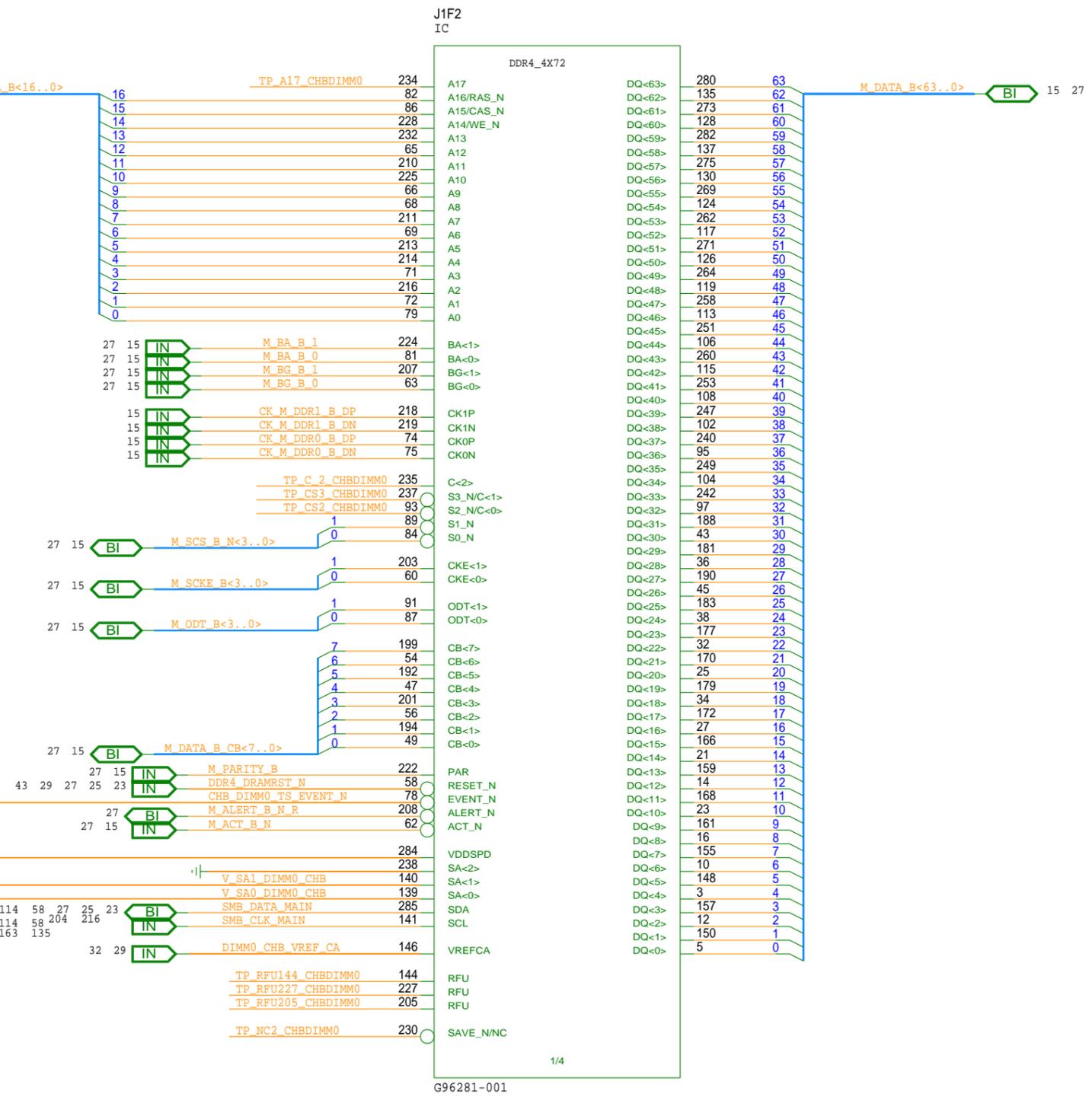
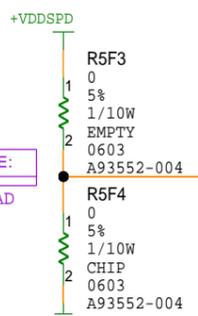
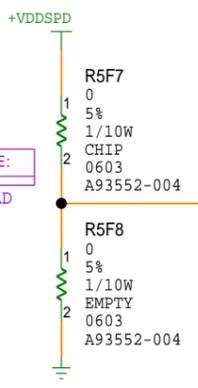
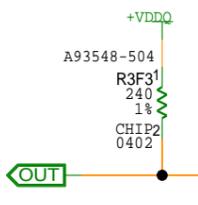
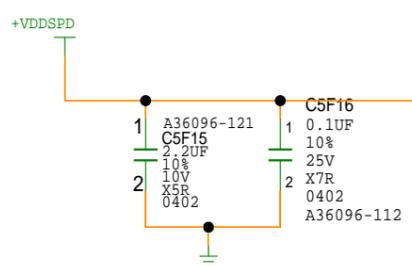
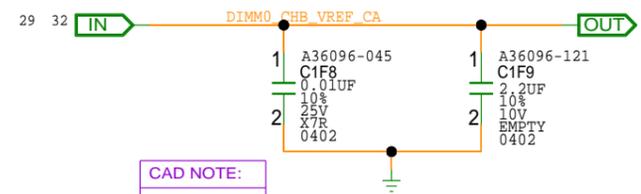
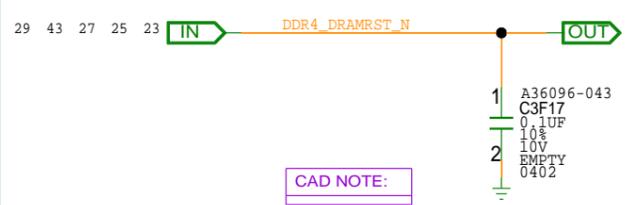
PLACE THE CAP CLOSE TO DIMM

CAD NOTE:

USE 3 PAD

CAD NOTE:

USE 3 PAD



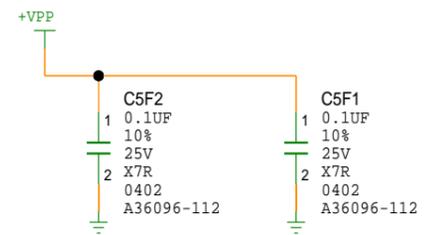
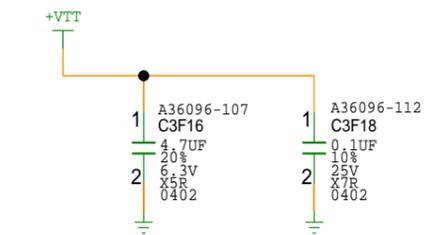
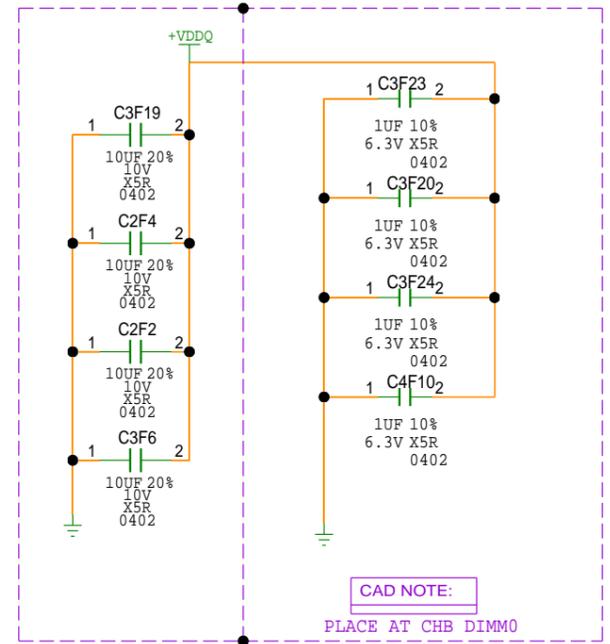
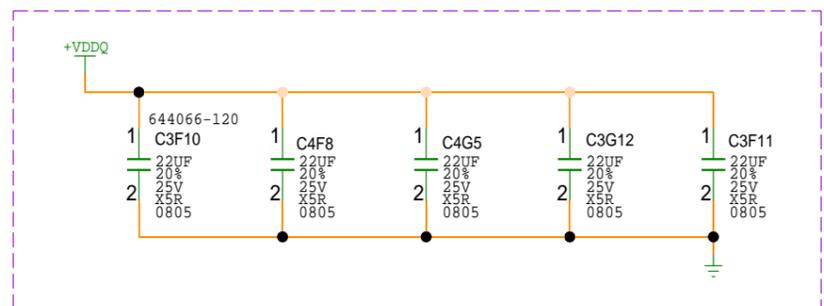
BPAGE DRAWING

udimm_sch_1.29
 Fri Sep 27 16:39:38 2019

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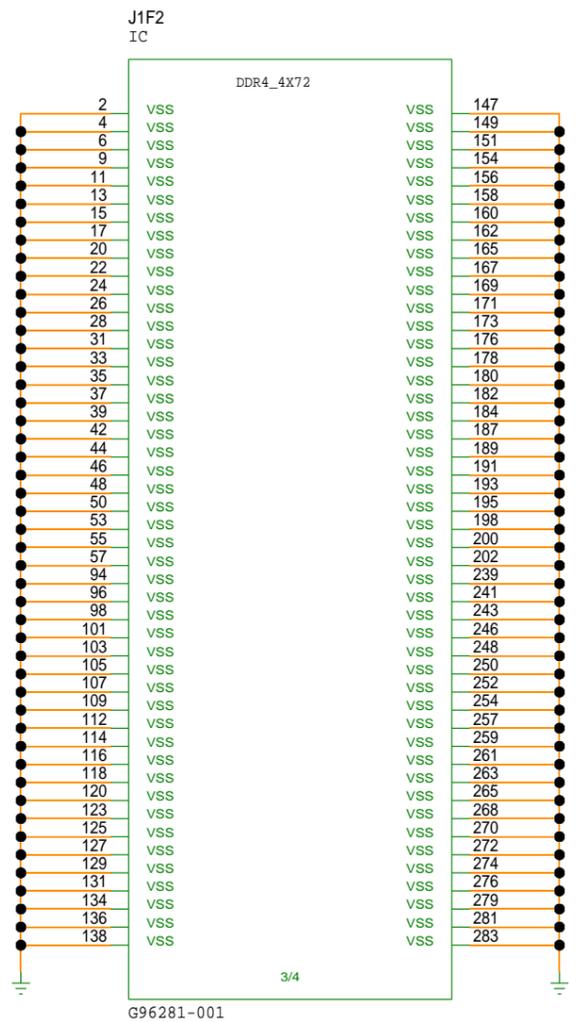
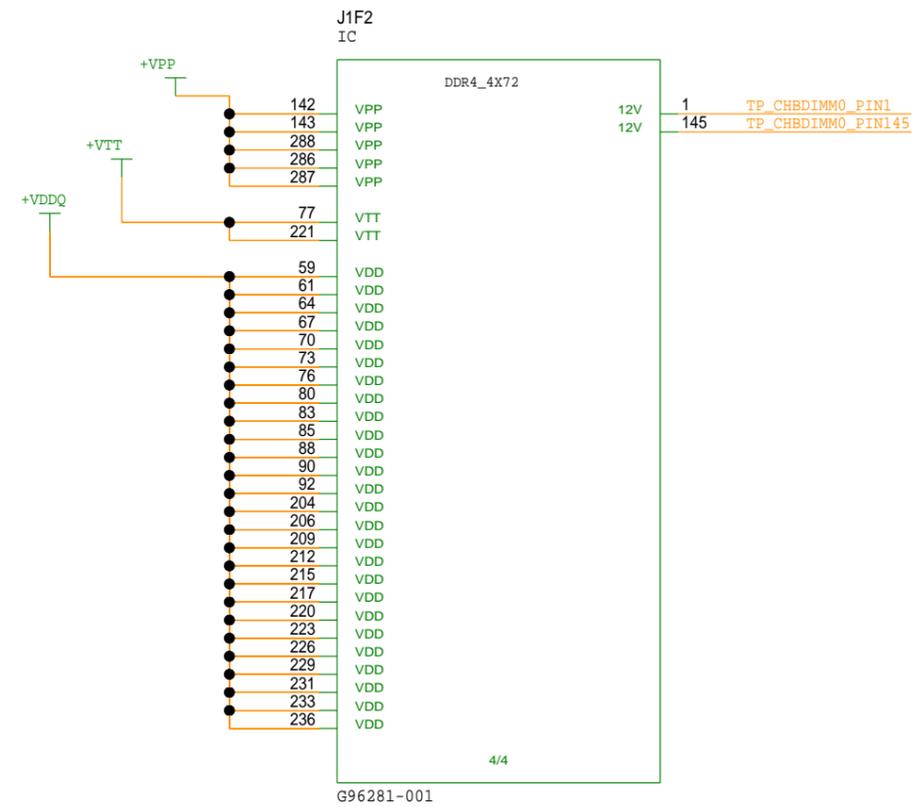
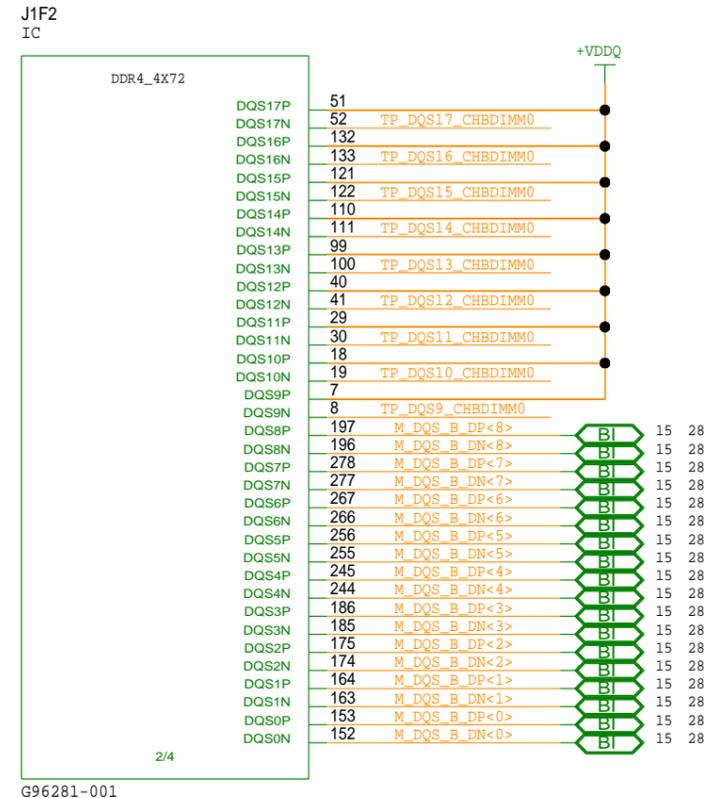
MODULE REV DETAILS

MODULE NAME	REV	DATE



DESIGN NOTE:
CH B VDDQ_VIT DECOUPLING CAPS

CAD NOTE:
PLACE AT CHB DIMM0

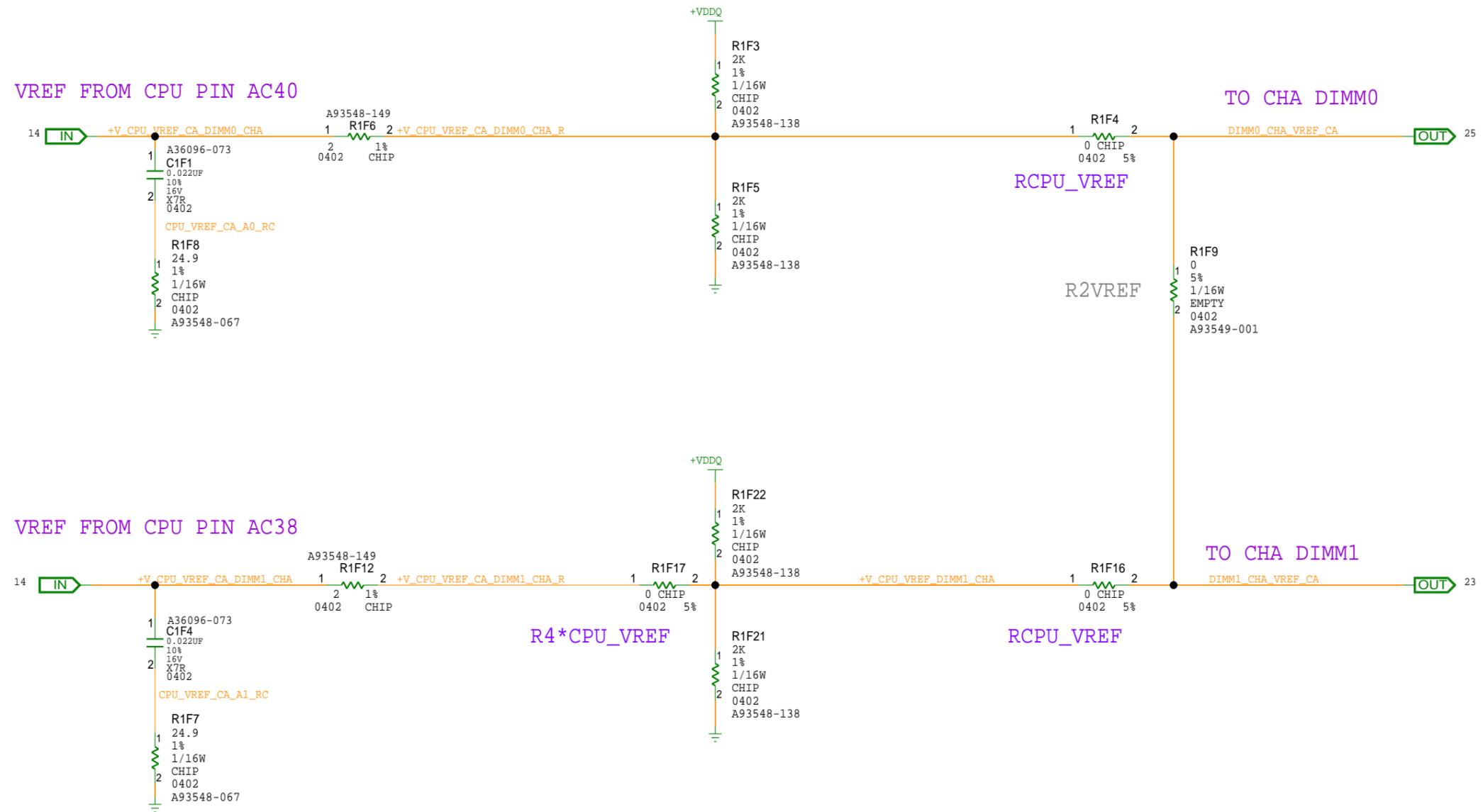


BPAGE DRAWING
udimm.sch.1.30
Fri Sep 27 16:39:39 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 30	REV 0.7
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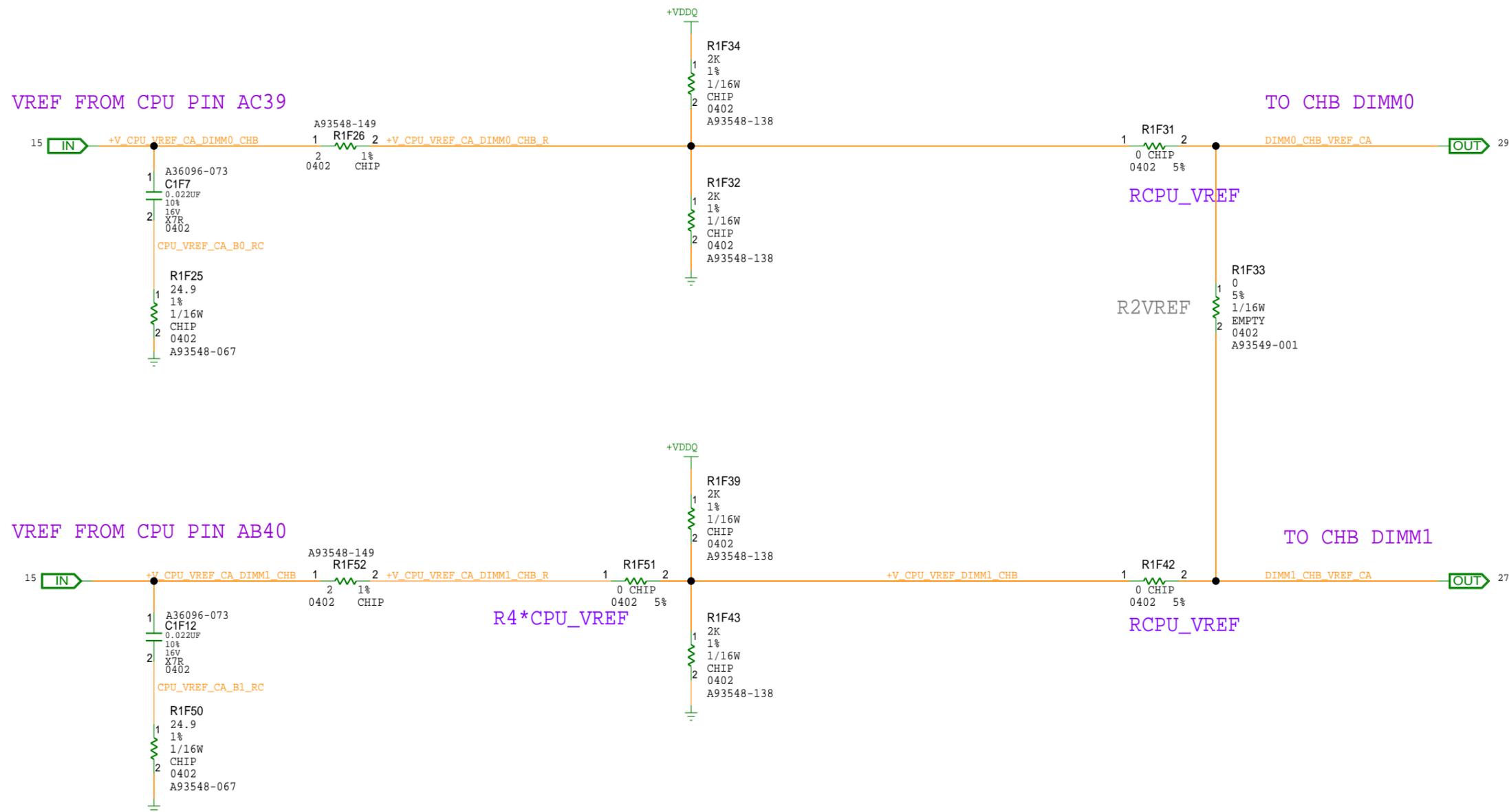
MODULE REV DETAILS

MODULE NAME	REV	DATE



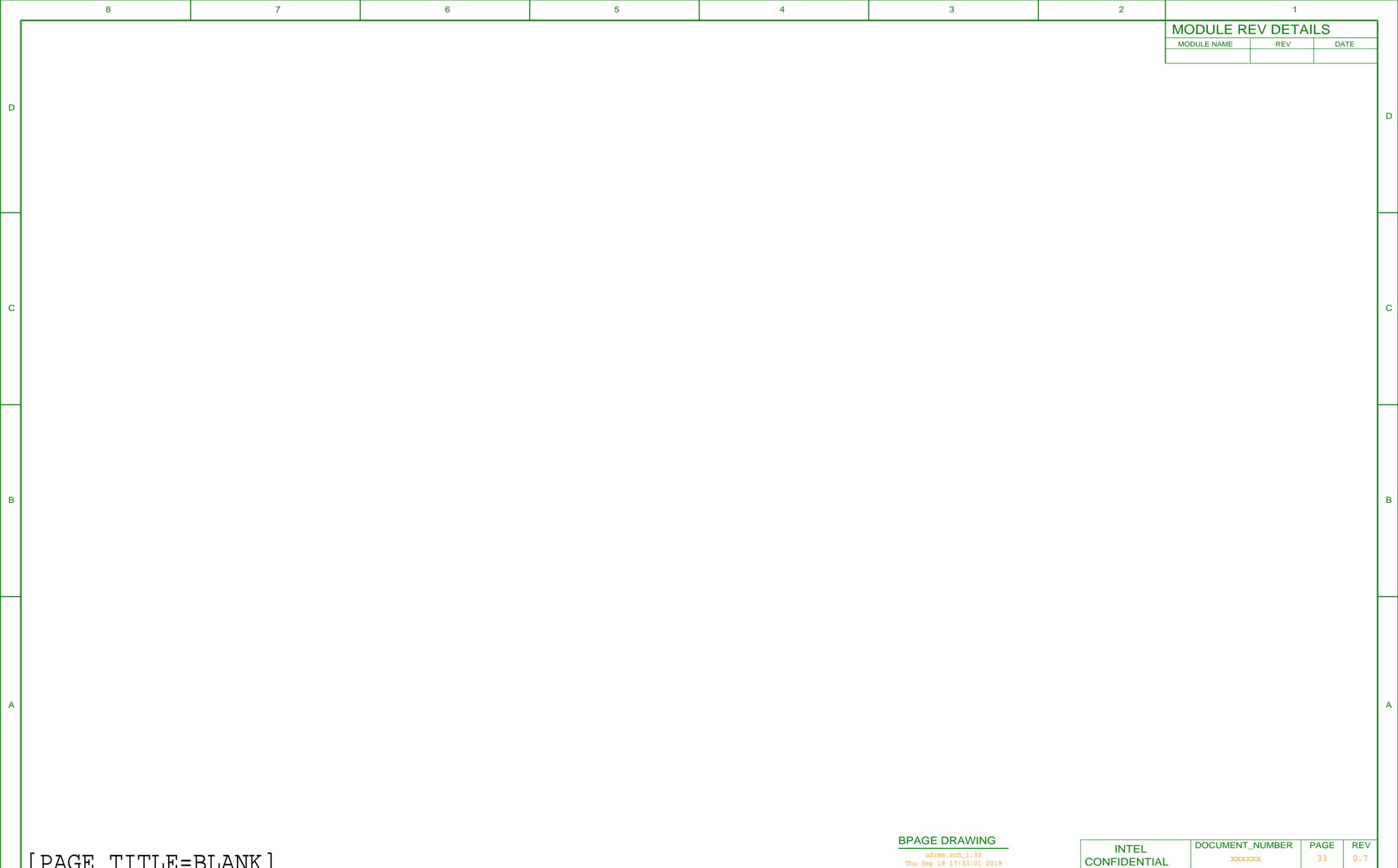
MODULE REV DETAILS

MODULE NAME	REV	DATE



MODULE REV DETAILS

MODULE NAME	REV	DATE



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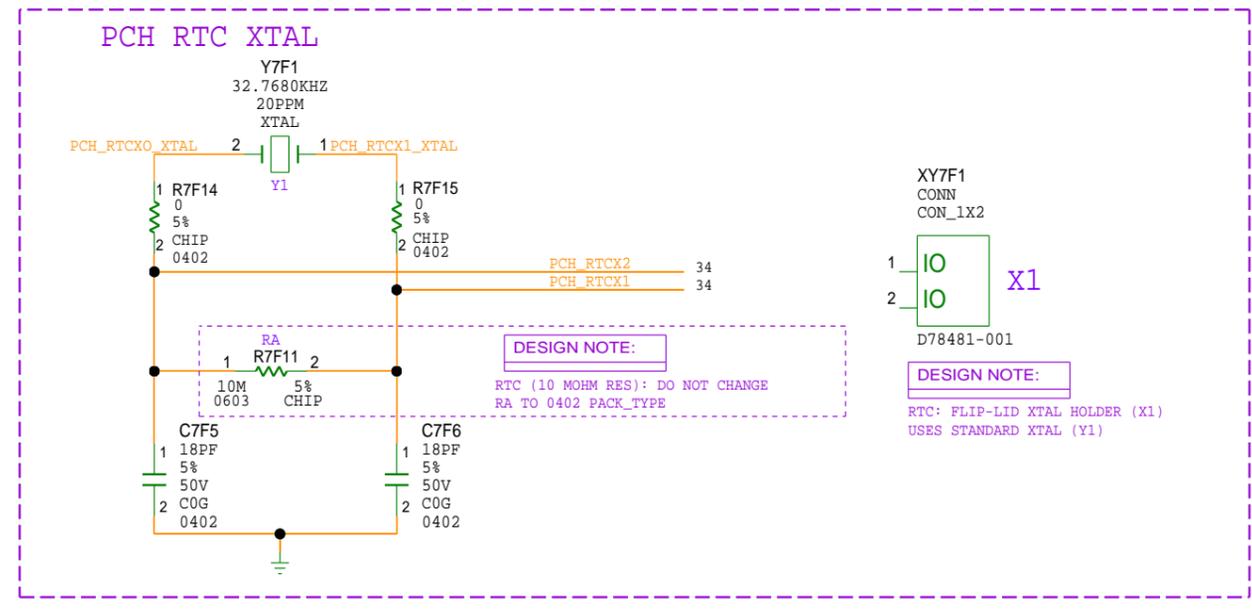
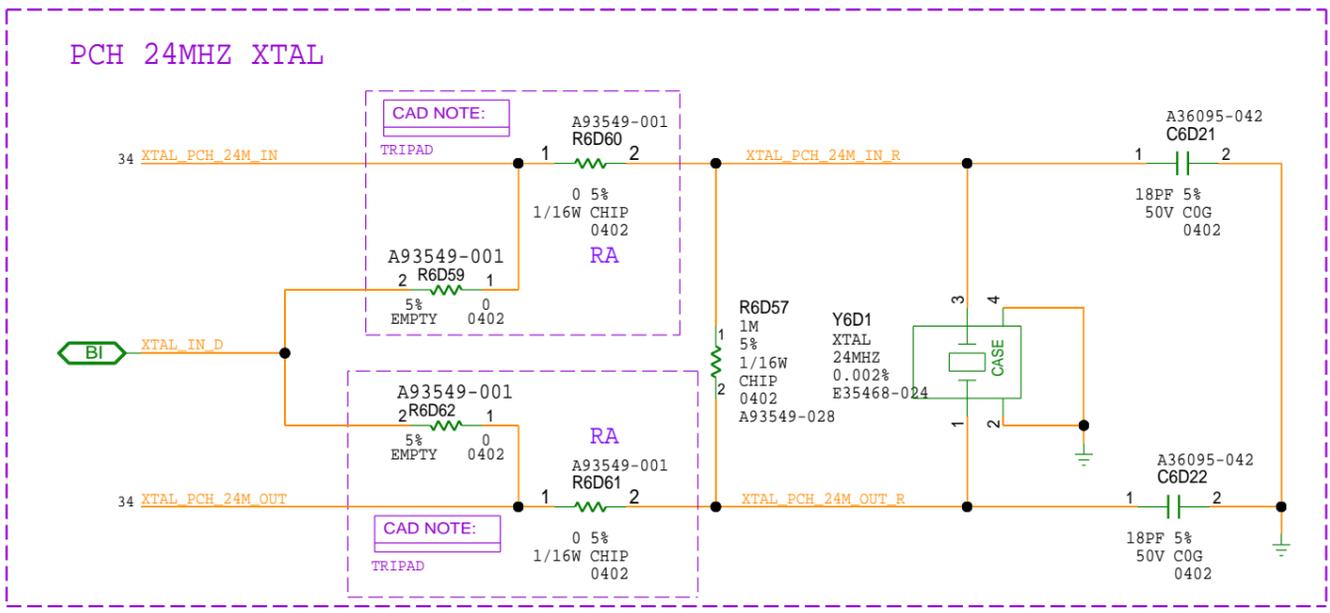
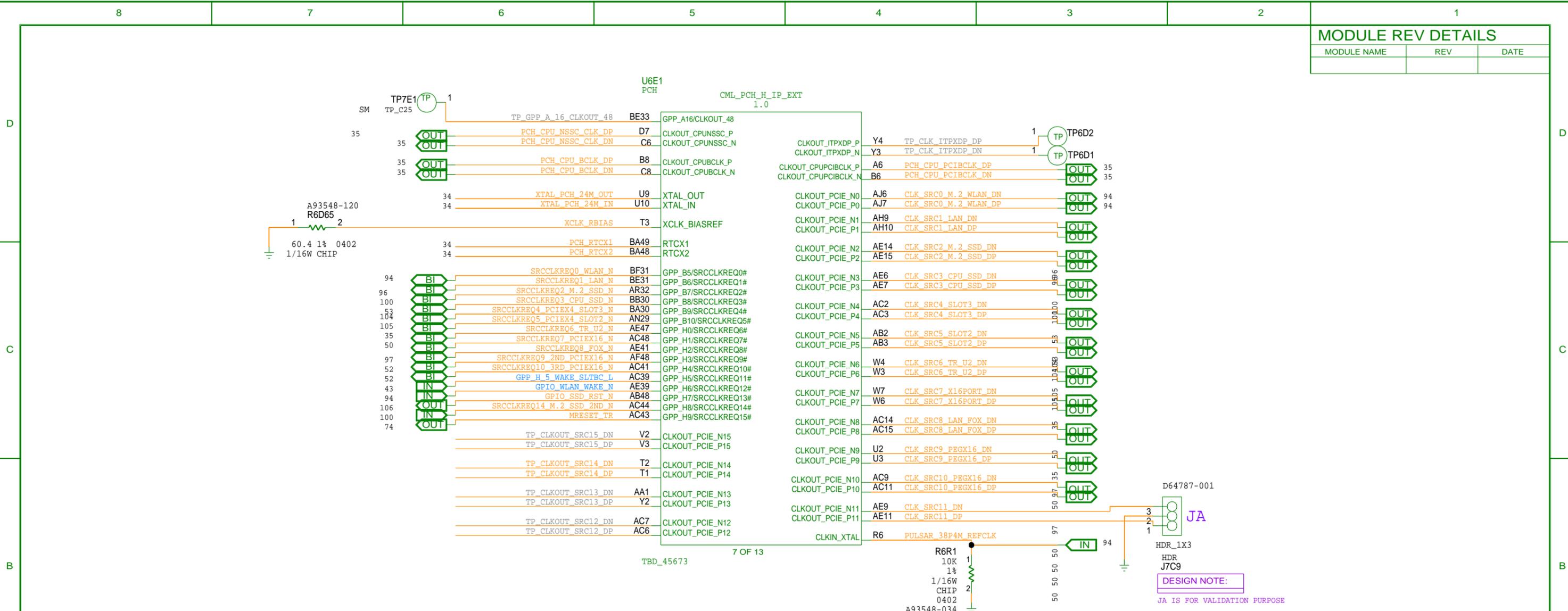
BPAGE DRAWING

udimm.sch_1.33
Thu Sep 19 17:33:01 2019

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MODULE REV DETAILS

MODULE NAME	REV	DATE



[PAGE_TITLE=CMP PCH H CLOCK]

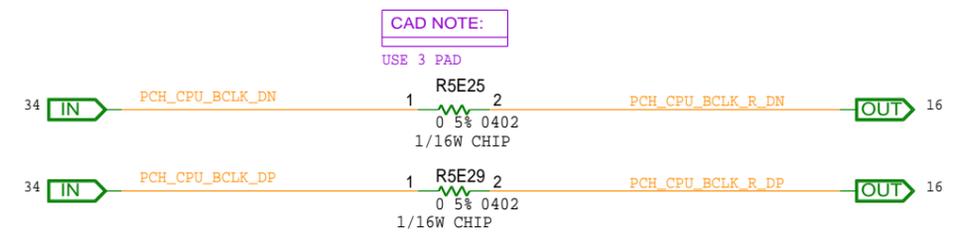
BPAGE DRAWING

udimm.sch_1.34
Tue Oct 01 09:57:35 2019

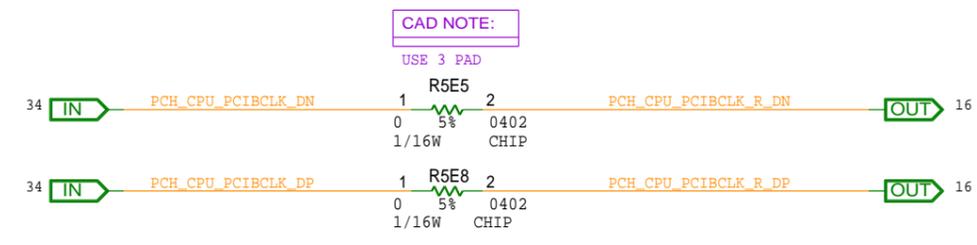
INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 34	REV 0.7
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MODULE REV DETAILS		
MODULE NAME	REV	DATE

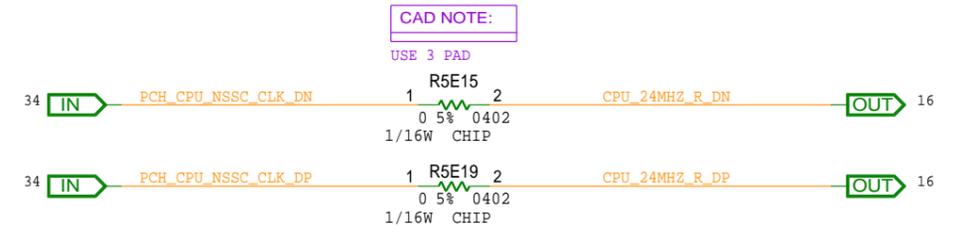
CPU BCLK OPTIONS



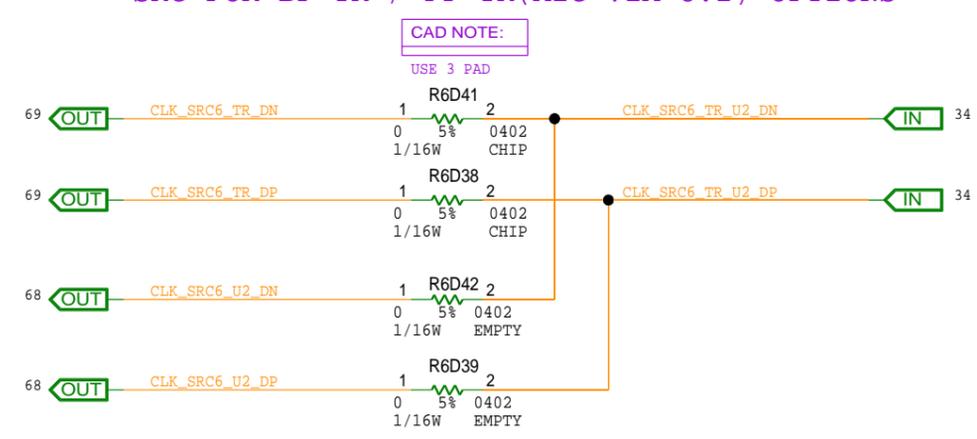
CPU PCIBCLK OPTIONS



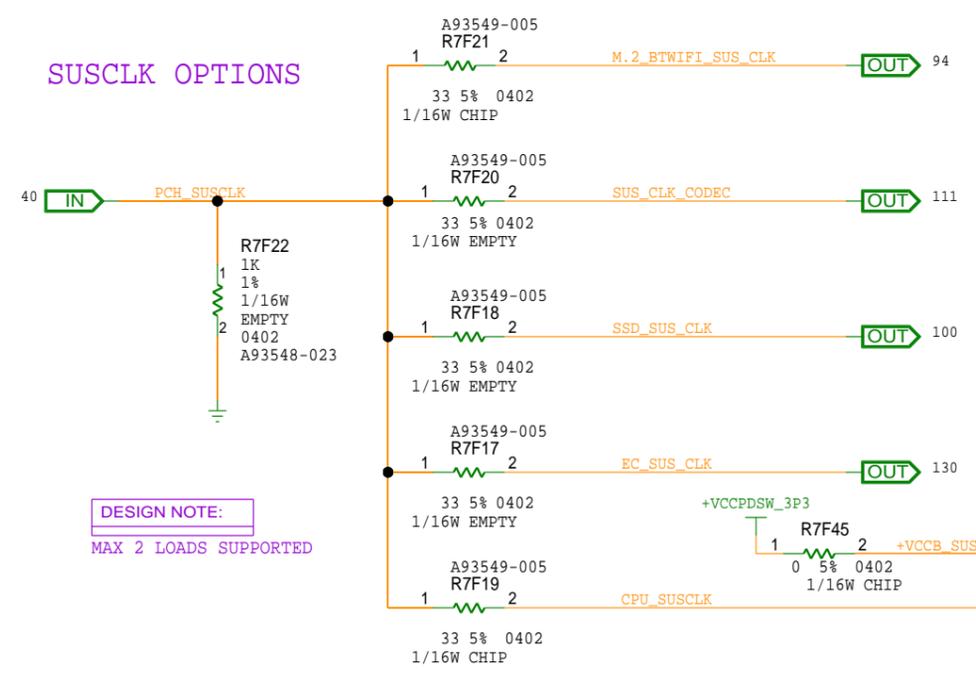
CPU NSSC CLK OPTIONS



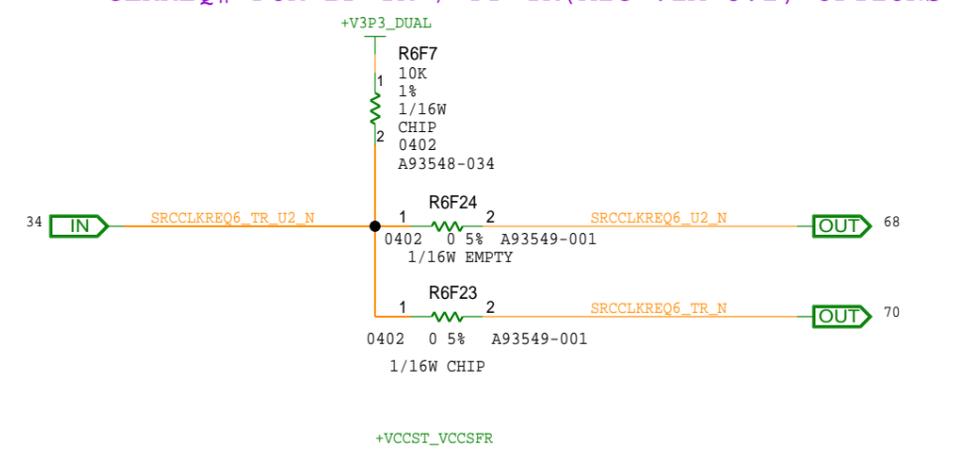
SRC FOR BP TR / FP TR(AIC VIA U.2) OPTIONS



SUSCLK OPTIONS



CLKREQ# FOR BP TR / FP TR(AIC VIA U.2) OPTIONS



MODULE REV DETAILS

MODULE NAME	REV	DATE



USB3.1 TYPE-A BP STACK1
USB2 P1:2

USB3.1 TYPE-A BP STACK1
USB2 P3:4

USB3.1 TYPE-A BP STACK2
USB2 P5:6

BP USBC P7

USB3.1 TYPE-A VERITCAL P8

USB3.1 TYPE-C FP P9

USB3.1 TYPE-A FP P10&13

USB2.0 FP

USB3.1 TYPE-A FP P10&13

M.2 BT

USB3.1 TYPE-A BACK PANEL
PORT 4&7

USB3.1 FRONT PANEL
PORT 5&8

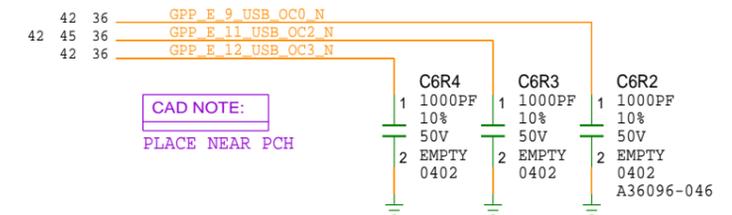
FOXVILLE LAN
PCIE P3

M.2 WLAN
PCIE P4

TR/U.2 CO-LAYOUT
PCIE P5:8

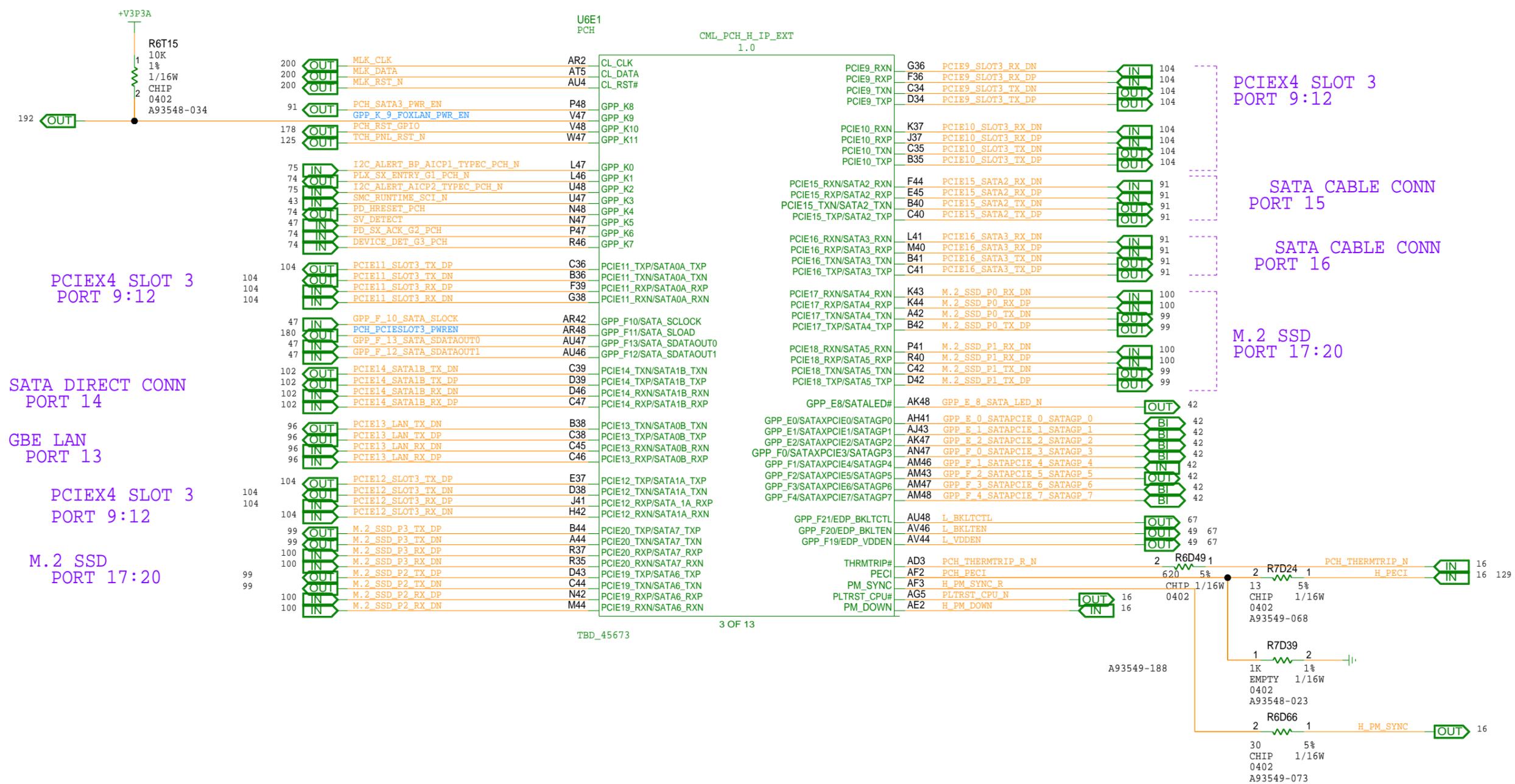
CAD NOTE:
USB2 COMP RES:
PLACE WITHIN 1 INCH

PCIEX4 SLOT2
PCIE P21:24



MODULE REV DETAILS

MODULE NAME	REV	DATE



PCIEX4 SLOT 3 PORT 9:12

SATA DIRECT CONN PORT 14

GBE LAN PORT 13

PCIEX4 SLOT 3 PORT 9:12

M.2 SSD PORT 17:20

PCIEX4 SLOT 3 PORT 9:12

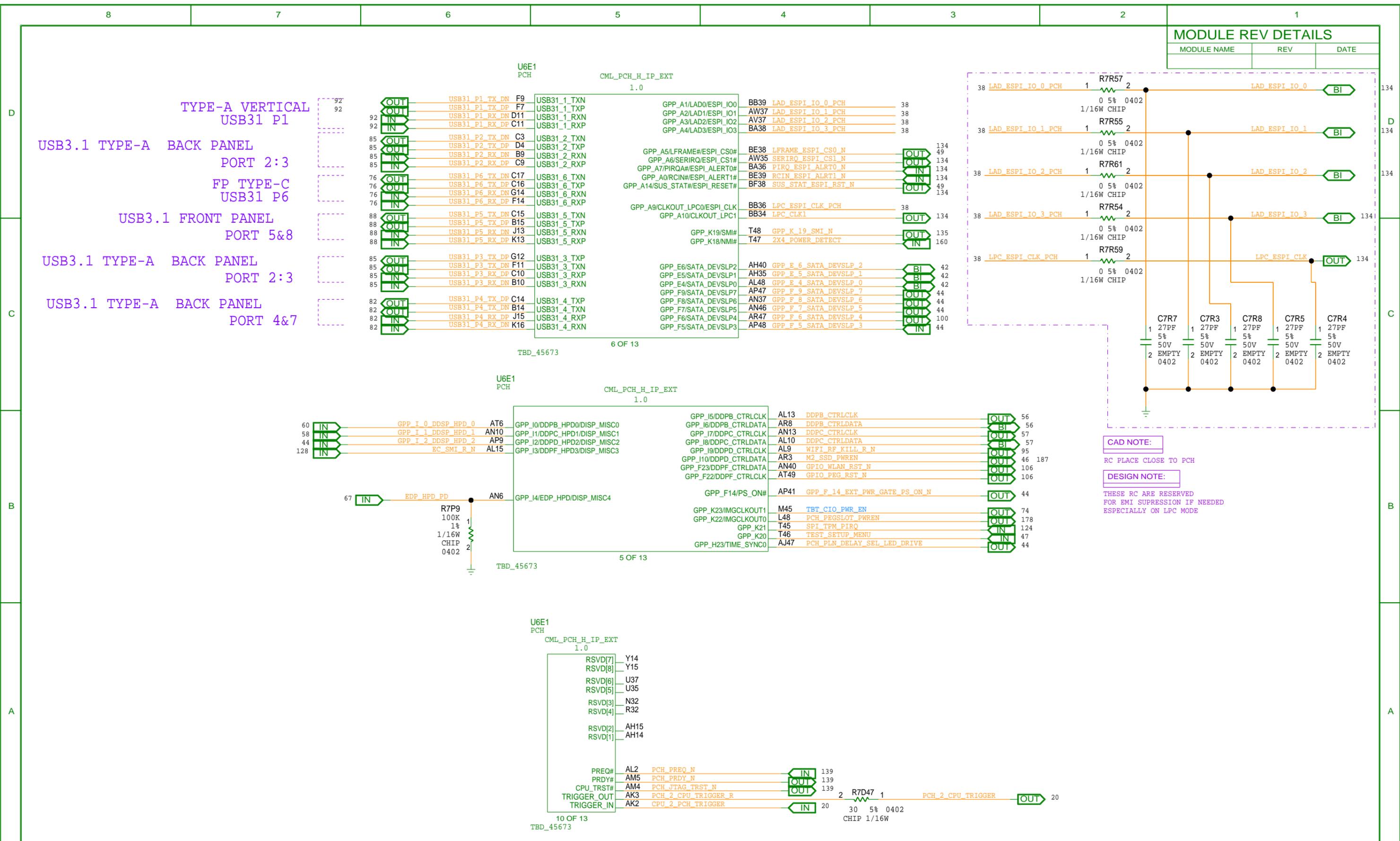
SATA CABLE CONN PORT 15

SATA CABLE CONN PORT 16

M.2 SSD PORT 17:20

MODULE REV DETAILS

MODULE NAME	REV	DATE



CAD NOTE:
RC PLACE CLOSE TO PCH

DESIGN NOTE:
THESE RC ARE RESERVED FOR EMI SUPPRESSION IF NEEDED ESPECIALLY ON LPC MODE

BPAGE DRAWING

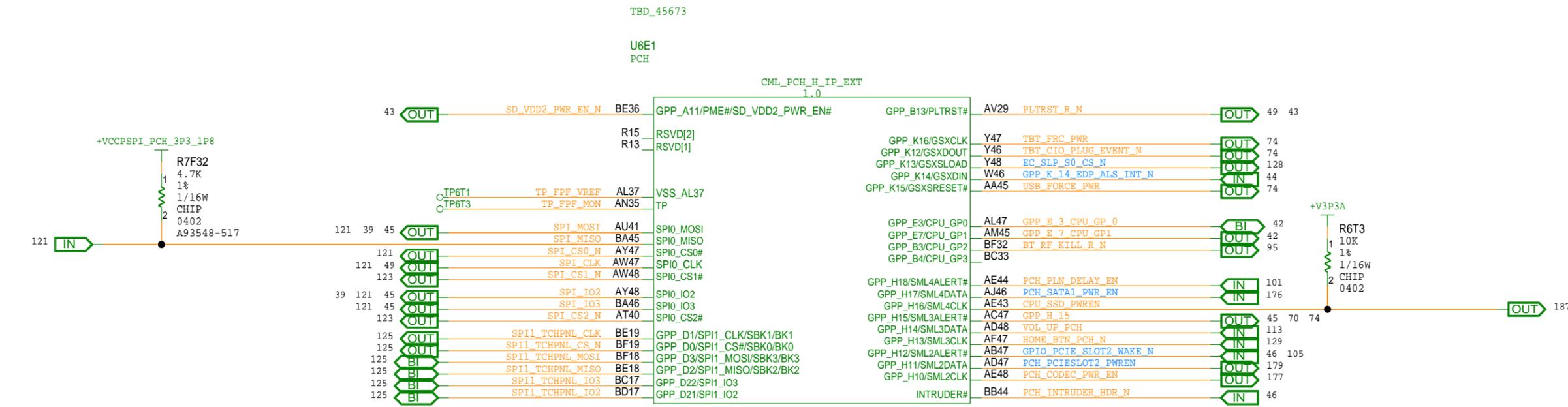
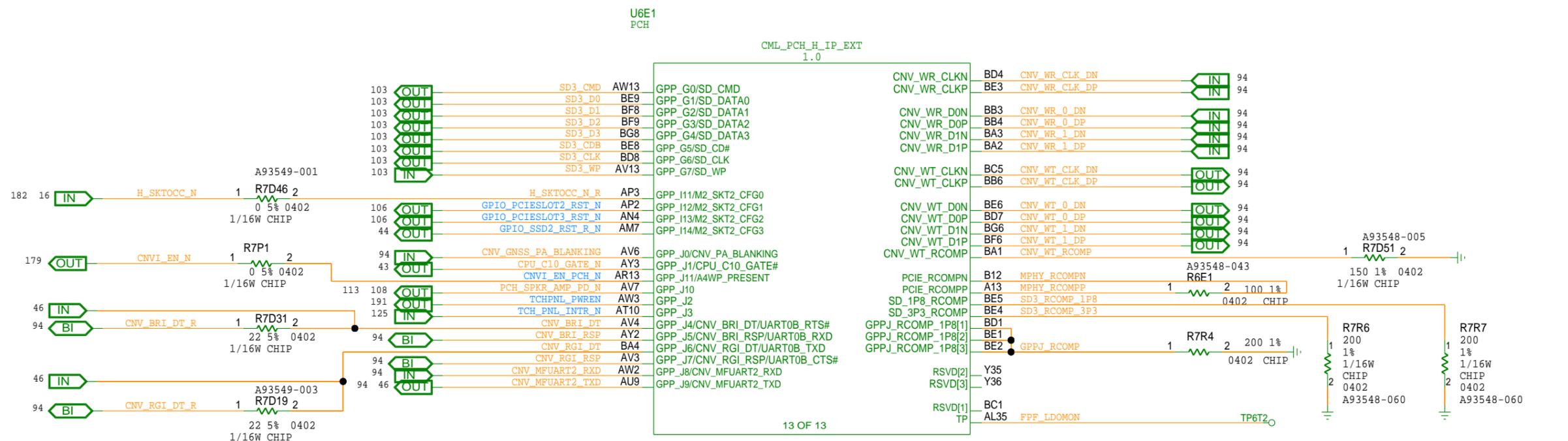
udimm.sch_1.38
Fri Sep 27 16:39:47 2019

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[PAGE_TITLE=CML PCH H USB3 GPIOA/E/F/I/J]

MODULE REV DETAILS

MODULE NAME	REV	DATE



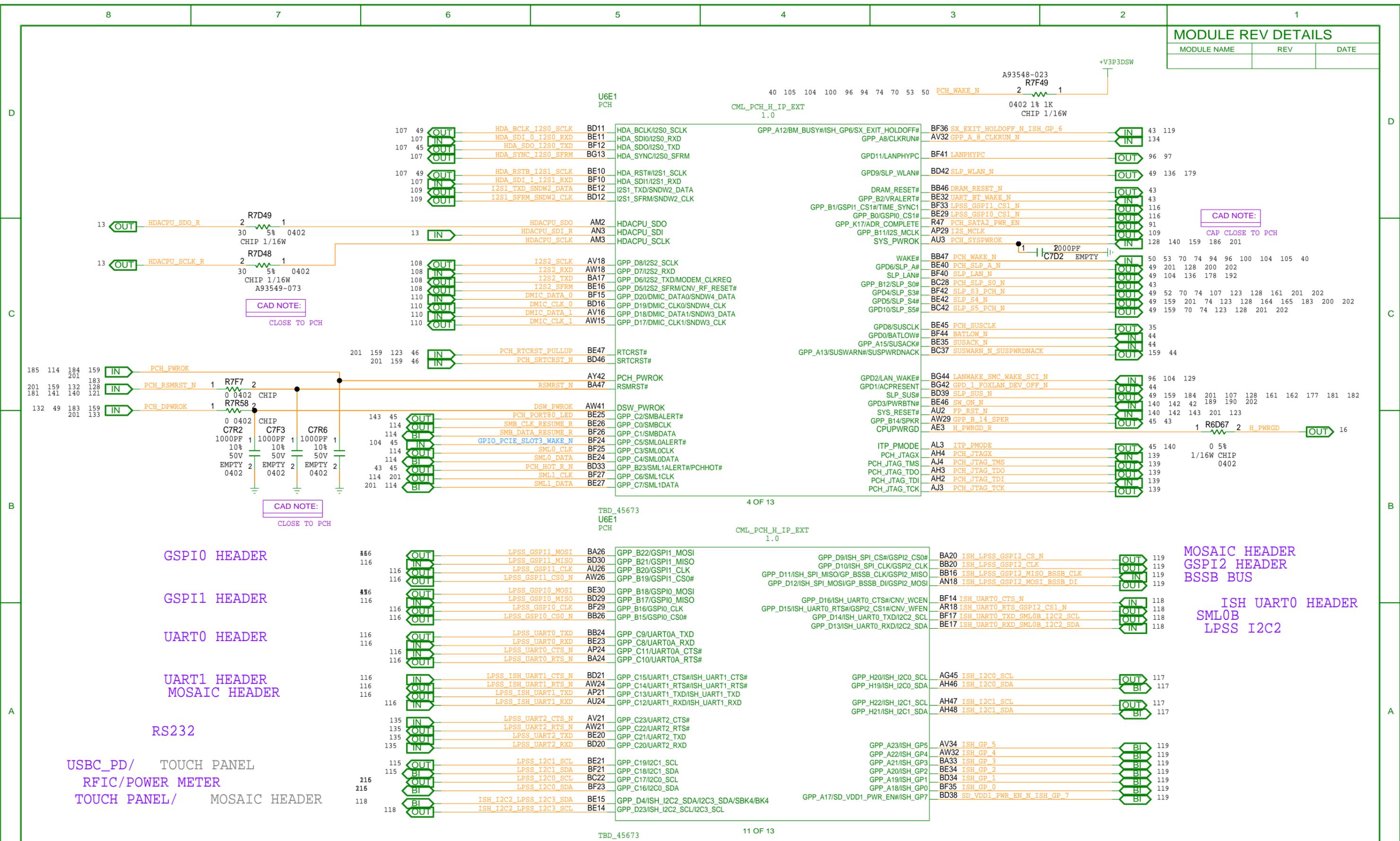
[PAGE_TITLE=CML_PCH_H_CNVI_SD_SPI_GPIOH/I/J]

BPAGE DRAWING
udimm.sch_1.39
Fri Sep 27 16:39:48 2019

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MODULE REV DETAILS

MODULE NAME	REV	DATE



GSPI0 HEADER

GSPI1 HEADER

UART0 HEADER

UART1 HEADER
MOSAIC HEADER

RS232

USBC_PD/ TOUCH PANEL
RFIC/POWER METER
TOUCH PANEL/ MOSAIC HEADER

MOSAIC HEADER
GSPI2 HEADER
BSSB BUS

ISH UART0 HEADER
SML0B
LPSS I2C2

TBD_45673 11 OF 13

BPAGE DRAWING

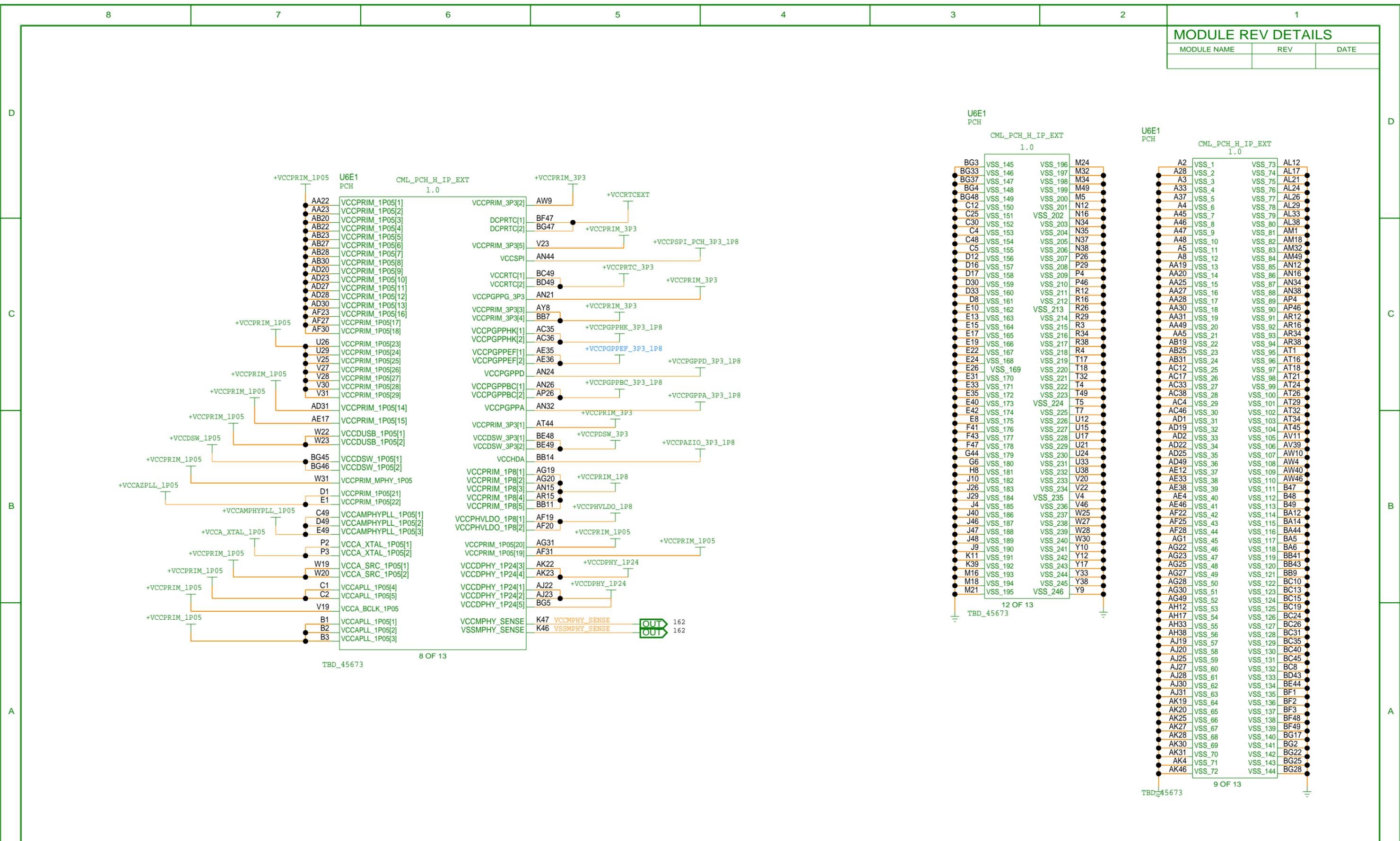
udimm.sch_1.40
Tue Oct 01 09:43:48 2019

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[PAGE_TITLE=CML PCH H AUDIO LPSS PM GPIOB/C/D]

MODULE REV DETAILS

MODULE NAME	REV	DATE



TBD_45673 8 OF 13

12 OF 13
TBD_45673

9 OF 13
TBD_45673

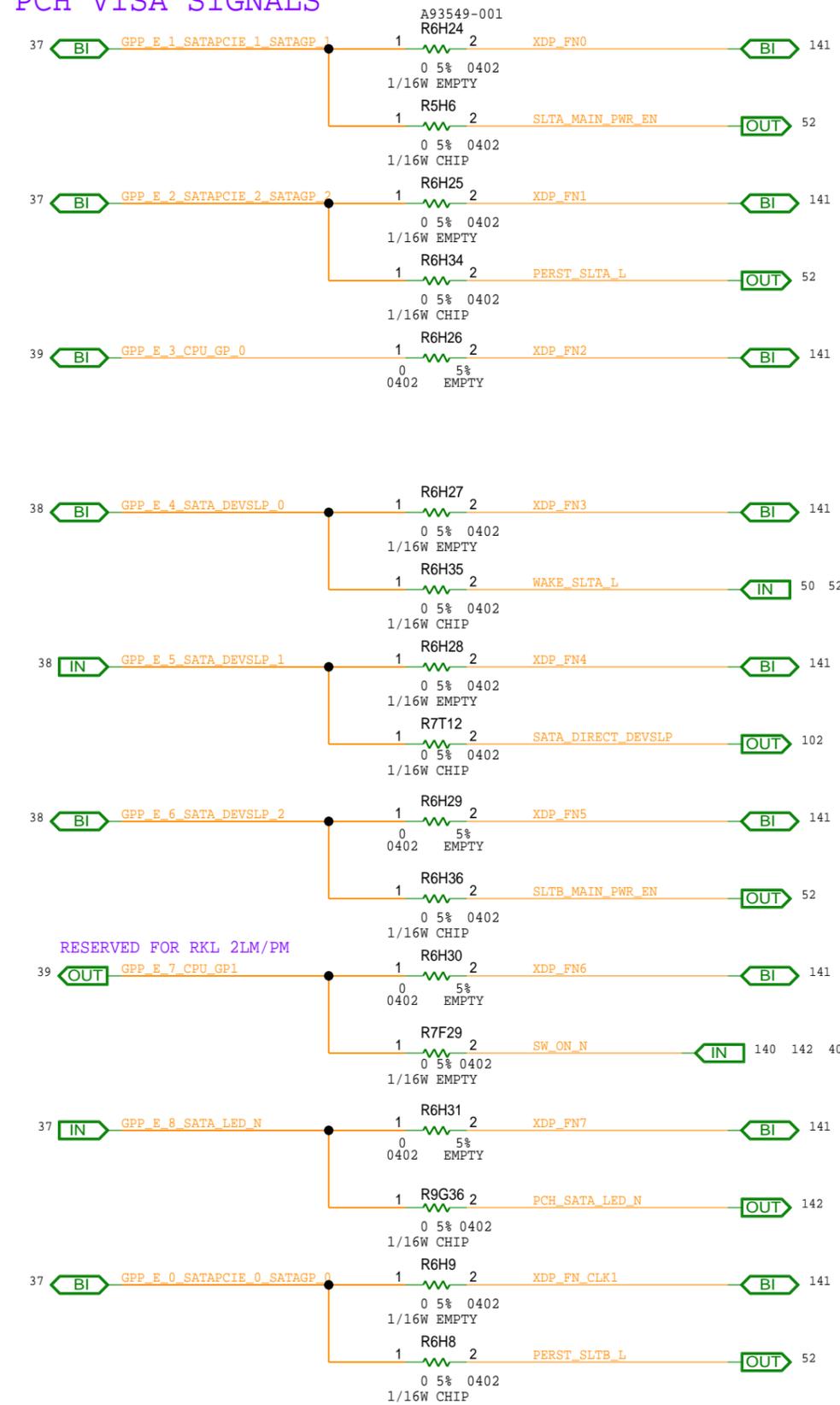
BPAGE DRAWING

udimm.sch_1.41
Fri Sep 27 16:39:50 2019

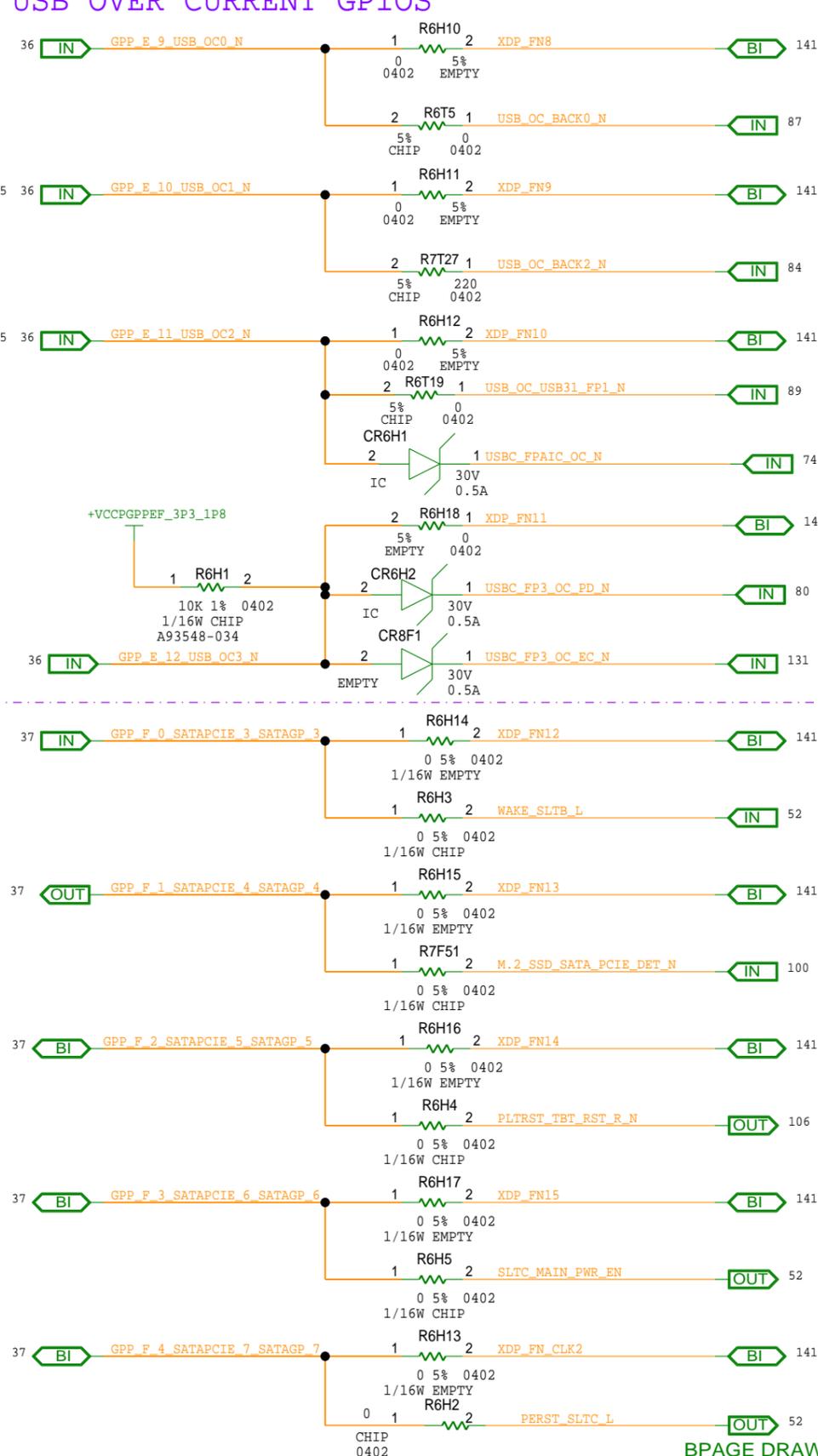
INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 41	REV 0.7
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[PAGE_TITLE=CML PCH H PWR AND GND]

PCH VISA SIGNALS

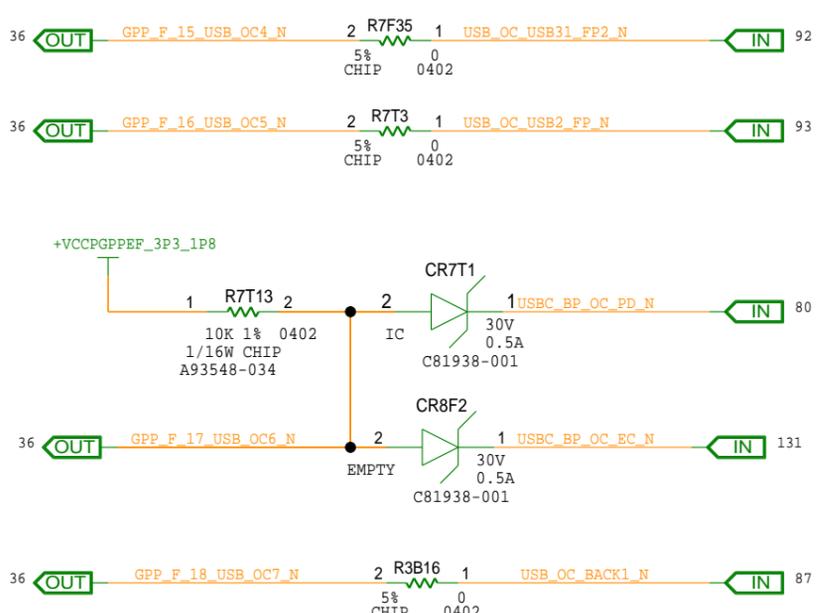


USB OVER CURRENT GPIOs



MODULE REV DETAILS

MODULE NAME	REV	DATE

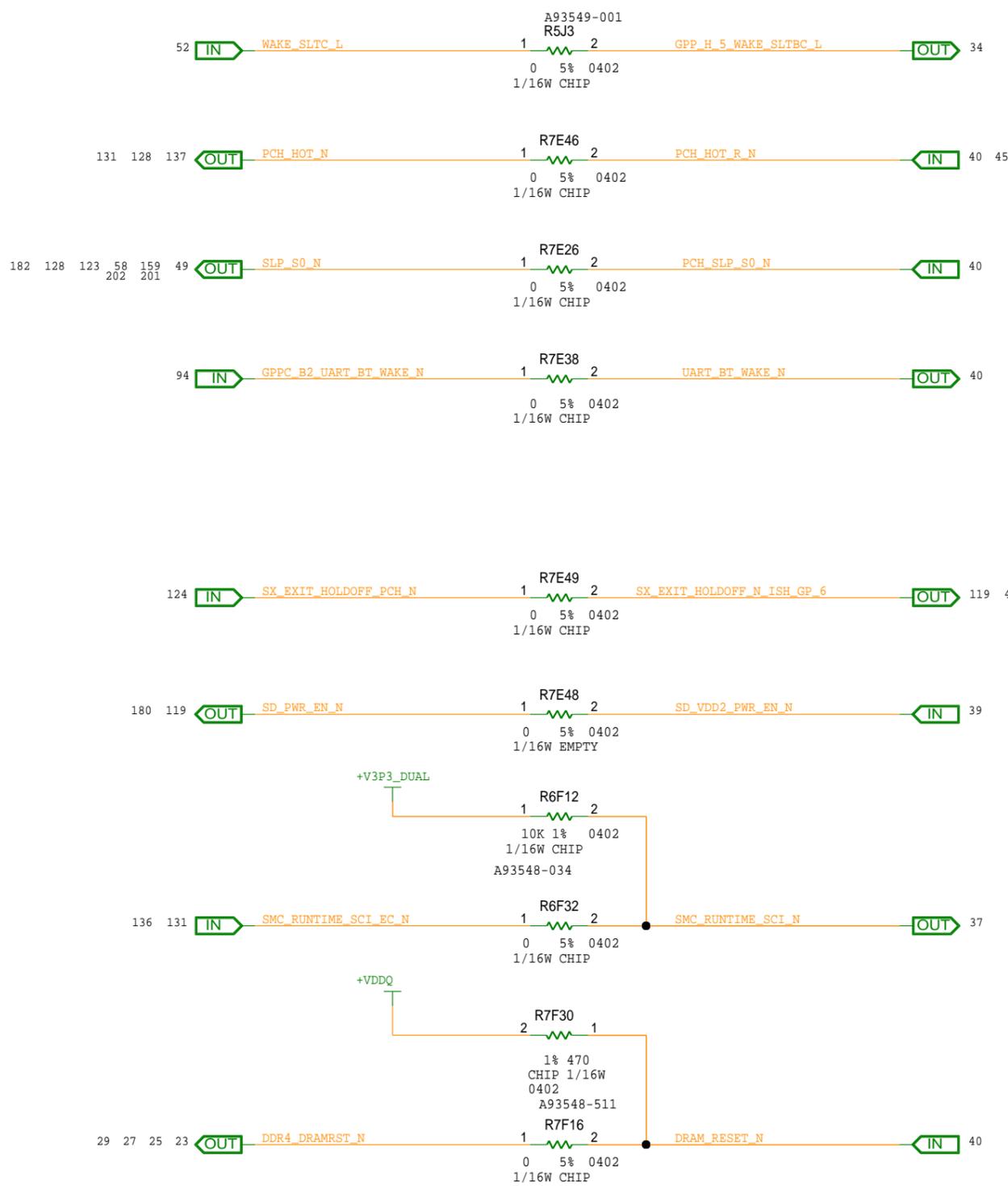


MODULE REV DETAILS

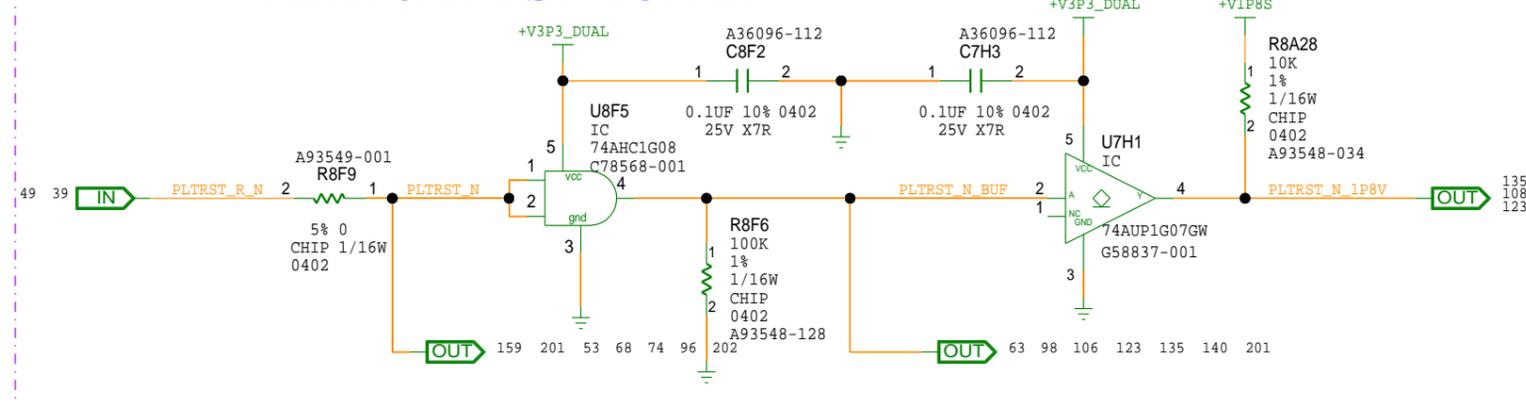
MODULE NAME	REV	DATE

END DEVICE

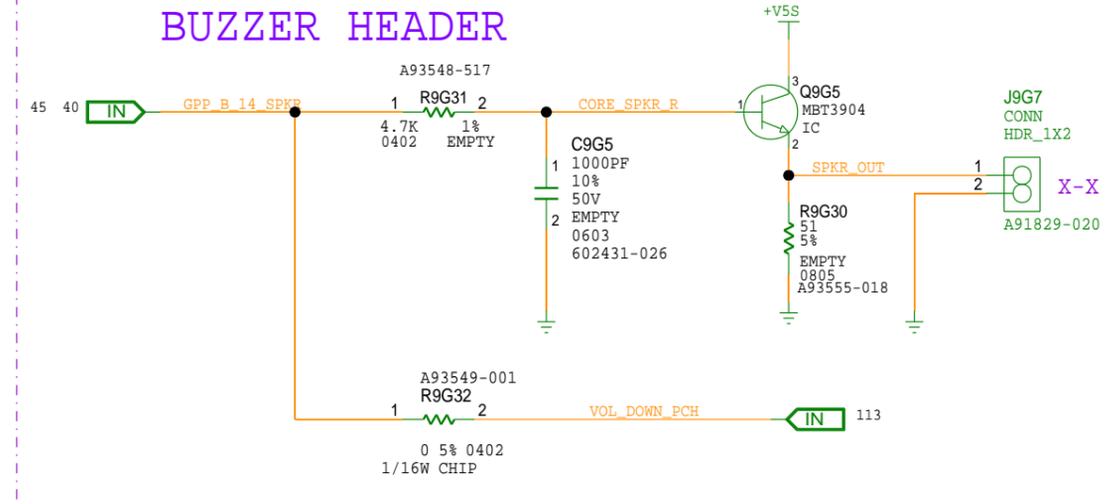
PCH GPIO



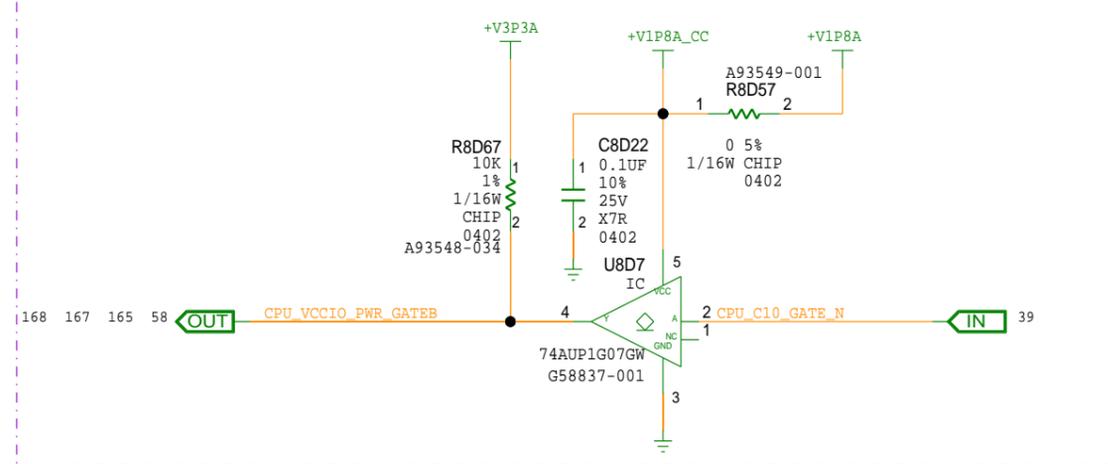
PLATFORM RST BUFFER



BUZZER HEADER



C10 GATE LEVEL SHIFTER



BPAGE DRAWING

udimm.sch_1.43
Fri Sep 27 16:39:52 2019

INTEL
CONFIDENTIAL

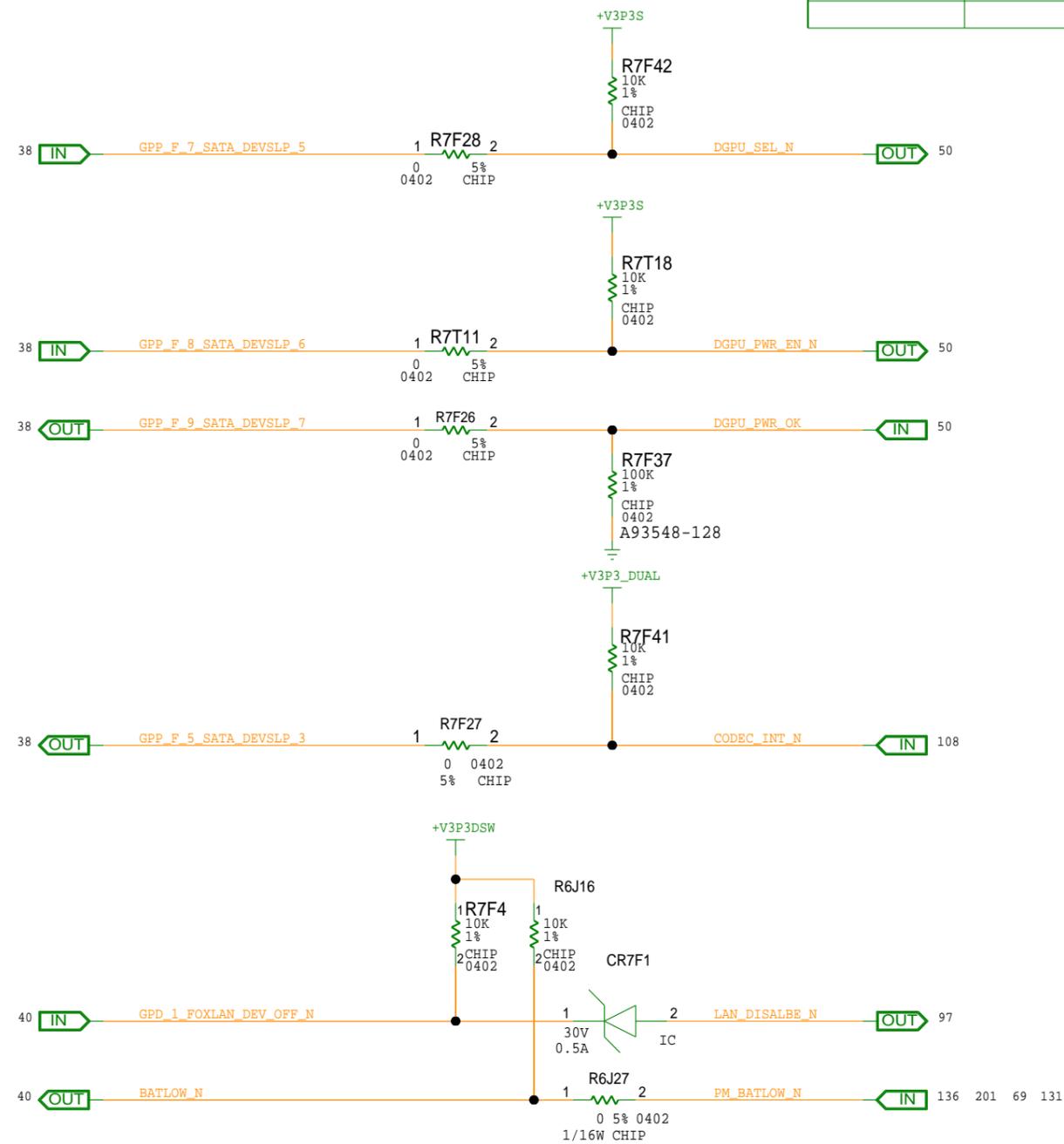
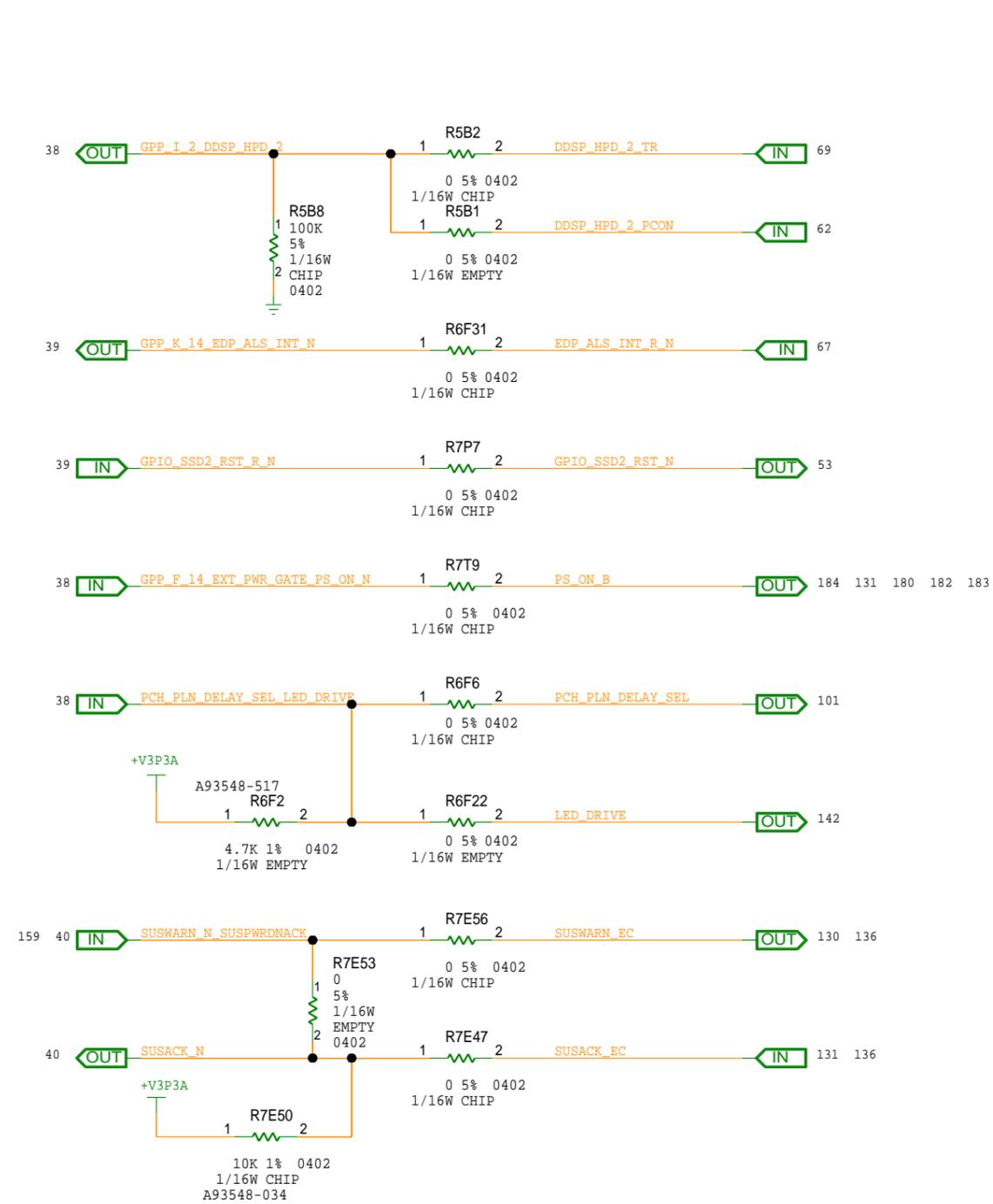
DOCUMENT_NUMBER
xxxxxxx

PAGE
43

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0.7

MODULE REV DETAILS

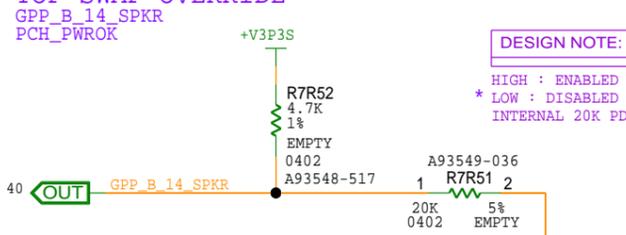
MODULE NAME	REV	DATE



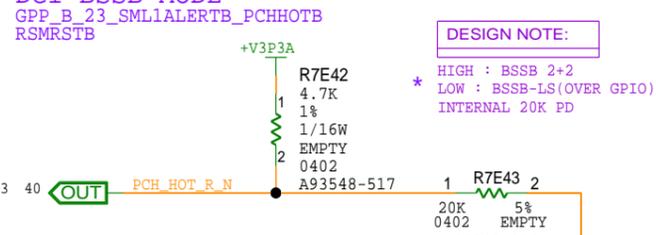
MODULE REV DETAILS

MODULE NAME	REV	DATE

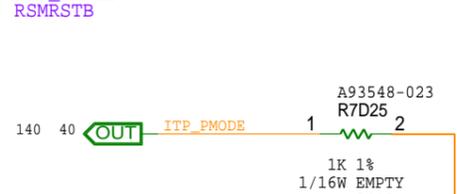
TOP SWAP OVERRIDE



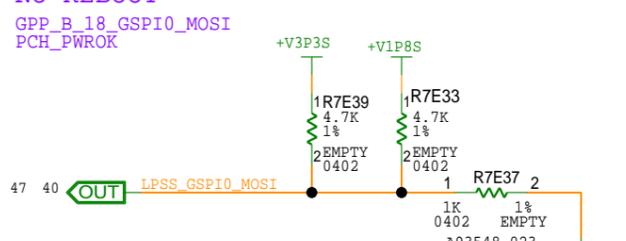
DCI BSSB MODE



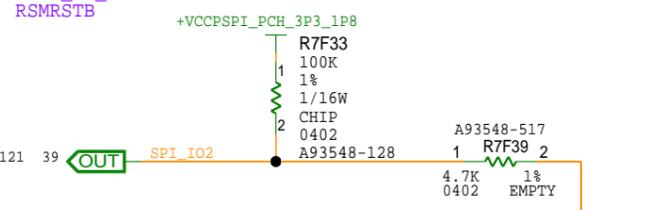
ITP_PMODE



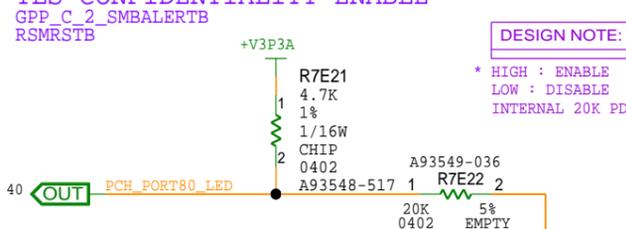
NO REBOOT



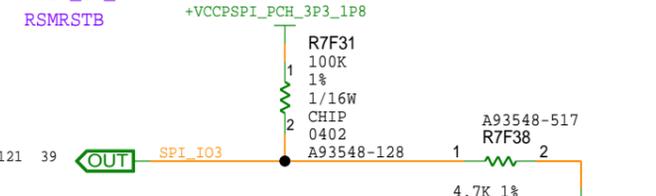
SPI0_IO_2



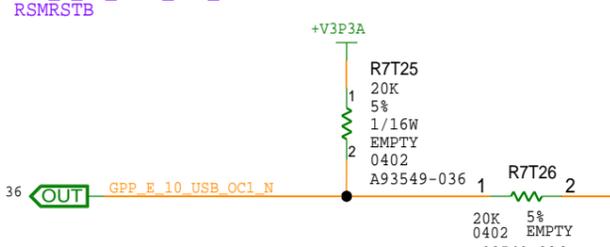
TLS CONFIDENTIALITY ENABLE



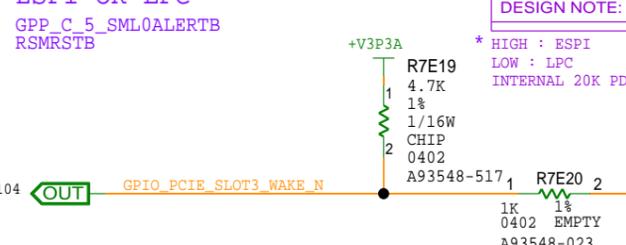
SPI0_IO_3



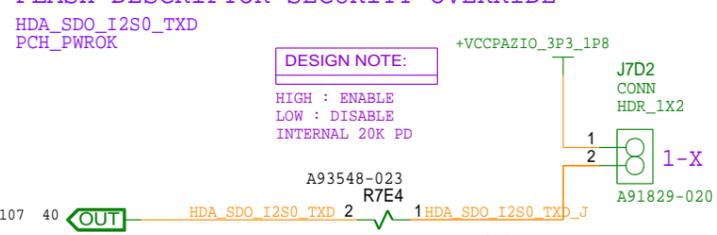
GPP_E_10_USB2_OCB_1



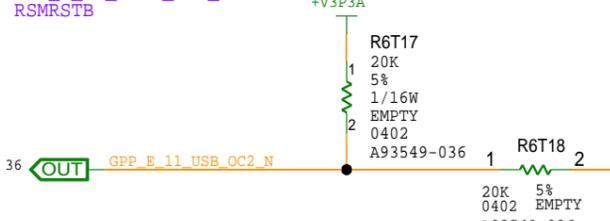
ESPI OR LPC



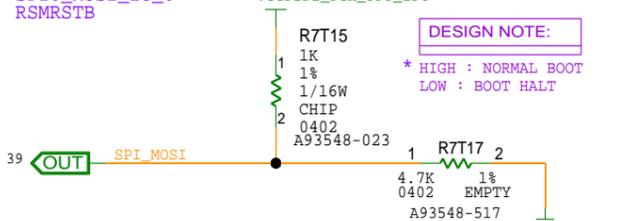
FLASH DESCRIPTOR SECURITY OVERRIDE



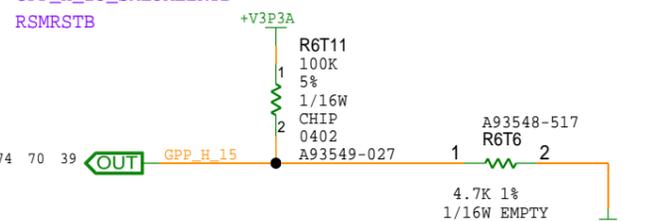
GPP_E_11_USB2_OCB_2



SPI0_MOSI_IO_0



GPP_H_15_SML3ALERTB



BPAGE DRAWING

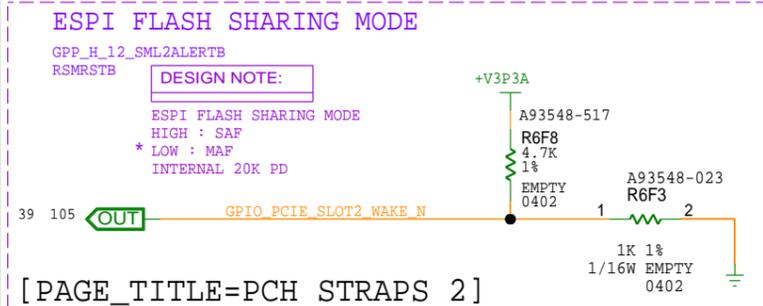
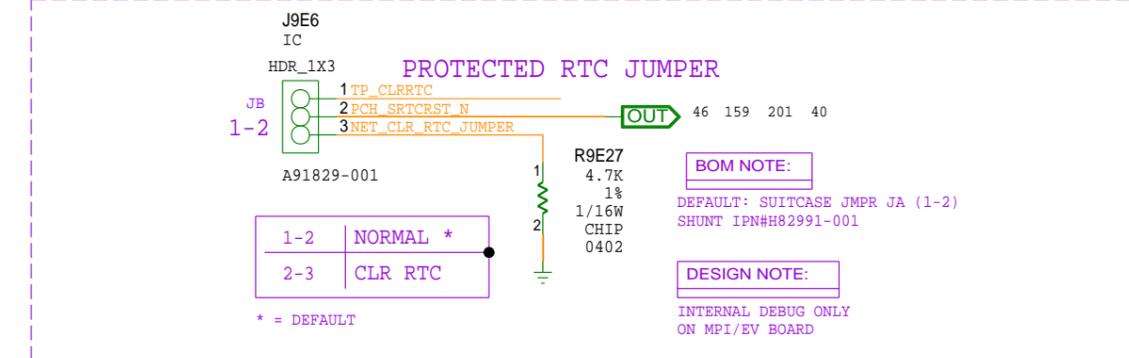
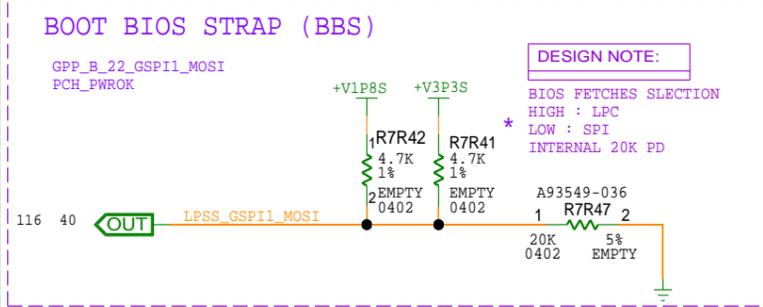
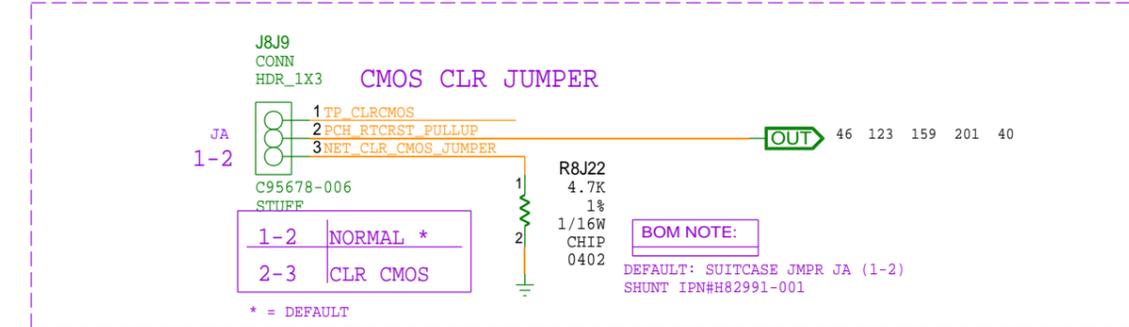
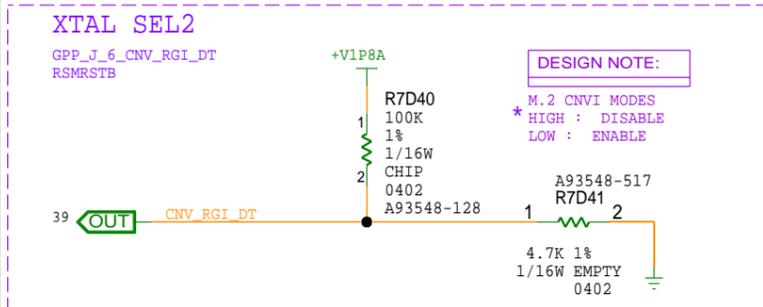
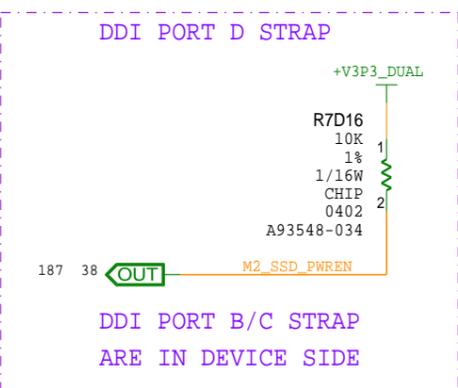
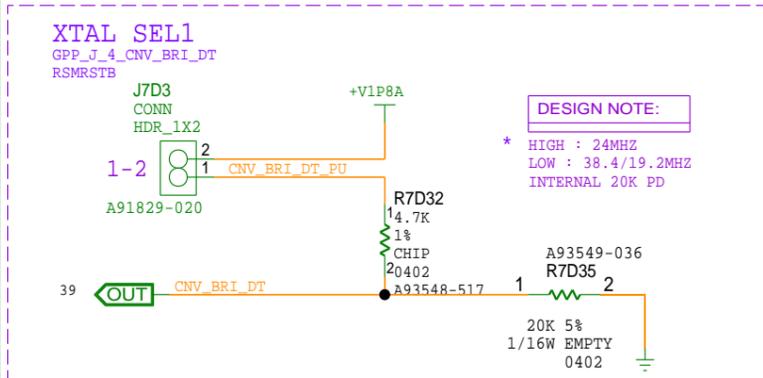
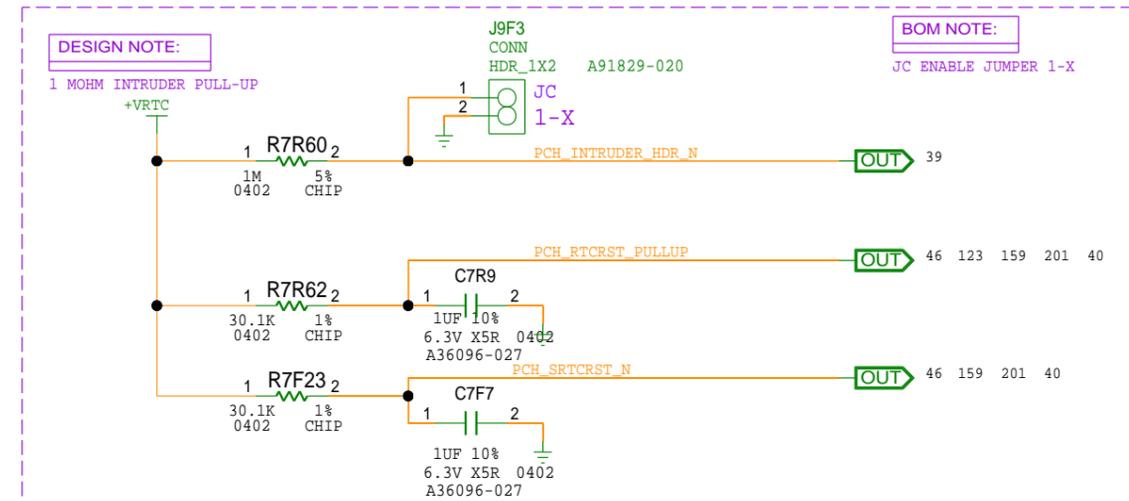
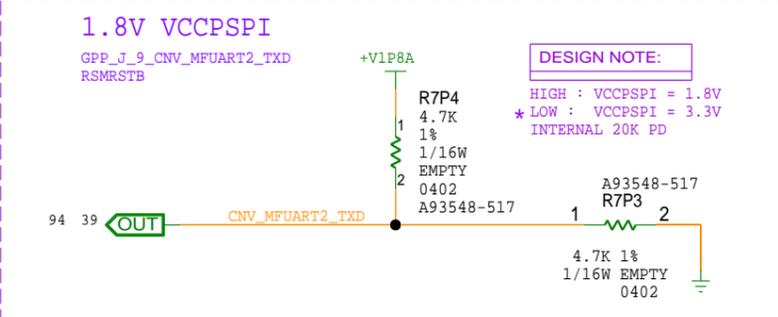
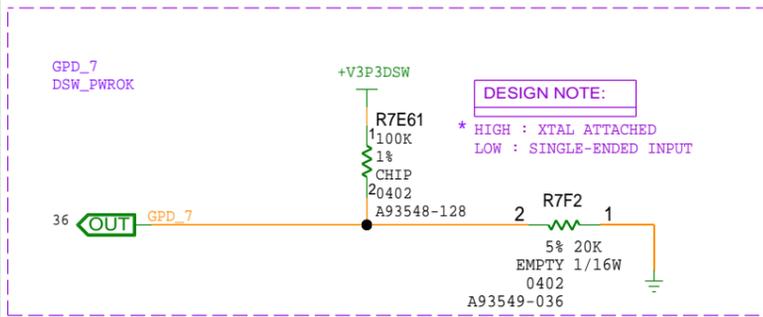
udimm.sch.1.45
Tue Oct 01 09:47:01 2019

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[PAGE_TITLE=PCH STRAPS 1]

MODULE REV DETAILS

MODULE NAME	REV	DATE



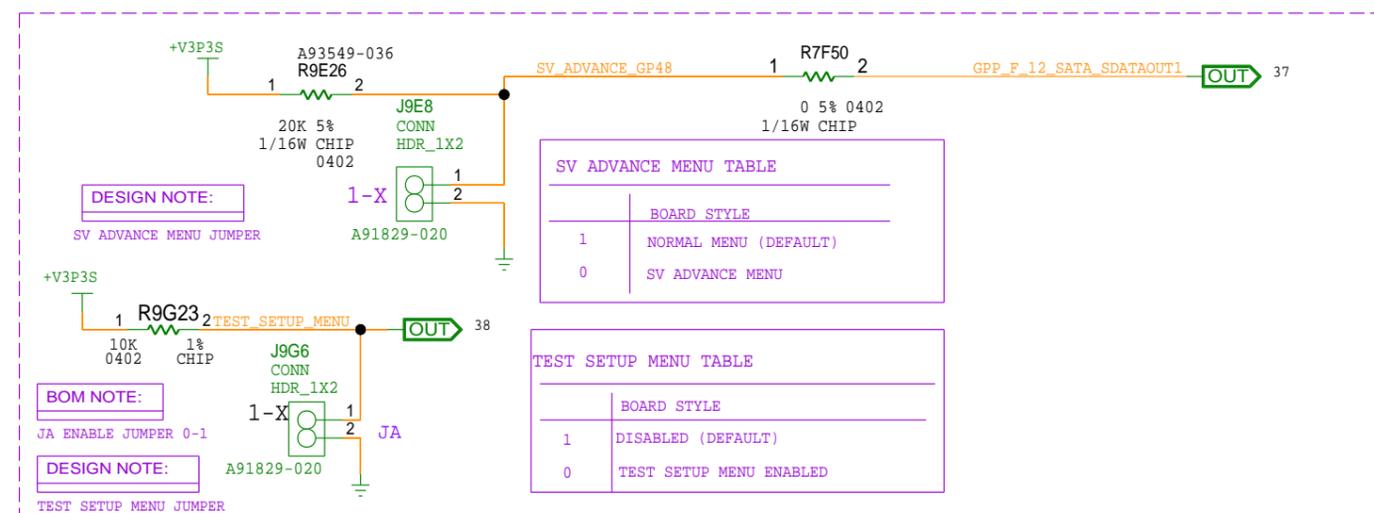
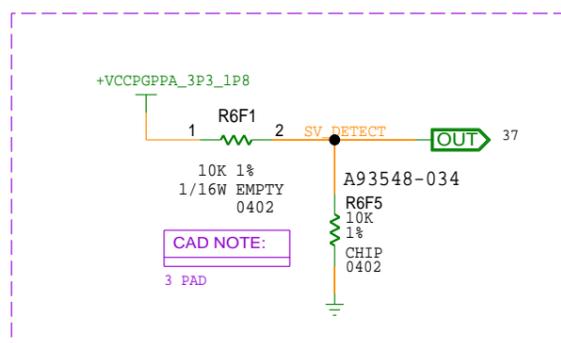
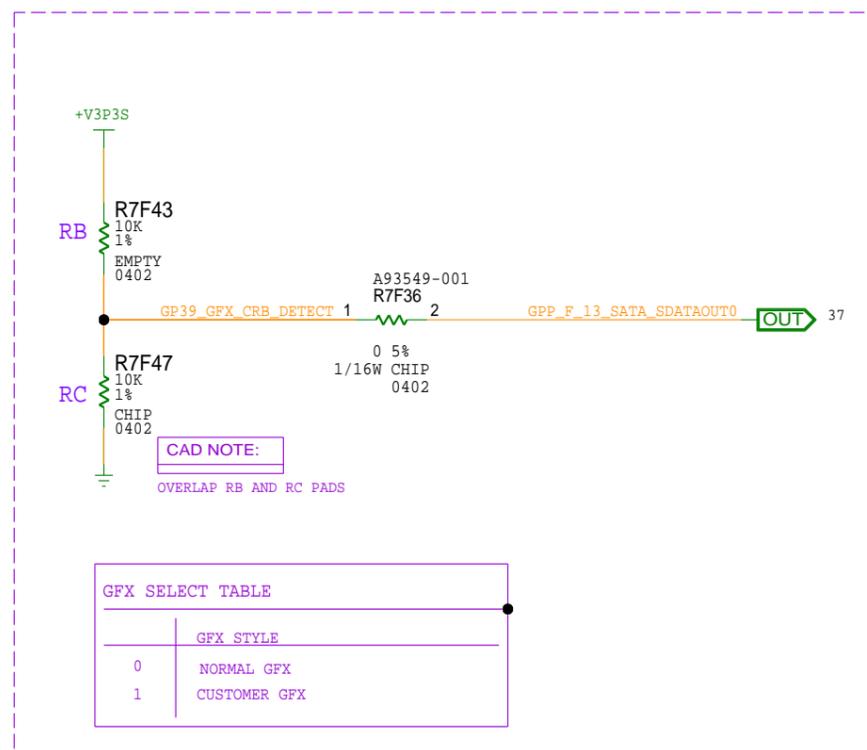
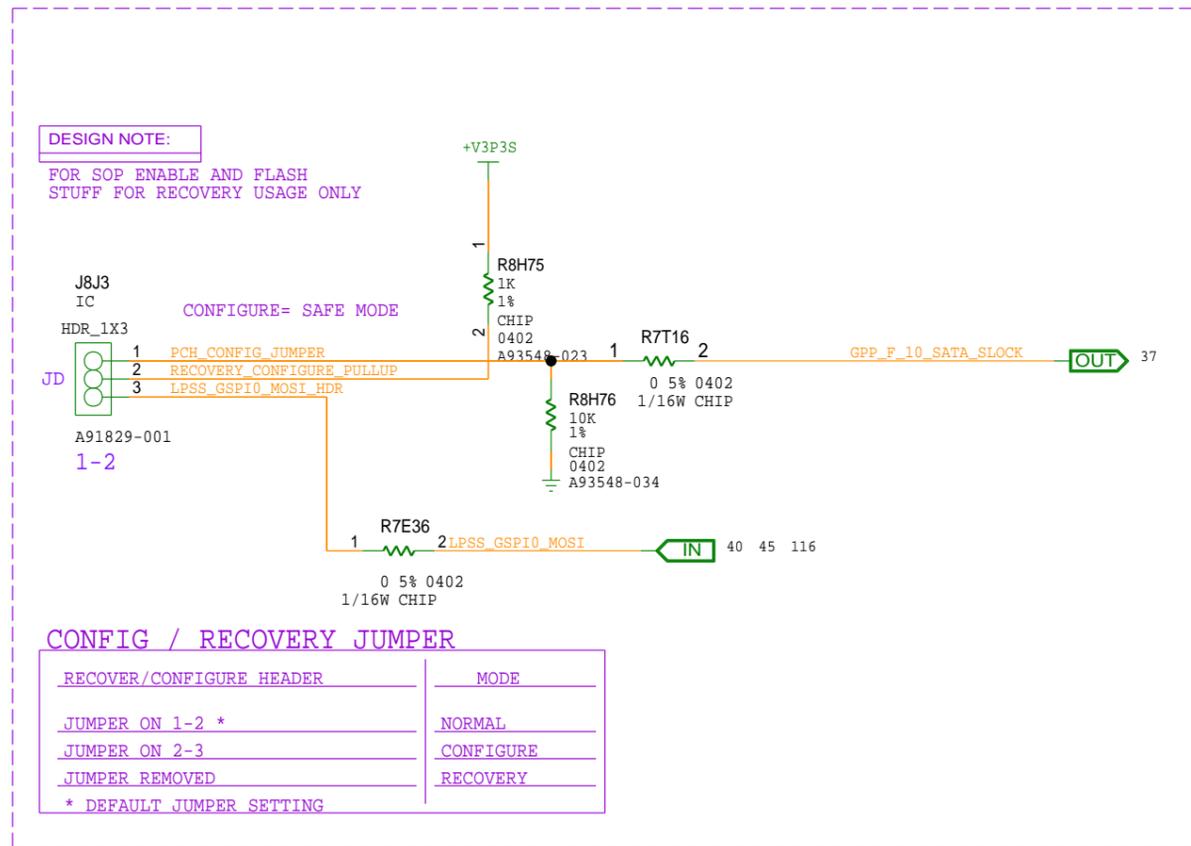
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udimm.sch_1.46
Fri Sep 27 16:39:54 2019

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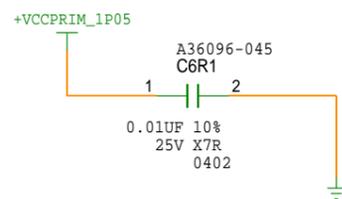
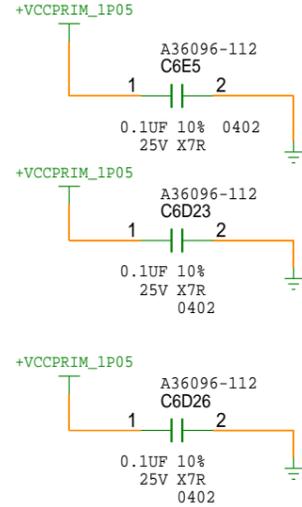
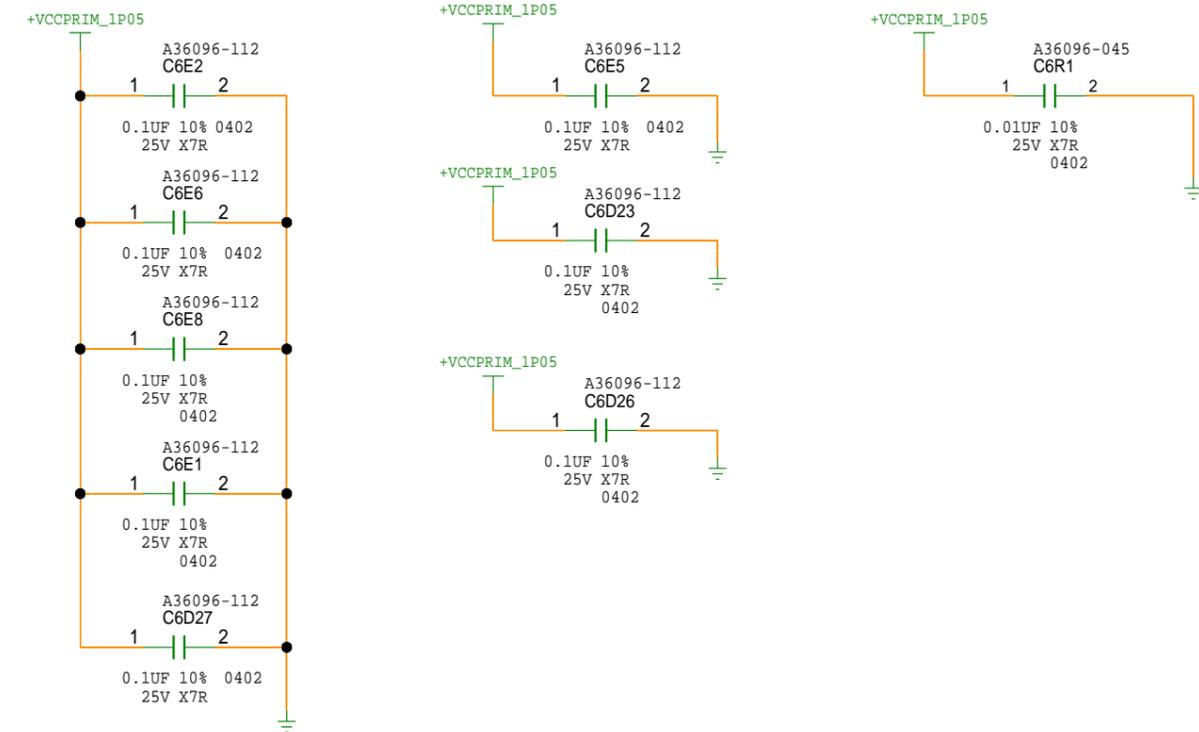
MODULE REV DETAILS

MODULE NAME	REV	DATE

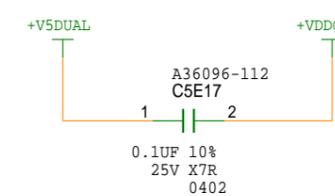
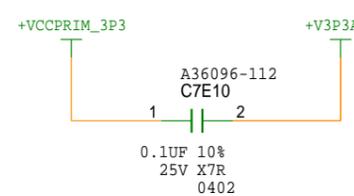
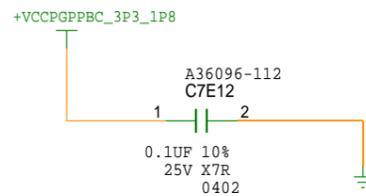
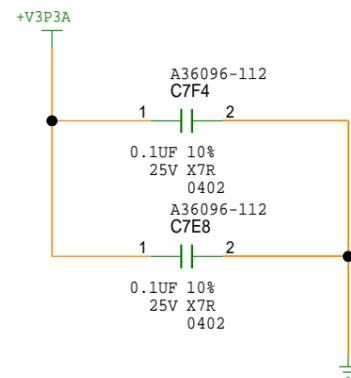
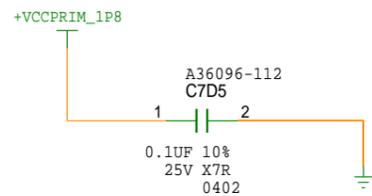
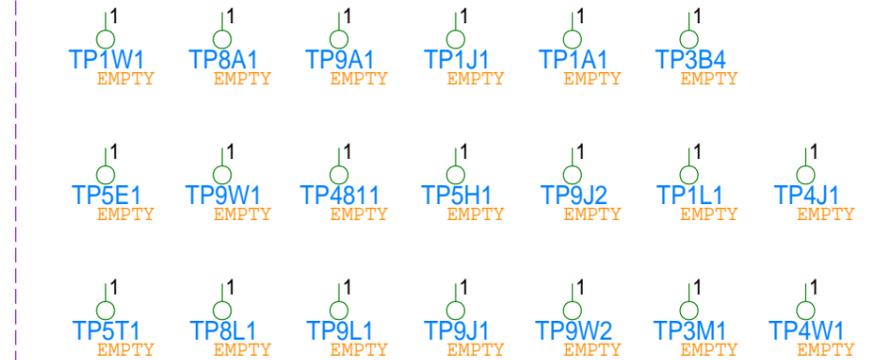


MODULE REV DETAILS

MODULE NAME	REV	DATE



FIDUCIAL SYMBOLS ADDED AS PER GIGABYTE'S REQUEST



[PAGE_TITLE=STITCH CAP]

BPAGE DRAWING

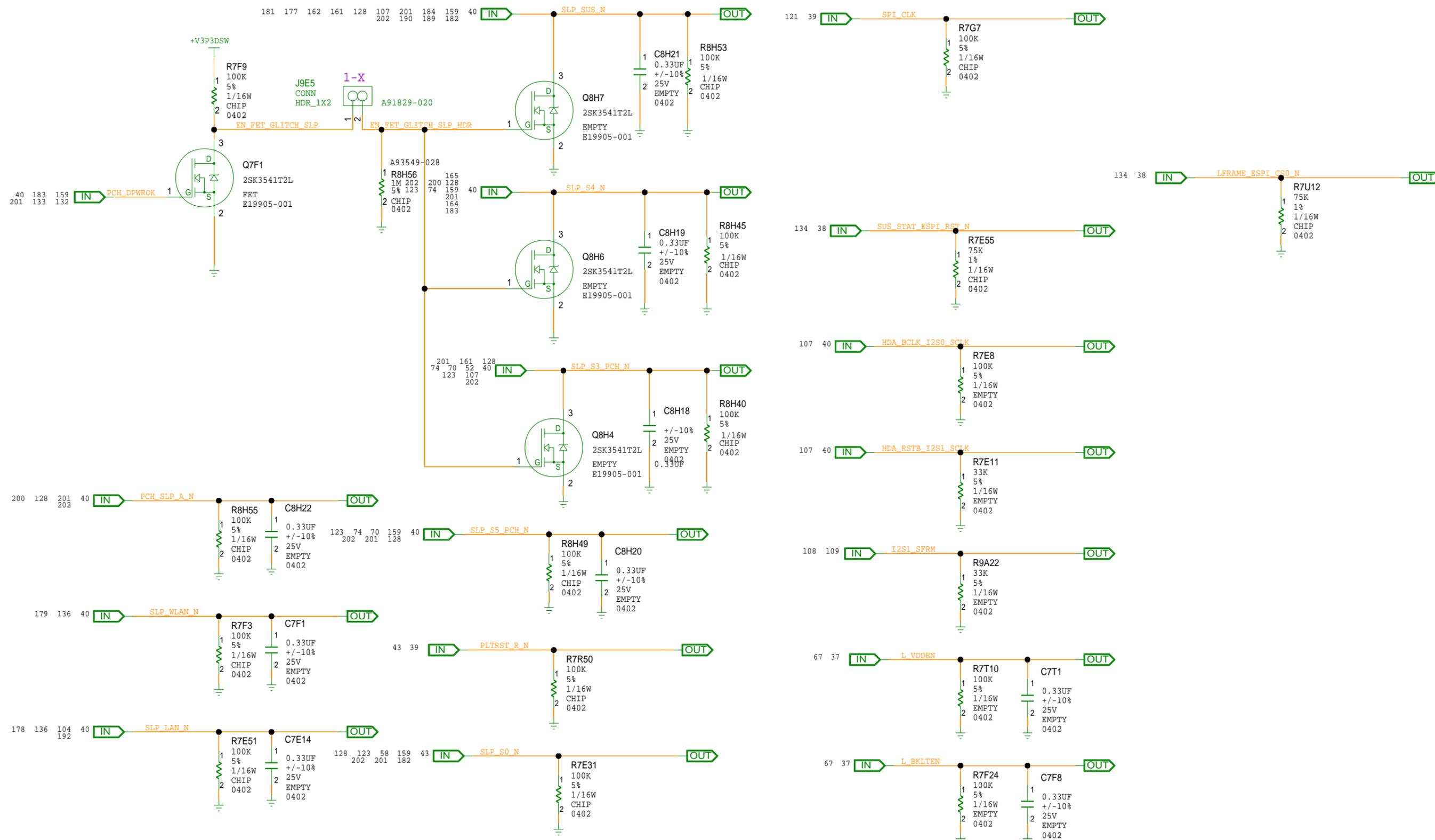
udimm.sch_1.48
Fri Sep 27 16:39:56 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 48	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE

PCH GLITCH ISSUE MITIGATION



BPAGE DRAWING

udimm_sch_1_49
Fri Sep 27 16:39:57 2019

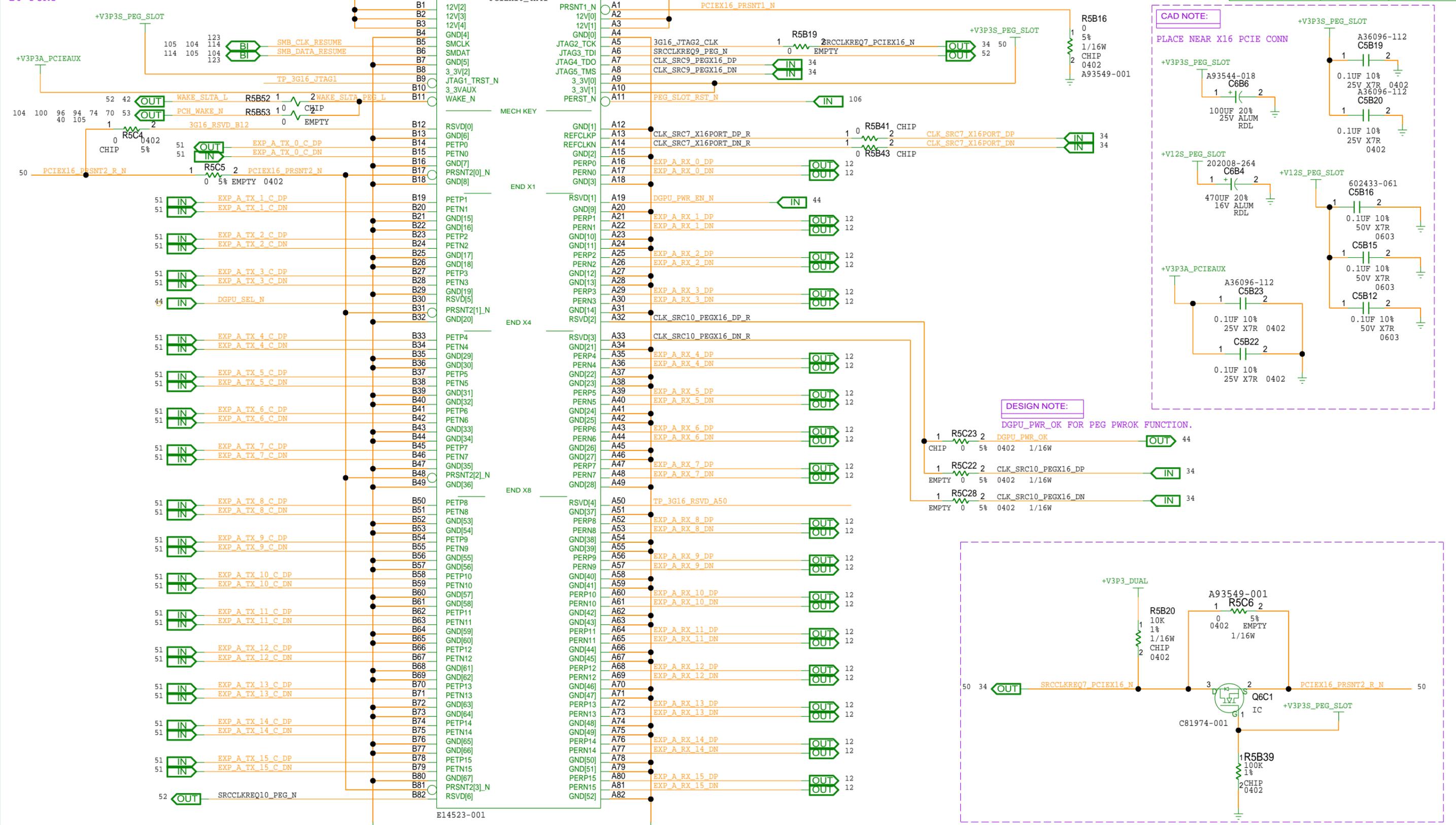
[PAGE_TITLE=GLITCH FREE CIRCUIT]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 49	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE

PCI EXPRESS ATX CONFIG 16-PORT



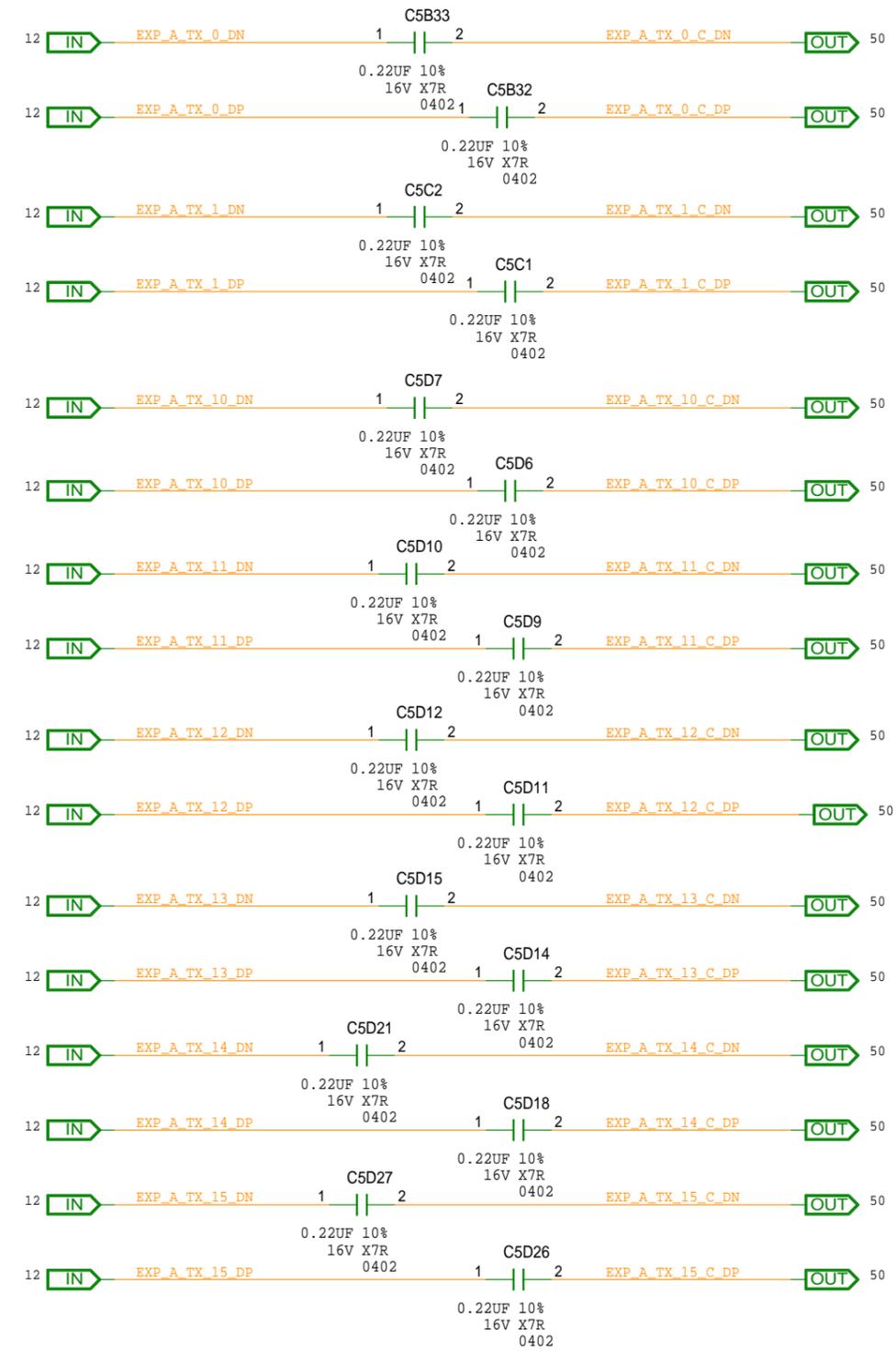
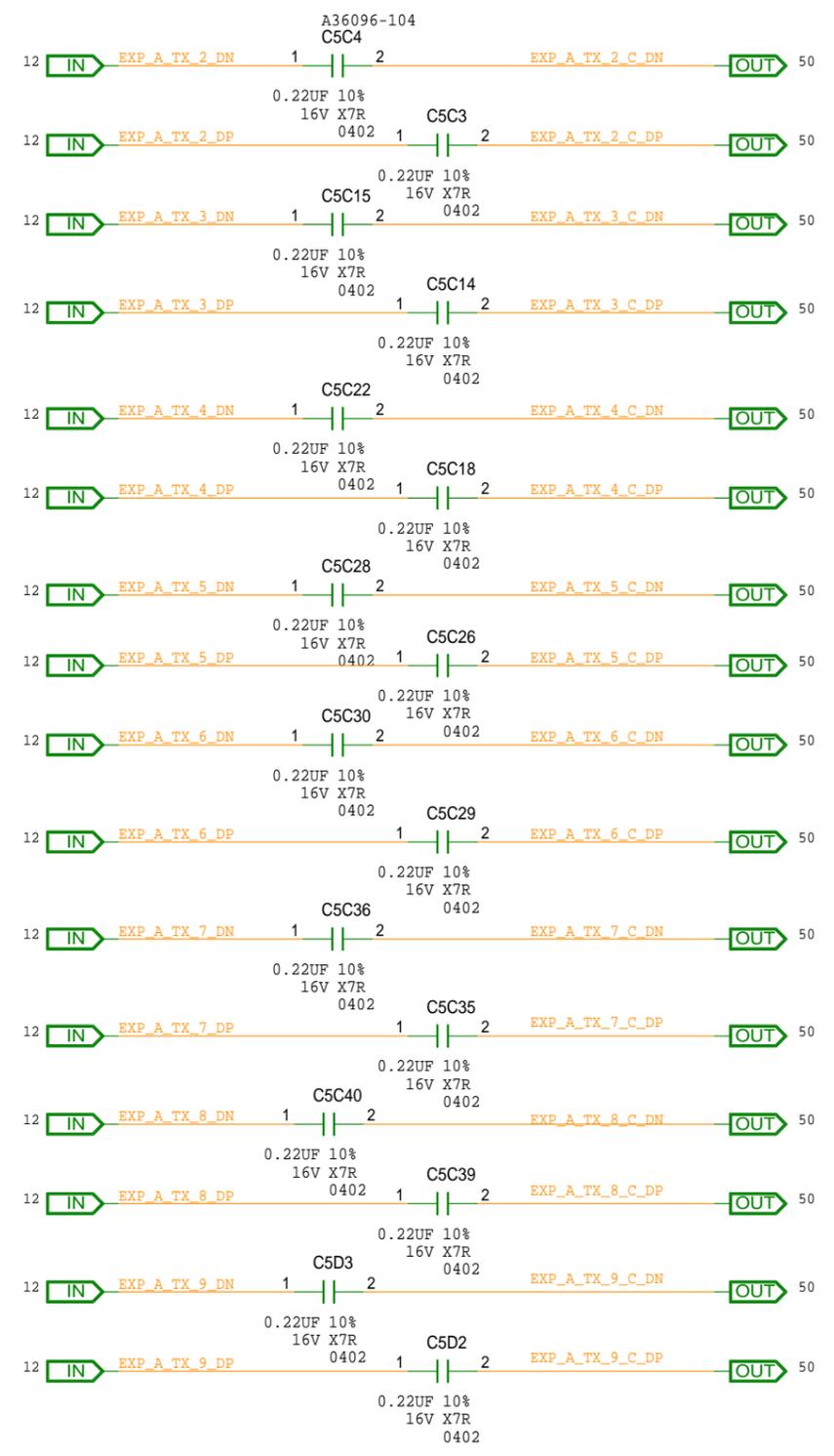
[PAGE_TITLE=PCI EXPRESS X16]

BPAGE DRAWING
udimm.sch_1.50
Fri Sep 27 16:39:58 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 50	REV 0.7
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CUSTOM TEXT BPAGE

MODULE REV DETAILS		
MODULE NAME	REV	DATE
BW_ATX_CORE	1.06.00	5-5-06



[PAGE_TITLE=PCI EXPRESS X16 COUPLING]

BPAGE DRAWING
udimm.sch_1.51
Fri Sep 13 12:44:24 2019

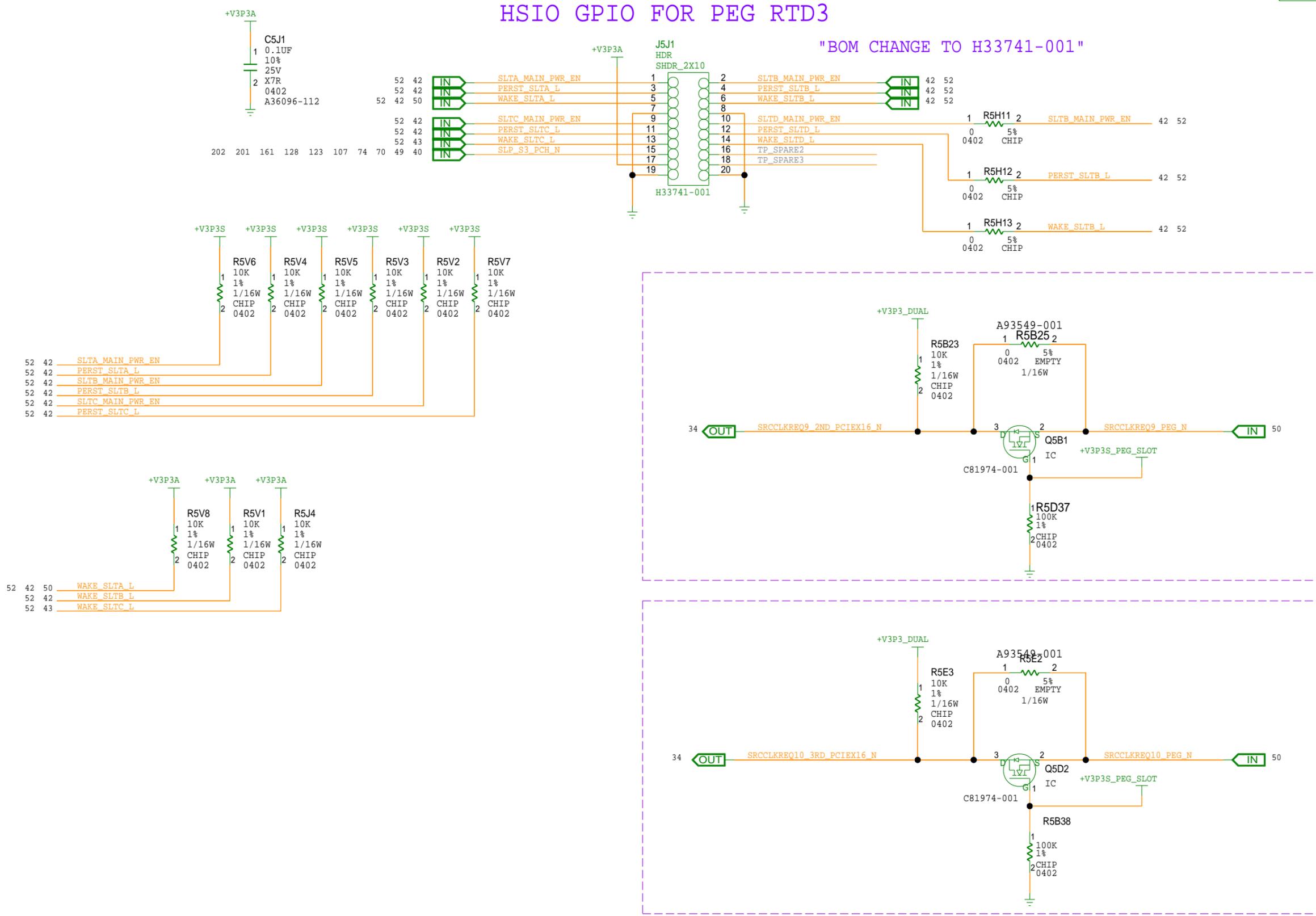
INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 51	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE

HSIO GPIO FOR PEG RTD3

"BOM CHANGE TO H33741-001"



[PAGE_TITLE=PEG RTD3 GPIO HEADER]

BPAGE DRAWING

udimm.sch_1.52
Fri Sep 27 16:39:59 2019

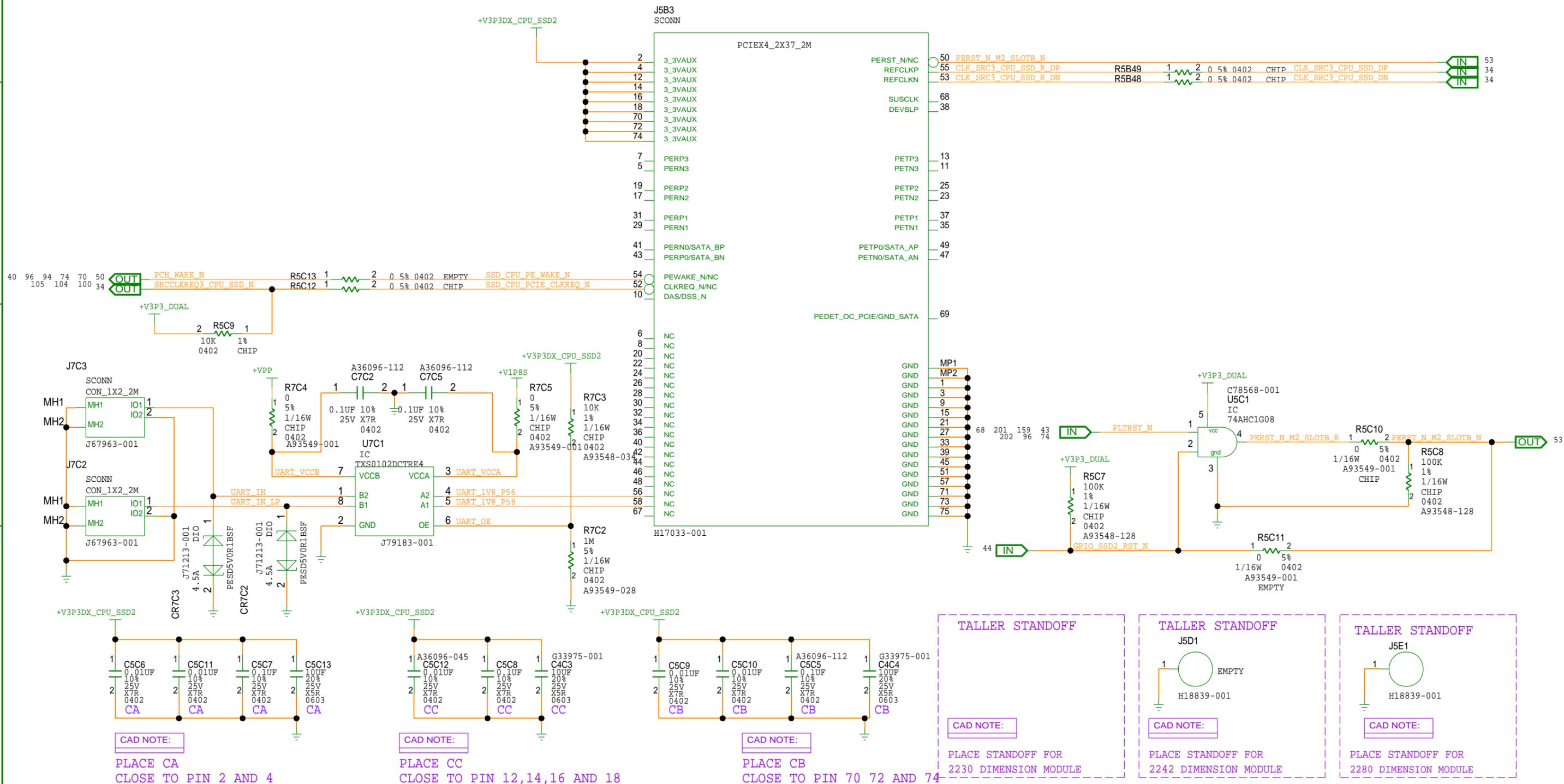
INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 52	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE

M.2 X4 CONNECTOR

8.2MM HEIGHT CONNECTOR



CAD NOTE:
PLACE CA
CLOSE TO PIN 2 AND 4

CAD NOTE:
PLACE CC
CLOSE TO PIN 12,14,16 AND 18

CAD NOTE:
PLACE CB
CLOSE TO PIN 70 72 AND 74

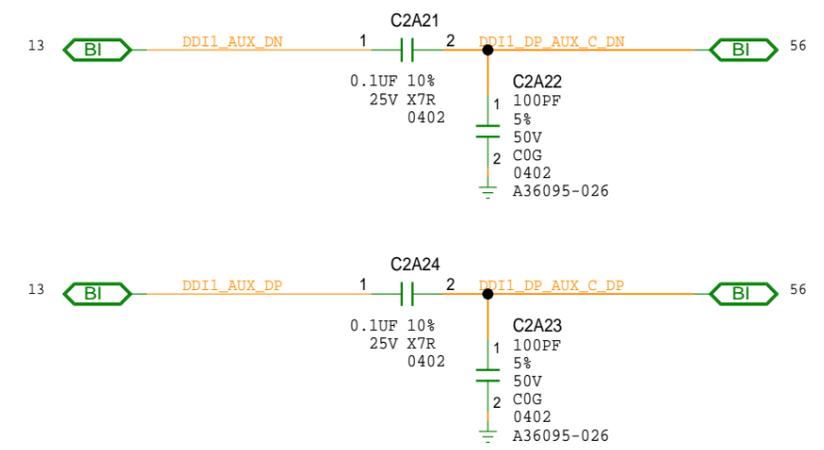
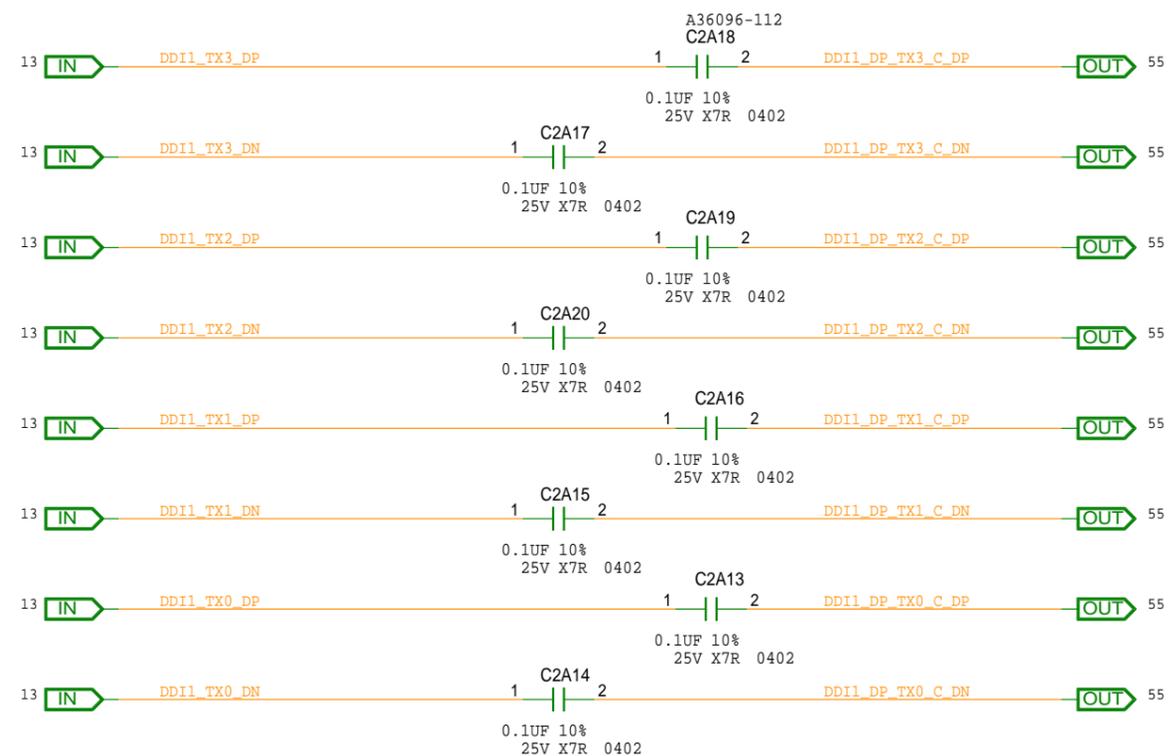
TALLER STANDOFF
CAD NOTE:
PLACE STANDOFF FOR
2230 DIMENSION MODULE

TALLER STANDOFF
CAD NOTE:
PLACE STANDOFF FOR
2242 DIMENSION MODULE

TALLER STANDOFF
CAD NOTE:
PLACE STANDOFF FOR
2280 DIMENSION MODULE

MODULE REV DETAILS

MODULE NAME	REV	DATE



[PAGE_TITLE=DISPLAY - DDI1 PORT, AC CAP]

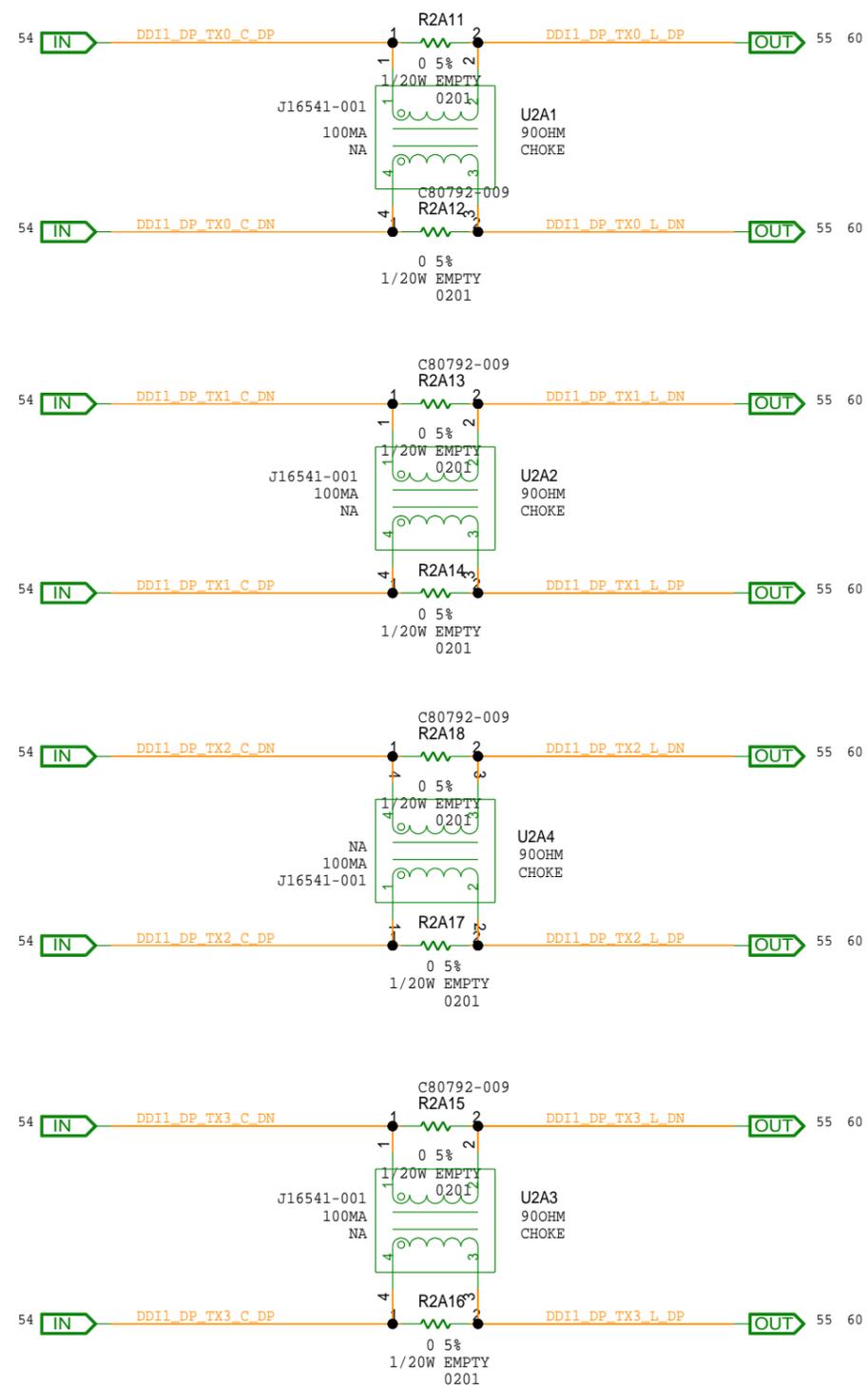
BPAGE DRAWING
 udimm.sch_1.54
 Fri Sep 27 16:40:01 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 54	REV 0.7
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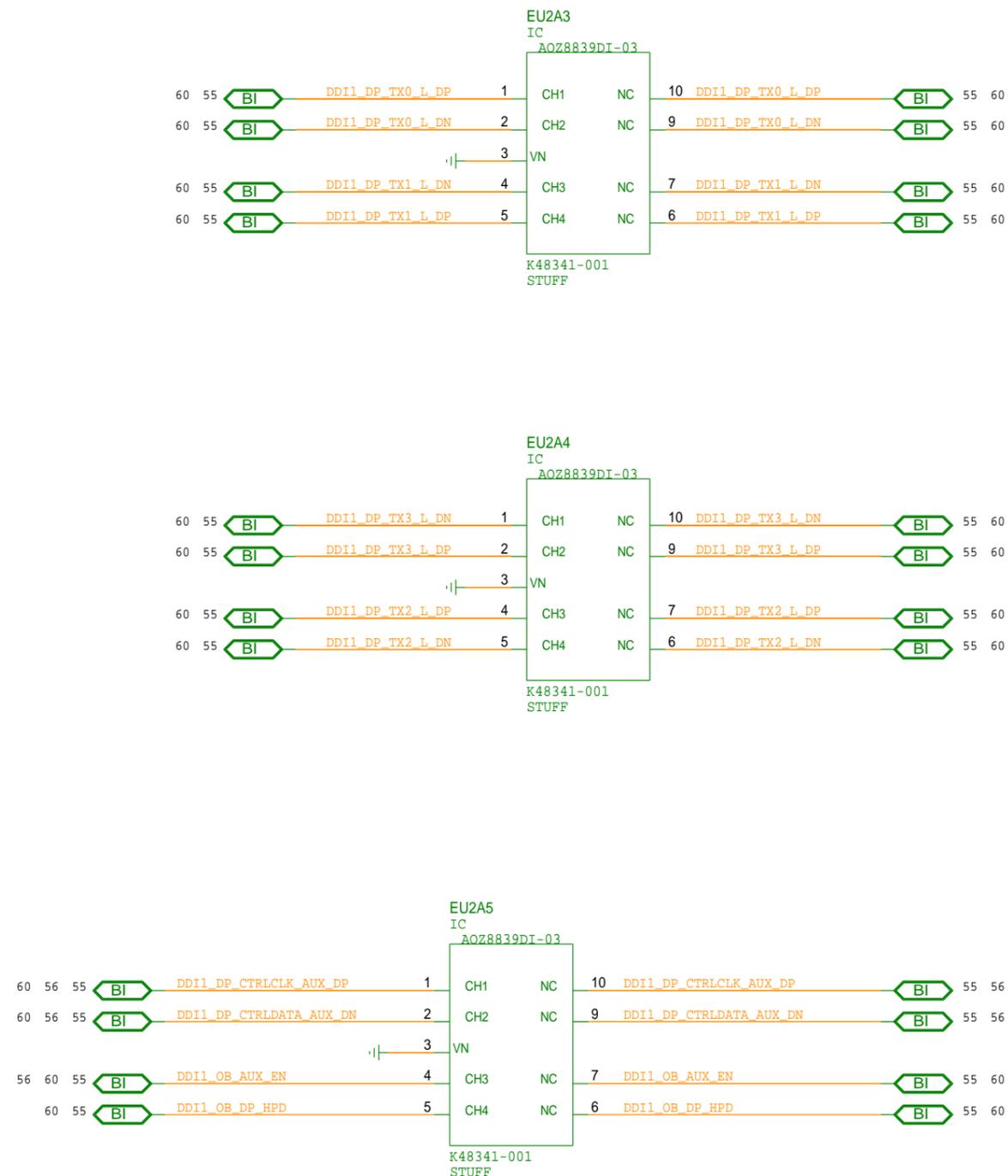
MODULE REV DETAILS

MODULE NAME	REV	DATE

DP CONNECTOR 1, CMC



DP CONNECTOR 1, ESD



[PAGE_TITLE=DISPLAY - DP CONNECTOR 1, CMC & ESD]

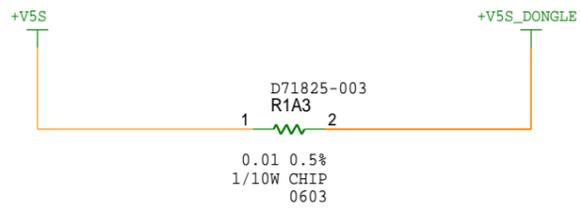
BPAGE DRAWING

udimm.sch_1.55
Fri Sep 27 16:40:02 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 55	REV 0.7
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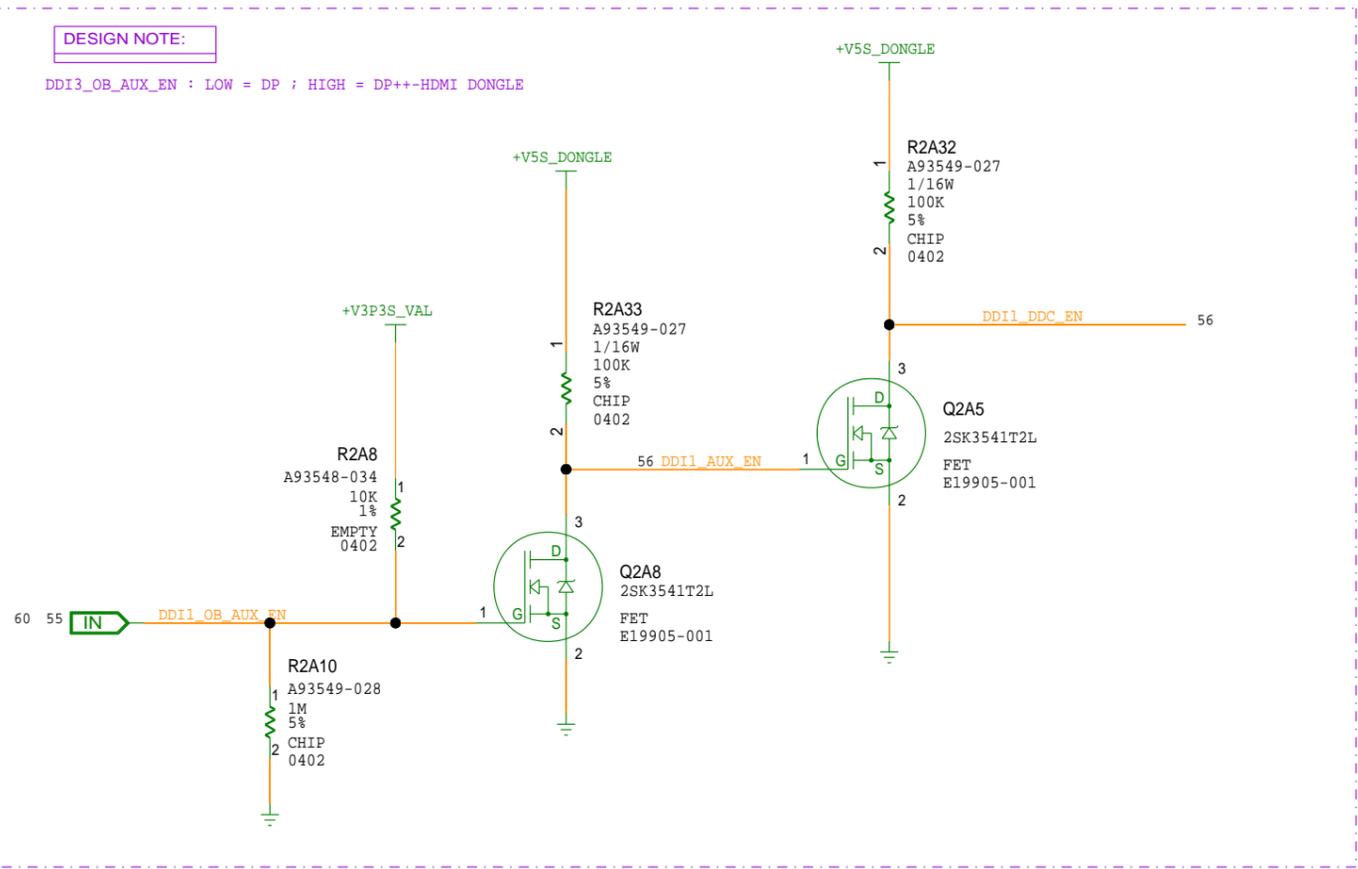
MODULE REV DETAILS

MODULE NAME	REV	DATE



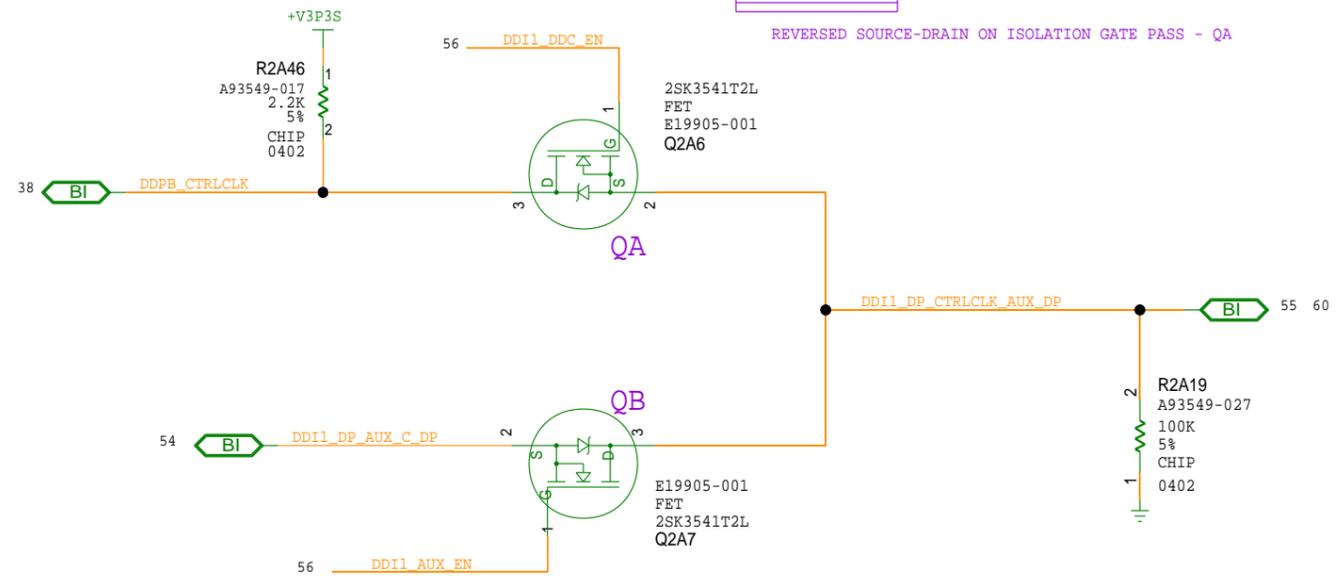
DESIGN NOTE:

DDI3_OB_AUX_EN : LOW = DP ; HIGH = DP++-HDMI DONGLE

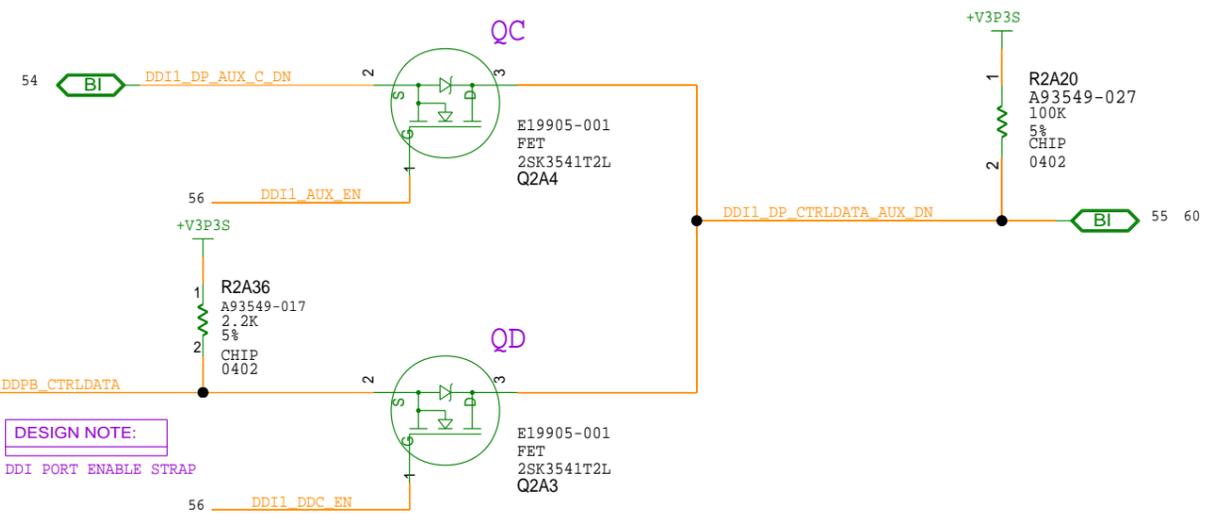


DESIGN NOTE:

REVERSED SOURCE-DRAIN ON ISOLATION GATE PASS - QA



QA,QB,QC,QD: VGSTH < 1.5V

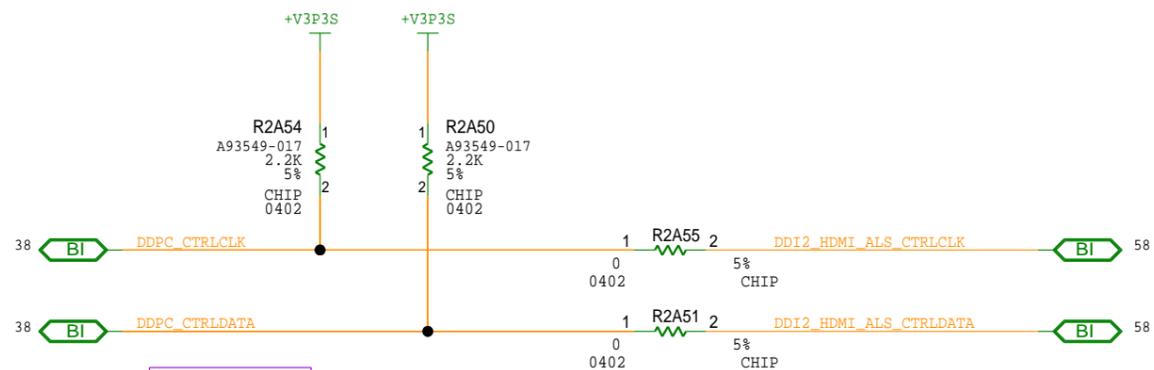
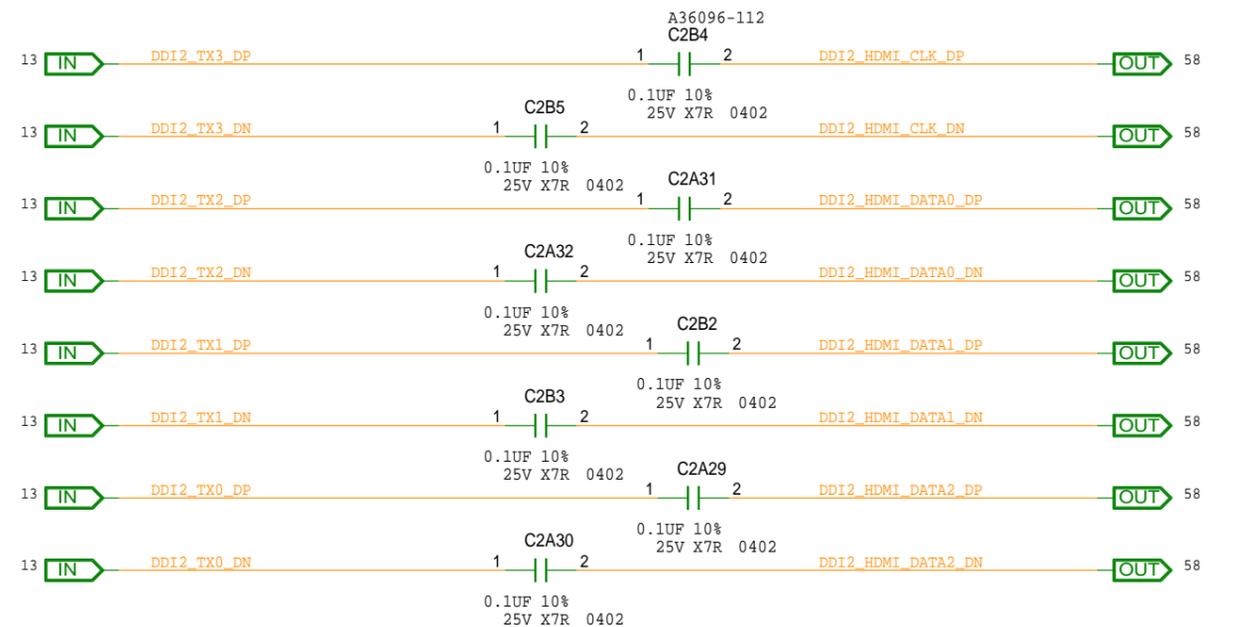


DESIGN NOTE:

DDI PORT ENABLE STRAP

MODULE REV DETAILS

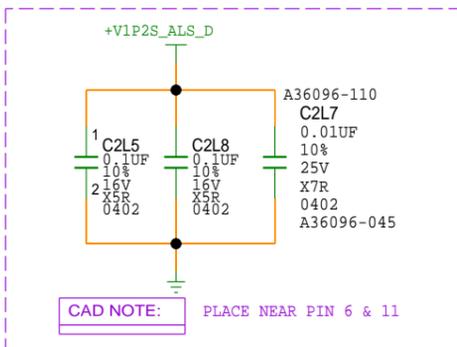
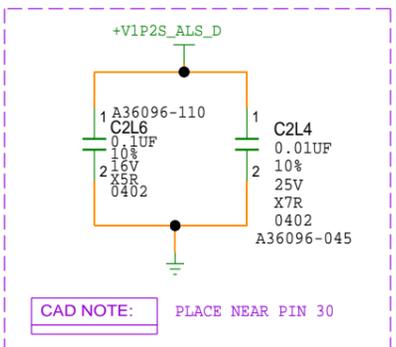
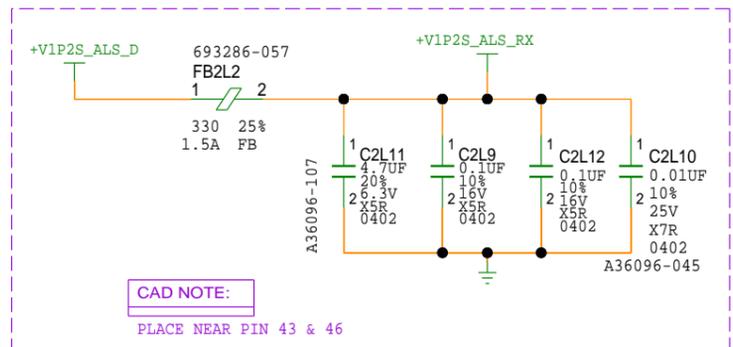
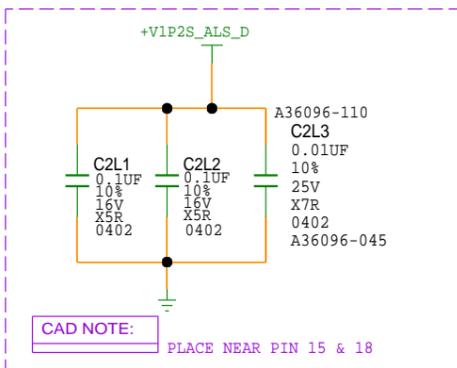
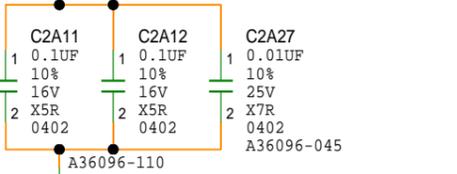
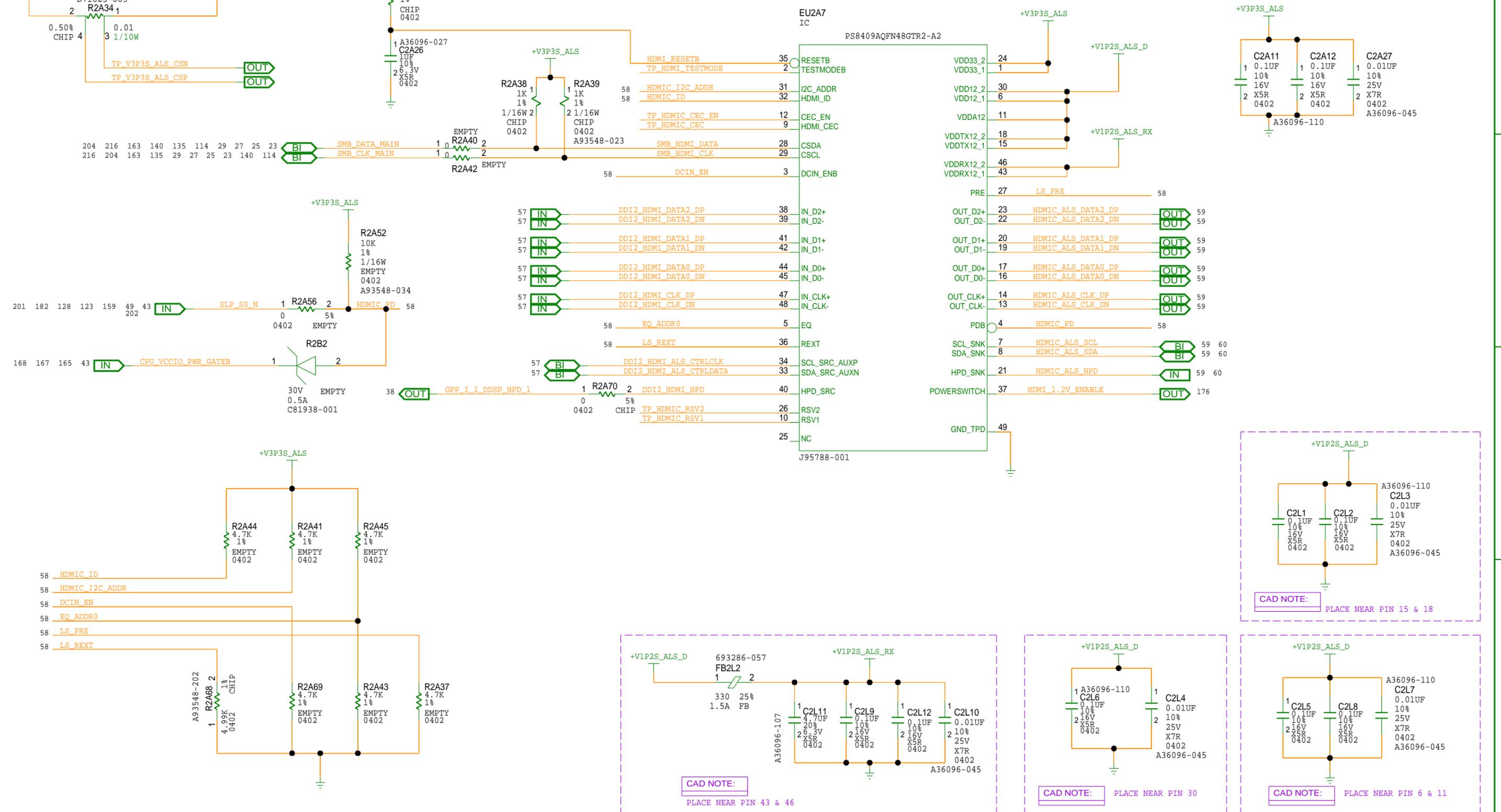
MODULE NAME	REV	DATE



DESIGN NOTE:
DDI PORT ENABLE STRAP

MODULE REV DETAILS		
MODULE NAME	REV	DATE

HDMI RETIMING LEVEL SHIFTER



BPAGE DRAWING

udimm.sch_1.58
Fri Sep 27 16:40:05 2019

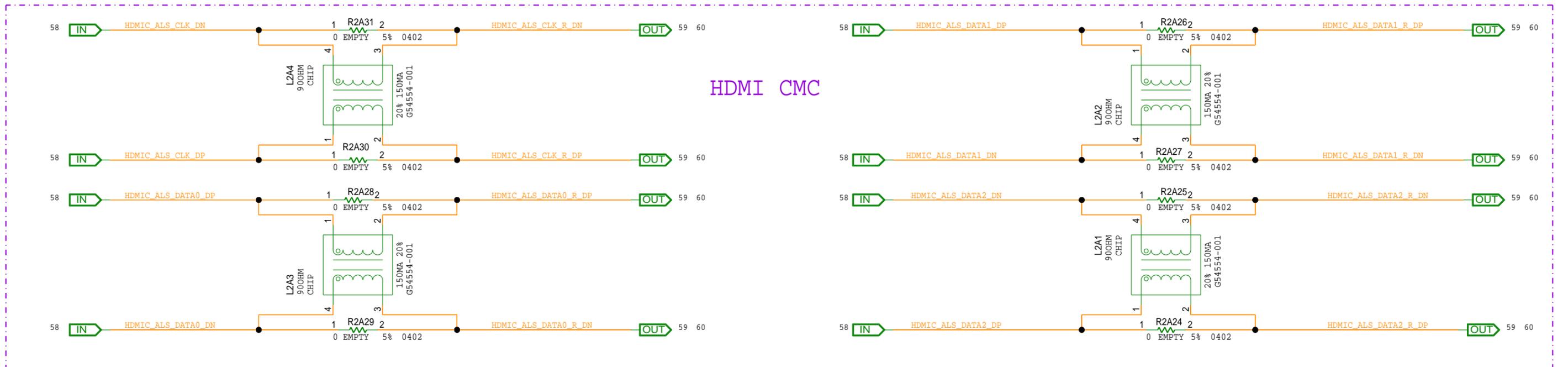
INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 58	REV 0.7
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[PAGE_TITLE=DISPLAY - HDMI CONN 1, RETIMING LEVEL SHIFTER]

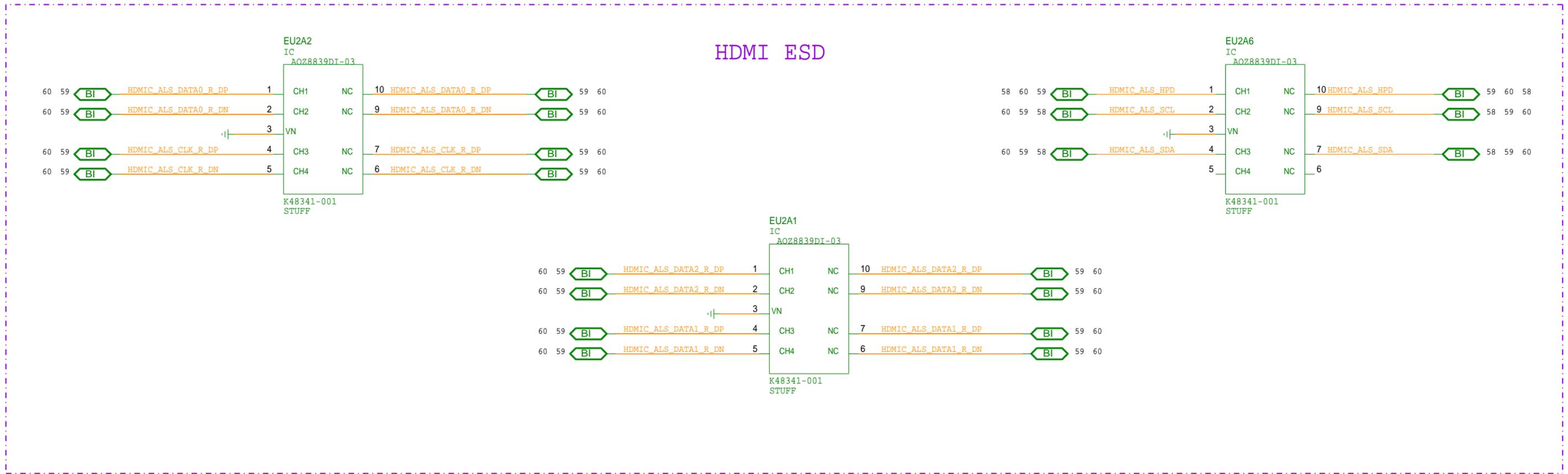
MODULE REV DETAILS

MODULE NAME	REV	DATE

HDMI CMC

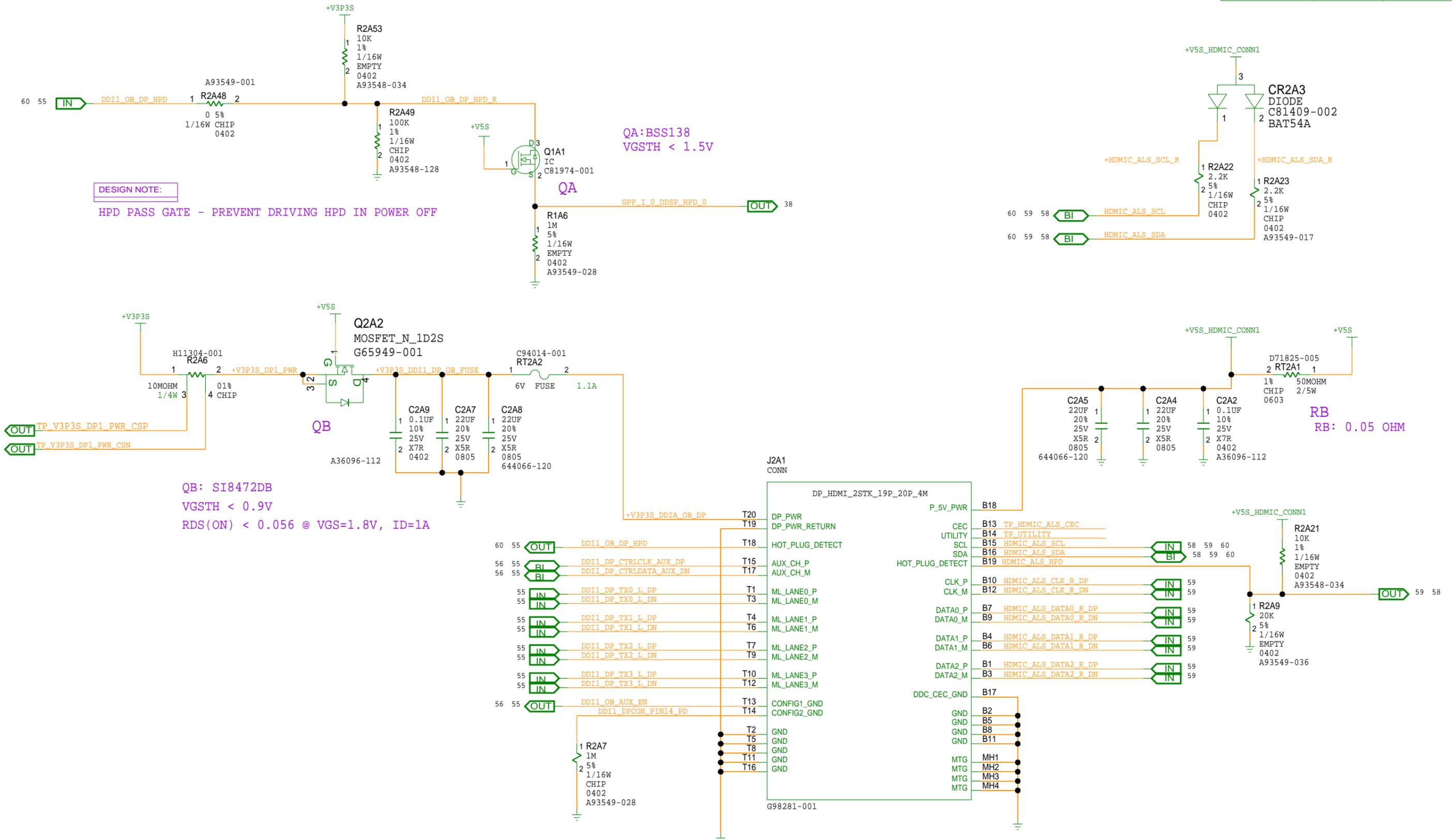


HDMI ESD



MODULE REV DETAILS

MODULE NAME	REV	DATE



DESIGN NOTE:

HPD PASS GATE - PREVENT DRIVING HPD IN POWER OFF

QB: SI8472DB
 VGSTH < 0.9V
 RDS(ON) < 0.056 @ VGS=1.8V, ID=1A

QA: BSS138
 VGSTH < 1.5V

RB: 0.05 OHM

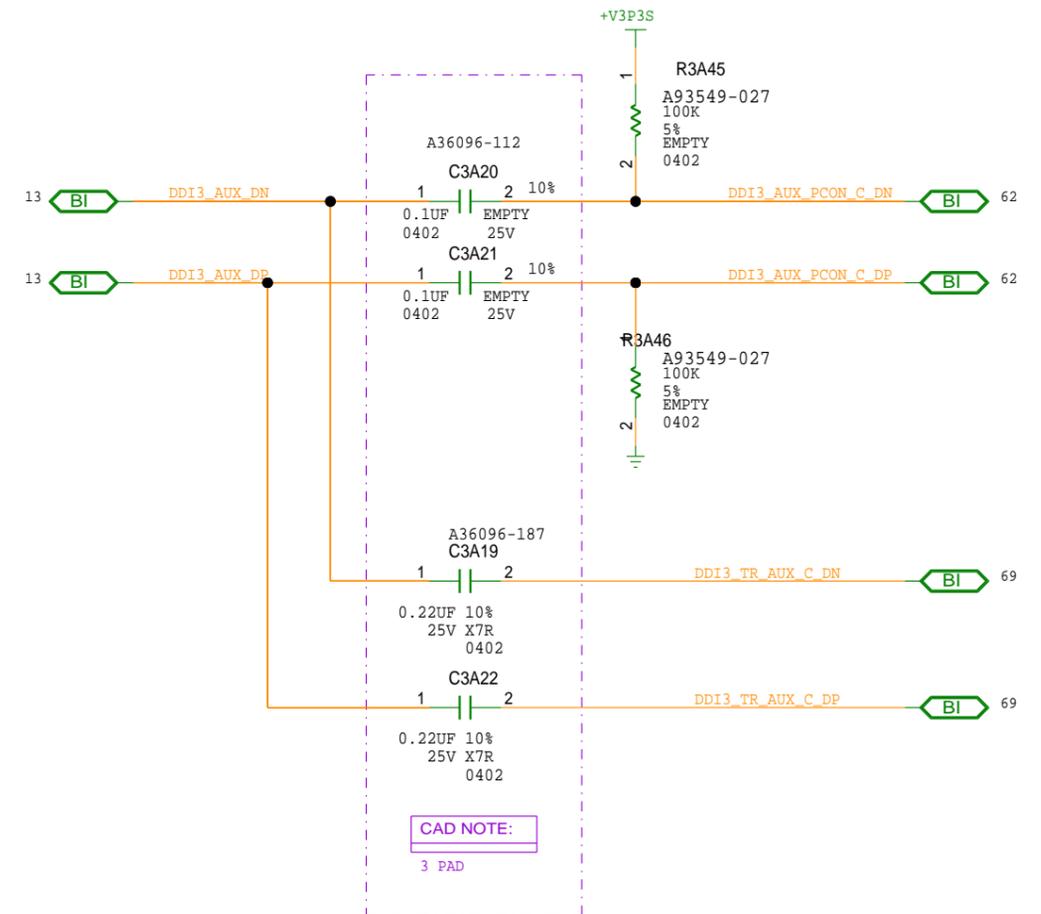
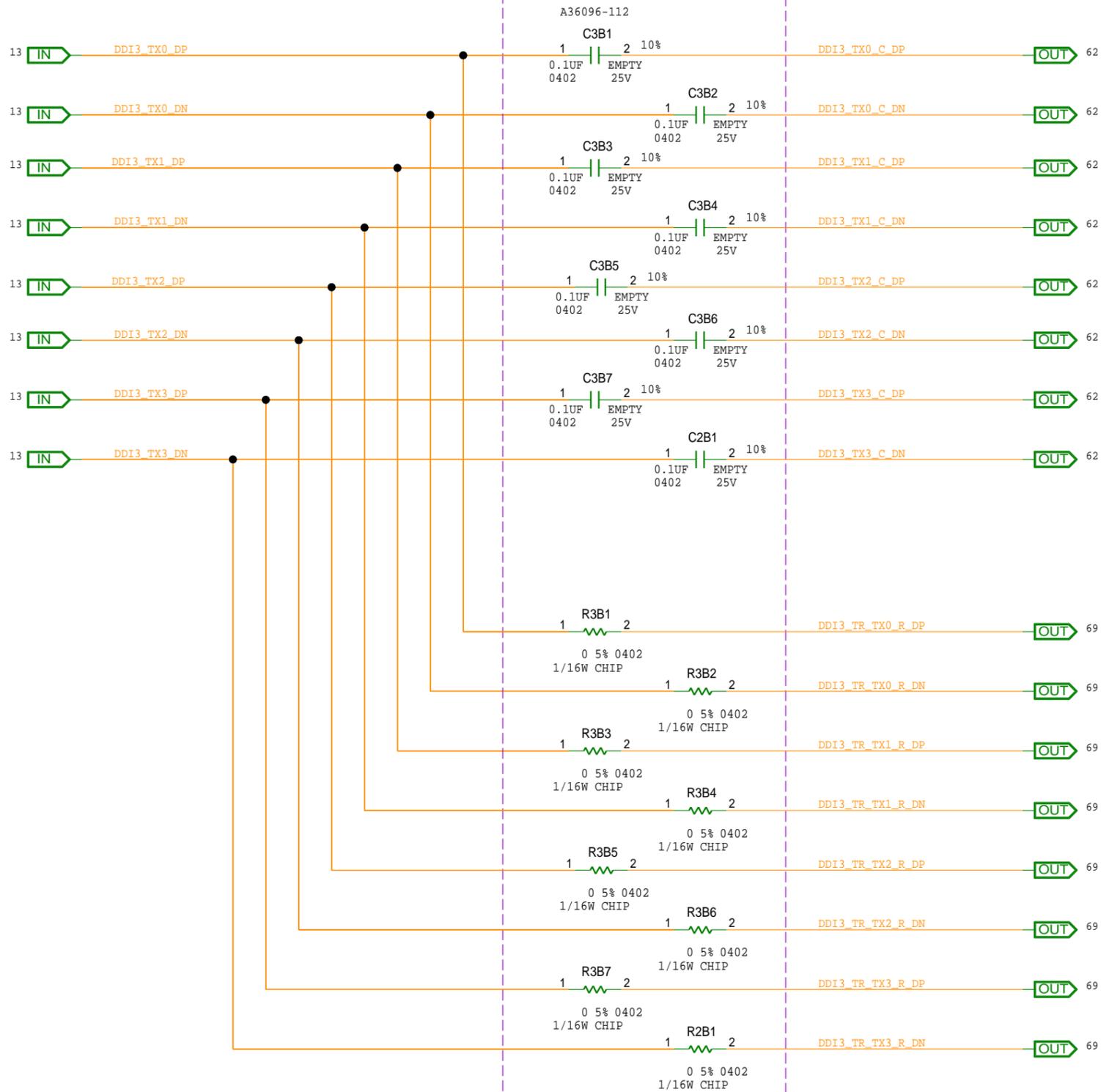
[PAGE_TITLE=DISPLAY - DP_HDMI_COMBO]

BPAGE DRAWING
 udimm_sch_1.60
 Fri Sep 27 16:40:07 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 60	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE



[PAGE_TITLE=DISPLAY - DDI3 PORT, AC CAPS]

BPAGE DRAWING

udimm.sch_1.61
Fri Sep 27 16:40:08 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 61	REV 0.7
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MODULE REV DETAILS

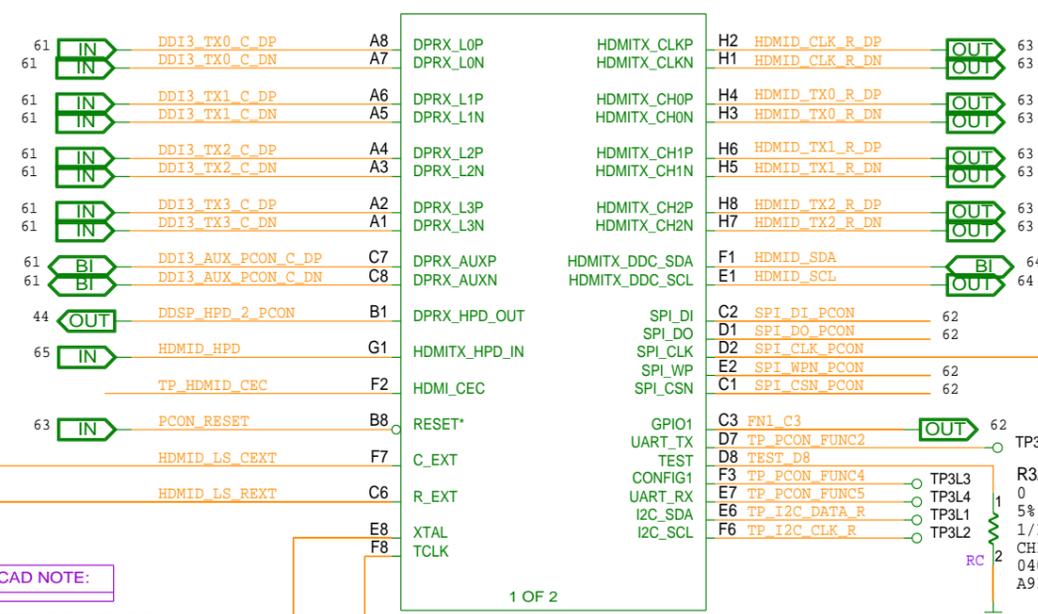
MODULE NAME	REV	DATE

CAD NOTE:

0.1UF DECOUPLING CAPACITORS TO BE PLACED CLOSE TO VDD AND VDDIO PINS

U3A5
IC

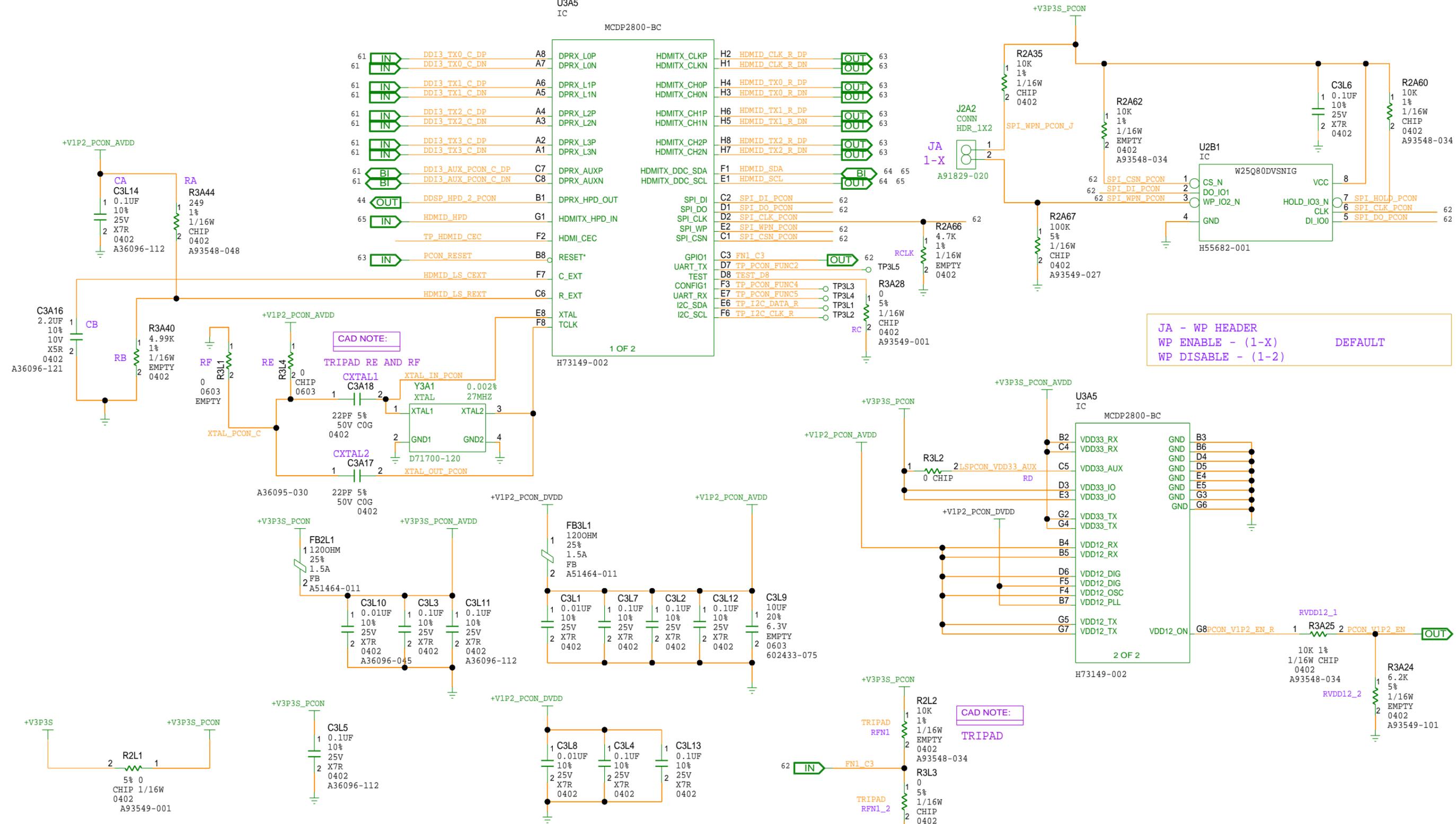
MCDP2800-BC



CAD NOTE:

TRIPAD RE AND RF

JA - WP HEADER
WP ENABLE - (1-X)
WP DISABLE - (1-2)



BPAGE DRAWING

udimm.sch_1.62
Fri Sep 27 16:40:09 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 62	REV 0.7
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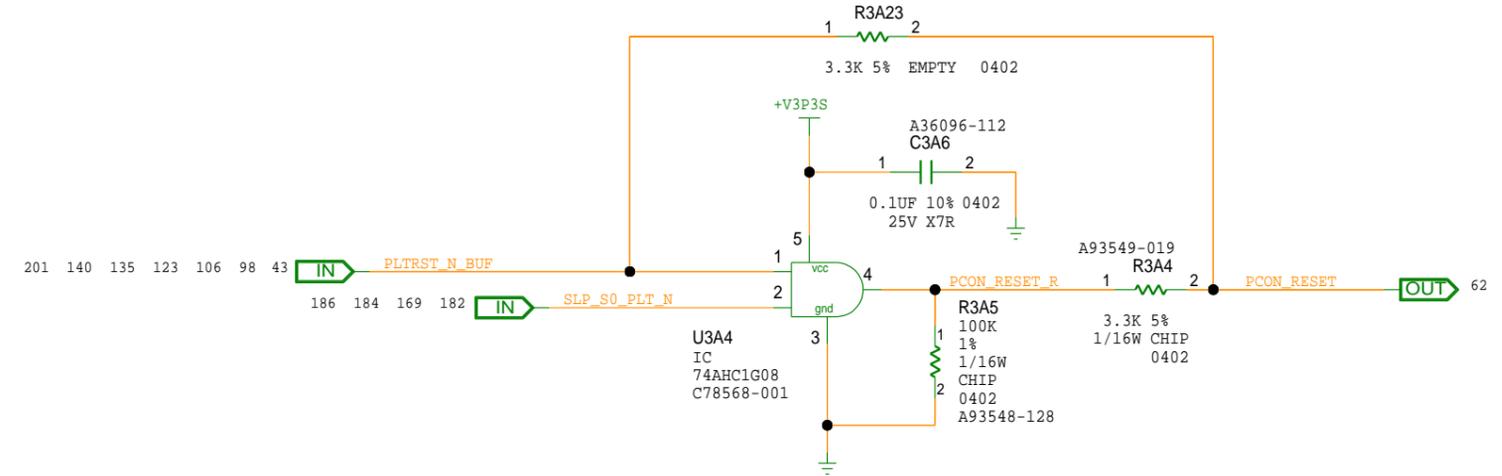
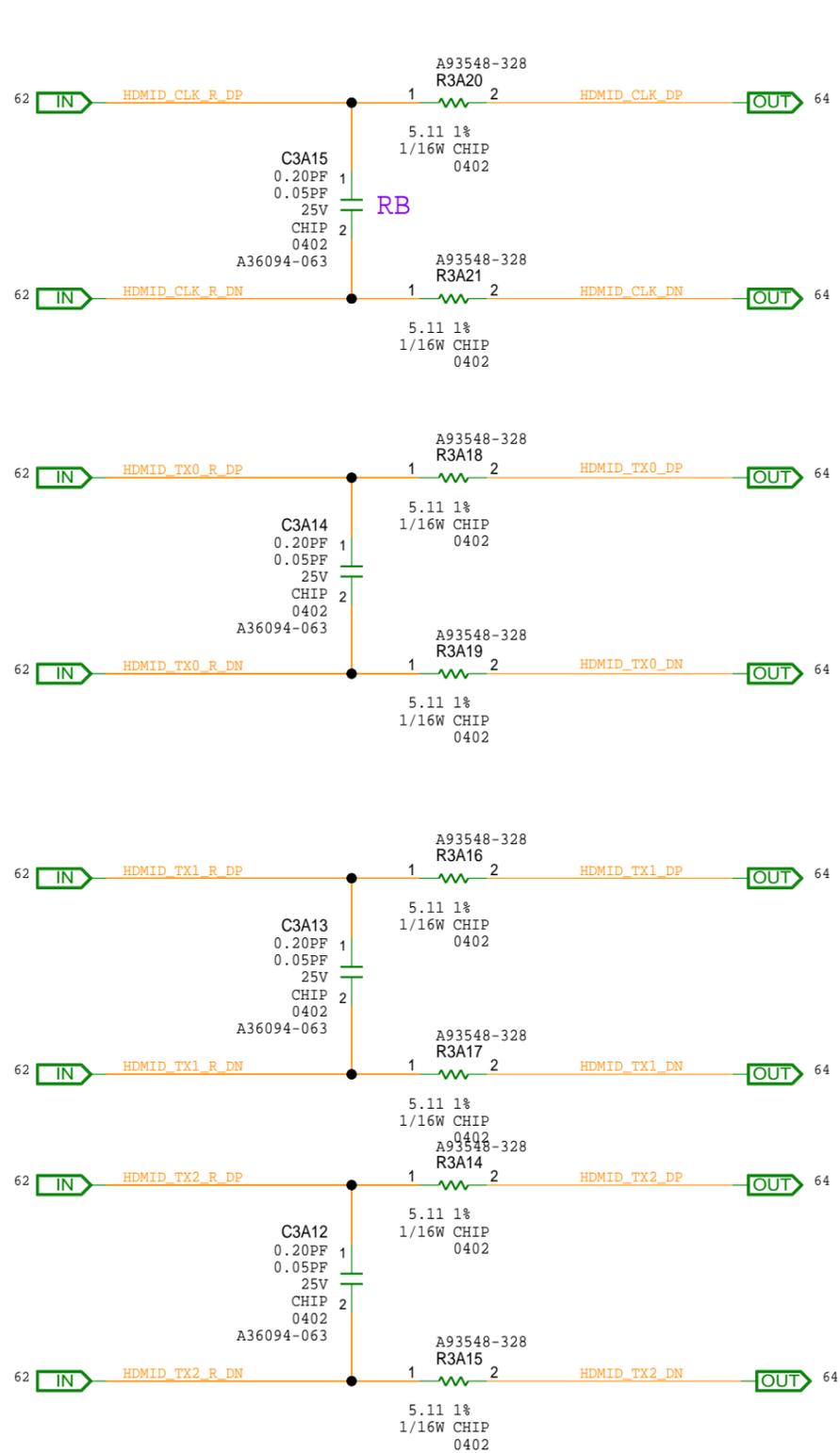
MODULE REV DETAILS

MODULE NAME	REV	DATE

LSPCON RESET

CAD NOTE:

COMMENT_BODY



[PAGE_TITLE=DISPLAY - LSPCON O/P SERIES RESISTOR]

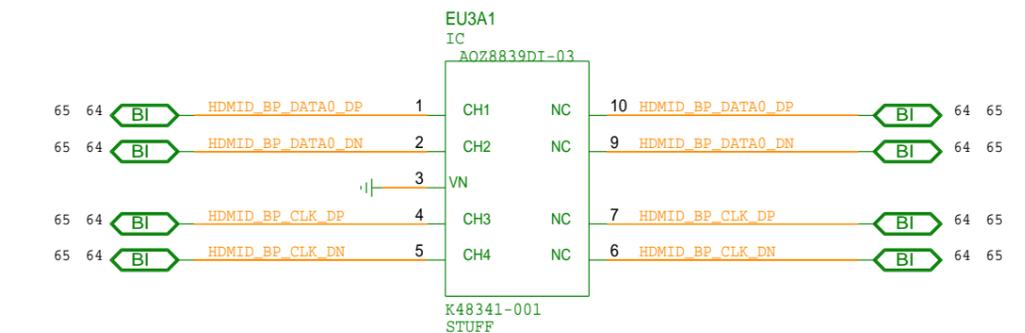
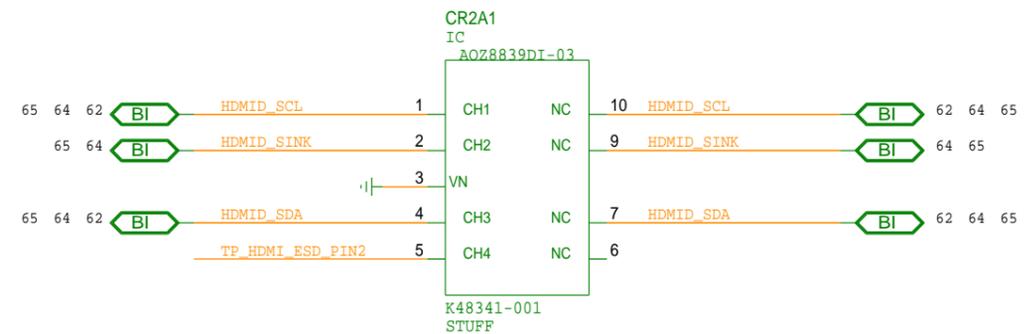
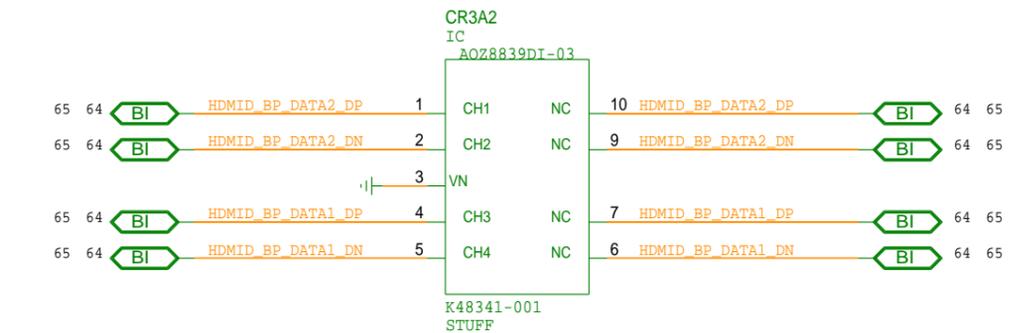
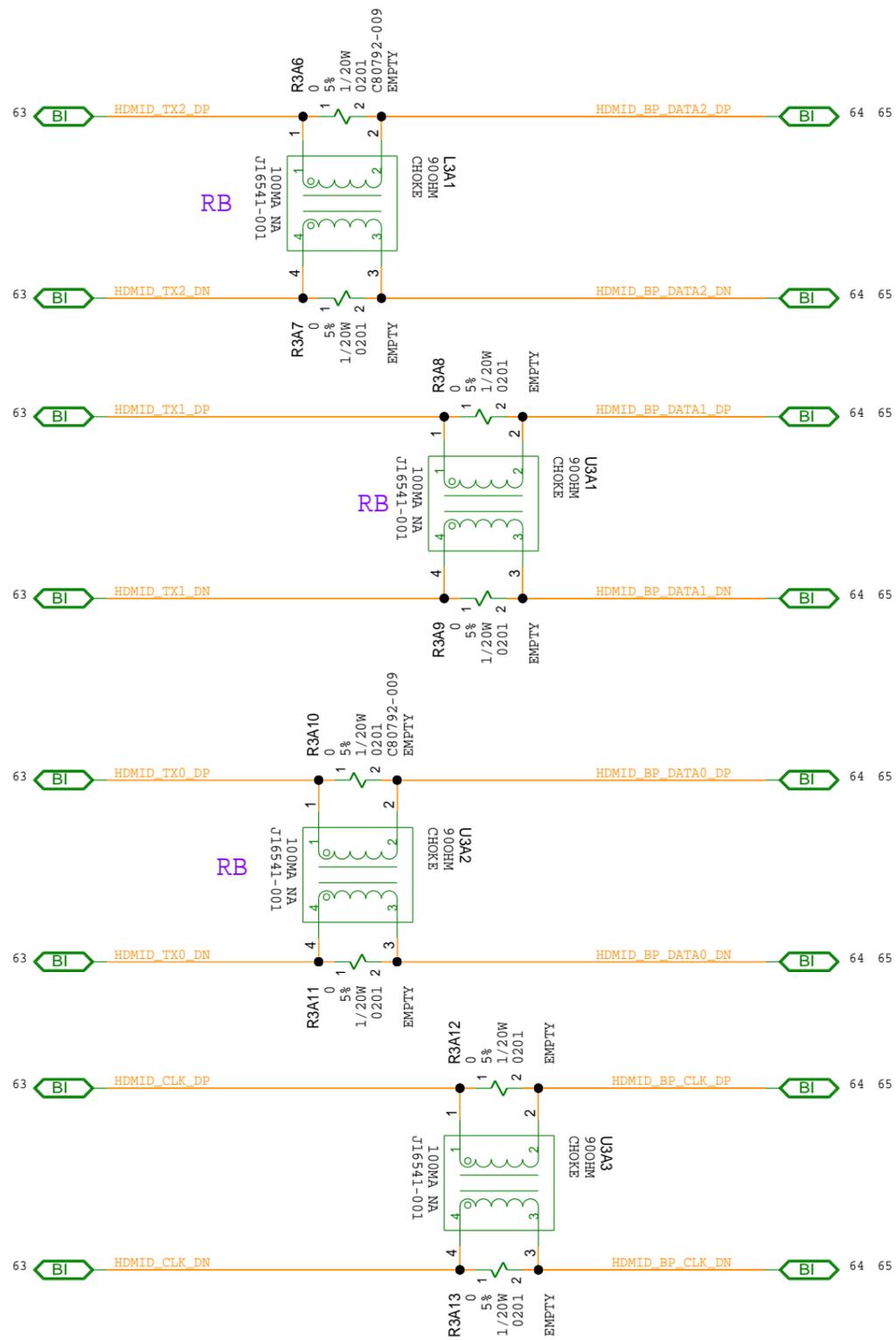
BPAGE DRAWING

udimm.sch_1.63
Fri Sep 27 16:40:10 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 63	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE

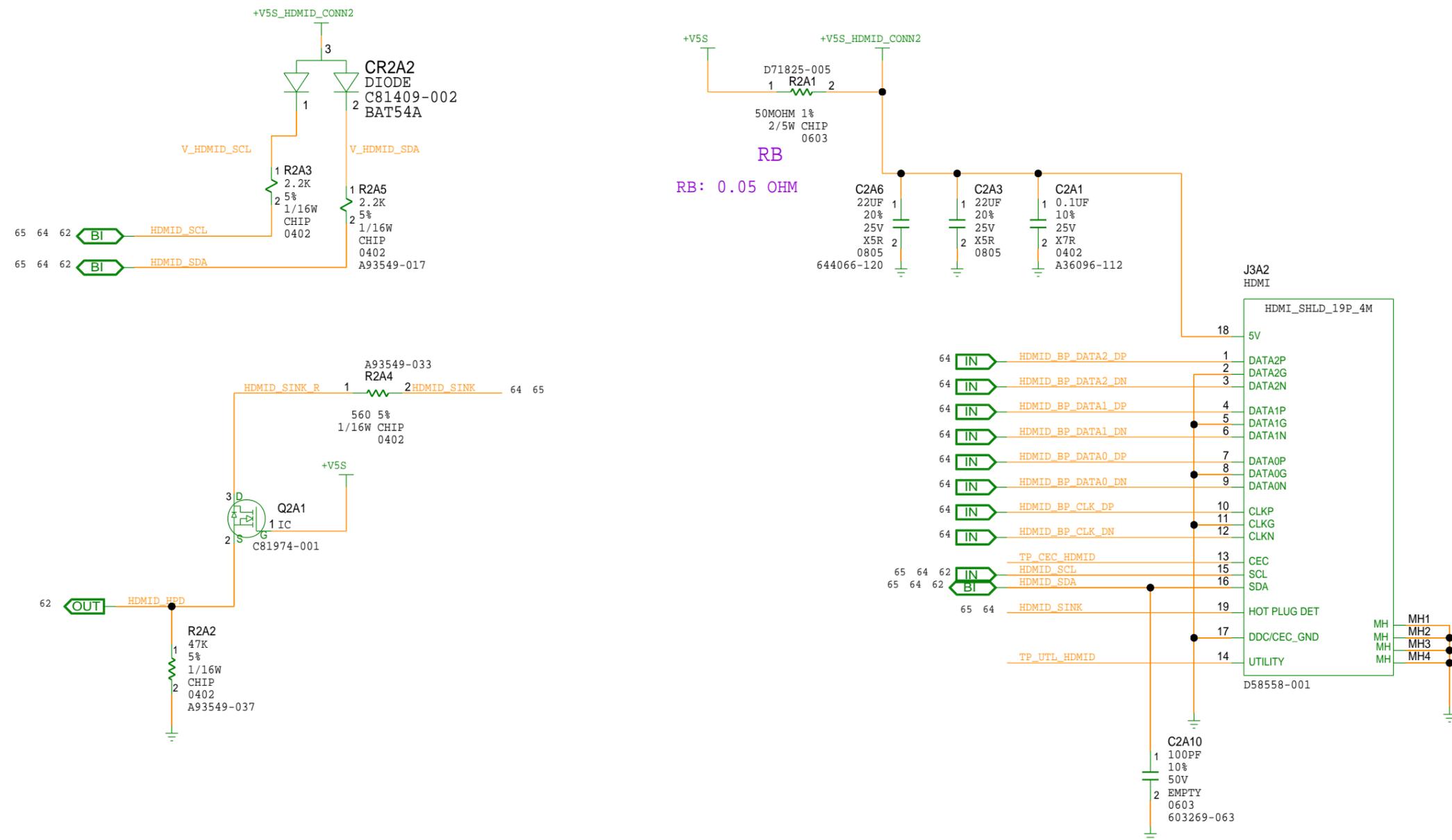


CAD NOTE:

PLACE ESD DIODES NEAR BACK PANEL CONNECTORS

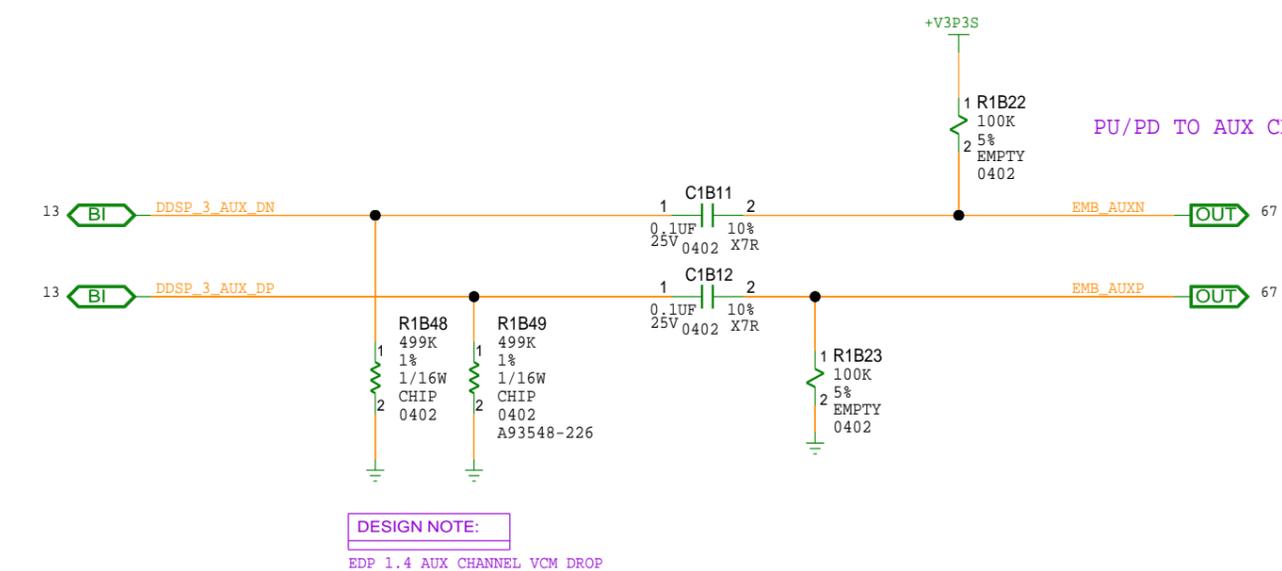
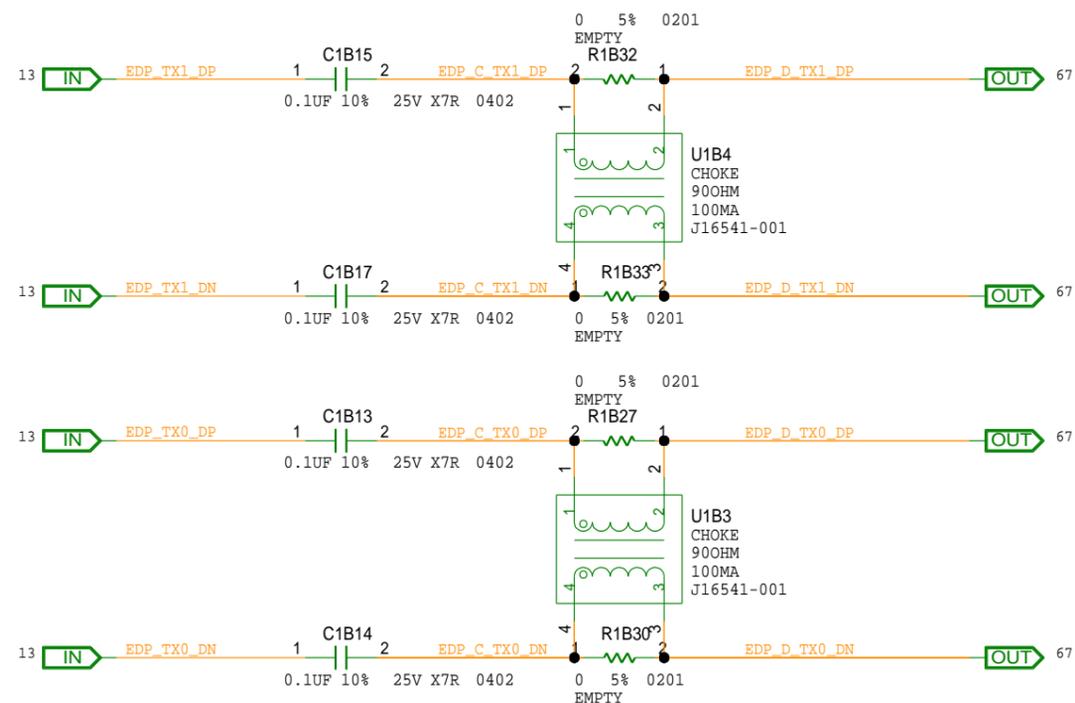
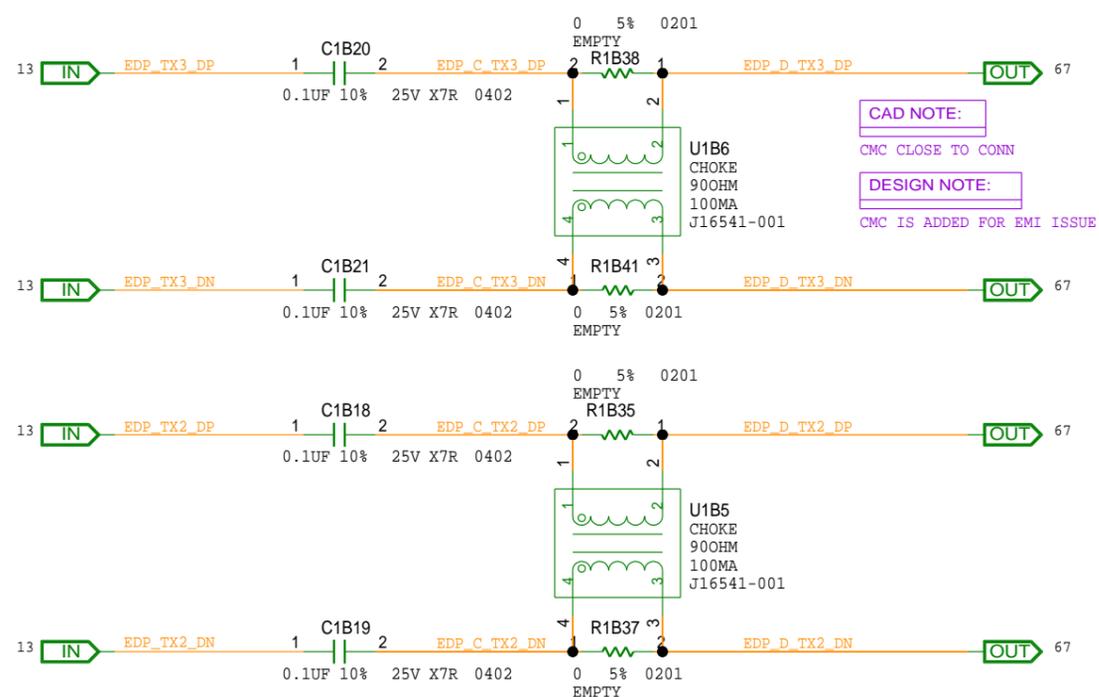
MODULE REV DETAILS

MODULE NAME	REV	DATE



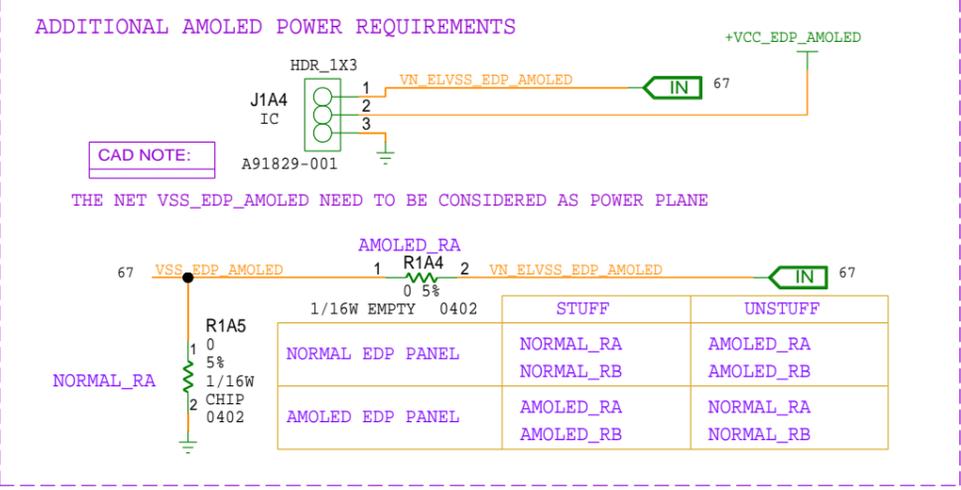
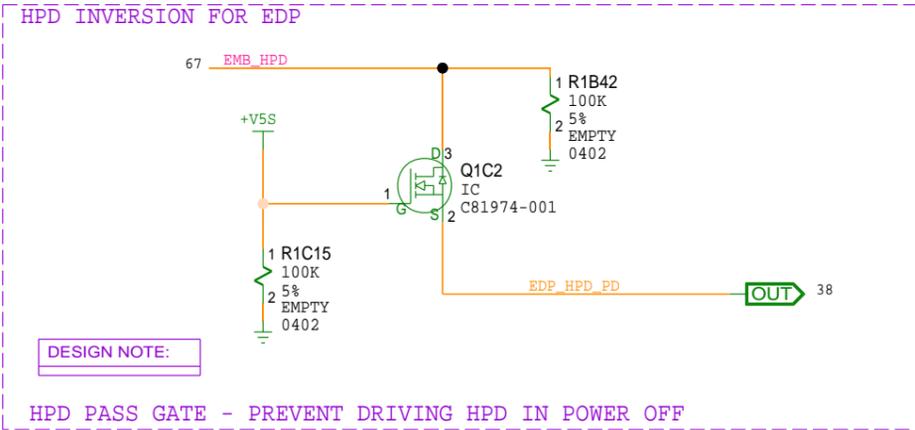
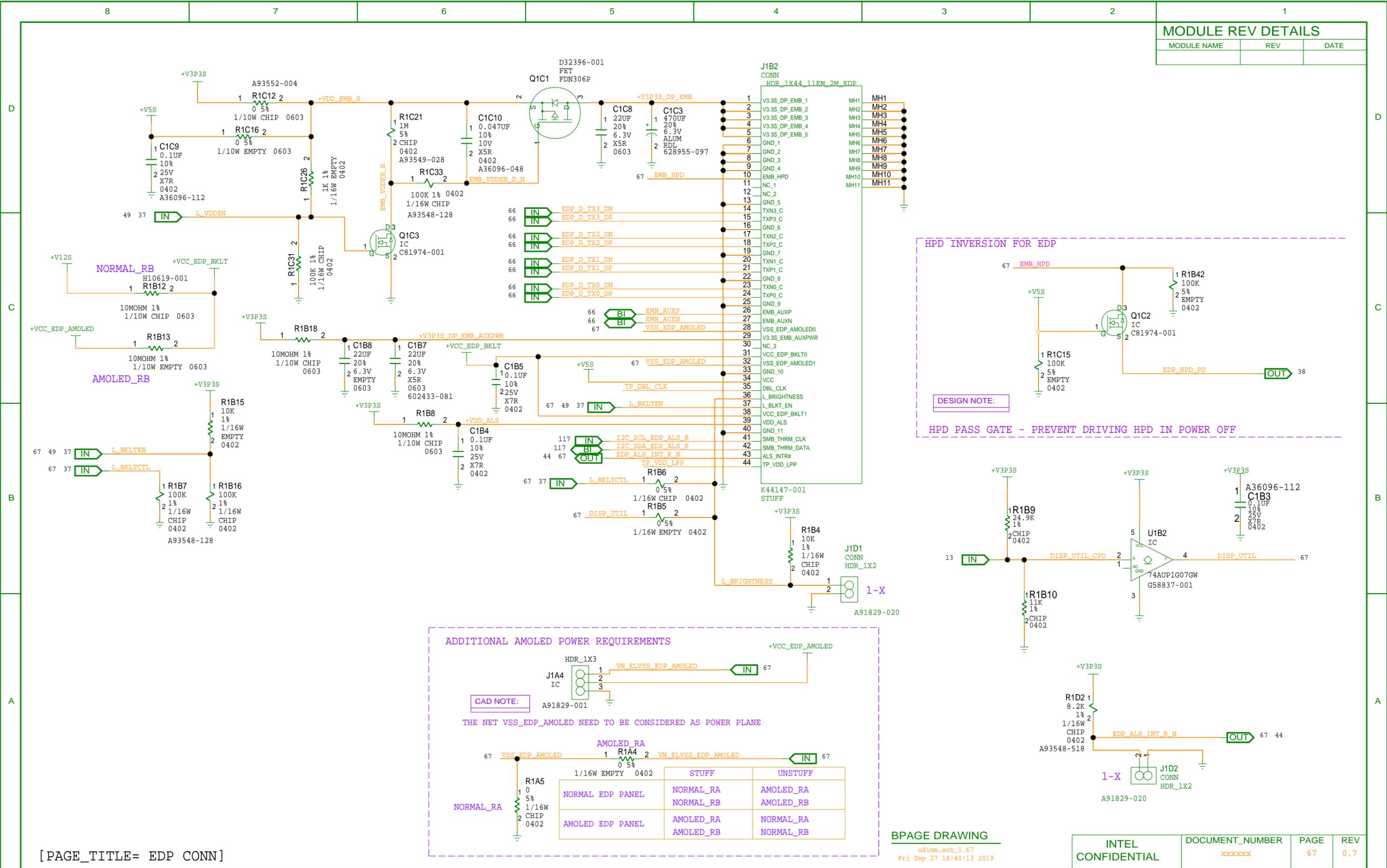
MODULE REV DETAILS

MODULE NAME	REV	DATE



MODULE REV DETAILS

MODULE NAME	REV	DATE



BPAGE DRAWING
udimm_sch_1.67
Fri Sep 27 16:40:13 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 67	REV 0.7
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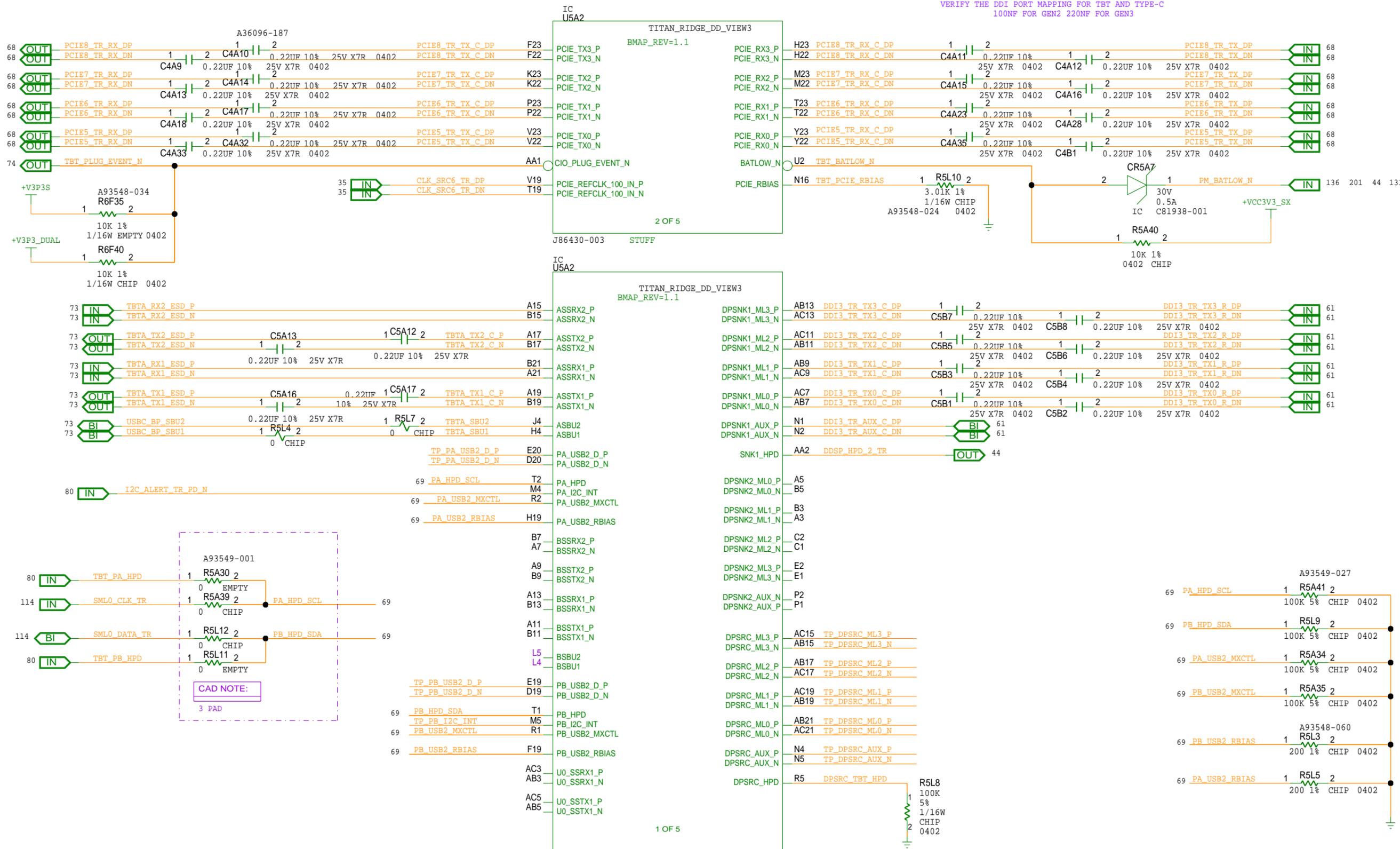
[PAGE_TITLE= EDP CONN]

TYPE-C PORT0-TBT

MODULE REV DETAILS

MODULE NAME	REV	DATE

VERIFY THE DDI PORT MAPPING FOR TBT AND TYPE-C
100NF FOR GEN2 220NF FOR GEN3



BPAGE DRAWING

udimm.sch_1.69
Fri Sep 27 16:40:15 2019

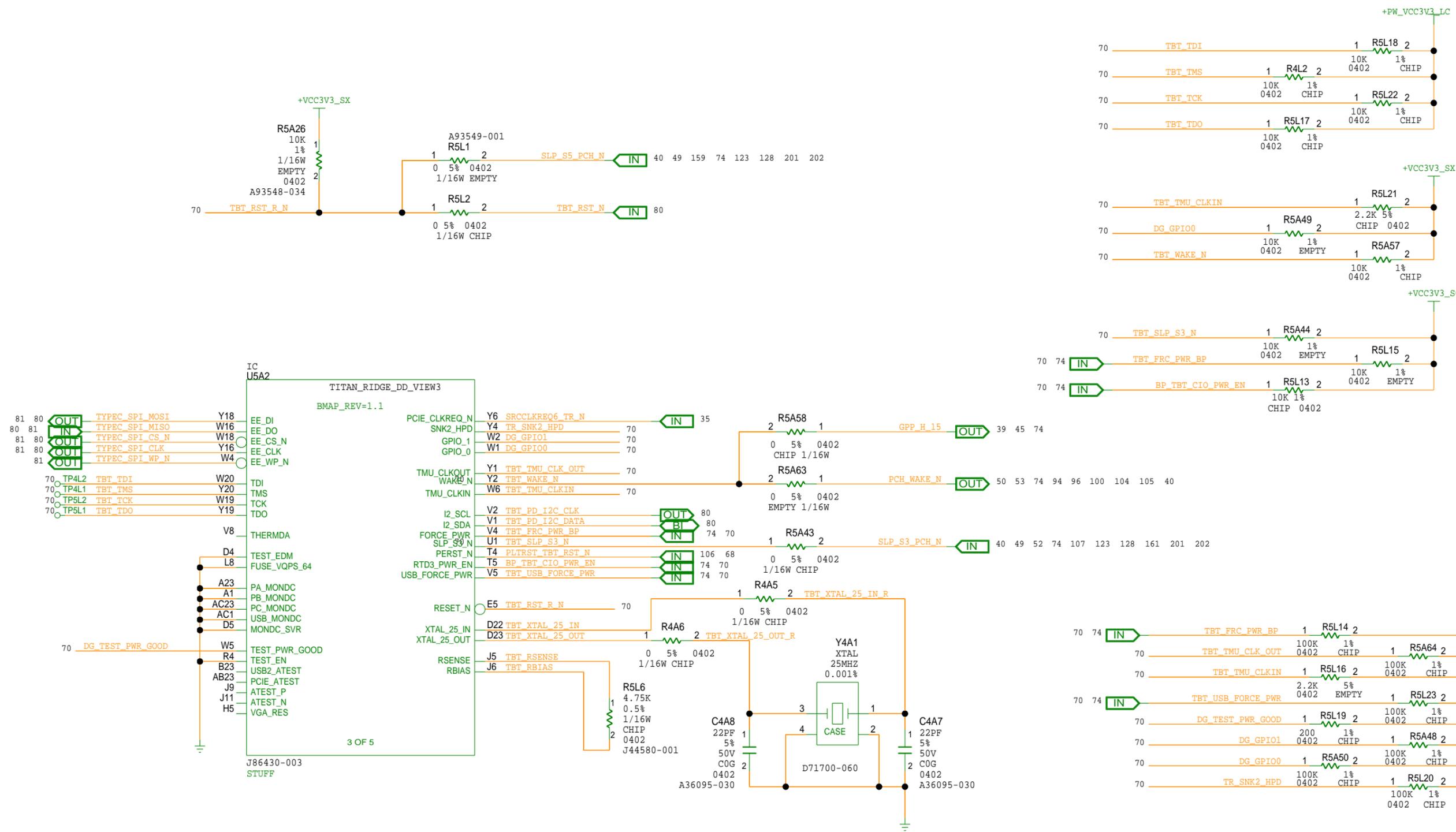
INTEL CONFIDENTIAL	DOCUMENT NUMBER xxxxxxx	PAGE 69	REV 0.7
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[PAGE_TITLE=TYPE-C PORT - TBT]

MODULE REV DETAILS

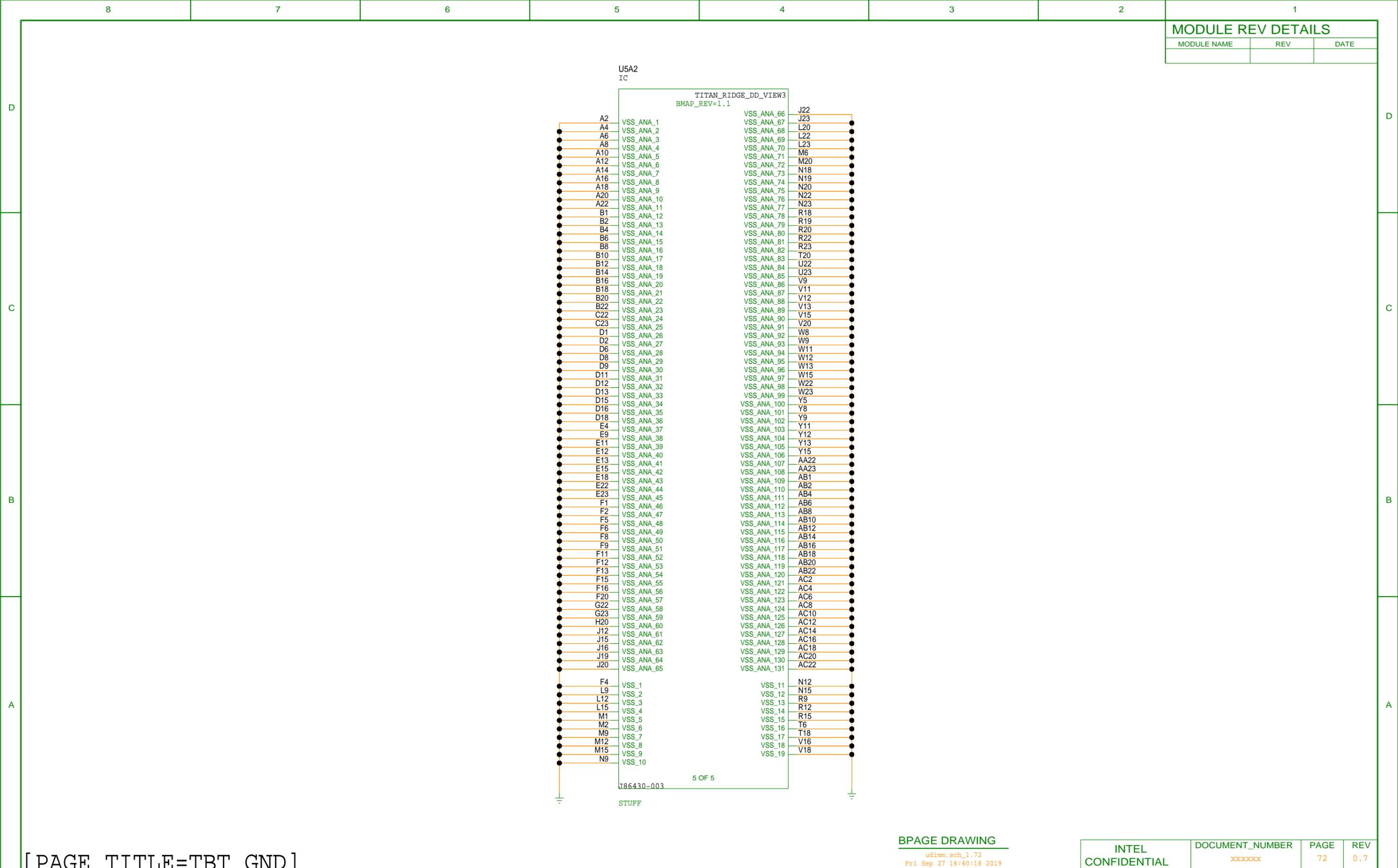
MODULE NAME	REV	DATE

TYPE-C PORT0-TBT



MODULE REV DETAILS

MODULE NAME	REV	DATE



[PAGE_TITLE=TBT GND]

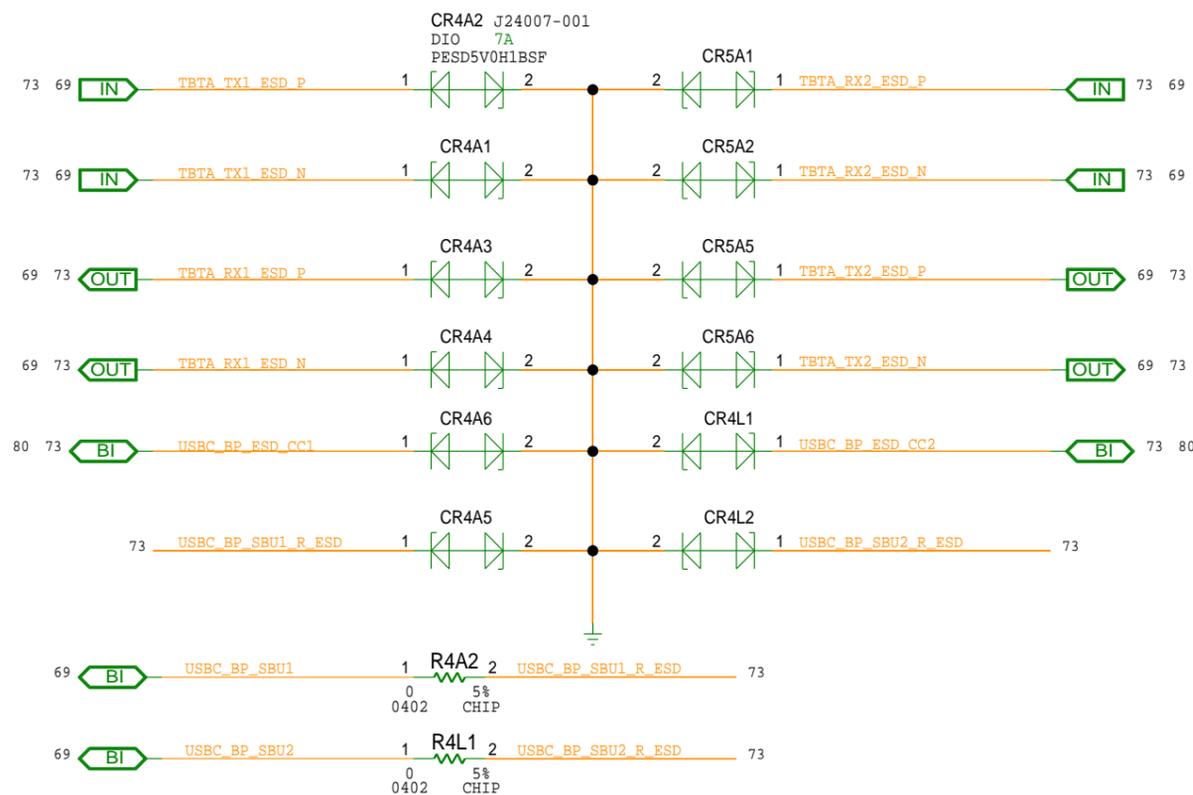
BPAGE DRAWING

udimm.sch_1.72
Fri Sep 27 16:40:18 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 72	REV 0.7
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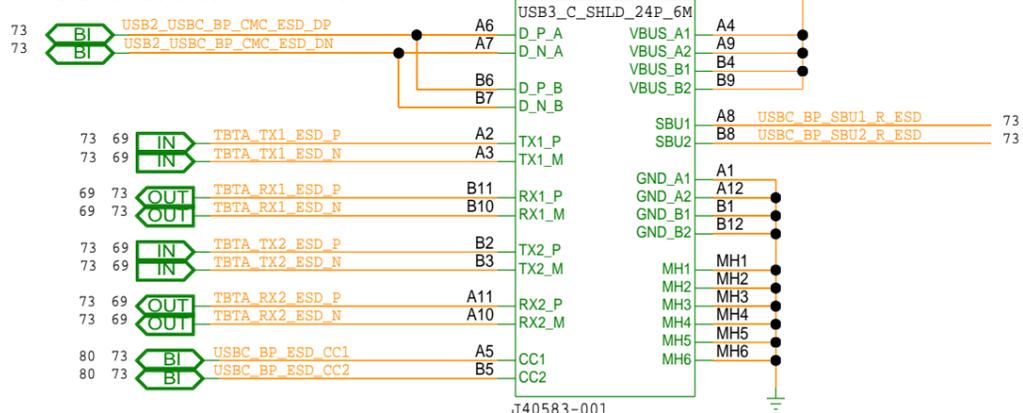
MODULE REV DETAILS

MODULE NAME	REV	DATE



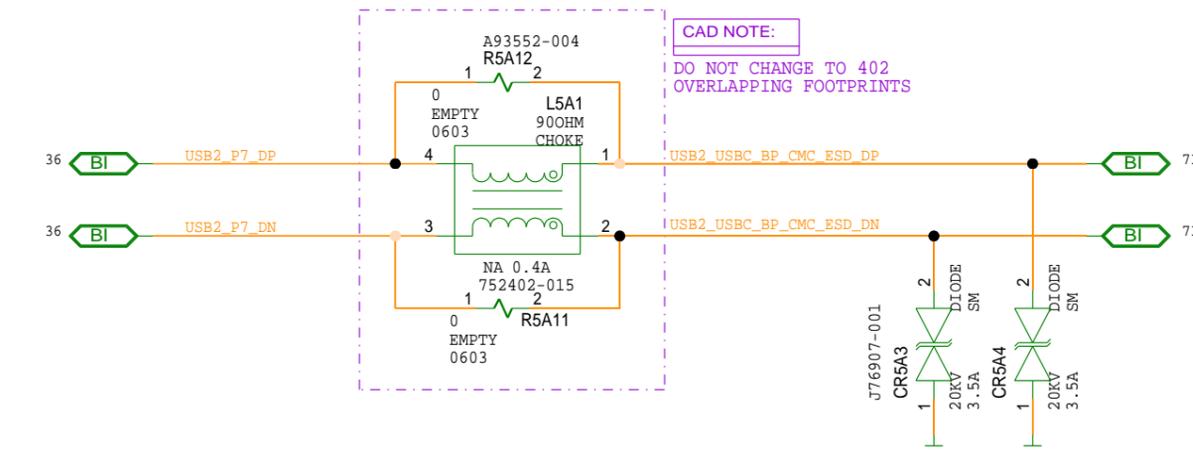
CAD NOTE:

PER PDG
STUB ON USBC CONN <140 MILS



CAD NOTE:

DO NOT CHANGE TO 402
OVERLAPPING FOOTPRINTS



[PAGE_TITLE= TBT TYPEC PORT]

[PAGE_TITLE= TBT TYPEC PORT]

BPAGE DRAWING

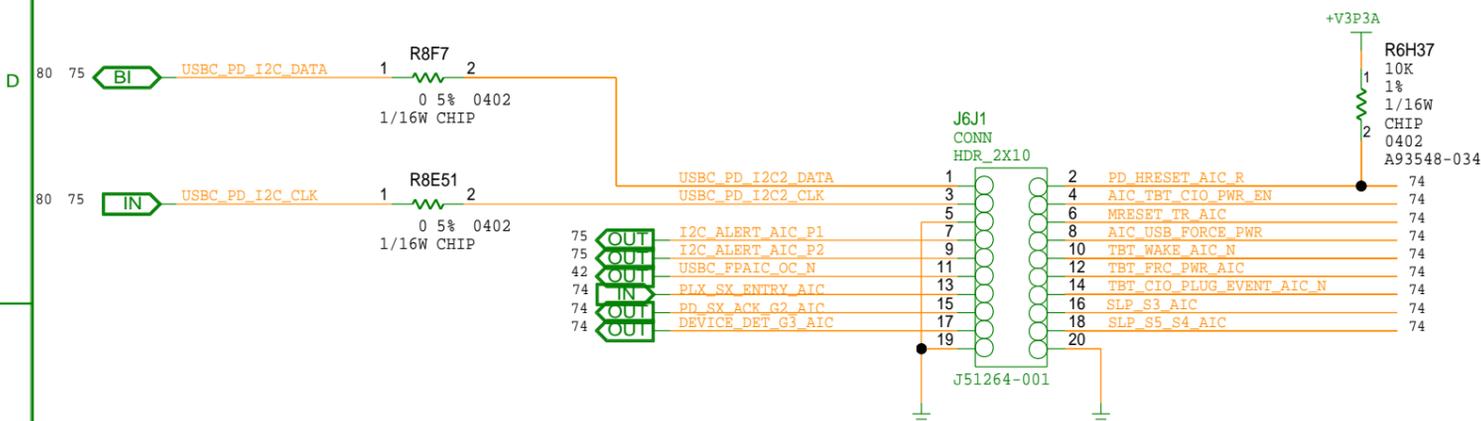
udimm_sch_1.73
Fri Sep 27 16:40:19 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 73	REV 0.7
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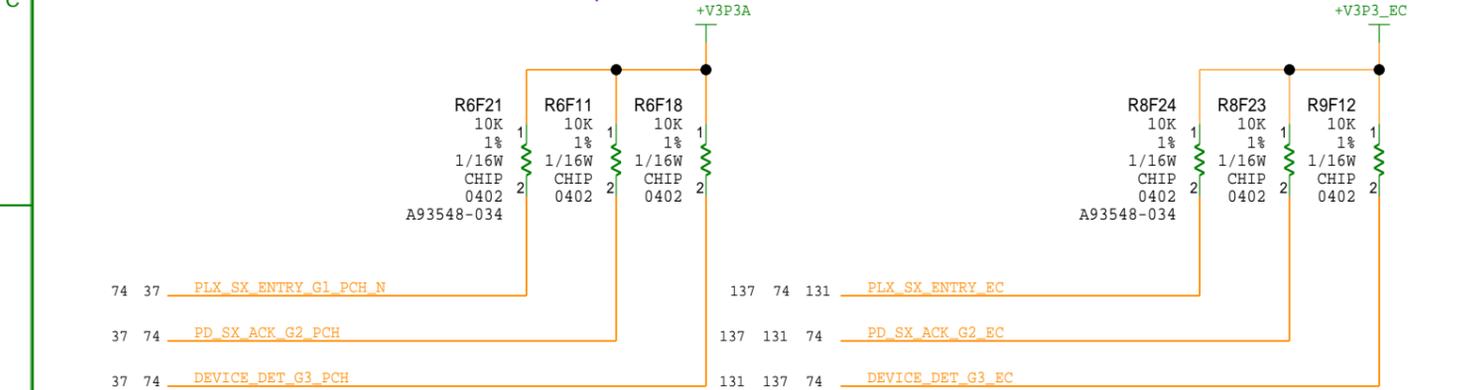
MODULE REV DETAILS

MODULE NAME	REV	DATE

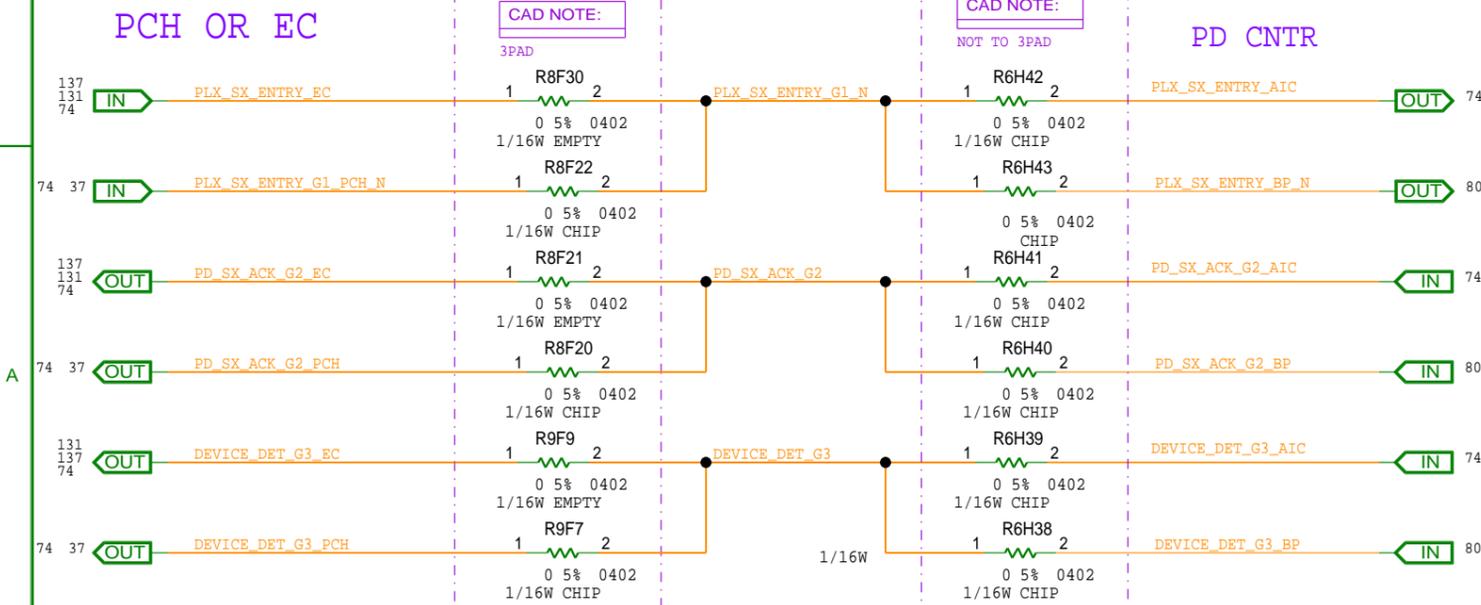
FP TYPE-C AIC SIDEBAND HEADER



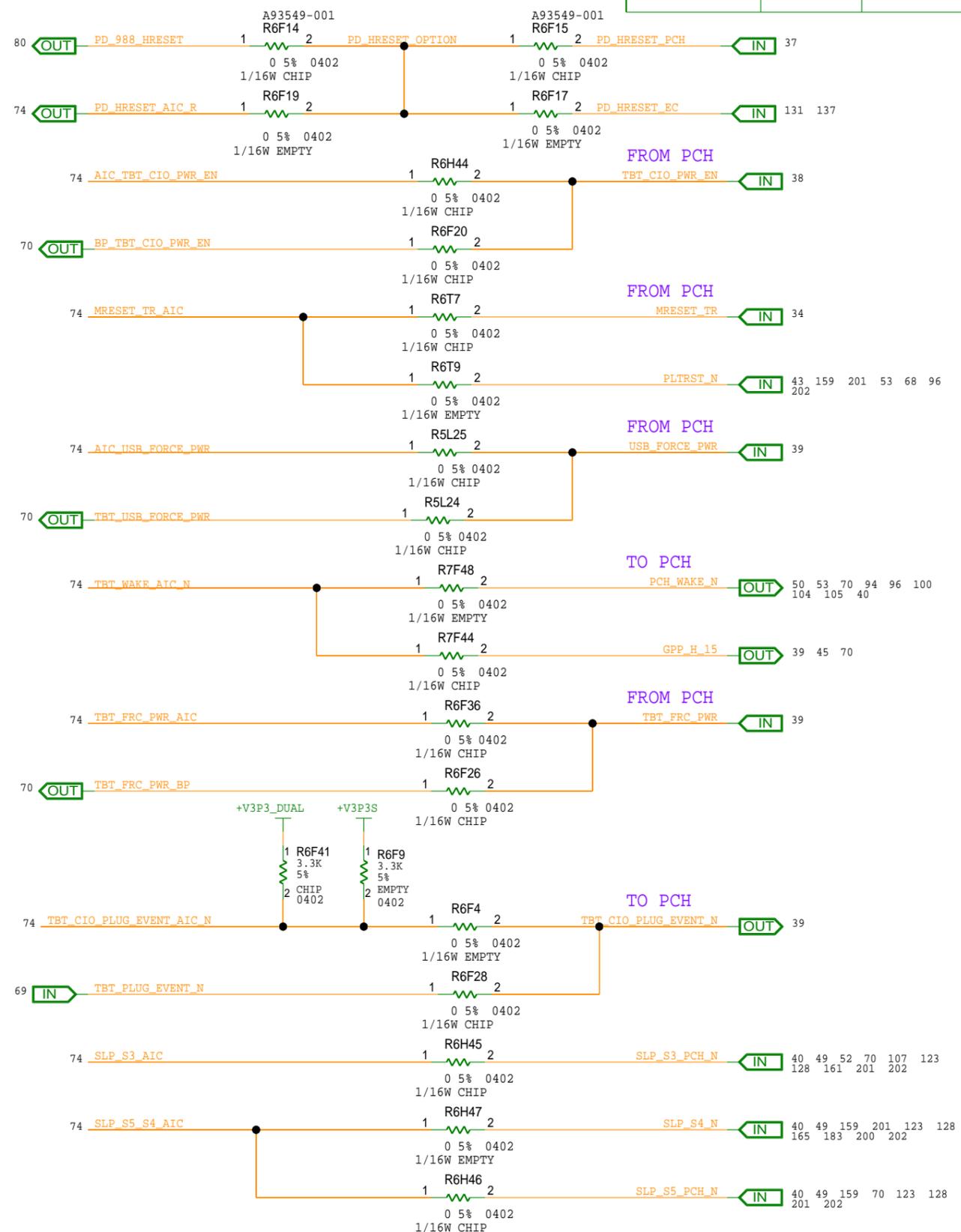
GPIOS FOR SX ENTRY/EXIT NOTICE



PCH OR EC



PD CNTR

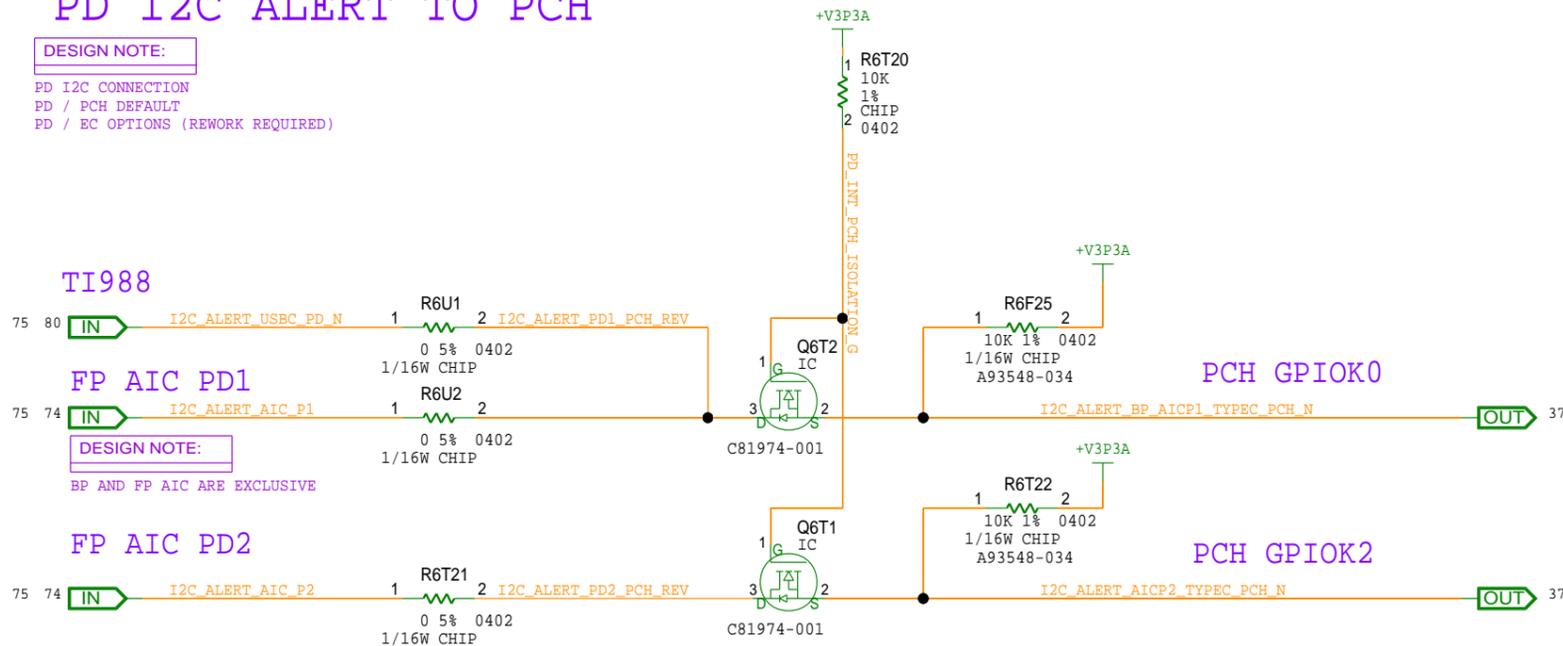


USBC PD I2C OPTIONS

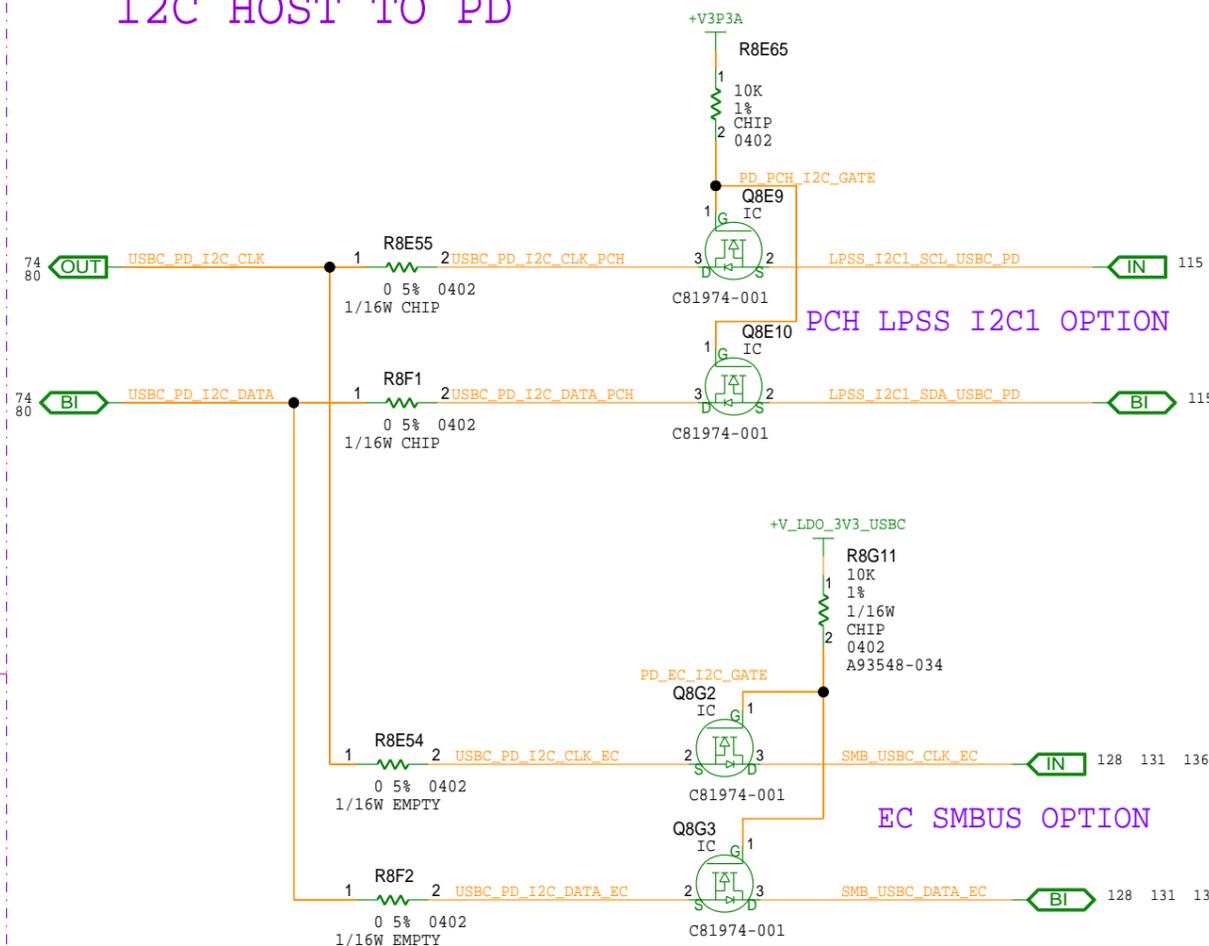
MODULE REV DETAILS		
MODULE NAME	REV	DATE

PD I2C ALERT TO PCH

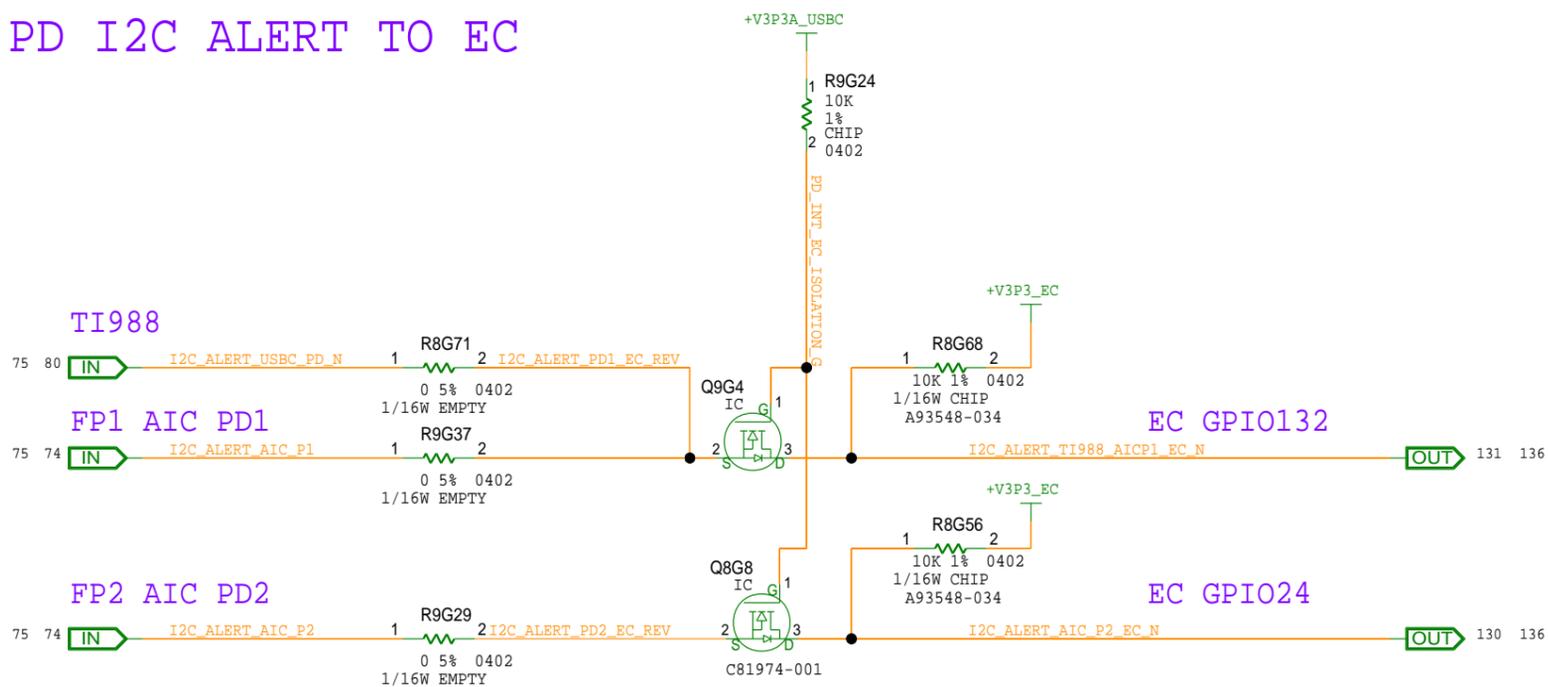
DESIGN NOTE:
 PD I2C CONNECTION
 PD / PCH DEFAULT
 PD / EC OPTIONS (REWORK REQUIRED)



I2C HOST TO PD



PD I2C ALERT TO EC



[PAGE_TITLE=TYPE-C PORTS - PD I2C OPTIONS]

BPAGE DRAWING

udimm_sch_1.75
 Fri Sep 27 16:40:21 2019

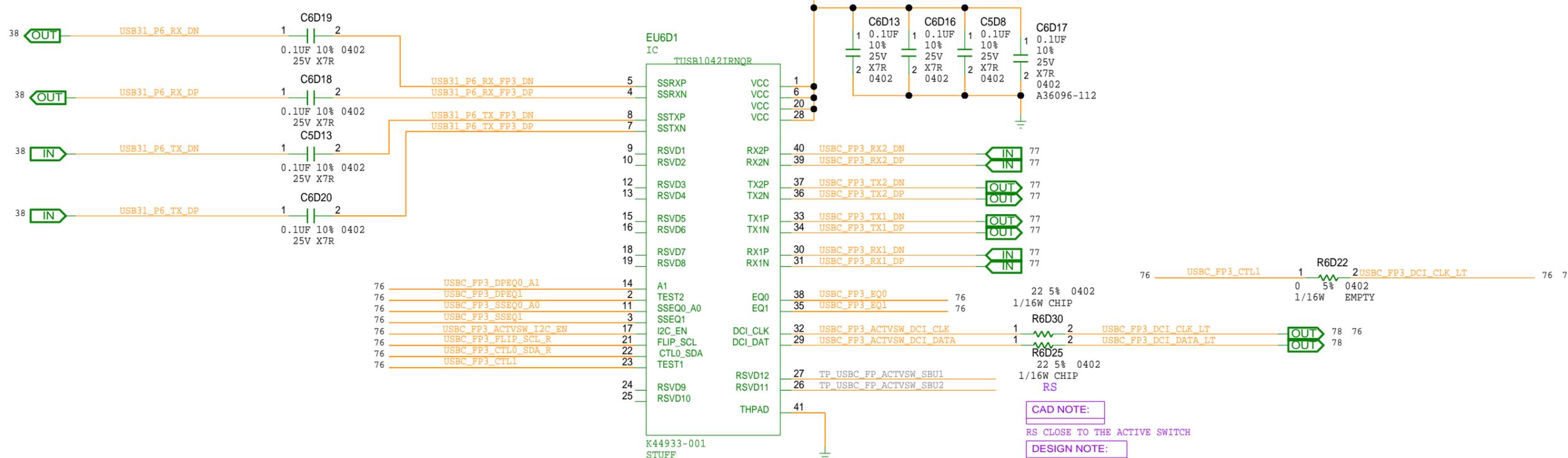
INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 75	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE

DESIGN NOTE:

USB31 PORT 6 P & N SWAP FOR PCB LAYOUT

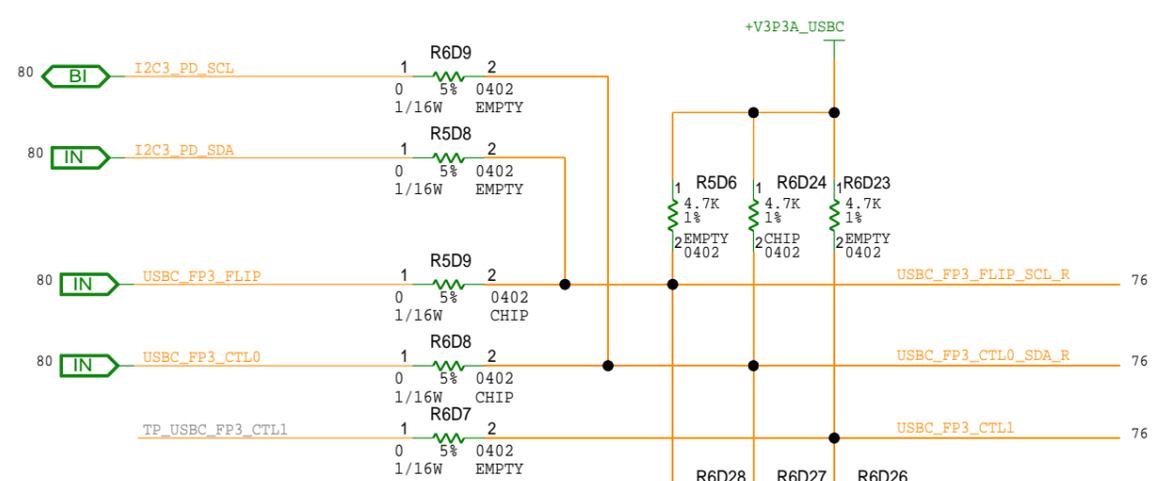


CAD NOTE:

RS CLOSE TO THE ACTIVE SWITCH

DESIGN NOTE:

PIN29/32
IN GPIO MODE, PIN29/32 = DCI_DAT/DCI_CLK
IN I2C MODE, PIN29/32 = CAD_SNK/HPDIN



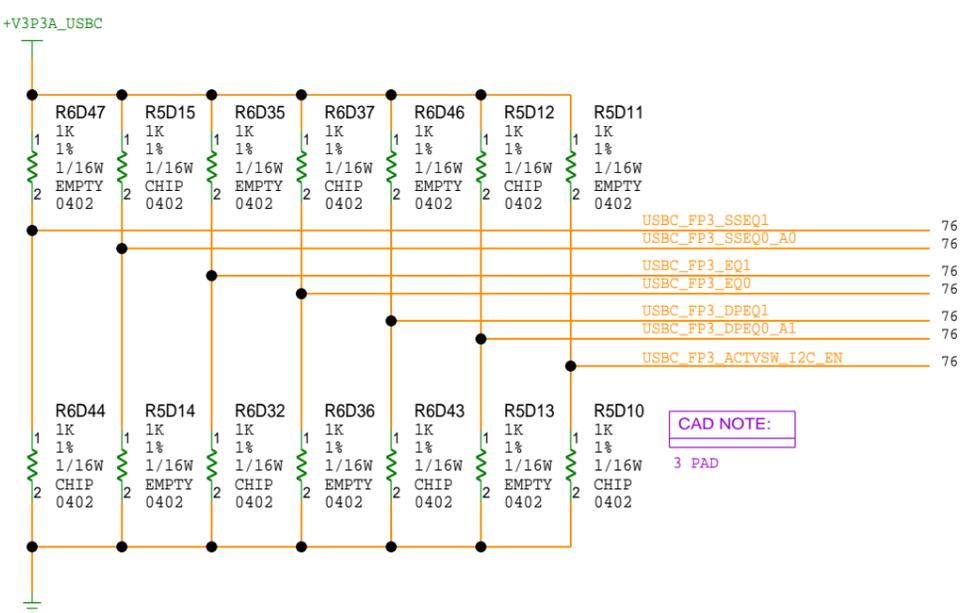
DESIGN NOTE:

TUSB104X GPIO CONFIG.WHILE I2C_EN=0

CTL1/CTL0/FLIP	104X CFG	DP CFG	AUX?=SBU?
L /L /L	PWR DOWN	NA	NA
L /L /H	PWR DOWN	NA	
L /H /L	USB NO FLIP	NA	
L /H /H	USB FLIP	NA	
H /L /L	4*DP NO FLIP	C AND E	P=1/N=2
H /L /H	4*DP FLIP	C AND E	P=2/N=1
H /H /L	USB+2*DP NO FLIP	D AND F	P=1/N=2
H /H /H	USB+2*DP FLIP	D AND F	P=2/N=1

CAD NOTE:

3 PAD



CAD NOTE:

3 PAD

DESIGN NOTE:

TUSB104X 4-LEVEL INPUTS
0 > 1K PD OR GND DIRECTLY
R > 20K PD
F > OPEN
1 > 1K PU OR VCC DIRECTLY

DESIGN NOTE:

TUSB104X EQ SETTING WITH DEFALUT BOM
USB UFP | SSEQ1/0 = 01 | 1.4DB
USB DFP | EQ1/0 = 01 | 3.2DB
DP | DPEQ1/0 = 01 | 6.5DB

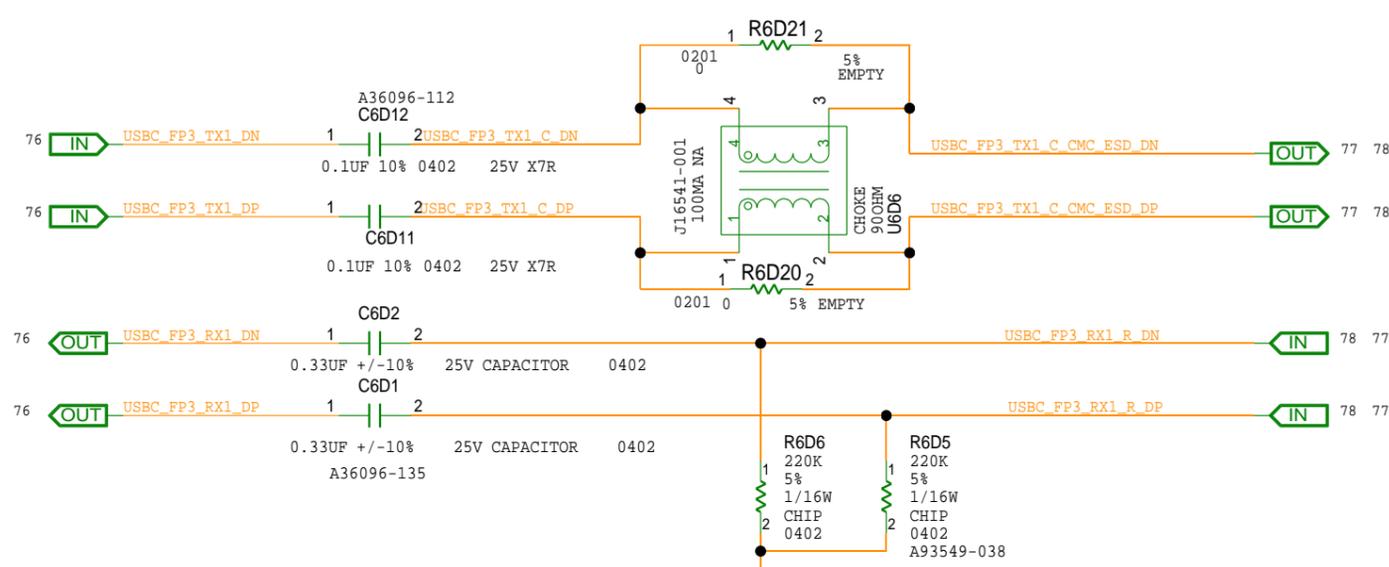
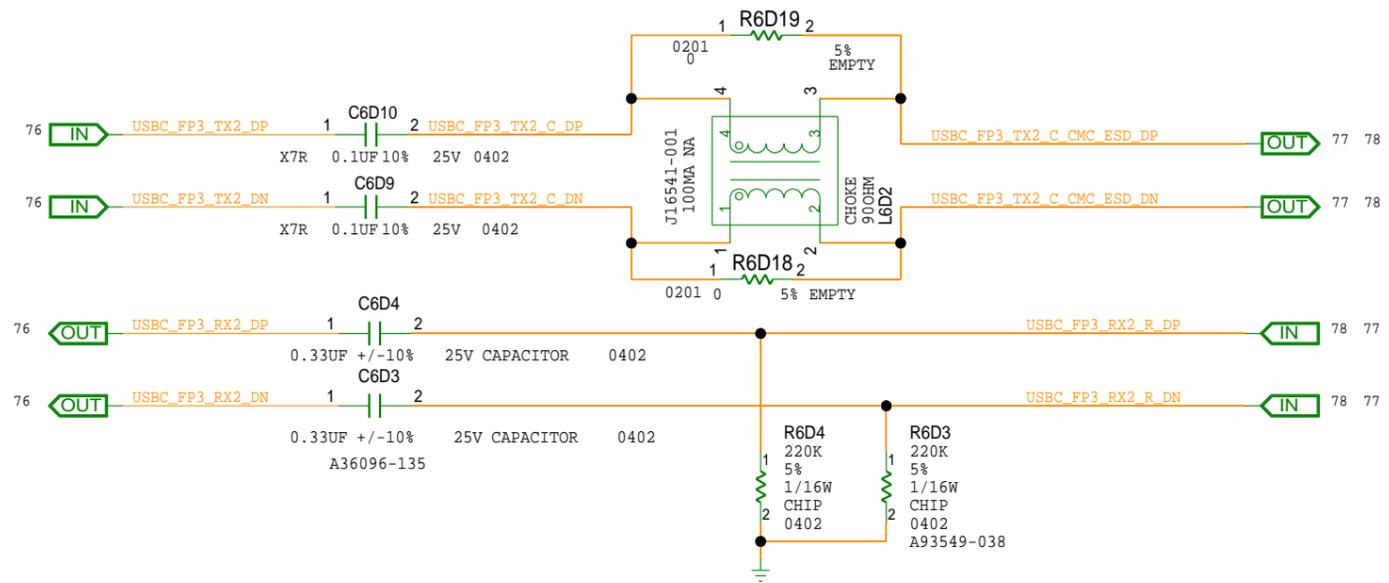
DESIGN NOTE:

TUSB104X I2C_EN STRAP
0 > GPIO (DEFAULT)
R > TI TEST MODE (I2C@3.3V)
F > I2C@1.8V
1 > I2C@3.3V
ONCE IN I2C MODE WITH DEFAULT A0/A1 STRAP ADDRESS = 0X0F(7BIT)

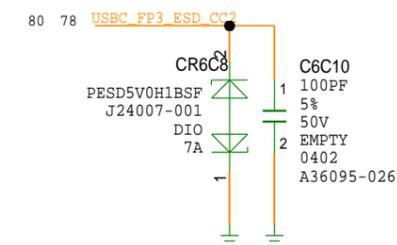
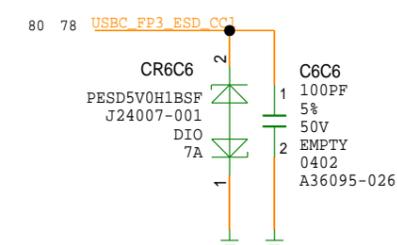
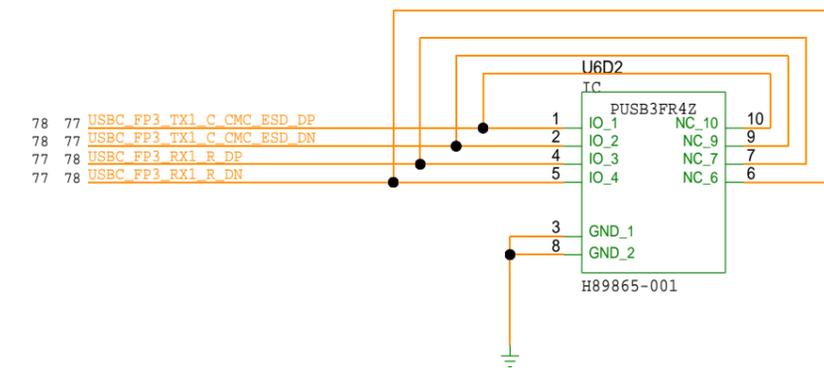
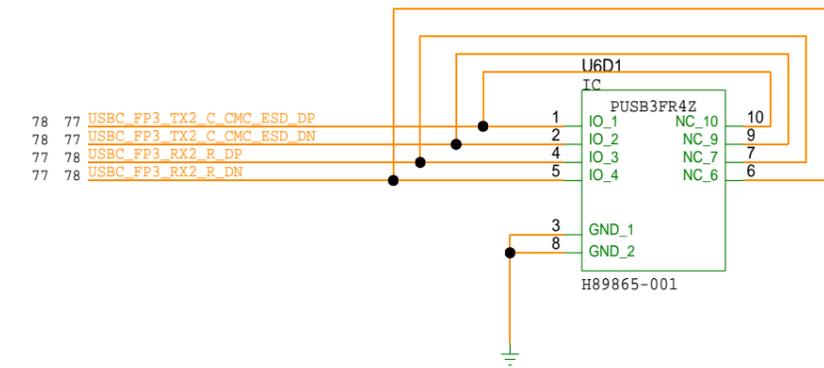
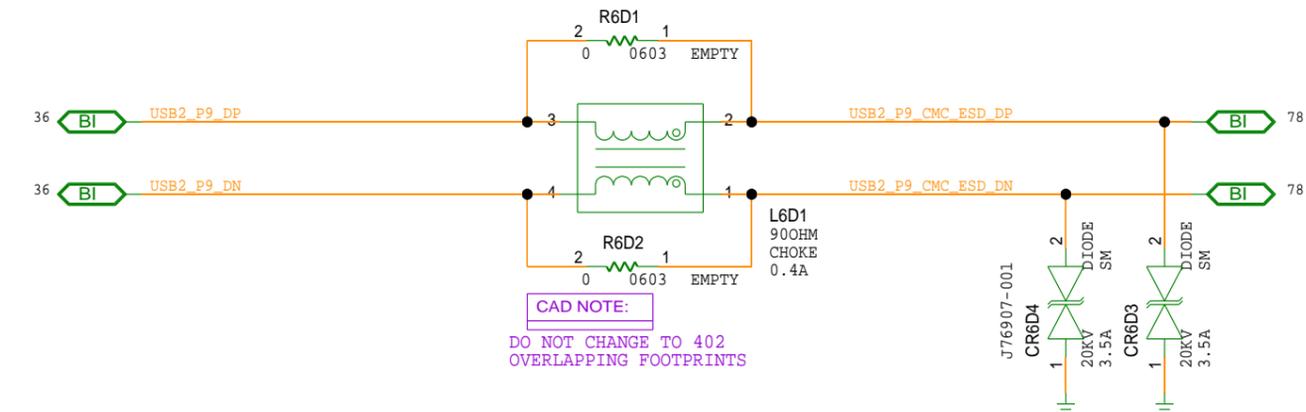
MODULE REV DETAILS

MODULE NAME	REV	DATE

USB31 P6 WITH 1:2 MUX CMC+ESD

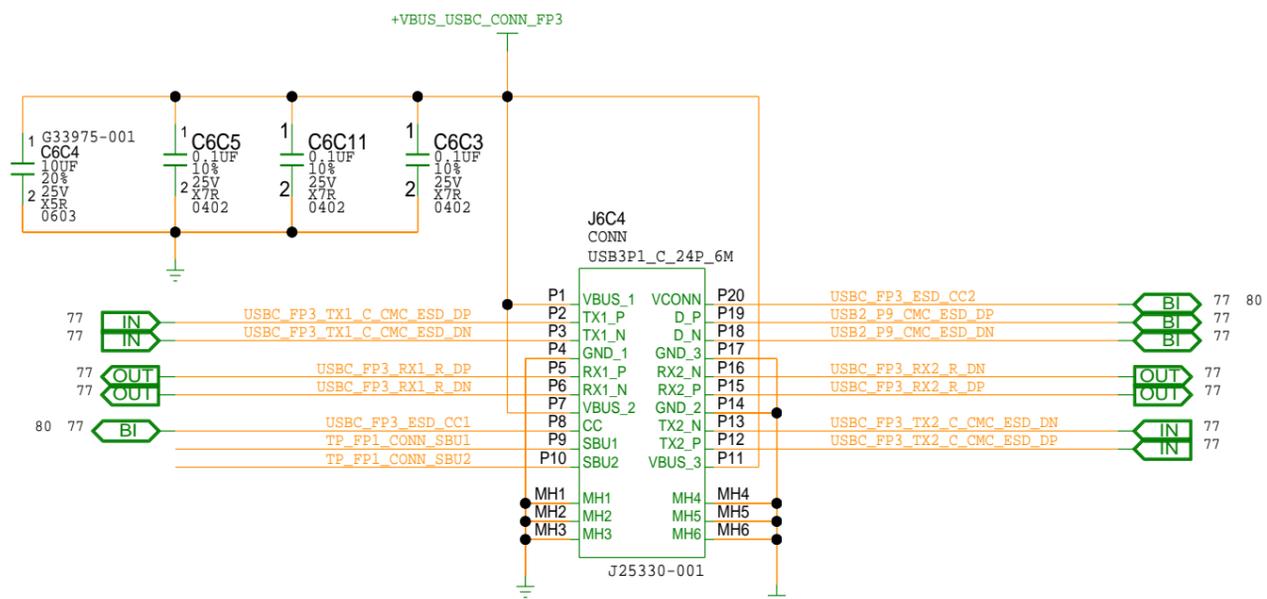


USB2 PORT9 CMC+ESD

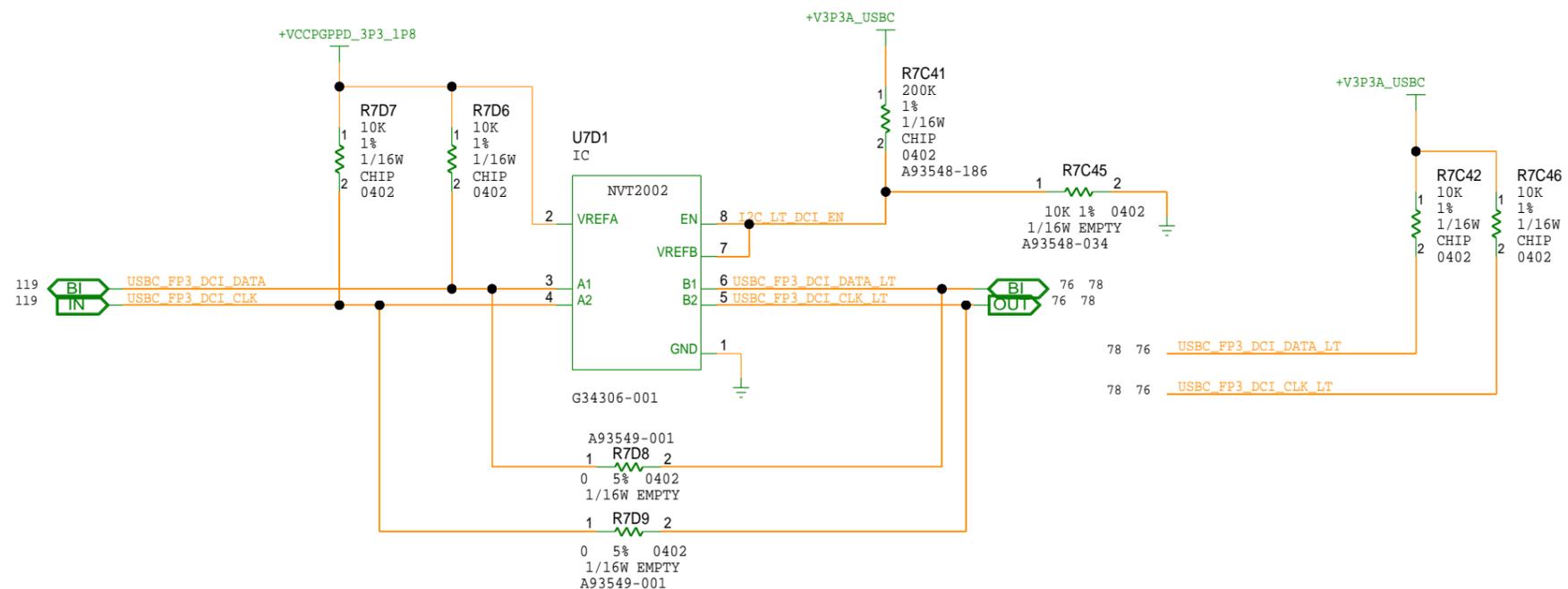


MODULE REV DETAILS		
MODULE NAME	REV	DATE

FRONT PANEL HEADER FOR TYPE-C

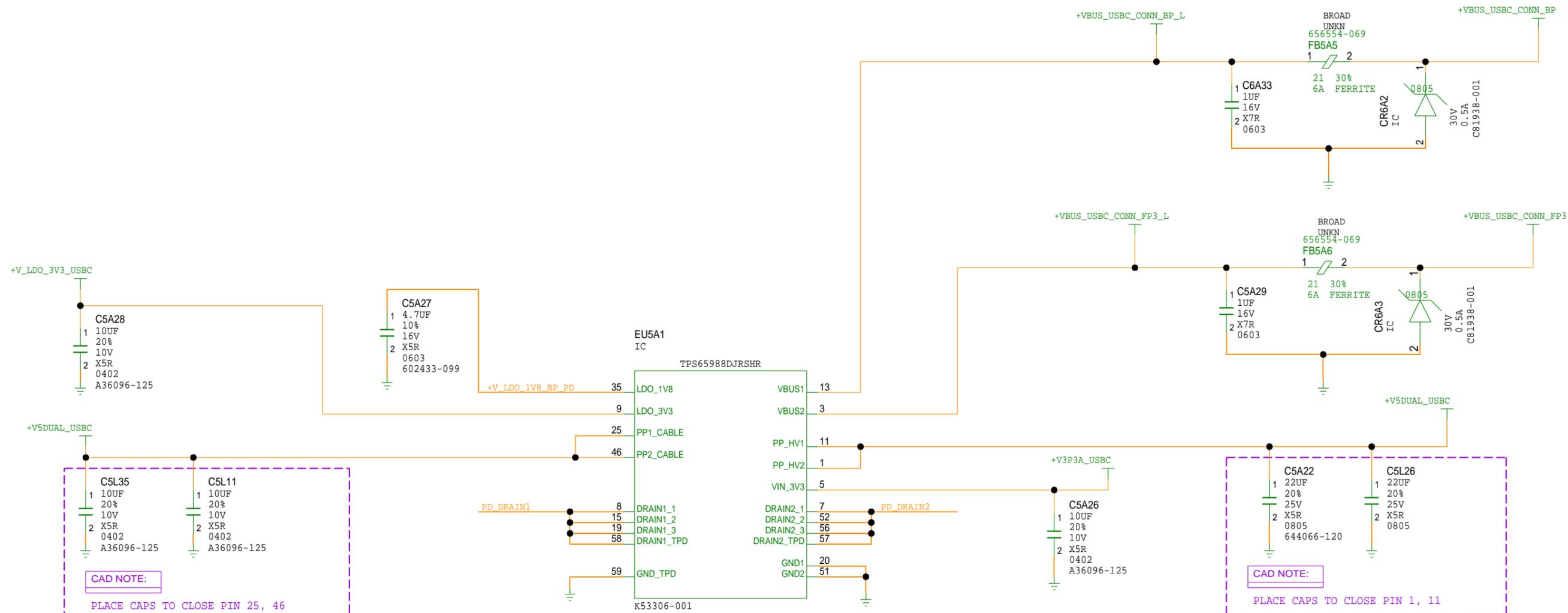


LEVEL SHIFTER FOR DCI OF FP TYPE-C PORT



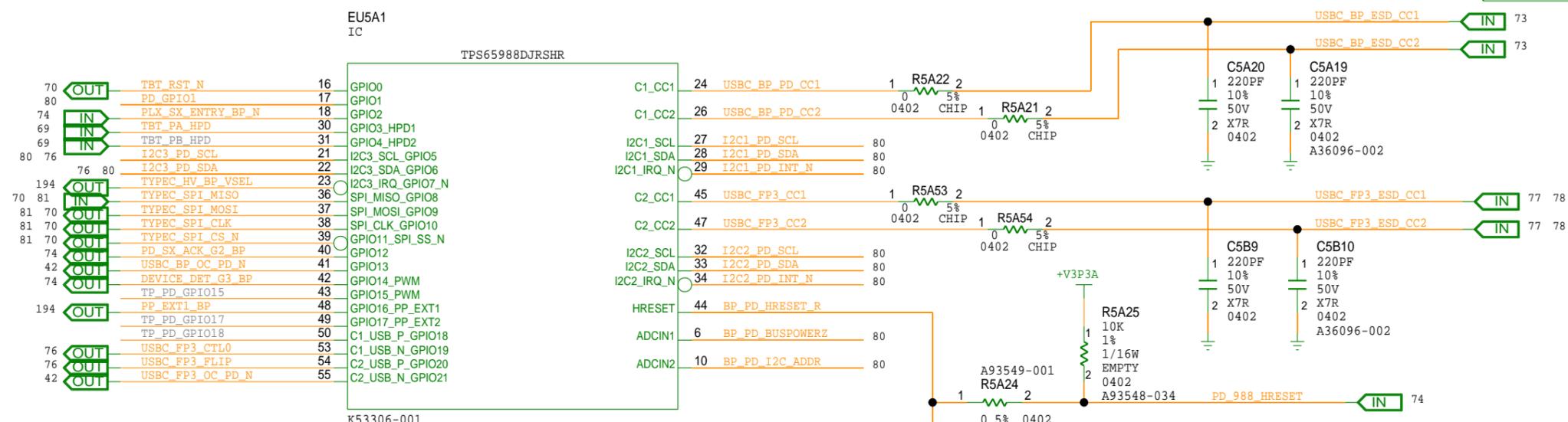
MODULE REV DETAILS

MODULE NAME	REV	DATE



MODULE REV DETAILS

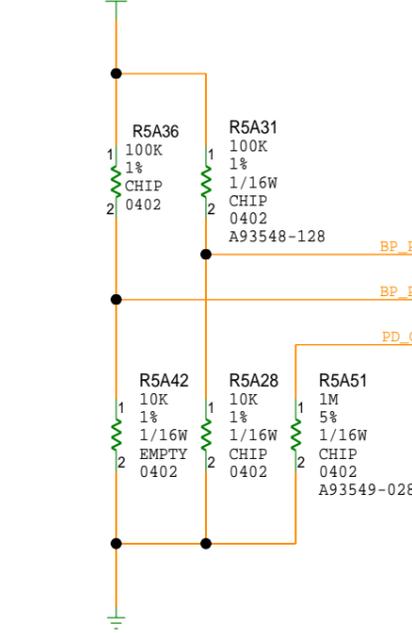
MODULE NAME	REV	DATE



K53306-001

Pin	Signal	IC Pin	IC Pin Name
70	OUT	16	GPIO0
80	OUT	17	GPIO1
74	IN	18	GPIO2
69	IN	30	GPIO3_HPD1
80	IN	31	GPIO4_HPD2
76	IN	21	I2C3_SCL_GPIO5
76	IN	22	I2C3_SDA_GPIO6
194	OUT	23	I2C3_IRQ_GPIO7_N
81	OUT	36	SPI_MISO_GPIO8
81	OUT	37	SPI_MOSI_GPIO9
81	OUT	38	SPI_CLK_GPIO10
81	OUT	39	GPIO11_SPI_SS_N
74	OUT	40	GPIO12
74	OUT	41	GPIO13
74	OUT	42	GPIO14_PWM
194	OUT	43	GPIO15_PWM
76	OUT	48	GPIO16_PP_EXT1
76	OUT	49	GPIO17_PP_EXT2
76	OUT	50	C1_USB_P_GPIO18
76	OUT	53	C1_USB_N_GPIO19
76	OUT	54	C2_USB_P_GPIO20
42	OUT	55	C2_USB_N_GPIO21

+V_LDO_3V3_USBC



DESIGN NOTE:

TI 988 ADCIN1:BUSPOWERZ
 DIV = R2/(R1+R2)
 0.0-0.18 = BUSPWR_NORESPONSE FOR ATX PWR SUPPLY ONLY

DESIGN NOTE:

TI 988 ADCIN2:I2C1 ADDRESS
 DIV = R2/(R1+R2)
 GND > PORT1:0X20 ; PORT2:0X24(7BIT)
 0.2-0.38 > PORT1:0X21 ; PORT2:0X25(7BIT)
 0.4-0.58 > PORT1:0X22 ; PORT2:0X26(7BIT)
 LDO_3V3 > PORT1:0X23 ; PORT2:0X27(7BIT)

DESIGN NOTE:

TI 988 I2C2 SLAVE ADDRESS
 PORT1 : 0X38 (7BIT) / 0X70,0X71(8BIT)
 PORT2 : 0X3F (7BIT)/ 0X7E,0X7F(8BIT)

DESIGN NOTE:

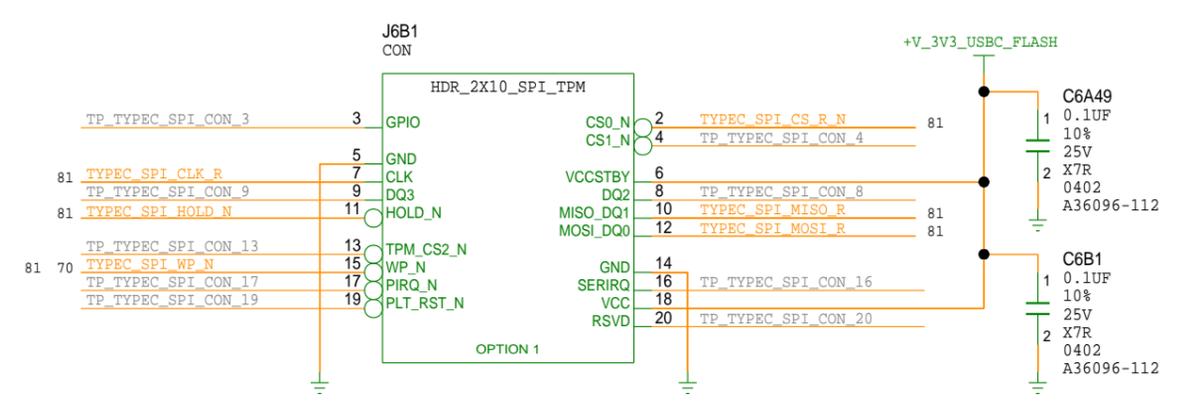
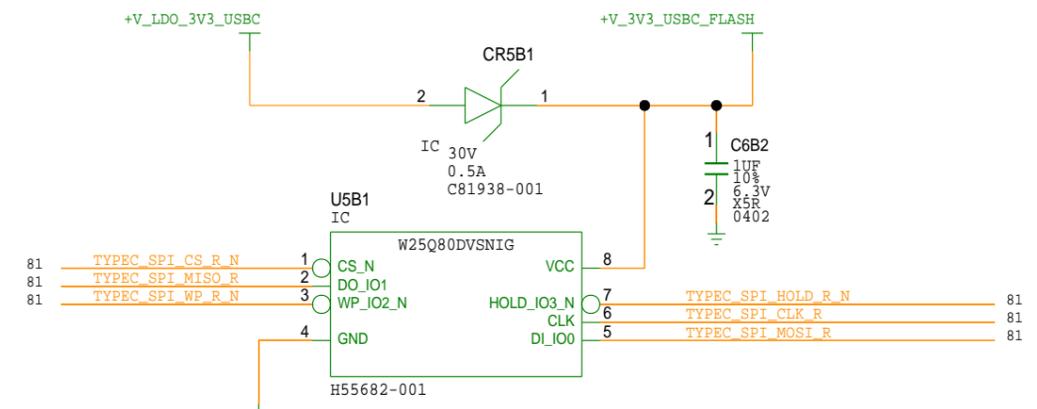
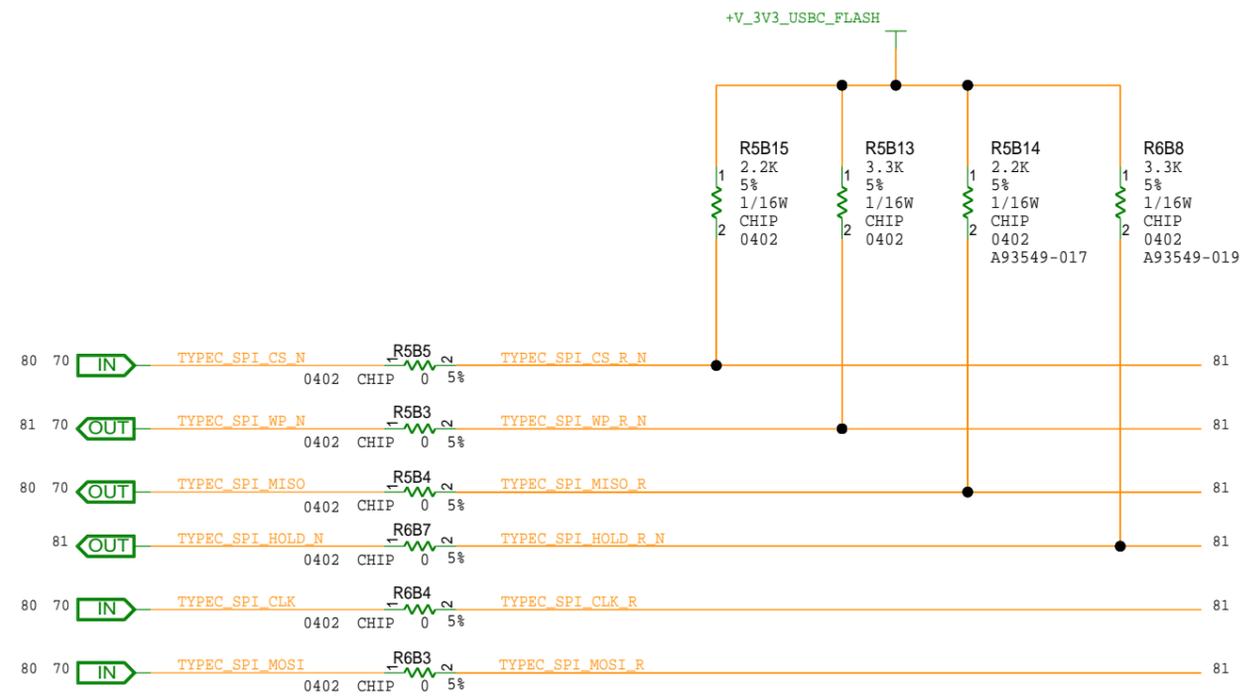
TI 988 ADCIN2:I2C1 ADDRESS
 DIV = R2/(R1+R2)
 GND > PORT1:0X20 ; PORT2:0X24(7BIT)
 0.2-0.38 > PORT1:0X21 ; PORT2:0X25(7BIT)
 0.4-0.58 > PORT1:0X22 ; PORT2:0X26(7BIT)
 LDO_3V3 > PORT1:0X23 ; PORT2:0X27(7BIT)

DESIGN NOTE:

TI 988 I2C3 IS A I2C MASTER (GPIO5/6)

MODULE REV DETAILS

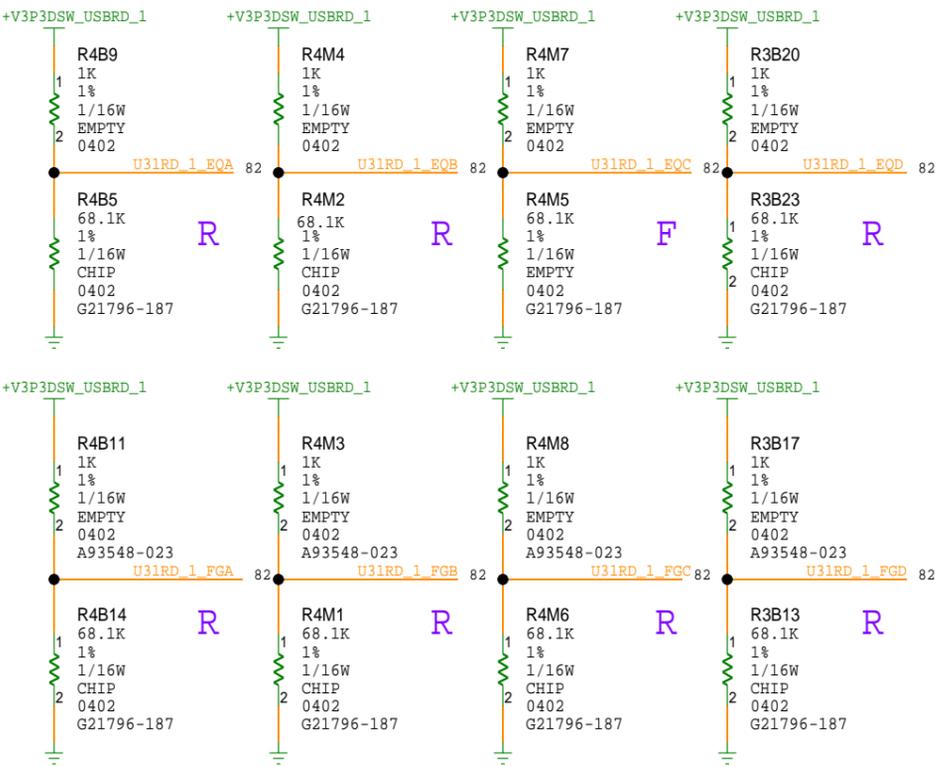
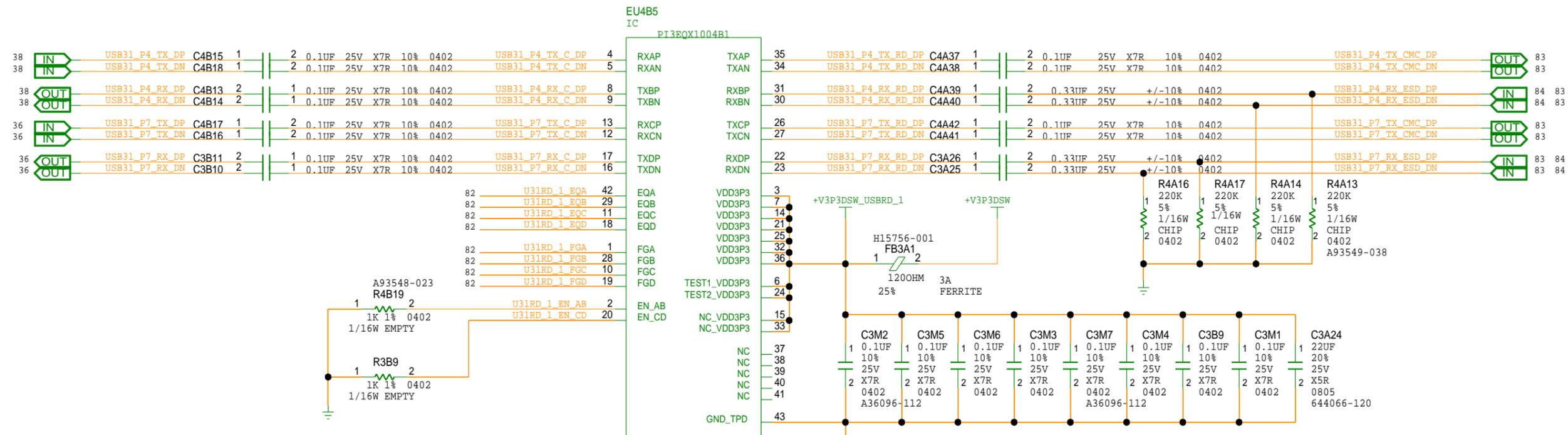
MODULE NAME	REV	DATE



MODULE REV DETAILS

MODULE NAME	REV	DATE

USB3.1 TYPE-A BACK PANEL - REDRIVER
PORT4/7



DESIGN NOTE:
EQ SETTING (DB) @2.5 / 5GHZ
0(0 OHM TO GND) = 6.7 / 12.4
R(68K TO GND) = 3.5 / 8
F(LEAVE OPEN) = 5.3 / 10.6
1(0 OHM TO VDD) = 8.4 / 14.6
EQA/B/C/D = F/F/F/F

DESIGN NOTE:
FG SETTING (DB)
0(0 OHM TO GND) = -1.6
R(68K TO GND) = -0.5
F(LEAVE OPEN) = 1
1(0 OHM TO VDD) = 2.7
FGA/B/C/D = 1/1/1/1

BPAGE DRAWING

udimm.sch_1.82
Fri Sep 27 16:40:27 2019

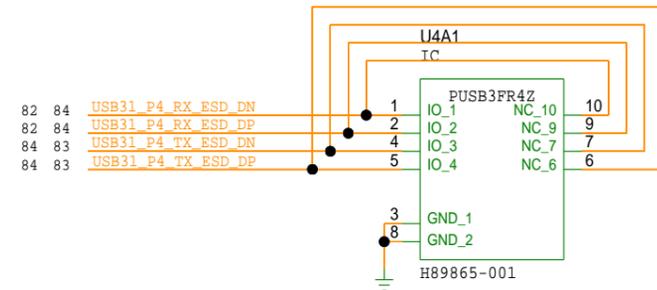
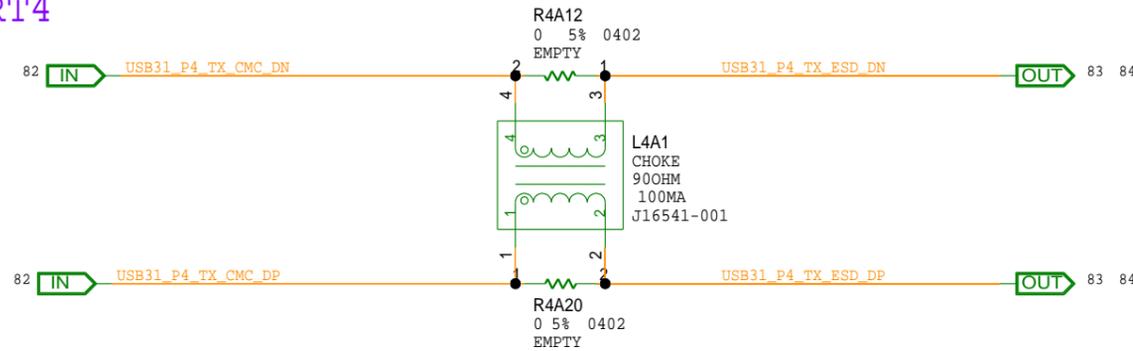
INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 82	REV 0.7
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MODULE REV DETAILS

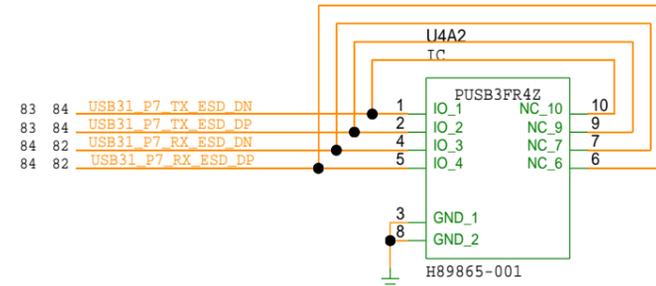
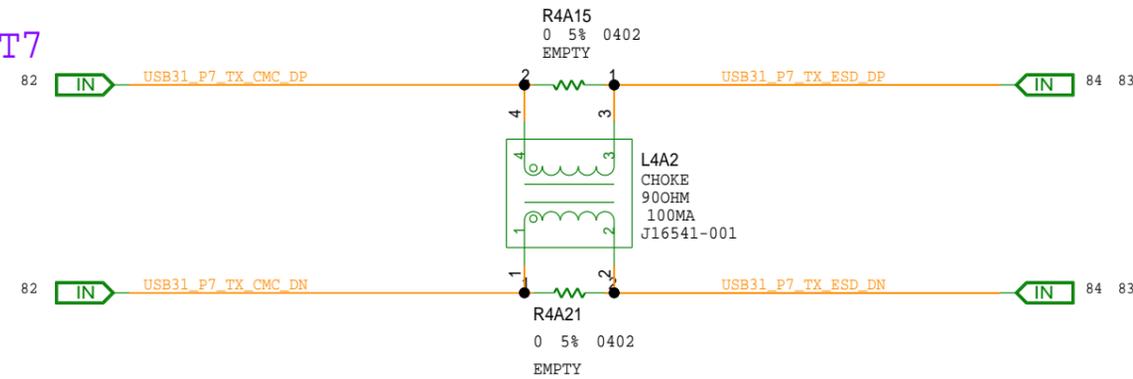
MODULE NAME	REV	DATE

USB3.1 TYPE-A BACK PANEL - CMC+ESD

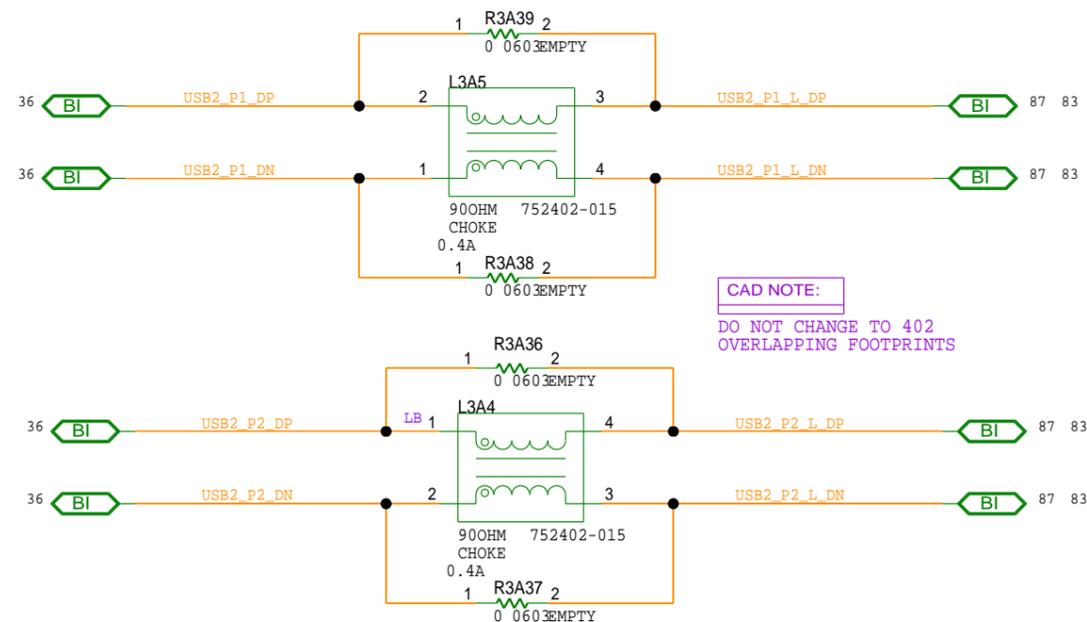
USB3.1 PORT4



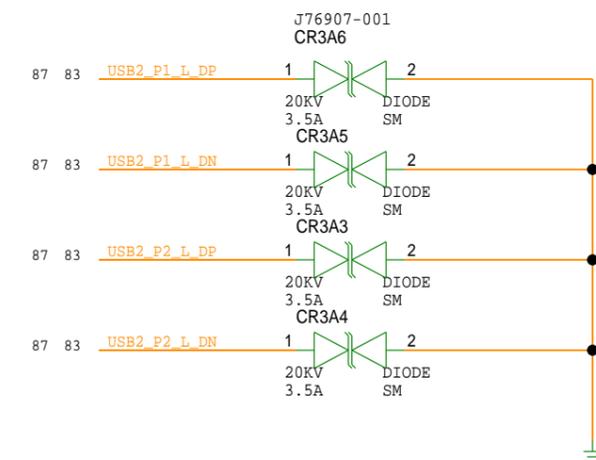
USB3.1 PORT7



USB2.0 PORT1/2 CMC+ESD



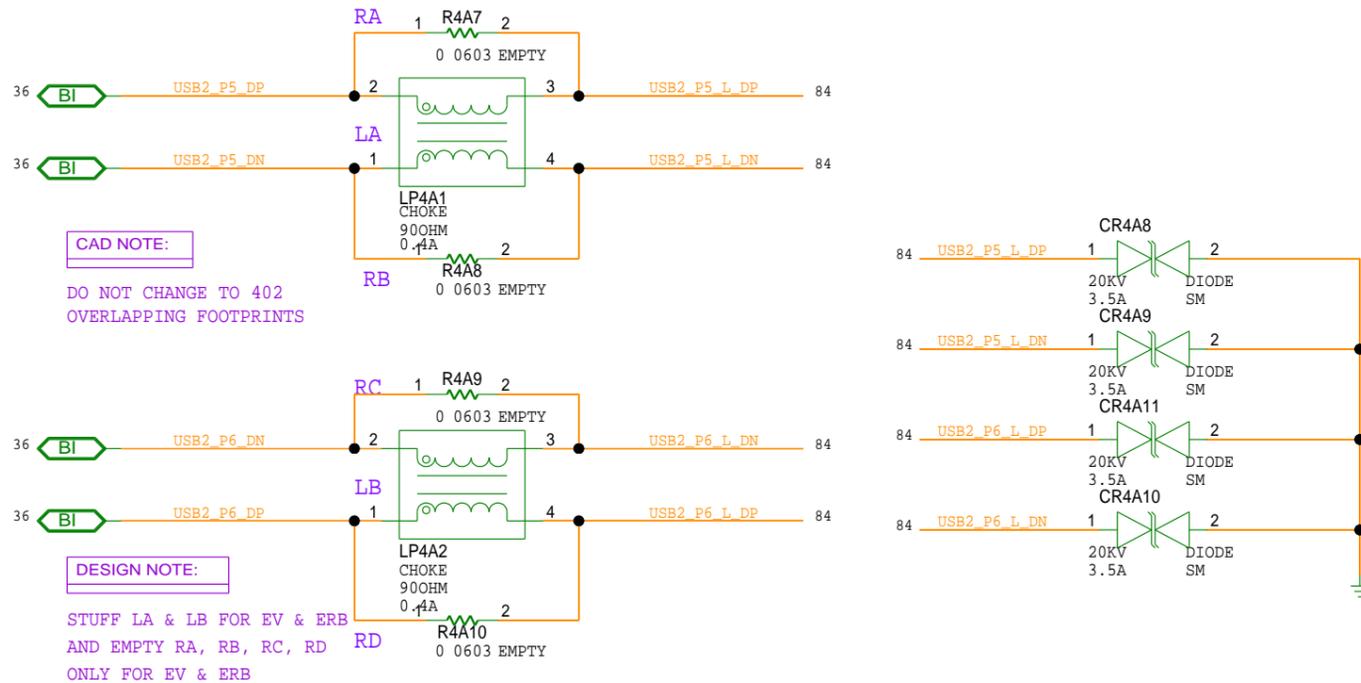
CAD NOTE:
DO NOT CHANGE TO 402
OVERLAPPING FOOTPRINTS



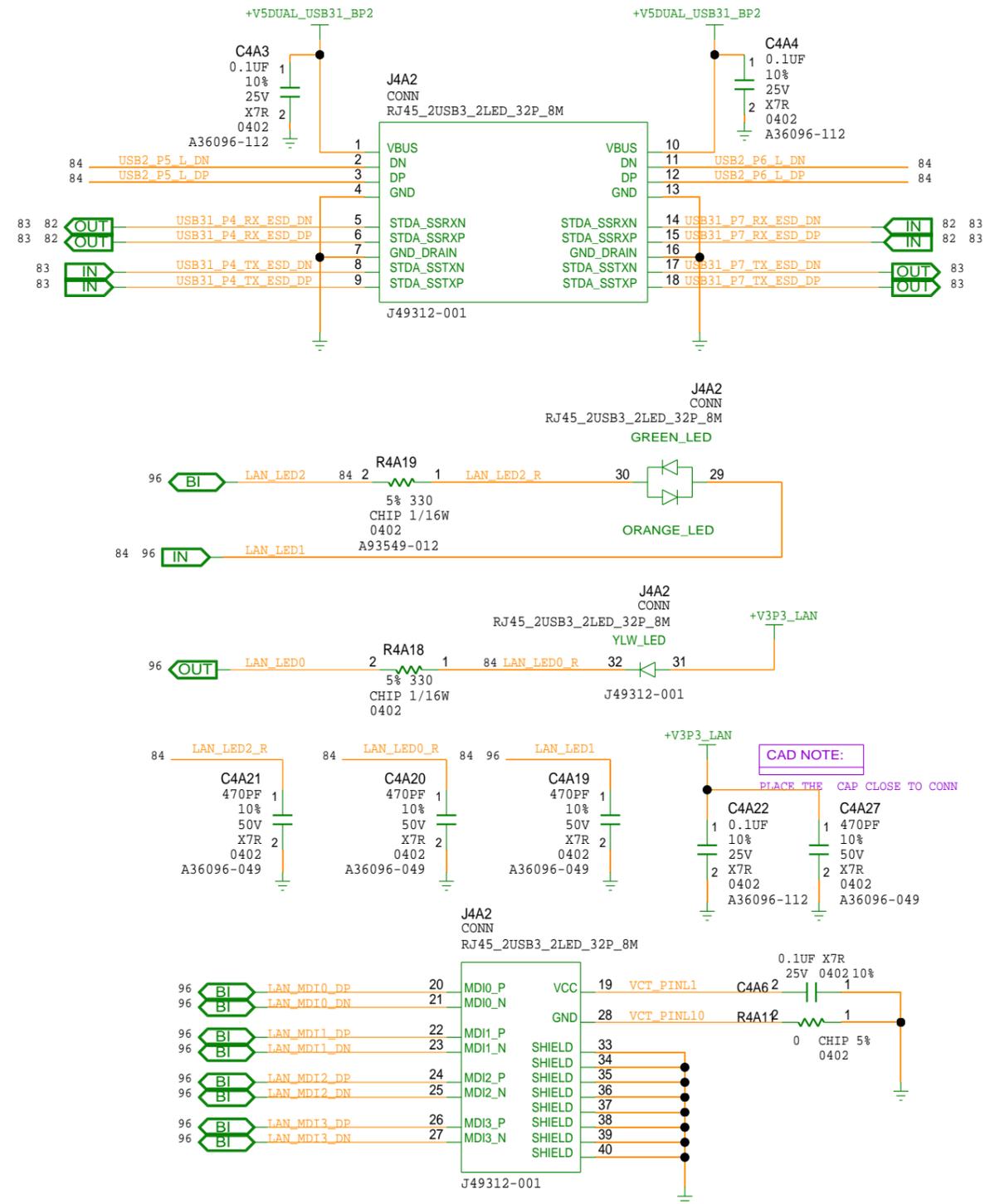
MODULE REV DETAILS

MODULE NAME	REV	DATE

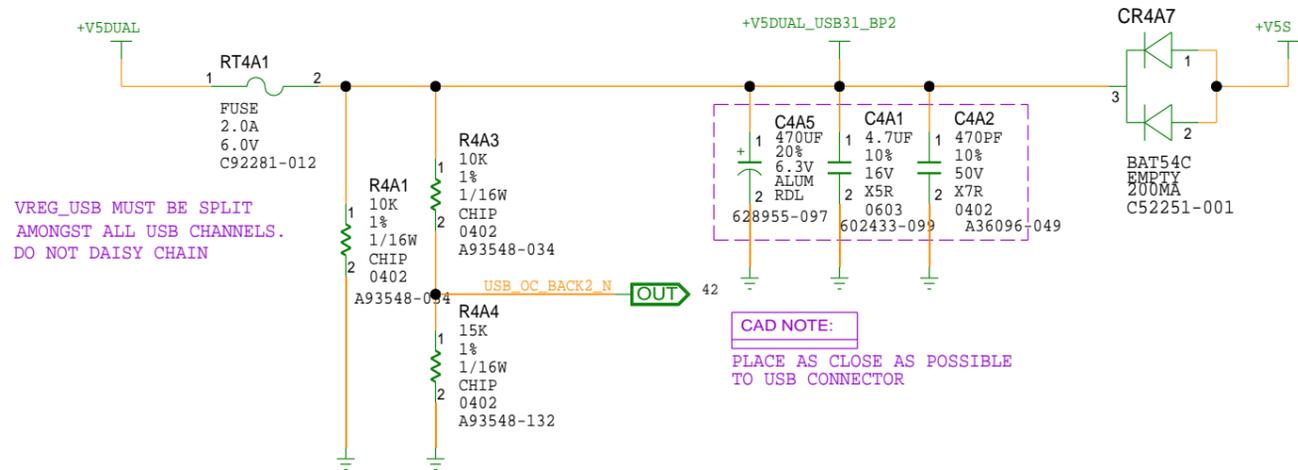
USB2.0 CMC+ESD



RJ45 & DUAL USB3.1 TYPEA STACK CONNECTOR



USB3.1 POWER FOR RJ45/USB STACK CONECTOR



[PAGE_TITLE=USB3.1 TYPE-A BACK PANEL 1&2 - CONN]

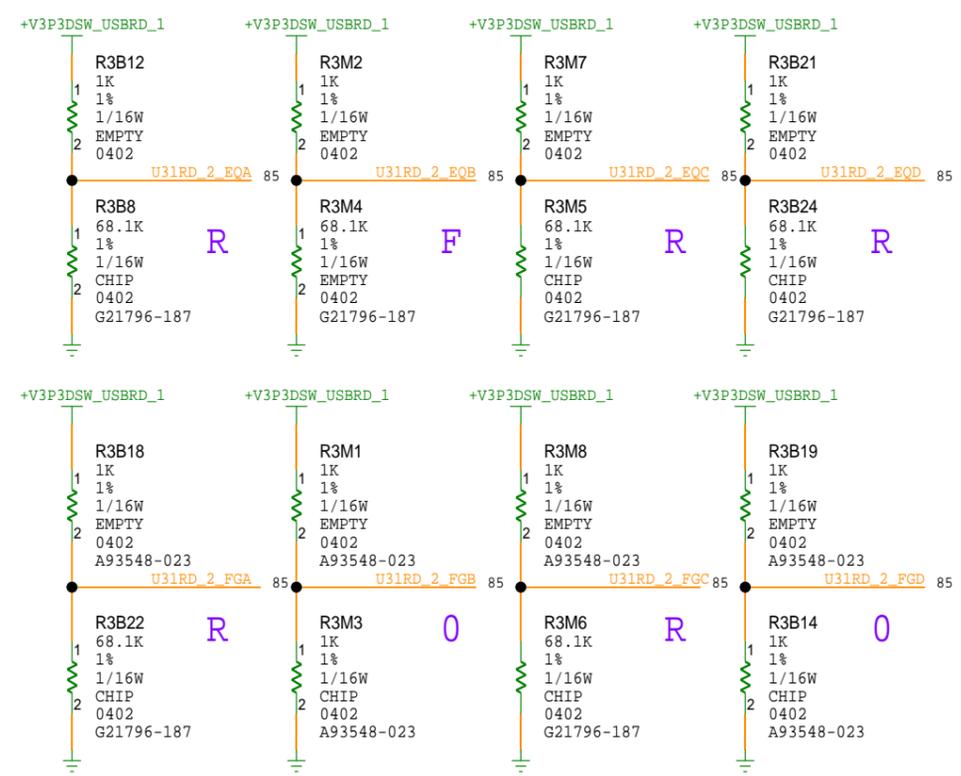
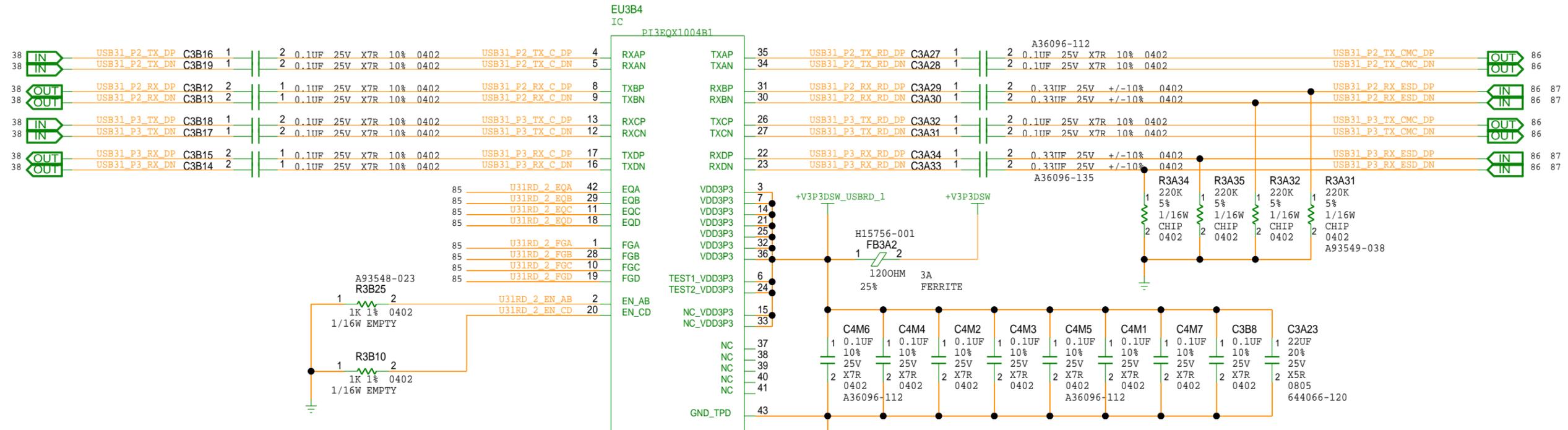
BPAGE DRAWING

udimm.sch_1.84
Fri Sep 27 16:40:29 2019

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USB3.1 TYPE-A BACK PANEL - REDRIVER PORT2/3

MODULE REV DETAILS		
MODULE NAME	REV	DATE



DESIGN NOTE:
EQ SETTING (DB) @2.5 / 5GHZ
0(0 OHM TO GND) = 6.7 / 12.4
R(68K TO GND) = 3.5 / 8
F(LEAVE OPEN) = 5.3 / 10.6
1(0 OHM TO VDD) = 8.4 / 14.6
EQA/B/C/D = F/F/F/F

DESIGN NOTE:
FG SETTING (DB)
0(0 OHM TO GND) = -1.6
R(68K TO GND) = -0.5
F(LEAVE OPEN) = 1
1(0 OHM TO VDD) = 2.7
FGA/B/C/D = 1/1/1/1

[PAGE_TITLE=USB3.1 TYPE-A BACK PANEL 3&4 - REDDRIVERS]

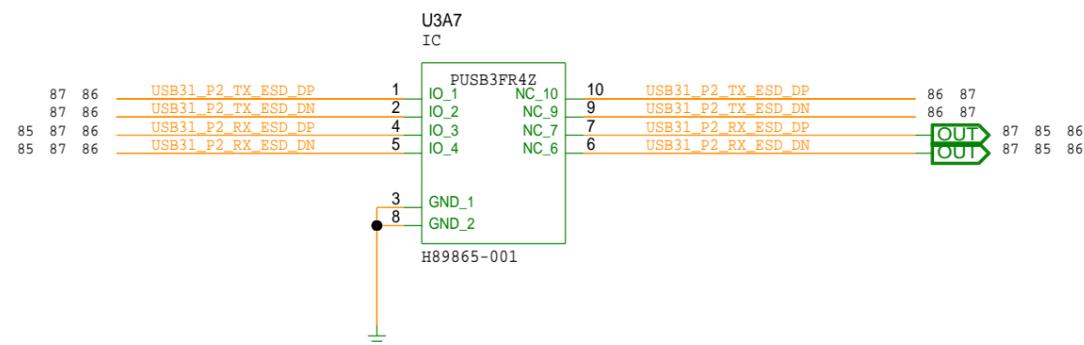
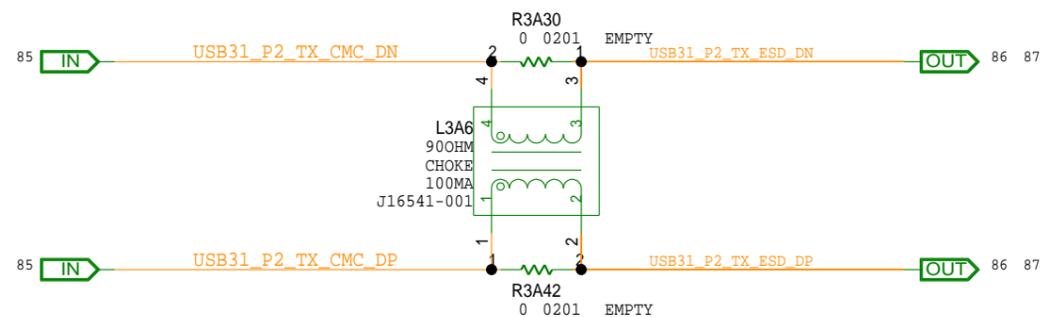
BPAGE DRAWING
udimm.sch_1.85
Fri Sep 27 16:40:30 2019

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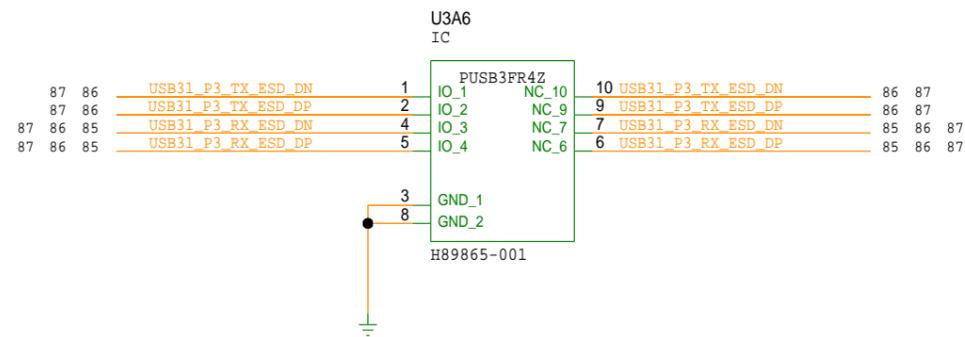
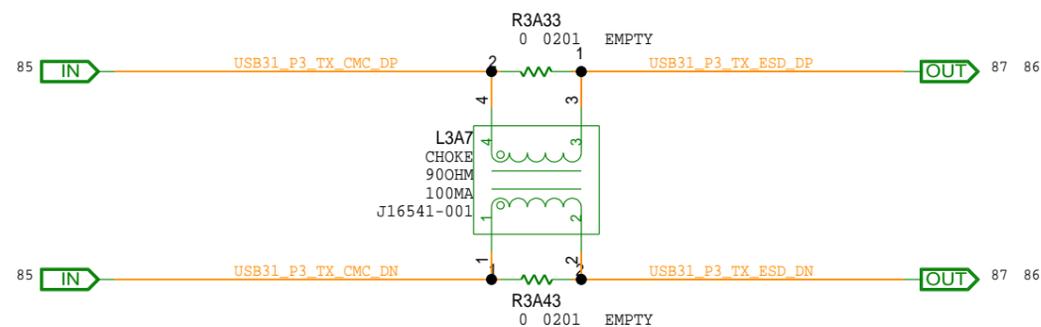
MODULE REV DETAILS

MODULE NAME	REV	DATE

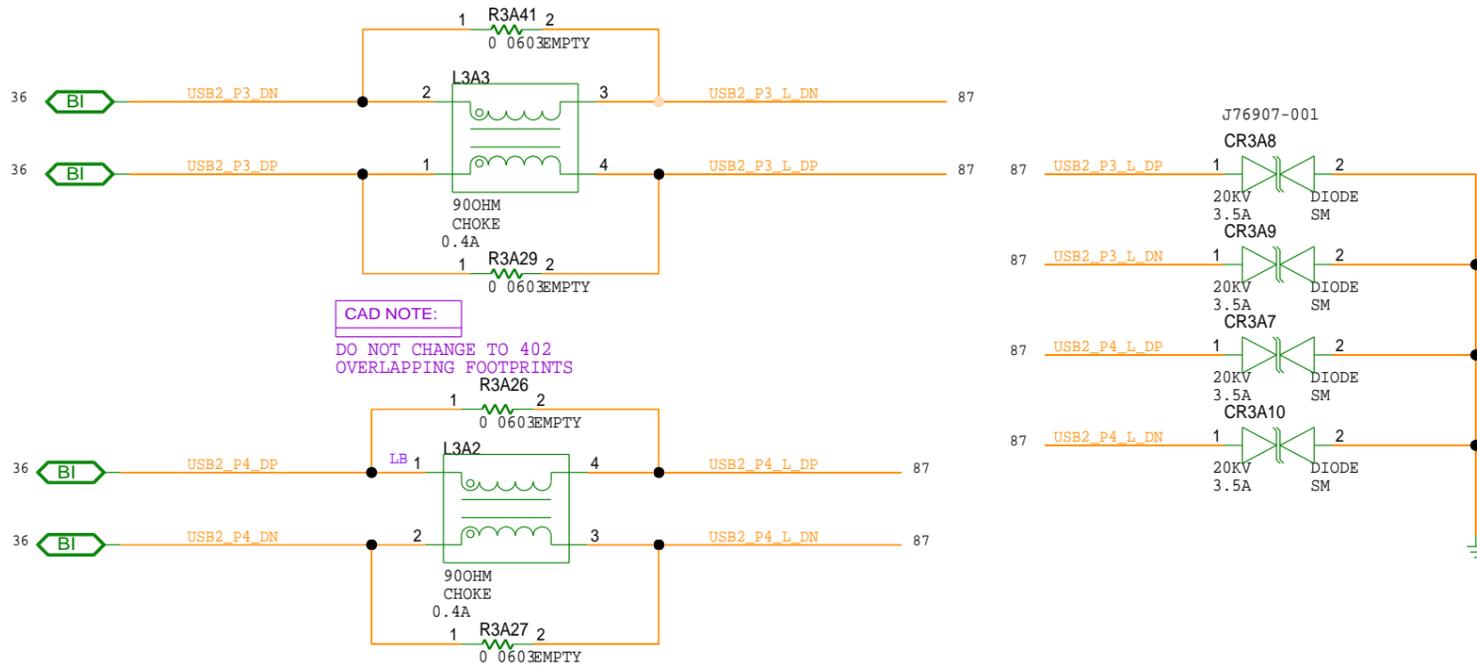
USB3.1 TYPE-A BACK PANEL - CMC+ESD
USB3.1 PORT2



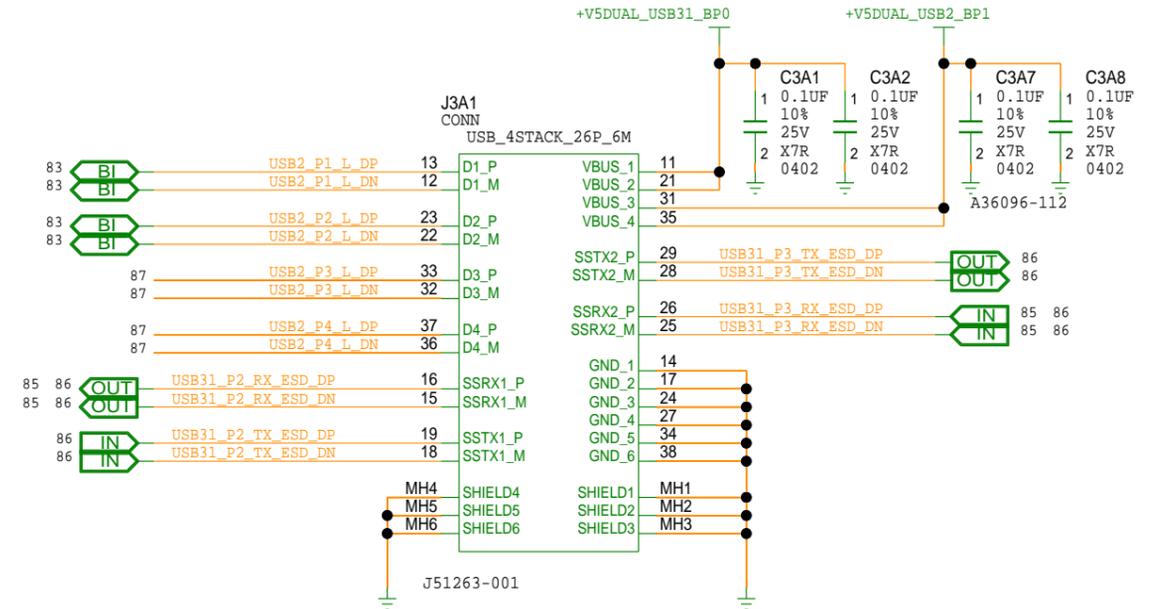
USB3.1 PORT3



USB3.1 TYPE-A BACK PANEL - CONNECTOR
 USB2.0 PORT3/4 CMC+ESD



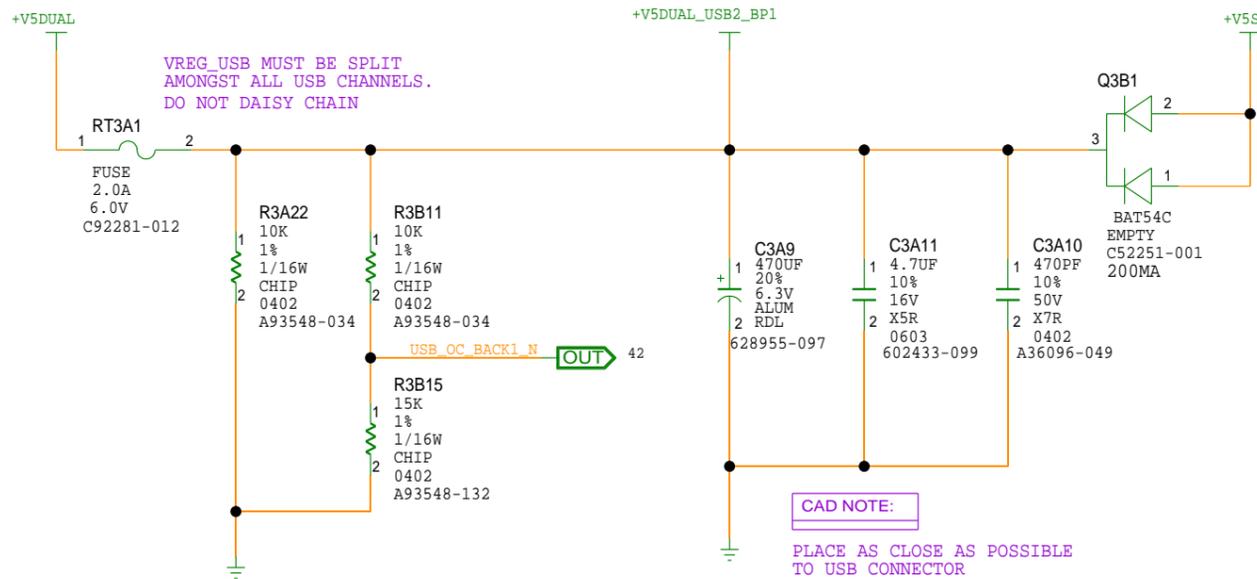
USB31 STACK CONN



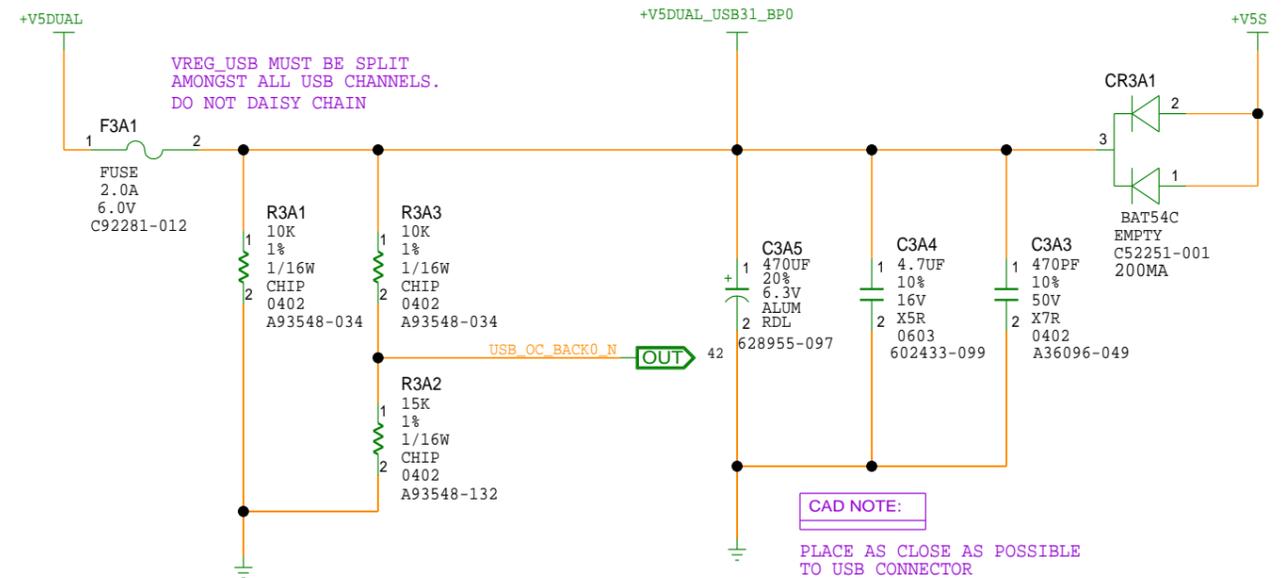
MODULE REV DETAILS

MODULE NAME	REV	DATE

USB POWER



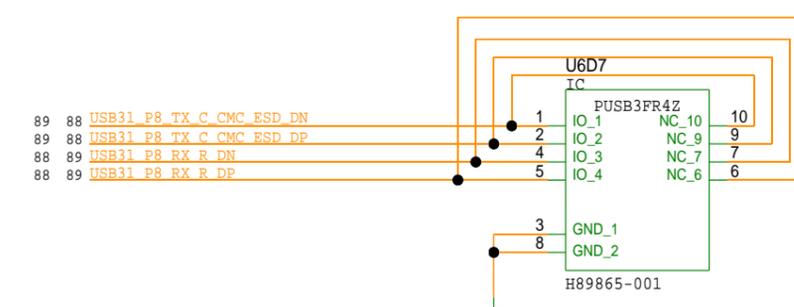
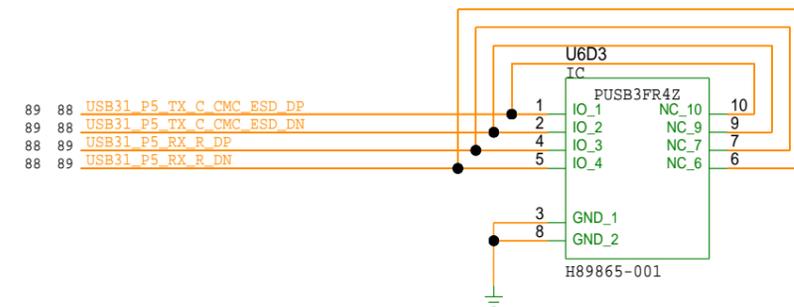
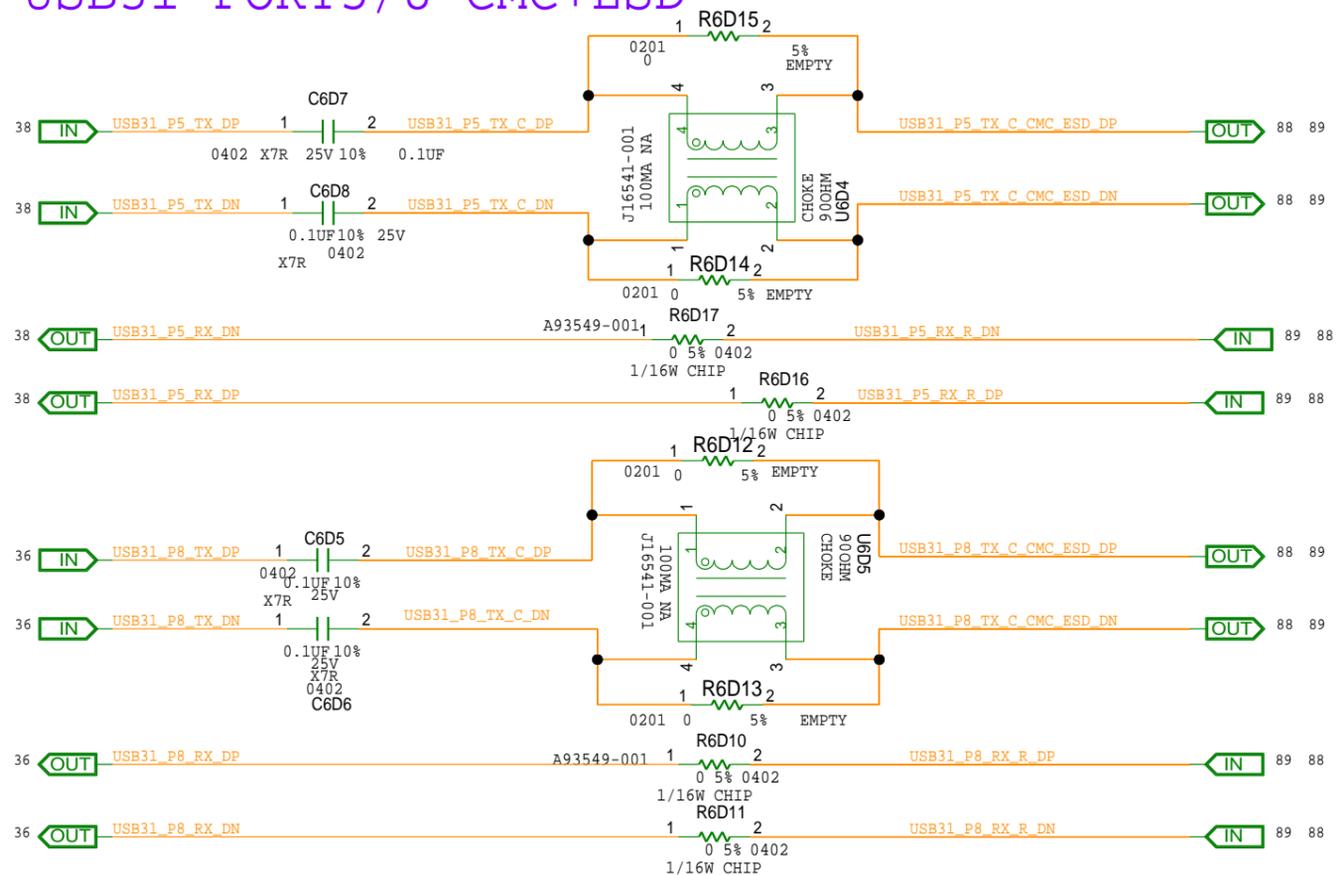
USB POWER



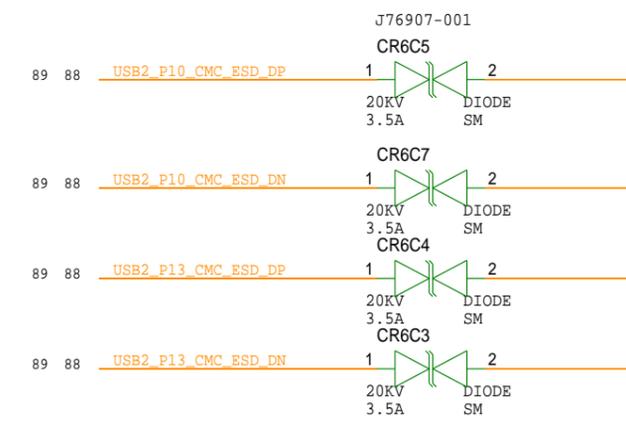
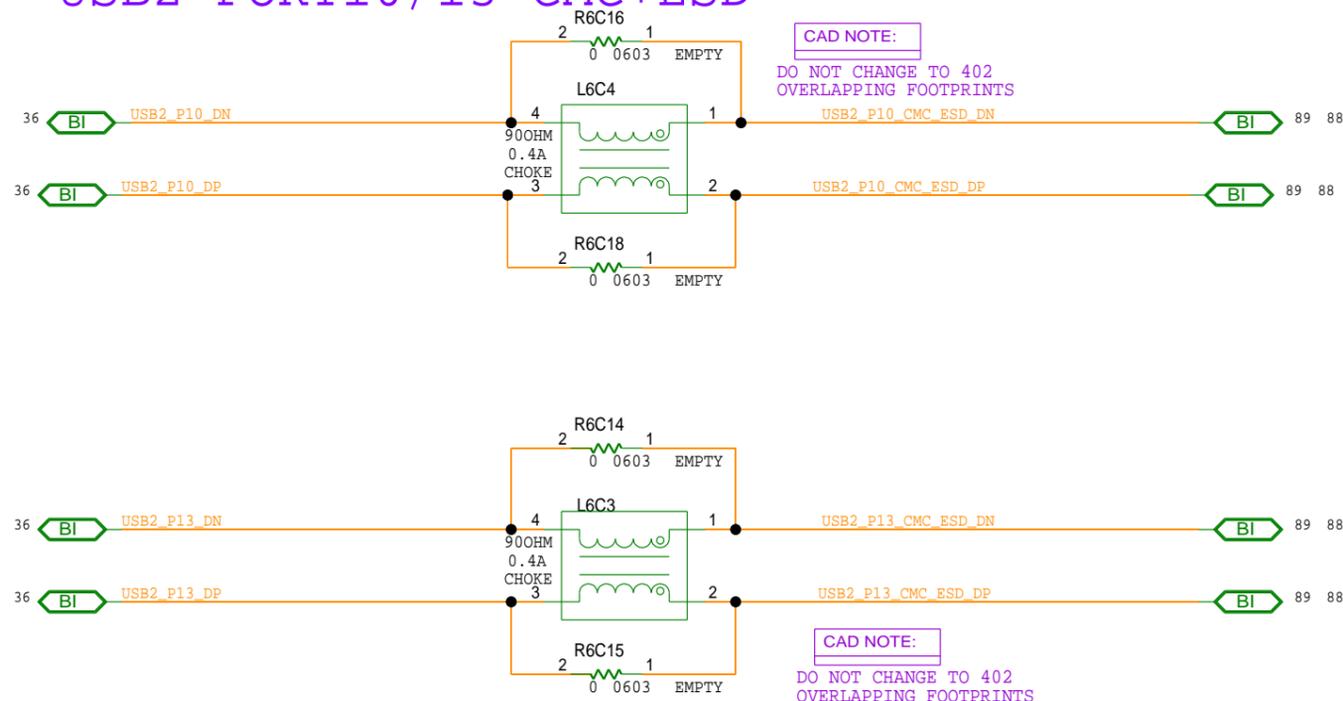
MODULE REV DETAILS

MODULE NAME	REV	DATE

USB31 PORT5/8 CMC+ESD

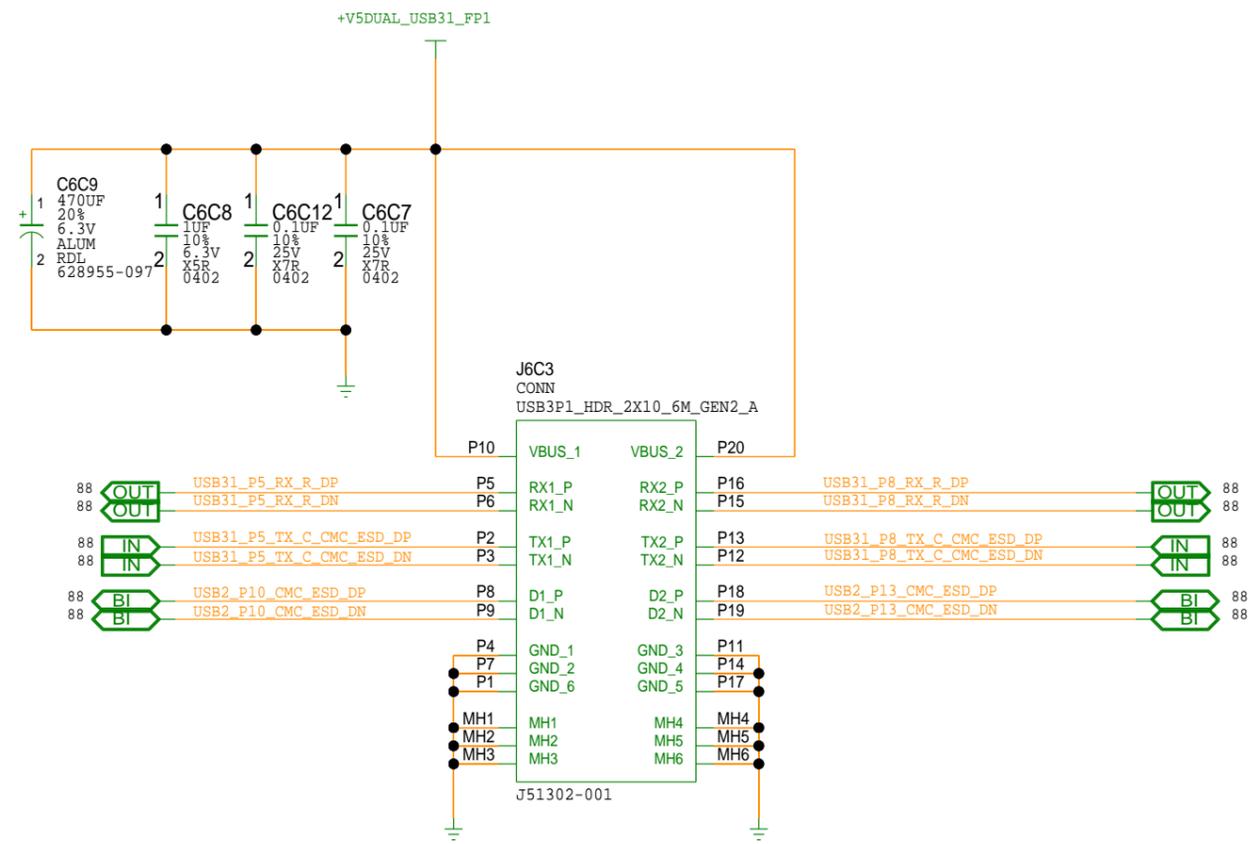


USB2 PORT10/13 CMC+ESD



MODULE REV DETAILS		
MODULE NAME	REV	DATE

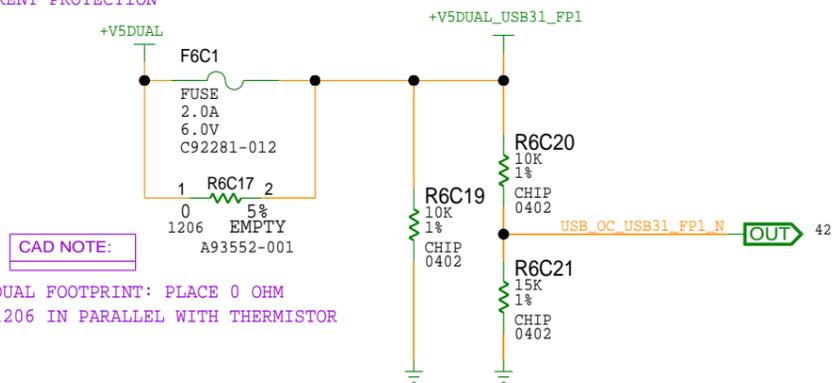
FRONT PANEL HEADER FOR TYPE-A



DESIGN NOTE:

STUFFING THE THERMISTOR ASSUMES FRONT PANEL CARD HAS NO FUSE AND DOES NOT PROVIDE OVER-CURRENT PROTECTION

FRONT PANEL POWER



CAD NOTE:

DUAL FOOTPRINT: PLACE 0 OHM 1206 IN PARALLEL WITH THERMISTOR

MODULE REV DETAILS

MODULE NAME	REV	DATE



[PAGE_TITLE=BLANK]

BPAGE DRAWING

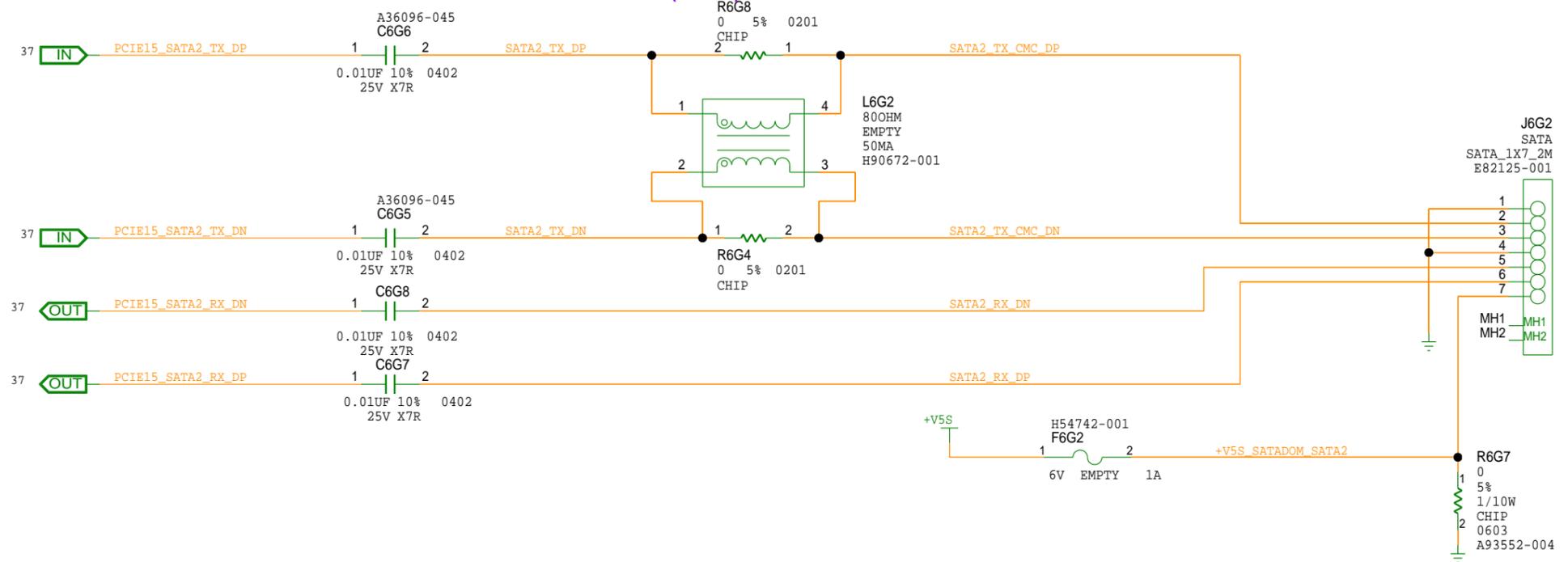
udimm.sch_1.90
Fri Sep 20 10:35:27 2019

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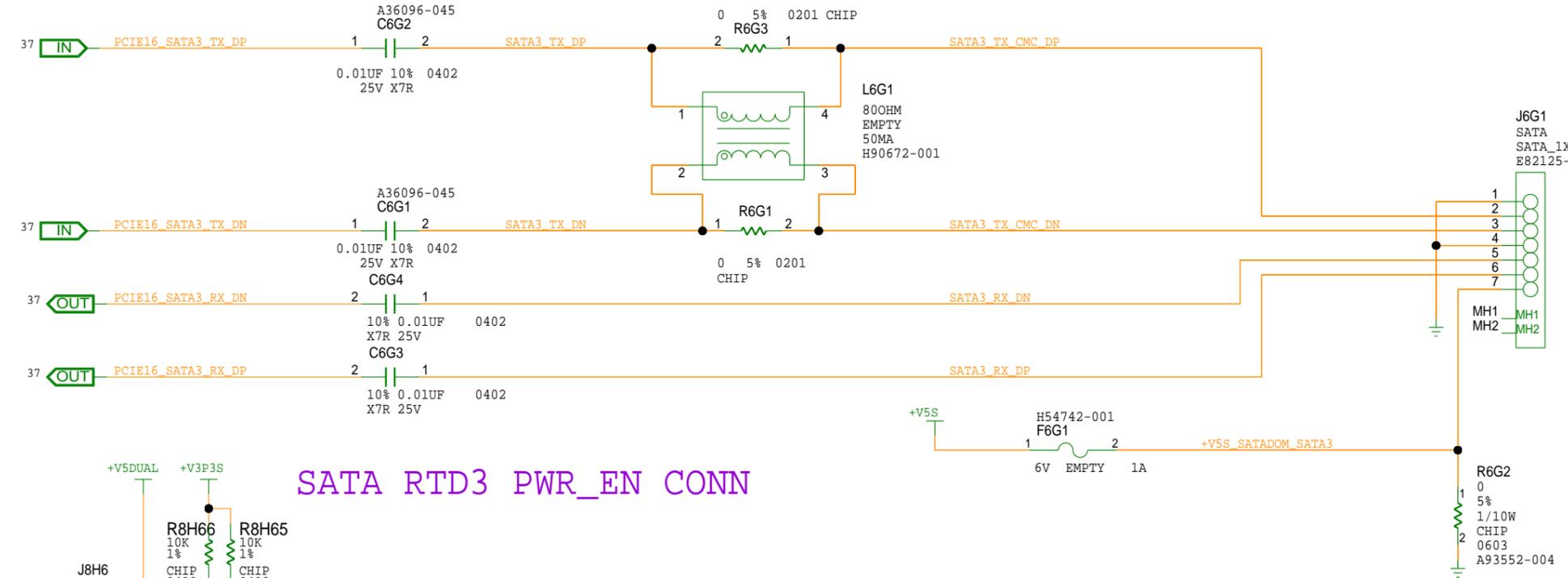
MODULE REV DETAILS

MODULE NAME	REV	DATE

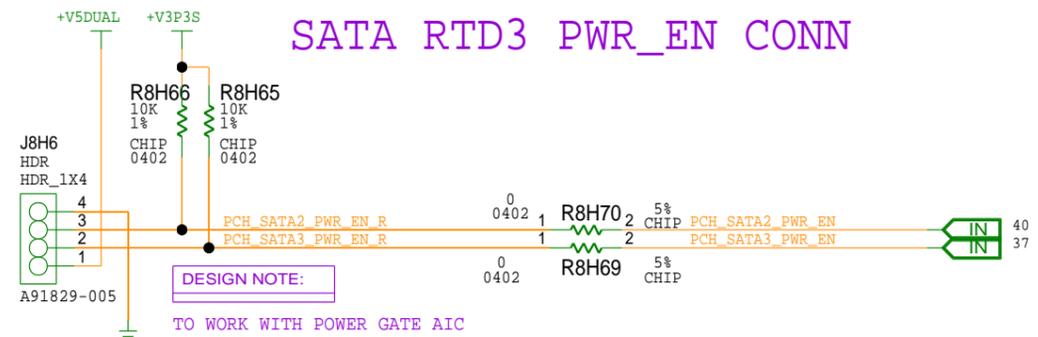
SATA GEN3 CABLE CONNECTOR(P2)



SATA GEN3 CABLE CONNECTOR(P3)



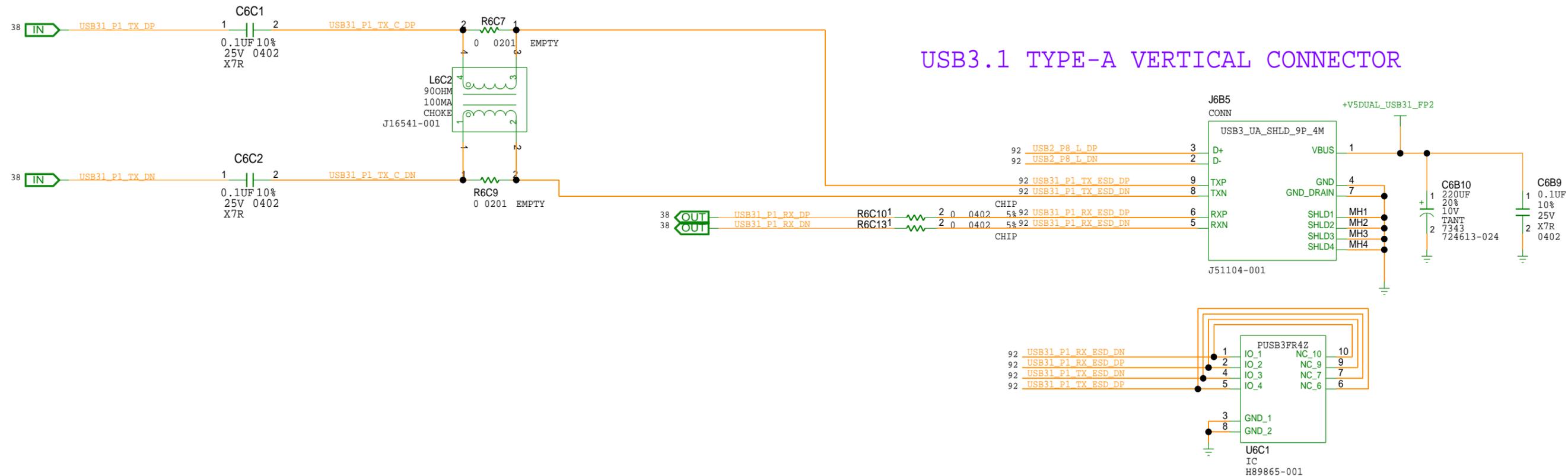
SATA RTD3 PWR_EN CONN



MODULE REV DETAILS		
MODULE NAME	REV	DATE

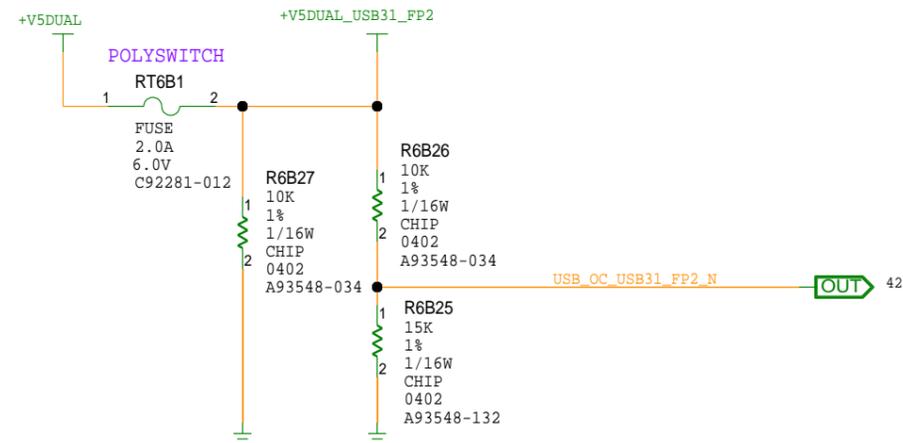
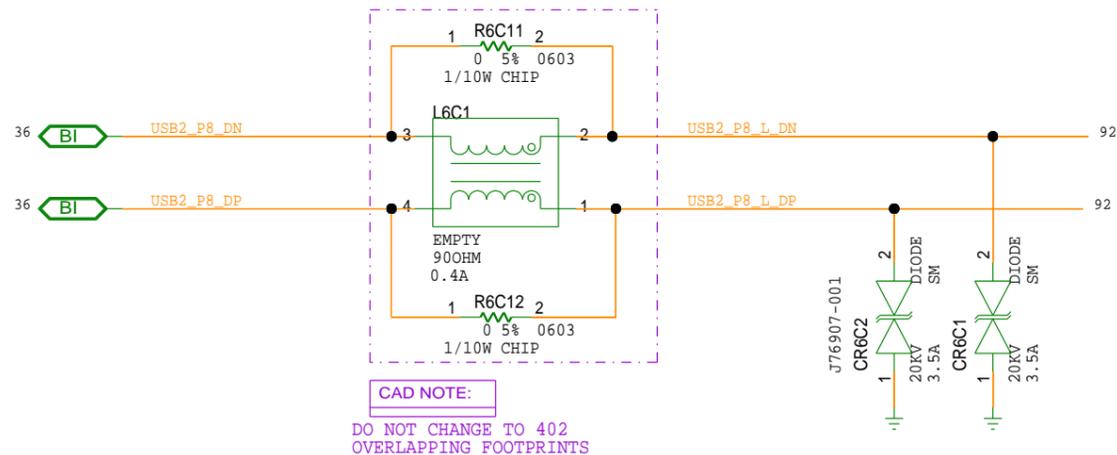
USB3.1 CMC+ESD PORT 1 - VERTICAL TYPE-A

USB3.1 TYPE-A VERTICAL CONNECTOR



USB2.0 CMC+ESD PORT 8 - VERTICAL TYPE-A

USB POWER -VERTICAL TYPE-A



[PAGE_TITLE = USB3.1 TYPE-A VERTICAL]

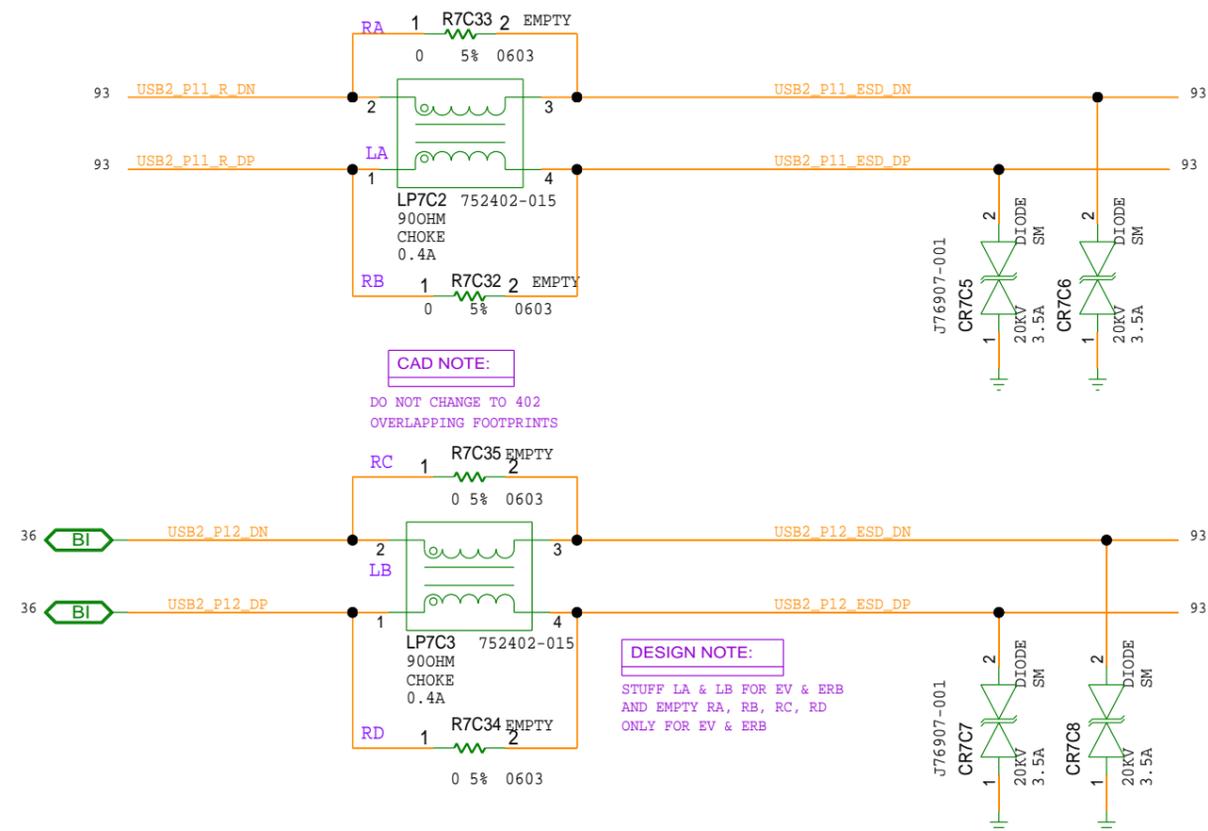
BPAGE DRAWING
udimm.sch_1.92
Fri Sep 27 16:40:36 2019

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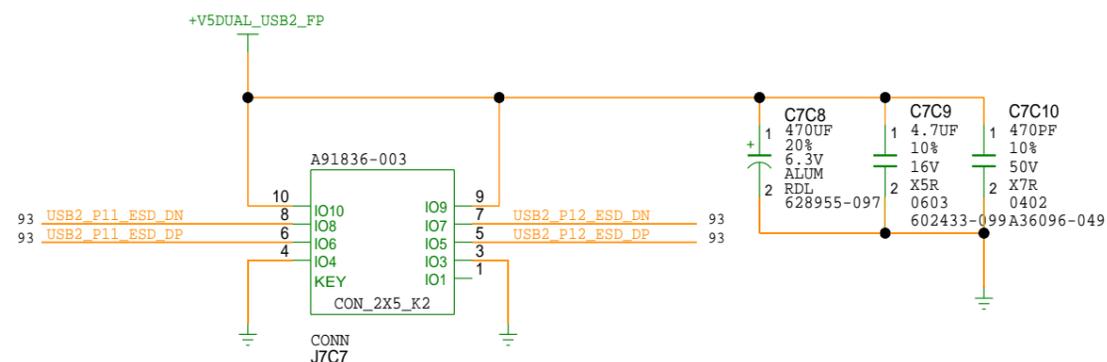
MODULE REV DETAILS

MODULE NAME	REV	DATE

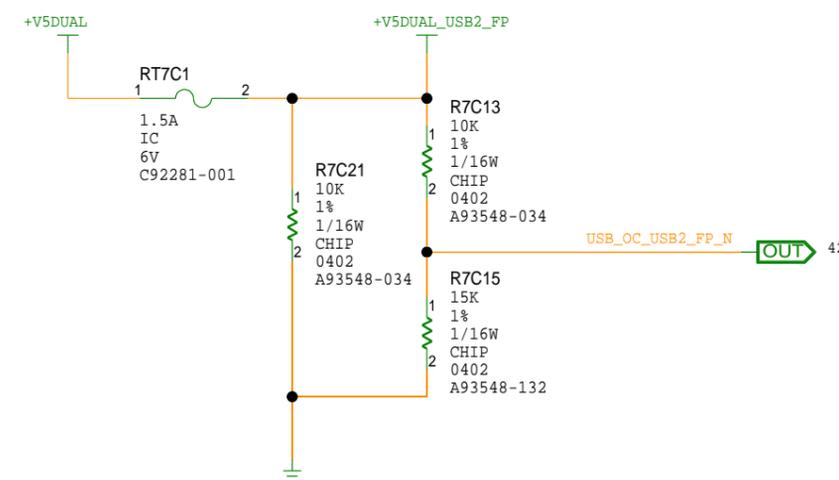
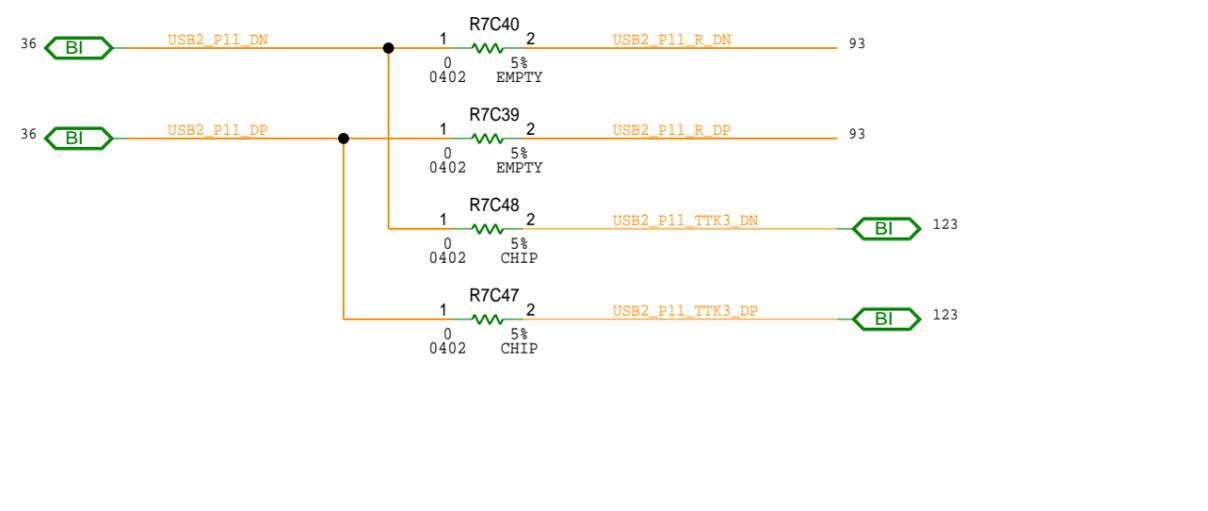
USB2.0 CMC+ESD
PORT 11:12 - FRONT PANEL



USB2.0 FRONT PANEL HEADER



USB2.0 POWER - FRONT PANEL*2 PORT



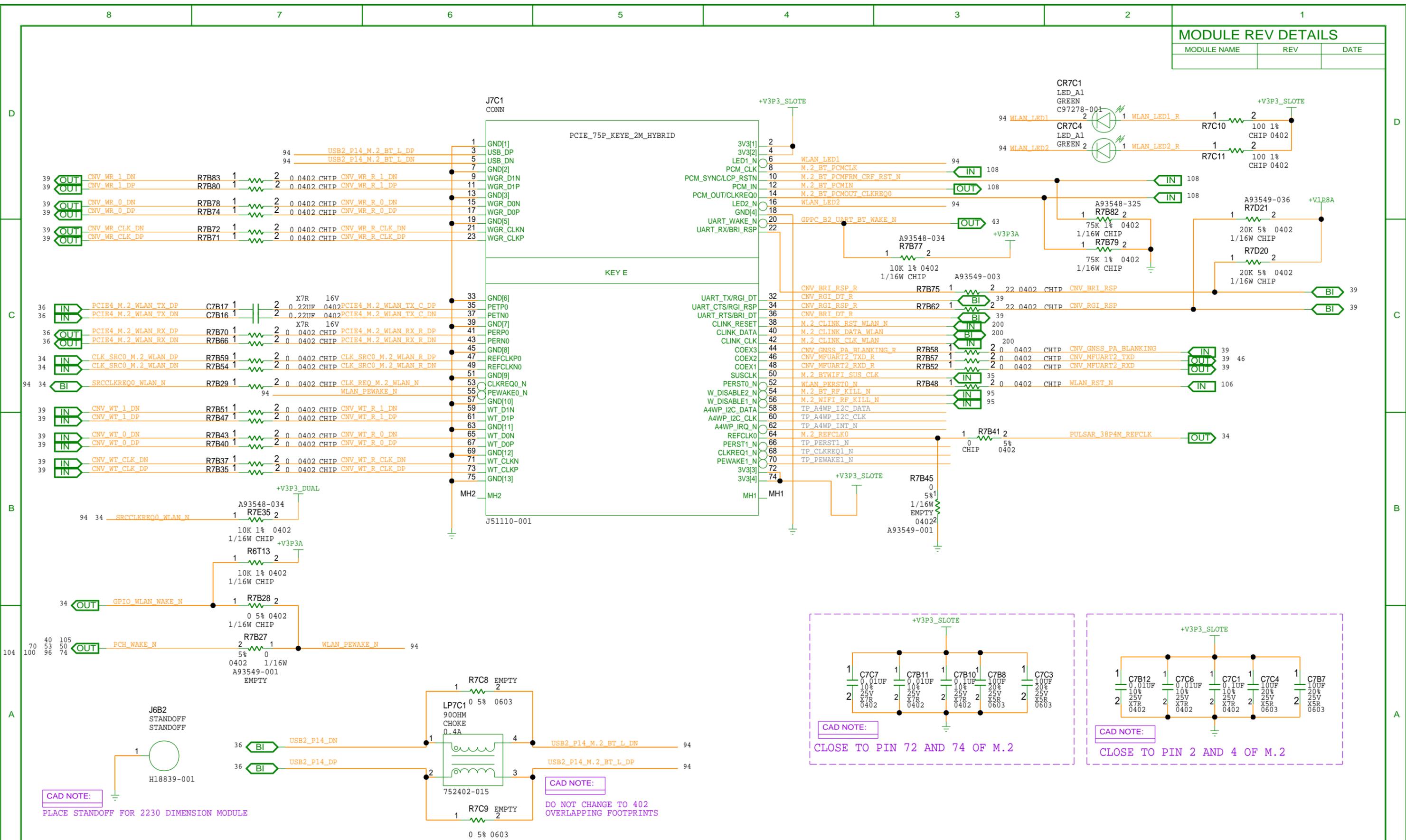
[PAGE_TITLE=USB2.0 FRONT PANEL HEADER]

BPAGE DRAWING
udimm_sch_1.93
Fri Sep 27 16:40:37 2019

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MODULE REV DETAILS

MODULE NAME	REV	DATE



CAD NOTE:
PLACE STANDOFF FOR 2230 DIMENSION MODULE

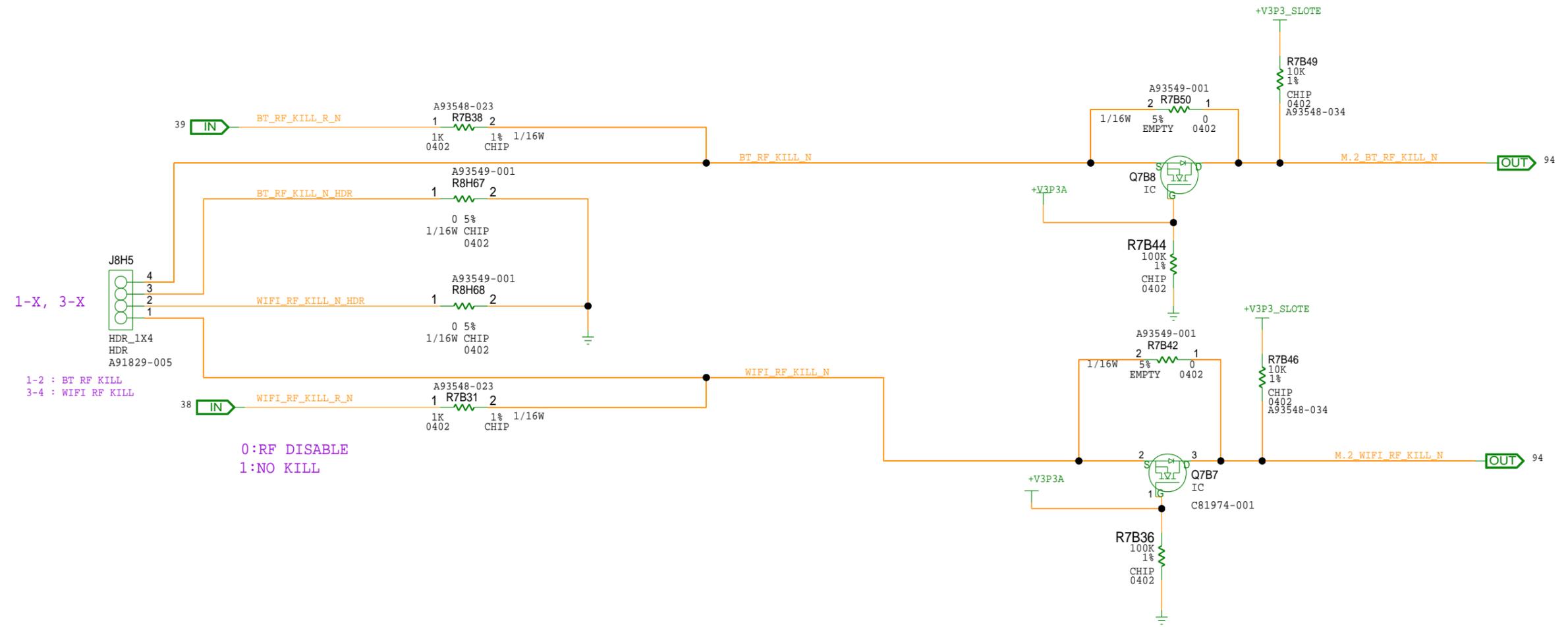
CAD NOTE:
DO NOT CHANGE TO 402
OVERLAPPING FOOTPRINTS

CAD NOTE:
CLOSE TO PIN 72 AND 74 OF M.2

CAD NOTE:
CLOSE TO PIN 2 AND 4 OF M.2

MODULE REV DETAILS

MODULE NAME	REV	DATE



[PAGE_TITLE=CONNECTIVITY - M.2 KEY-E WLAN/BT RF KILL CKT]

BPAGE DRAWING

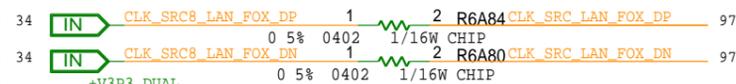
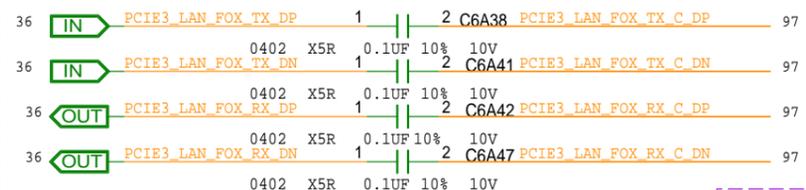
udimm.sch_1.95
Fri Sep 27 16:40:39 2019

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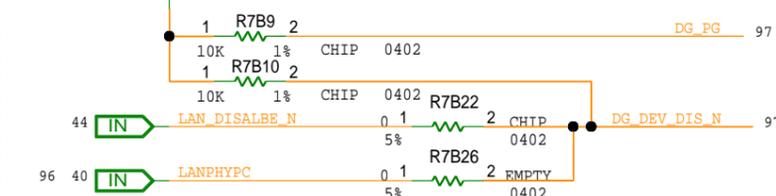
MODULE REV DETAILS

MODULE NAME	REV	DATE

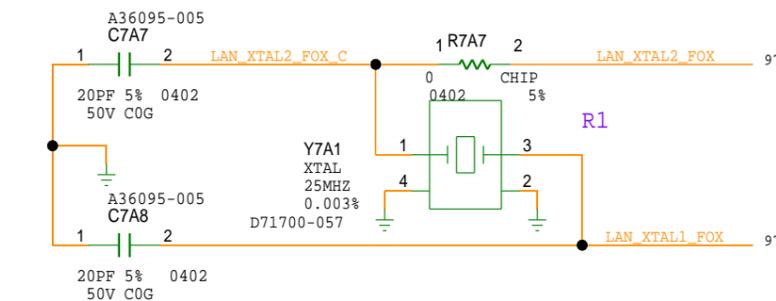
PCIE SIGNALS



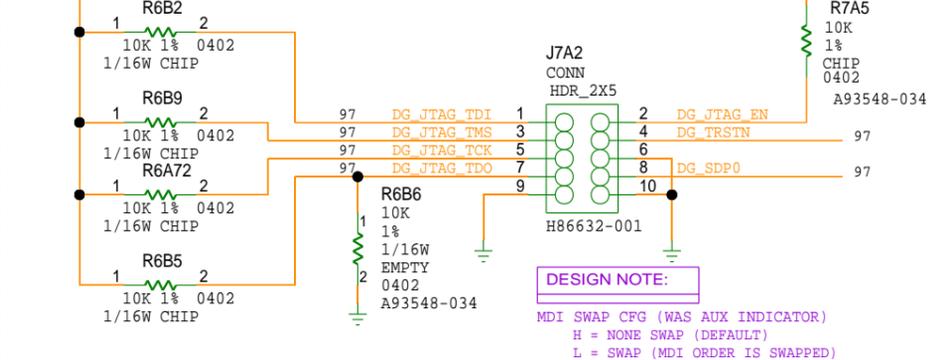
POWER MANAGEMENT



25MHZ / 3225 SMD CRYSTAL

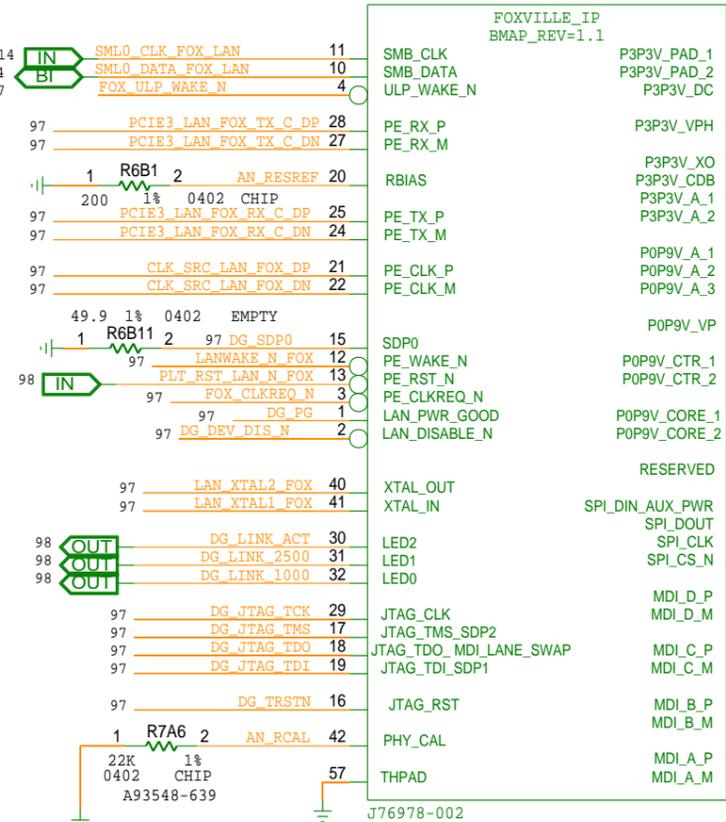


JTAG HEADER

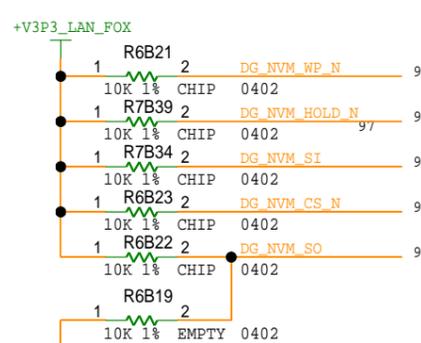


DESIGN NOTE:
MDI SWAP CFG (WAS AUX INDICATOR)
H = NONE SWAP (DEFAULT)
L = SWAP (MDI ORDER IS SWAPPED)

EU7A3 IC

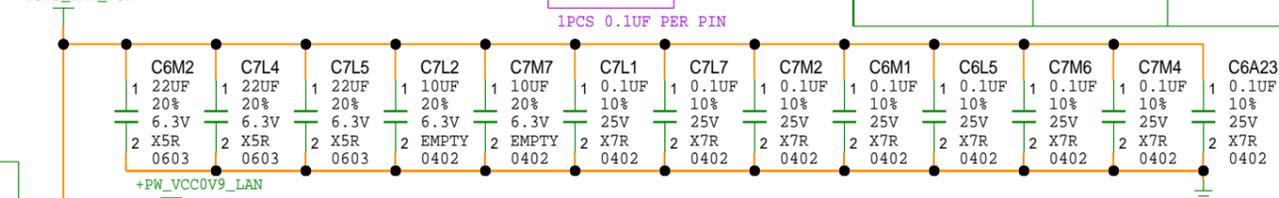


FLASH



DESIGN NOTE:
PCIE AUX INDICATOR IS NOT USED FOR LOM DESIGN.

+V3P3_LAN_FOX



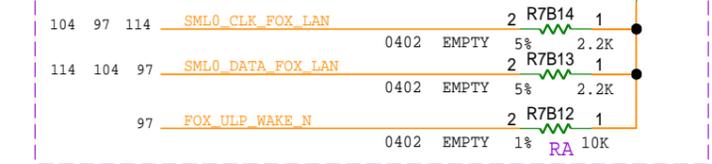
CAD NOTE:
1PCS 0.1UF PER PIN

CAD NOTE:
1PCS 0.1UF PER PIN

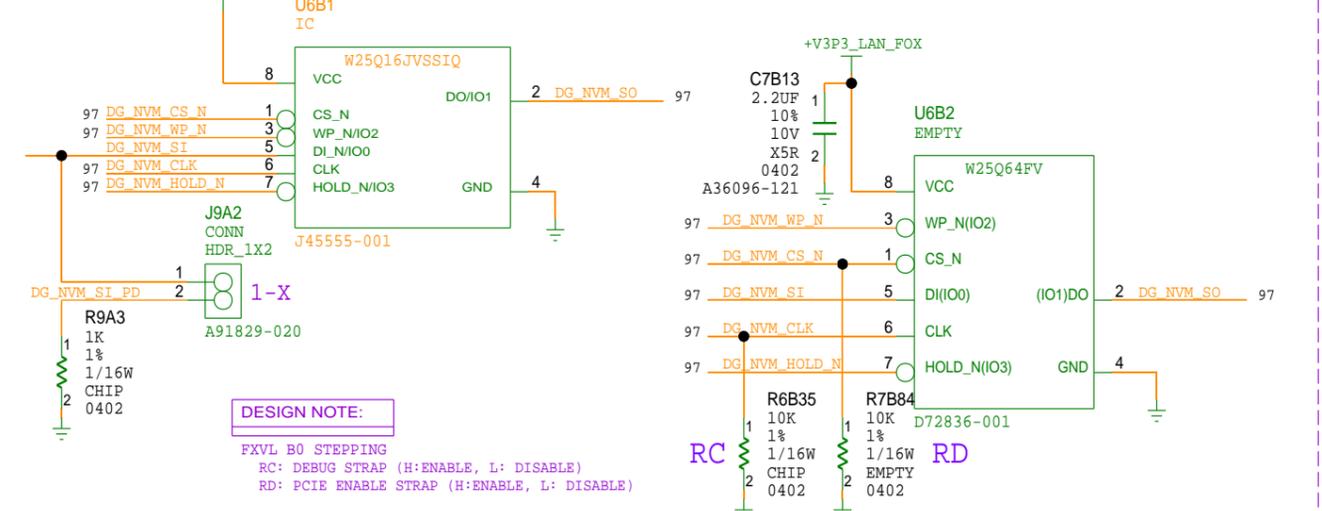
CAD NOTE:
1PCS 0.1UF PER PIN

DESIGN NOTE:
FOXVILLE CHIP
A0: STUFF RA, UNSTUFF RB
B0: STUFF RB, UNSTUFF RA

FOXVILLE SML PU



+V3P3_LAN_FOX



DESIGN NOTE:
FXVL B0 STEPPING
RC: DEBUG STRAP (H:ENABLE, L: DISABLE)
RD: PCIE ENABLE STRAP (H:ENABLE, L: DISABLE)

BPAGE DRAWING

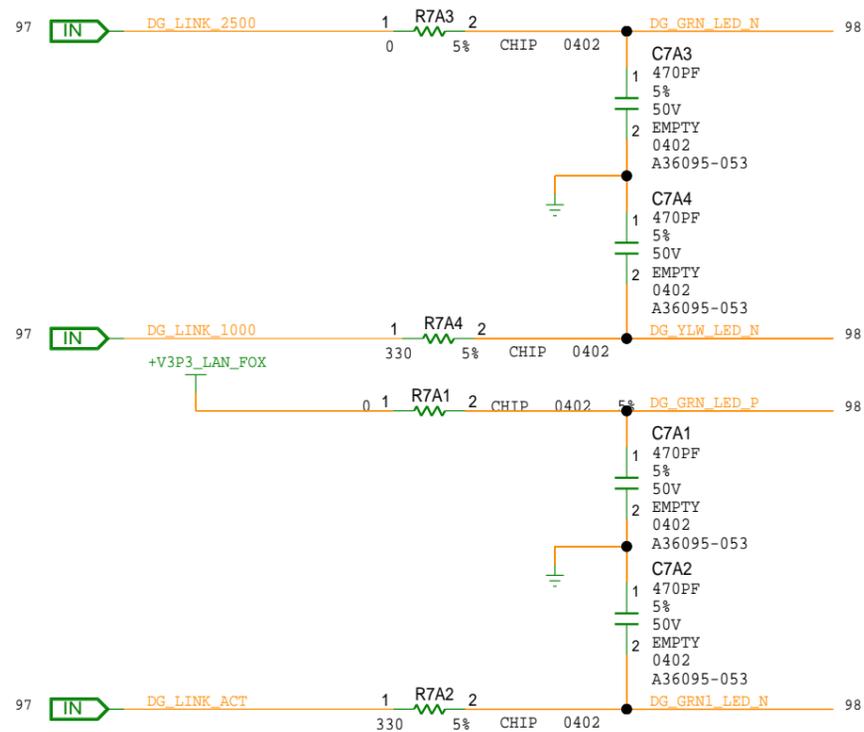
udimm.sch_1.97
Fri Sep 27 16:40:41 2019

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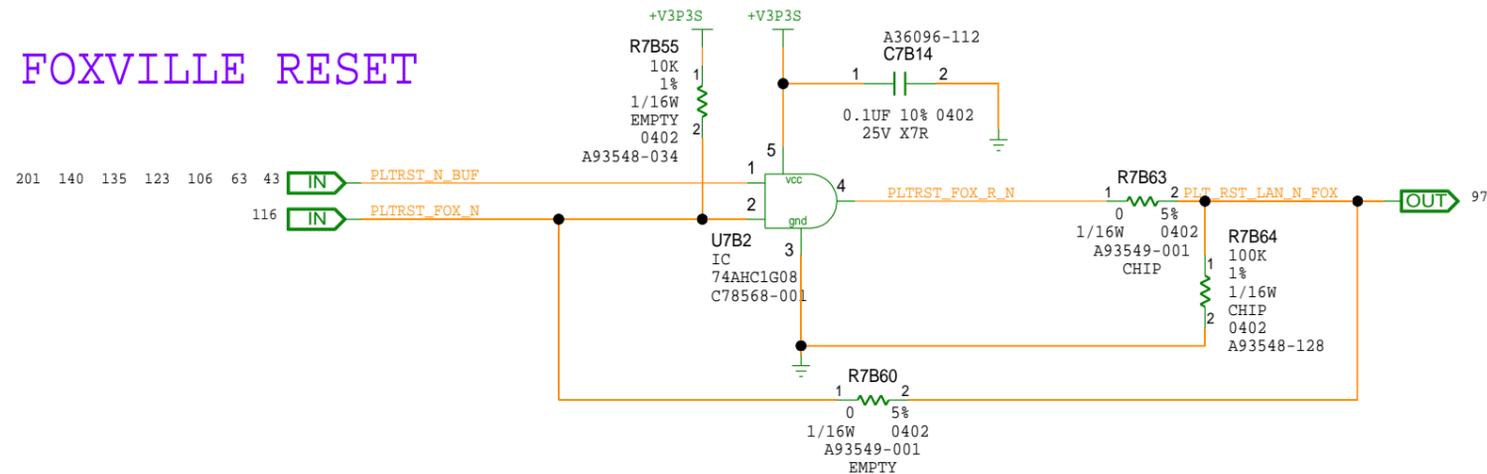
MODULE REV DETAILS

MODULE NAME	REV	DATE

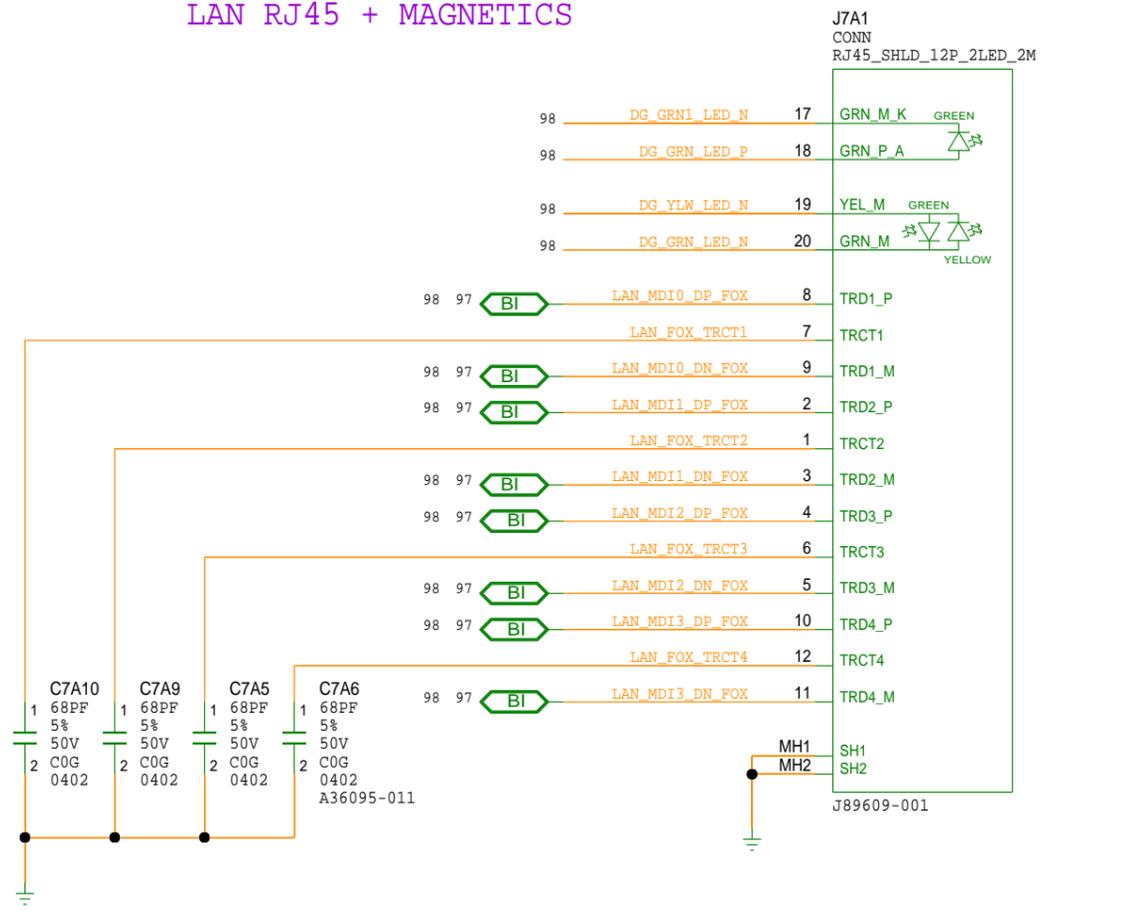
RJ45 LED CIRCUIT



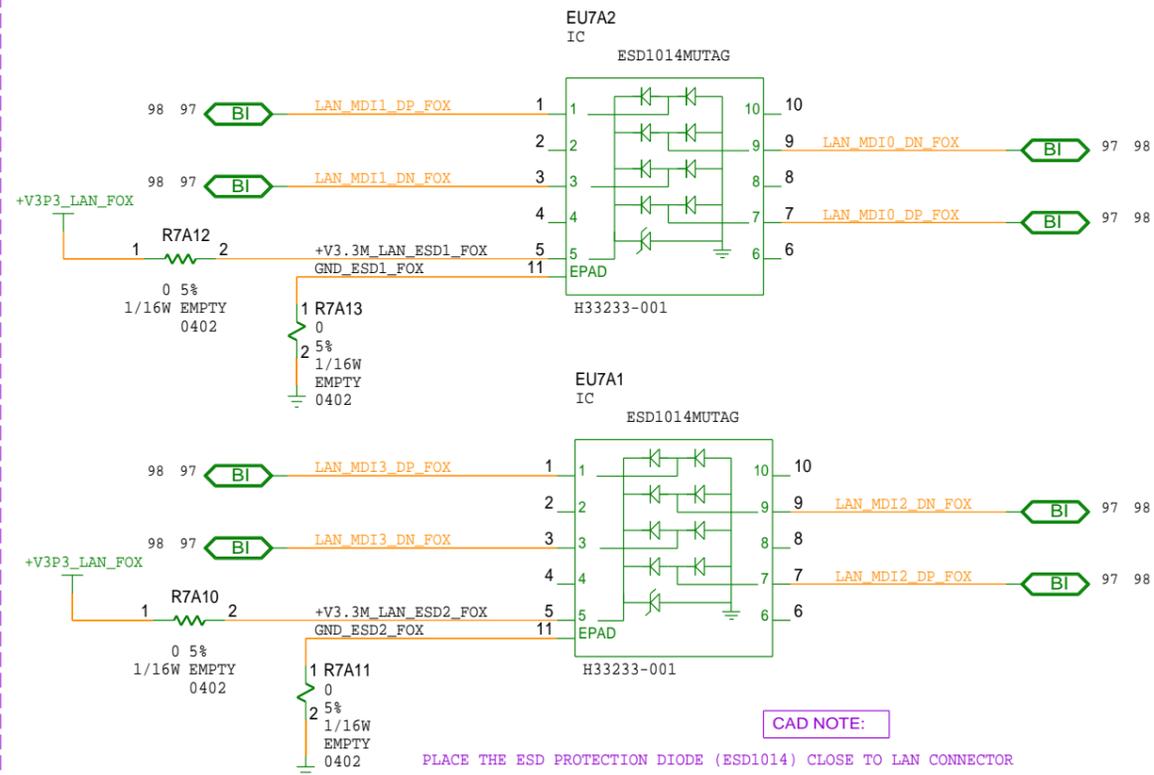
FOXVILLE RESET



LAN RJ45 + MAGNETICS



ESD PROTECTION DIODES



CAD NOTE:

PLACE THE ESD PROTECTION DIODE (ESD1014) CLOSE TO LAN CONNECTOR

BPAGE DRAWING

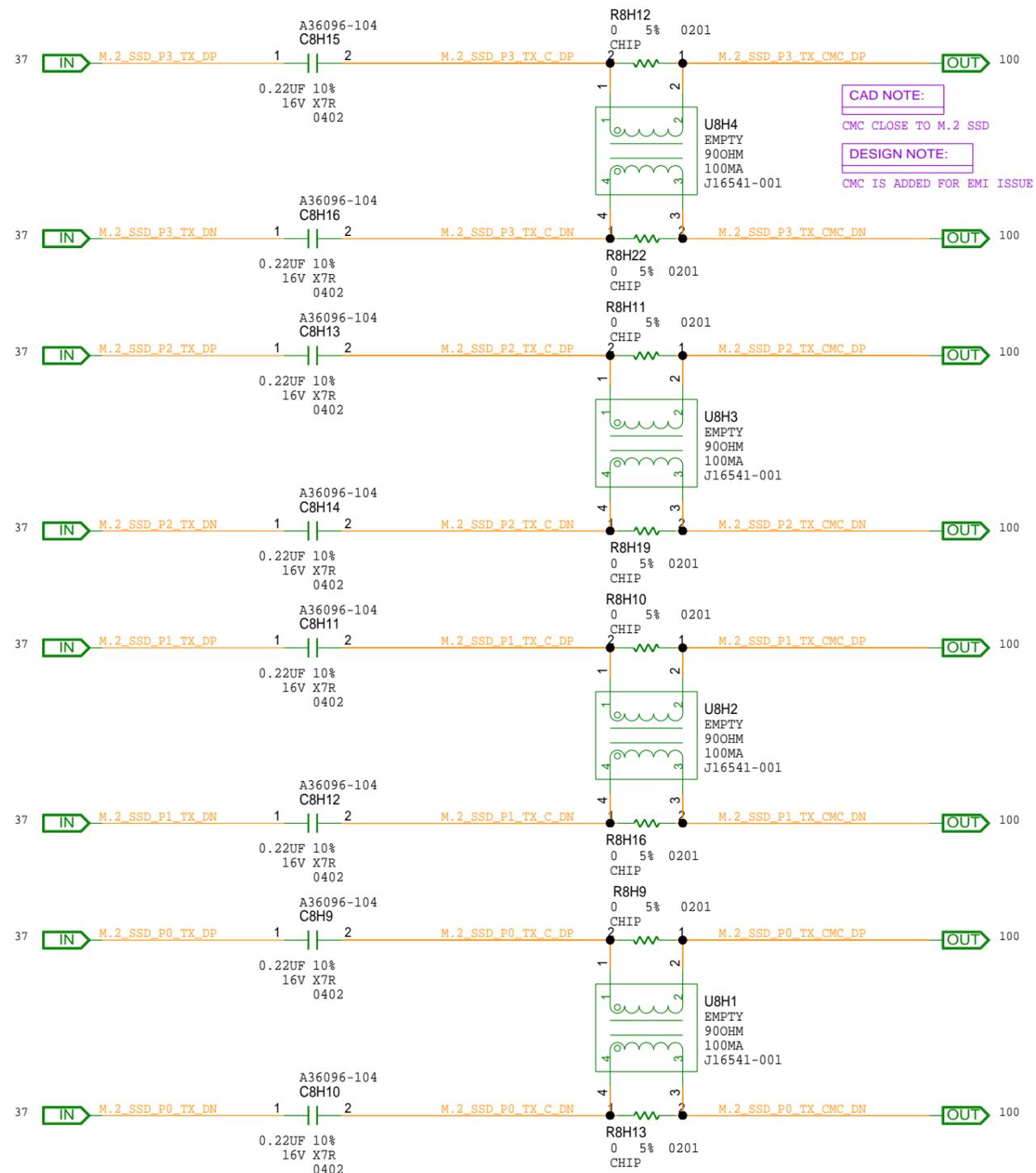
udimm.sch_1.98
Fri Sep 27 16:40:42 2019

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MODULE REV DETAILS

MODULE NAME	REV	DATE

AC CAP + CMC FOR M.2 SOCKET-3 SSD



CAD NOTE:
CMC CLOSE TO M.2 SSD

DESIGN NOTE:
CMC IS ADDED FOR EMI ISSUE

BPAGE DRAWING
udimm.sch_1.99
Fri Sep 27 16:40:43 2019

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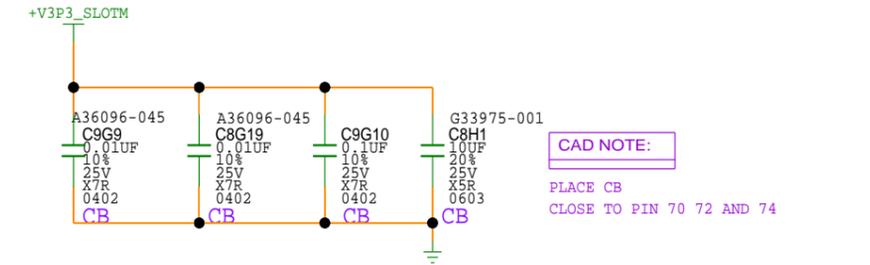
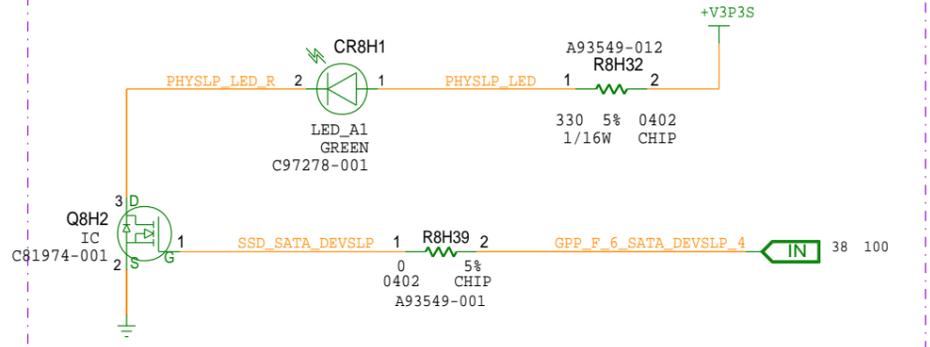
MODULE REV DETAILS

MODULE NAME	REV	DATE

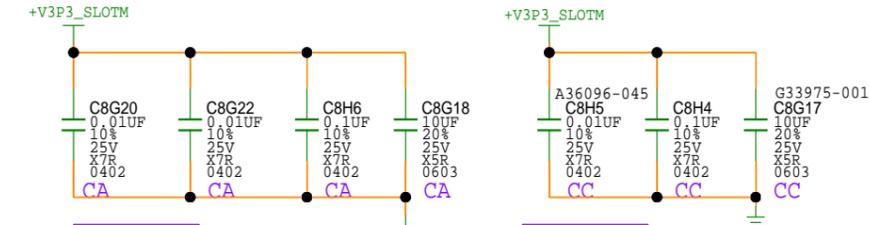
M.2 SOCKET-3 SSD

8.2MM HEIGHT CONNECTOR

SATA DEVSLEP LED FOR M.2 SSD

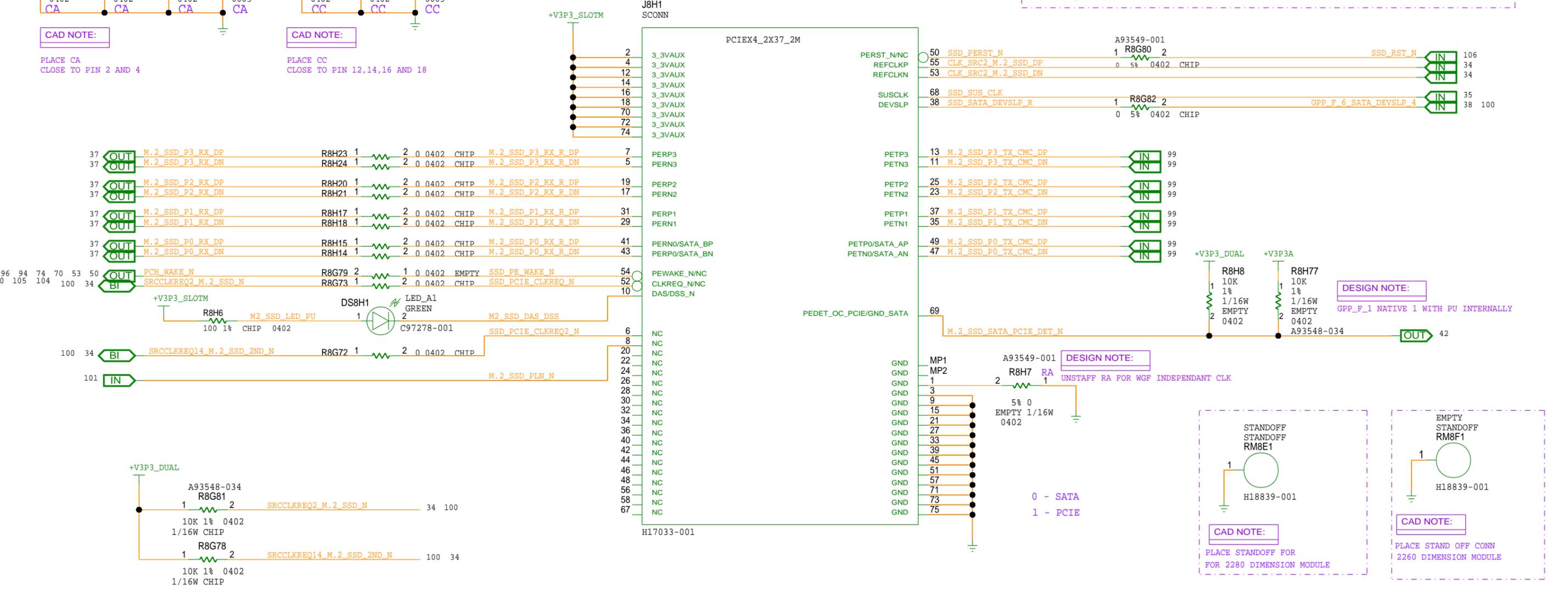


CAD NOTE:
PLACE CB
CLOSE TO PIN 70 72 AND 74



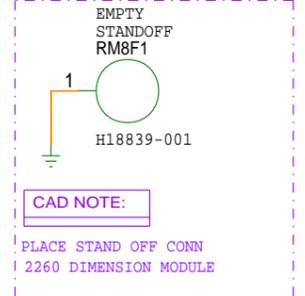
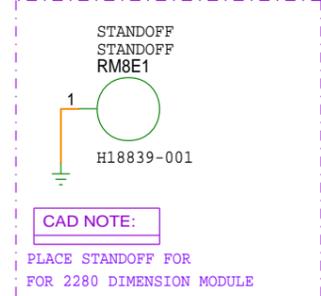
CAD NOTE:
PLACE CA
CLOSE TO PIN 2 AND 4

CAD NOTE:
PLACE CC
CLOSE TO PIN 12,14,16 AND 18



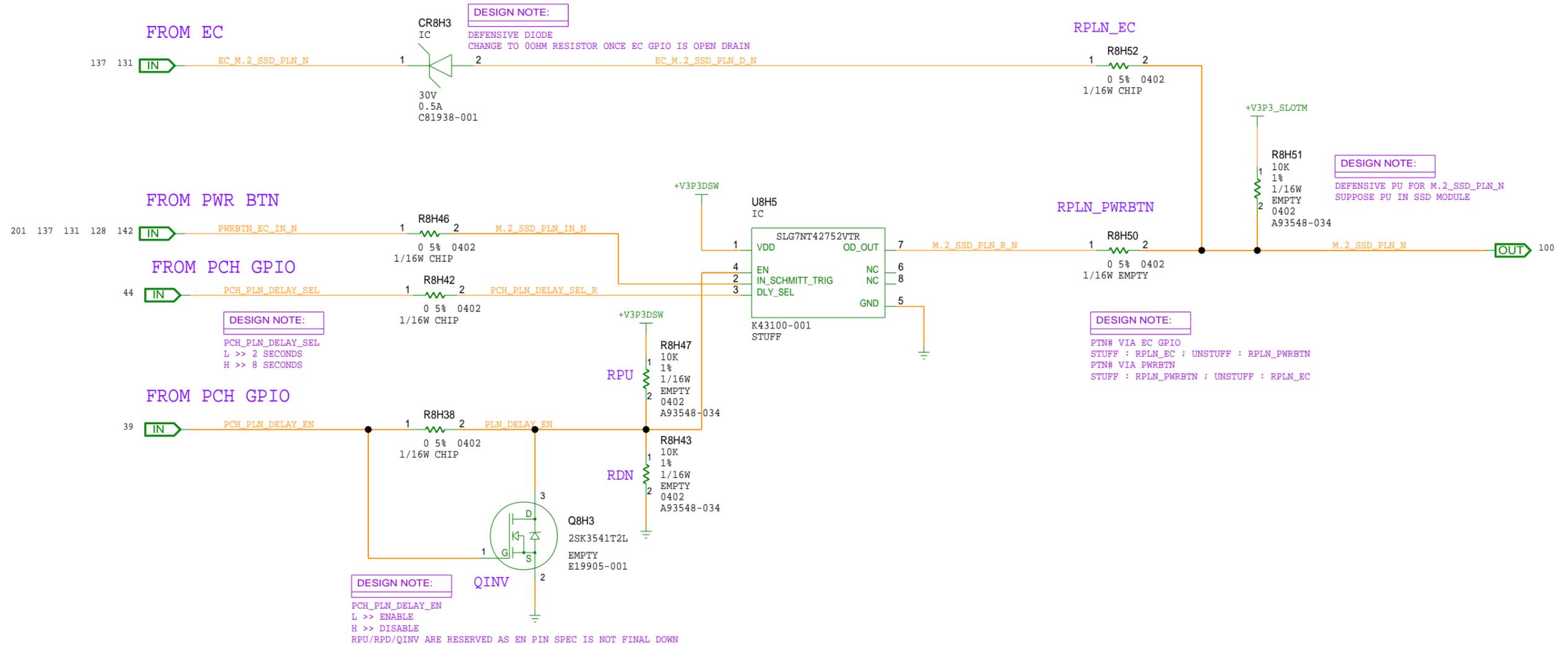
DESIGN NOTE:
GPP_F_1 NATIVE 1 WITH PU INTERNALLY

DESIGN NOTE:
UNSTAFF RA FOR WGF INDEPENDANT CLK



MODULE REV DETAILS		
MODULE NAME	REV	DATE
	-	

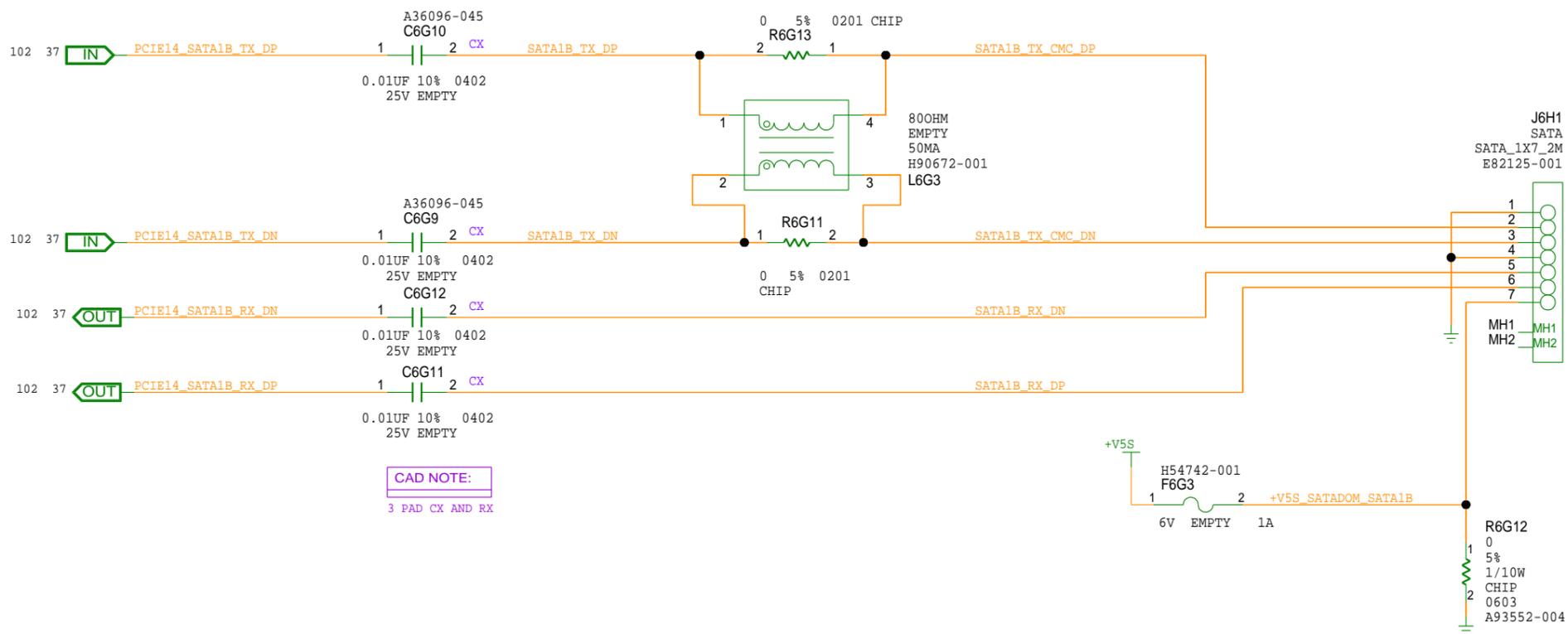
M.2 SOCKET-3 SSD PLN# CIRCUIT



MODULE REV DETAILS

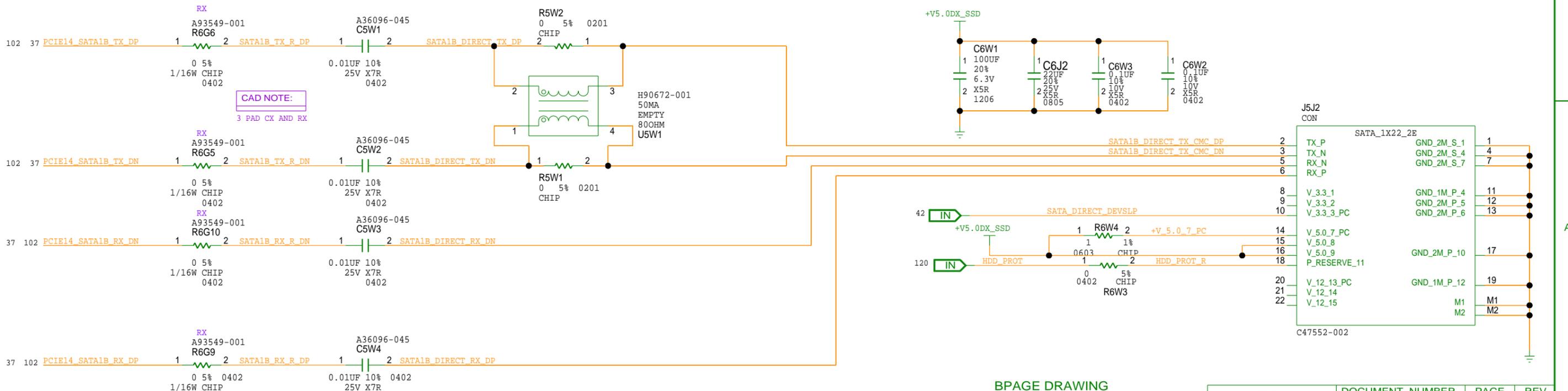
MODULE NAME	REV	DATE

SATA GEN3 CABLE CONNECTOR(P1B)



CAD NOTE:
3 PAD CX AND RX

SATA GEN3 DIRECT CONNECTOR (P1B)



CAD NOTE:
3 PAD CX AND RX

BPAGE DRAWING

udimm.sch_1.102
Fri Sep 27 16:40:46 2019

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[PAGE_TITLE=STORAGE - SATA P1B DIRECT CONNECTOR]

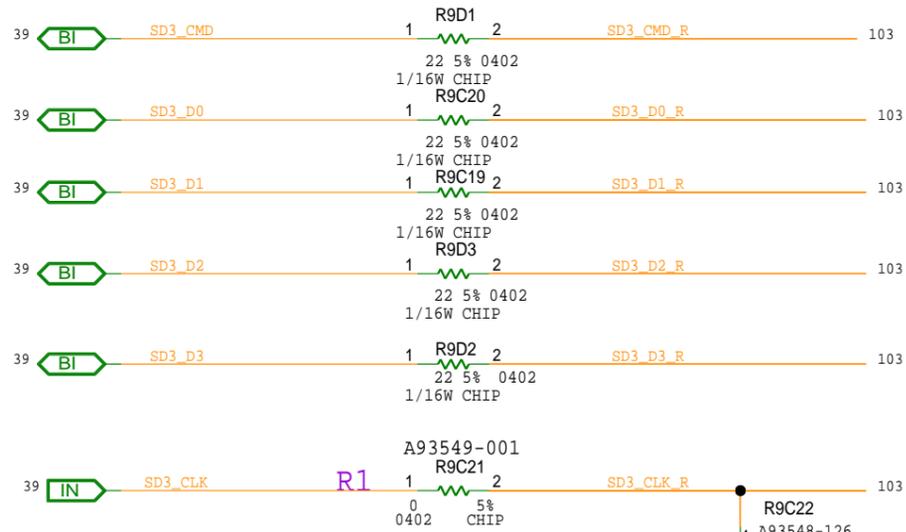
MODULE REV DETAILS

MODULE NAME	REV	DATE

STORAGE - SD CONNECTOR

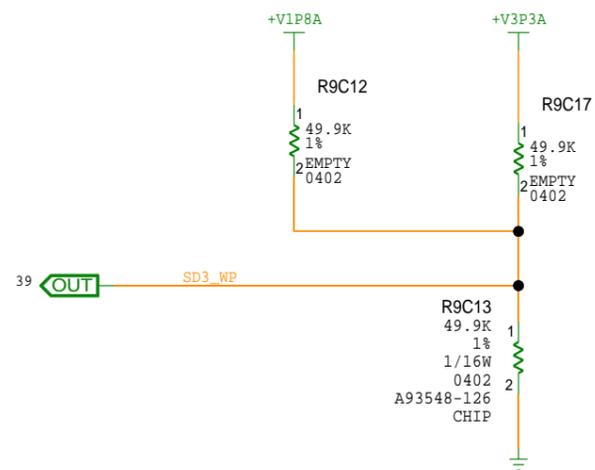
CAD NOTE:

PLACE SERIES RESISTORS CLOSE TO CONNECTOR WITHIN 12.7MM

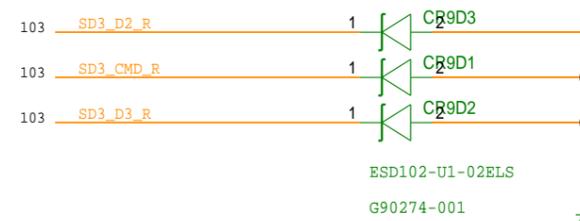
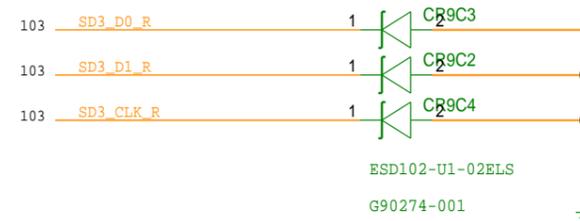


DESIGN NOTE:

R1 IS FOR DEBUG PURPOSE. SERIES RESISTOR ON SD3_CLK IS NOT REQUIRED



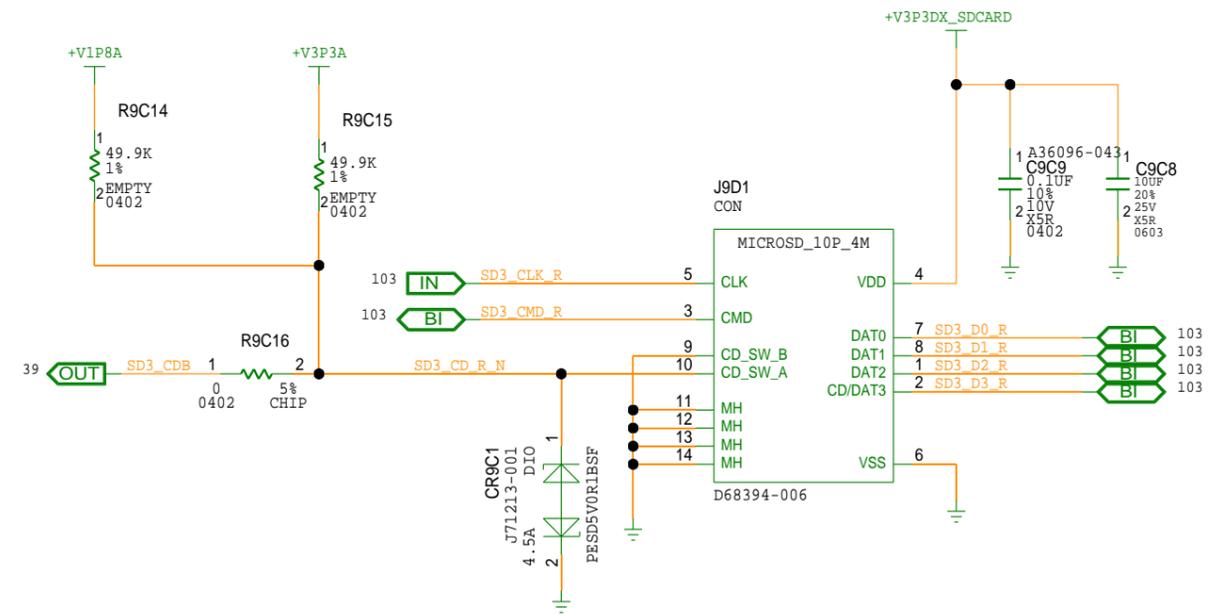
ESD PROTECTION DIODE



DESIGN NOTE:

ESD3V3XU1US COMPLIANCE

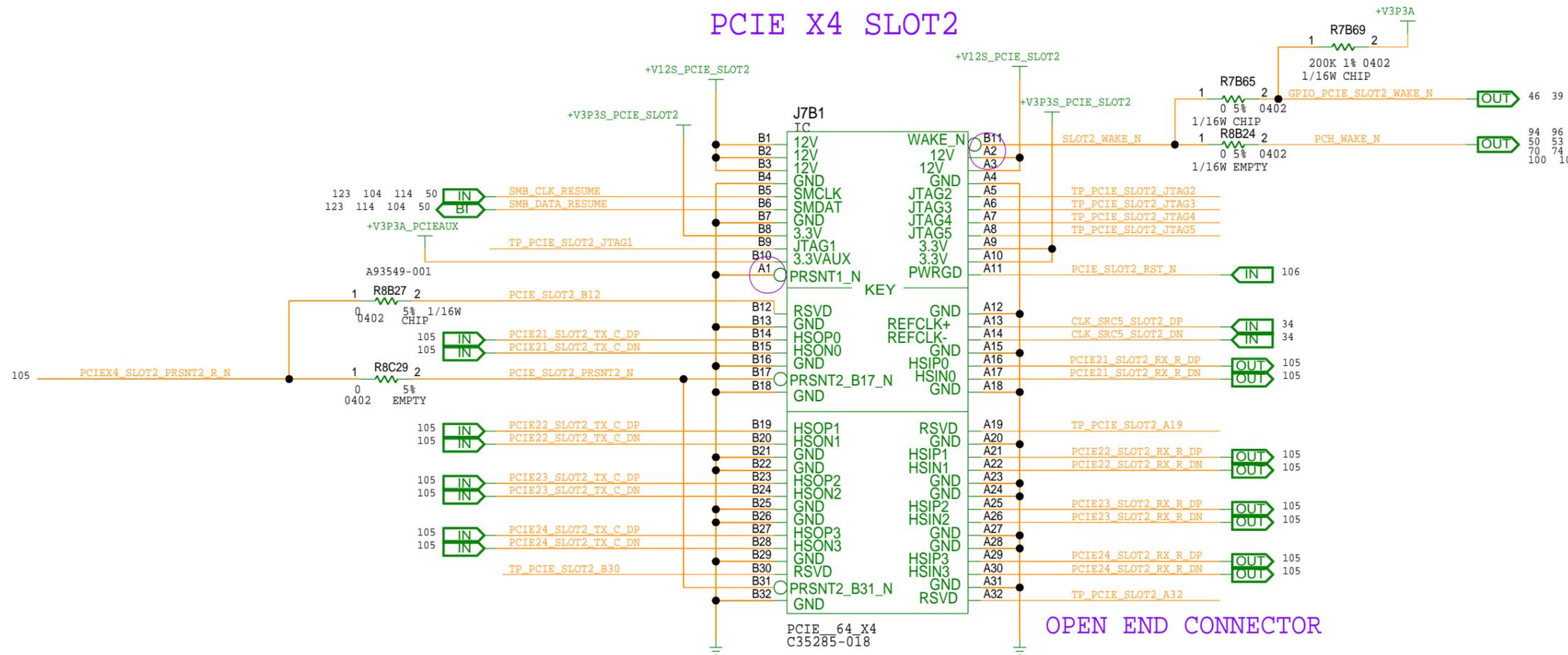
MICRO SD3.0 CARD CONNECTOR



MODULE REV DETAILS

MODULE NAME	REV	DATE

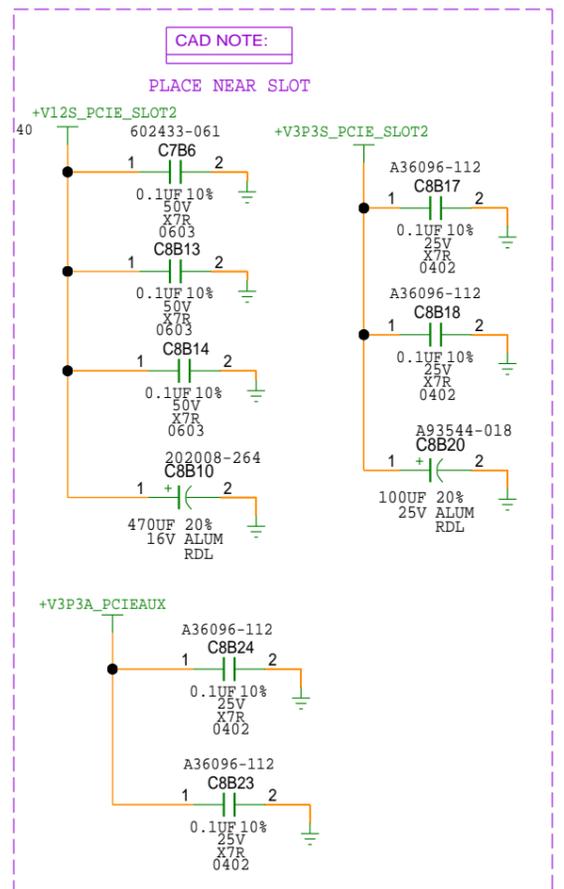
PCIE X4 SLOT2



OPEN END CONNECTOR

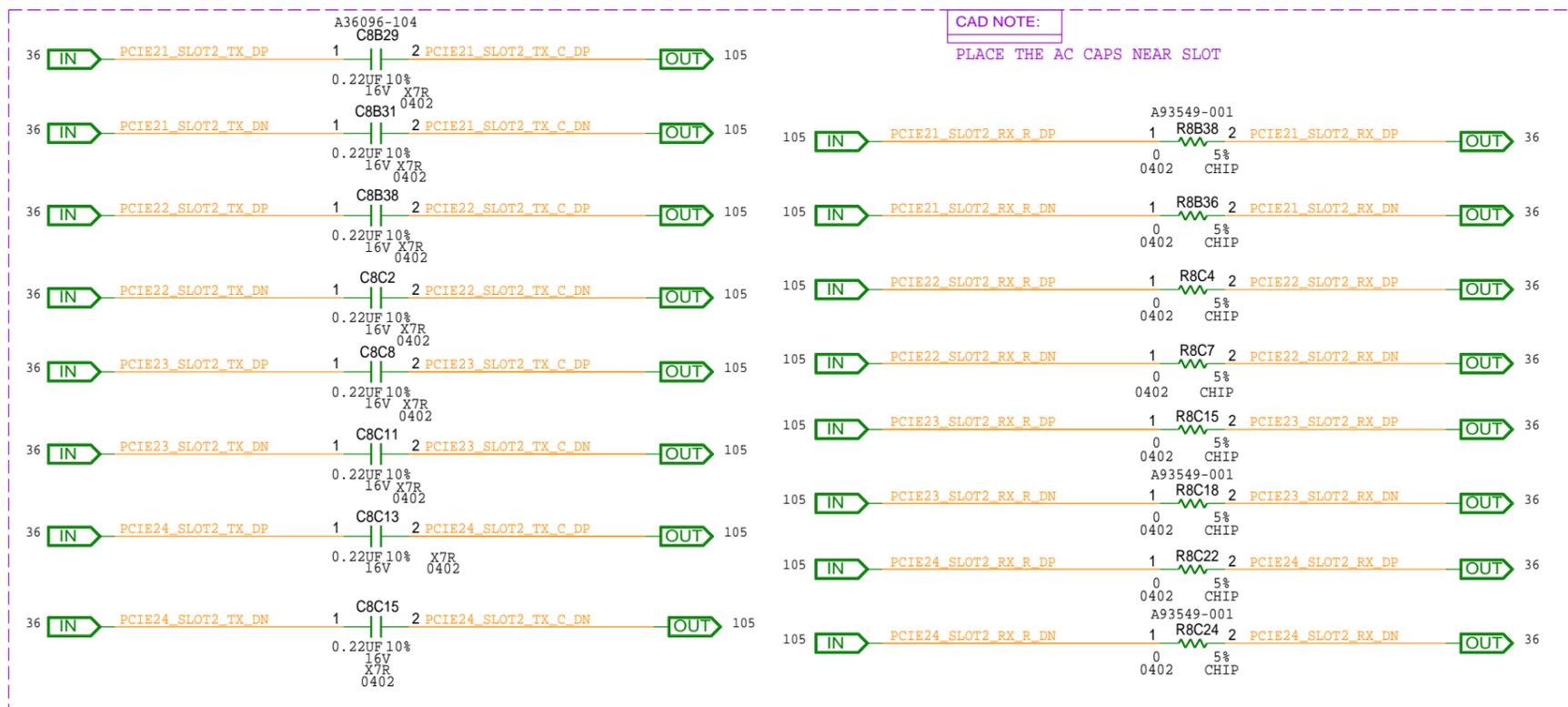
CAD NOTE:

PLACE NEAR SLOT



CAD NOTE:

PLACE THE AC CAPS NEAR SLOT



BPAGE DRAWING

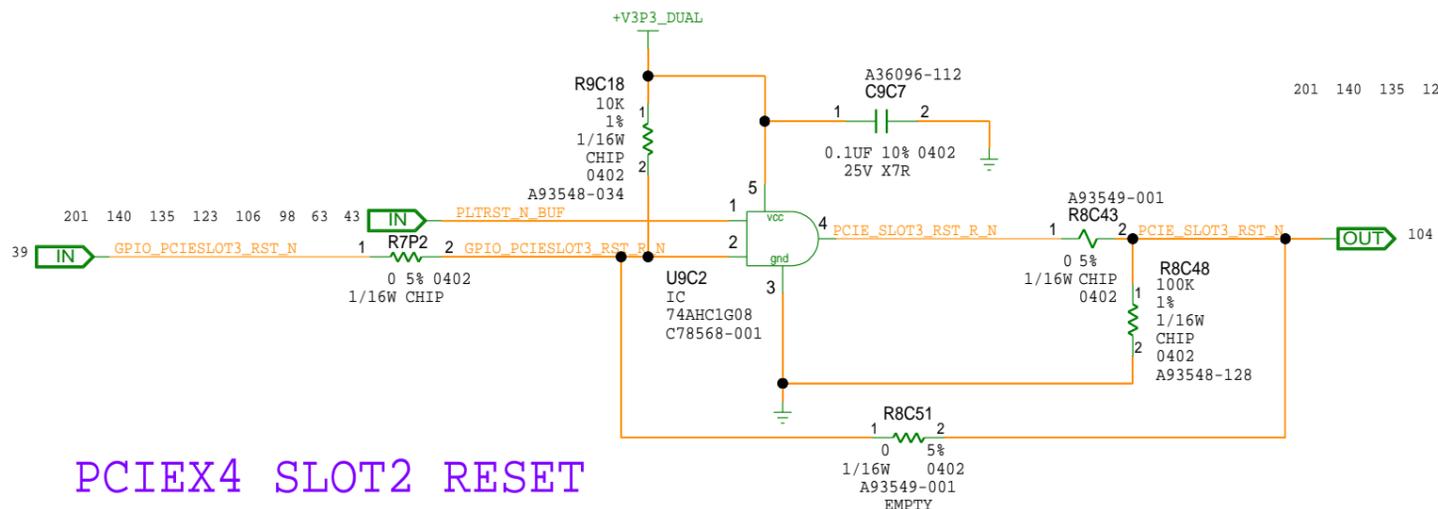
udimm.sch_1.105
Fri Sep 27 16:40:49 2019

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	xxxxxxx	105	0.7

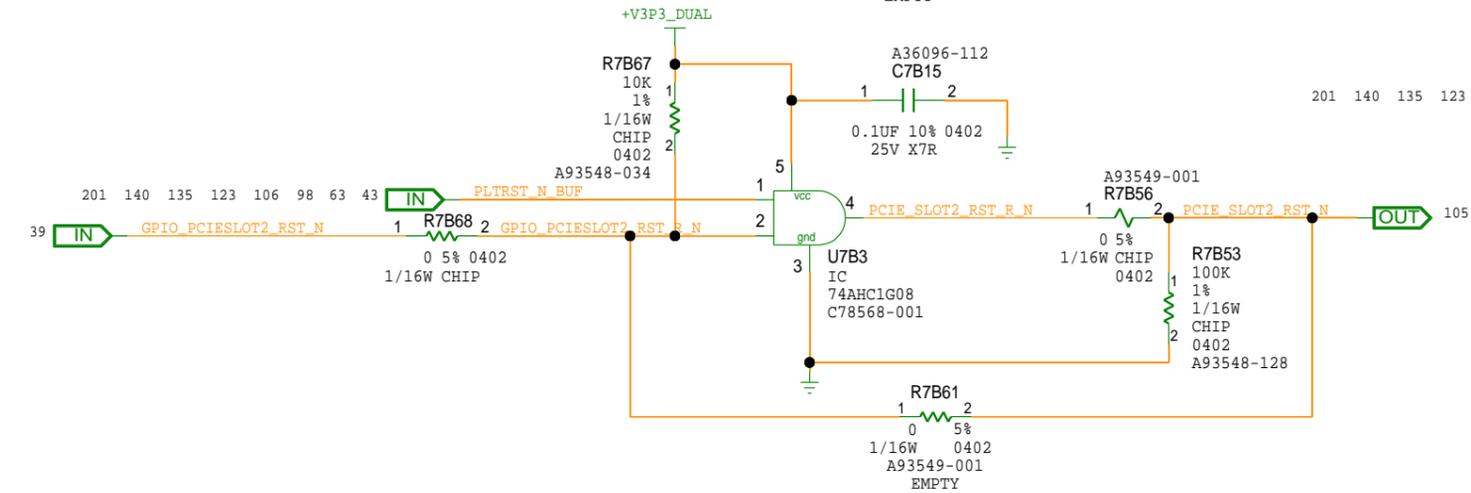
[PAGE_TITLE = PCIE X4 SLOT2]

MODULE REV DETAILS		
MODULE NAME	REV	DATE

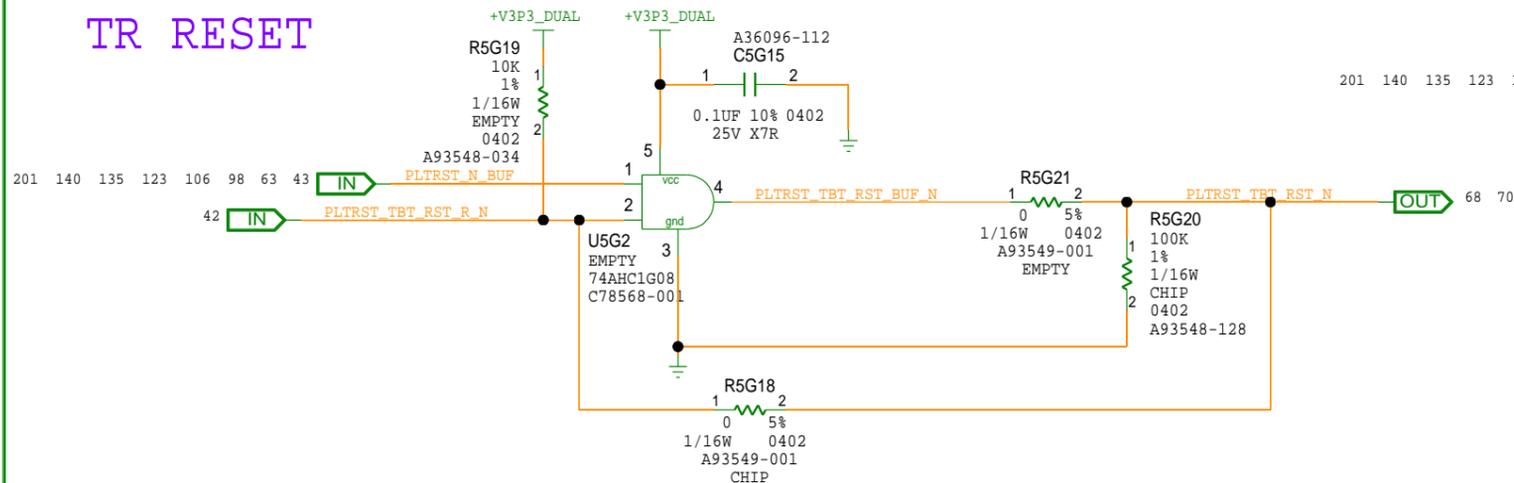
PCIEX4 SLOT3 RESET



PCIEX4 SLOT2 RESET

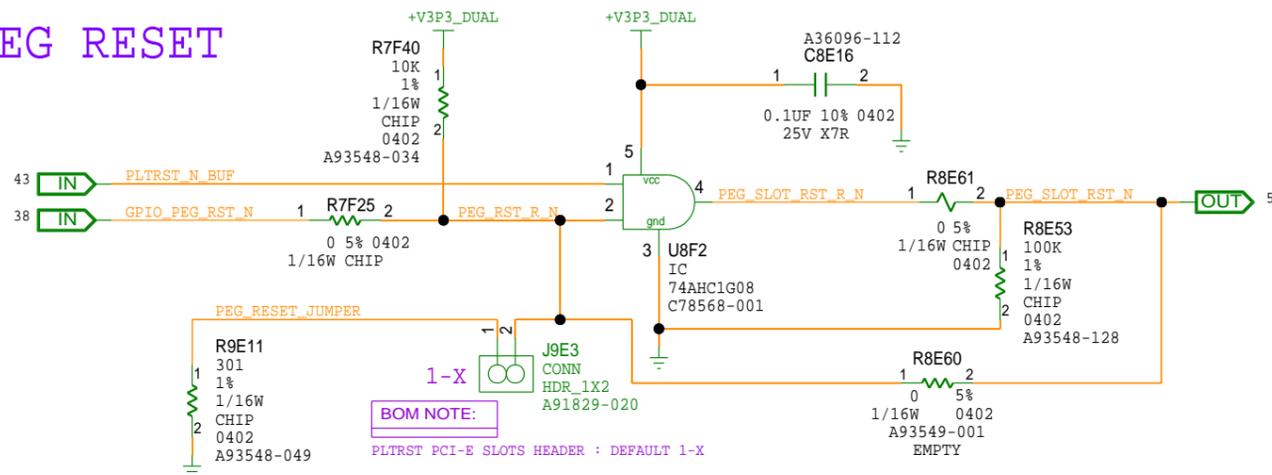


TR RESET

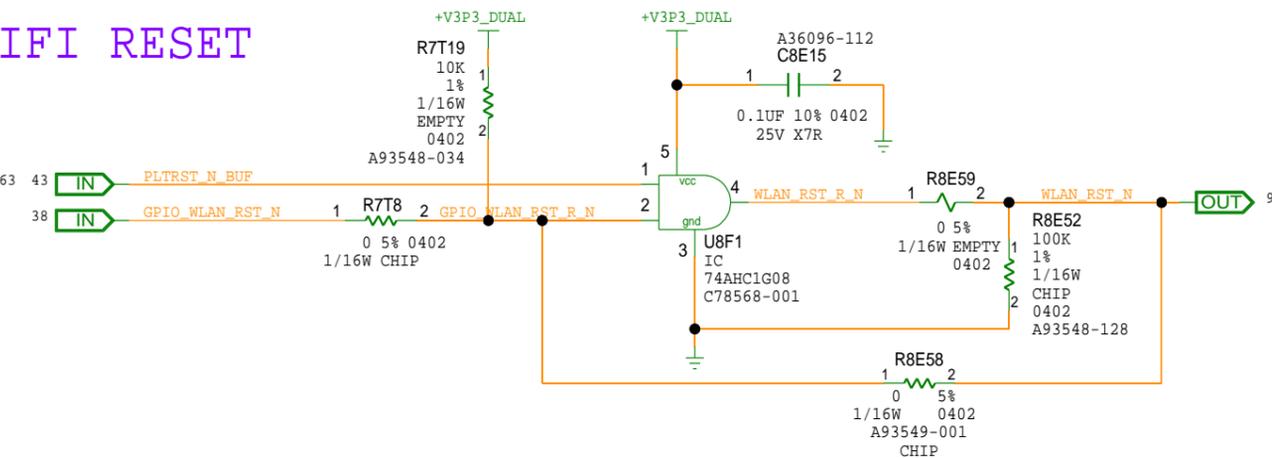


[PAGE_TITLE=PCIE RESET LOGIC]

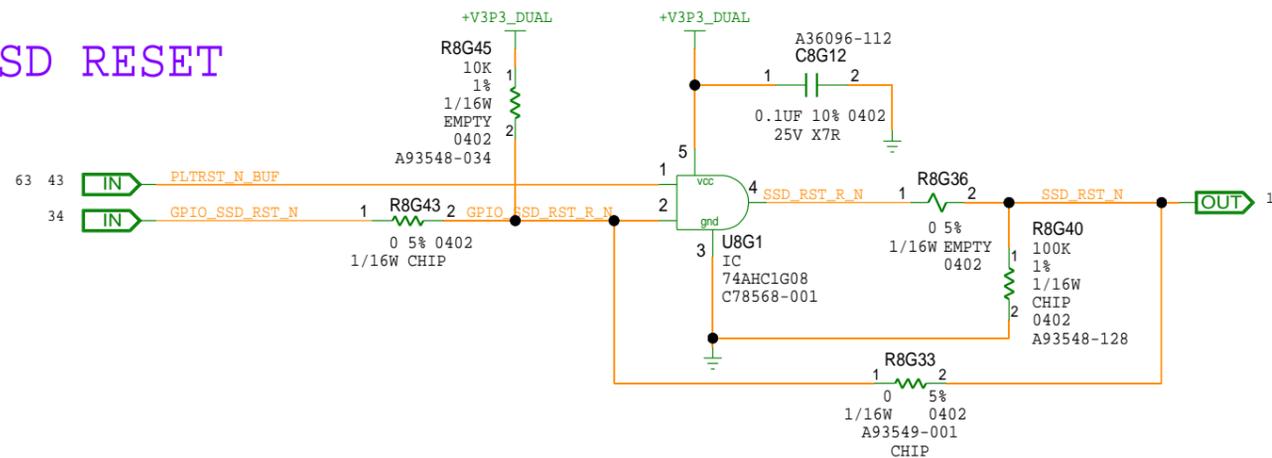
PEG RESET



WIFI RESET



SSD RESET



BPAGE DRAWING

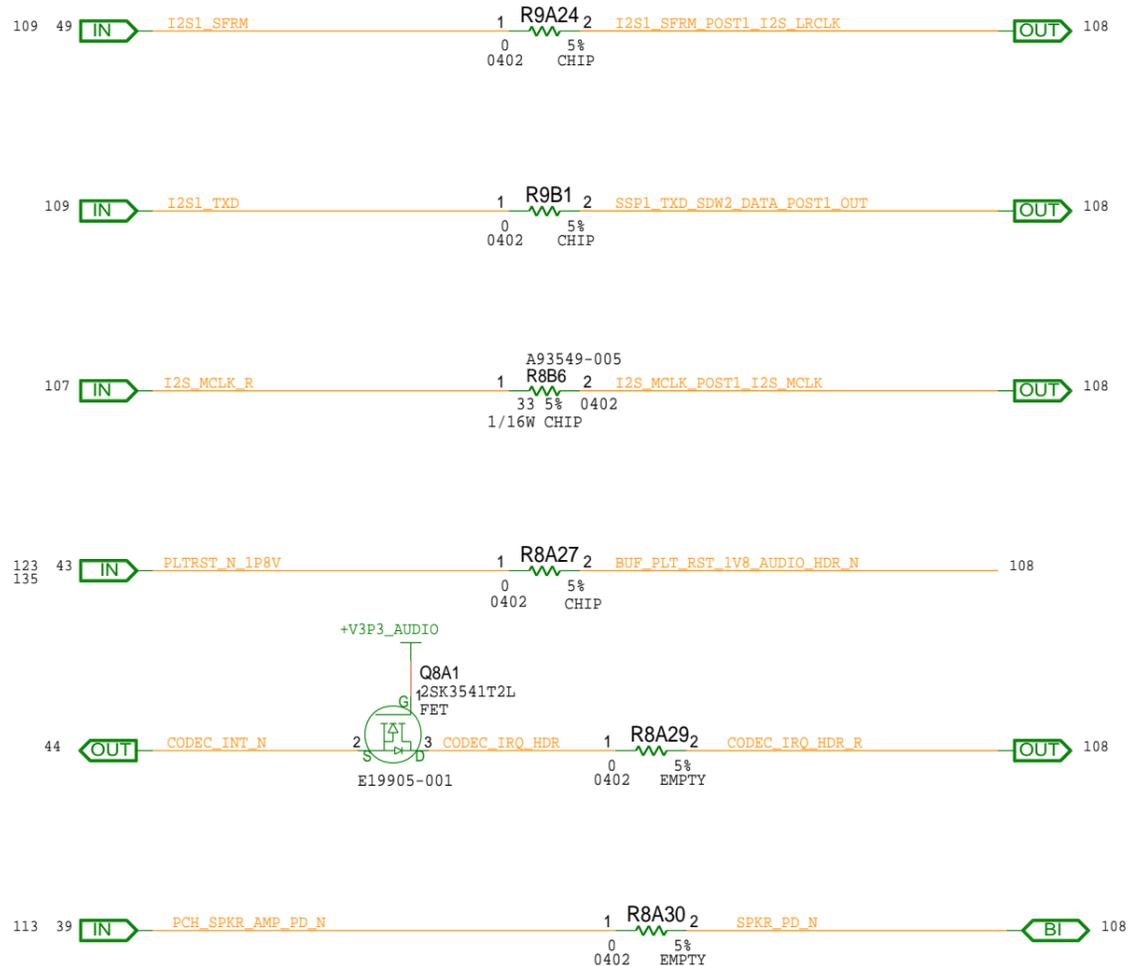
ditmy.sch_1.105
Tue Apr 17 15:10:34 2018

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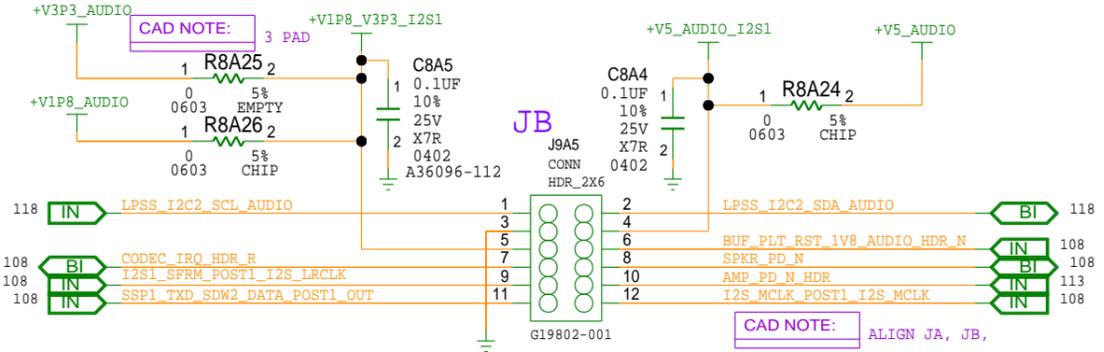
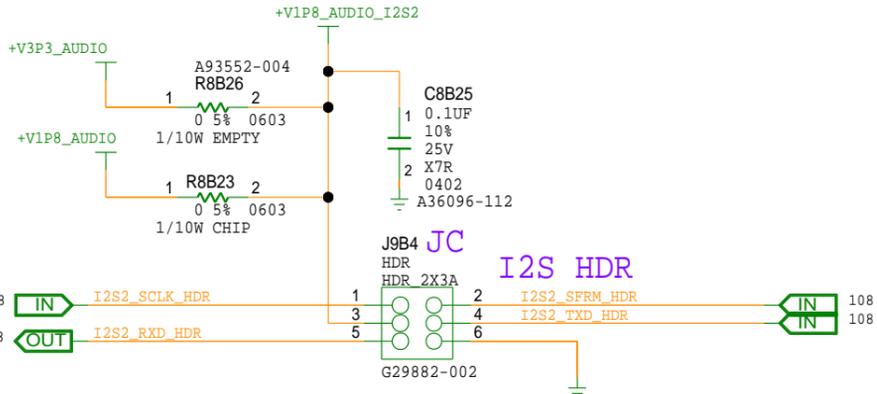
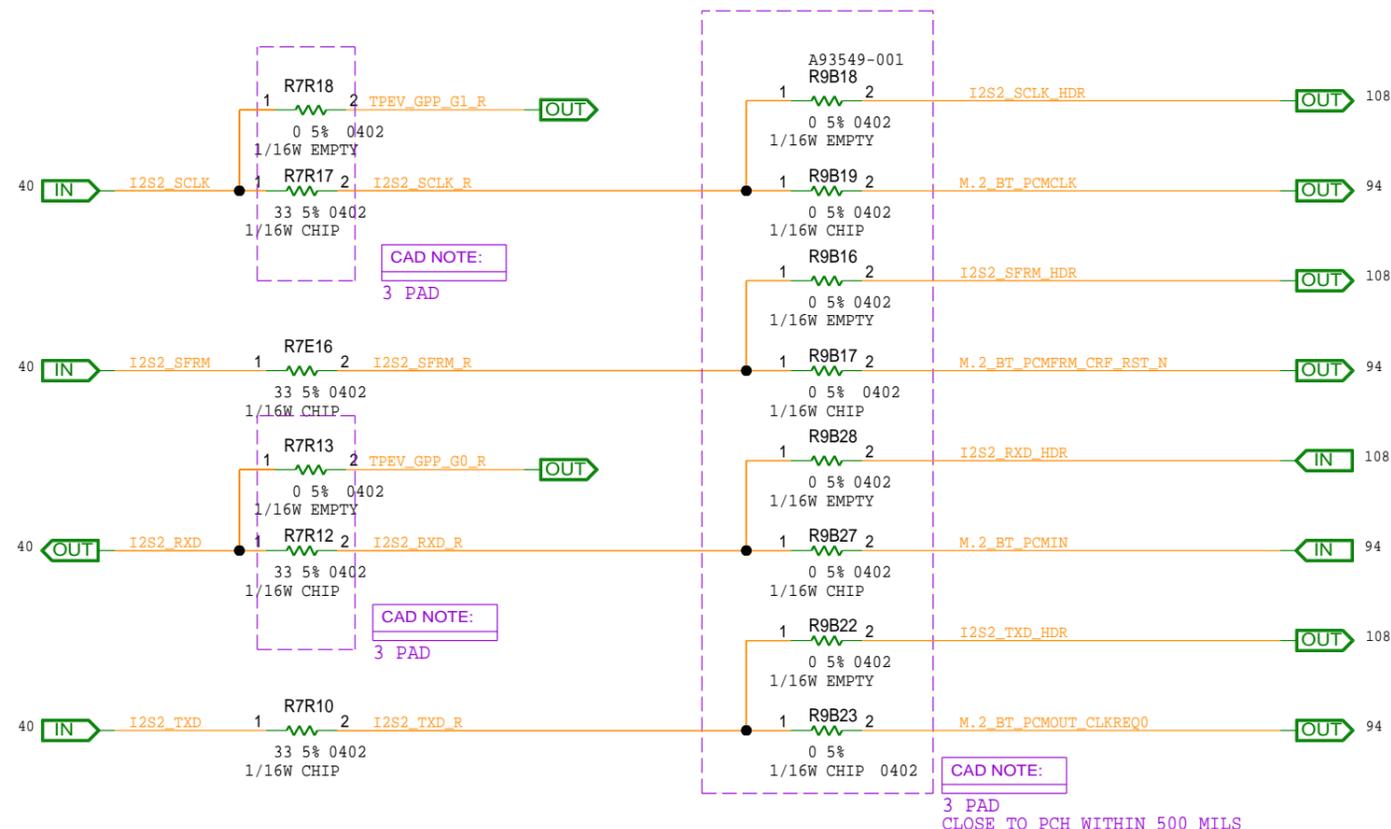
MODULE REV DETAILS

MODULE NAME	REV	DATE

PCH I2S1 TO HDR



I2S2 OPTIONS TO M.2 BT OR HDR

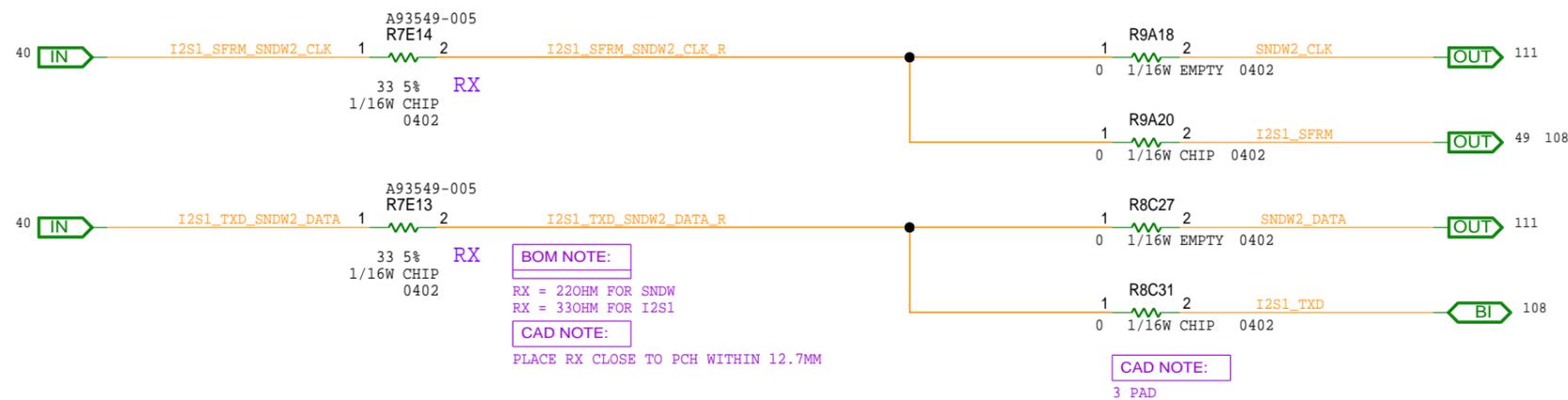


CAD NOTE: ALIGN JA, JB,

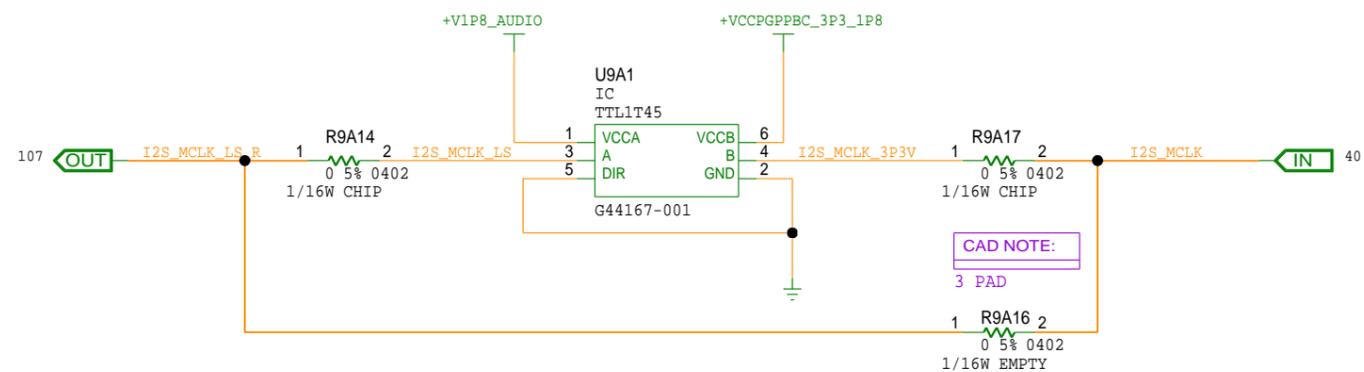
MODULE REV DETAILS

MODULE NAME	REV	DATE

SNDW2/I2S1 1 LOAD TOPOLOGY



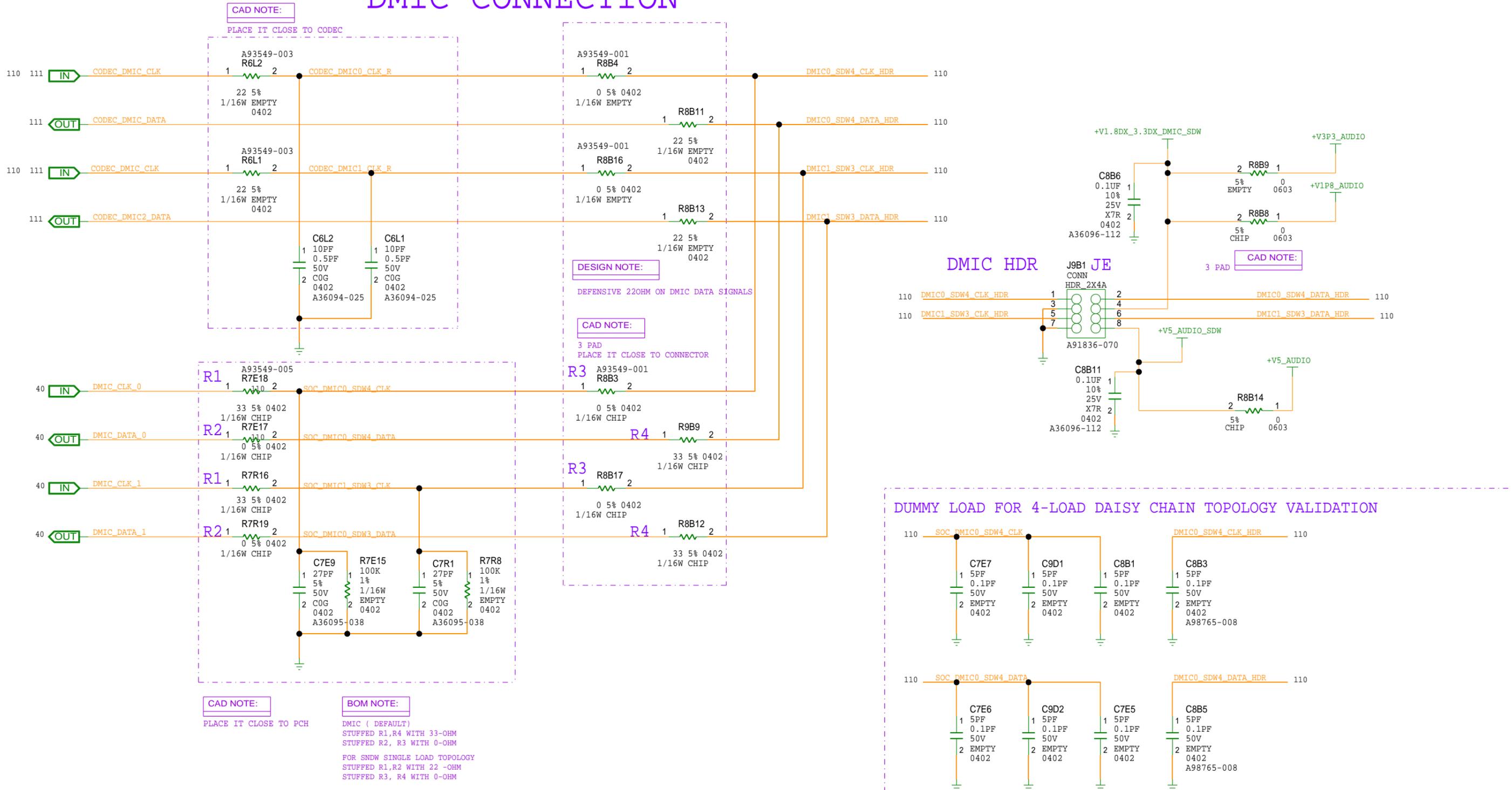
I2S_MCLK LEVEL SHIFTER



MODULE REV DETAILS

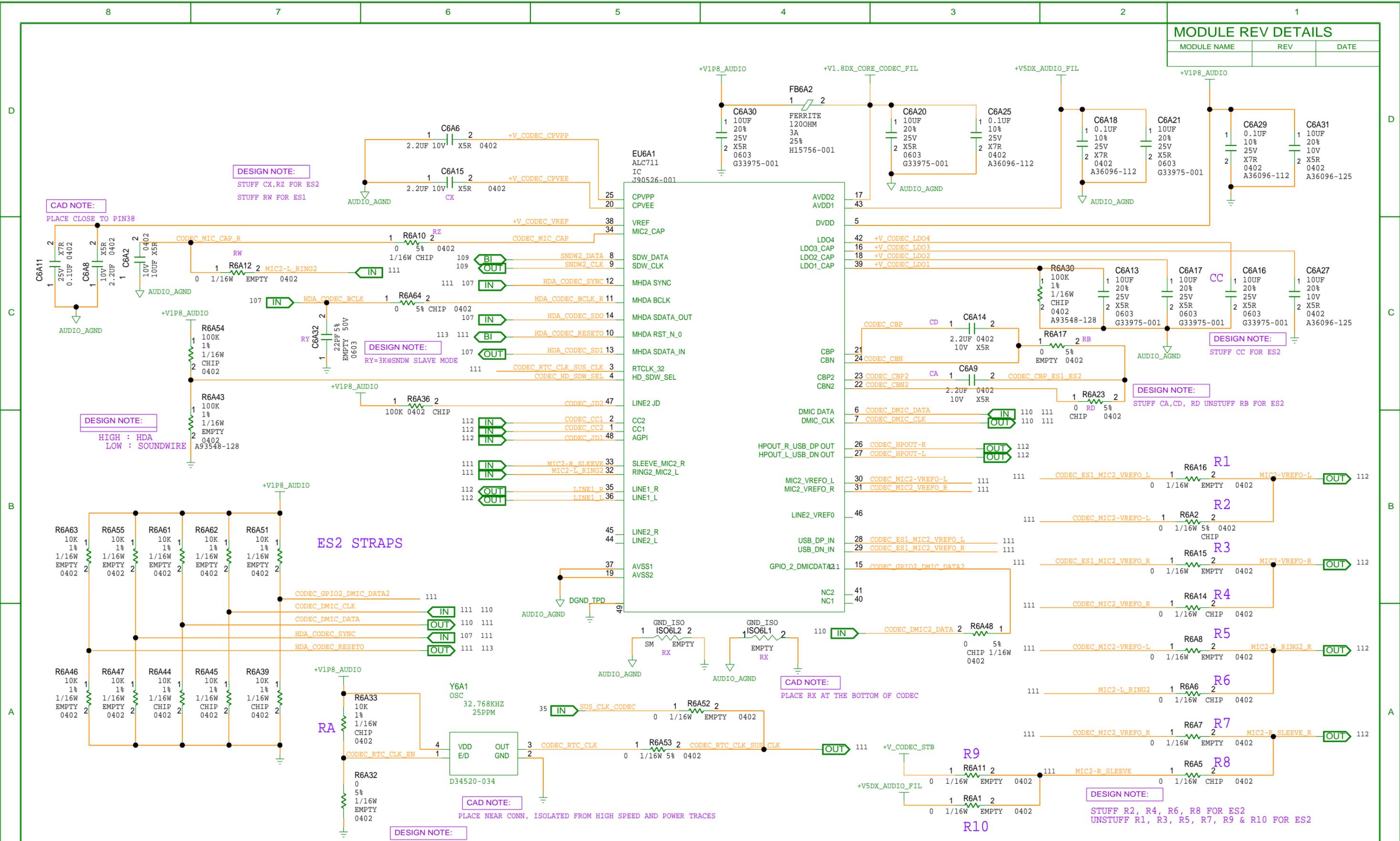
MODULE NAME	REV	DATE

DMIC CONNECTION



MODULE REV DETAILS

MODULE NAME	REV	DATE



DESIGN NOTE:
STUFF CX,RZ FOR ES2
STUFF RW FOR ES1

CAD NOTE:
PLACE CLOSE TO PIN38

DESIGN NOTE:
RY=3K@SNDW SLAVE MODE

DESIGN NOTE:
HIGH : HDA
LOW : SOUNDWIRE

ES2 STRAPS

CAD NOTE:
PLACE RX AT THE BOTTOM OF CODEC

CAD NOTE:
PLACE NEAR CONN, ISOLATED FROM HIGH SPEED AND POWER TRACES

DESIGN NOTE:
STUFF RA FOR ES2 TO ENABLE VAD

DESIGN NOTE:
STUFF CC FOR ES2

DESIGN NOTE:
STUFF CA,CD, RD UNSTUFF RB FOR ES2

DESIGN NOTE:
STUFF R2, R4, R6, R8 FOR ES2
UNSTUFF R1, R3, R5, R7, R9 & R10 FOR ES2

[PAGE_TITLE=AUDIO - CODEC ALC711]

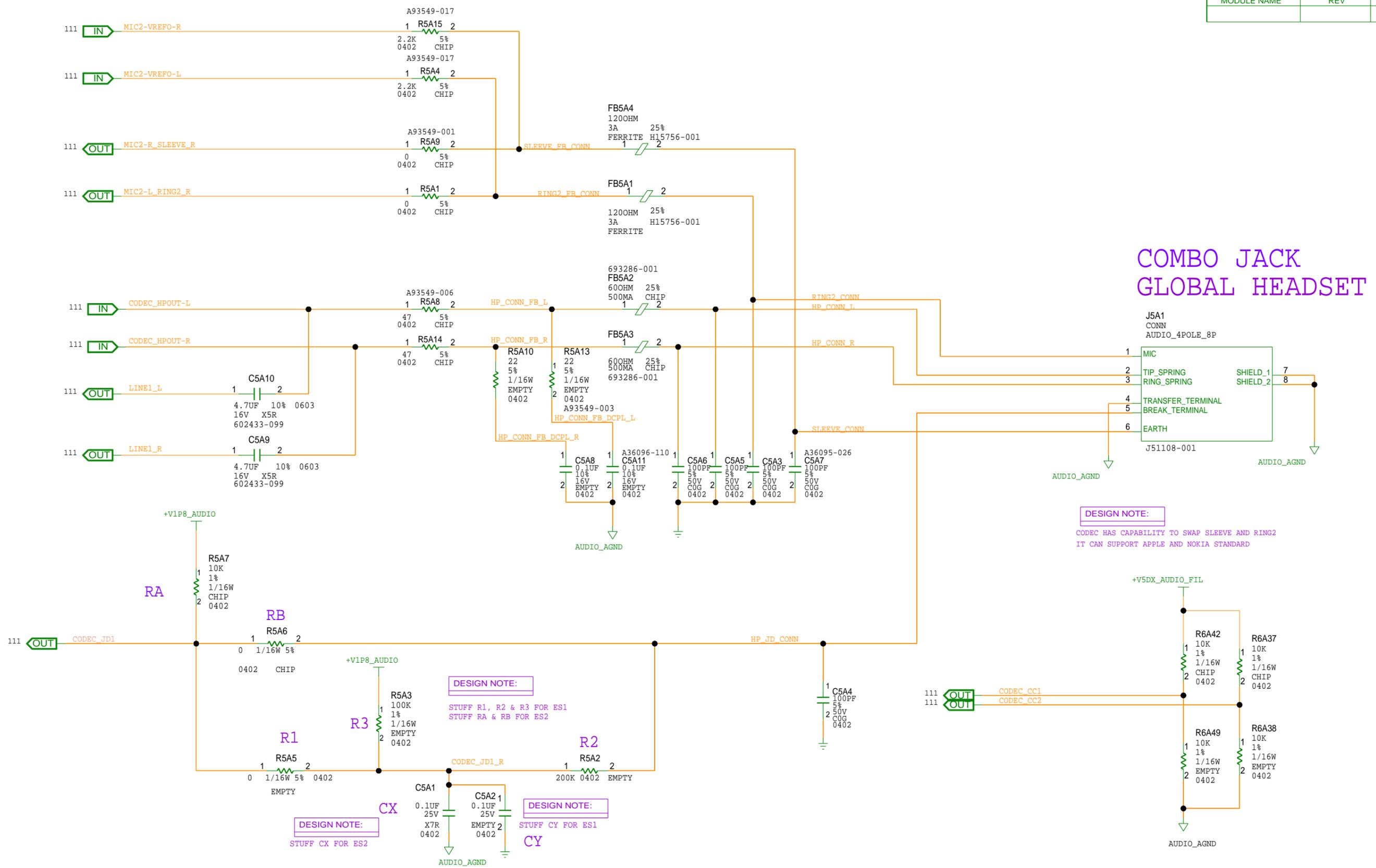
BPAGE DRAWING

udimm.sch.1.111
Fri Sep 27 16:40:56 2019

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MODULE REV DETAILS

MODULE NAME	REV	DATE



COMBO JACK GLOBAL HEADSET

DESIGN NOTE:
CODEC HAS CAPABILITY TO SWAP SLEEVE AND RING2
IT CAN SUPPORT APPLE AND NOKIA STANDARD

DESIGN NOTE:
STUFF R1, R2 & R3 FOR ES1
STUFF RA & RB FOR ES2

DESIGN NOTE:
STUFF CY FOR ES1

DESIGN NOTE:
STUFF CX FOR ES2

[PAGE_TITLE =AUDIO - COMBO JACK]

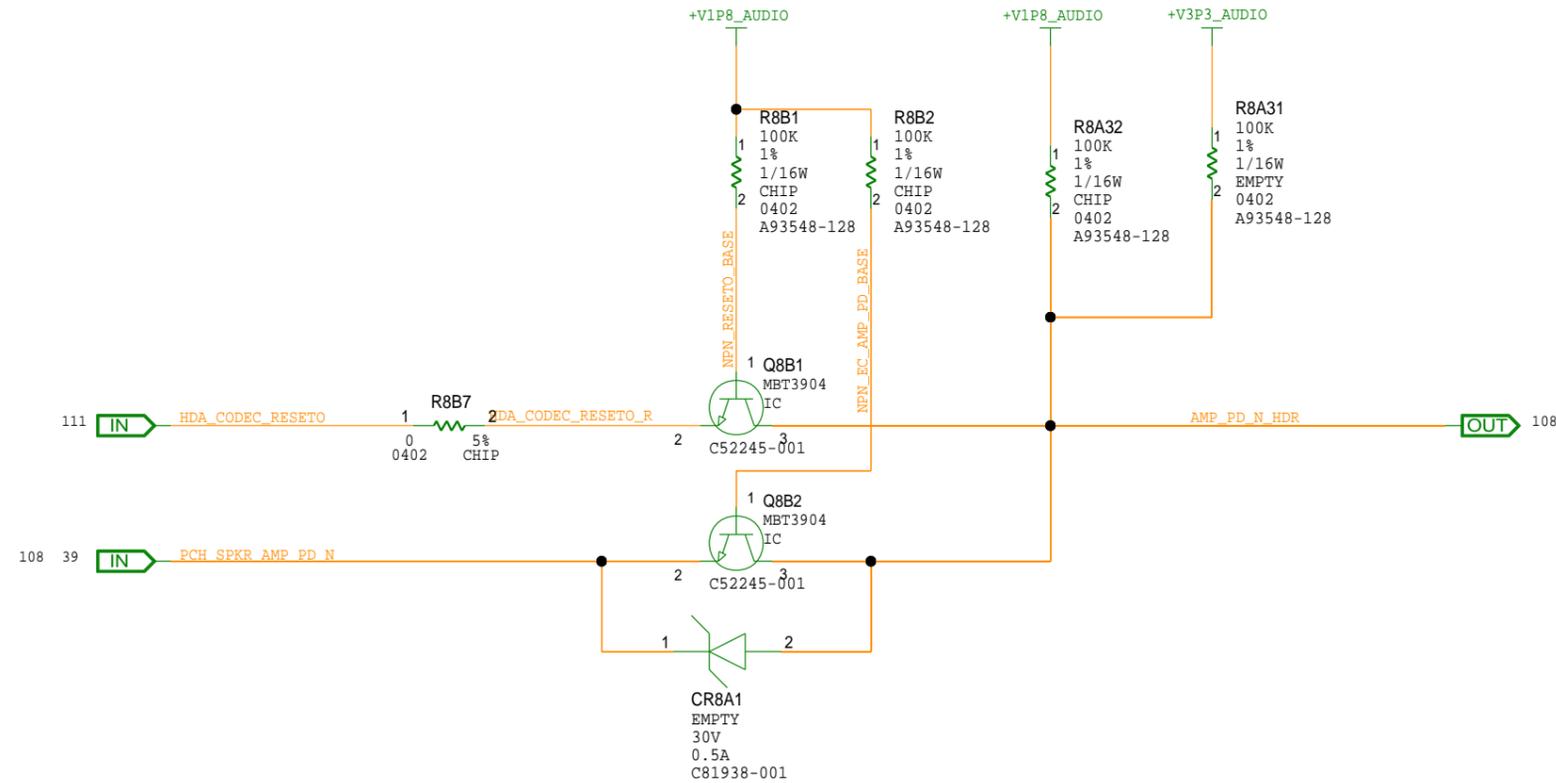
BPAGE DRAWING
udimm.sch_1.112
Fri Sep 27 16:40:57 2019

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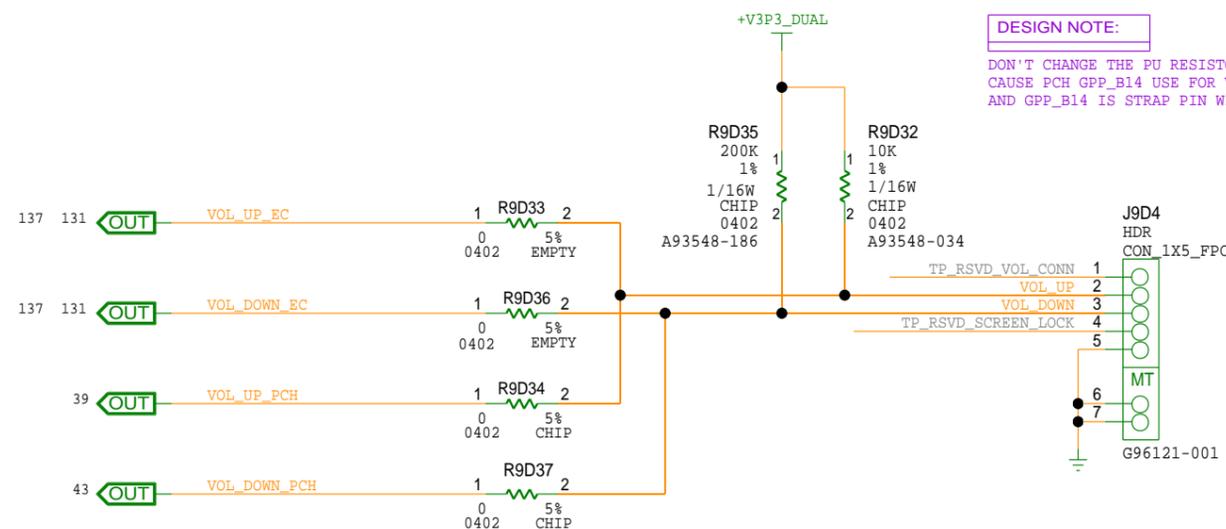
MODULE REV DETAILS

MODULE NAME	REV	DATE

AMP POWER DOWN CIRCUIT



VOLUME UP-DOWN HEADER



DESIGN NOTE:
 DON'T CHANGE THE PU RESISTOR VALUE OF VOL_DOWN
 CAUSE PCH GPP_B14 USE FOR VOL_DOWN_PCH
 AND GPP_B14 IS STRAP PIN WITH INTERNAL PD 20K

[PAGE_TITLE =AUDIO -AMP PD, VOL CONTROL]

BPAGE DRAWING

udimm.sch_1.113
 Fri Sep 27 16:40:58 2019

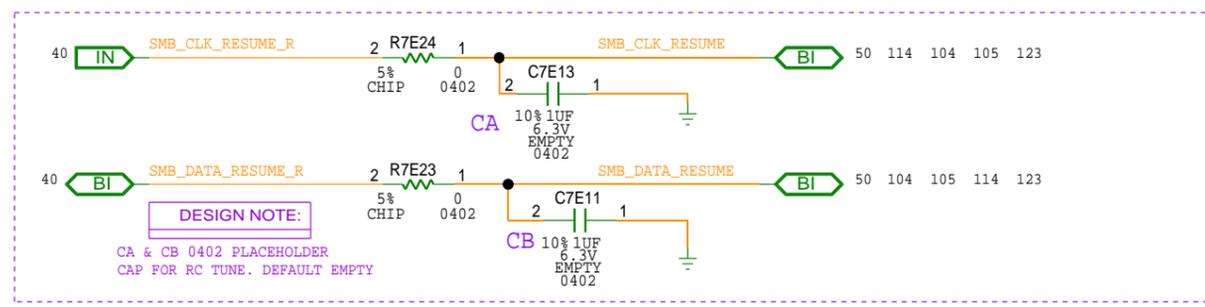
INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 113	REV 0.7
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PCH SMBUS

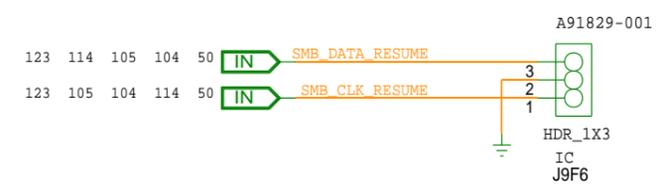
MODULE REV DETAILS

MODULE NAME	REV	DATE

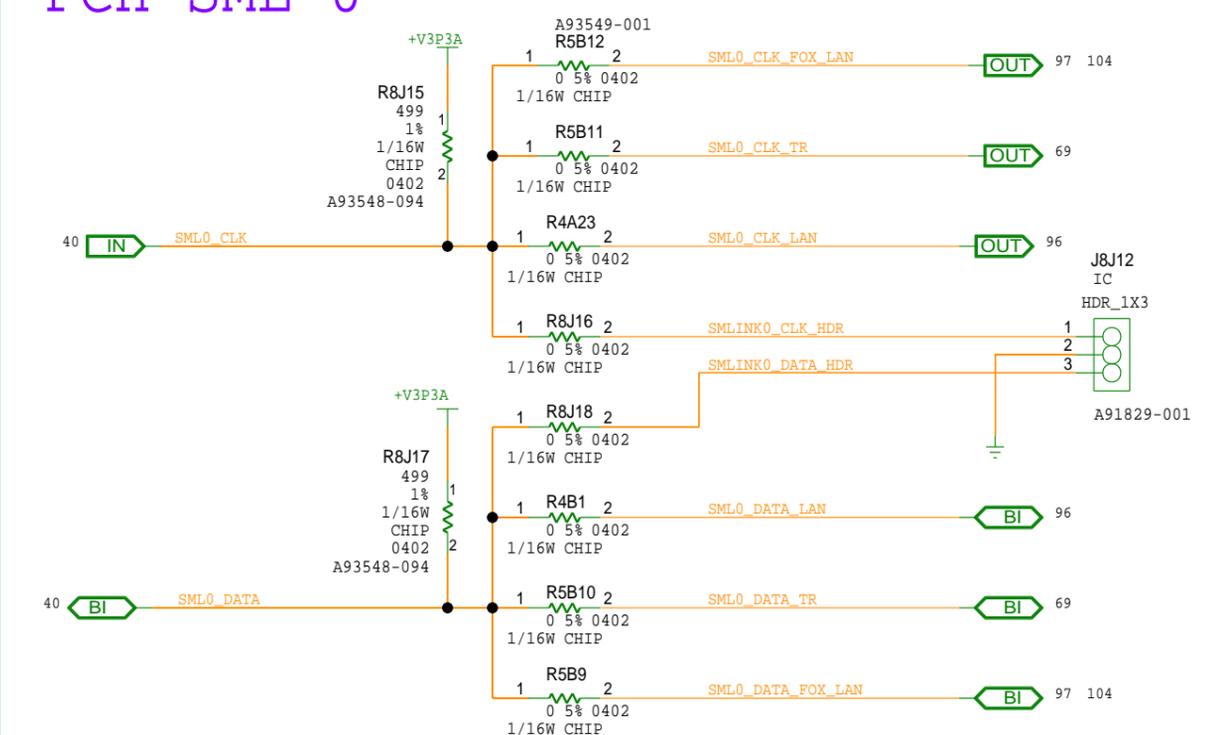
DESIGN NOTE:
SMB RESUME/MAIN LOGIC



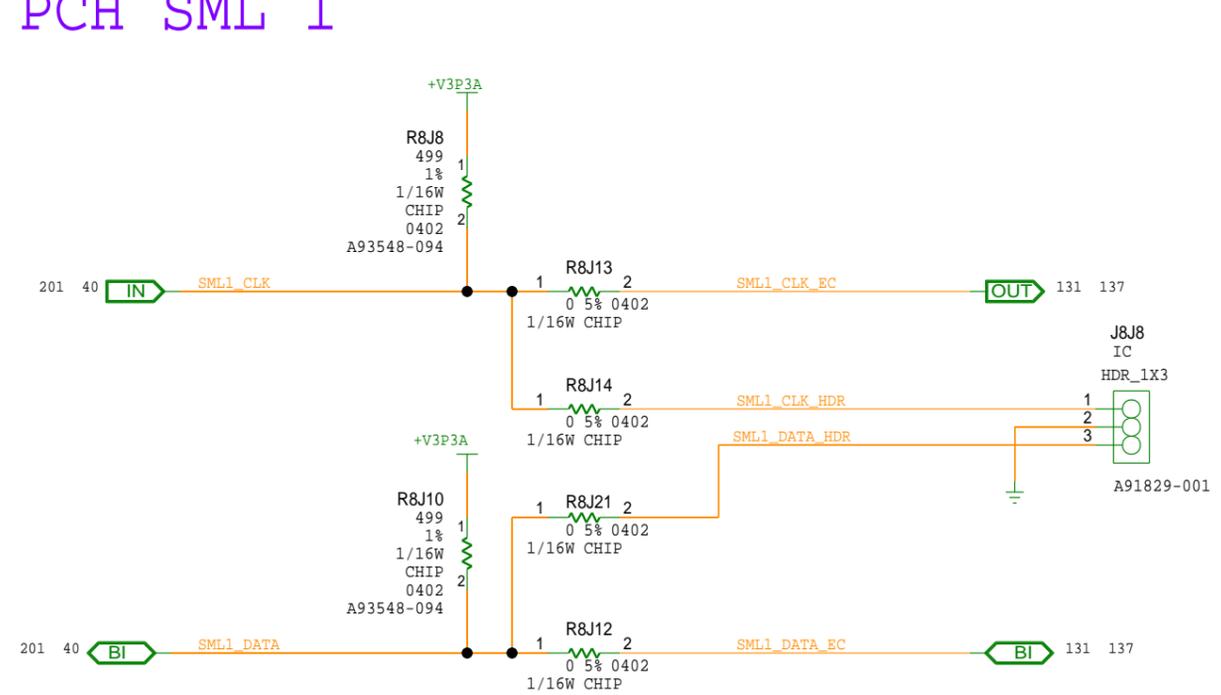
DESIGN NOTE:
CA & CB 0402 PLACEHOLDER
CAP FOR RC TUNE. DEFAULT EMPTY



PCH SML 0



PCH SML 1



[PAGE_TITLE=LPSS - SMBUS / SMLINK OPTIONS]

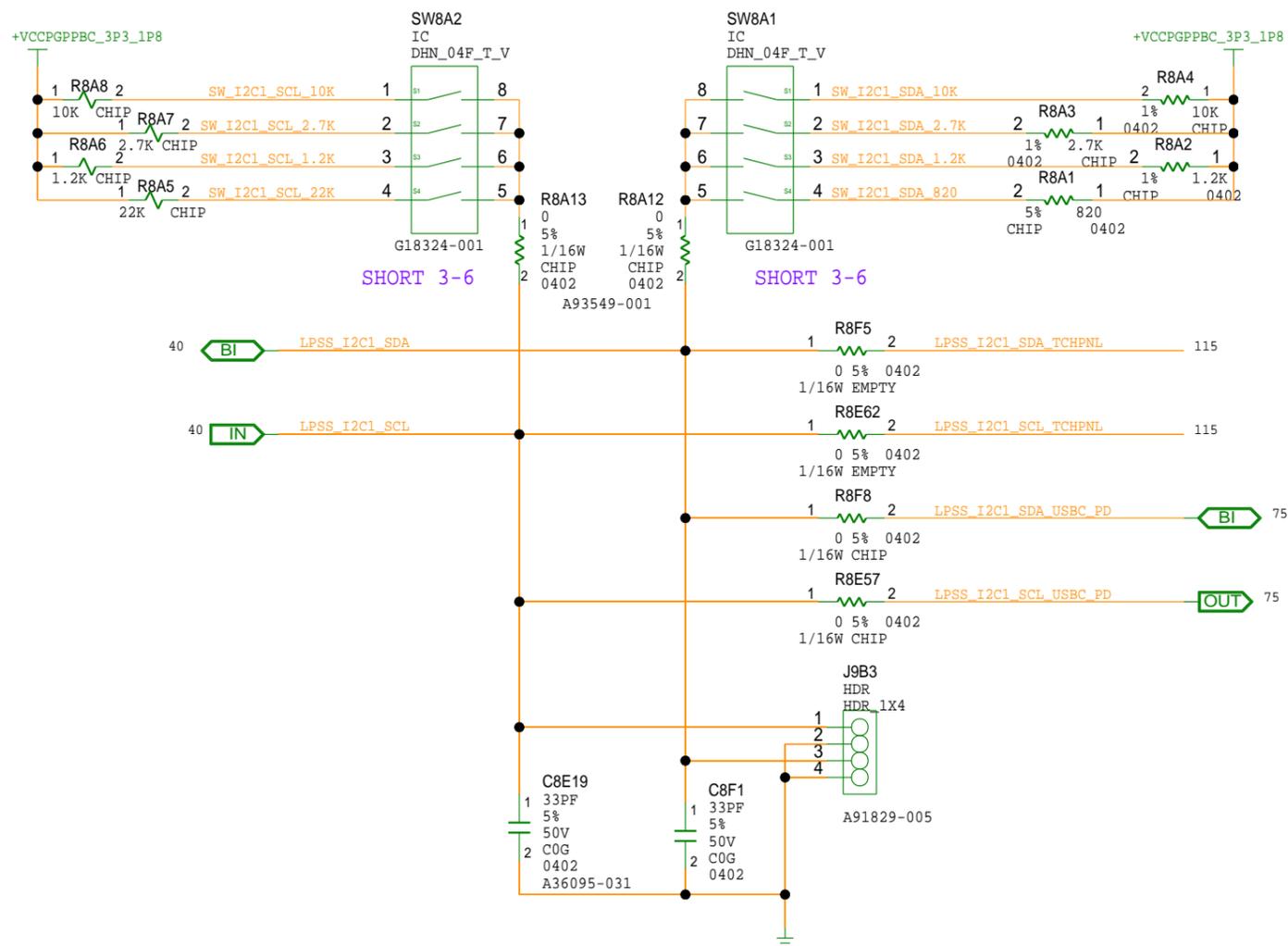
BPAGE DRAWING
udimm.sch_1.114
Fri Sep 27 16:41:00 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 114	REV 0.7
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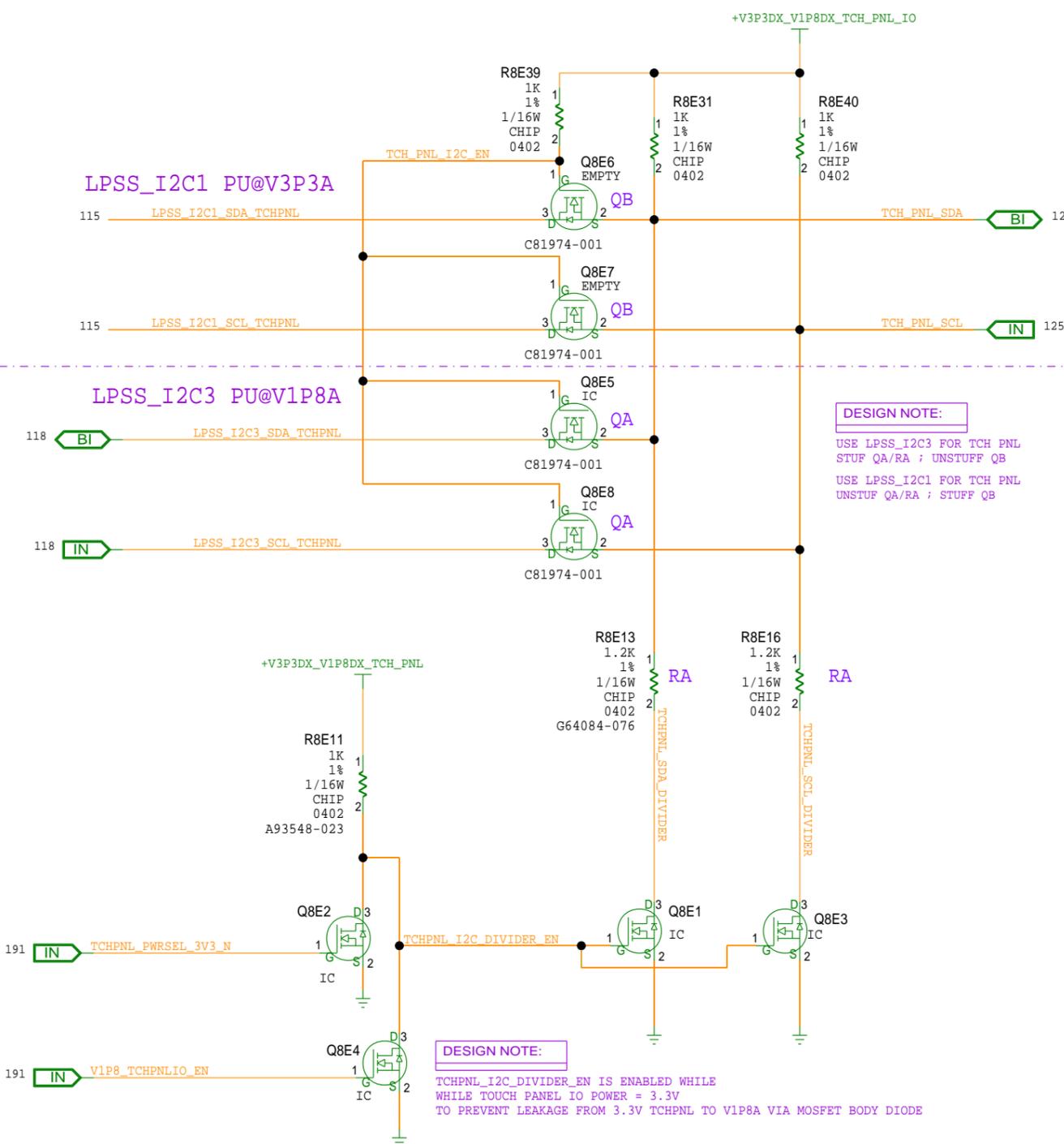
MODULE REV DETAILS

MODULE NAME	REV	DATE

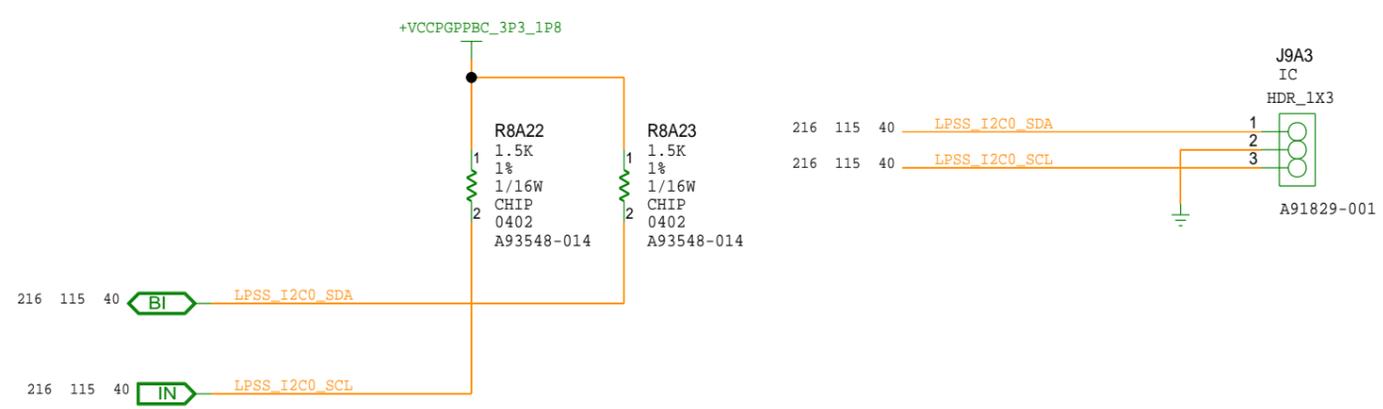
PCH LPSS I2C1



TOUCH PANEL I2C OPTIONS



PCH LPSS I2C0



[PAGE_TITLE =LPSS - I2C]

BPAGE DRAWING
udimm.sch_1.115
Fri Sep 27 16:41:01 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 115	REV 0.7
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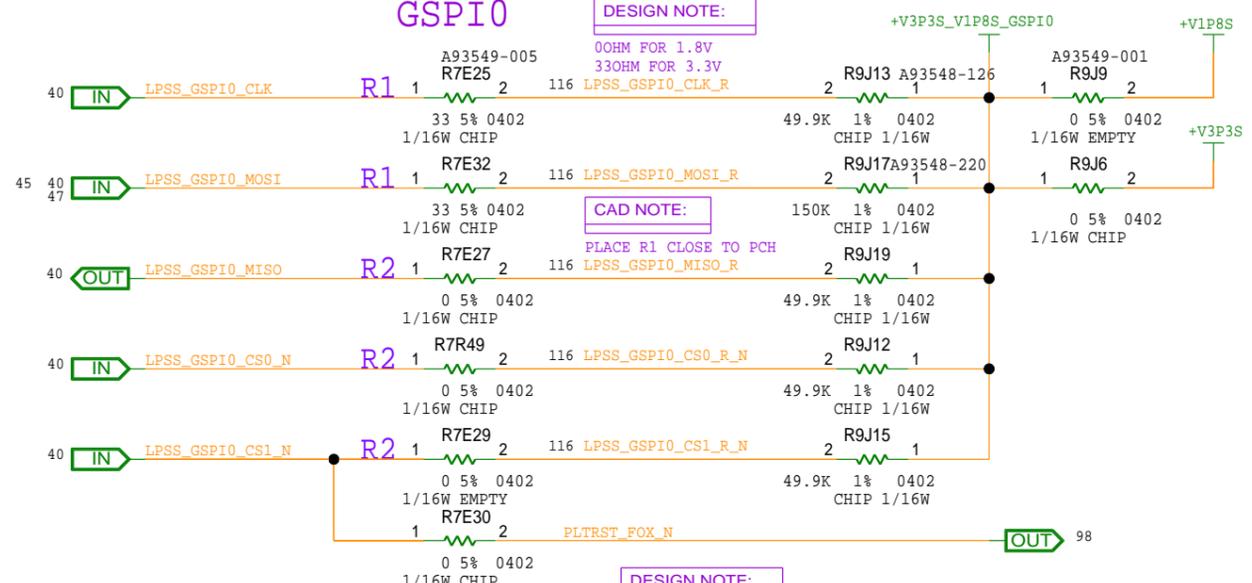
LPSS - GSPI0/1 UART0/1 HEADER

MODULE REV DETAILS

MODULE NAME	REV	DATE

GSPI0

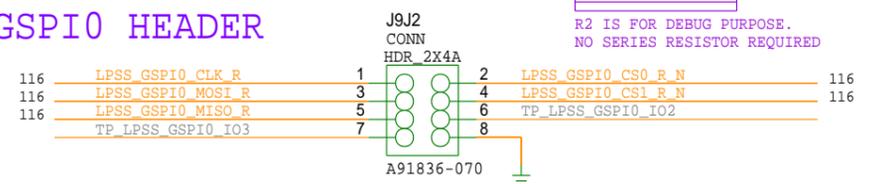
DESIGN NOTE:
00HM FOR 1.8V
330HM FOR 3.3V



CAD NOTE:
PLACE R1 CLOSE TO PCH
LPSS_GSPI0_MISO_R

DESIGN NOTE:
R2 IS FOR DEBUG PURPOSE.
NO SERIES RESISTOR REQUIRED

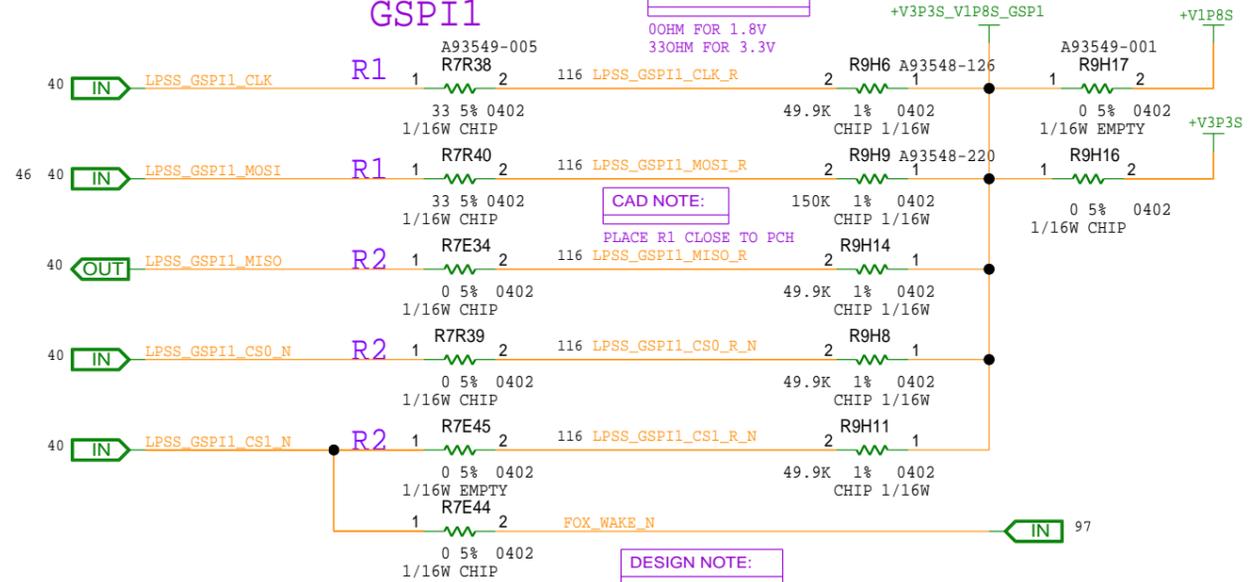
GSPI0 HEADER



CAD NOTE:
PLACE THE HEADER IN EV AREA

GSPI1

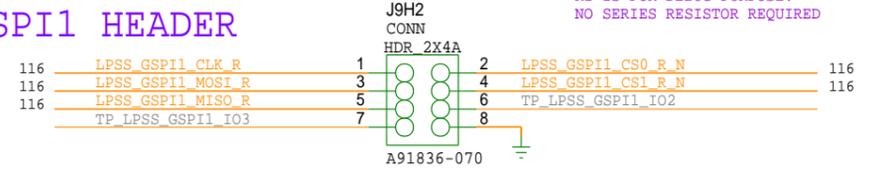
DESIGN NOTE:
00HM FOR 1.8V
330HM FOR 3.3V



CAD NOTE:
PLACE R1 CLOSE TO PCH
LPSS_GSPI1_MISO_R

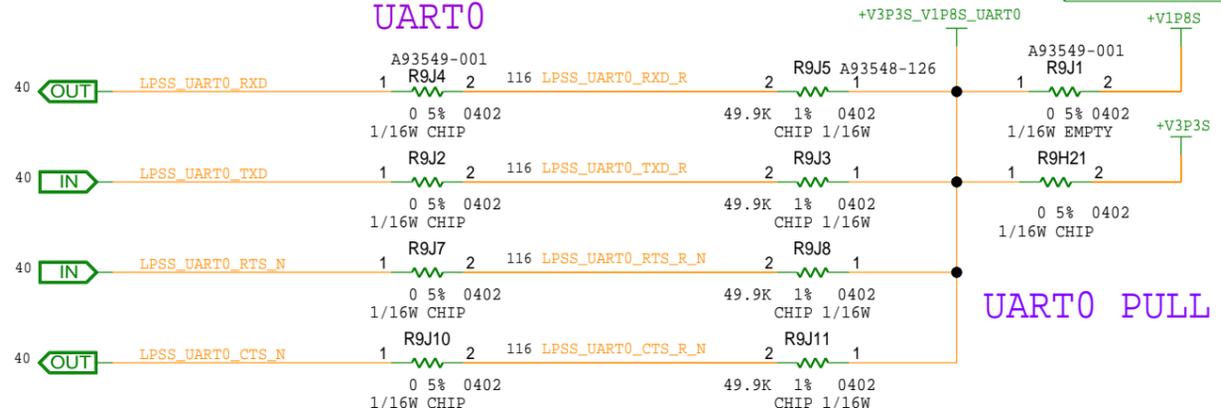
DESIGN NOTE:
R2 IS FOR DEBUG PURPOSE.
NO SERIES RESISTOR REQUIRED

GSPI1 HEADER



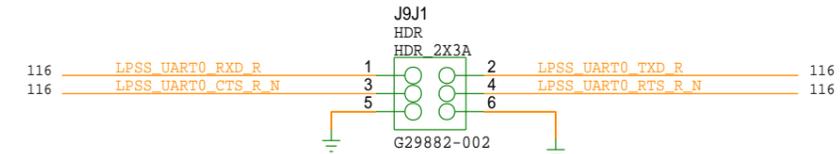
CAD NOTE:
PLACE THE HEADER IN EV AREA

UART0

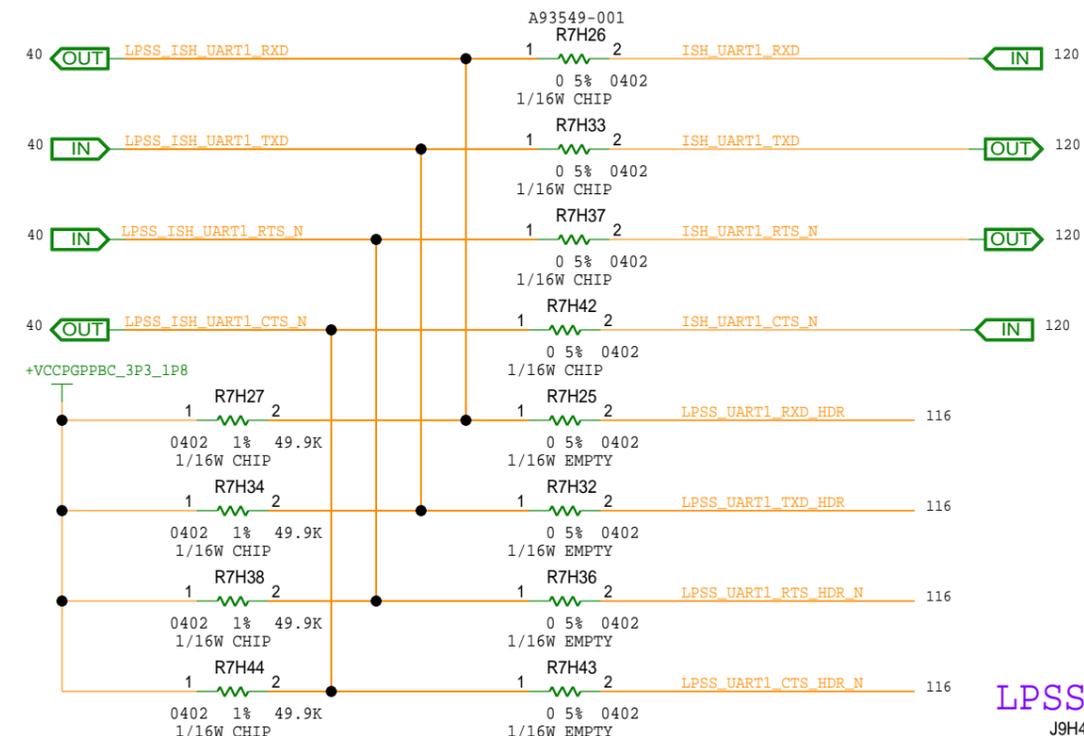


UART0 PULL UP

UART0 HEADER

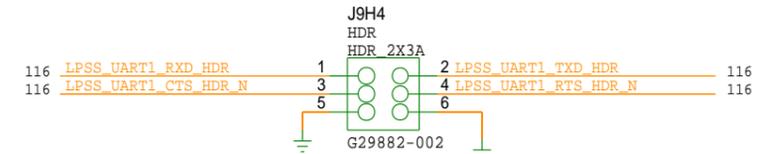


LPSS/ISH UART1 SELECTION



UART1 PULL UP

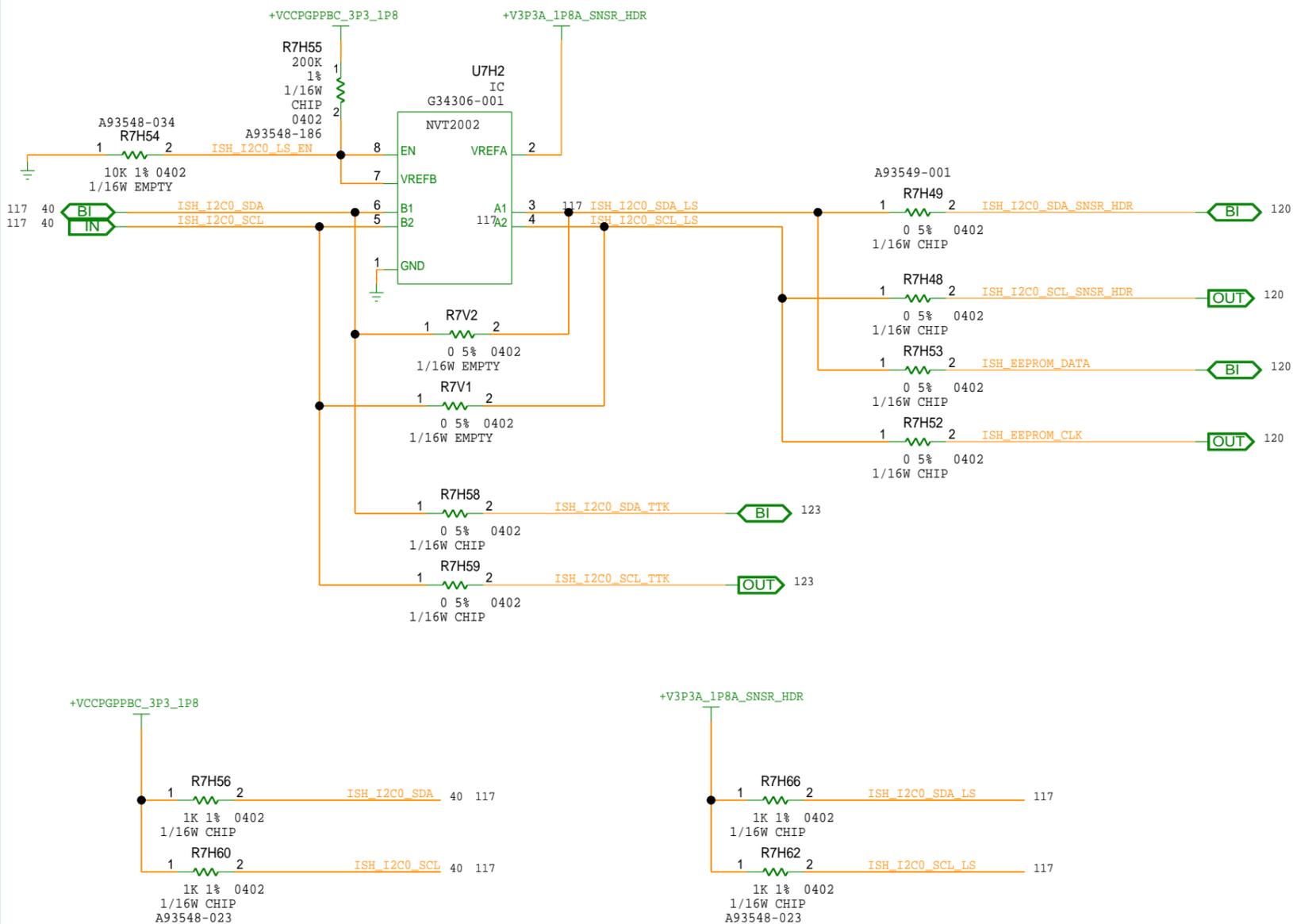
LPSS UART1 HEADER



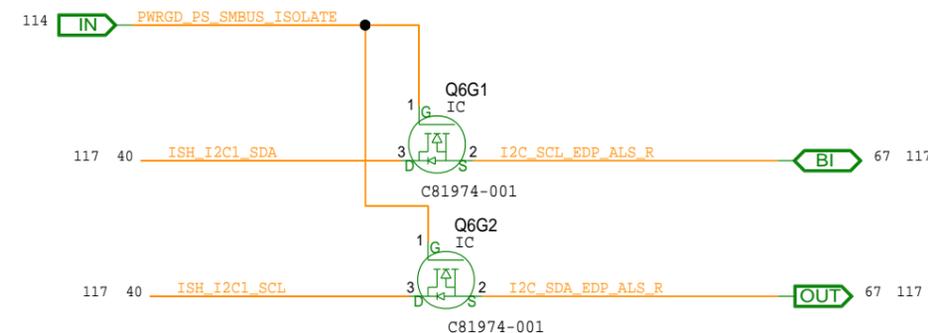
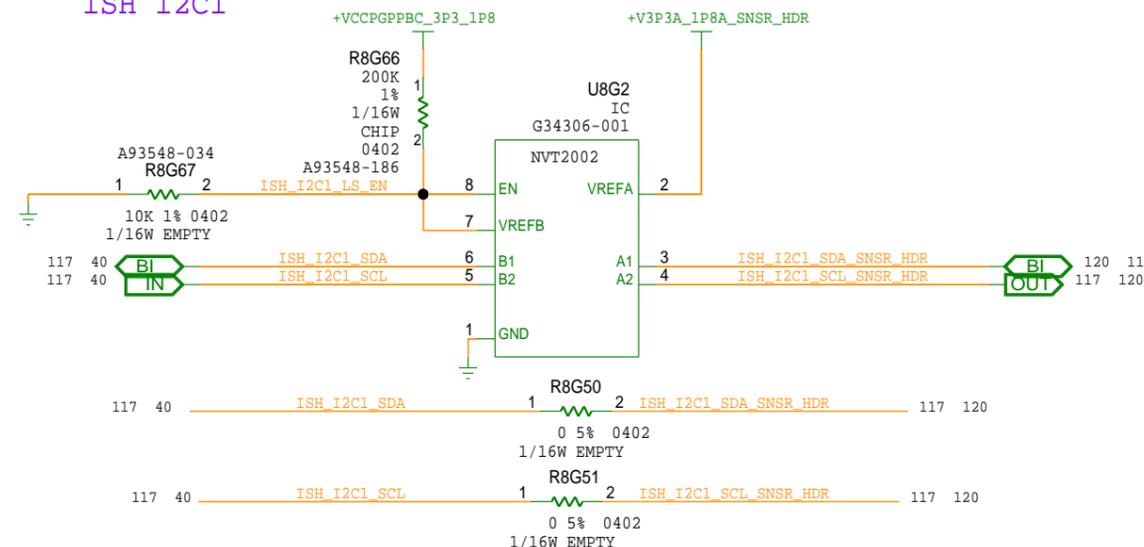
MODULE REV DETAILS

MODULE NAME	REV	DATE

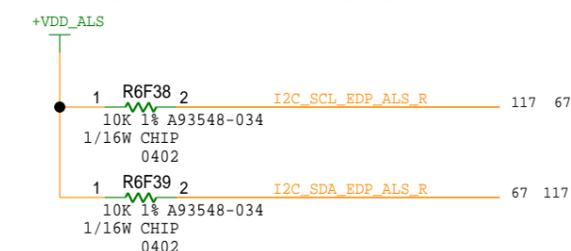
ISH I2C SELECTION
ISH I2C0



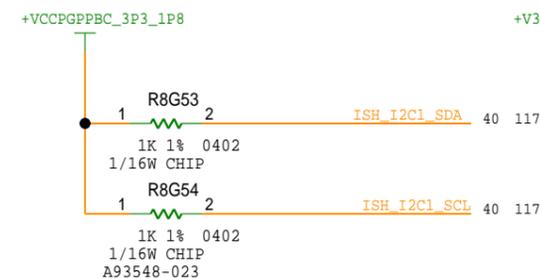
ISH I2C1



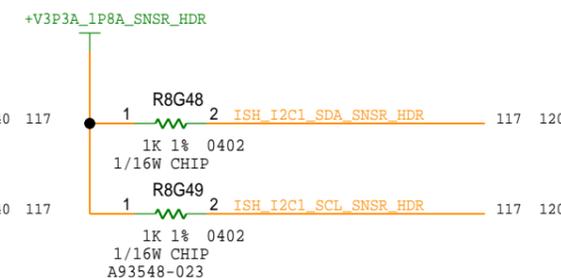
ISH I2C1 PU@ALS SIDE



ISH I2C1 PU



ISH I2C1 PU@SENSOR HEADER SIDE



[PAGE_TITLE=BLANK]

BPAGE DRAWING

udimm.sch_1.117
Fri Sep 27 16:41:04 2019

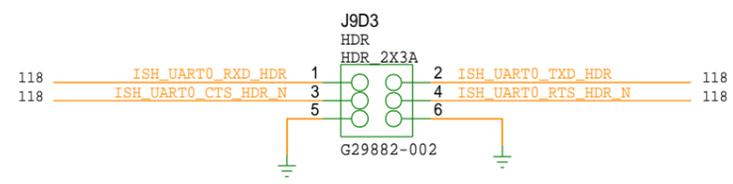
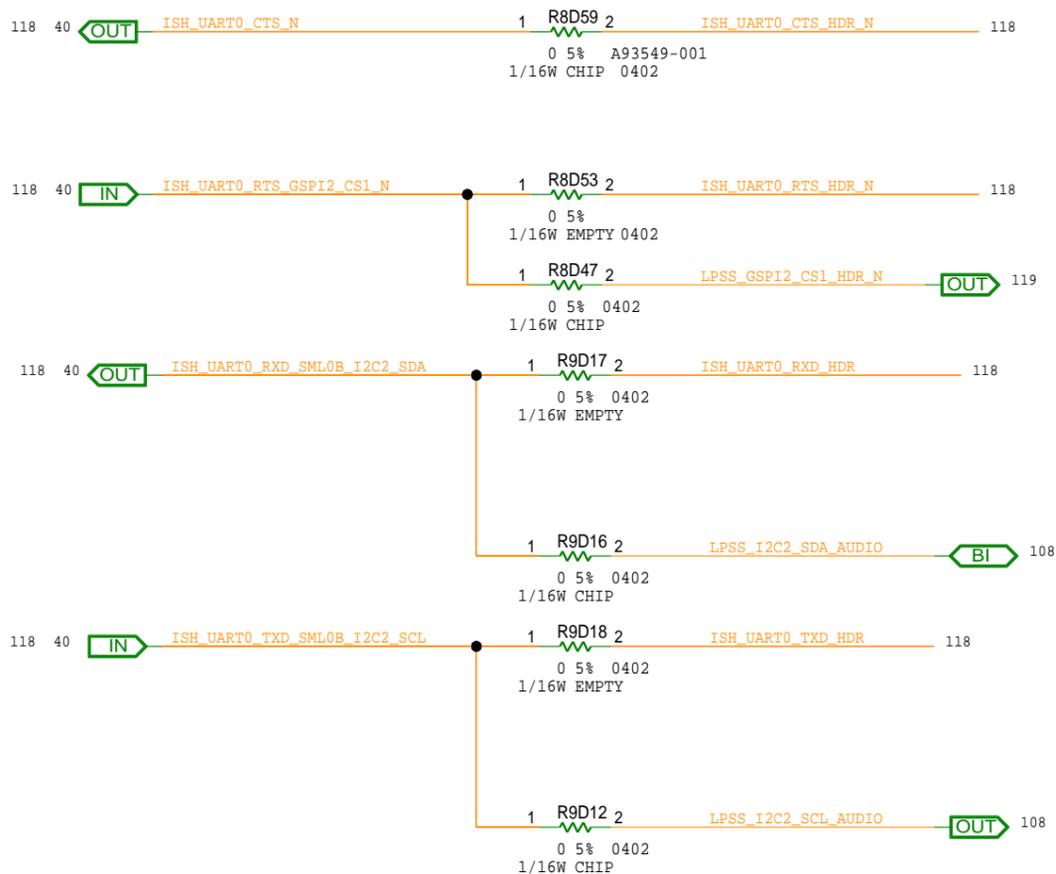
INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 117	REV 0.7
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MODULE REV DETAILS

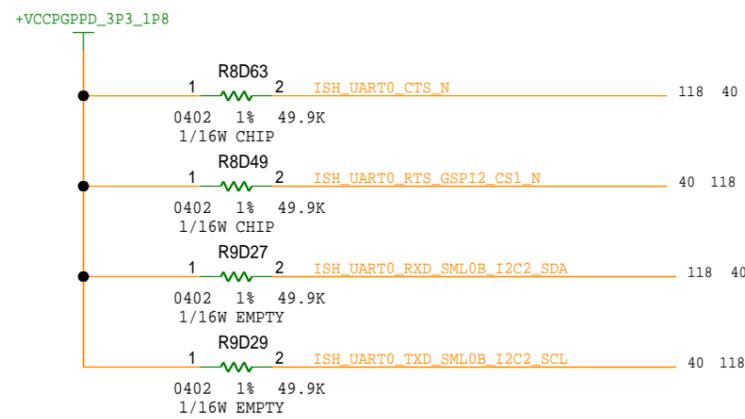
MODULE NAME	REV	DATE

ISH UART0 SELECTION

ISH UART0 HEADER



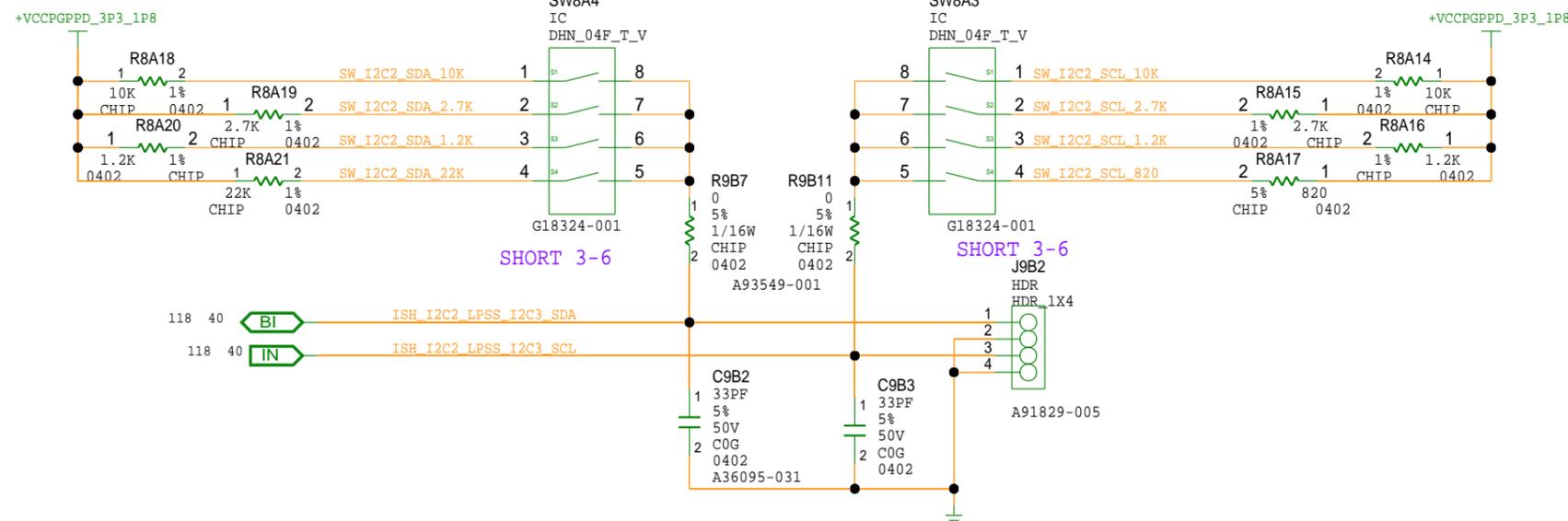
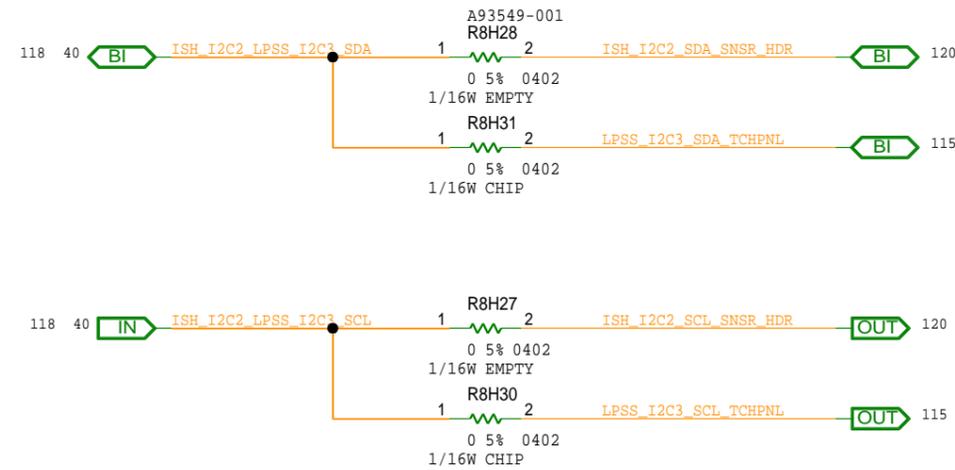
ISH UART0/SML0B/LPSS I2C PU



DESIGN NOTE:
49.9K PU FOR UART

ISH I2C2

ISH I2C2 PU



SHORT 3-6

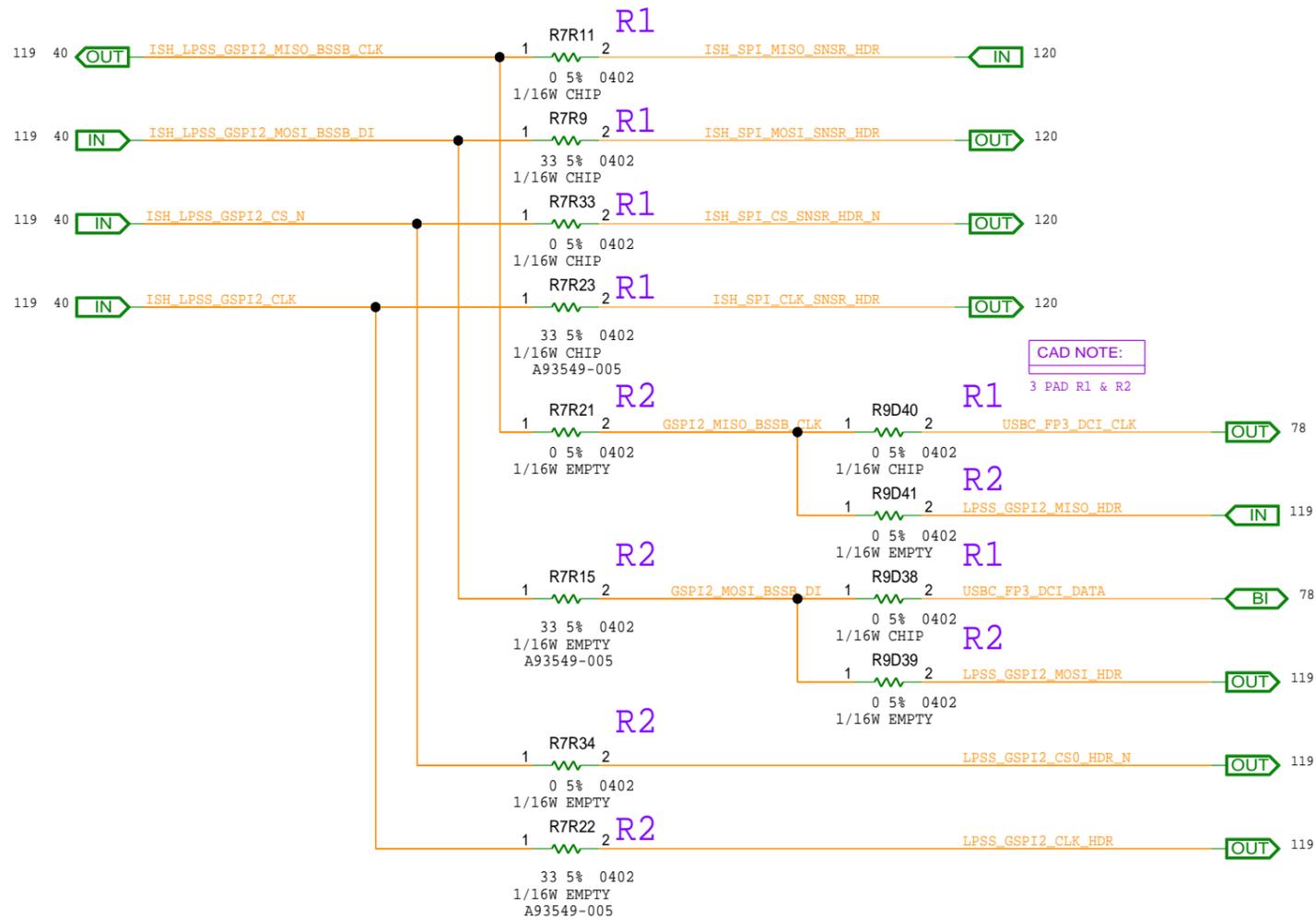
SHORT 3-6

ISH - ISH_SPI / GPIO OPTIONS

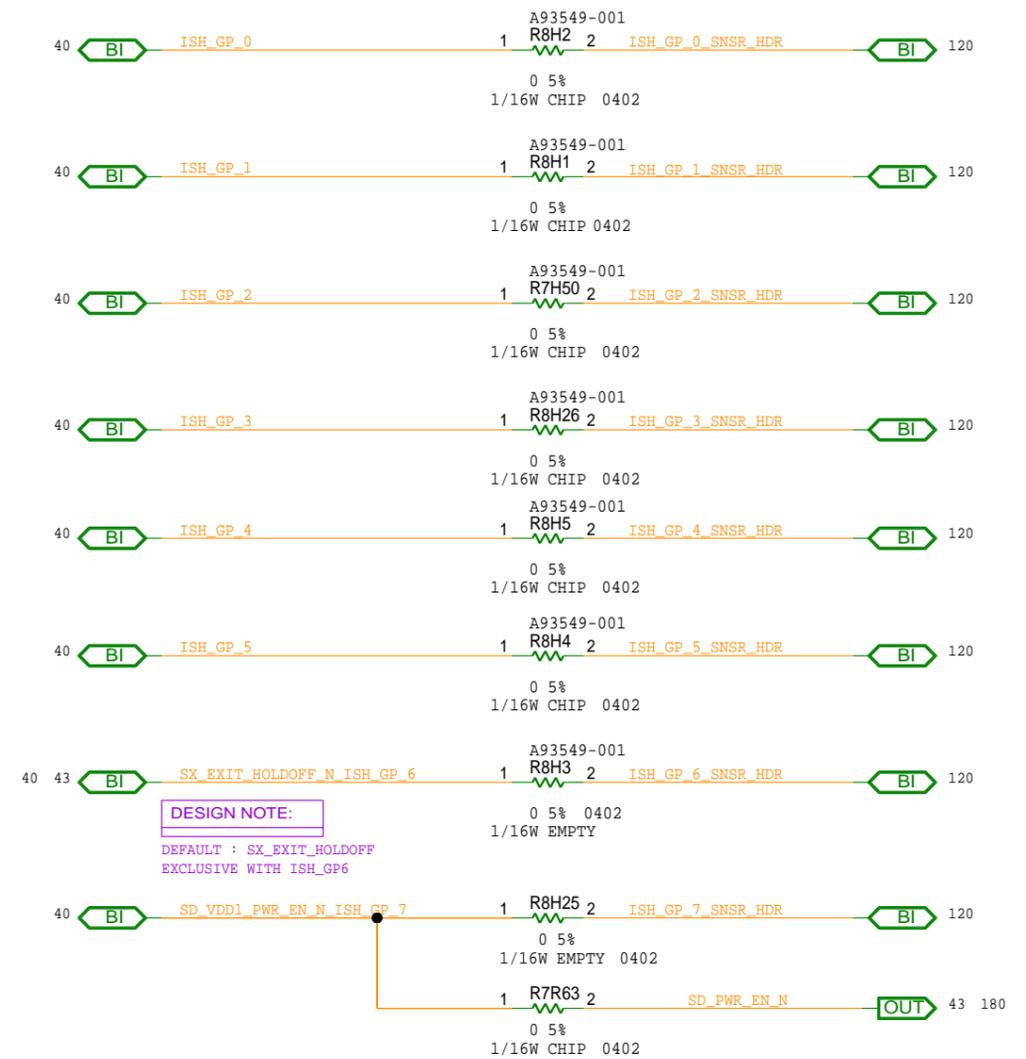
MODULE REV DETAILS

MODULE NAME	REV	DATE

ISH SPI/LPSS GSPI2 SELECTION

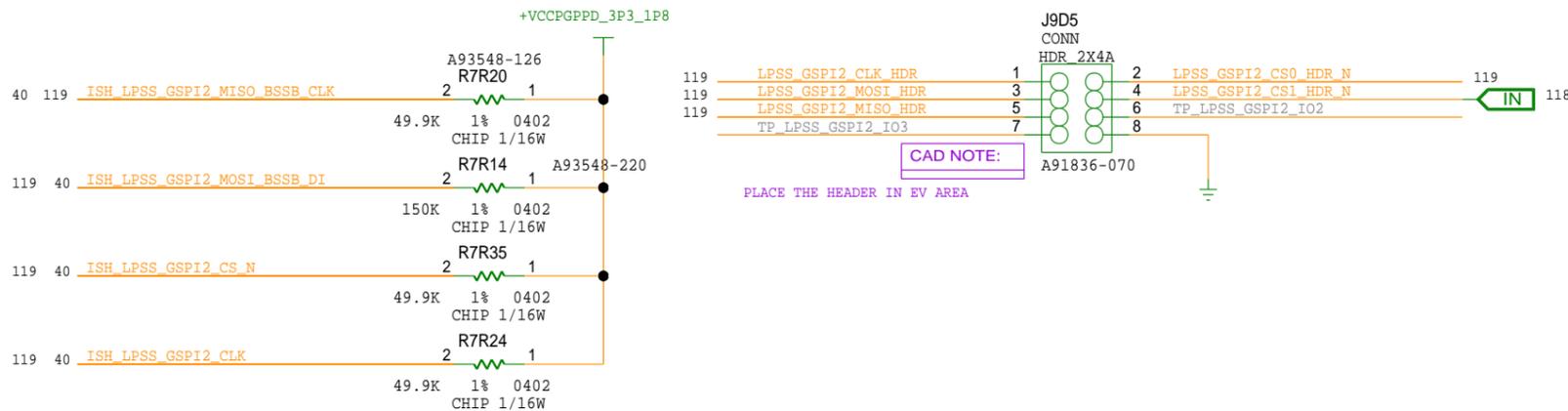


ISH GPP SELECTION



ISH LPSS GSPI PULL-UP

GSPI2 HEADER



[PAGE_TITLE=ISH - ISH_SPI / UART0 / I2C0/1/2 SELECTION]

BPAGE DRAWING

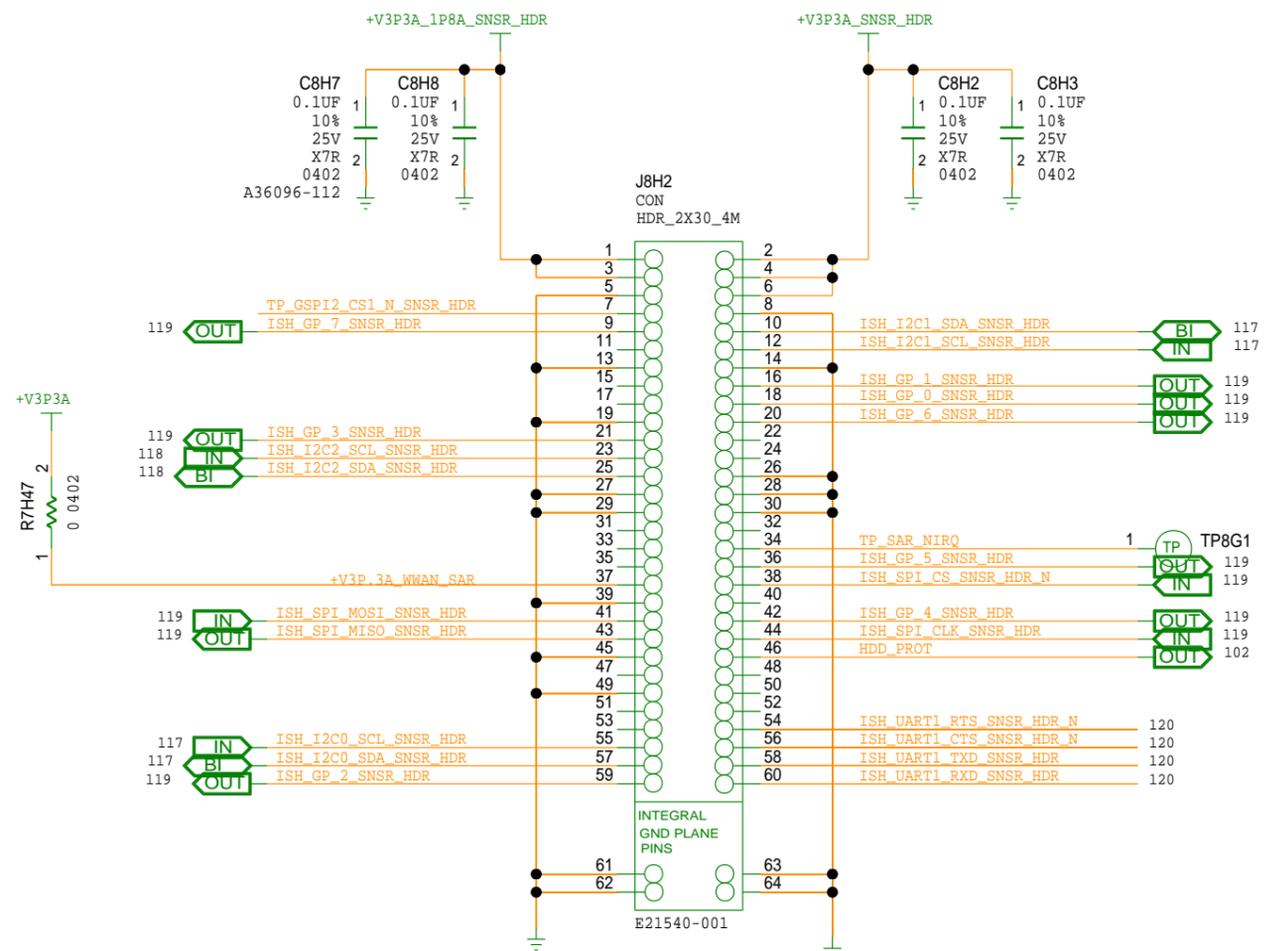
udimm.sch_1.119
Fri Sep 27 16:41:06 2019

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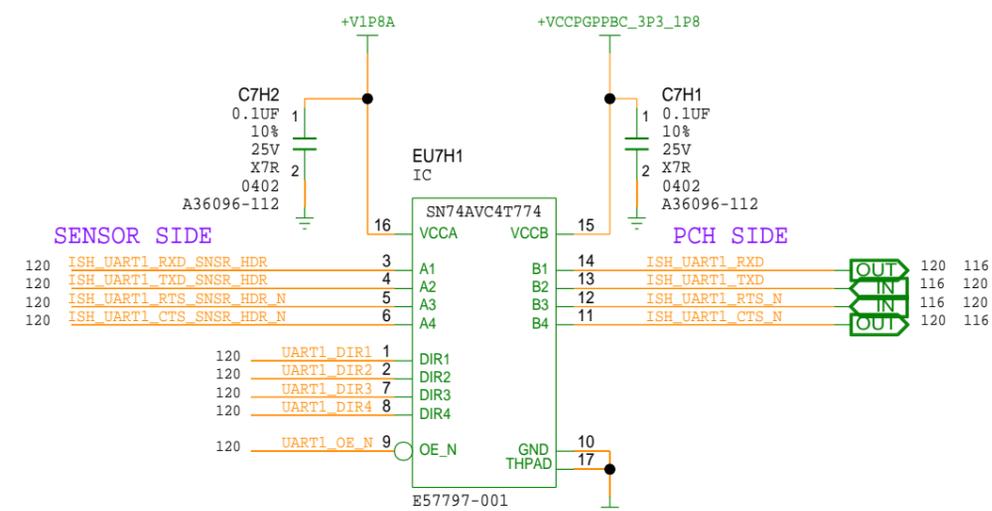
MODULE REV DETAILS

MODULE NAME	REV	DATE

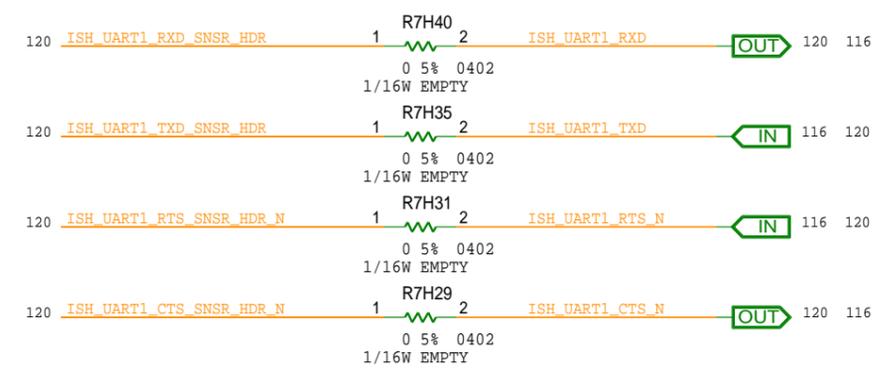
ISH AIC HEADER(MOSAIC)



ISH UART1 LEVEL SHIFTER

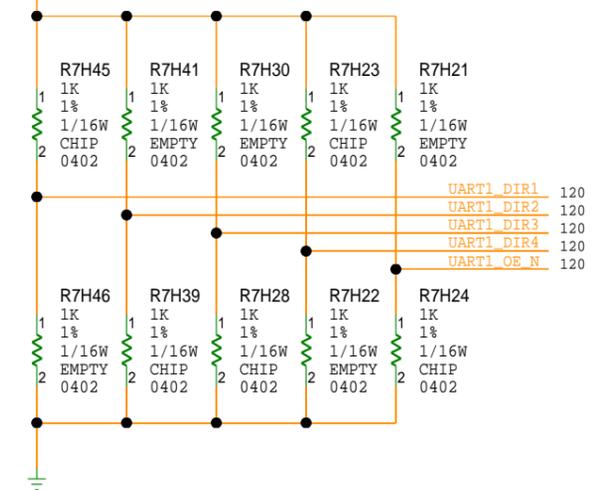


BYPASS LEVEL SHIFTER OPTIONS



DESIGN NOTE:
DIR PIN WHILE OE = L
H = A TO B
L = B TO A

CAD NOTE:
3 PAD



BPAGE DRAWING

udimm.sch_1.120
Fri Sep 27 16:41:07 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 120	REV 0.7
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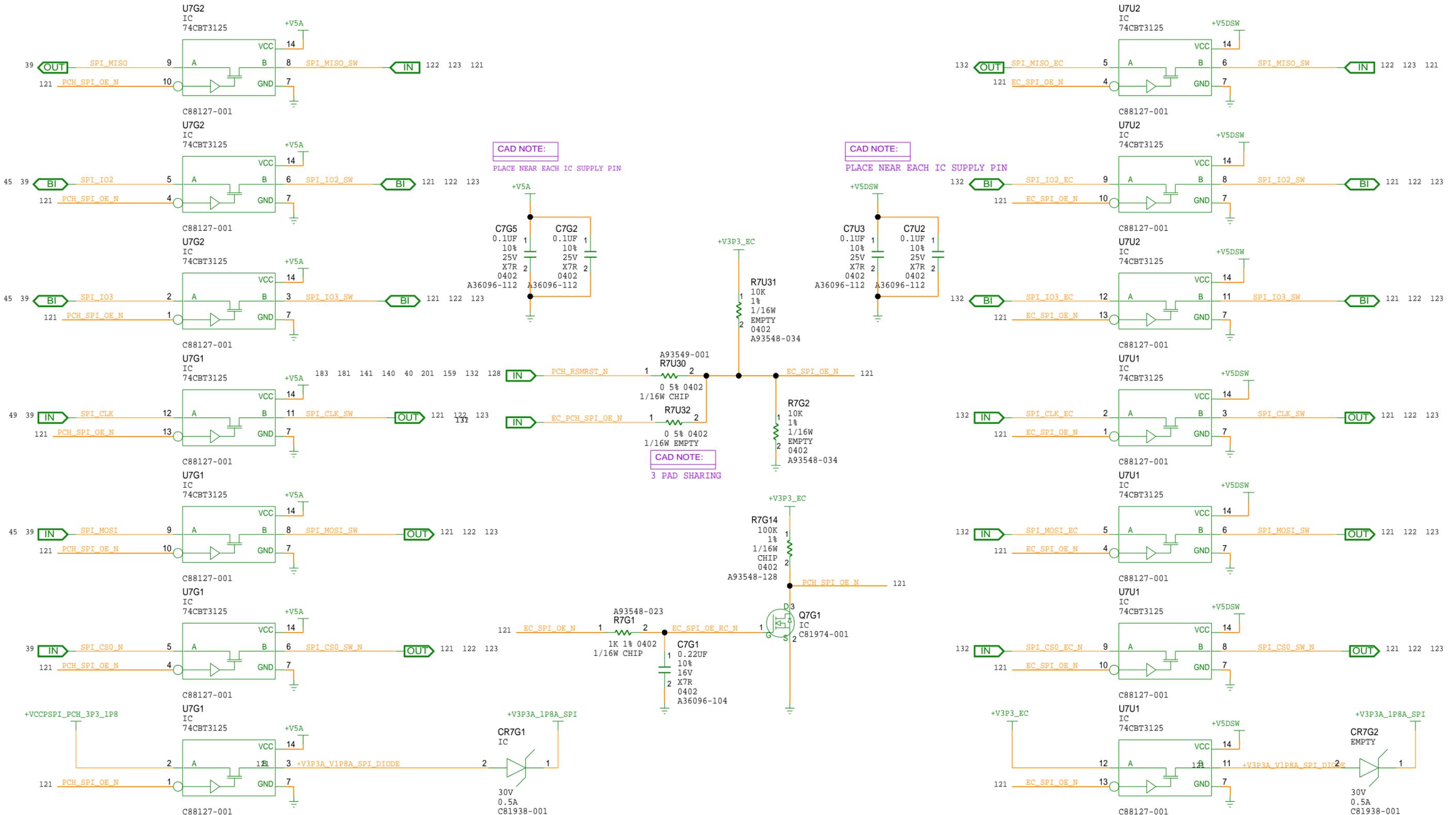
[PAGE_TITLE=ISH - SENSOR HEADER]

PCH SPI G3 FLASH PROGRAMMING ISOLATION CIRCUIT

PCH-EC FLASH SHARING WITH WIRED-OR TOPOLOGY

MODULE REV DETAILS

MODULE NAME	REV	DATE



CAD NOTE:
PLACE NEAR EACH IC SUPPLY PIN

CAD NOTE:
PLACE NEAR EACH IC SUPPLY PIN

CAD NOTE:
3 PAD SHARING

[PAGE_TITLE=SPI - FLASH MUX CIRCUIT]

BPAGE DRAWING

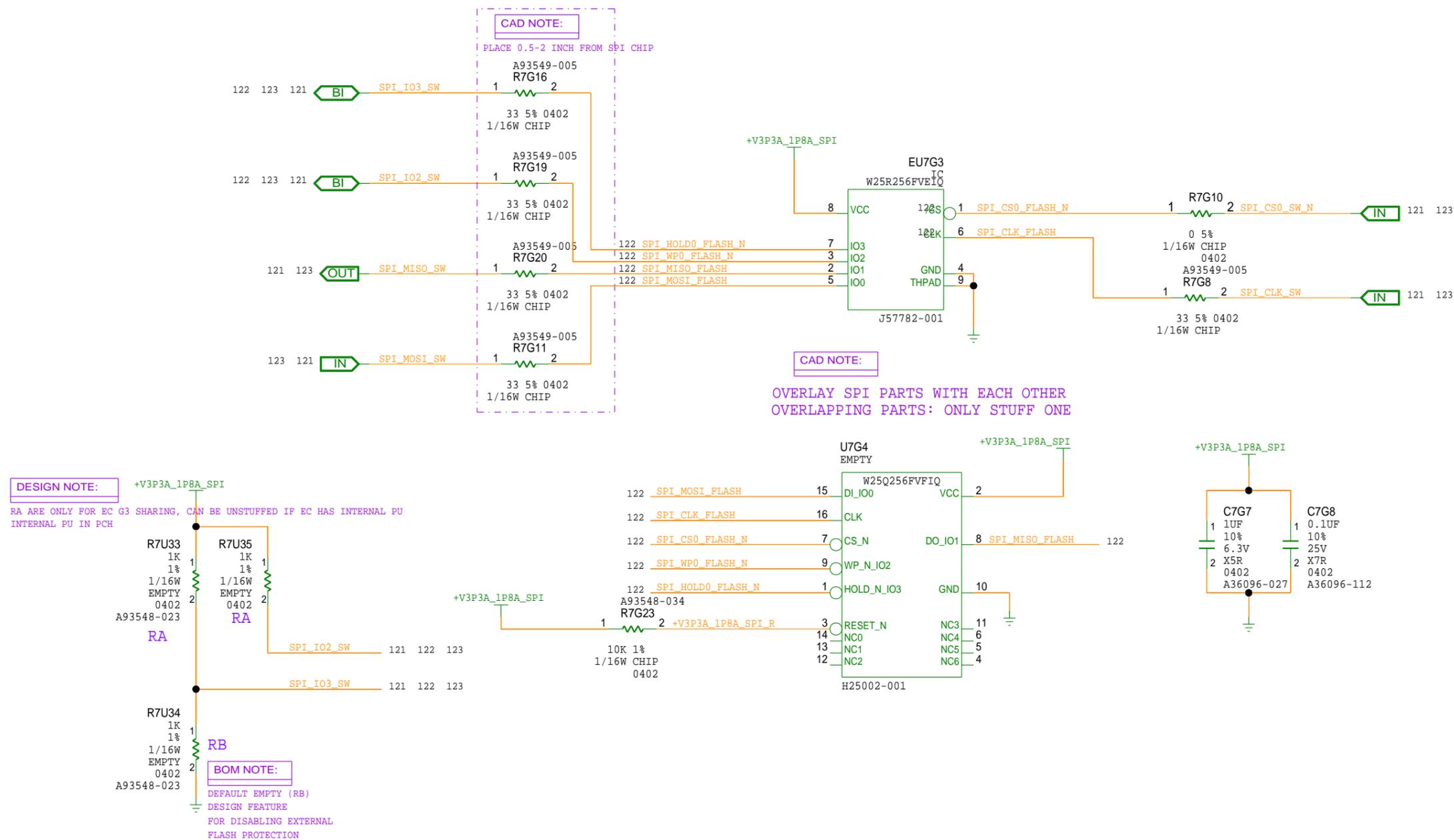
udimm.sch_1.121
Fri Sep 27 16:41:08 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 121	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE

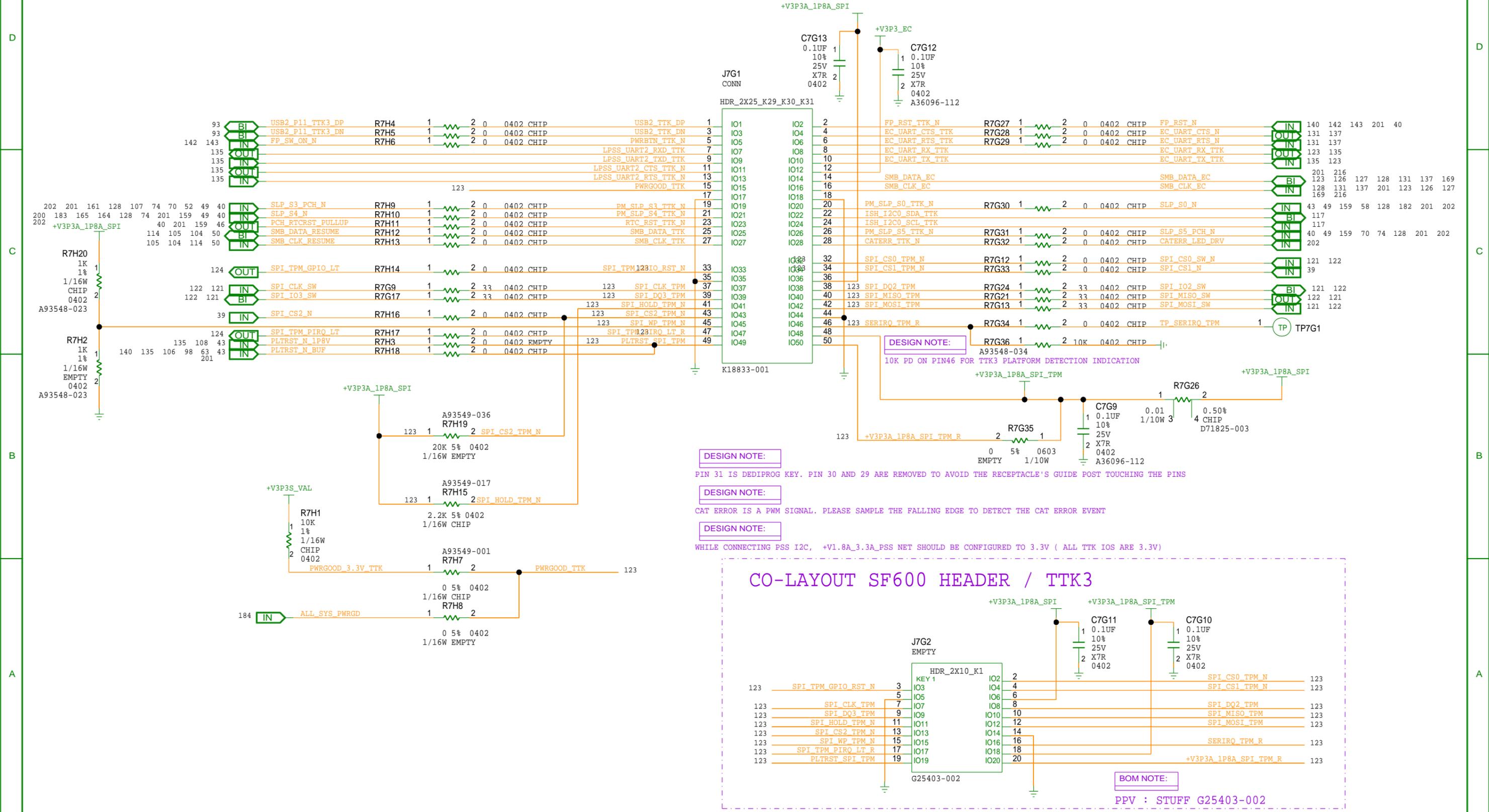
PRIMARY SERIAL FLASH



TTK3 UNIFIED HEADER

MODULE REV DETAILS

MODULE NAME	REV	DATE



DESIGN NOTE:

PIN 31 IS DEDIPROG KEY. PIN 30 AND 29 ARE REMOVED TO AVOID THE RECEPTACLE'S GUIDE POST TOUCHING THE PINS

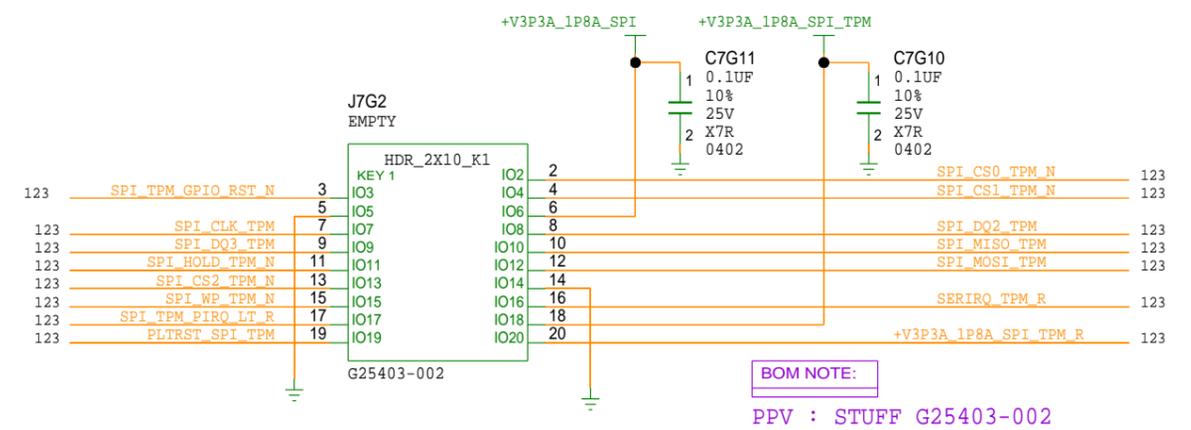
DESIGN NOTE:

CAT ERROR IS A PWM SIGNAL. PLEASE SAMPLE THE FALLING EDGE TO DETECT THE CAT ERROR EVENT

DESIGN NOTE:

WHILE CONNECTING PSS I2C, +V1.8A_3.3A_PSS NET SHOULD BE CONFIGURED TO 3.3V (ALL TTK IOS ARE 3.3V)

CO-LAYOUT SF600 HEADER / TTK3



BOM NOTE:

PPV : STUFF G25403-002

[PAGE_TITLE= SPI - TTK3/SF600/TPM HEADER]

BPAGE DRAWING

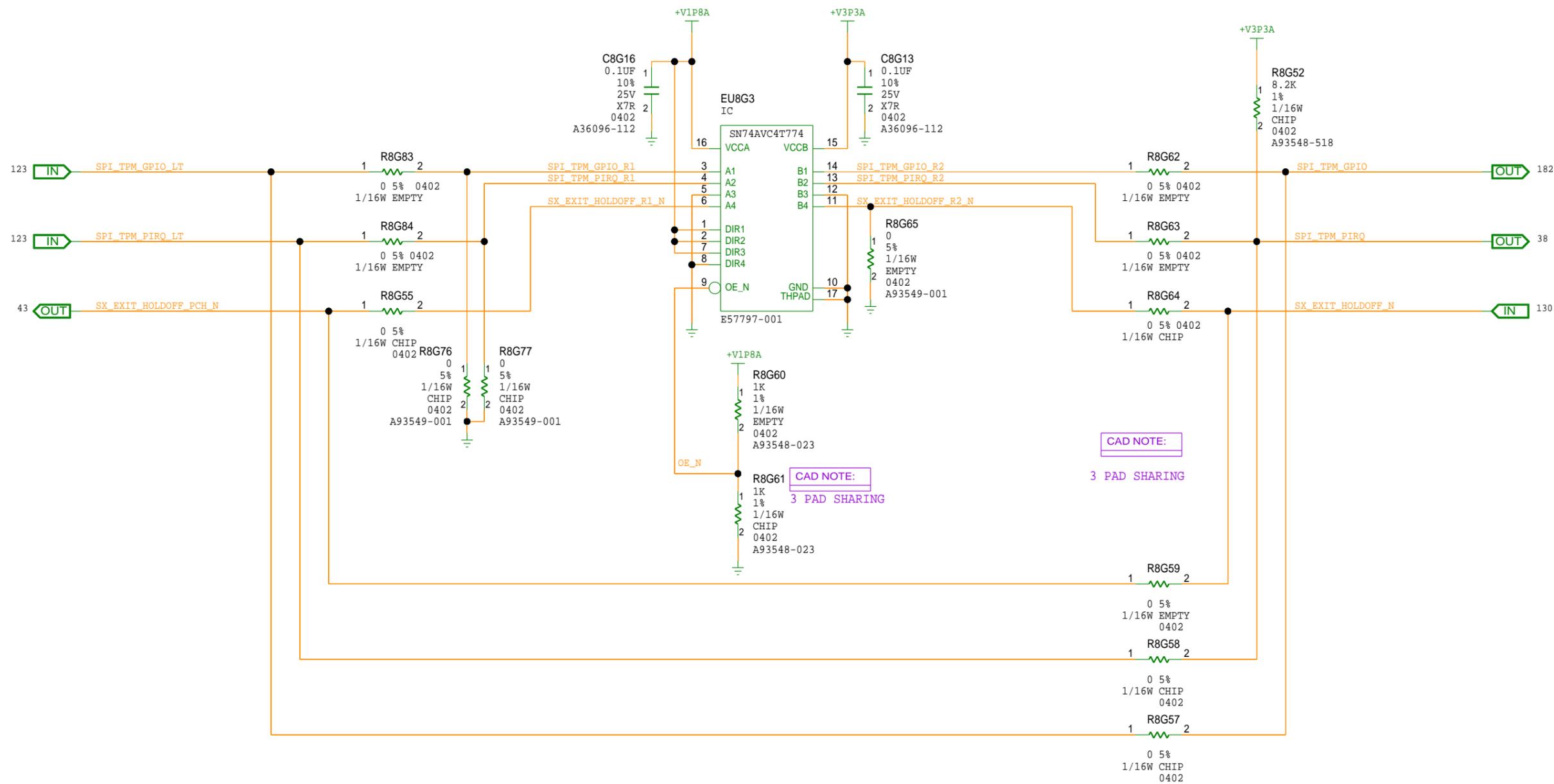
udimm.sch_1.123
Fri Sep 27 16:41:10 2019

INTEL
CONFIDENTIAL

DOCUMENT_NUMBER	PAGE	REV
xxxxxxx	123	0.7

MODULE REV DETAILS

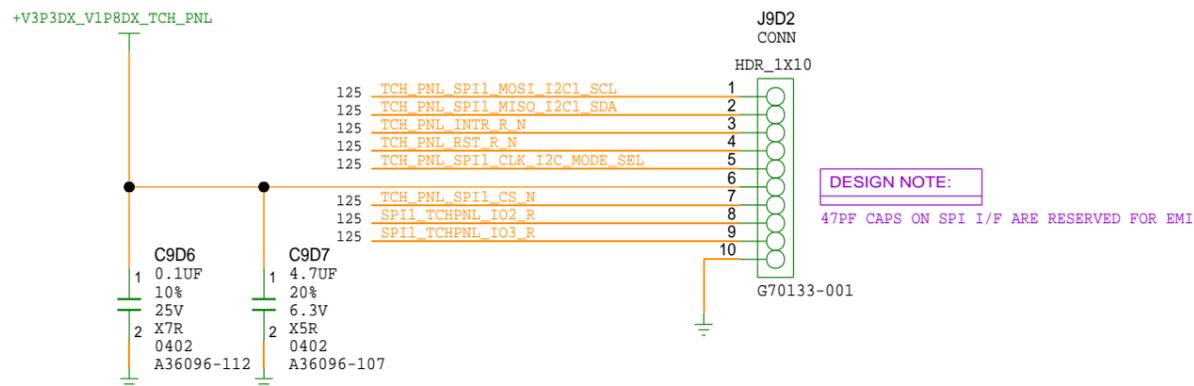
MODULE NAME	REV	DATE



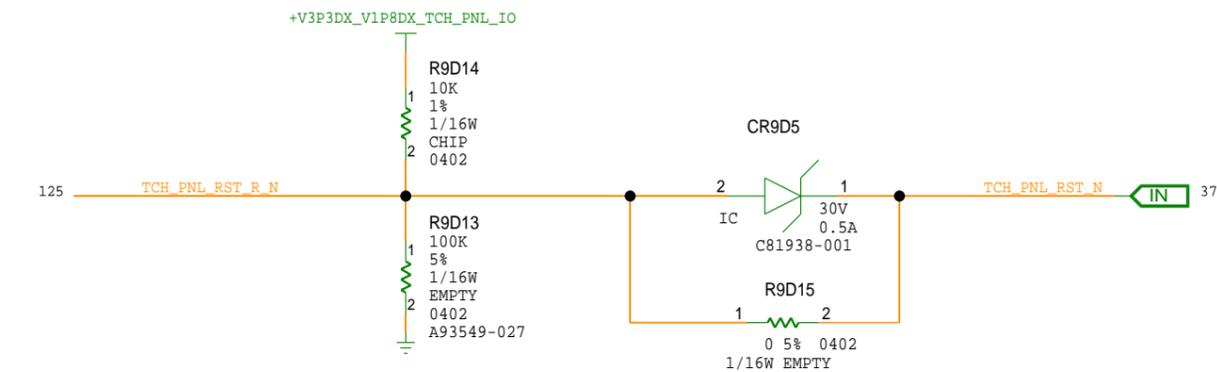
CAD NOTE:
3 PAD SHARING

CAD NOTE:
3 PAD SHARING

I2C/SPI TOUCH PANEL CONNECTOR

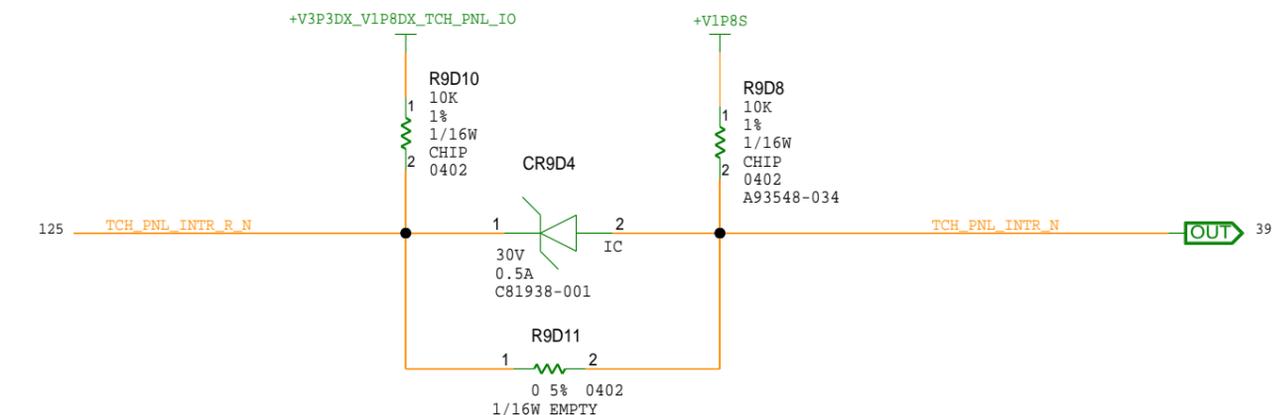


I2C TOUCH PANEL RST

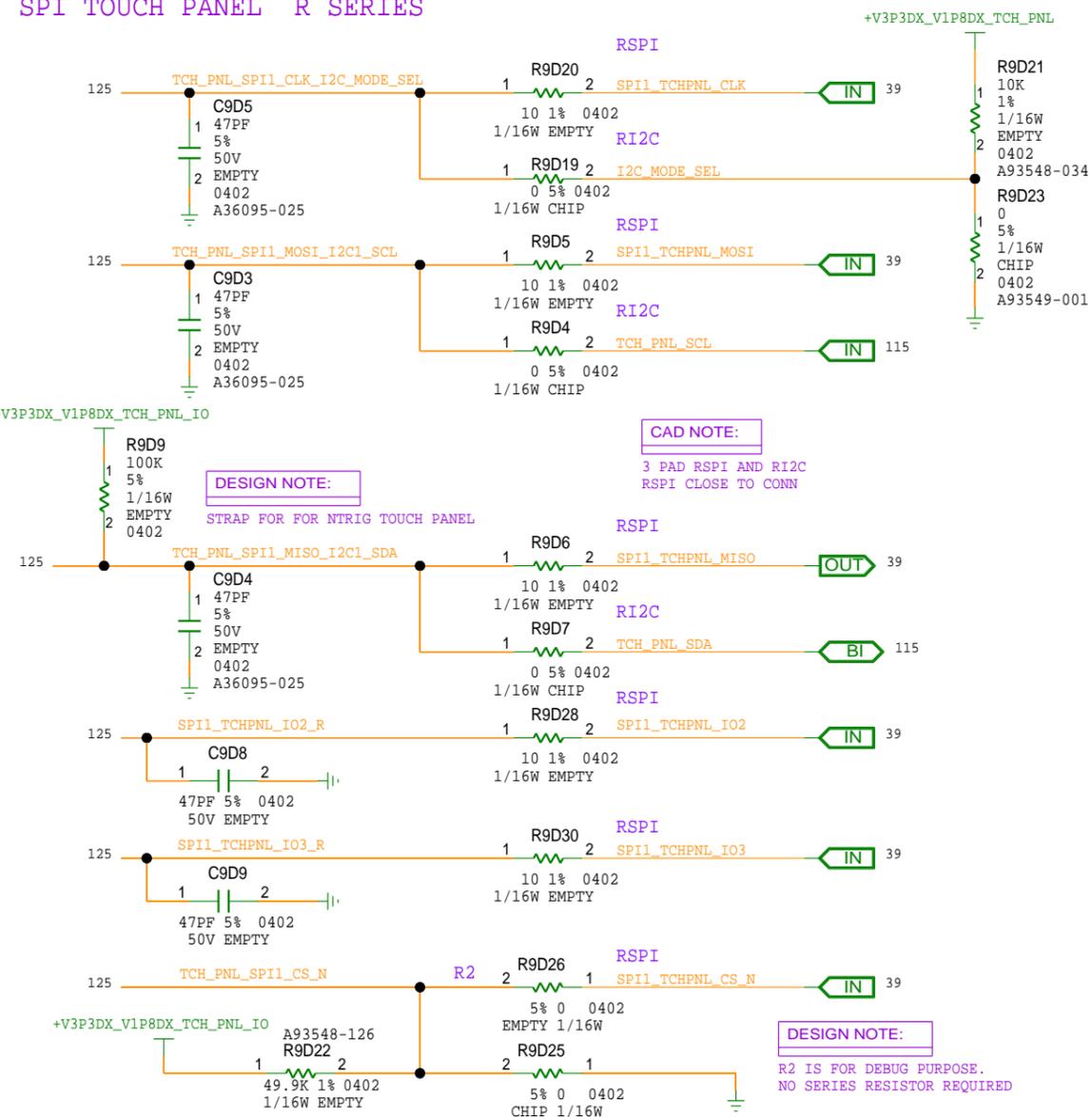


MODULE REV DETAILS		
MODULE NAME	REV	DATE

I2C TOUCH PANEL INTERRUPT



SPI TOUCH PANEL R SERIES



[PAGE_TITLE=TOUCH PANEL CONNECTOR]

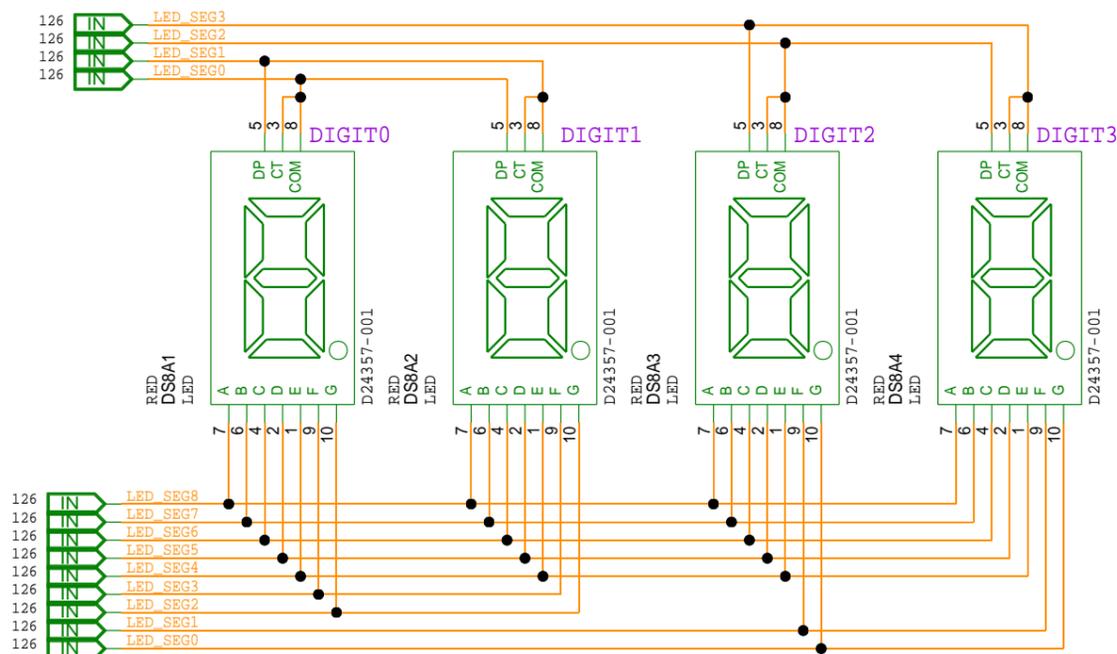
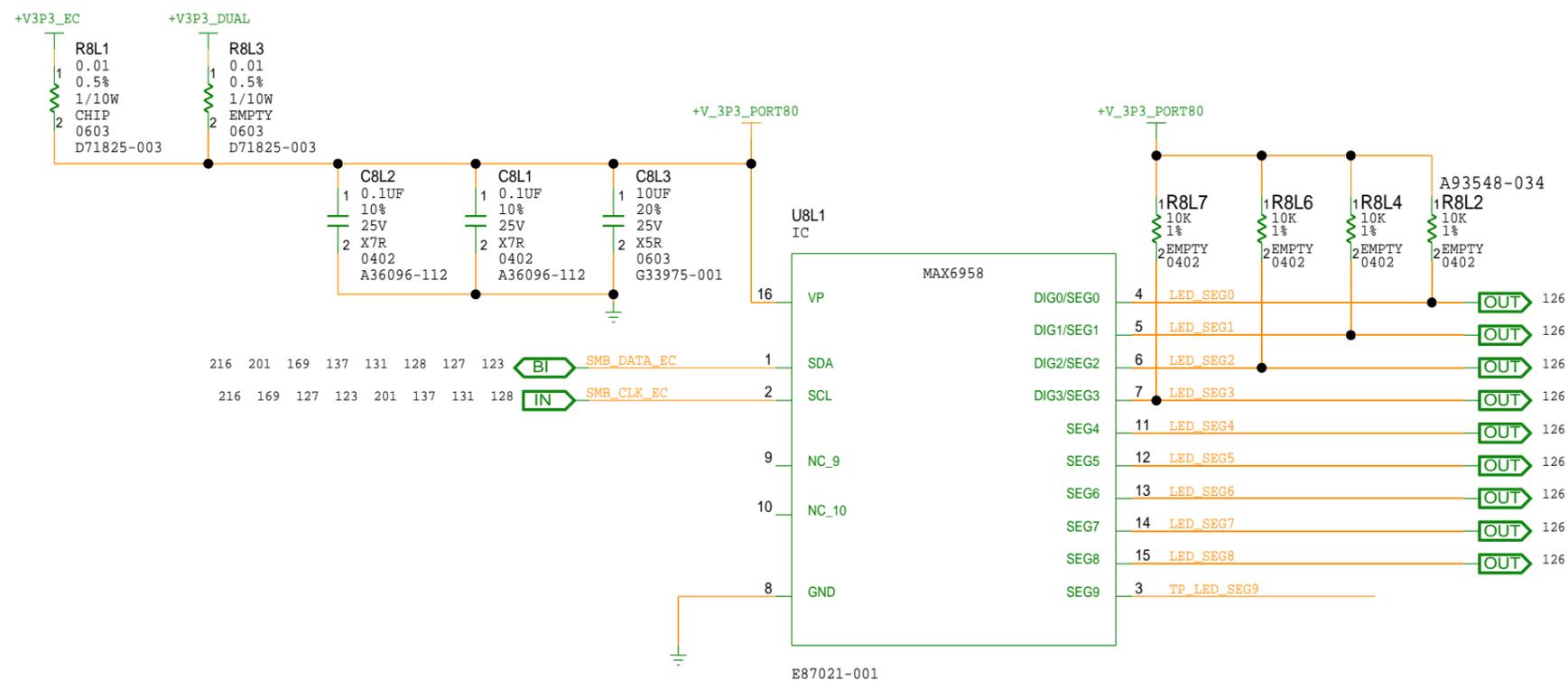
BPAGE DRAWING

udimm.sch_1.125
Fri Sep 27 16:41:12 2019

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MODULE REV DETAILS

MODULE NAME	REV	DATE



[PAGE_TITLE=ONBOARD PORT 80 DISPLAY]

BPAGE DRAWING

udimm.sch_1.126
Fri Sep 27 16:41:13 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 126	REV 0.7
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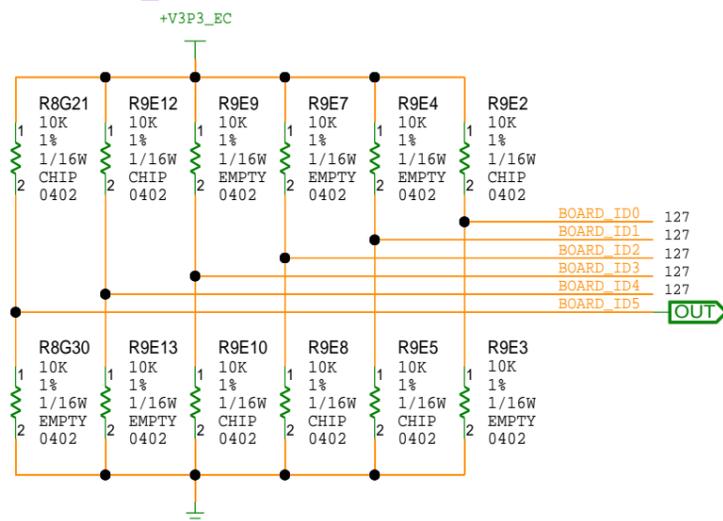
BOARD ID ,FAB ID & I/O EXPANDER

MODULE REV DETAILS

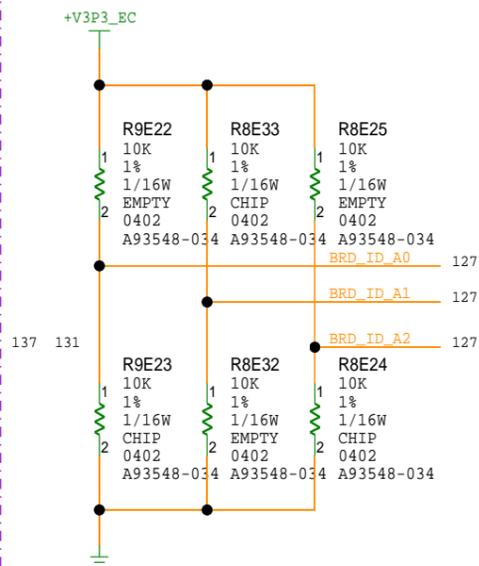
MODULE NAME	REV	DATE

BOARD ID

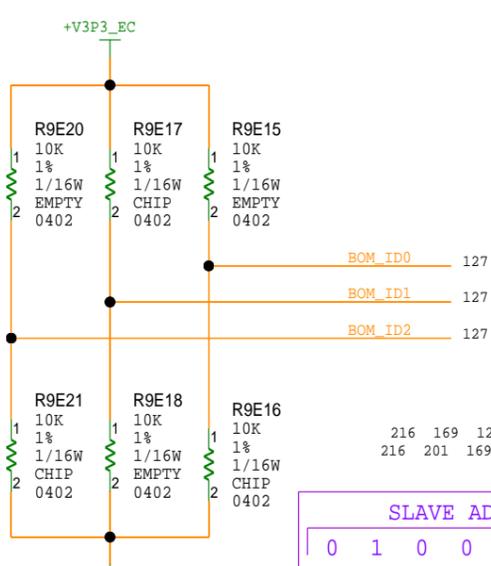
CML-S UDIMM RVP ERB/CRB 0X11H
BOARD_ID5 IS NOT USED



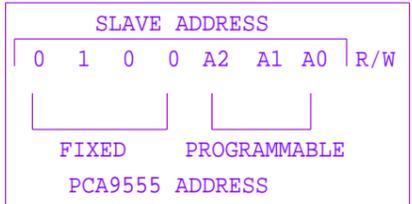
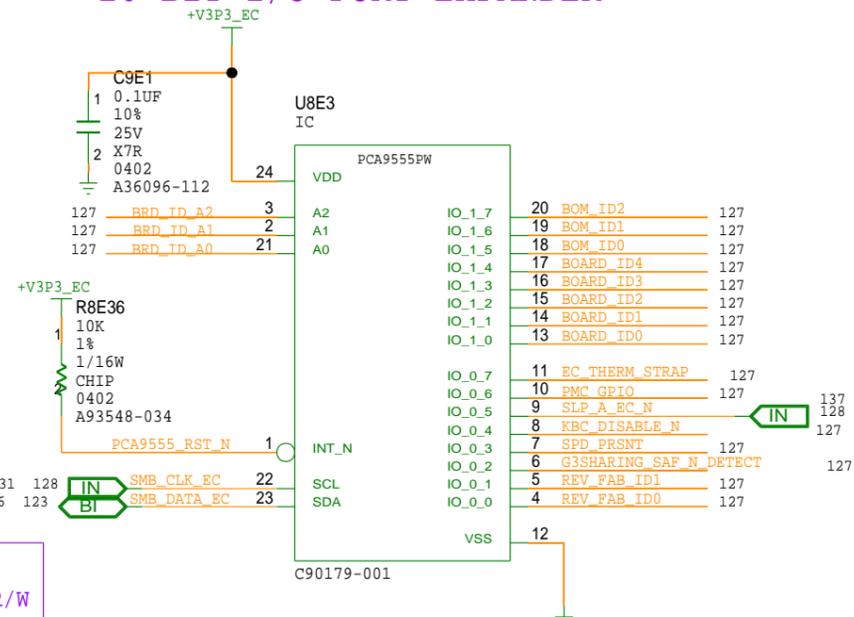
BOARD REVISION



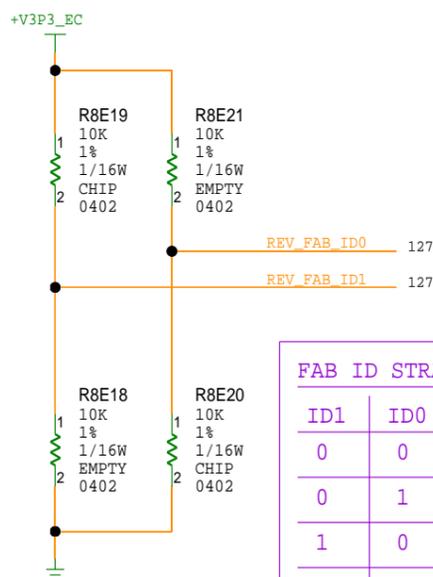
BOM ID



16-BIT I/O PORT EXPANDER



FAB REVISION



FAB ID STRAPPING TABLE

ID1	ID0	FAB ID
0	0	1
0	1	2
1	0	3
1	1	4

MODE SELECTION

DESIGN NOTE:

DISABLE KSC TIMEOUTS ON BOOT SEQUENCE

BOM NOTE:

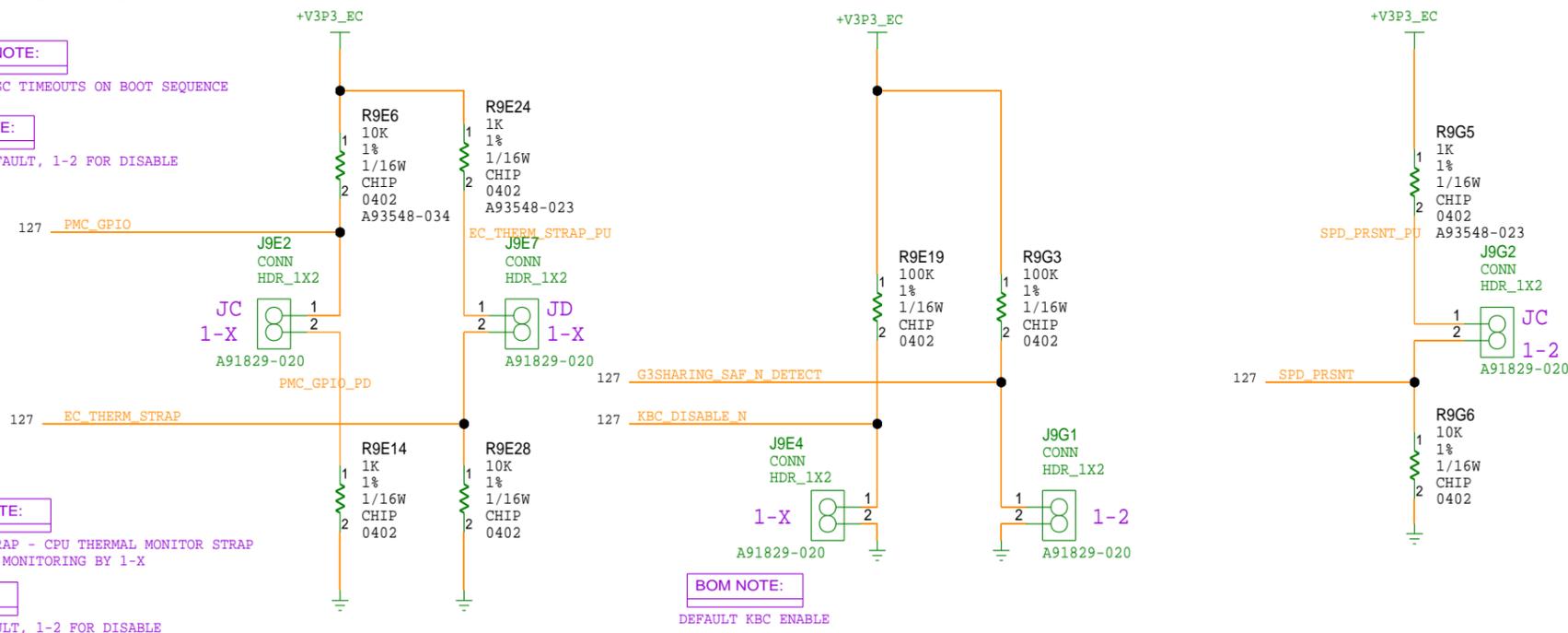
JC 1-X DEFAULT, 1-2 FOR DISABLE

DESIGN NOTE:

EC_THERM_STRAP - CPU THERMAL MONITOR STRAP
ENABLE PECE MONITORING BY 1-X

BOM NOTE:

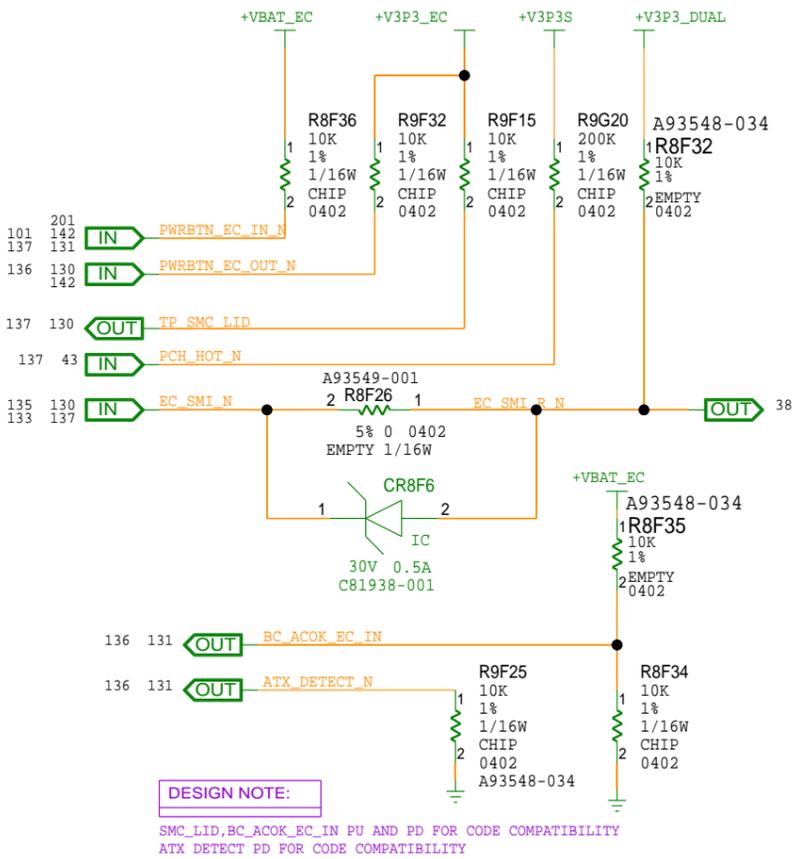
JD 1-X DEFAULT, 1-2 FOR DISABLE



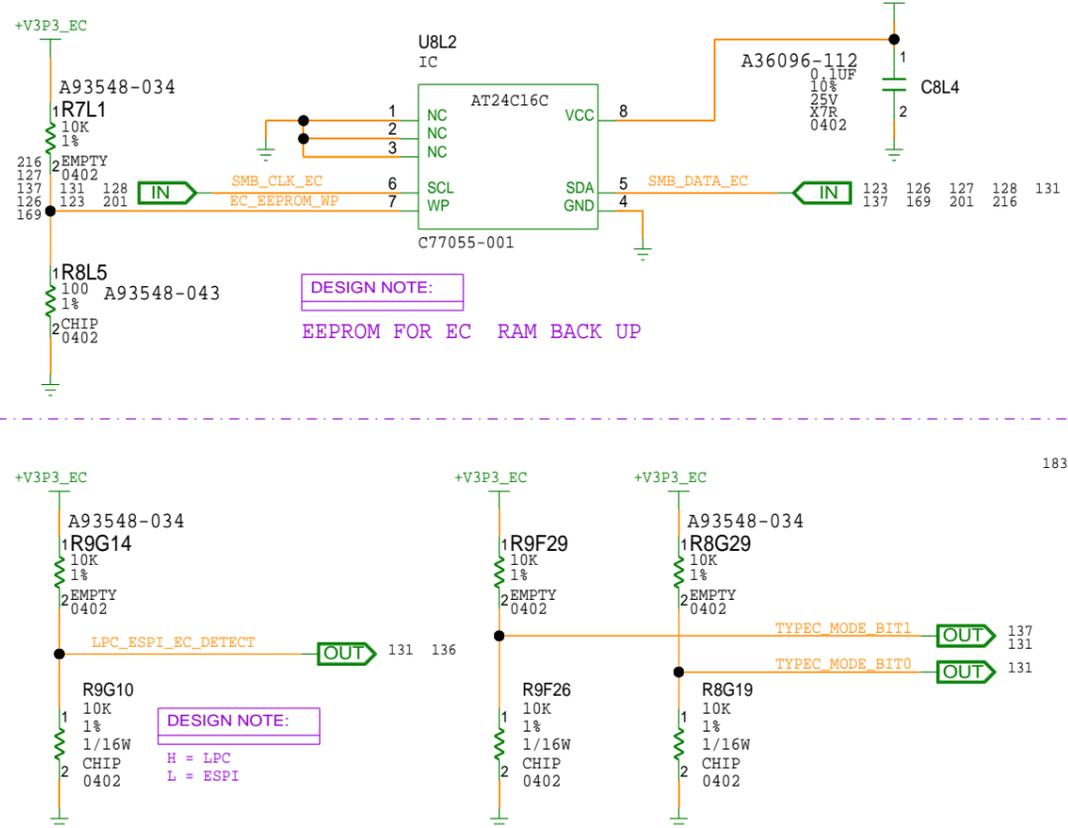
MODULE REV DETAILS

MODULE NAME	REV	DATE

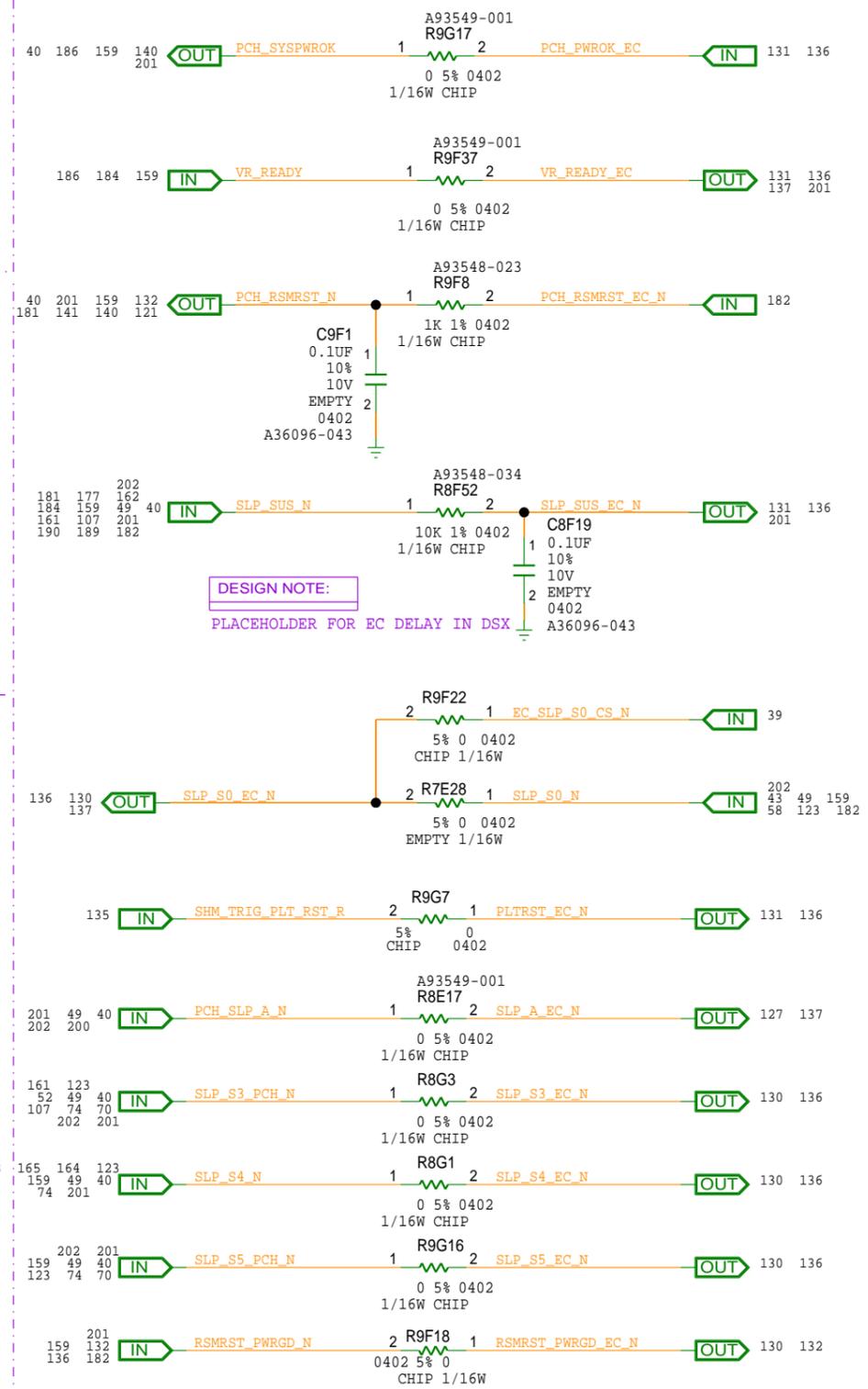
PU AND PD



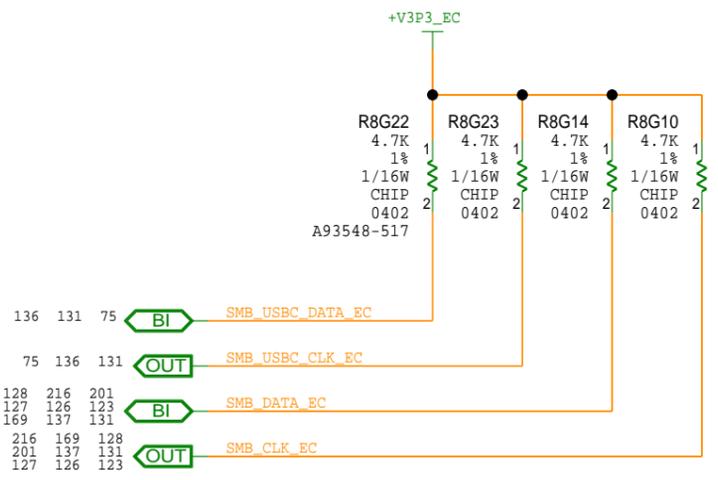
EC RAM BACKUP



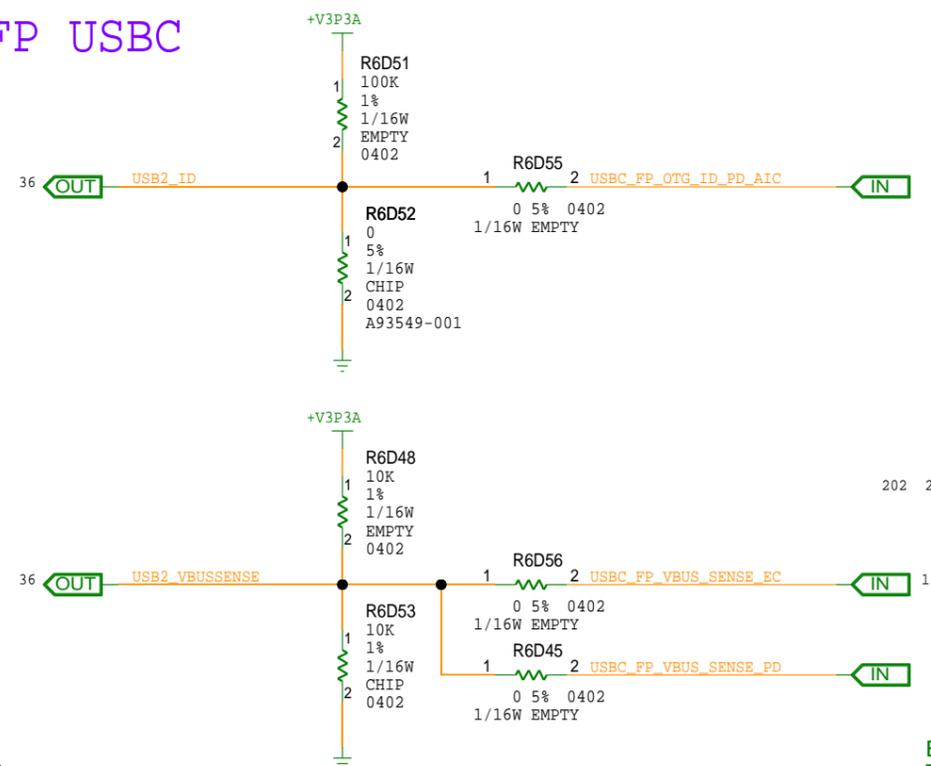
POWER SEQUENCE SIGNALS



EC SMBUS PU



FP USBC



[PAGE_TITLE=EC - MISCELLANEOUS]

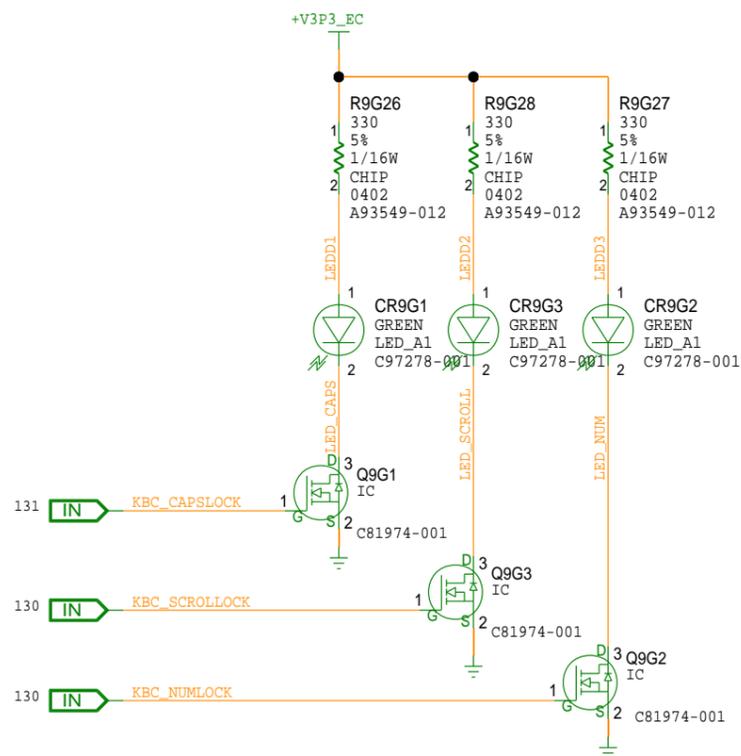
BPAGE DRAWING

udimm.sch_1.128
Fri Sep 27 16:41:15 2019

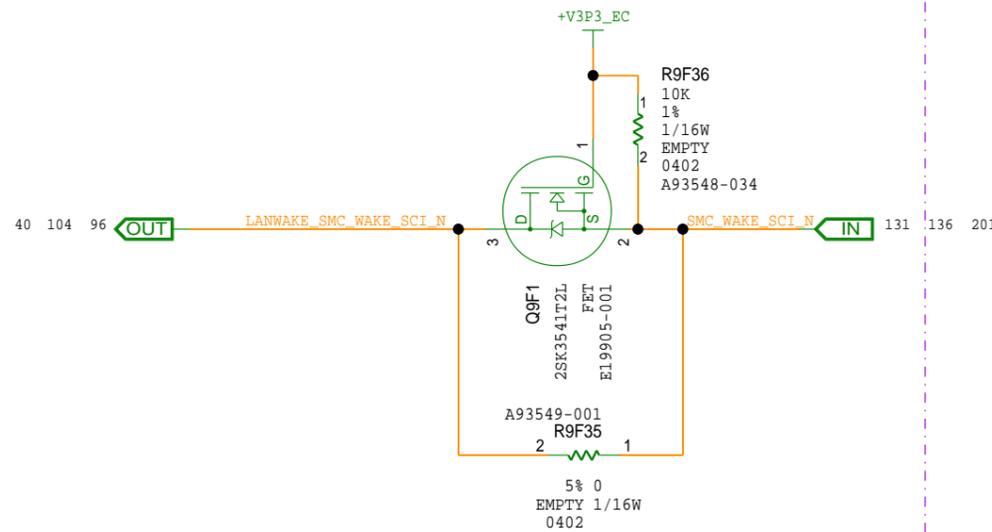
INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 128	REV 0.7
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MODULE REV DETAILS		
MODULE NAME	REV	DATE

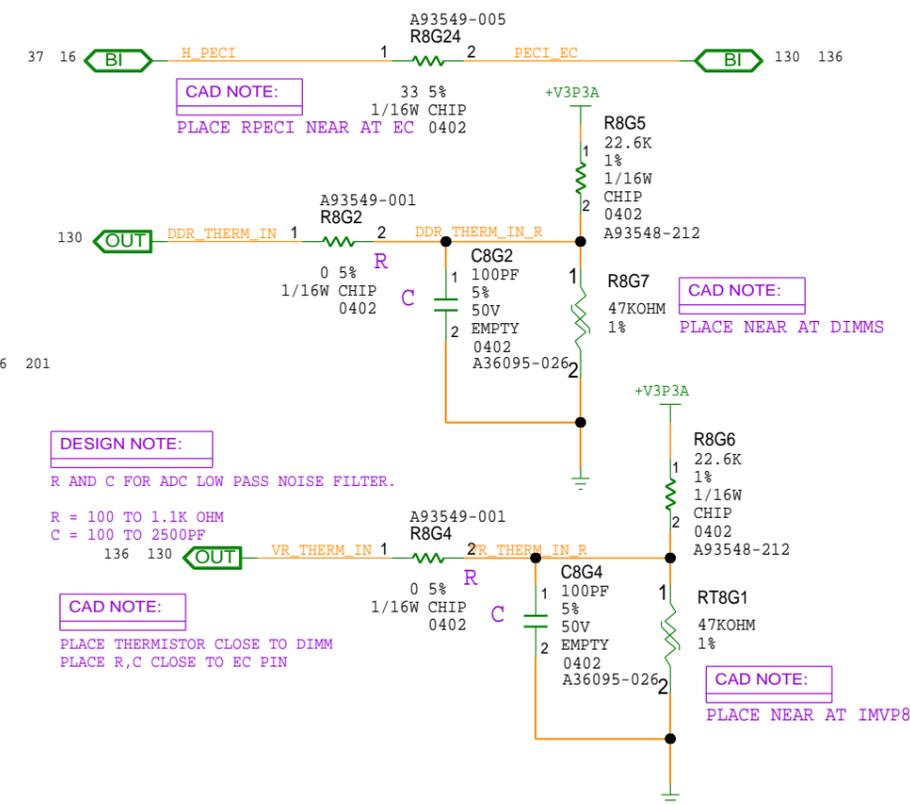
KB LEDS



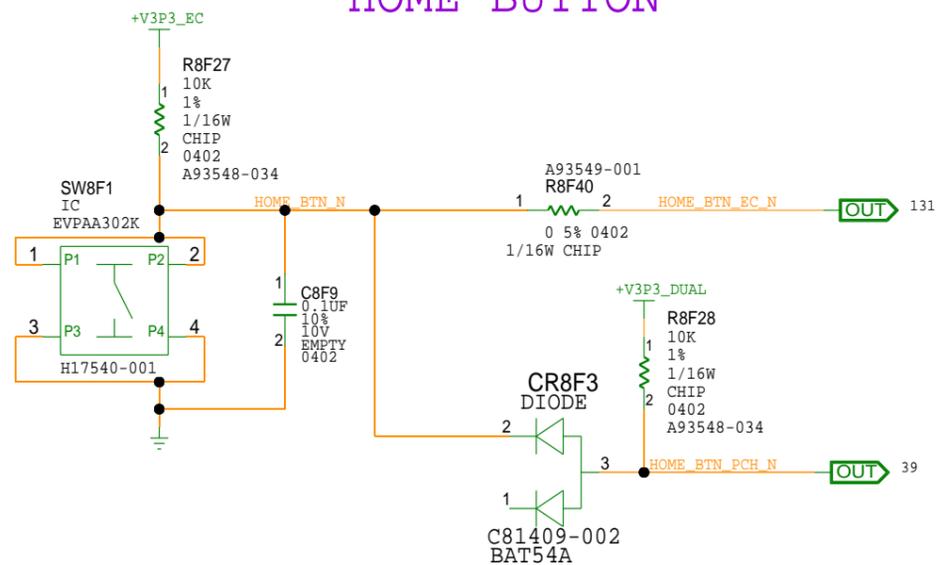
LAN WAKE



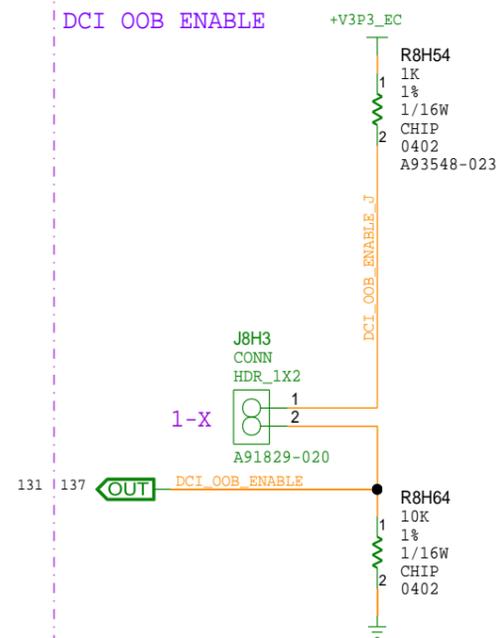
THERMAL MANAGEMENT



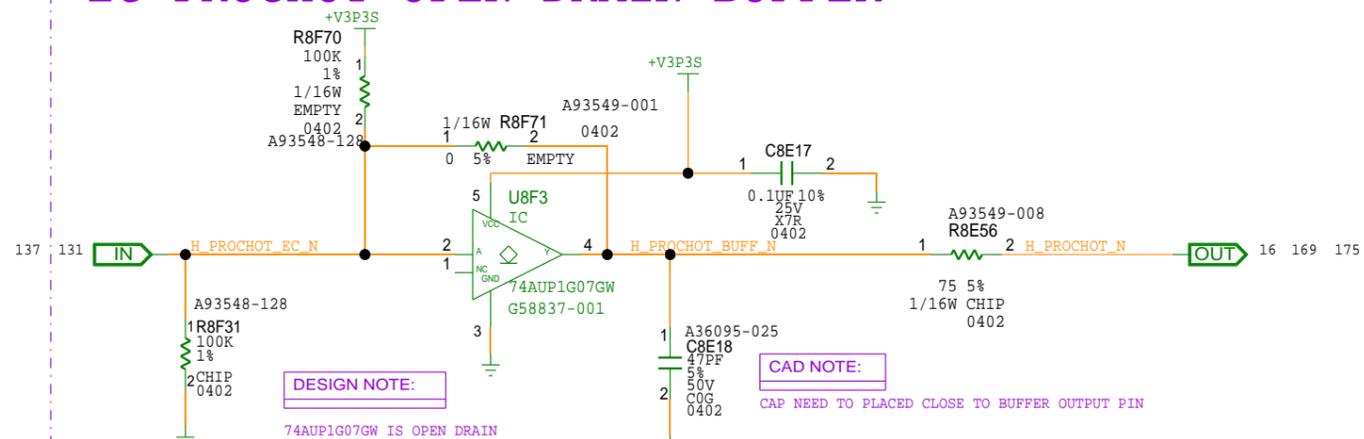
HOME BUTTON



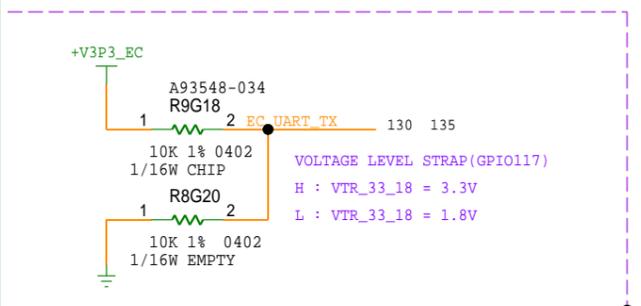
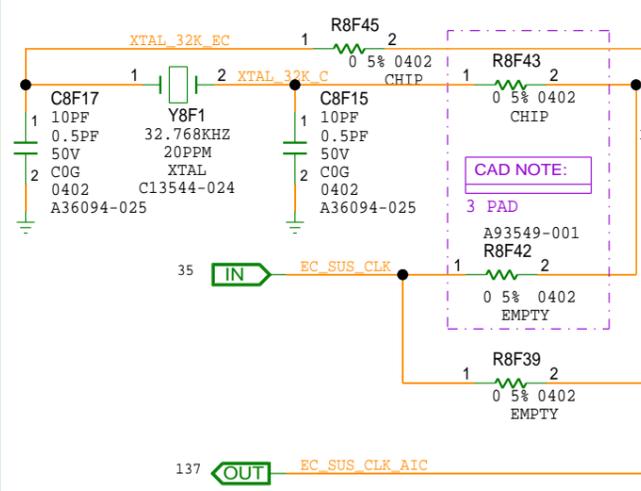
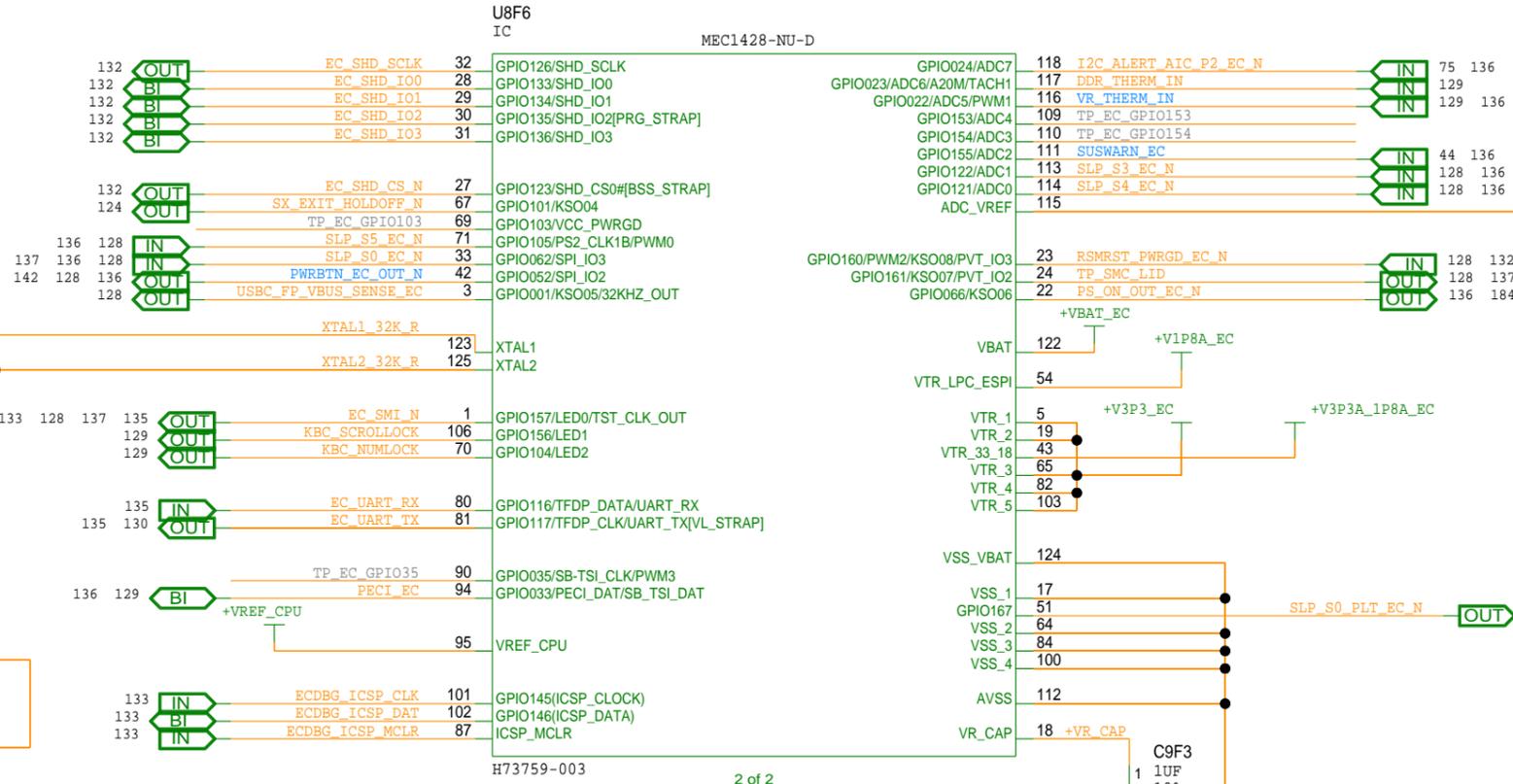
DCI OOB ENABLE



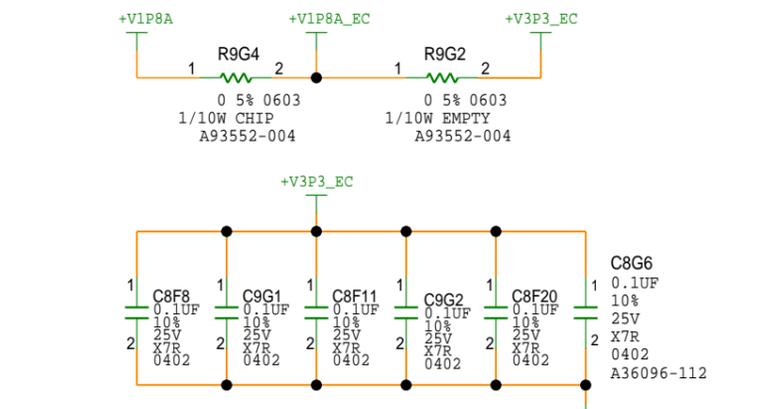
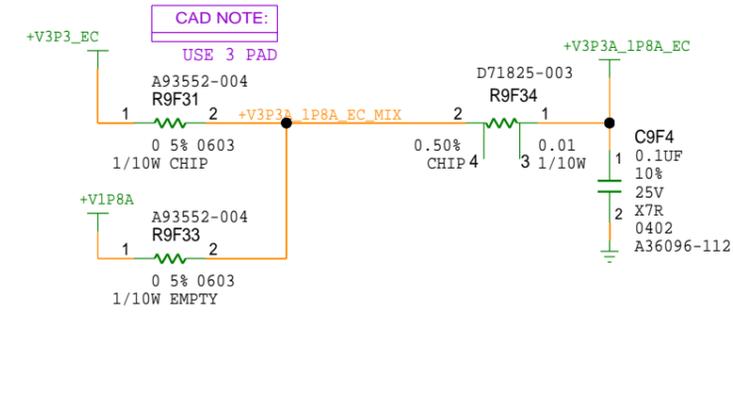
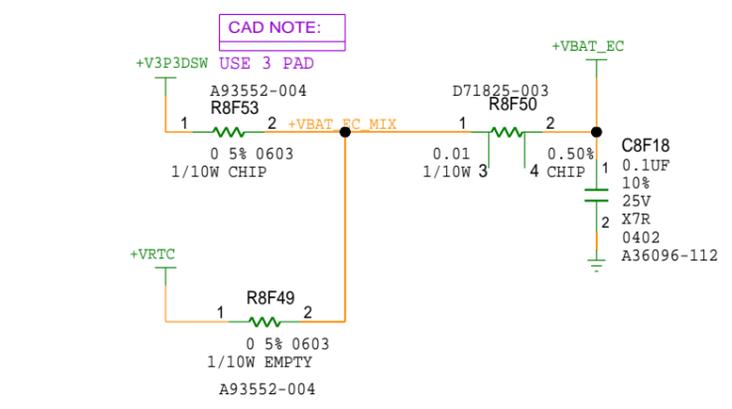
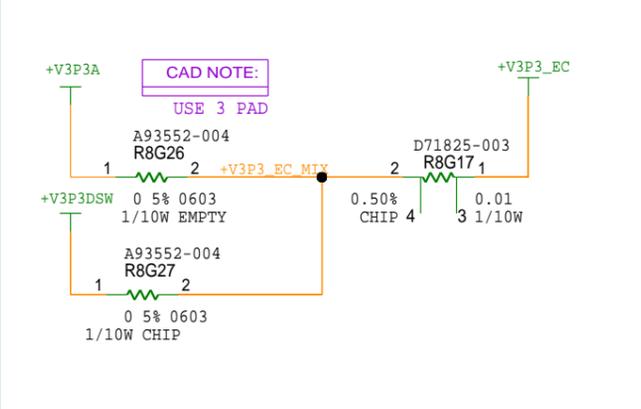
EC PROCHOT OPEN-DRAIN BUFFER



MODULE REV DETAILS		
MODULE NAME	REV	DATE



EC POWER WELL



BPAGE DRAWING
udimm.sch_1.130
Fri Sep 27 16:41:17 2019

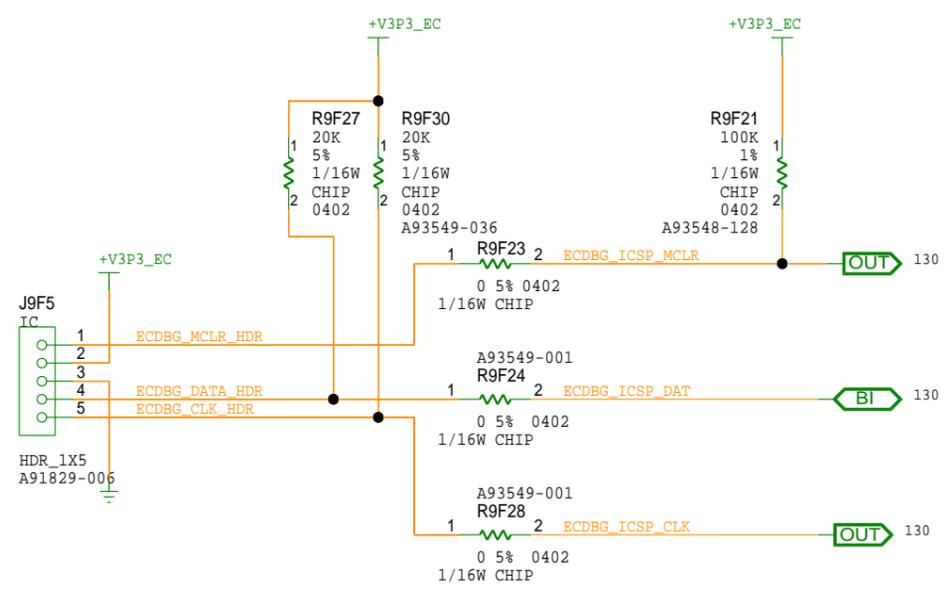
[PAGE_TITLE=EC - MEC14128 (1 OF 2)]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 130	REV 0.7
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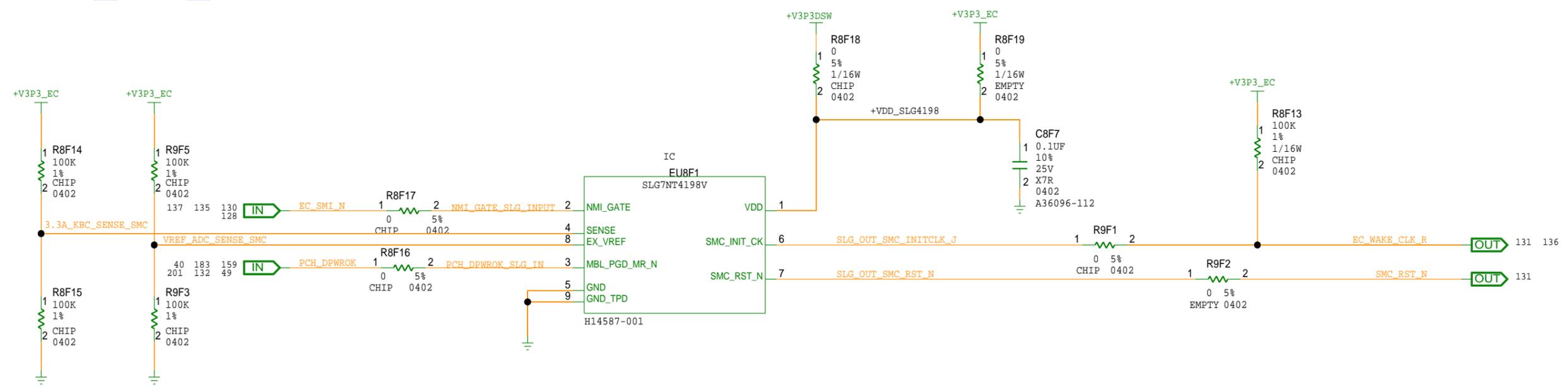
MODULE REV DETAILS

MODULE NAME	REV	DATE

ICSP DEBUG HEADER

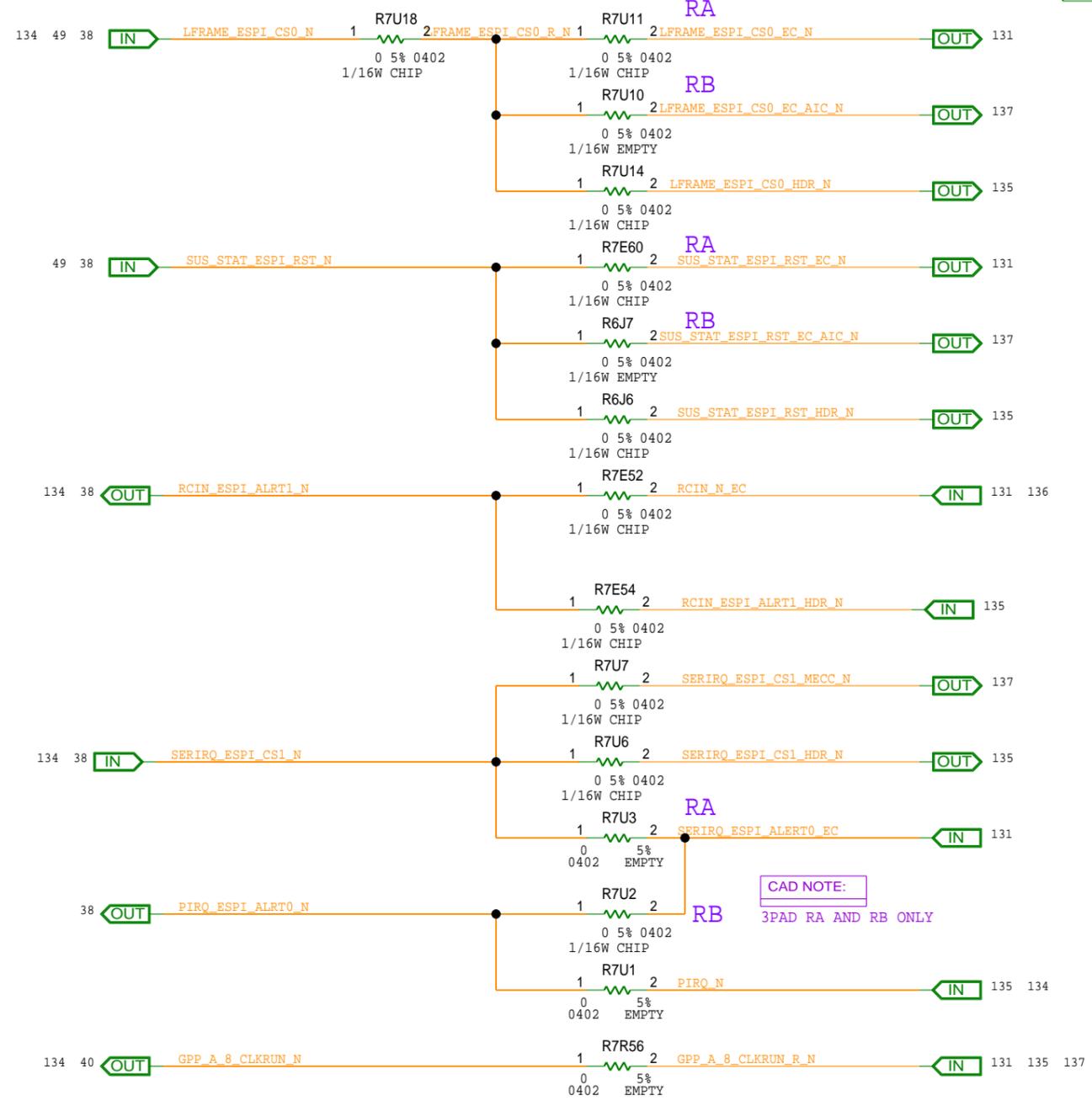
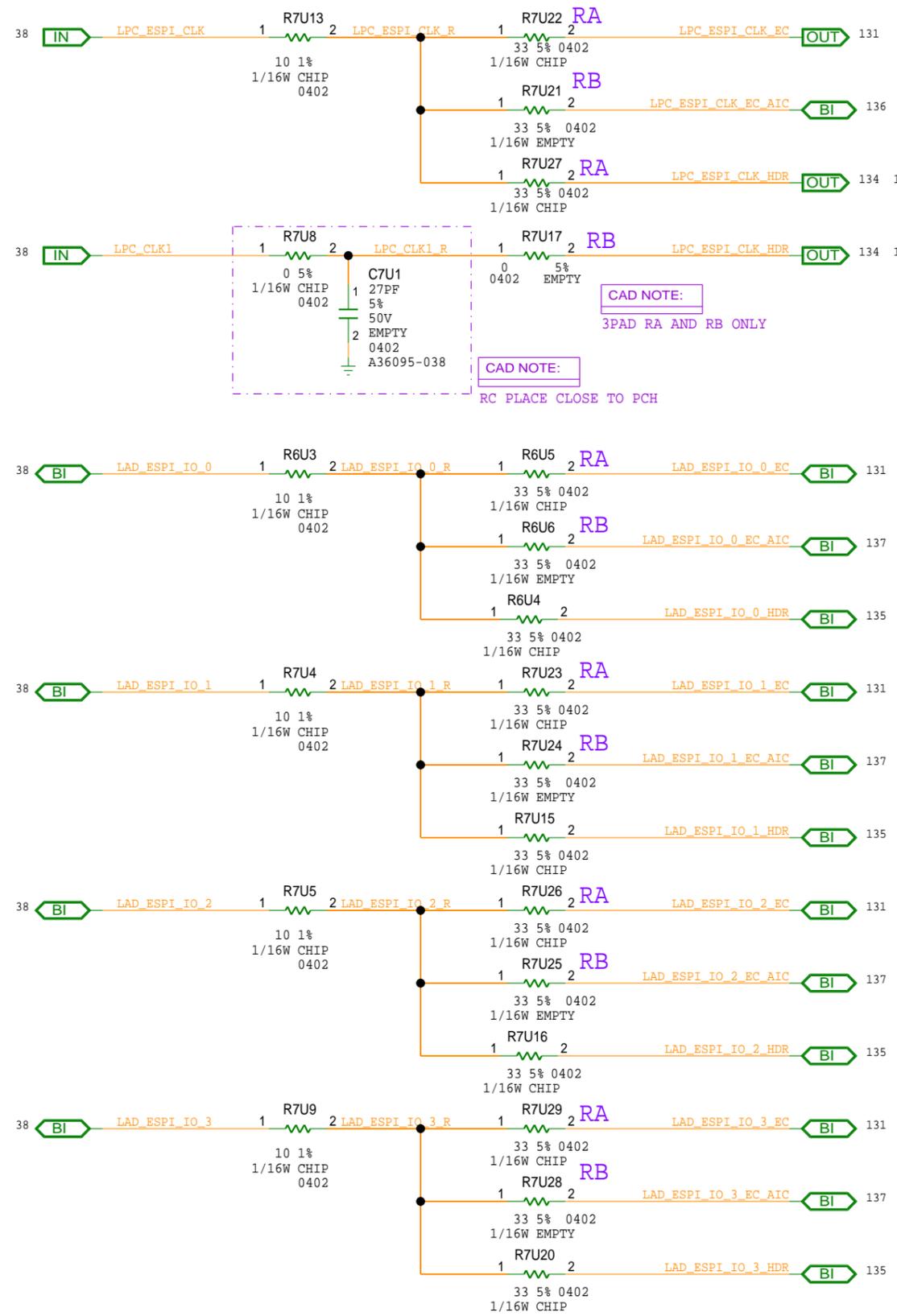


SMC_RST_N AND 1HZ CLOCK GENERATION



MODULE REV DETAILS		
MODULE NAME	REV	DATE

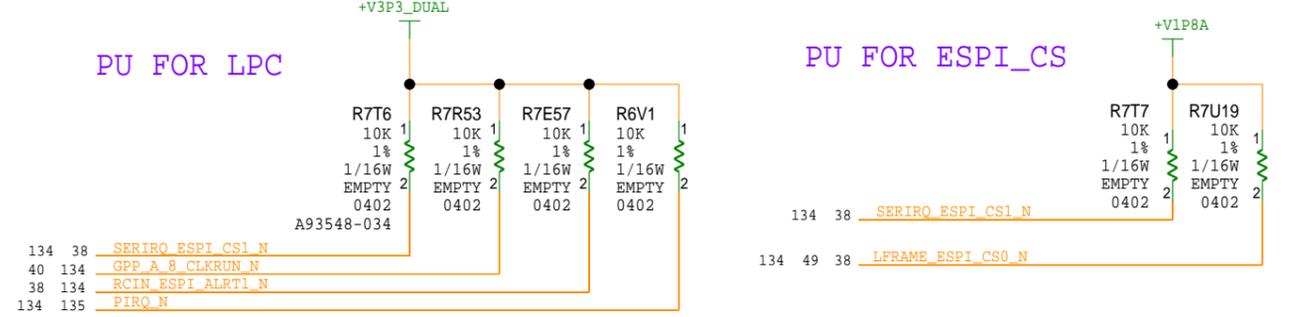
ESPI/LPC 2 LOAD TOPOLOGY (NOT TO 3PAD *_EC/*_HDR , ONLY 3PAD RA/RB)



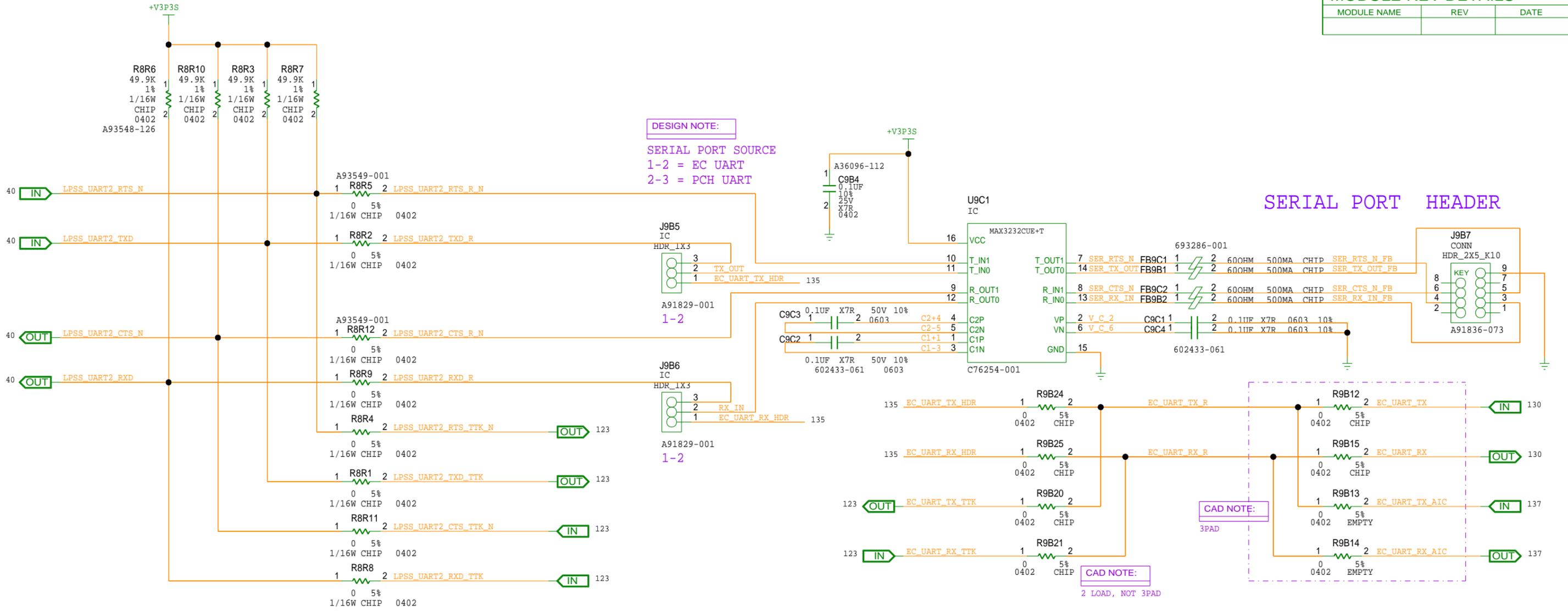
CAD NOTE:
3PAD RA AND RB ONLY

CAD NOTE:
RC PLACE CLOSE TO PCH

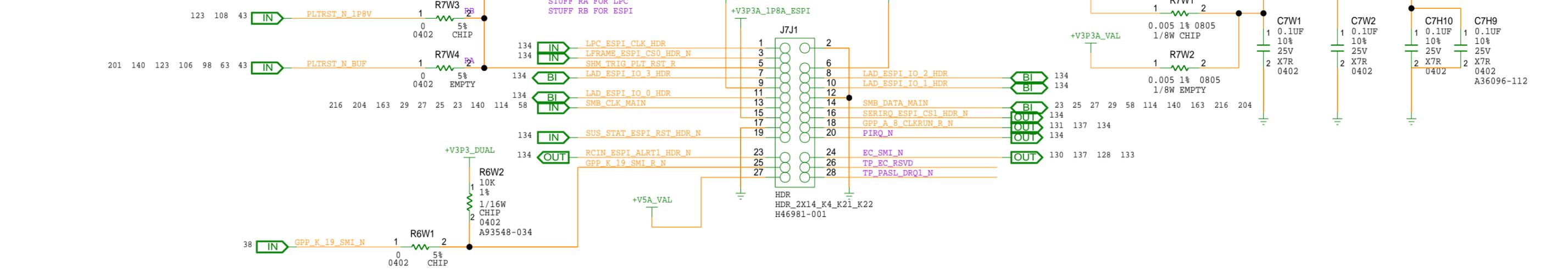
CAD NOTE:
3PAD RA AND RB ONLY



MODULE REV DETAILS		
MODULE NAME	REV	DATE



ESPI/LPC HEADER

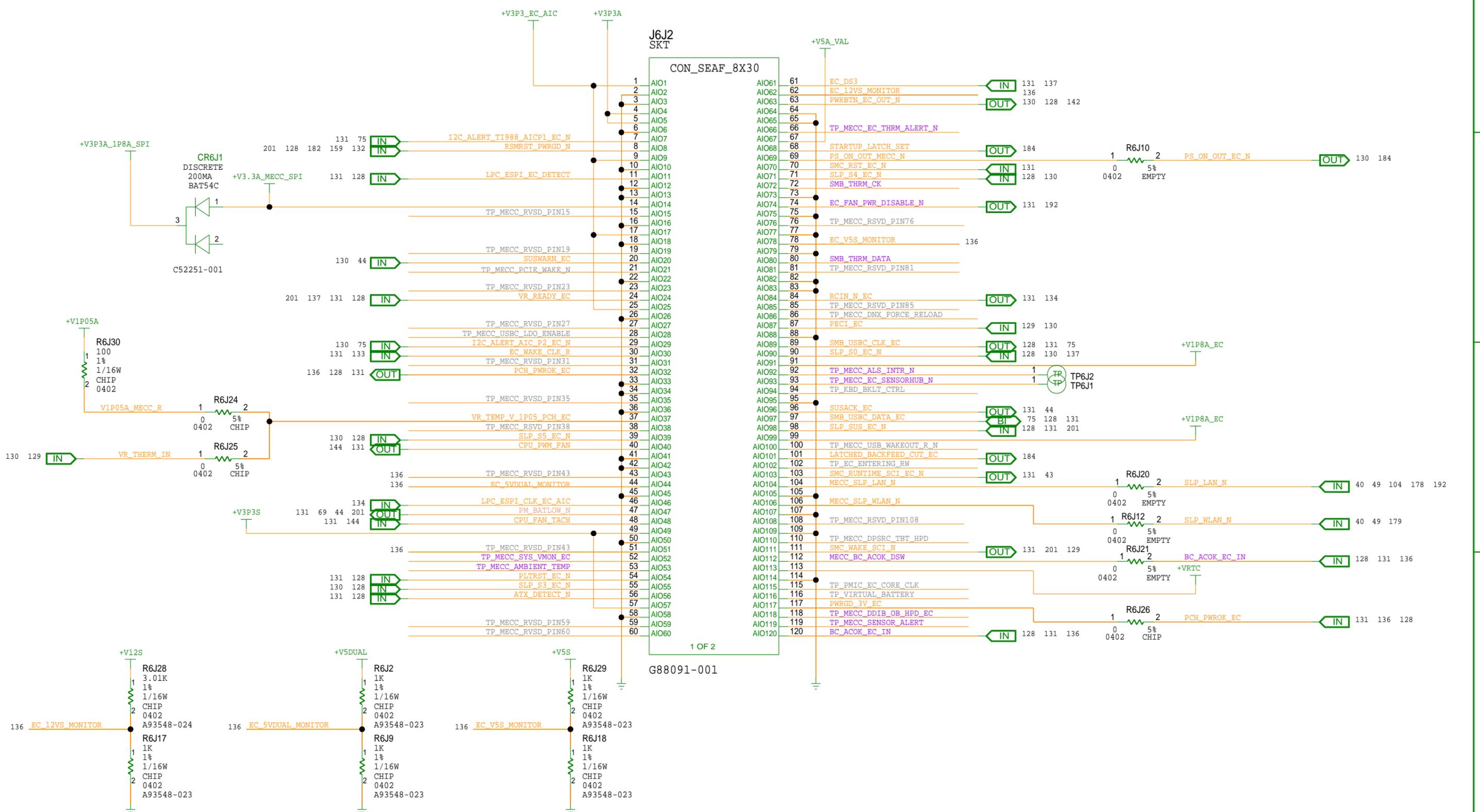


[PAGE_TITLE=EC - SERIAL PORT]

BPAGE DRAWING
udimm.sch_1.135
Fri Sep 27 16:41:22 2019

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MODULE REV DETAILS		
MODULE NAME	REV	DATE



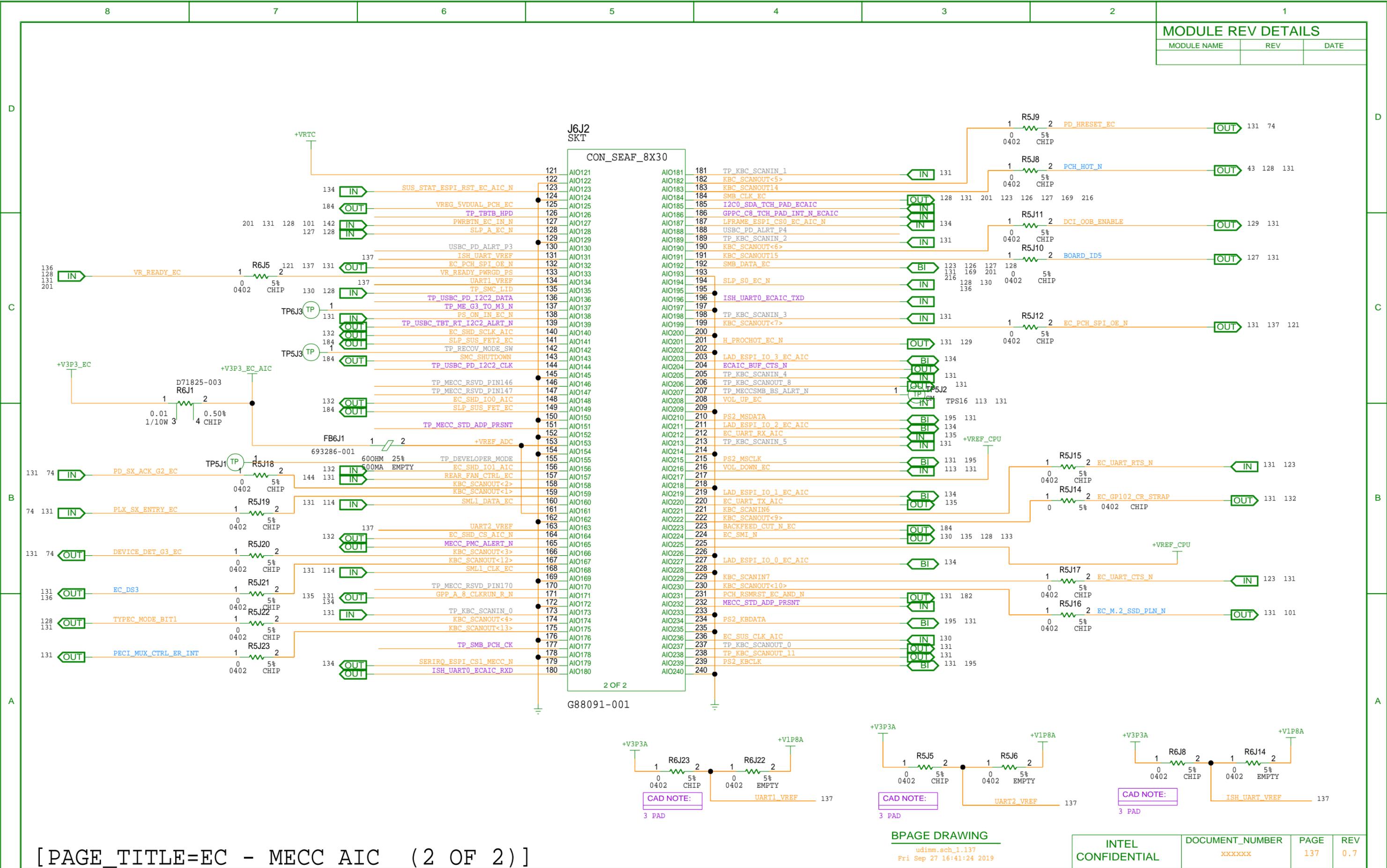
[PAGE_TITLE=EC - MECC AIC (1 OF 2)]

BPAGE DRAWING
 udimm.sch_1.136
 Fri Sep 27 16:41:23 2019

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MODULE REV DETAILS

MODULE NAME	REV	DATE



[PAGE_TITLE=EC - MECC AIC (2 OF 2)]

BPAGE DRAWING

udimm.sch_1.137
Fri Sep 27 16:41:24 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 137	REV 0.7
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CUSTOM TEXT BPAGE

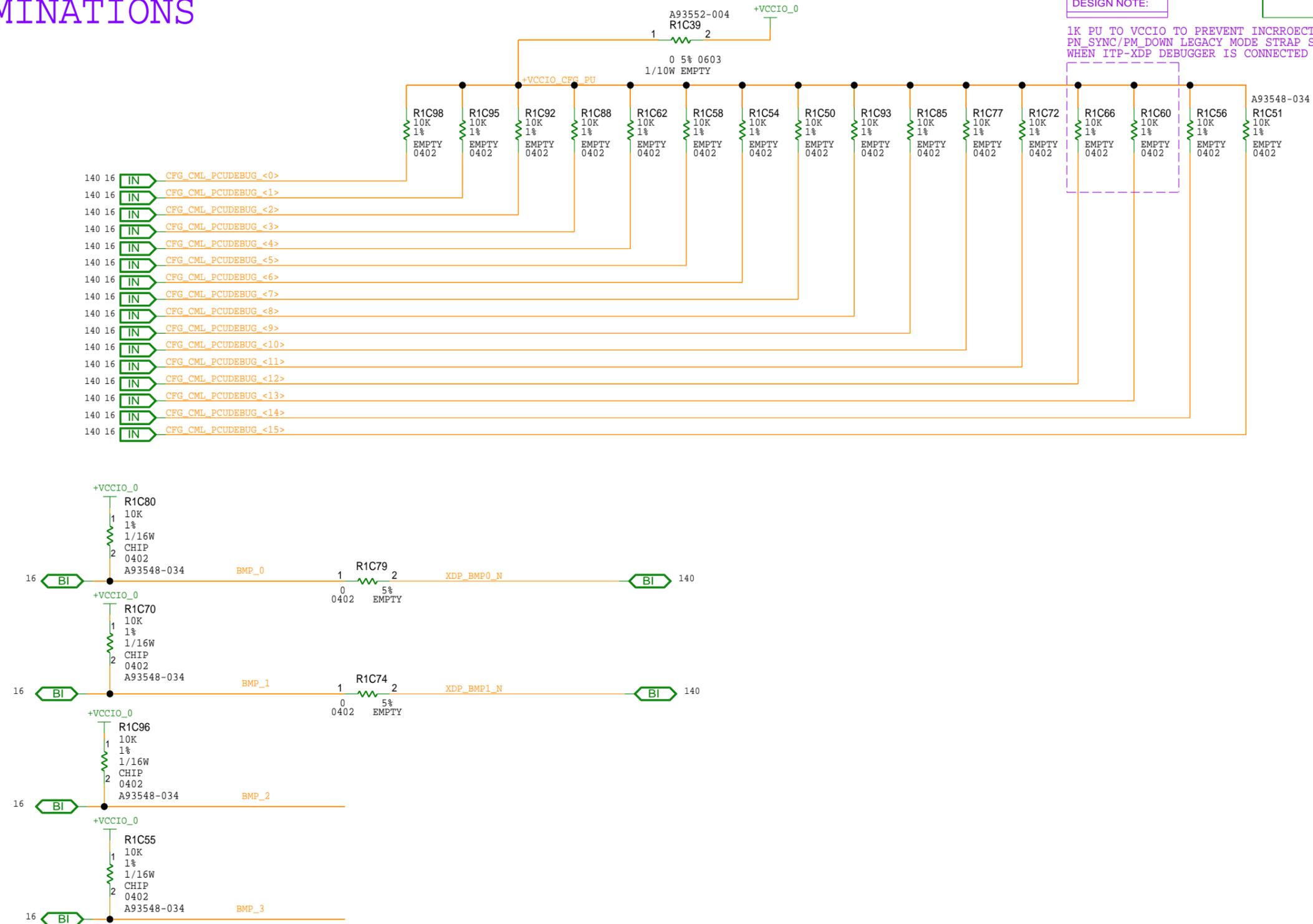
CFG TERMINATIONS

MODULE REV DETAILS

MODULE NAME	REV	DATE

DESIGN NOTE:

1K PU TO VCCIO TO PREVENT INCRORECT
PN_SYNC/PM_DOWN LEGACY MODE STRAP SAMPLING
WHEN ITP-XDP DEBUGGER IS CONNECTED



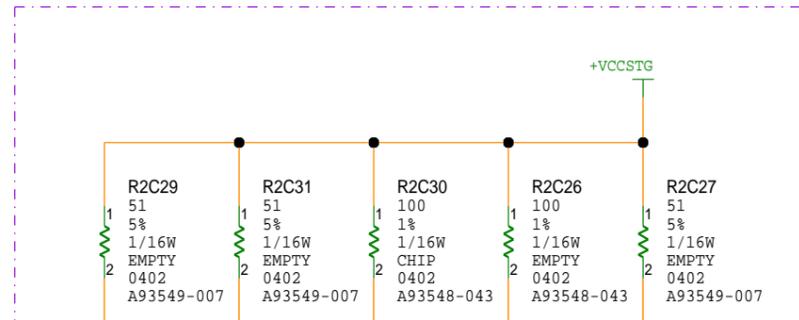
MODULE REV DETAILS

MODULE NAME	REV	DATE

MERGED XDP JTAG SIGNALS

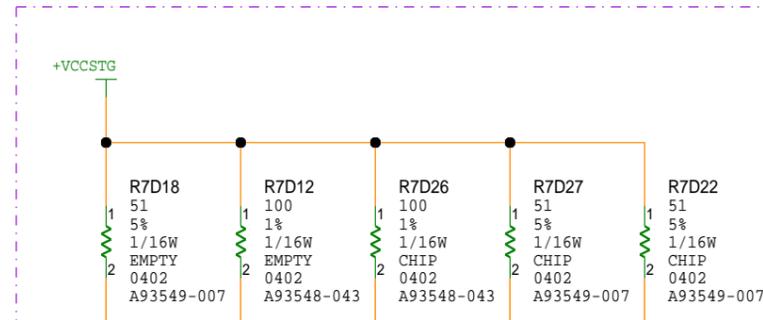
CAD NOTE:

PLACE WITHIN 1.1INCH OF CPU



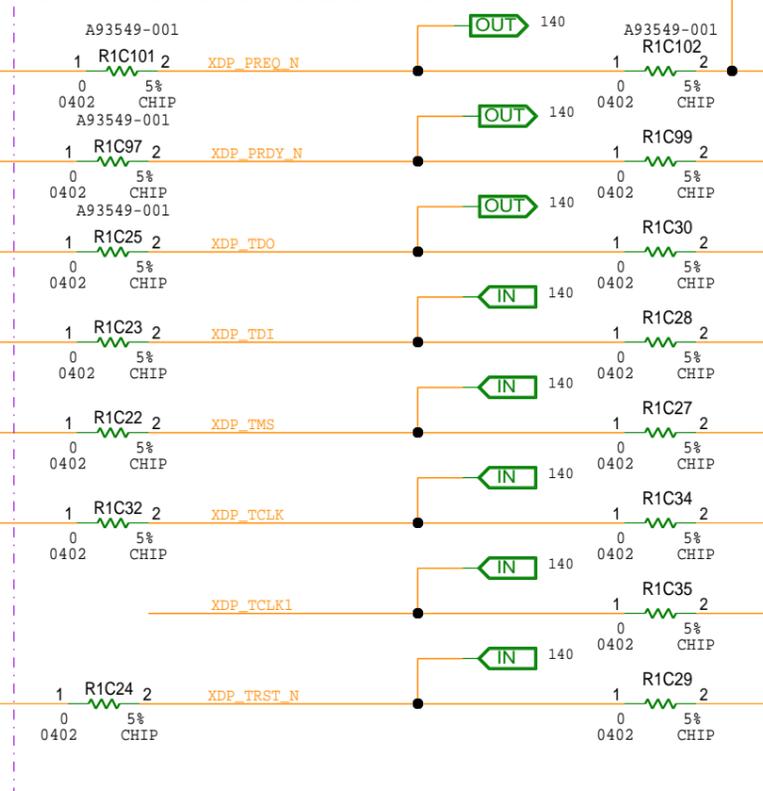
CAD NOTE:

PLACE WITHIN 1.1INCH OF PCH

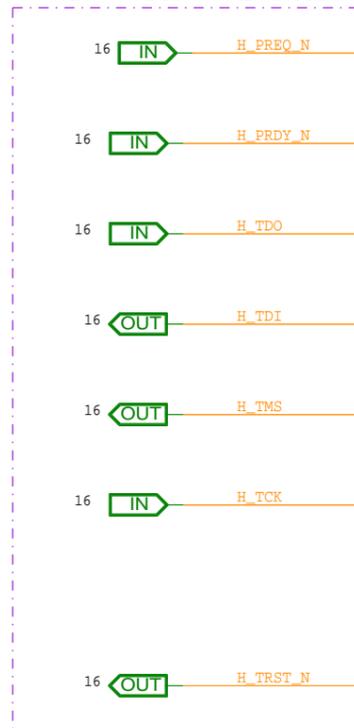


CAD NOTE: TO XDP CONN

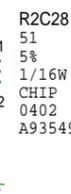
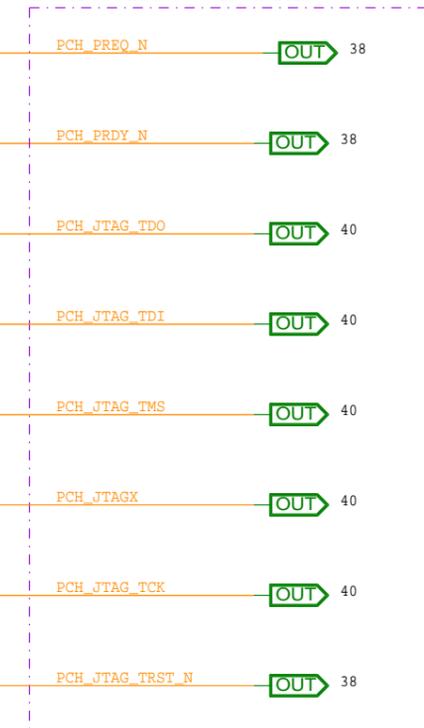
PLACE RS WITHIN 1.1INCH OF MERGED XDP CONNECTOR



CPU JTAG SIGNALS



PCH JTAG SIGNALS

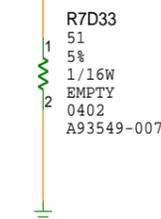


CAD NOTE:

PLACE 51OHM PD WITHIN 1.1INCH OF CPU

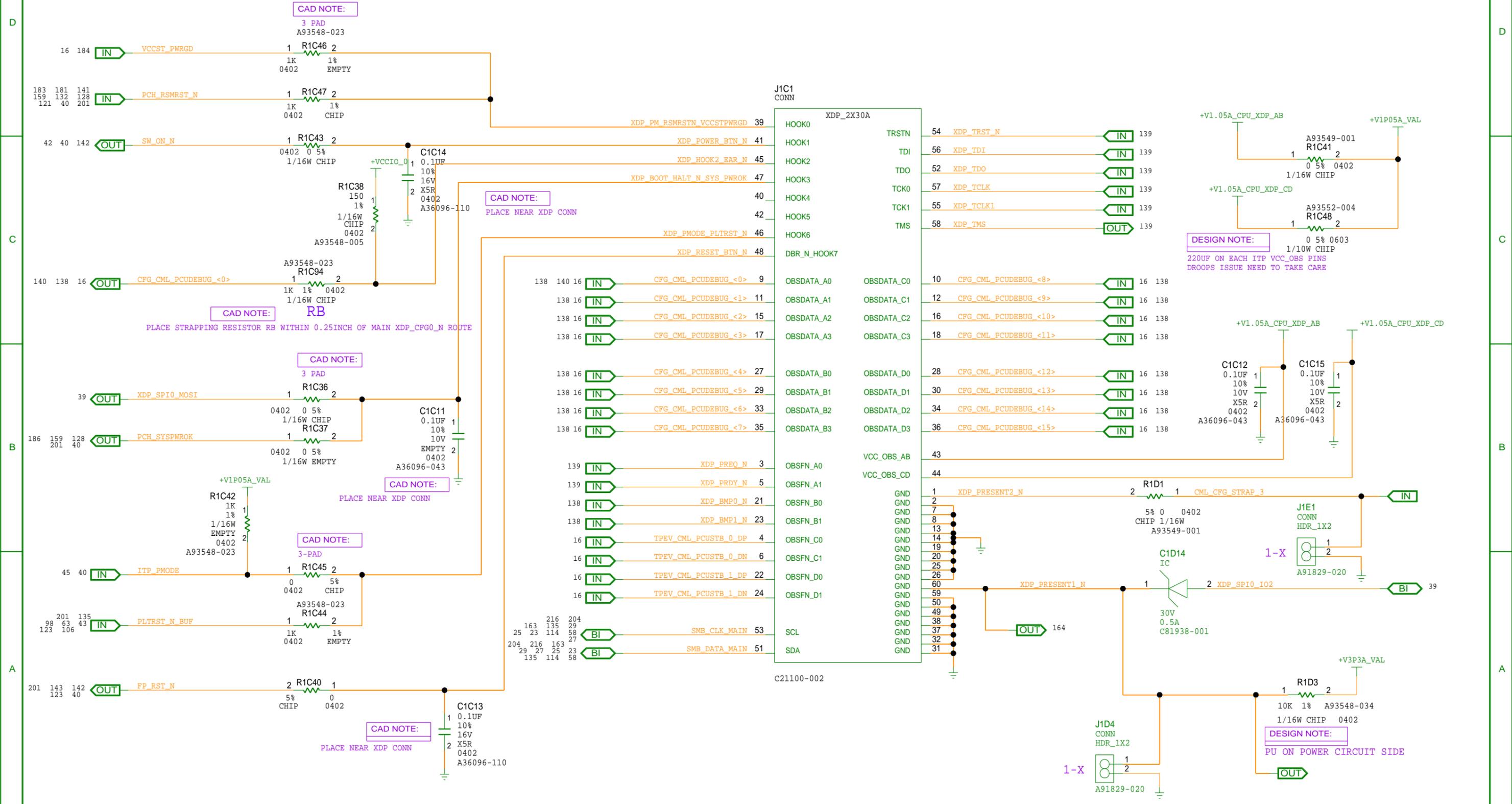
CAD NOTE:

PLACE 51OHM PD WITHIN 1.1INCH OF PCH



MERGED XDP CONNECTOR

MODULE REV DETAILS		
MODULE NAME	REV	DATE



[PAGE_TITLE=JTAG/CFG - MERGED XDP CONNECTOR]

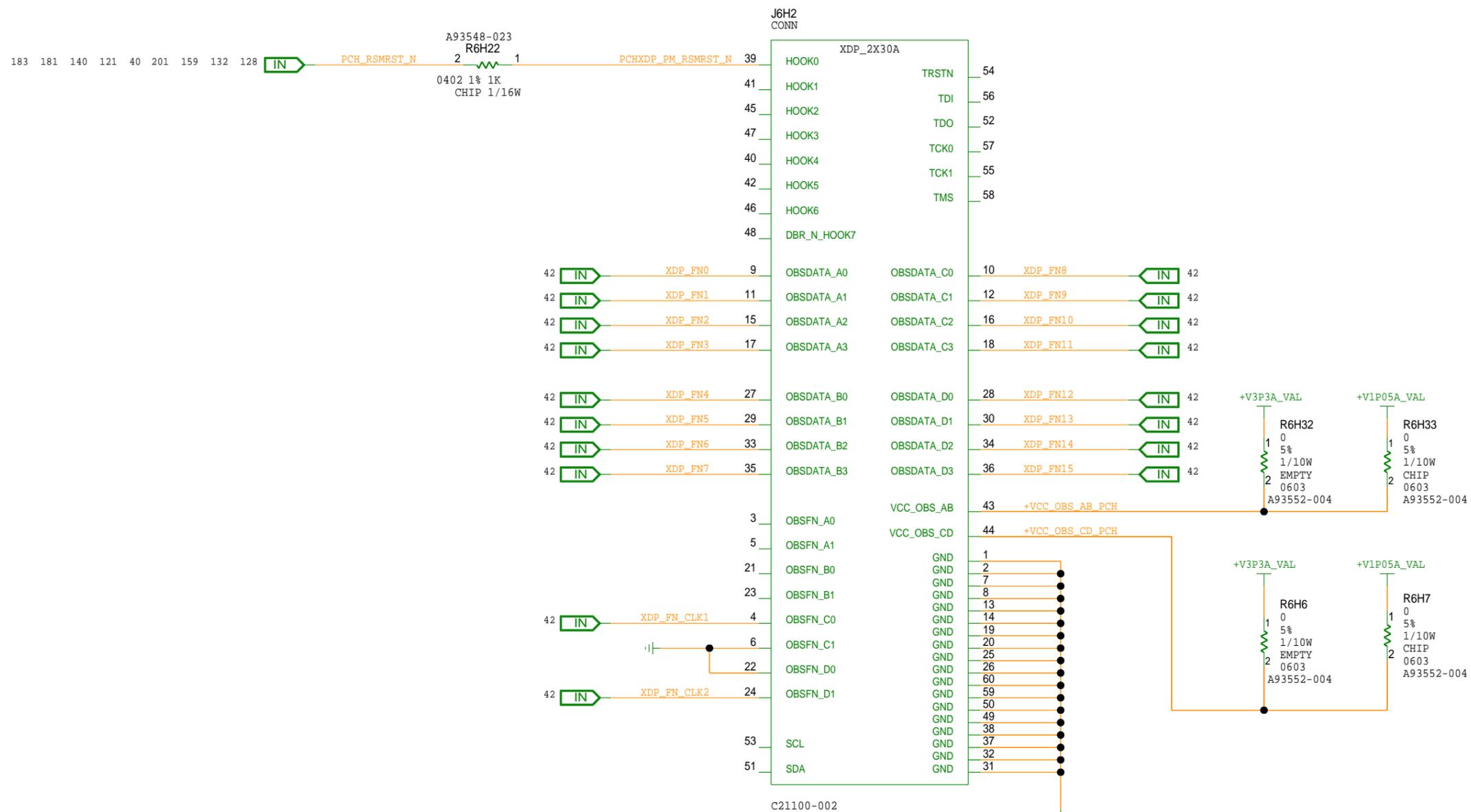
BPAGE DRAWING
udimm.sch_1.140
Fri Sep 27 16:41:27 2019

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MODULE REV DETAILS

MODULE NAME	REV	DATE

PCH VISA ONLY XDP CONNECTOR



[PAGE_TITLE=JTAG/CFG - JTAG/CFG - PCH VISA-ONLY XDP CONNECTOR]

BPAGE DRAWING

udimm.sch_1.141
Fri Sep 27 16:41:27 2019

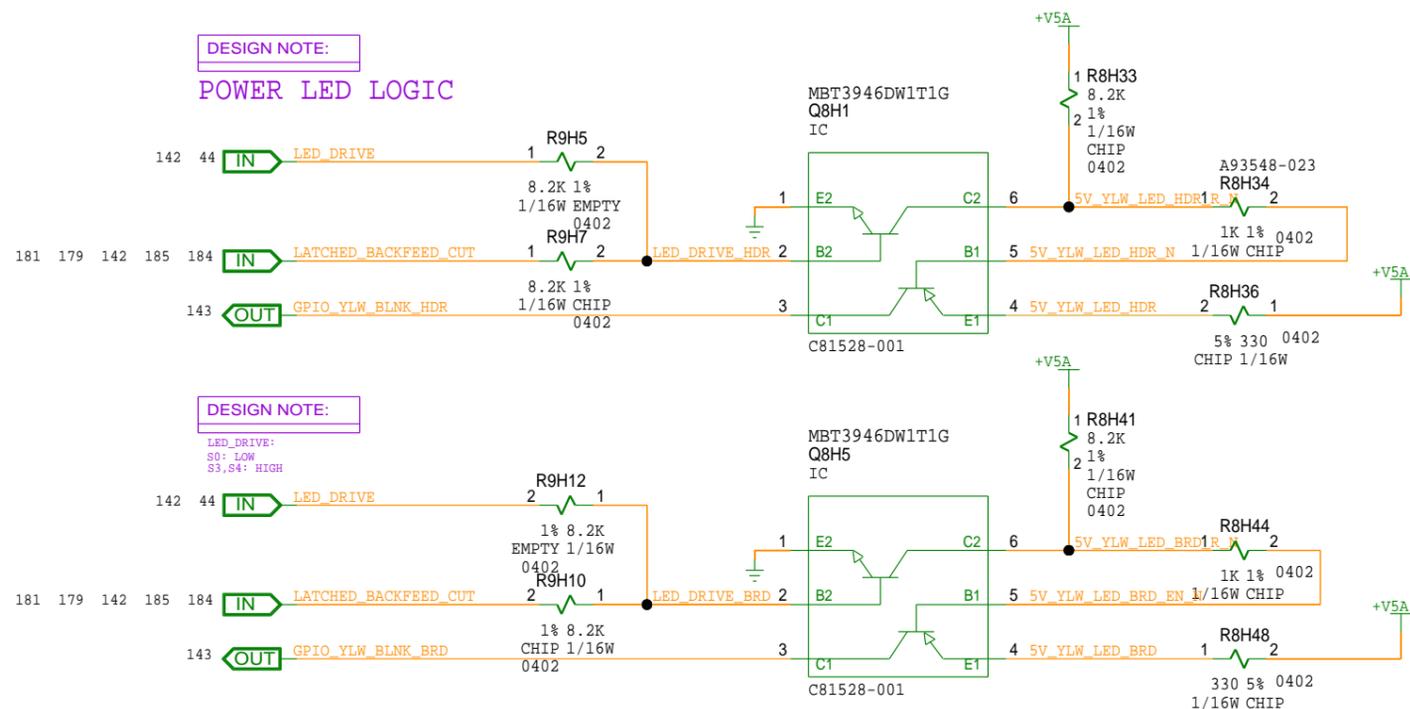
INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 141	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE

DESIGN NOTE:

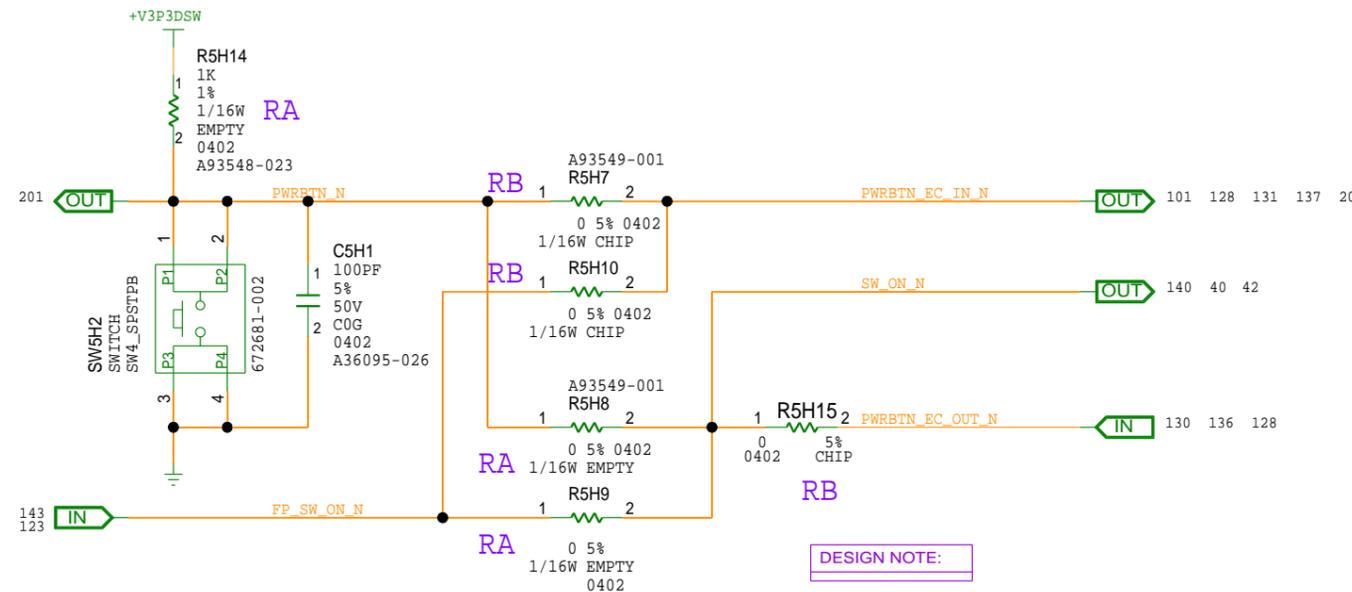
POWER LED LOGIC



DESIGN NOTE:

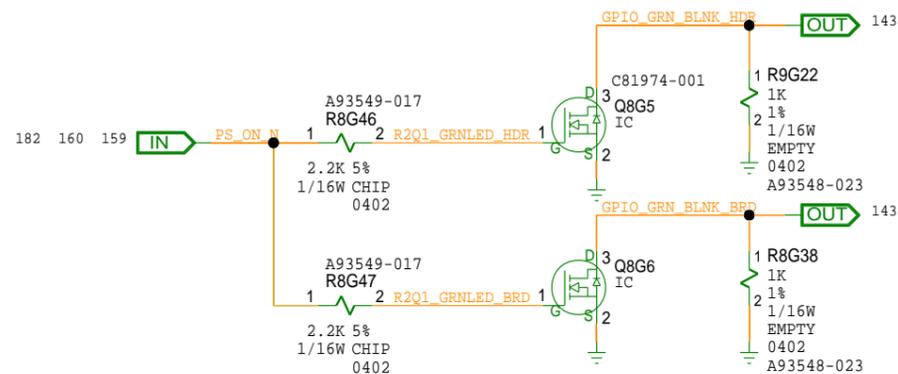
LED_DRIVE:
S0: LOW
S3,S4: HIGH

SWITCH



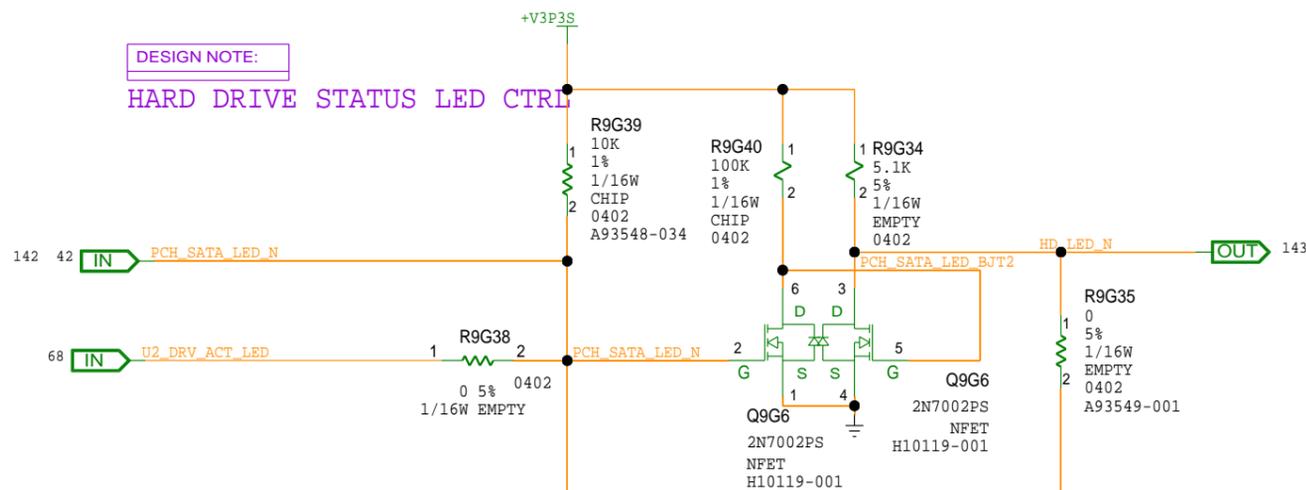
DESIGN NOTE:

RA & RB STUFF EXCLUSIVELY
RA : PWR BTN TO PCH DIRECTLY
RB : PWR BTN TO PCH VIA EC



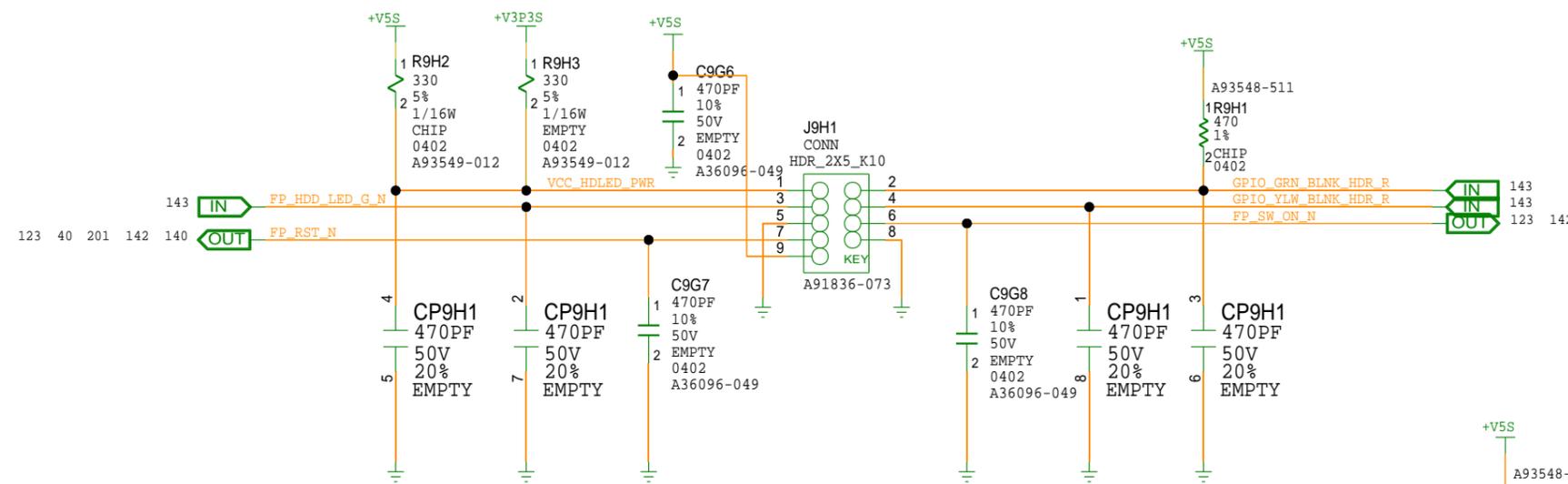
DESIGN NOTE:

HARD DRIVE STATUS LED CTRL



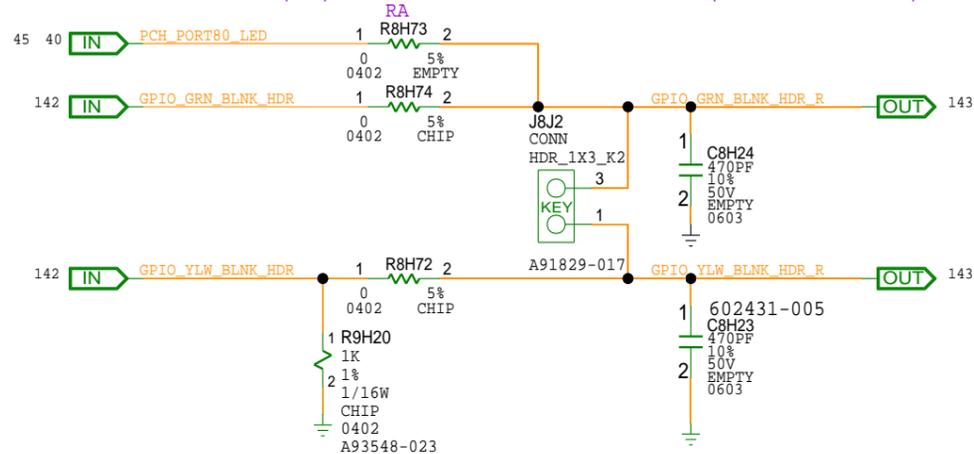
MODULE REV DETAILS

MODULE NAME	REV	DATE



BOM NOTE:

DEFAULT EMPTY: STUFF 0 OHM RES (RA) FOR PCH PORT80 LED FEATURE (TDE EXPERIMENT)

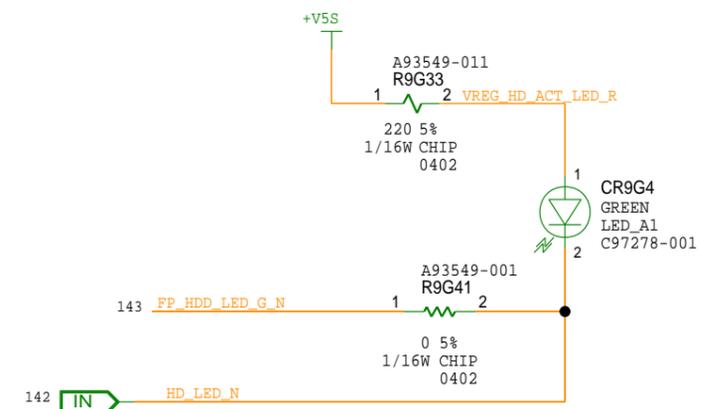
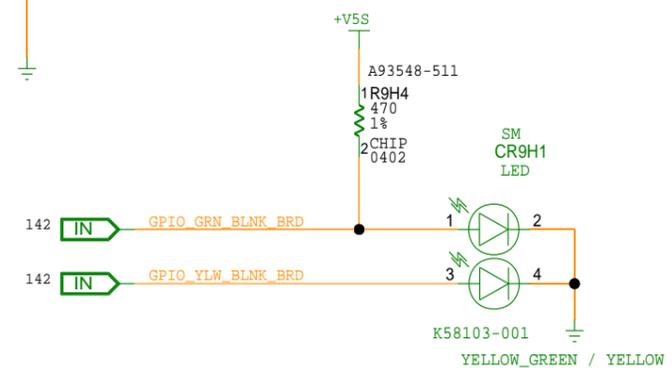


DESIGN NOTE:

S0: GREEN LIGHT
S3: YELLOW LIGHT

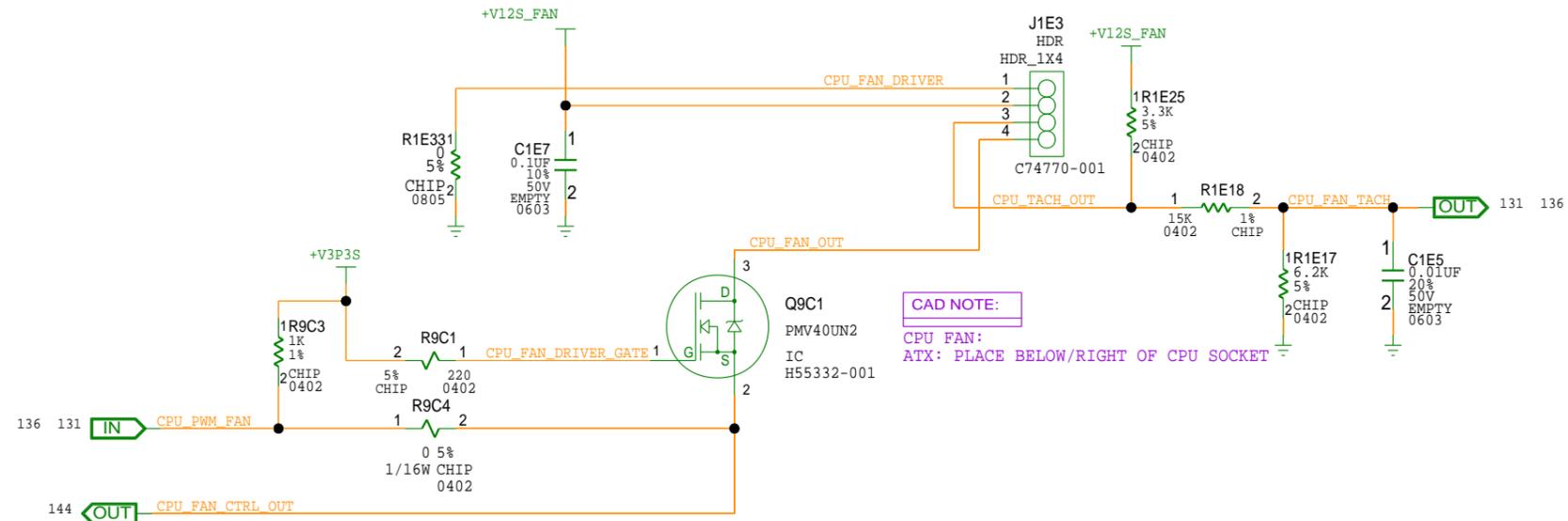
CAD NOTE:

SILKSCREEN ON BRD: S0 = GREEN LIGHT, S3 = YELLOW LIGHT

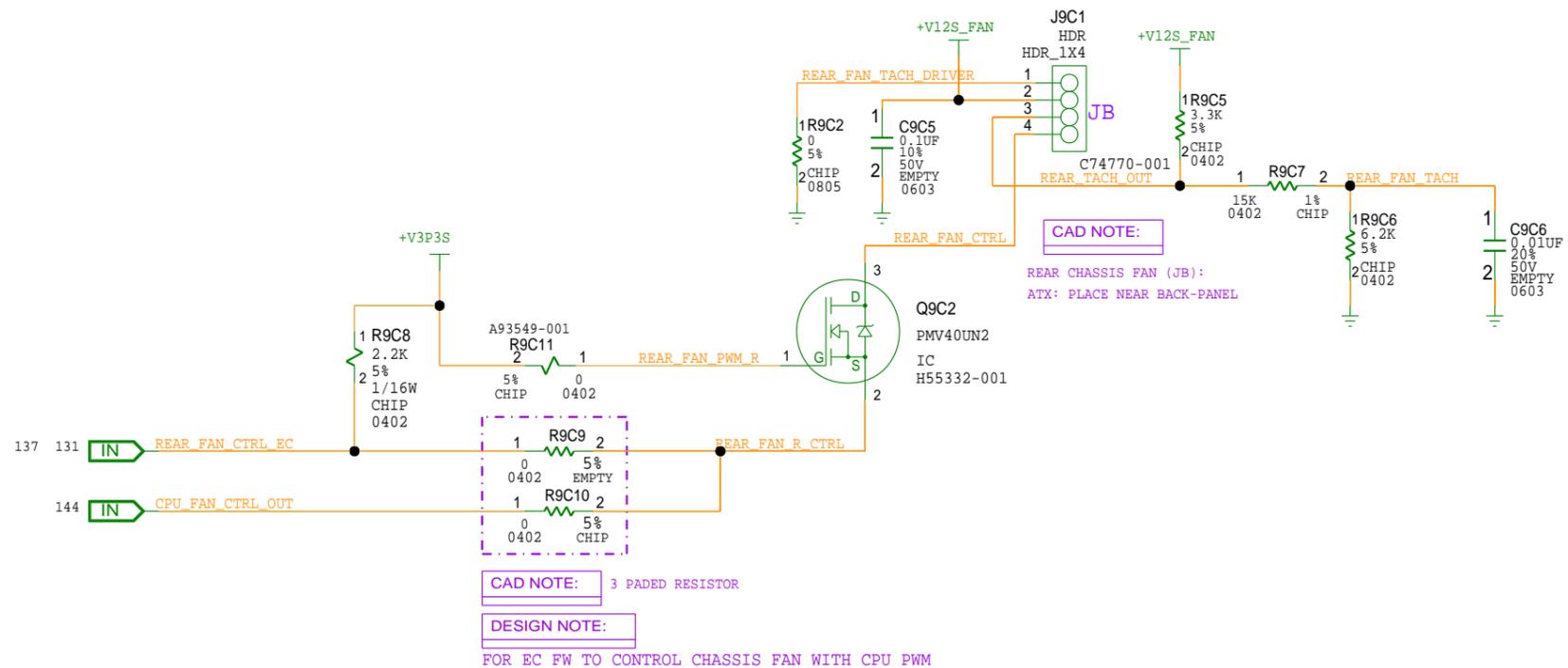


MODULE REV DETAILS		
MODULE NAME	REV	DATE

CPU FAN HEADER

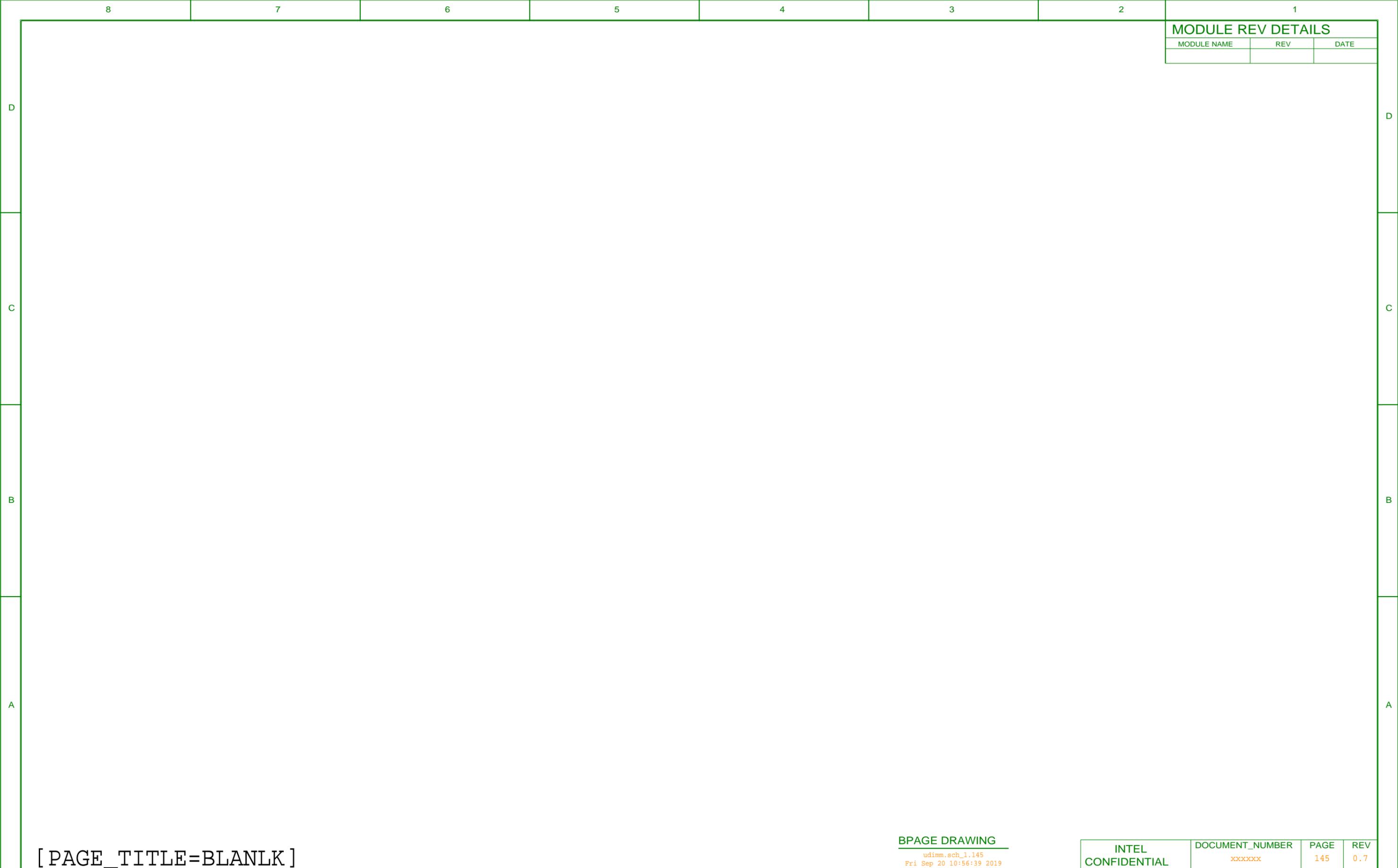


REAR CHASSIS FAN HEADER



MODULE REV DETAILS

MODULE NAME	REV	DATE



[PAGE_TITLE=BLANLK]

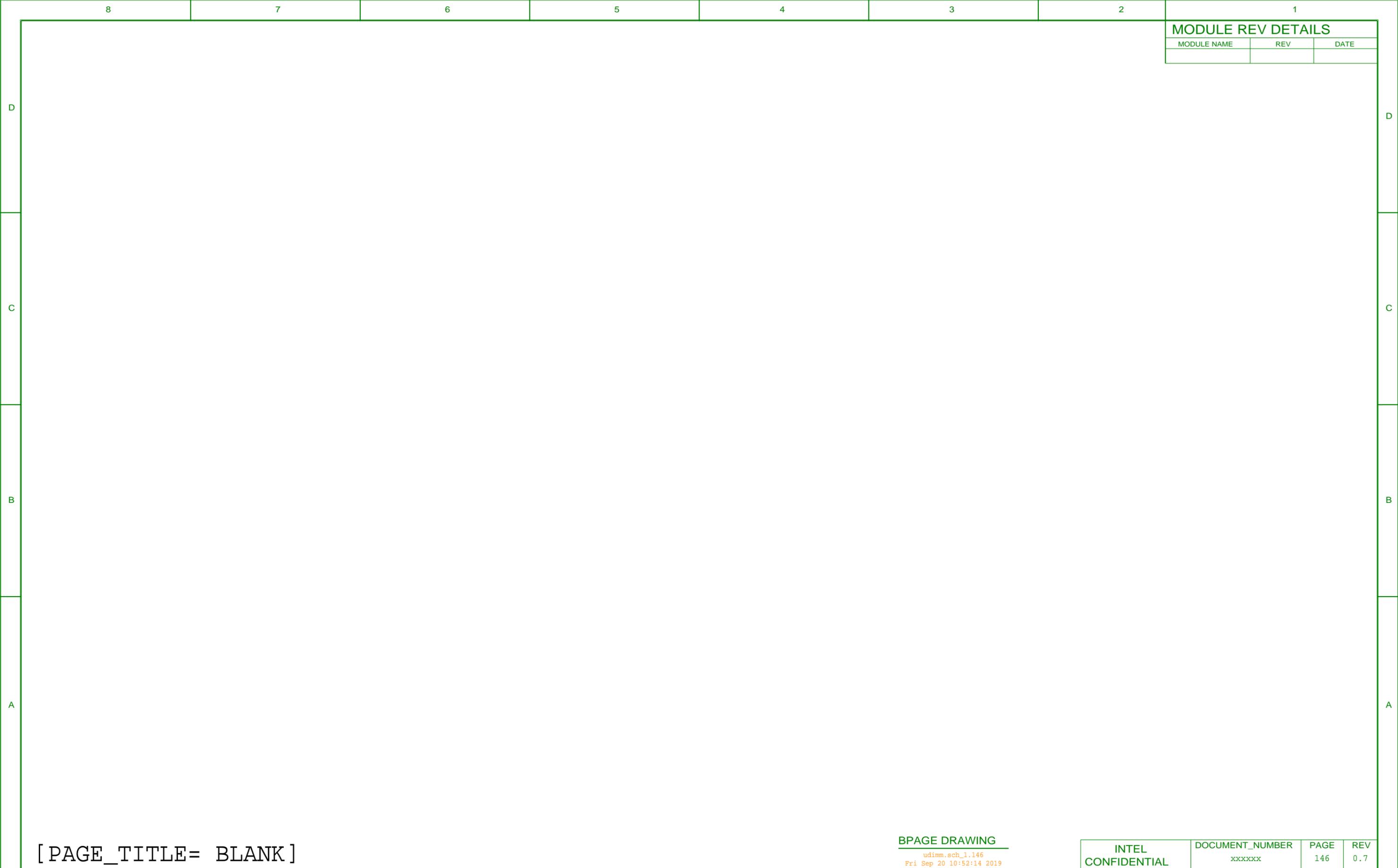
BPAGE DRAWING

udimm.sch_1.145
Fri Sep 20 10:56:39 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 145	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE



[PAGE_TITLE= BLANK]

BPAGE DRAWING

udimm.sch_1.146
Fri Sep 20 10:52:14 2019

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MODULE REV DETAILS

MODULE NAME	REV	DATE

DESIGN NOTE:

PB MOUNTING HOLE

STF_MTG_HOLE
EMPTY
MH9F1
MTG_HOLE
NC9 9
GND=1,2,3,4,5,6,7,8
G39082-001

STF_MTG_HOLE
EMPTY
MH9H1
MTG_HOLE
NC9 9
GND=1,2,3,4,5,6,7,8
G39082-001

STF_MTG_HOLE
EMPTY
MH5F1
MTG_HOLE
NC9 9
GND=1,2,3,4,5,6,7,8
G39082-001

STF_MTG_HOLE
EMPTY
MH1H1
MTG_HOLE
NC9 9
GND=1,2,3,4,5,6,7,8
G39082-001

STF_MTG_HOLE
EMPTY
MH9A1
MTG_HOLE
NC9 9
GND=1,2,3,4,5,6,7,8
G39082-001

STF_MTG_HOLE
EMPTY
MH7A1
MTG_HOLE
NC9 9
GND=1,2,3,4,5,6,7,8
G39082-001

STF_MTG_HOLE
EMPTY
MH5H1
MTG_HOLE
NC9 9
GND=1,2,3,4,5,6,7,8
G39082-001

STF_MTG_HOLE
EMPTY
MH5A1
MTG_HOLE
NC9 9
GND=1,2,3,4,5,6,7,8
G39082-001

STF_MTG_HOLE
EMPTY
MH1B1
MTG_HOLE
NC9 9
GND=1,2,3,4,5,6,7,8
G39082-001

STF_MTG_HOLE
EMPTY
MH1F1
MTG_HOLE
NC9 9
GND=1,2,3,4,5,6,7,8
G39082-001

LB6H1

LABEL_PBF_2LI



2LI

LB5G2

LABEL_JEDEC_E1



LB5G1

LABEL_JEDEC_B4



MODULE REV DETAILS

MODULE NAME	REV	DATE

D

D

C

C

B

B

A

A

[PAGE_TITLE= BLANK]

BPAGE DRAWING

udimm.sch_1.148
Fri Sep 20 11:05:34 2019

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8

7

6

5

4

3

2

1

8

7

6

5

4

3

2

1

MODULE REV DETAILS

MODULE NAME	REV	DATE



[PAGE_TITLE= BLANK]

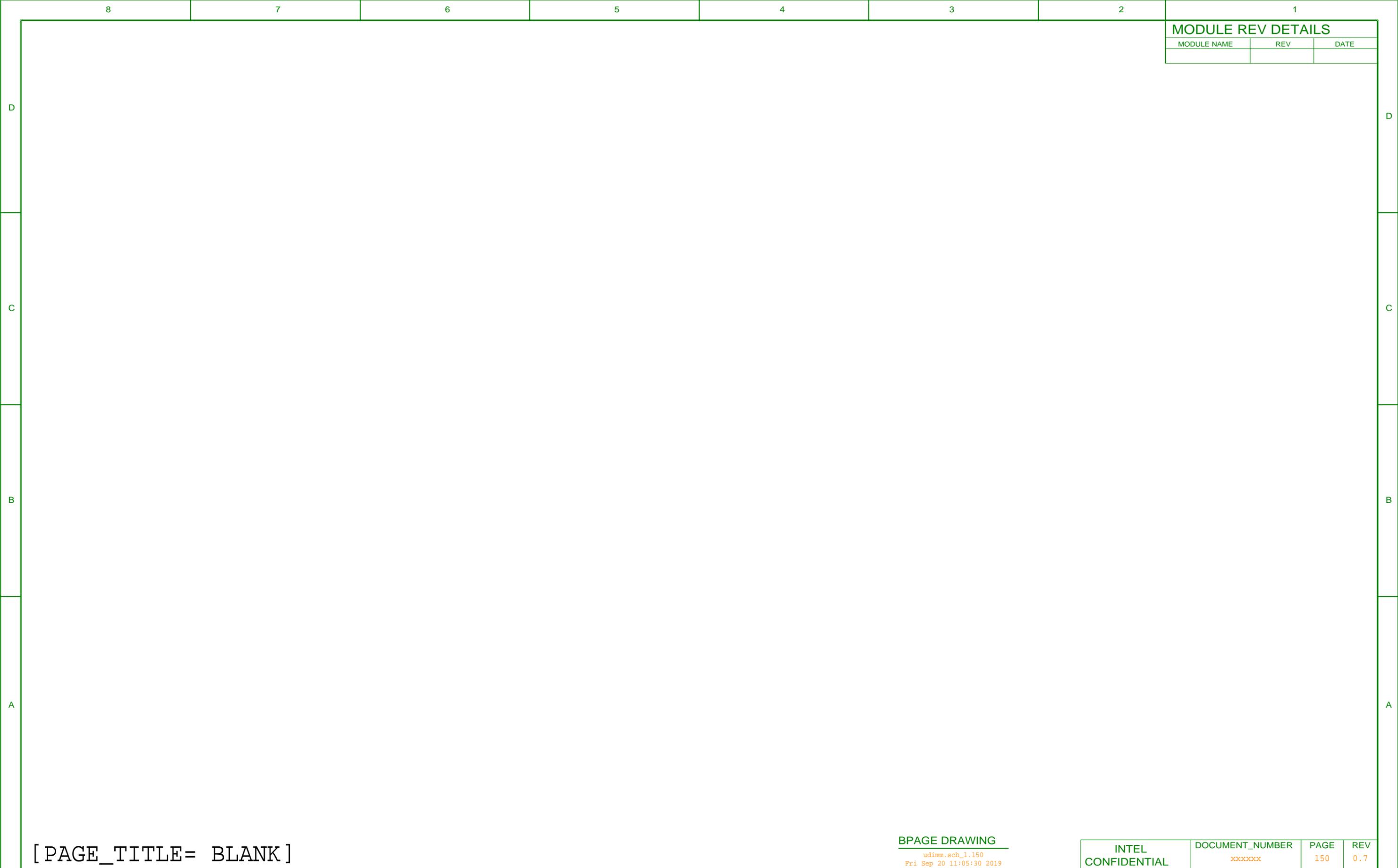
BPAGE DRAWING

udimm.sch_1.149
Fri Sep 20 11:05:28 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 149	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE



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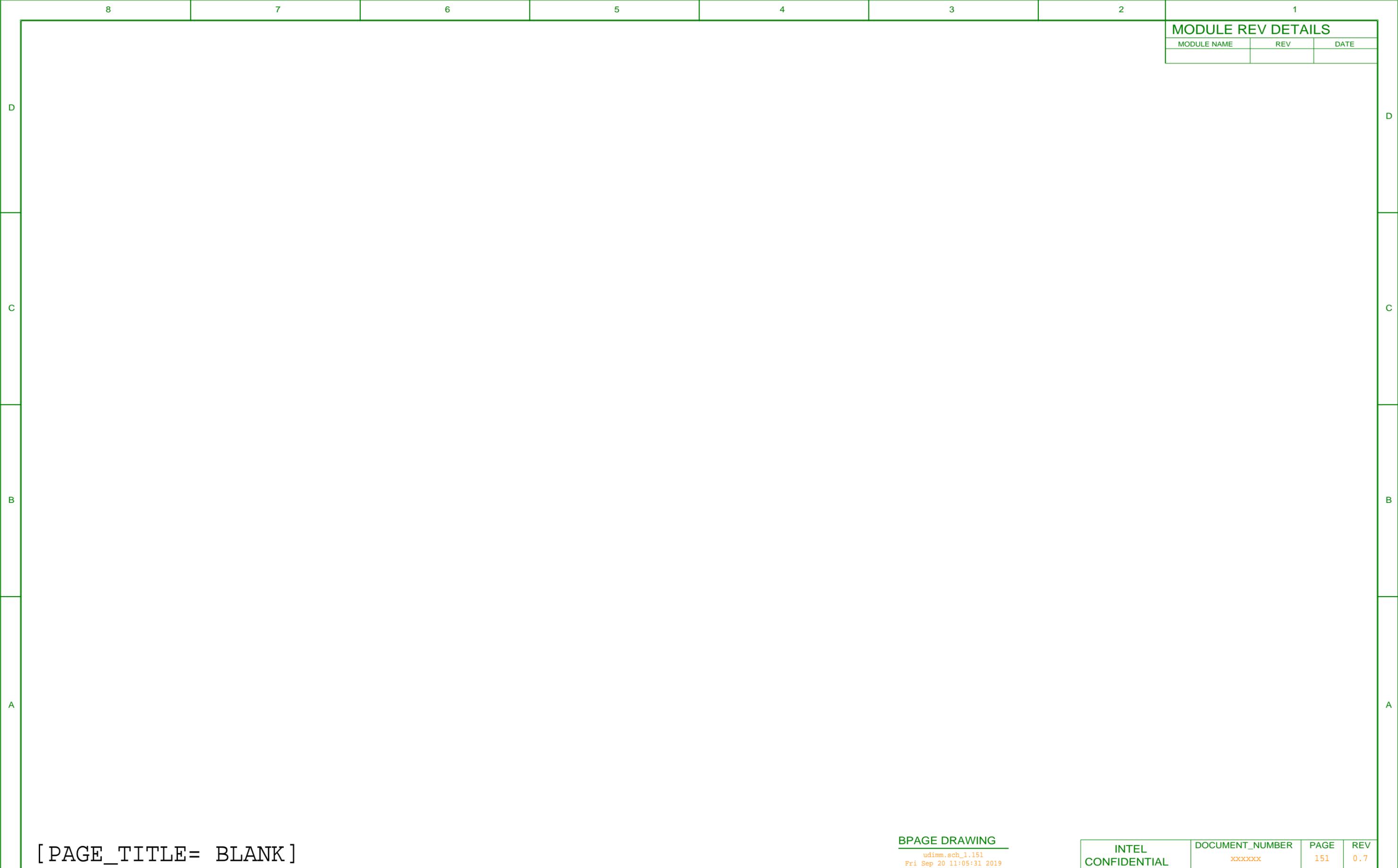
BPAGE DRAWING

udimm.sch_1.150
Fri Sep 20 11:05:30 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 150	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE



[PAGE_TITLE= BLANK]

BPAGE DRAWING

udimm.sch_1.151
Fri Sep 20 11:05:31 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 151	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE



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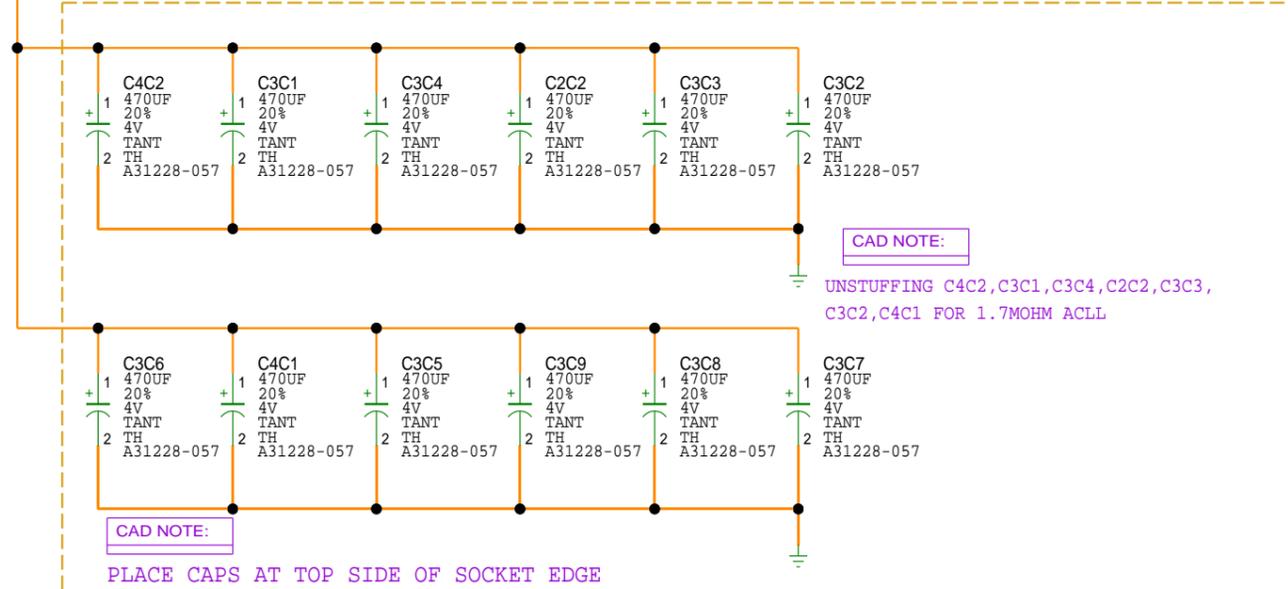
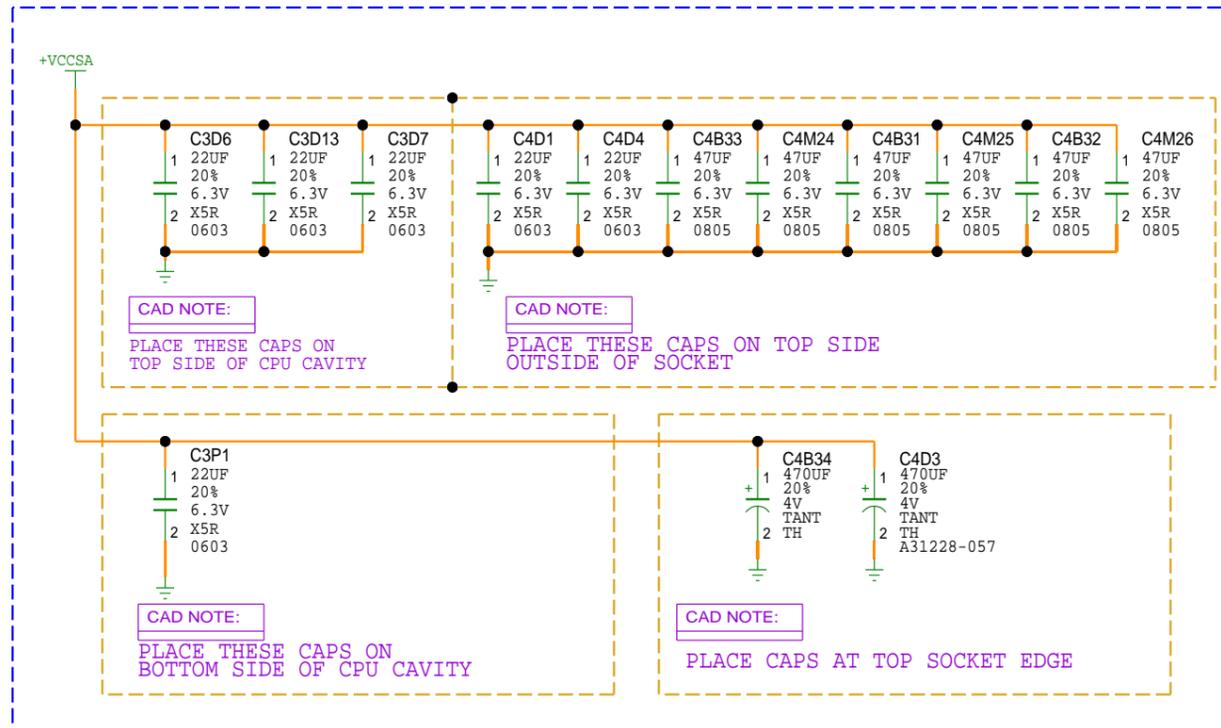
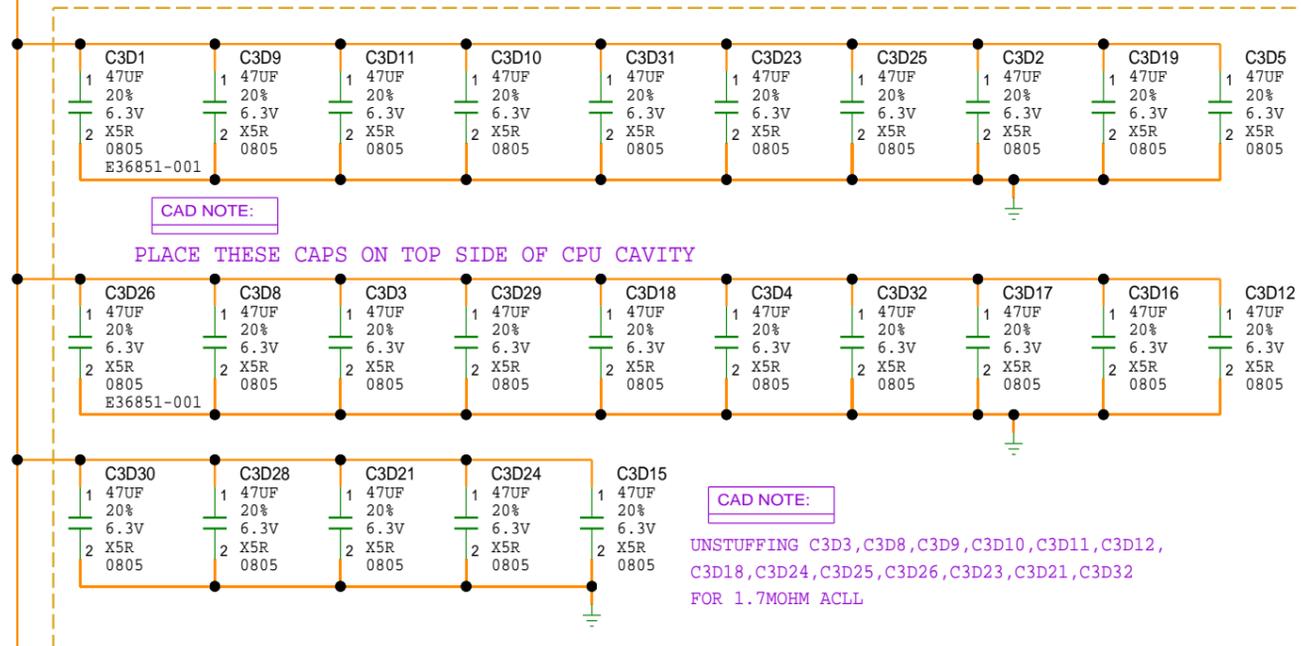
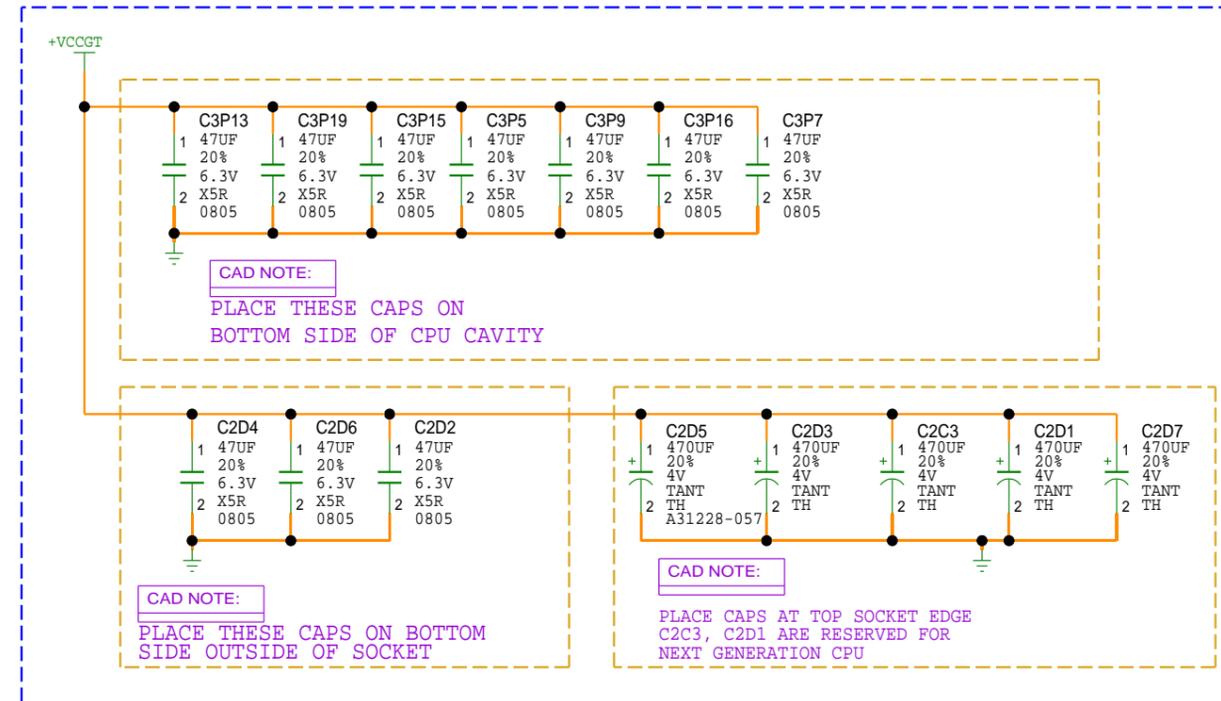
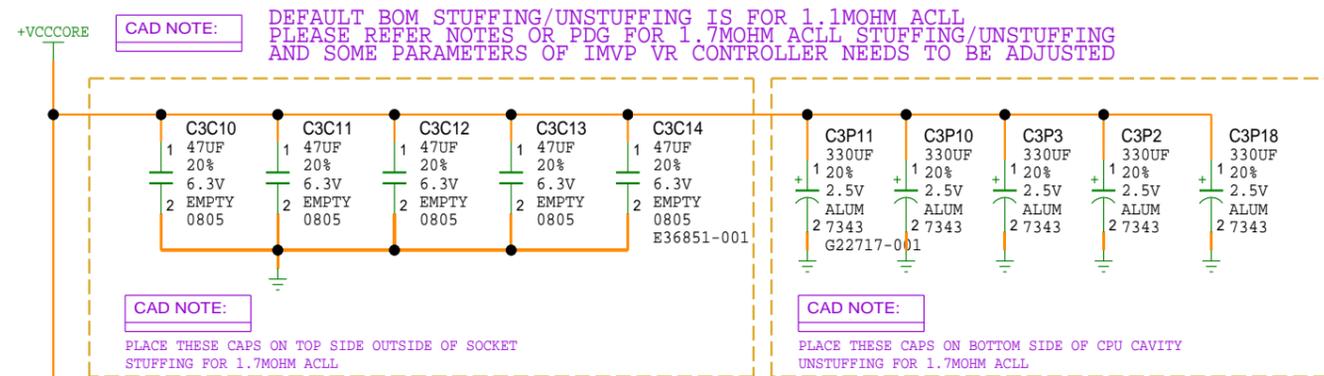
BPAGE DRAWING

udimm.sch_1.152
Fri Sep 20 11:05:32 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 152	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE



[PAGE_TITLE=CPU PD BOM-1 OF 2, VCCCORE, VCCGT, VCCSA]

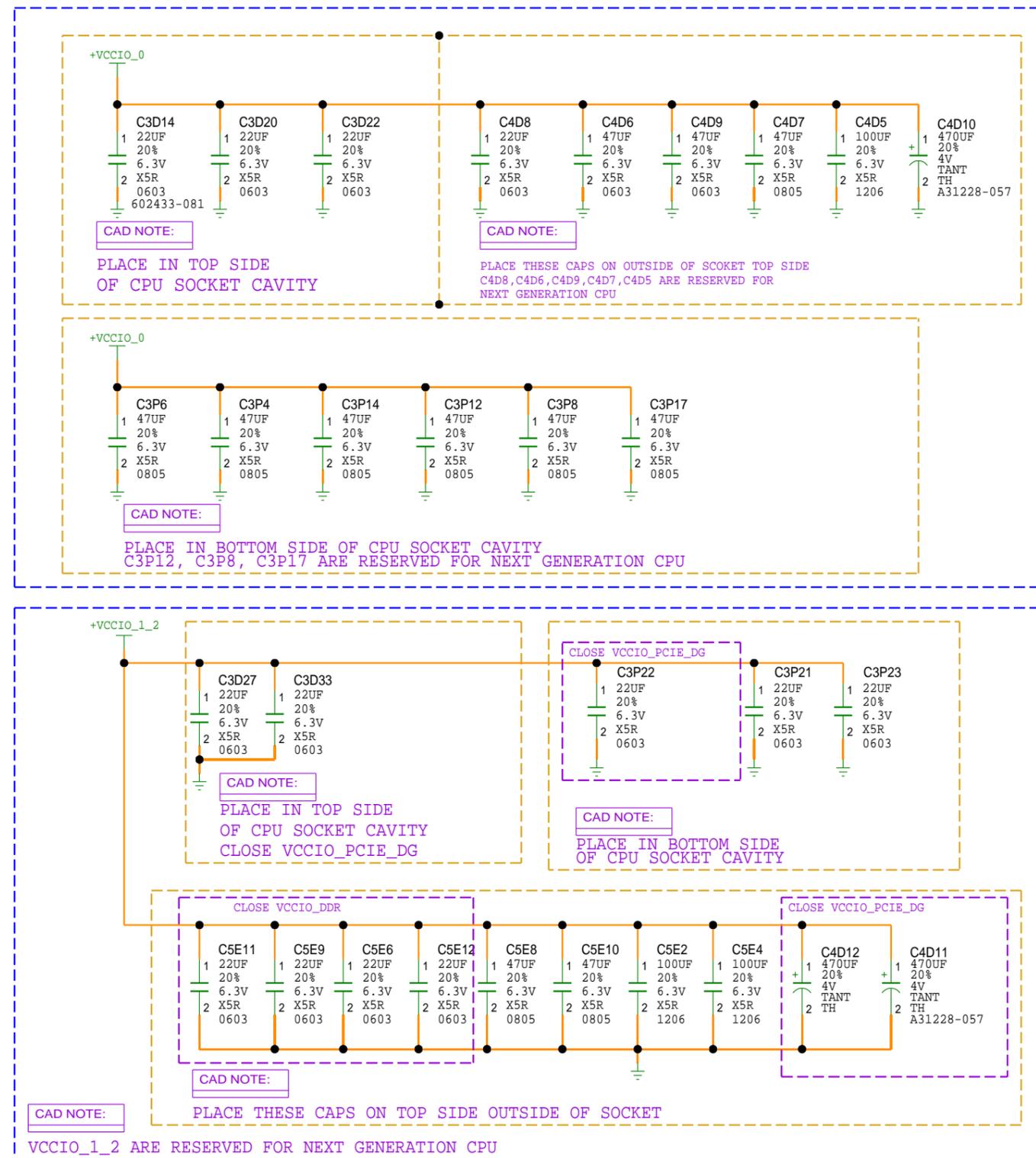
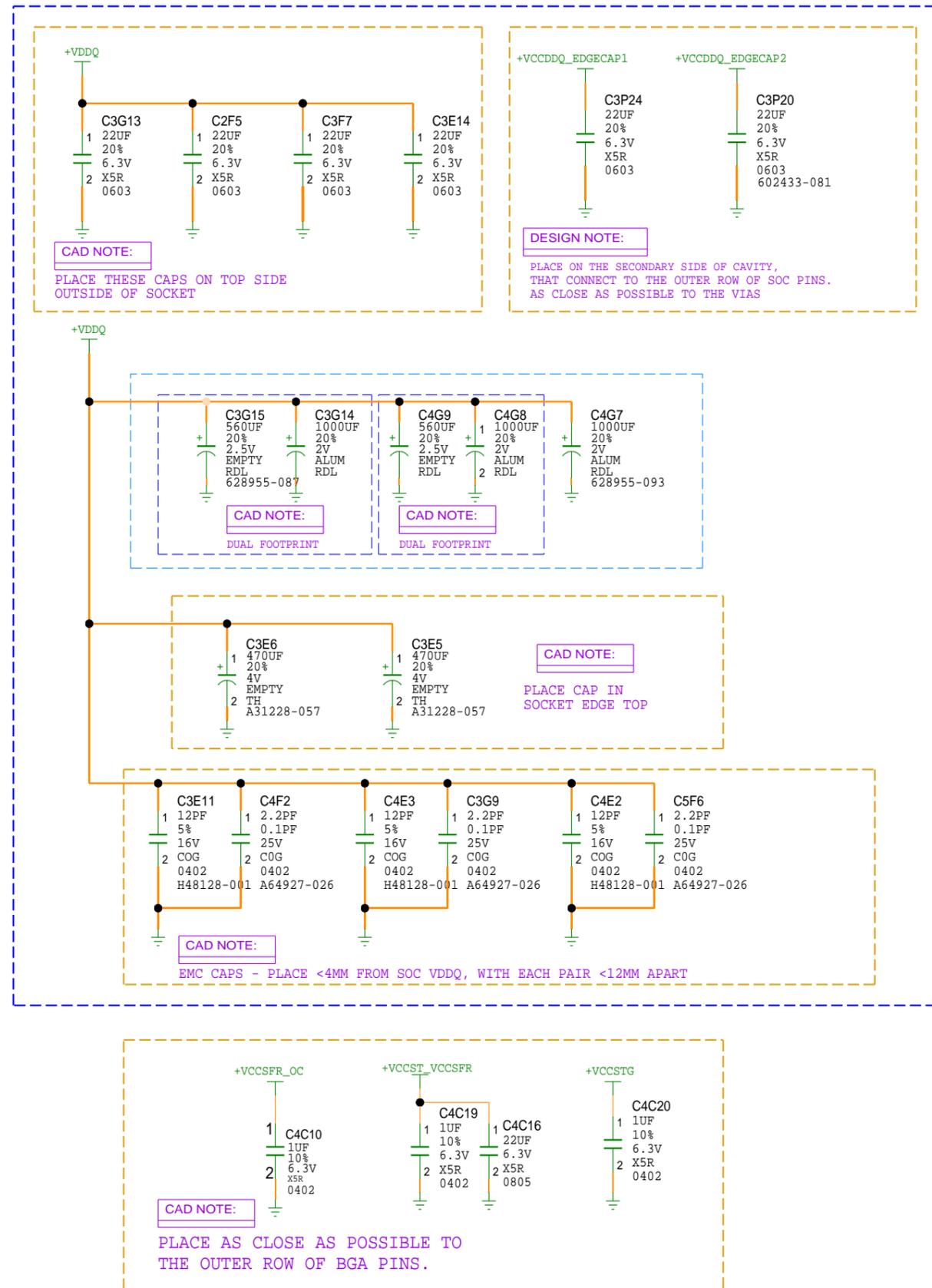
BPAGE DRAWING

udimm.sch_1.153
Fri Sep 27 16:41:37 2019

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MODULE REV DETAILS

MODULE NAME	REV	DATE



[PAGE_TITLE=CPU PD BOM-2 OF 2,VDDQ,VCCIO,VCCST_VCCSFR,VCCSFR_OC]

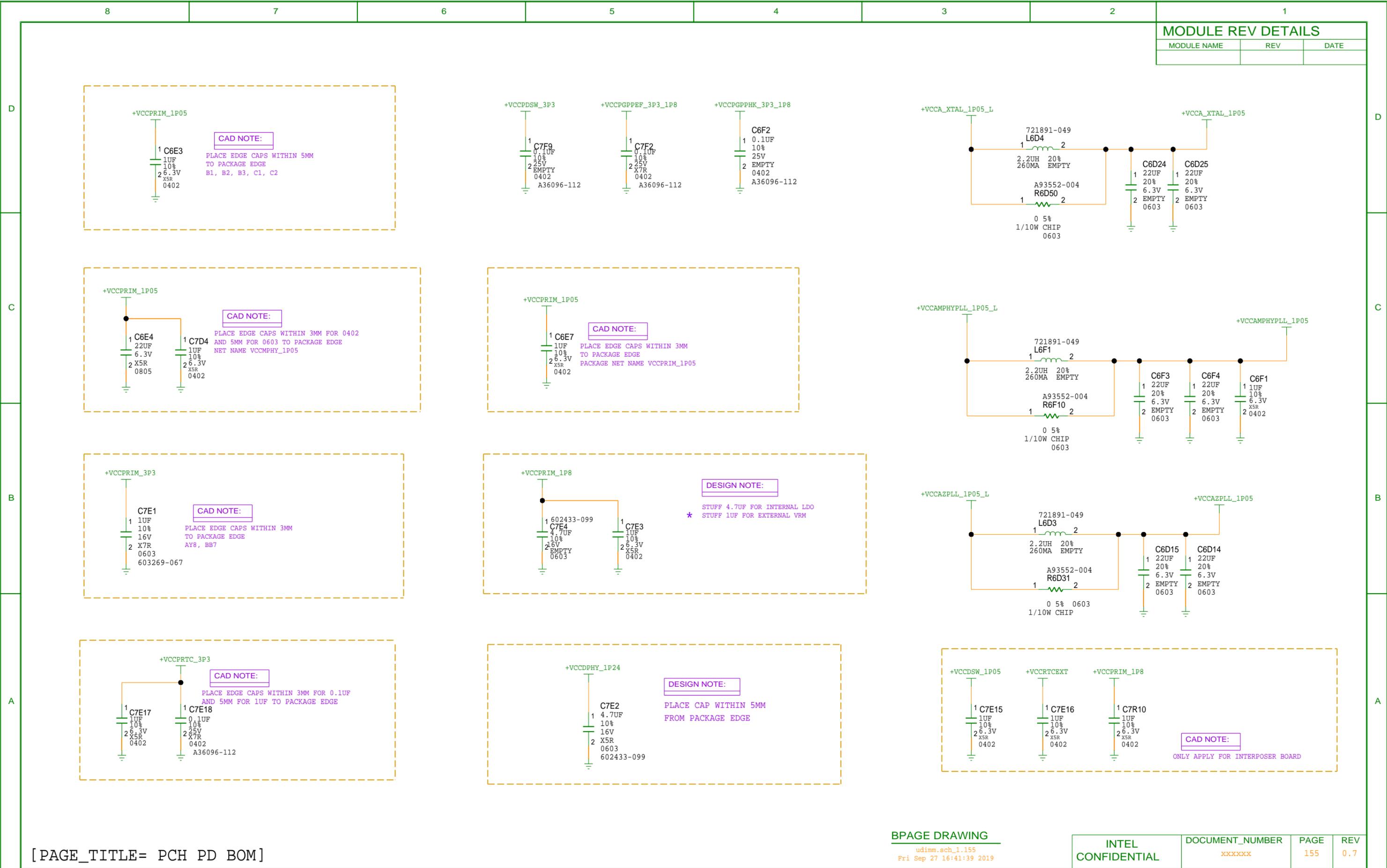
BPAGE DRAWING

udimm.sch_1.154
Fri Sep 27 16:41:38 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 154	REV 0.7
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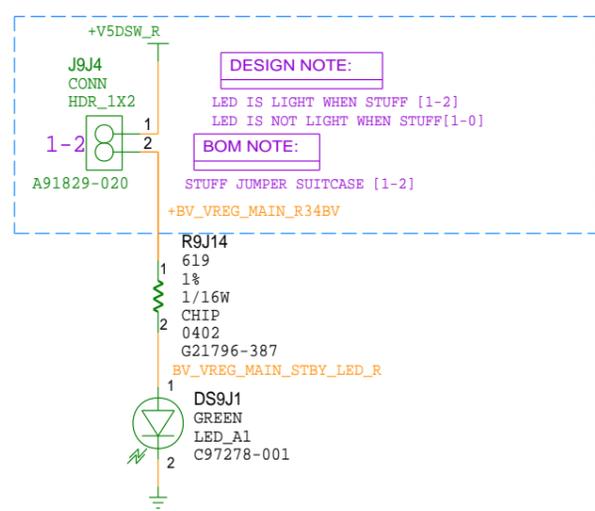
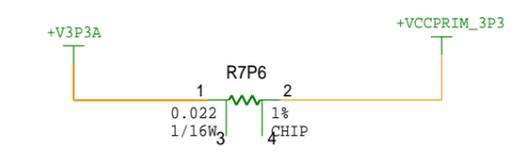
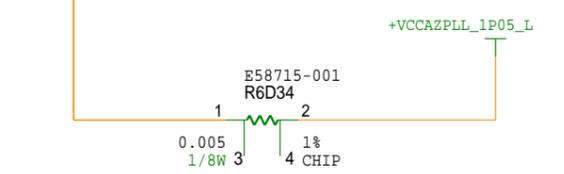
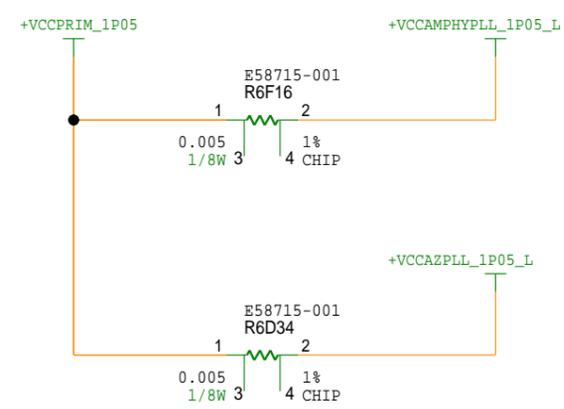
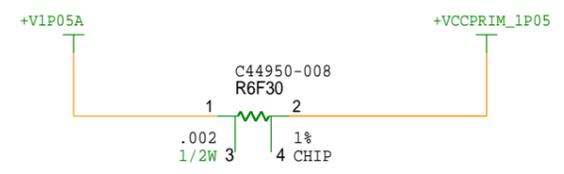
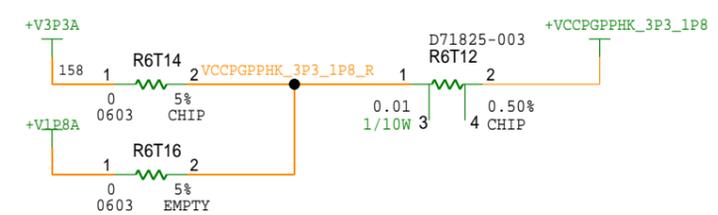
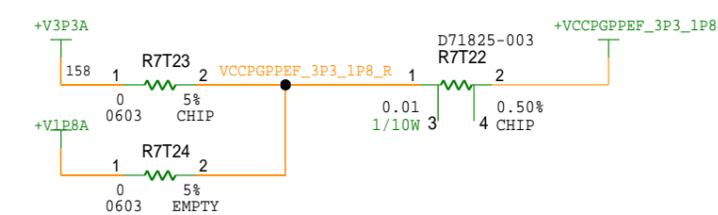
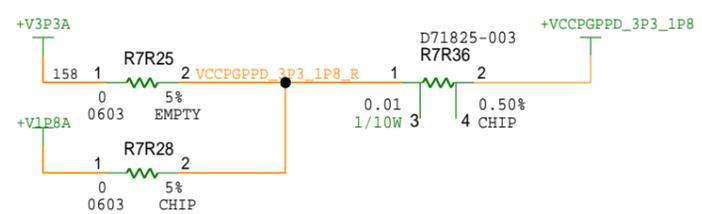
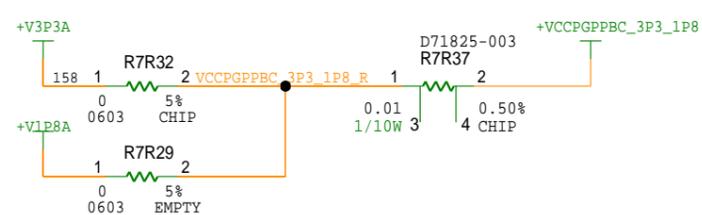
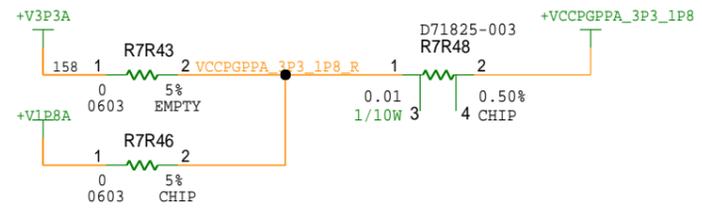
MODULE REV DETAILS

MODULE NAME	REV	DATE



MODULE REV DETAILS

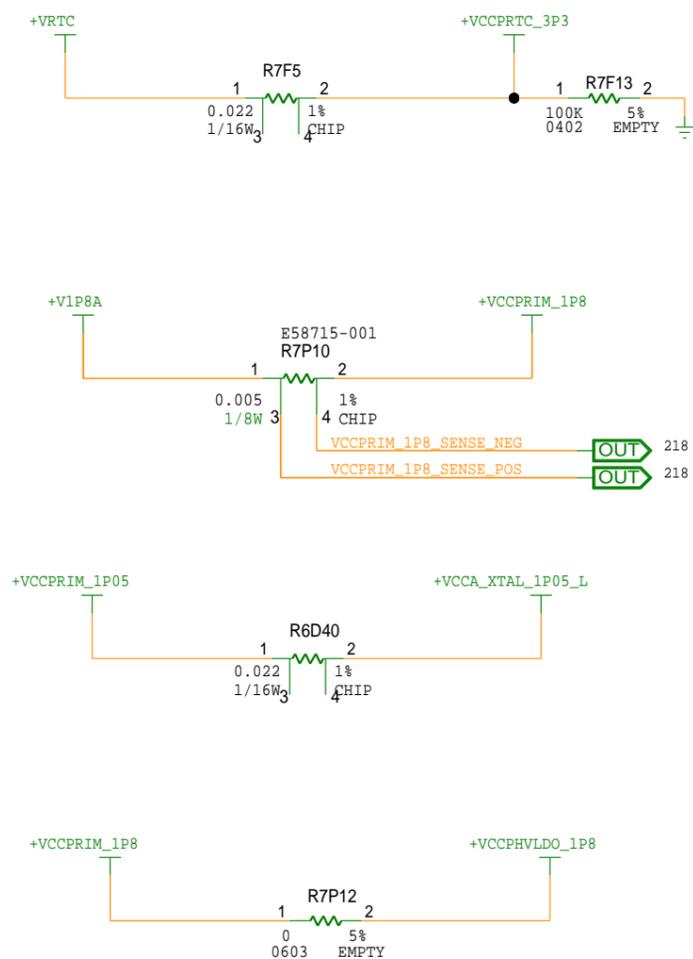
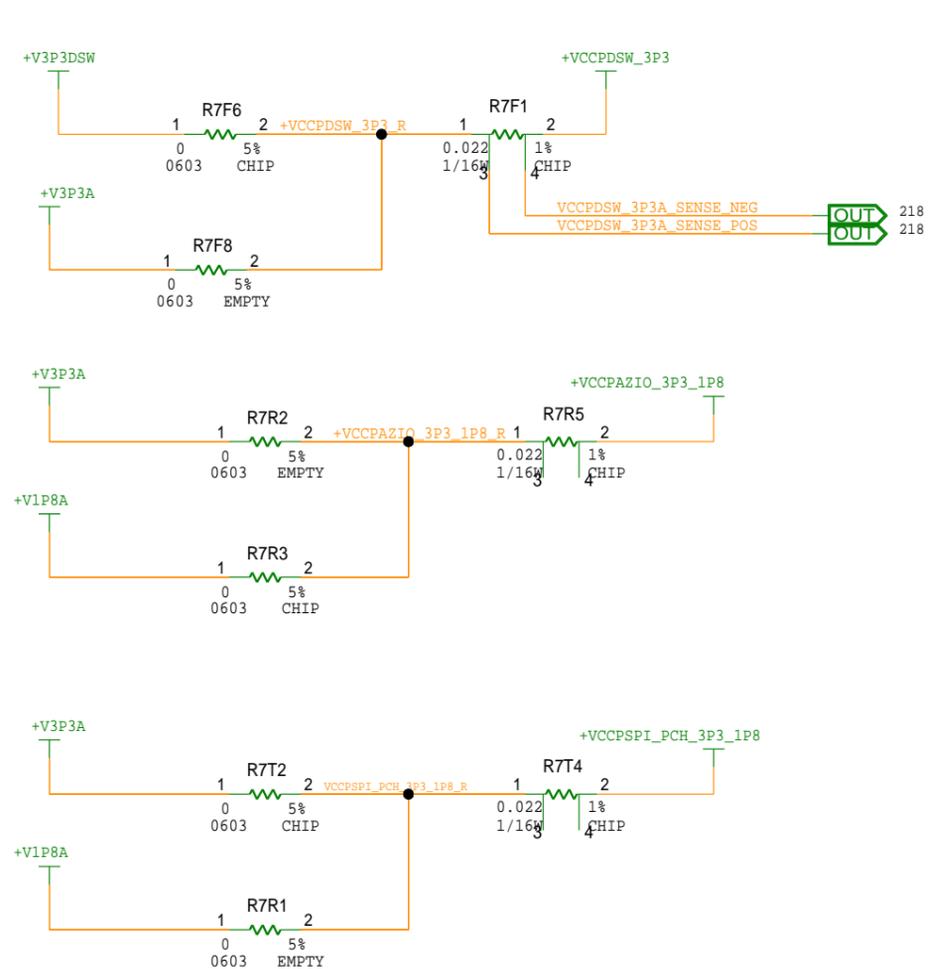
MODULE NAME	REV	DATE



MODULE REV DETAILS

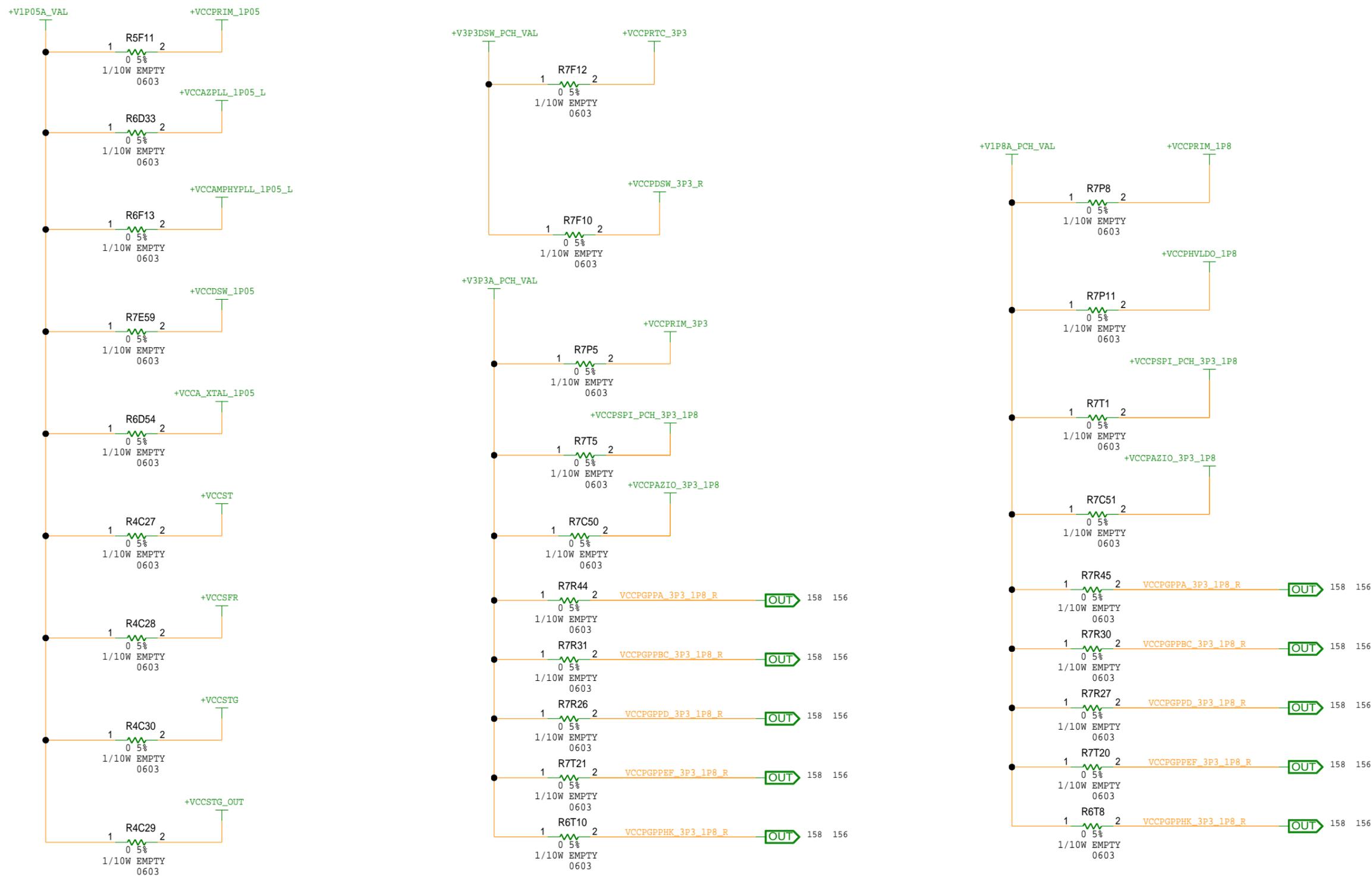
MODULE NAME	REV	DATE

PCH DERIVED RAILS



MODULE REV DETAILS

MODULE NAME	REV	DATE



[PAGE_TITLE=RESERVED FOR VALIDATION]

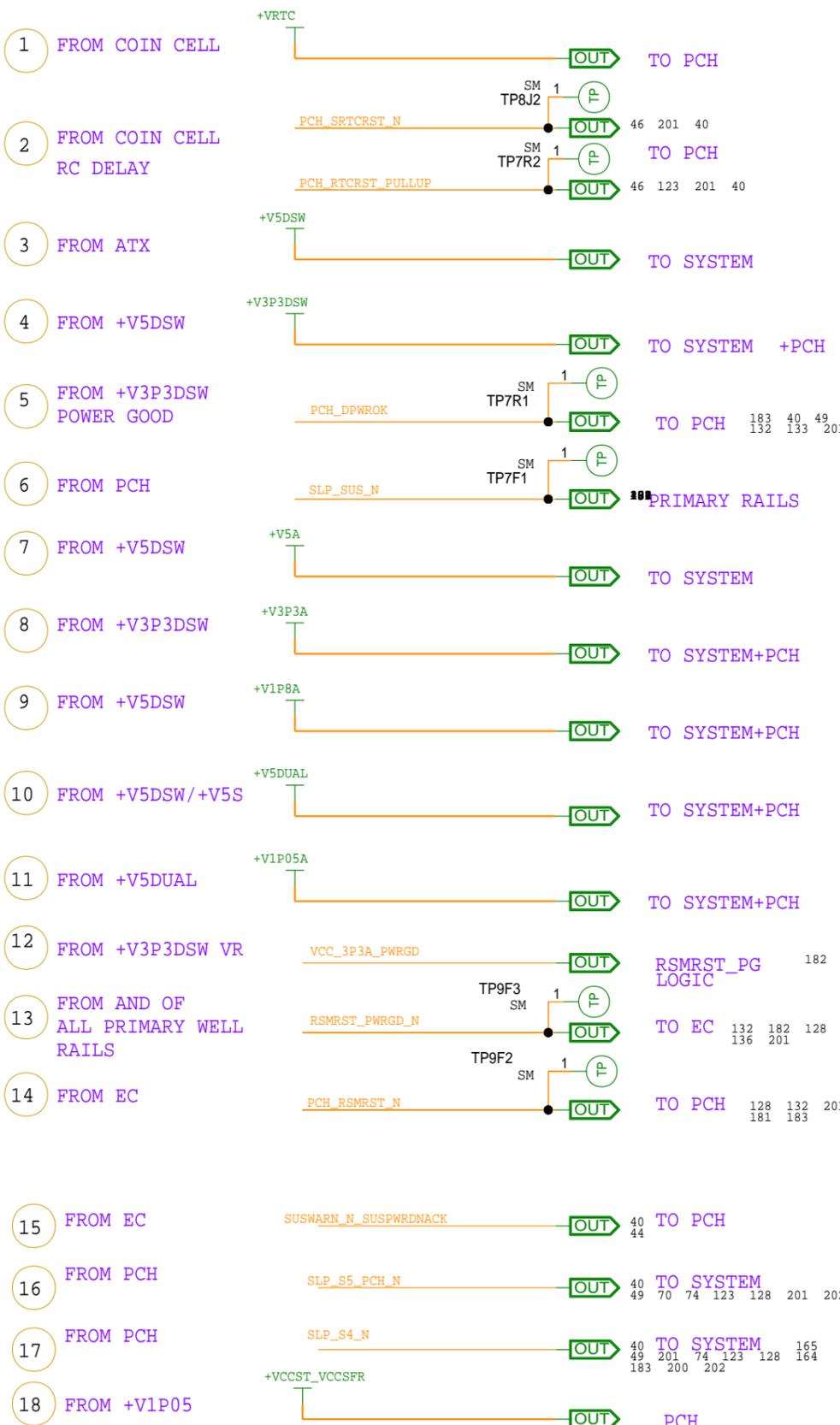
BPAGE DRAWING

udimm.sch_1.158
Fri Sep 27 16:41:43 2019

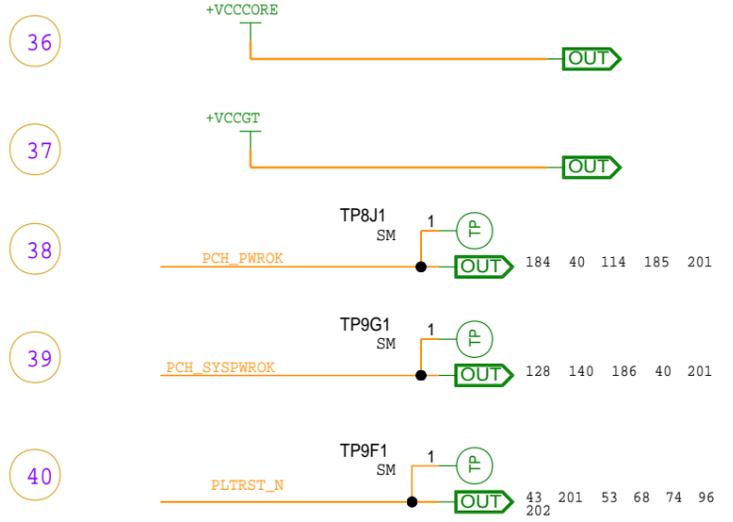
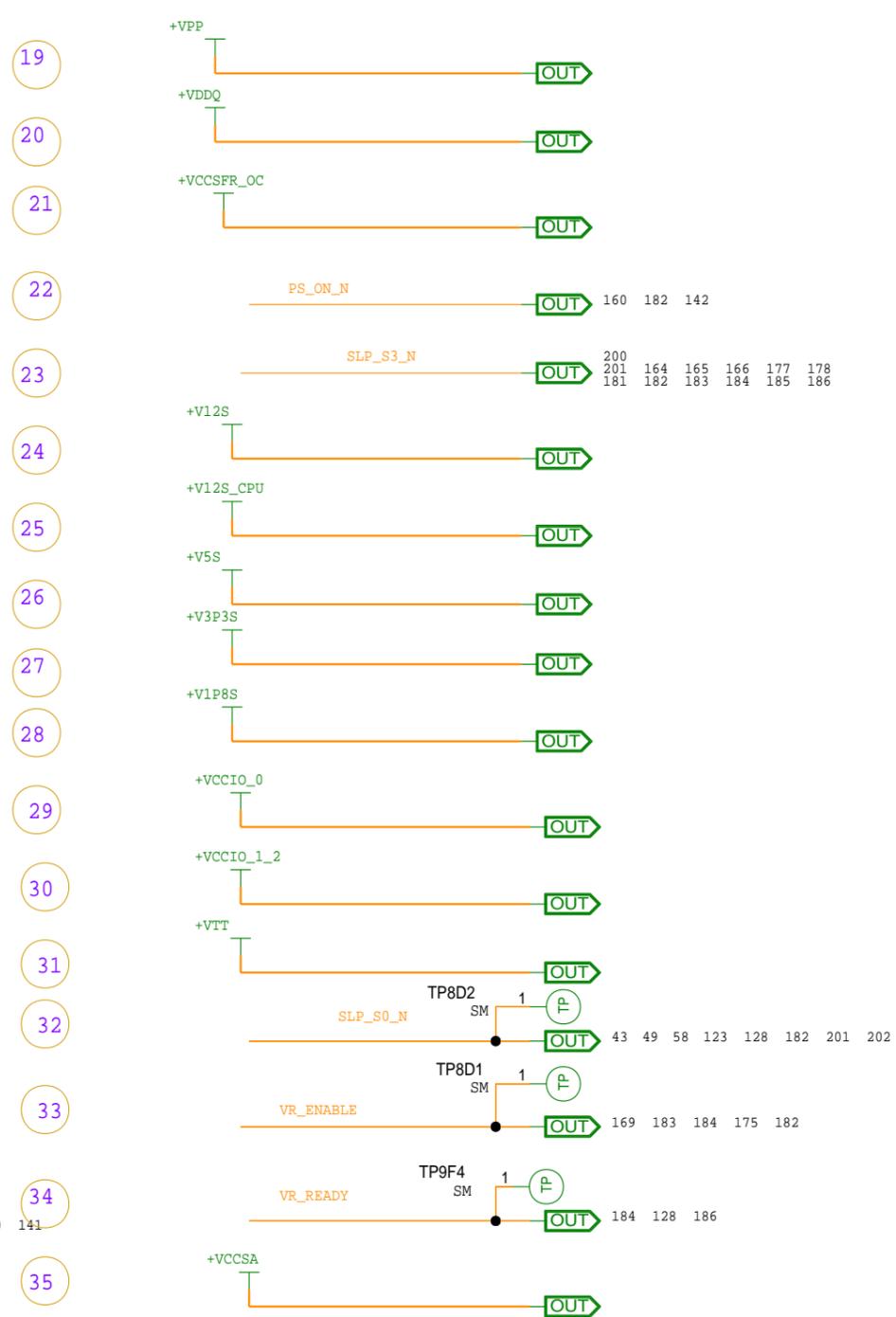
INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 158	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE



TEXT TO BE UPDATED



NOTE: +VCCIO_1_2 IS REQUIRED TO SUPPORT FORWARD COMPATIBILITY WITH 2021 NEXT. GEN S-SERIES CPU ON CML-S BASED BOARDS. +VCCIO_1_2 IS NOT REQUIRED IF BOARD IS DESIGNED TO SUPPORT CML-S CPU ONLY.

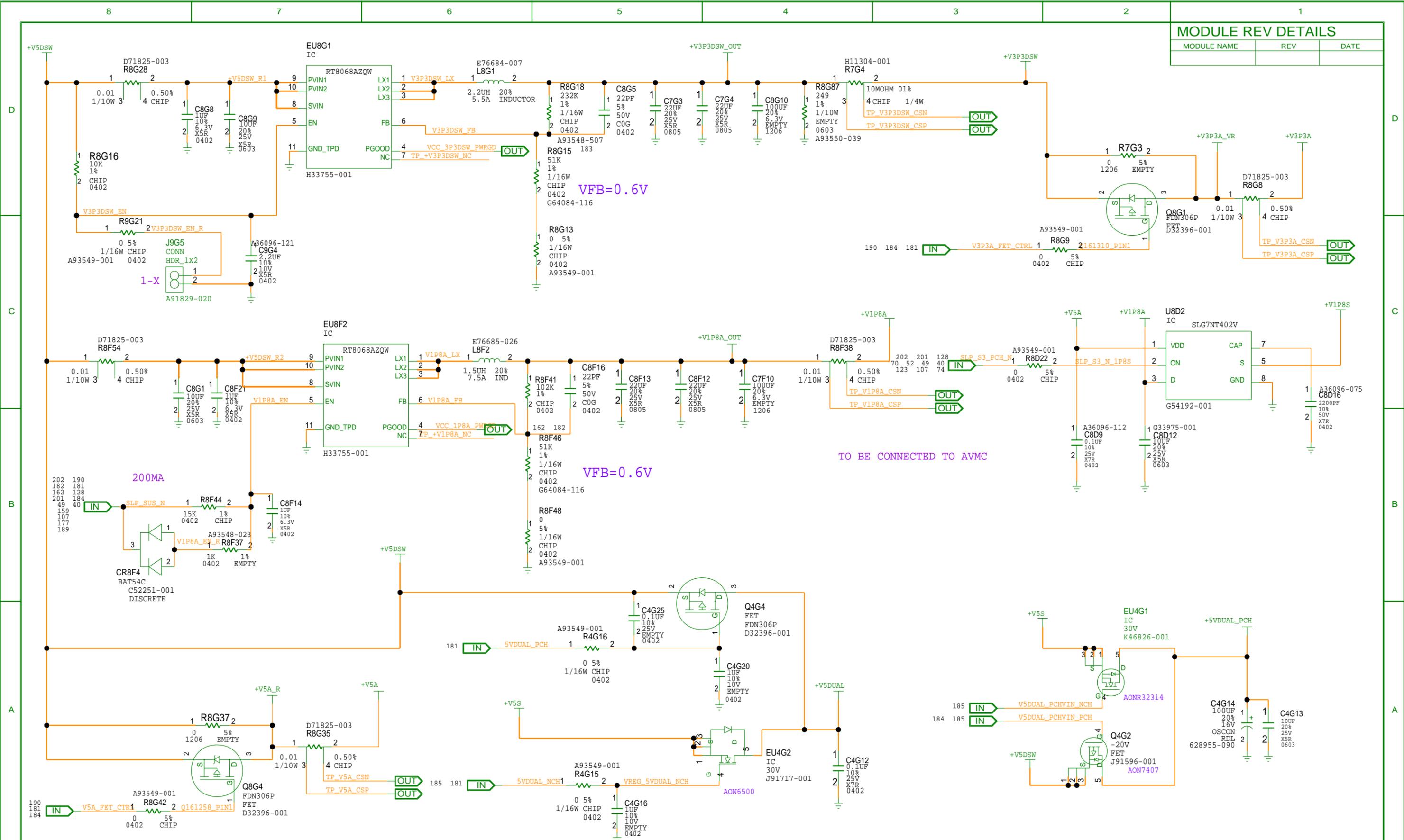
[PAGE_TITLE= PD POWER SEQ FLOW, TEST POINTS]

BPAGE DRAWING
udimm.sch_1.159
Fri Sep 27 16:41:44 2019

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MODULE REV DETAILS

MODULE NAME	REV	DATE



VFB=0.6V

VFB=0.6V

TO BE CONNECTED TO AVMC

BPAGE DRAWING

udimm.sch_1.161
Fri Sep 27 16:41:46 2019

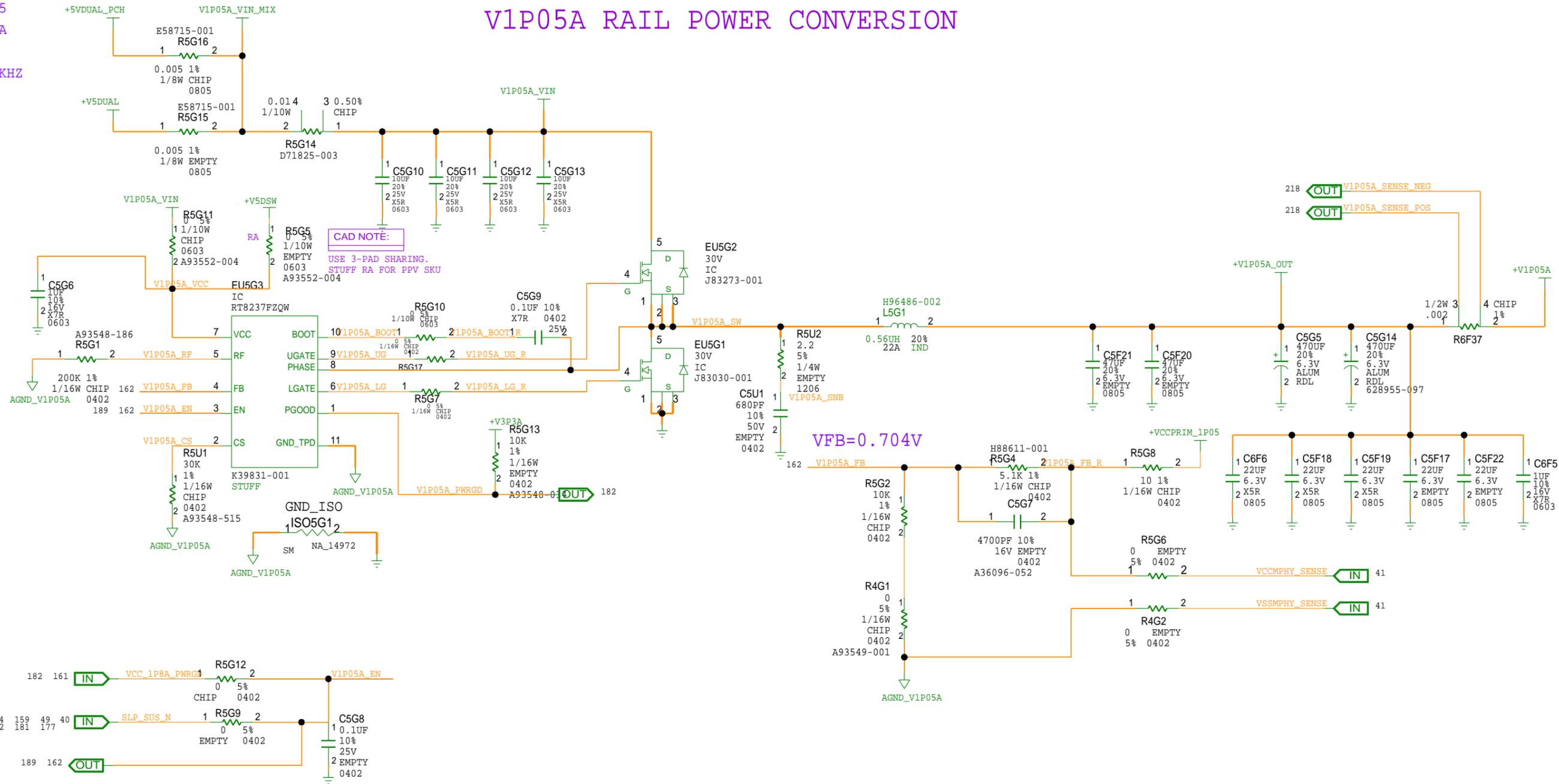
[PAGE_TITLE= 3.3V, 5V AND 1.8V GENERATION]

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MODULE REV DETAILS		
MODULE NAME	REV	DATE

RAIL : V1P05
 IOUT = 16.5A
 OCP = 20A
 SW FREQ=340KHZ

V1P05A RAIL POWER CONVERSION



CAD NOTE:
 USE 3-PAD SHARING.
 STUFF RA FOR PPV SKU

VFB=0.704V

PLACE SNUBBER CLOSE TO THE FET
 PLACE C_VCC CLOSE TO THE VR IC
 PLACE VIN CAP CLOSE TO THE CSD FET

[PAGE_TITLE=V1P05A GENERATION]

BPAGE DRAWING
 udimm.sch_1.162
 Fri Sep 27 16:41:47 2019

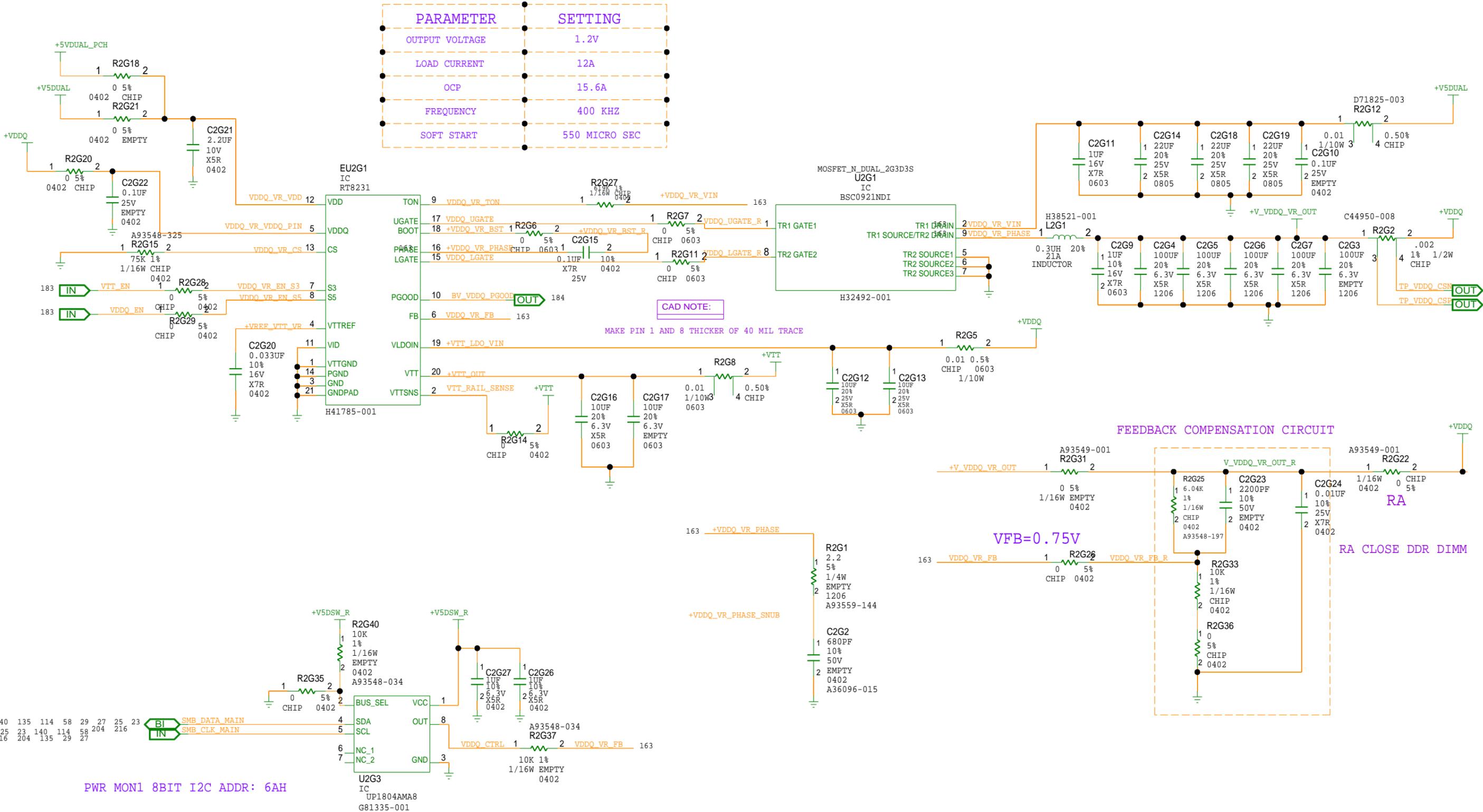
INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 162	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE

VDDQ AND VTT RAILS - POWER CONVERSION

PARAMETER	SETTING
OUTPUT VOLTAGE	1.2V
LOAD CURRENT	12A
OCV	15.6A
FREQUENCY	400 KHZ
SOFT START	550 MICRO SEC



CAD NOTE:
MAKE PIN 1 AND 8 THICKER OF 40 MIL TRACE

VFB=0.75V

RA CLOSE DDR DIMM

PWR MONI 8BIT I2C ADDR: 6AH

[PAGE_TITLE=VDDQ AND VTT GENERATION]

BPAGE DRAWING

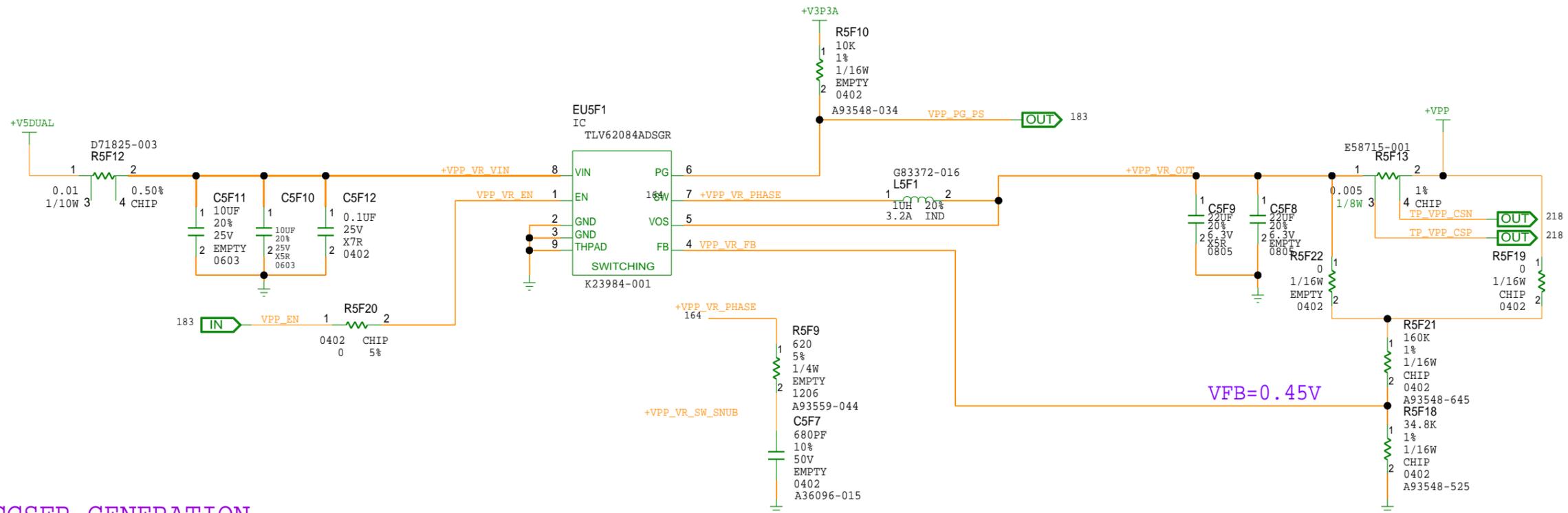
udimm.sch_1.163
Fri Sep 27 16:41:49 2019

INTEL CONFIDENTIAL	DOCUMENT NUMBER xxxxxxx	PAGE 163	REV 0.7
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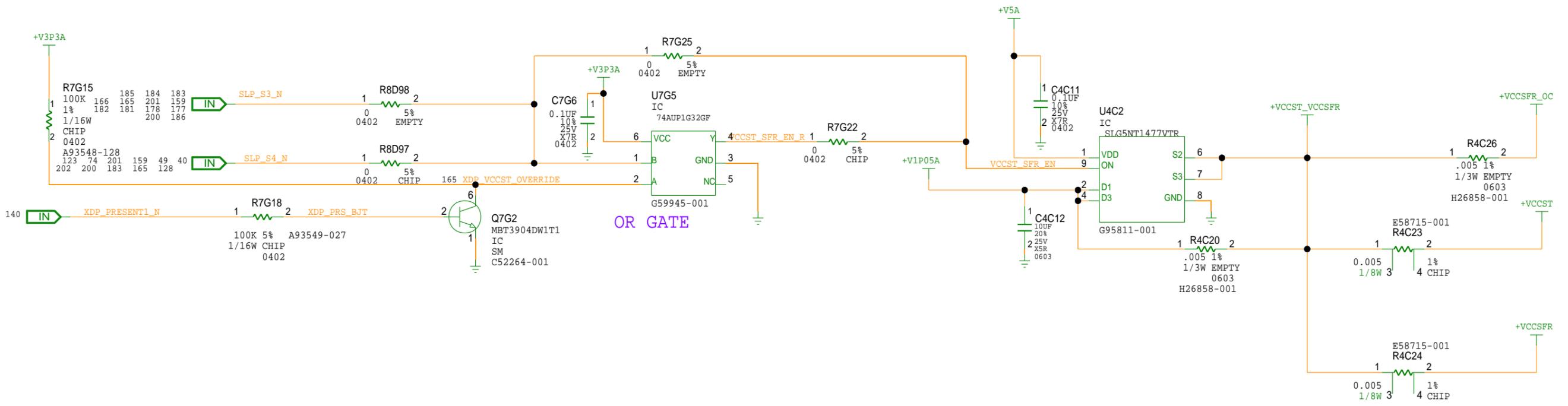
MODULE REV DETAILS		
MODULE NAME	REV	DATE

VPP 2.5V RAIL - POWER CONVERSION

RAIL : 2.5V
 IOUT = 2A
 OCP = 2.8A
 SW FREQ=1.5MHZ



VCCST & VCCSFR GENERATION



[PAGE_TITLE=VPP & VCCST_VCCSFR GENERATION]

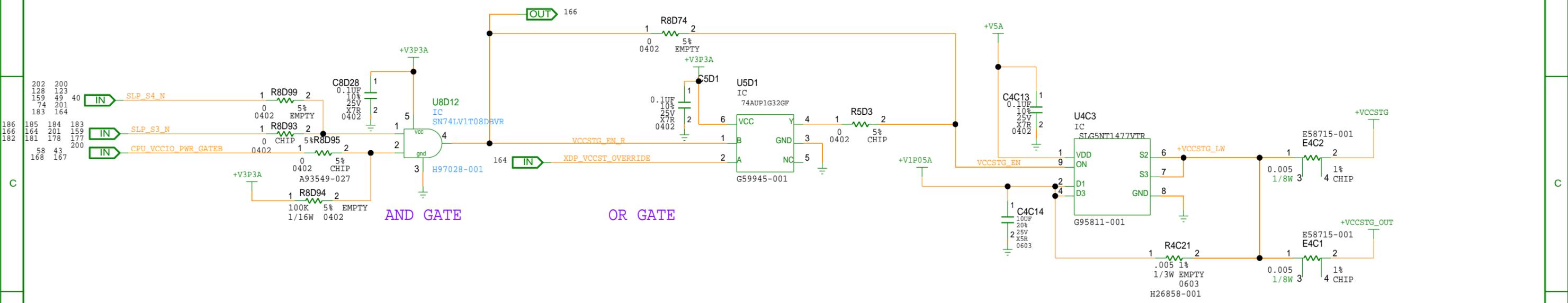
BPAGE DRAWING
 udimm.sch_1.164
 Fri Sep 27 16:41:52 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 164	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE

VCCSTG GENERATION



AND GATE

OR GATE

[PAGE_TITLE=VCCSTG

BPAGE DRAWING

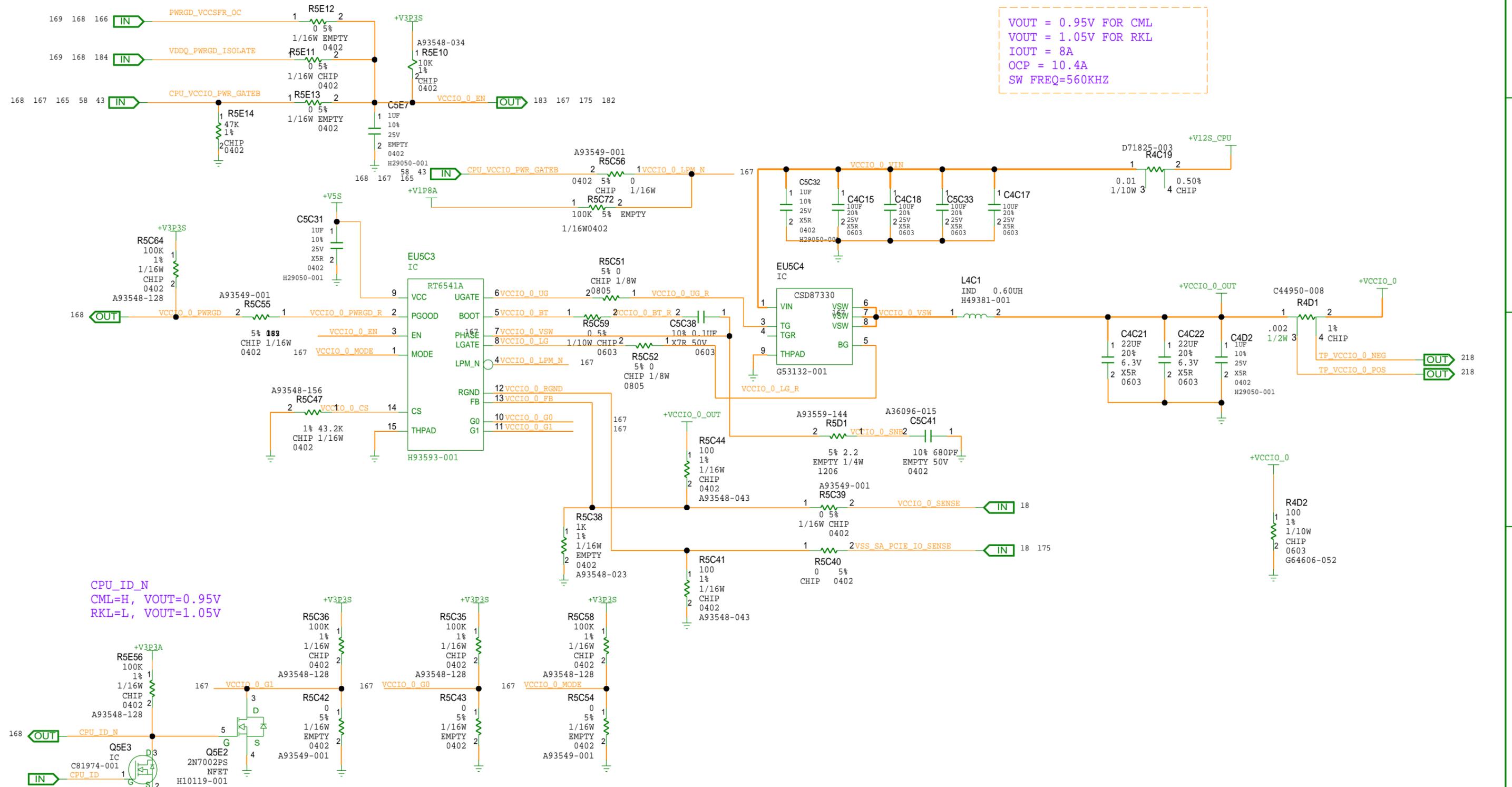
udimm.sch_1.165
Fri Sep 27 16:41:53 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 165	REV 0.7
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MODULE REV DETAILS		
MODULE NAME	REV	DATE

VCCIO_0

VOUT = 0.95V FOR CML
 VOUT = 1.05V FOR RKL
 IOU_T = 8A
 OCP = 10.4A
 SW FREQ=560KHZ



CPU_ID_N
 CML=H, VOUT=0.95V
 RKL=L, VOUT=1.05V

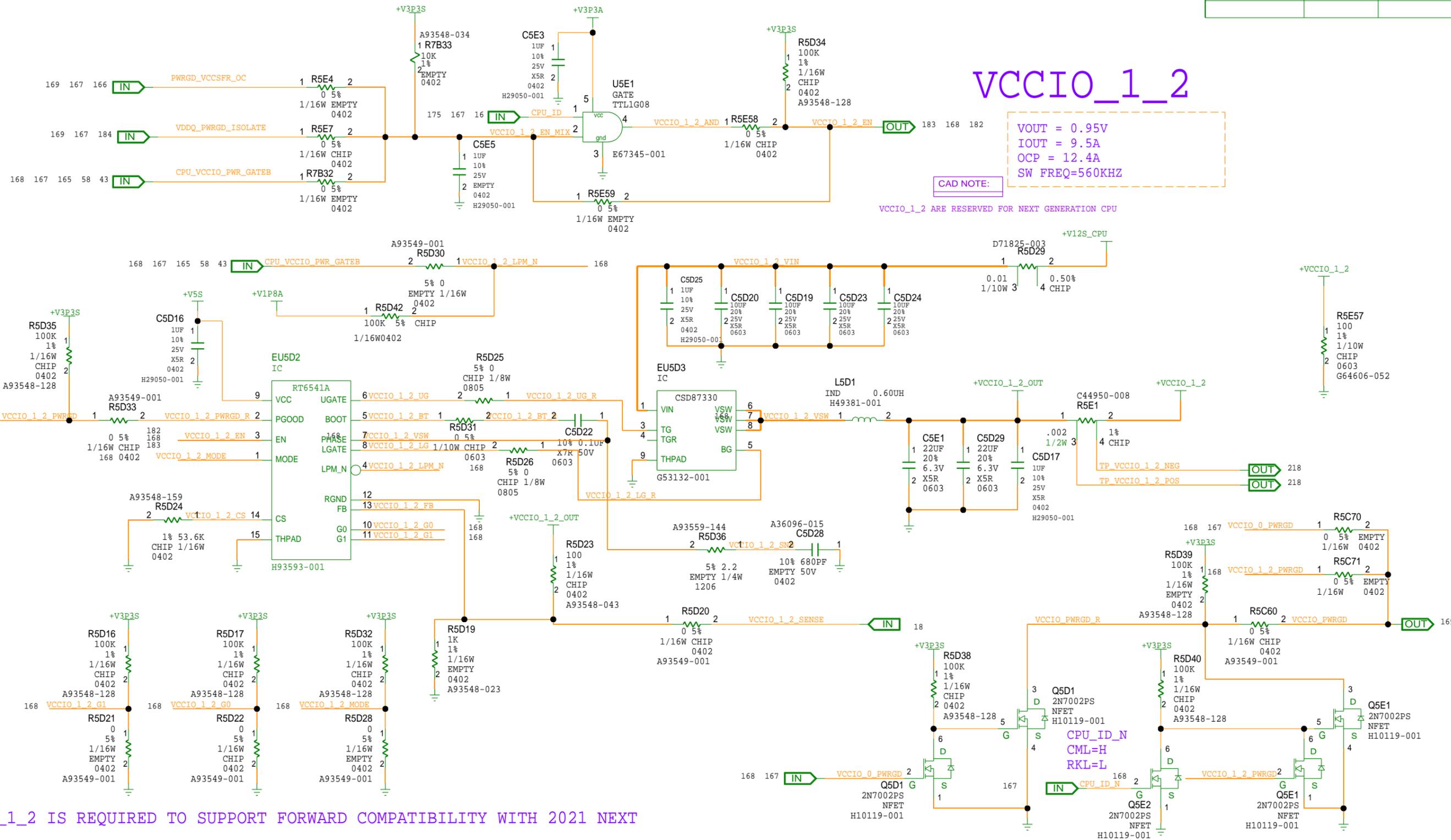
[PAGE_TITLE=VCCIO_0 GENERATION]

BPAGE DRAWING
 udimm.sch_1.167
 Fri Sep 27 16:41:55 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 167	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE



NOTE: +VCCIO_1_2 IS REQUIRED TO SUPPORT FORWARD COMPATIBILITY WITH 2021 NEXT GEN S-SERIES CPU ON CML-S BASED BOARDS.
+VCCIO_1_2 IS NOT REQUIRED IF BOARD IS DESIGNED TO SUPPORT CML-S CPU ONLY.

[PAGE_TITLE=VCCIO_1_2 GENERATION]

BPAGE DRAWING

udimm.sch_1.168
Fri Sep 27 16:41:56 2019

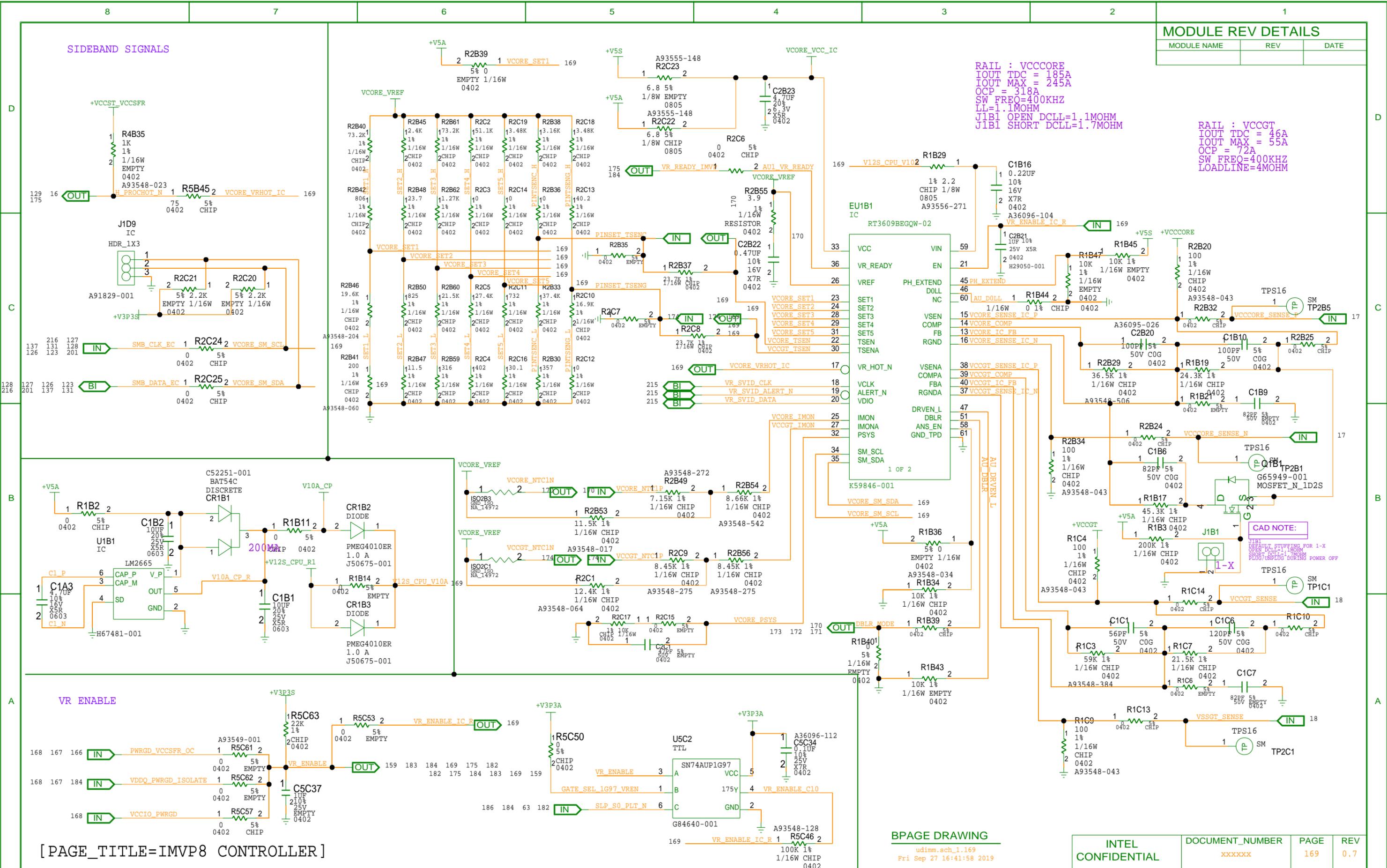
INTEL CONFIDENTIAL	DOCUMENT NUMBER xxxxxxx	PAGE 168	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE

RAIL : VCCCORE
 IOU TDC = 185A
 IOU MAX = 245A
 OCP = 318A
 SW FREQ=400KHZ
 LL=1.1MOHM
 J1B1 OPEN DCLL=1.1MOHM
 J1B1 SHORT DCLL=1.7MOHM

RAIL : VCCGT
 IOU TDC = 46A
 IOU MAX = 55A
 OCP = 72A
 SW FREQ=400KHZ
 LOADLINE=4MOHM



BPAGE DRAWING

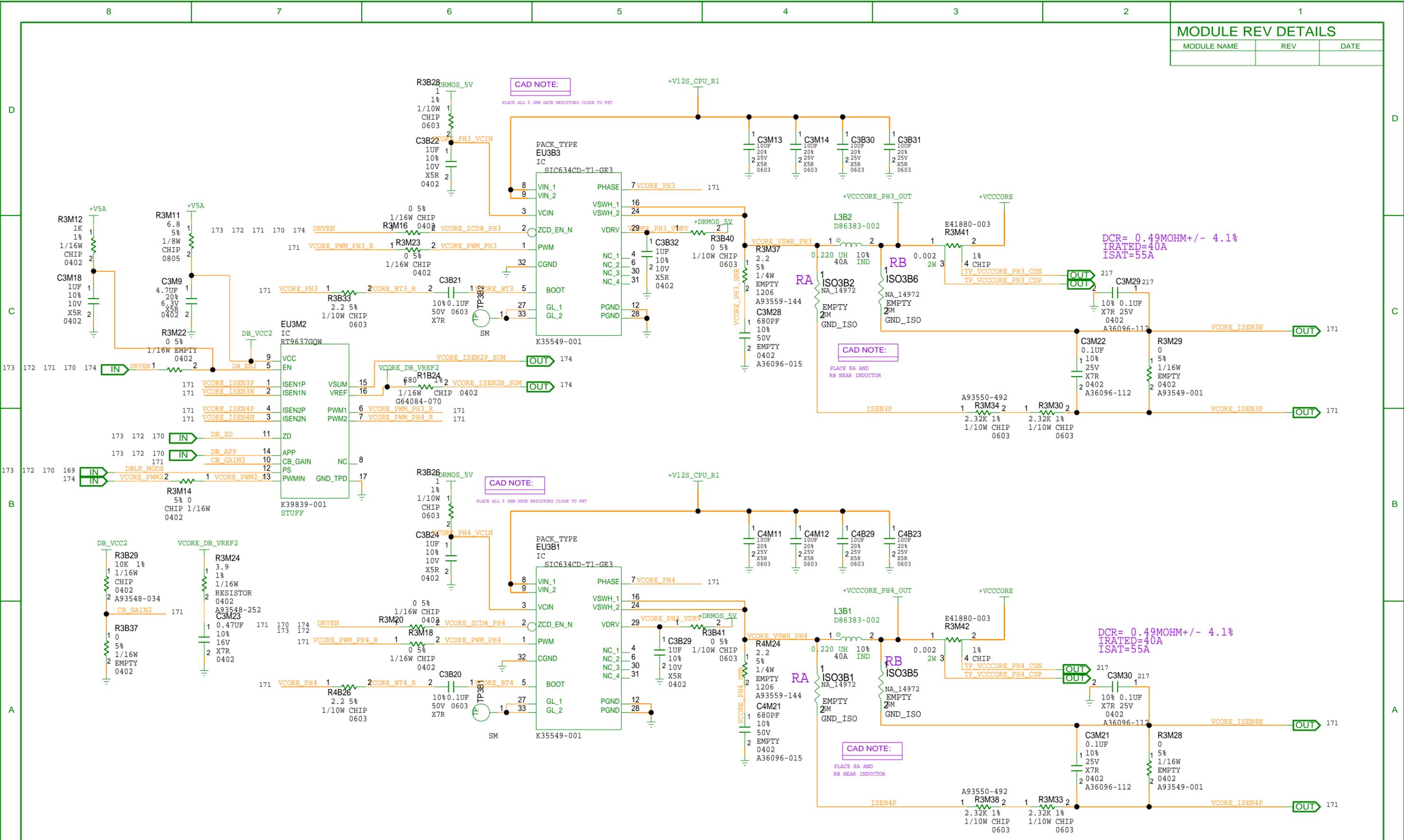
udimm.sch_1.169
 Fri Sep 27 16:41:58 2019

[PAGE_TITLE=IMVP8 CONTROLLER]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	xxxxxxx	169	0.7

MODULE REV DETAILS

MODULE NAME	REV	DATE



DCR= 0.49MOHM+/- 4.1%
 IRATED=40A
 ISAT=55A

DCR= 0.49MOHM+/- 4.1%
 IRATED=40A
 ISAT=55A

[PAGE_TITLE=VCCCORE PHASE 3 AND 4]

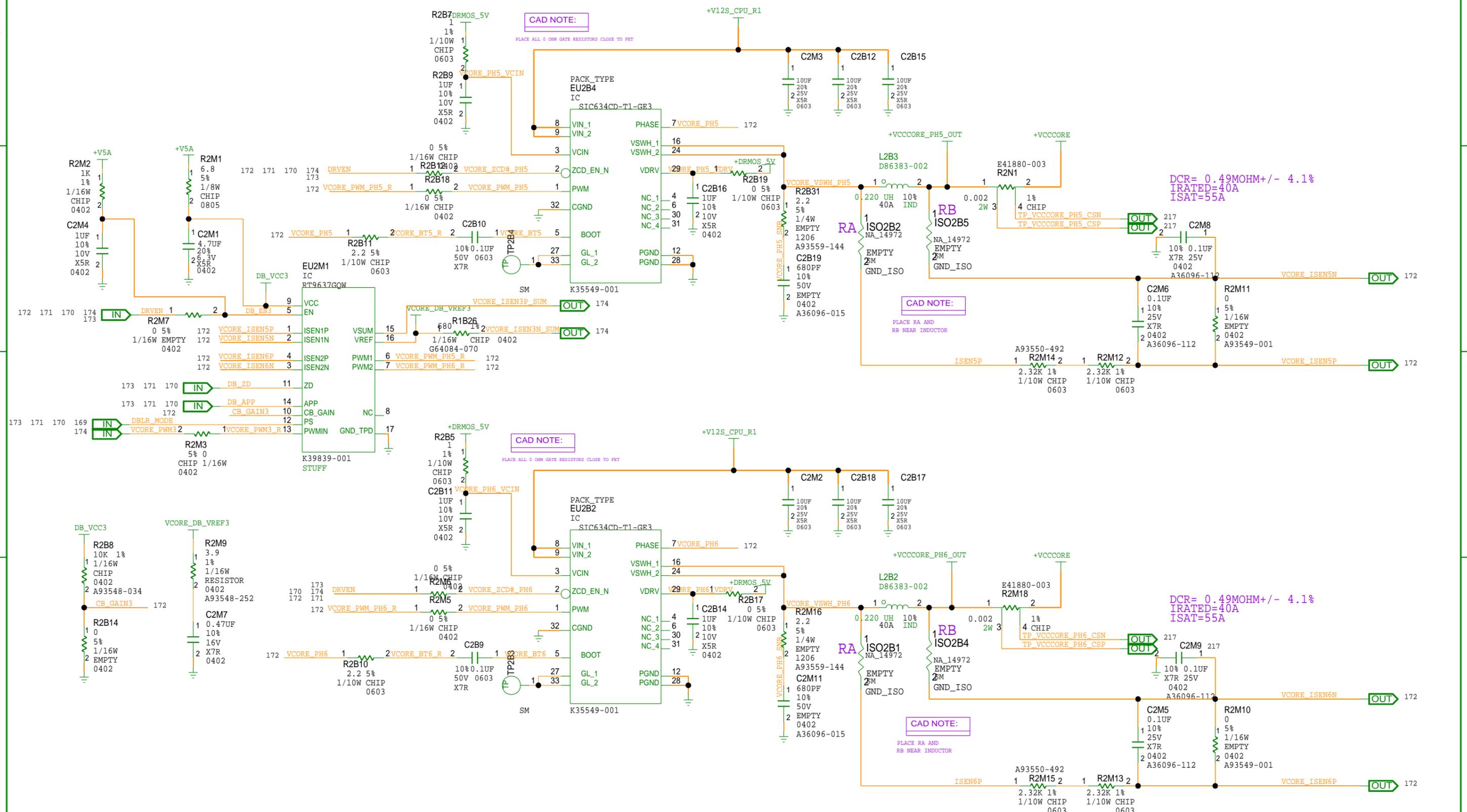
BPAGE DRAWING

udimm.sch_1.171
 Fri Sep 27 16:42:00 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 171	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE



[PAGE_TITLE=VCCCORE PHASE 5 AND 6]

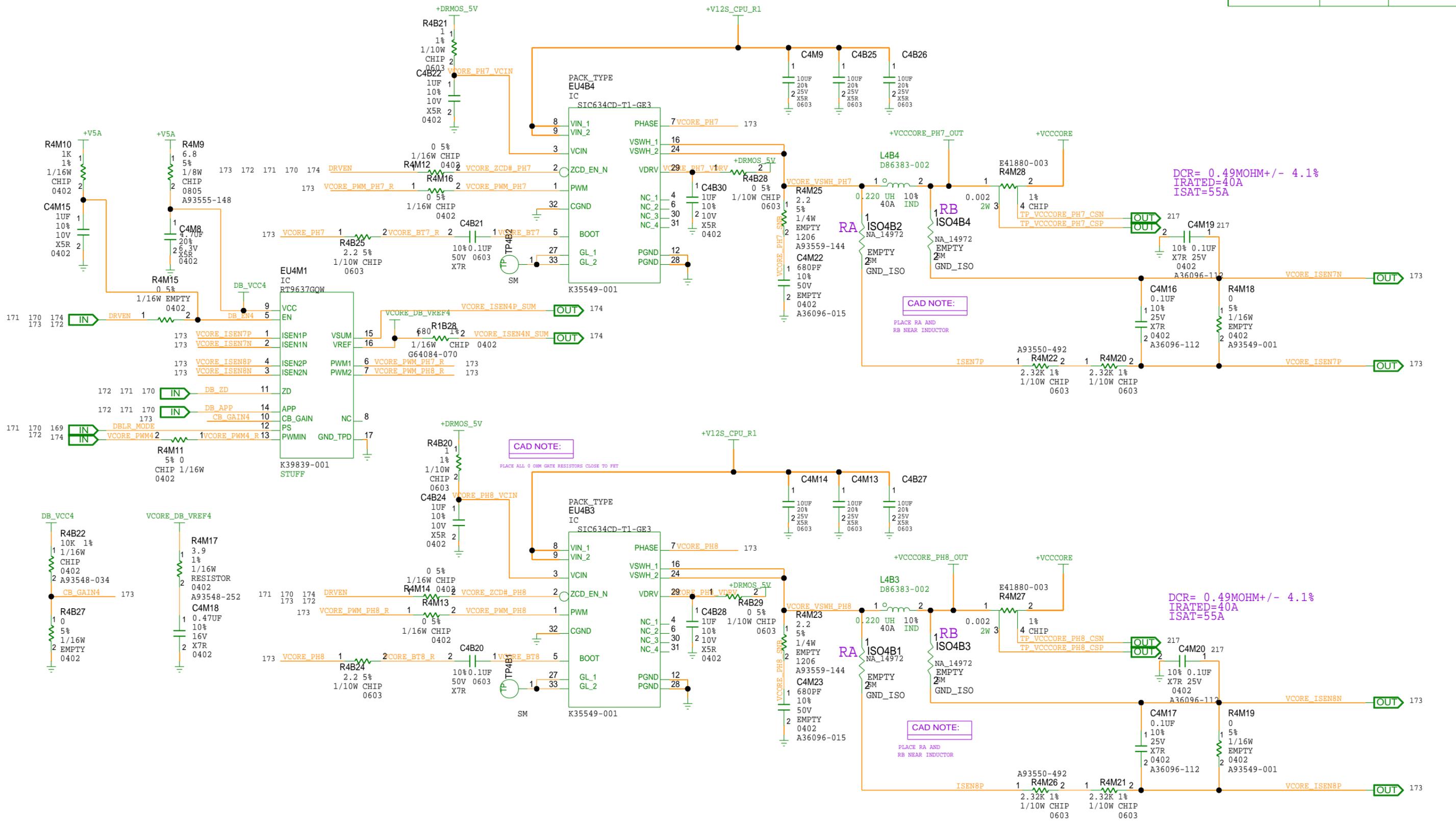
BPAGE DRAWING

udimm.sch_1.172
Fri Sep 27 16:42:01 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 172	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE



DCR= 0.49MOHM+/- 4.1%
 IRATED=40A
 ISAT=55A

DCR= 0.49MOHM+/- 4.1%
 IRATED=40A
 ISAT=55A

[PAGE_TITLE=VCCCORE PHASE 7 AND 8]

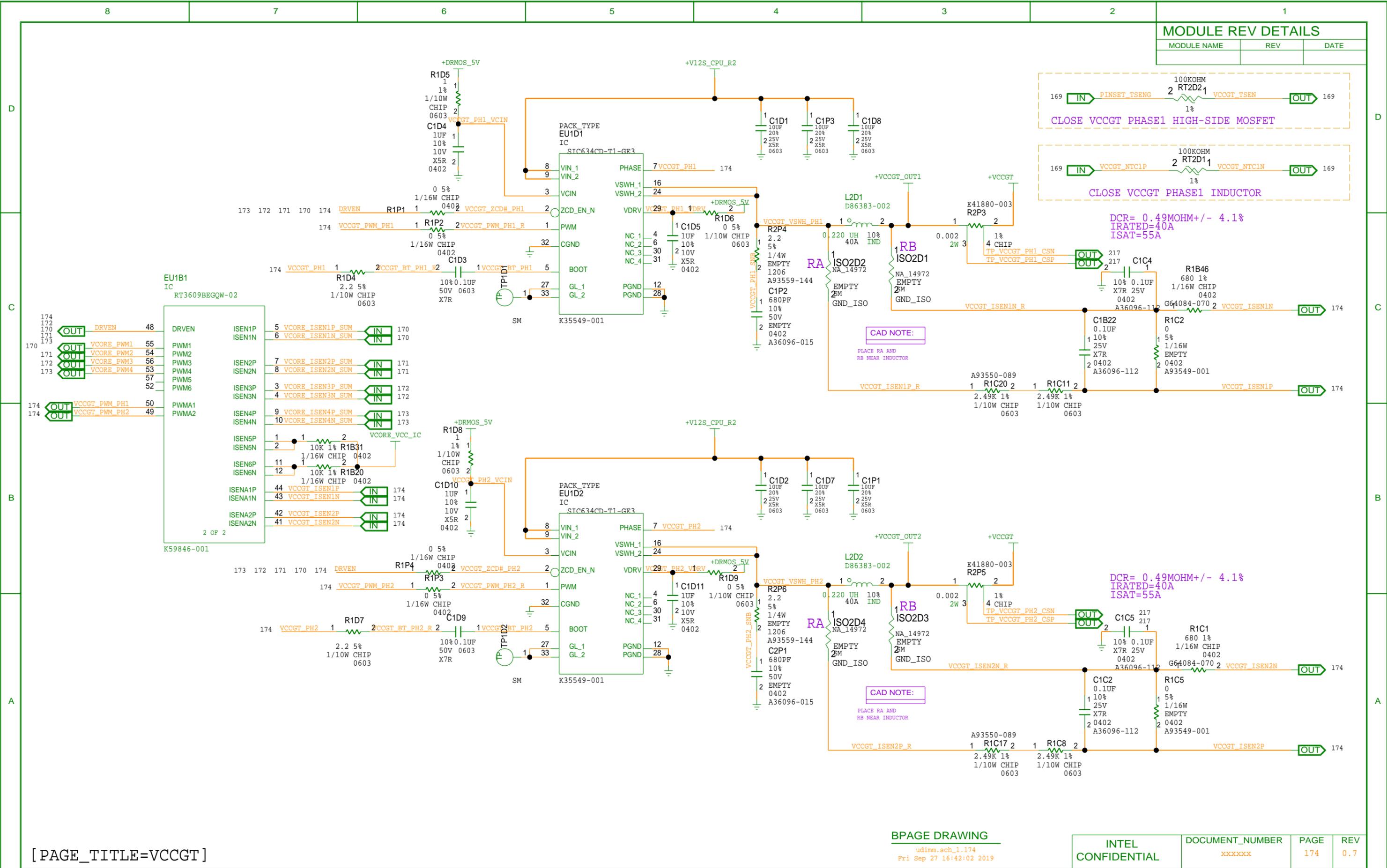
BPAGE DRAWING

udimm.sch_1.173
 Fri Sep 27 16:42:01 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 173	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE



100KOHM
RT2D2 1
VCCGT_TSEN
1%
CLOSE VCCGT PHASE1 HIGH-SIDE MOSFET

100KOHM
RT2D1 1
VCCGT_NTC1P
1%
CLOSE VCCGT PHASE1 INDUCTOR

DCR= 0.49MOHM +/- 4.1%
IRATED=40A
ISAT=55A

CAD NOTE:
PLACE RA AND
RB NEAR INDUCTOR

DCR= 0.49MOHM +/- 4.1%
IRATED=40A
ISAT=55A

CAD NOTE:
PLACE RA AND
RB NEAR INDUCTOR

[PAGE_TITLE=VCCGT]

BPAGE DRAWING
udimm.sch_1.174
Fri Sep 27 16:42:02 2019

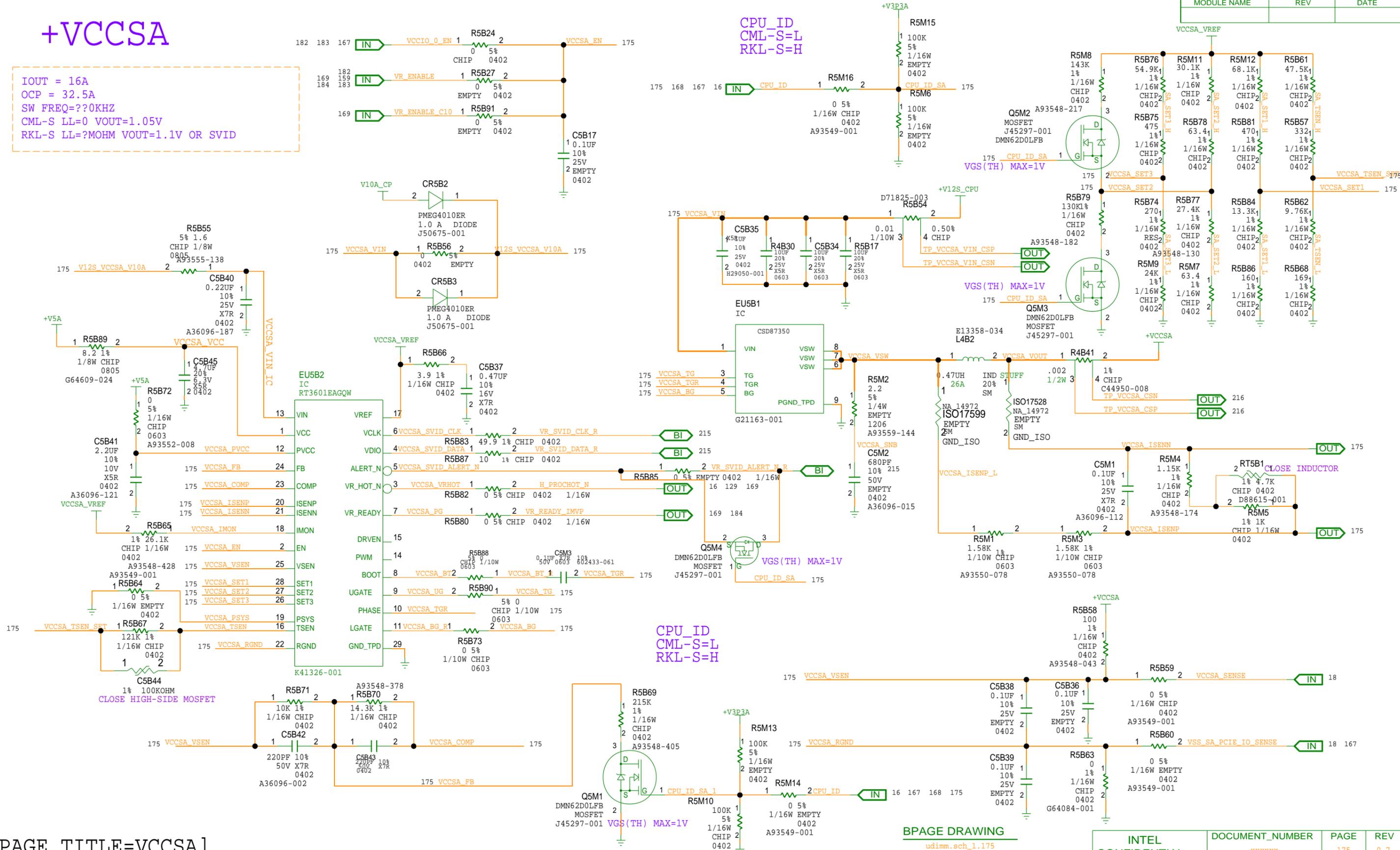
INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 174	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE

+VCCSA

IOUT = 16A
 OCP = 32.5A
 SW FREQ=??0KHZ
 CML-S LL=0 VOUT=1.05V
 RKL-S LL=?MOHM VOUT=1.1V OR SVID



[PAGE_TITLE=VCCSA]

BPAGE DRAWING
 udimm.sch_1.175
 Fri Sep 27 16:42:03 2019

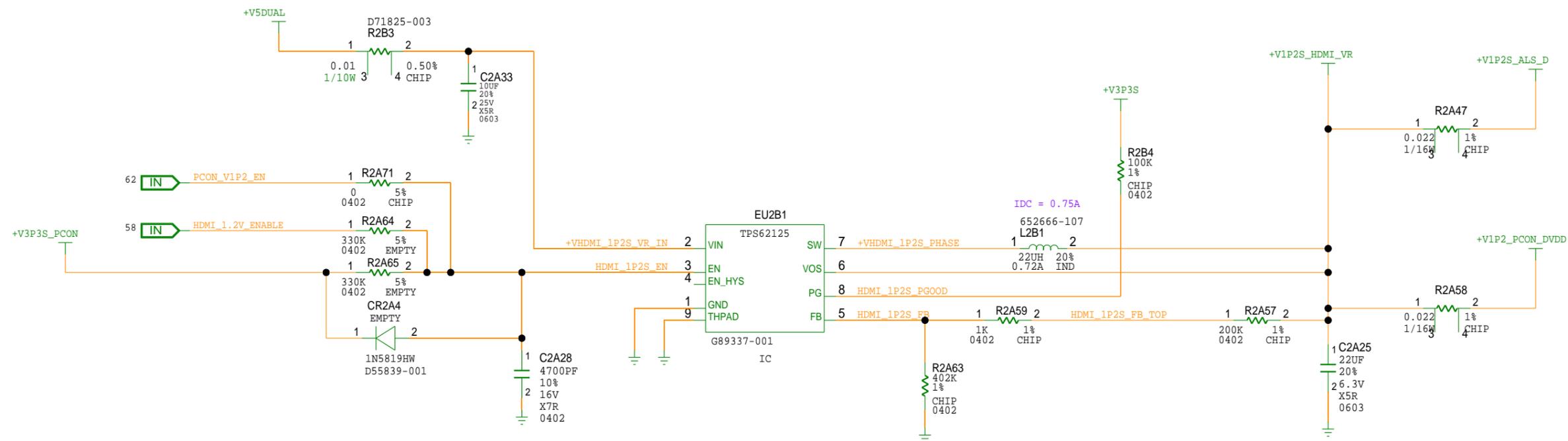
INTEL CONFIDENTIAL

DOCUMENT_NUMBER	PAGE	REV
xxxxxxx	175	0.7

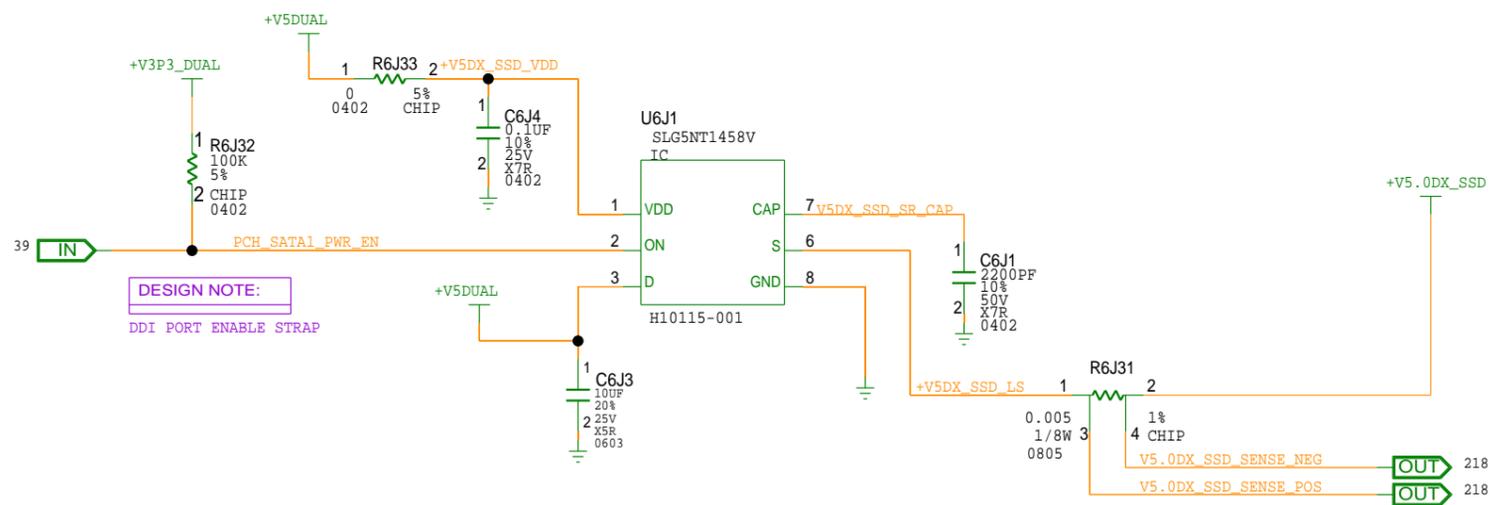
MODULE REV DETAILS

MODULE NAME	REV	DATE

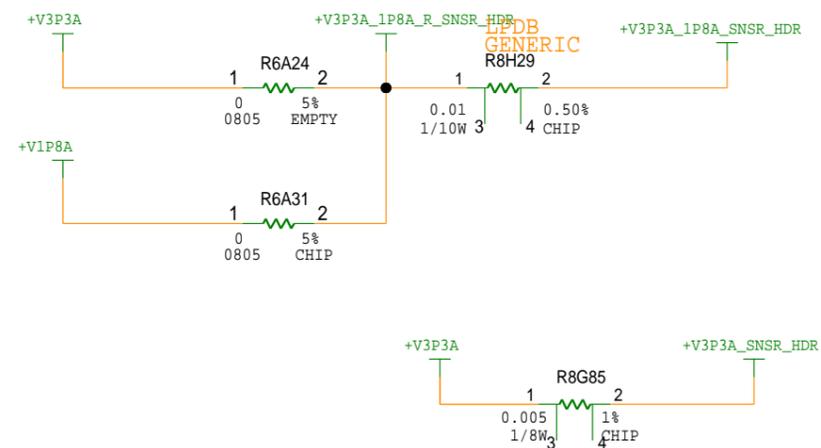
1P2V RAIL FOR HDMI AND UFS - POWER CONVERSION



V5DX_SSD DIRECT CONNECT GENERATION



ISH AIC POWER GENERATION



BPAGE DRAWING

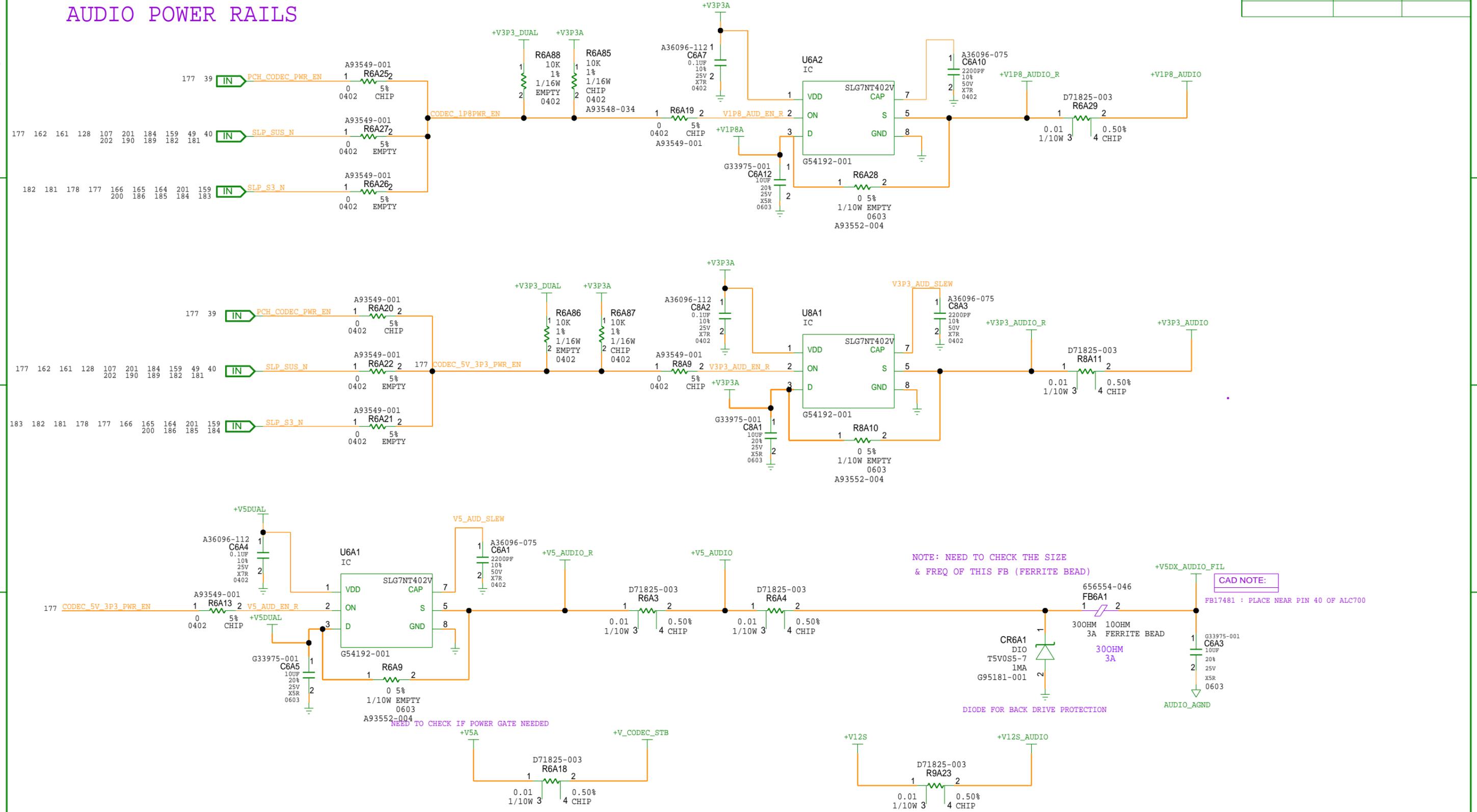
udimm.sch_1.176
Fri Sep 27 16:42:04 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 176	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE

AUDIO POWER RAILS



NOTE: NEED TO CHECK THE SIZE & FREQ OF THIS FB (FERRITE BEAD)

CAD NOTE:

FB17481 : PLACE NEAR PIN 40 OF ALC700

NEED TO CHECK IF POWER GATE NEEDED

DIODE FOR BACK DRIVE PROTECTION

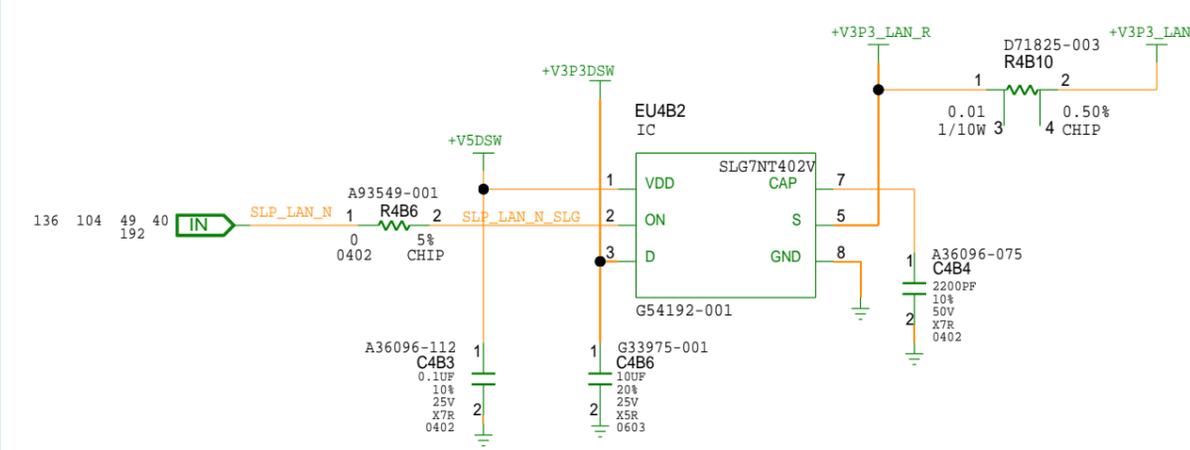
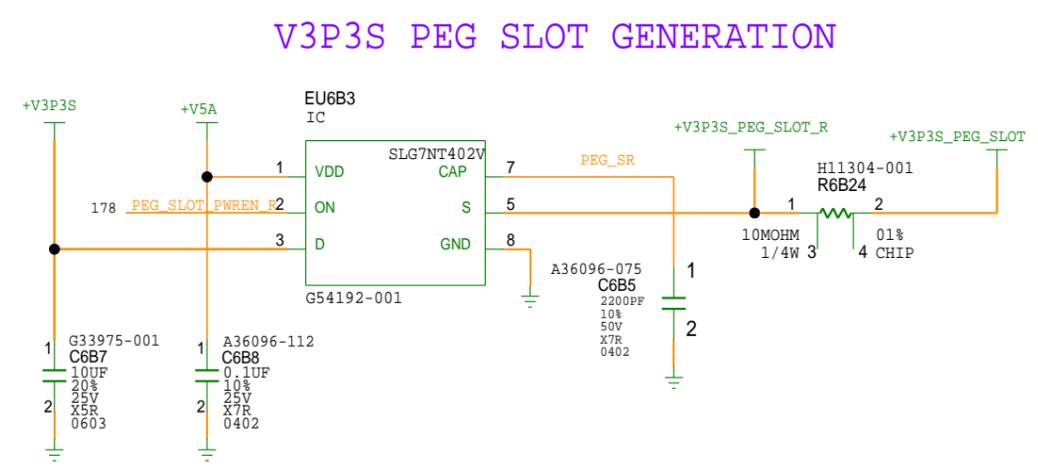
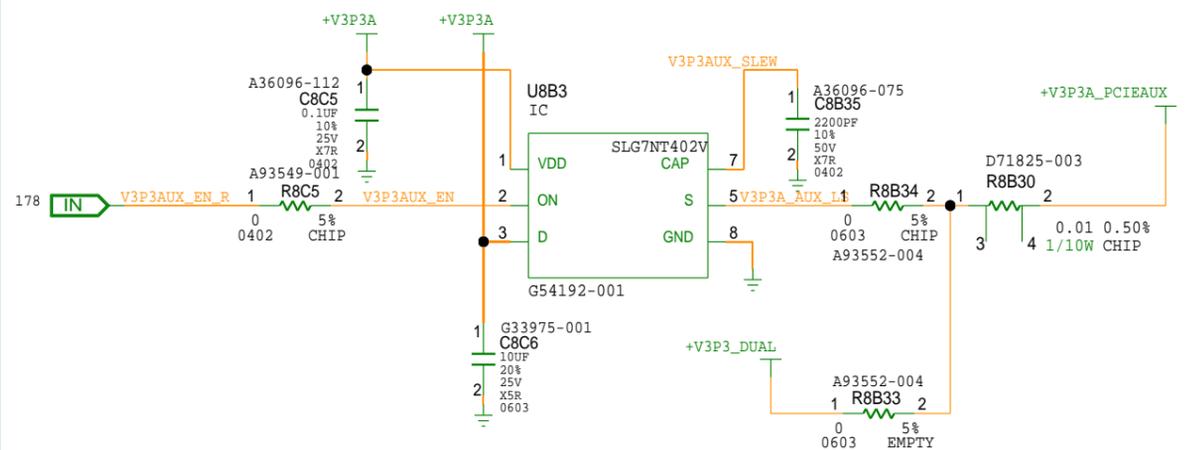
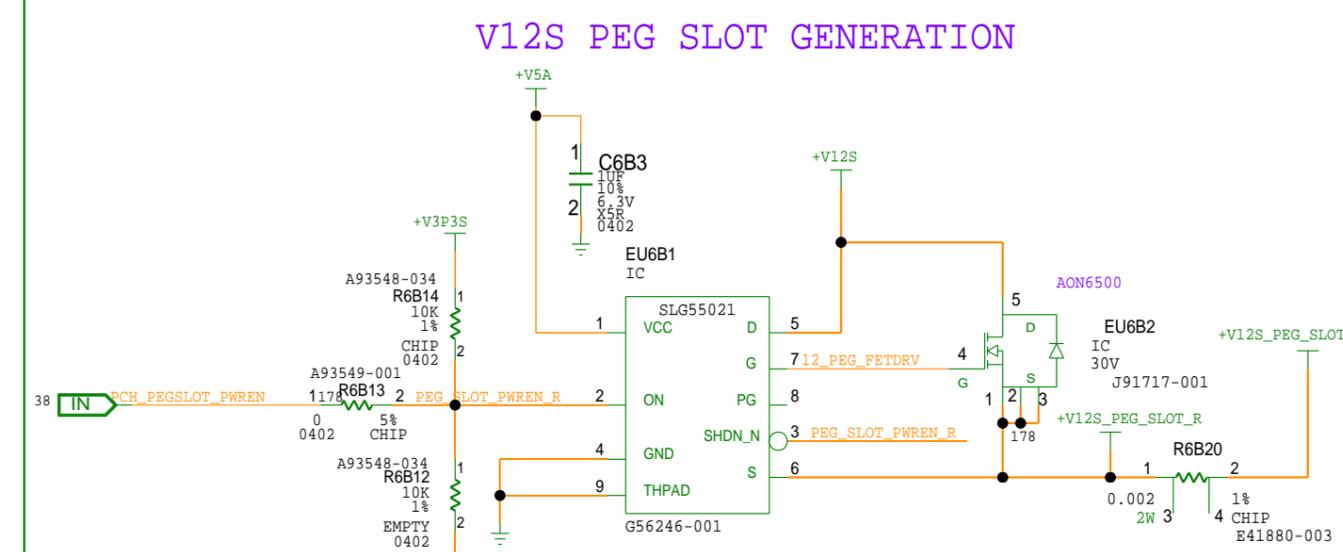
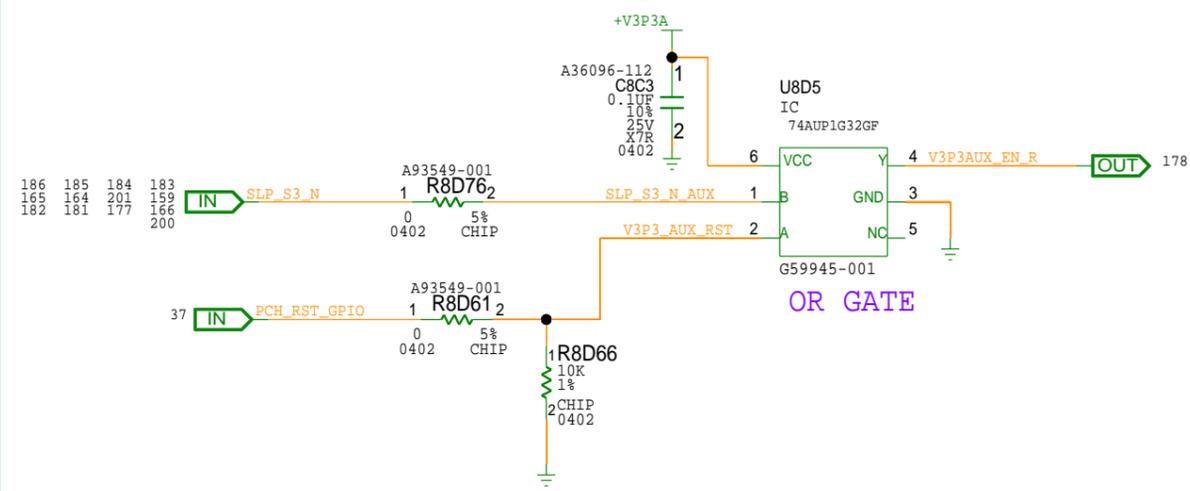
[PAGE_TITLE=AUDIO POWER RAILS]

BPAGE DRAWING

udimm.sch_1.177
Fri Sep 27 16:42:05 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 177	REV 0.7
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MODULE REV DETAILS		
MODULE NAME	REV	DATE

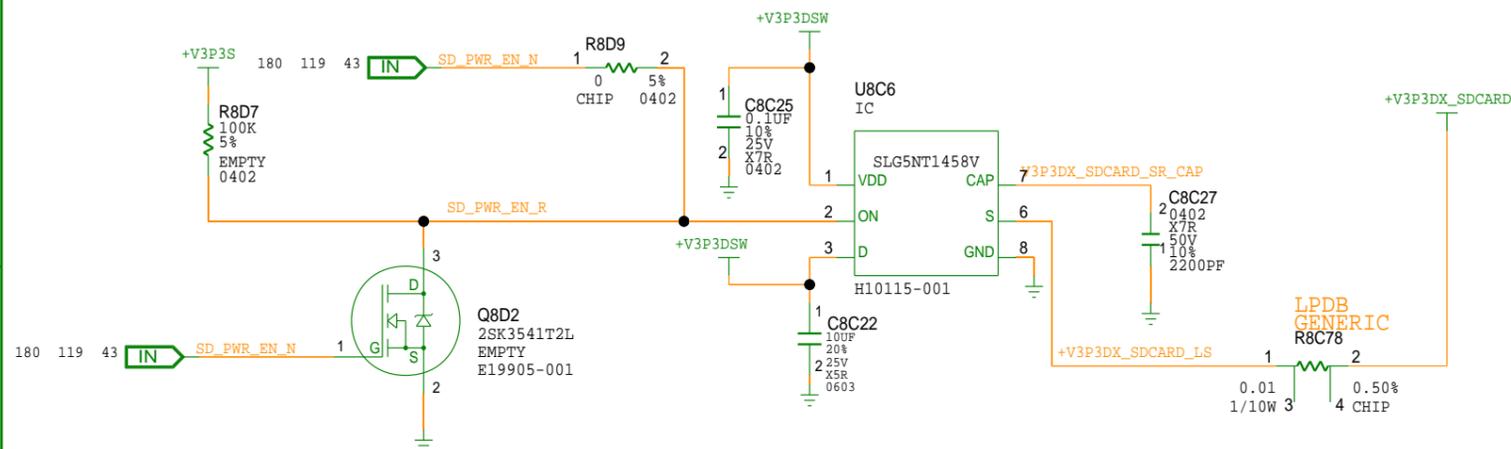


[PAGE_TITLE=PCIE SLOT AND PEG RAILS]

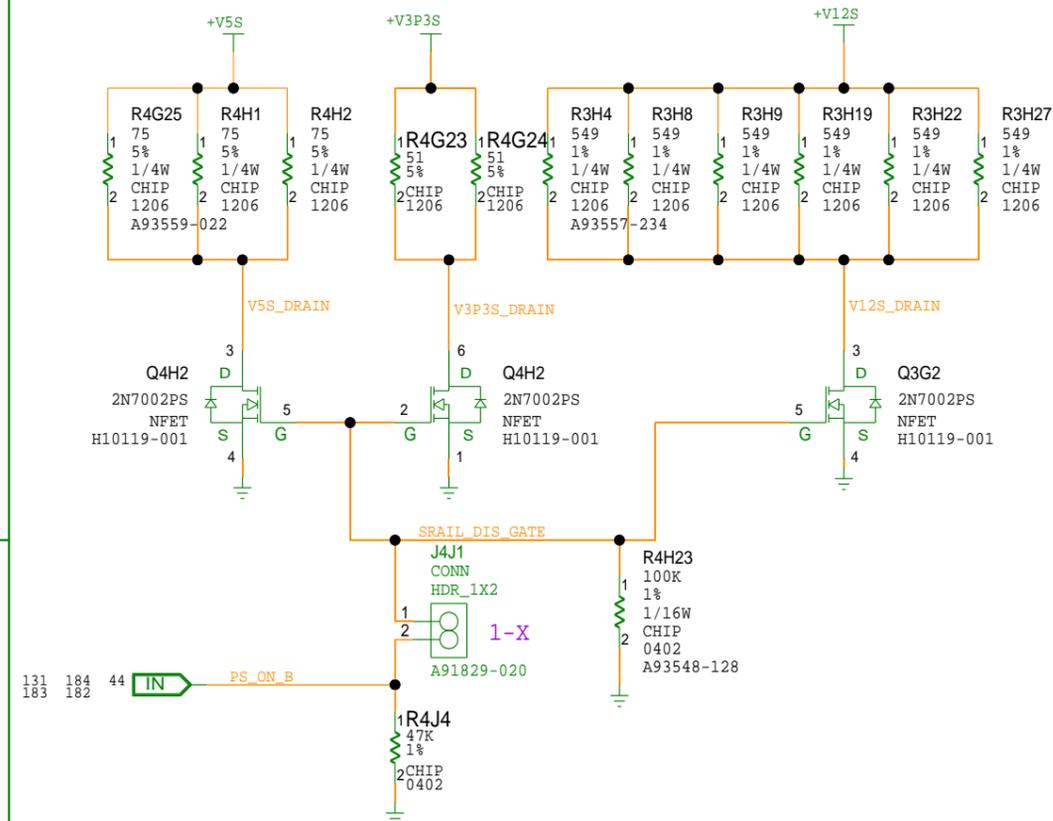
BPAGE DRAWING
 udimm.sch_1.178
 Fri Sep 27 16:42:06 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER	PAGE	REV
	xxxxxxx	178	0.7

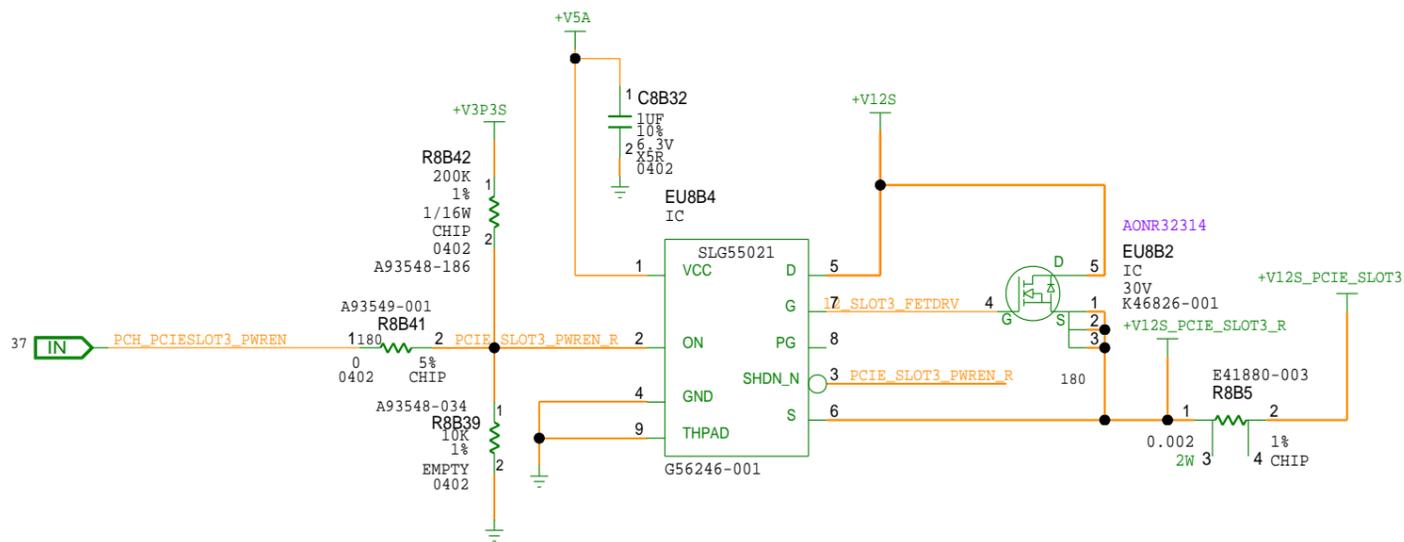
SD CARD POWER SUPPLY GENERATION



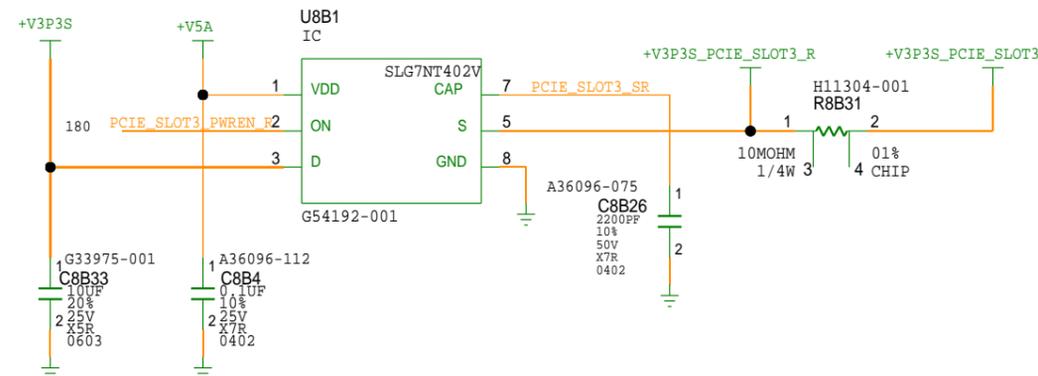
ATX S-RAIL DISCHARGE



V12S PCIE SLOT3 GENERATION



V3P3S PCIE SLOT3 GENERATION



[PAGE_TITLE=SDCARD RAILS, ATX-S DISCHARGE, PCIE SLOT3 POWER]

MODULE REV DETAILS

MODULE NAME	REV	DATE

BPAGE DRAWING

udimm.sch_1.180
Fri Sep 27 16:42:08 2019

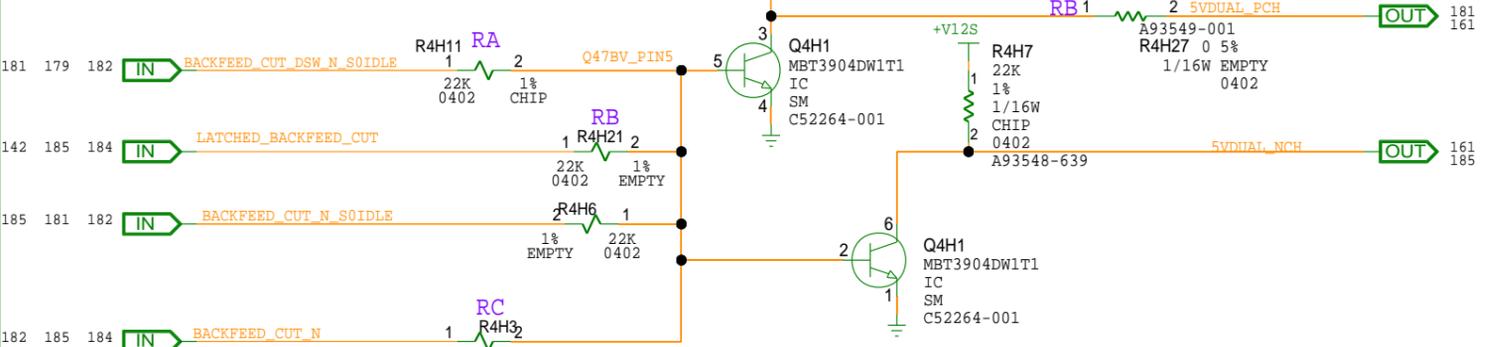
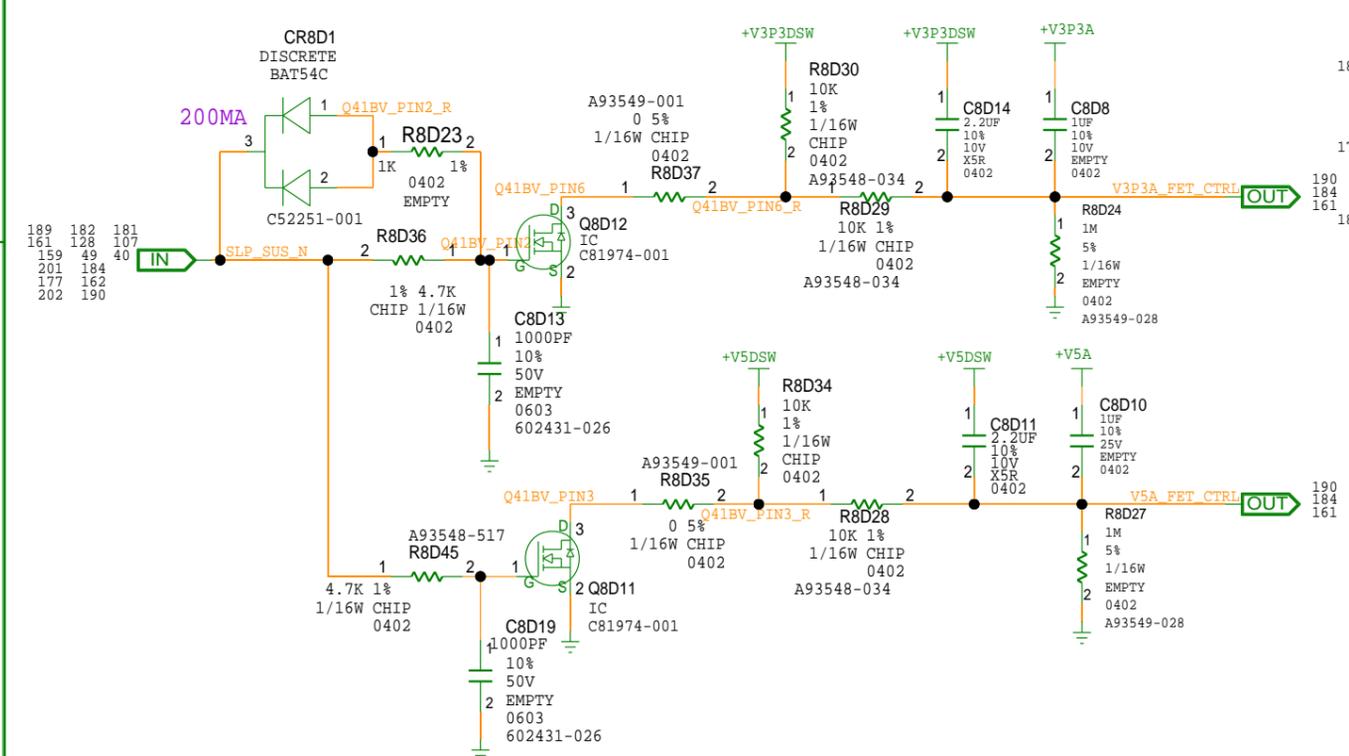
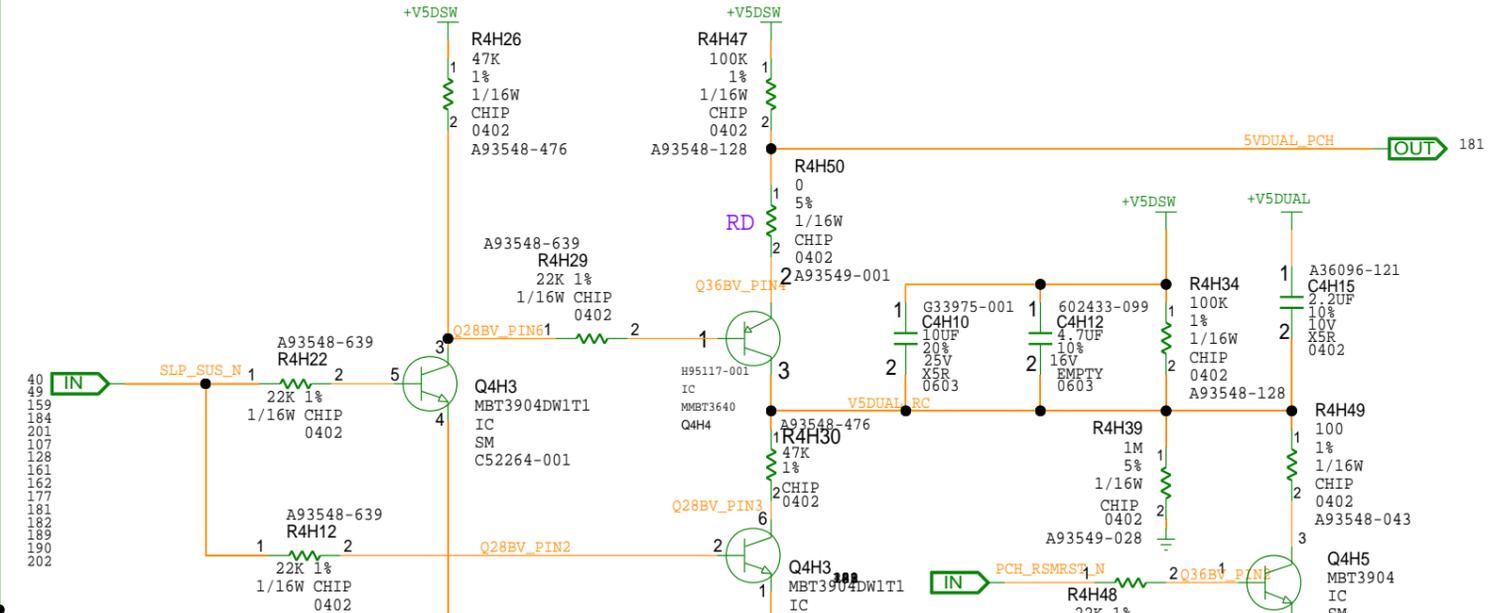
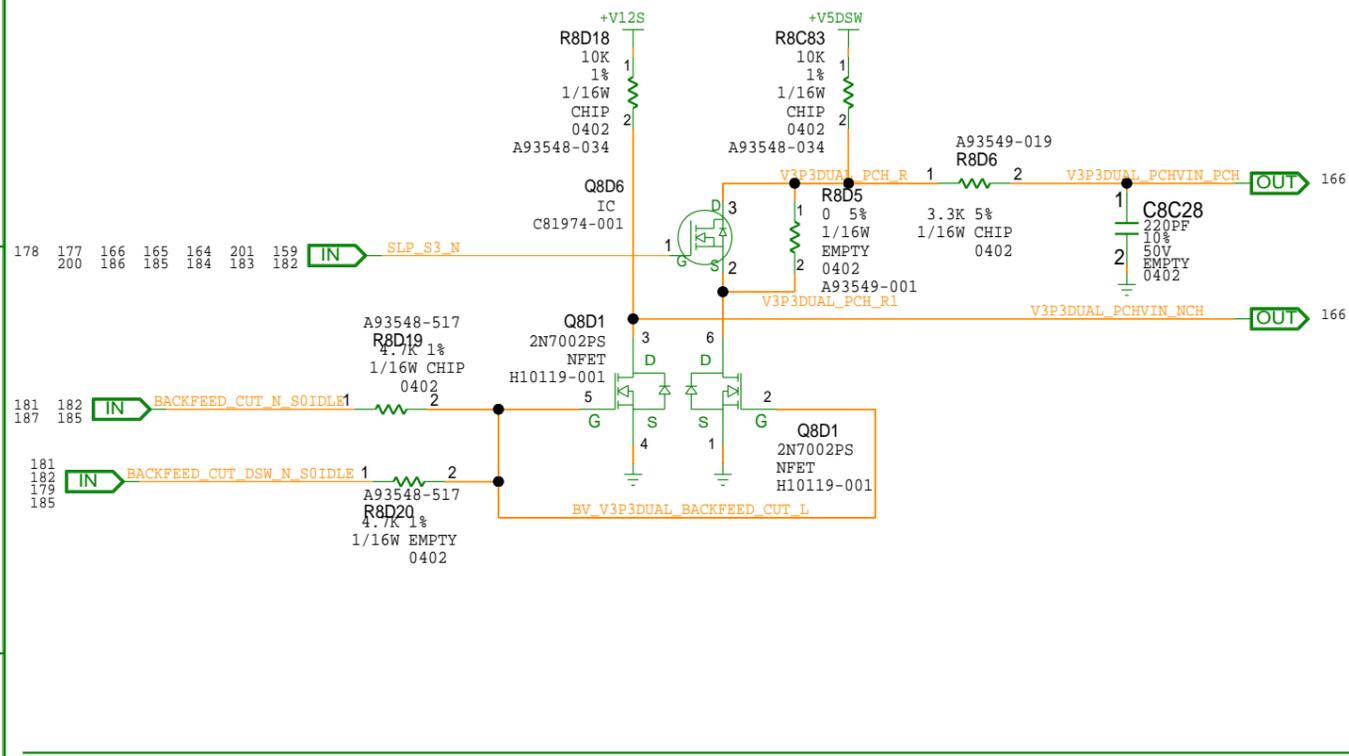
INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 180	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE

3P3_DUAL_GEN

5VDUAL_GEN



BOM NOTE:
 STUFF RA FOR USB WAKE FROM S4/S5
 STUFF RB; EMPTY RD FOR USB WAKE FROM S3 ONLY
 STUFF RC FOR USB WAKE FROM DS4/DS5

[PAGE_TITLE=5VDUAL, V3P3_DUAL SIGNALS GENERATION]

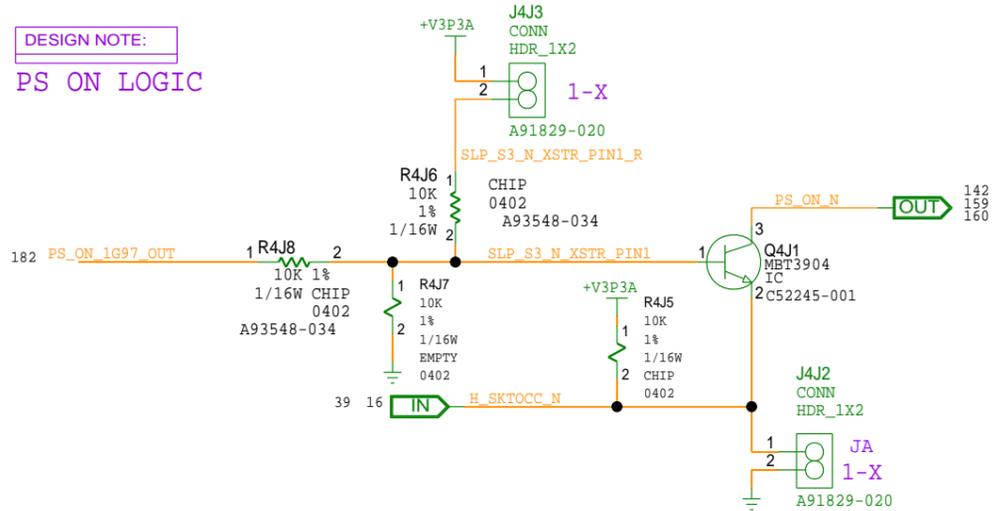
BPAGE DRAWING
udimm.sch_1.181
Fri Sep 27 16:42:09 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 181	REV 0.7
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MODULE REV DETAILS

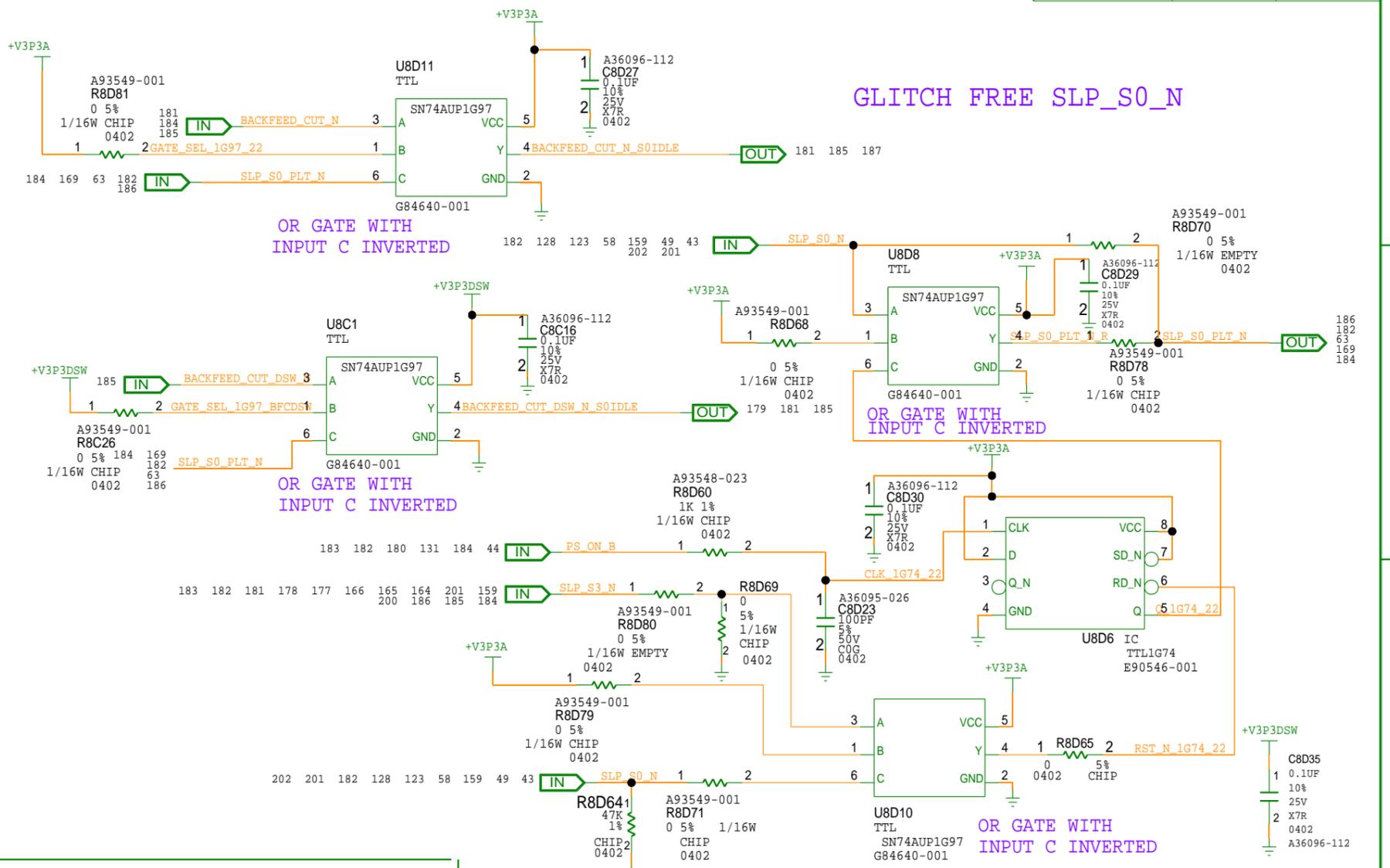
MODULE NAME	REV	DATE

DESIGN NOTE:
PS ON LOGIC



BOM NOTE:
INSERT JUMPER AT PIN 1-2 OF JA IF NO CPU STUFFED

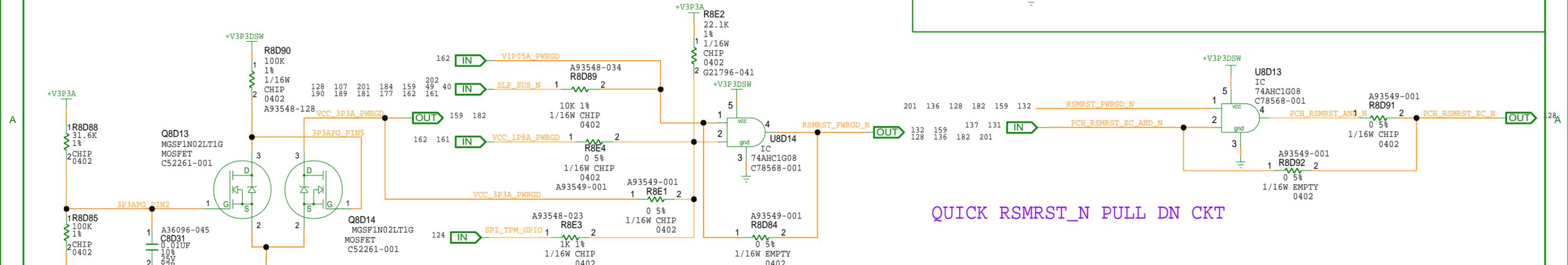
CEC RELATED SEQ LOGIC



GLITCH FREE SLP_S0_N

OR GATE WITH INPUT C INVERTED

FAST PD OF VCCIO_EN AND VR_ENABLE AT PS_ON_B=LOW



V3P3A PWRGD CIRCUIT

REQUEST EC TO GENERATE 10MS DELAY

QUICK RSMRST_N PULL DN CKT

BPAGE DRAWING

udimm.sch_1.182
Fri Sep 27 16:42:10 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 182	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE

DDR4 POWER SEQUENCE

CHANGED PWRGD CIRCUIT TO MORE ACCURATE

STUFF RA IF MERGE SA/IO RAIL

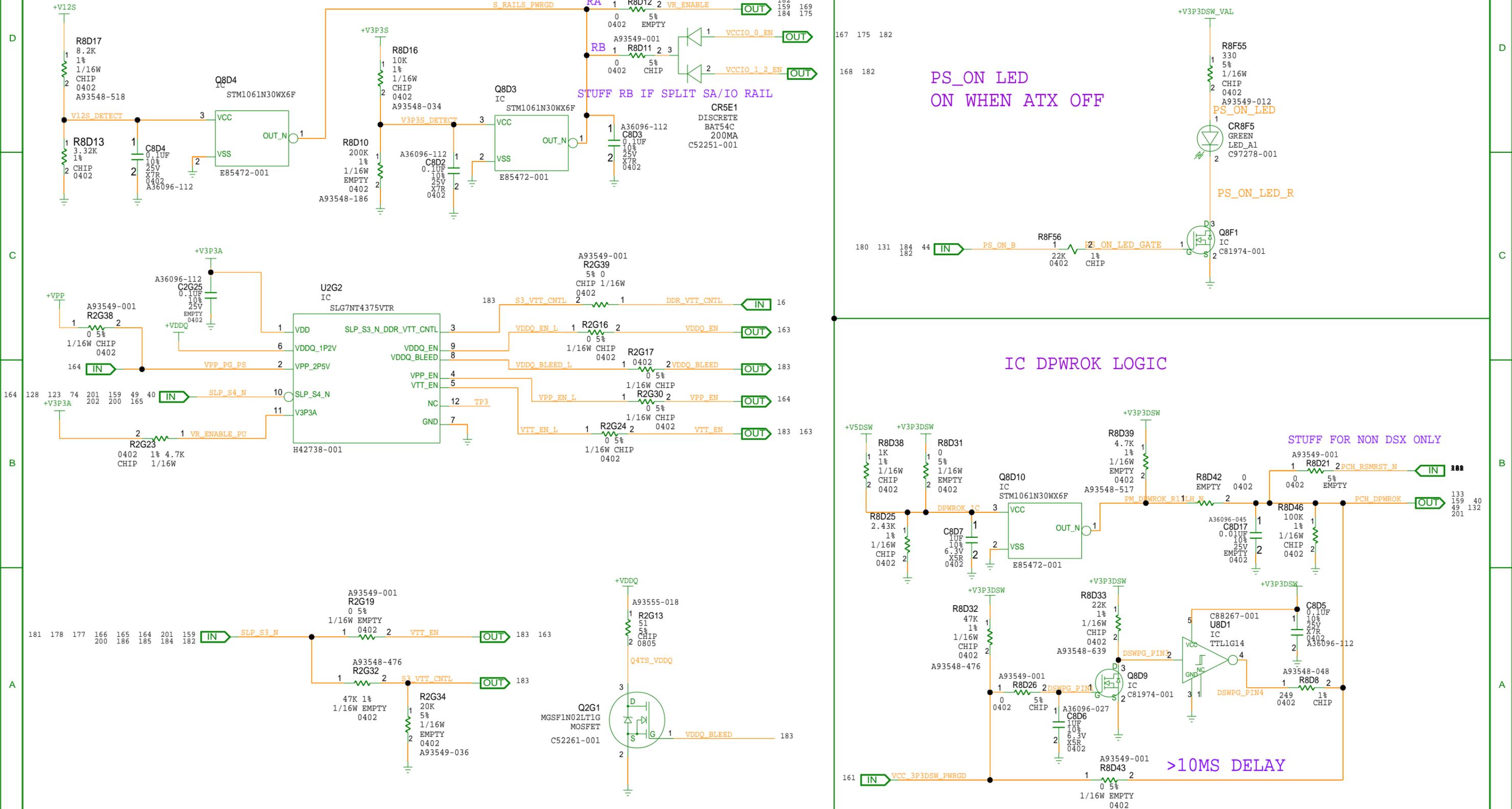
STUFF RB IF SPLIT SA/IO RAIL

PS_ON LED ON WHEN ATX OFF

IC DPWROK LOGIC

STUFF FOR NON DSX ONLY

>10MS DELAY



[PAGE_TITLE=VDDQ SEQUENCE AND DPWROK AND PS_ON LED]

BPAGE DRAWING

udimm.sch_1.183
Fri Sep 27 16:42:11 2019

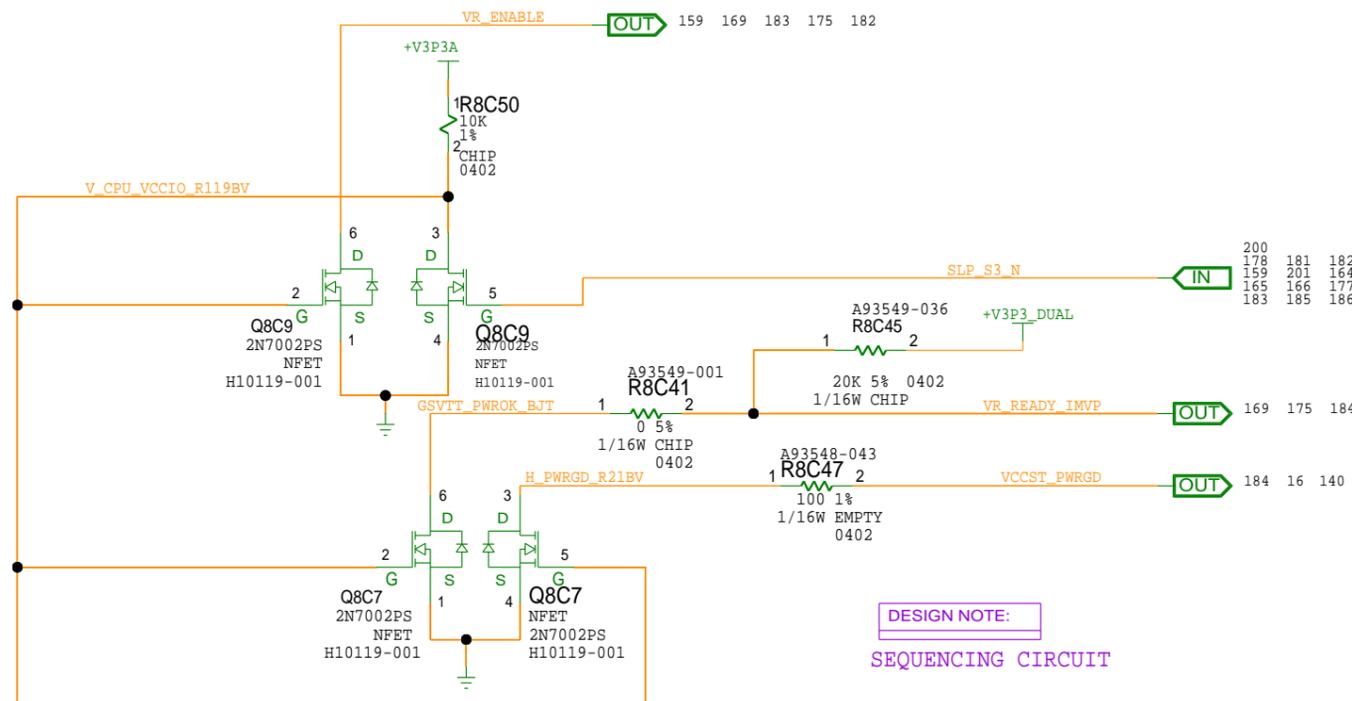
INTEL CONFIDENTIAL	DOCUMENT NUMBER xxxxxxx	PAGE 183	REV 0.7
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MODULE REV DETAILS

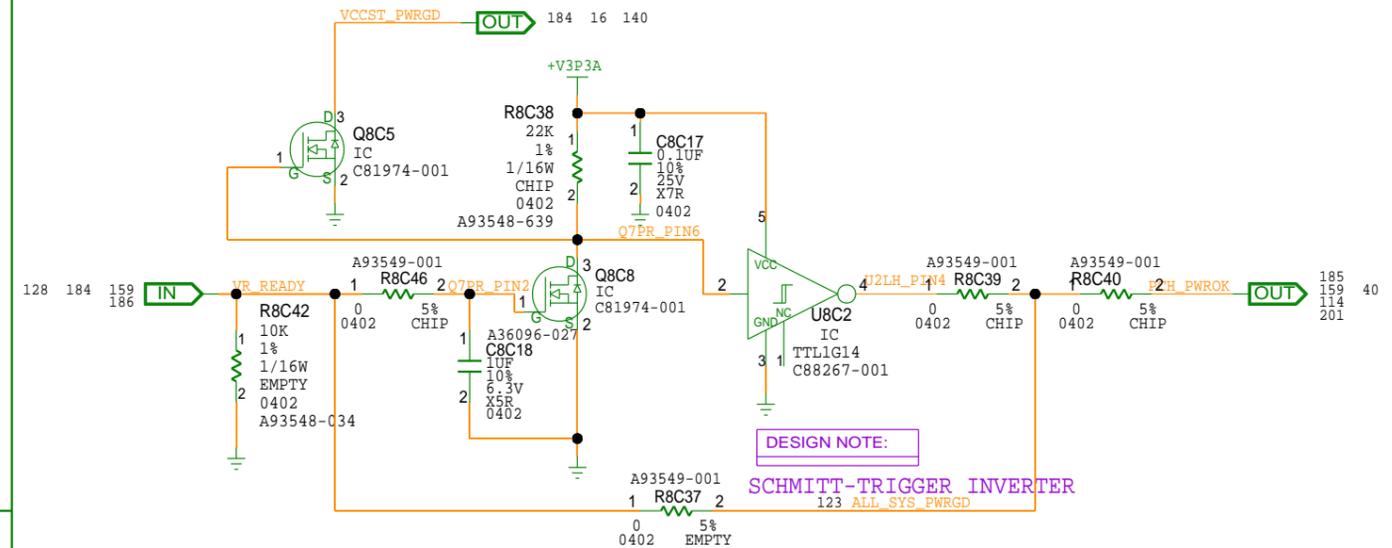
MODULE NAME	REV	DATE

3.3V, VOLDDIV AT CPU PAGE

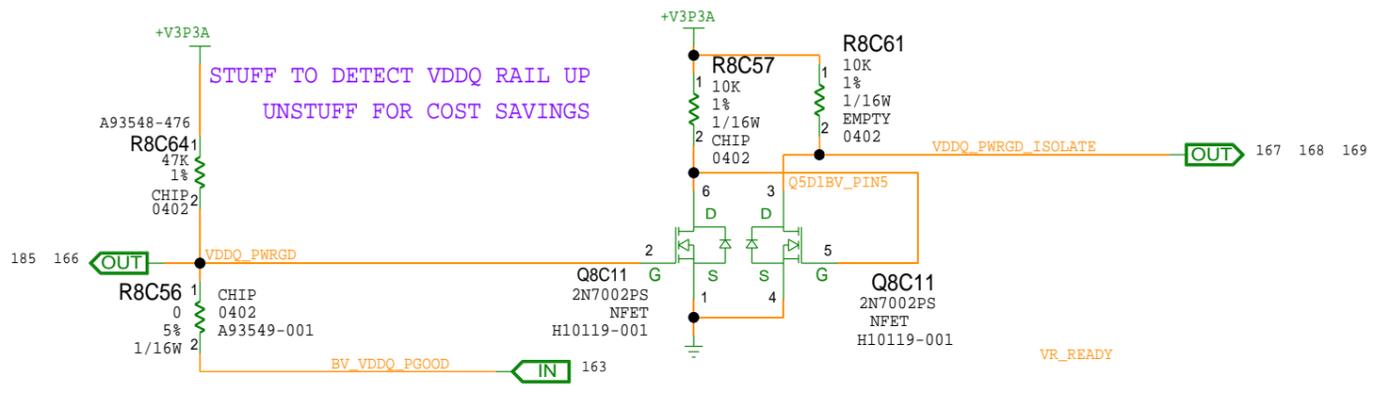
NEEDS TO BE OPTIMIZED PCH_PWRGD & VCCST_PWRGD



DESIGN NOTE:
SEQUENCING CIRCUIT

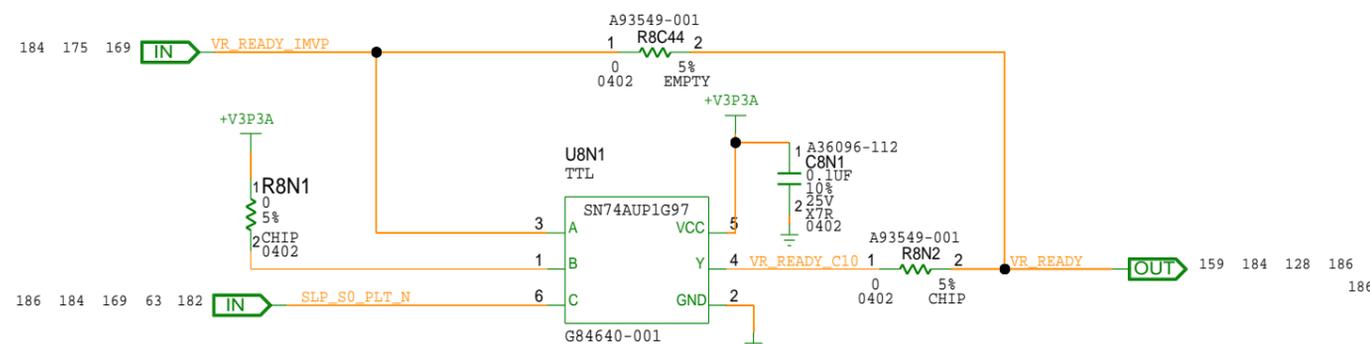
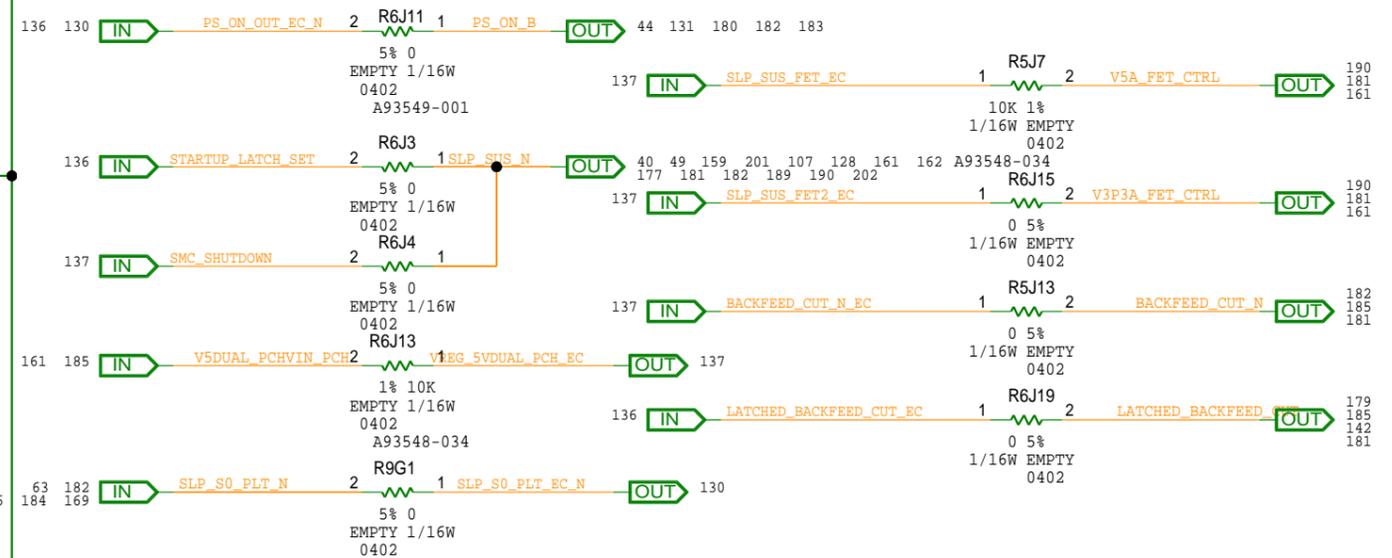


DESIGN NOTE:
SCHMITT-TRIGGER INVERTER



STUFF TO DETECT VDDQ RAIL UP
UNSTUFF FOR COST SAVINGS

MECC SIGNALS



BPAGE DRAWING

udimm.sch_1.184
Fri Sep 27 16:42:12 2019

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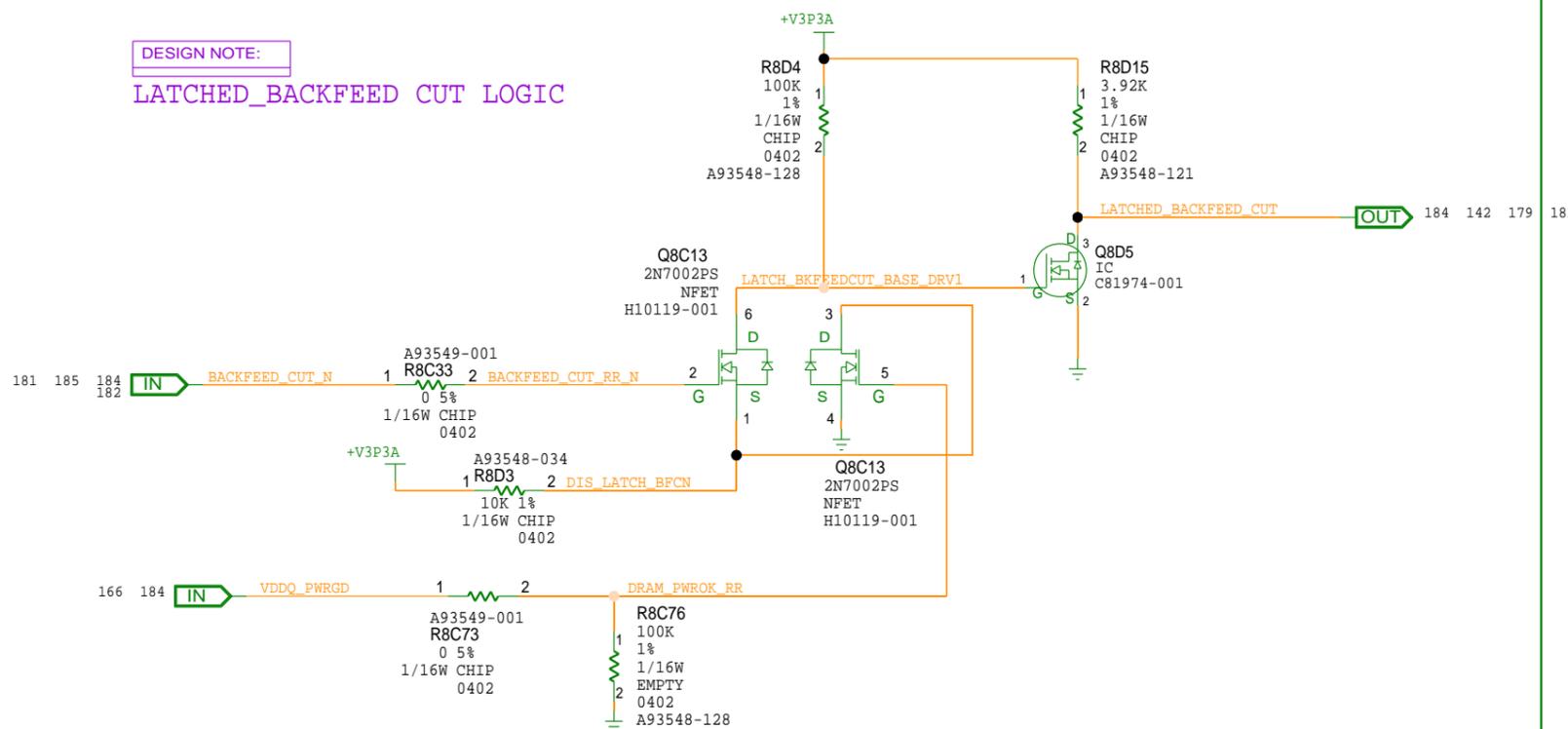
[PAGE_TITLE=VR_ENABLE, VCCIO_EN, VCCST_PWRGD, PCHPWROK]

MODULE REV DETAILS

MODULE NAME	REV	DATE

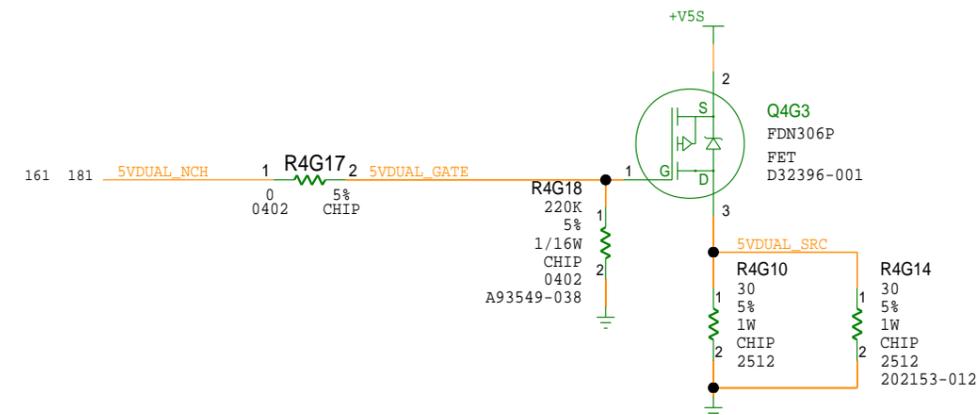
DESIGN NOTE:

LATCHED_BACKFEED CUT LOGIC



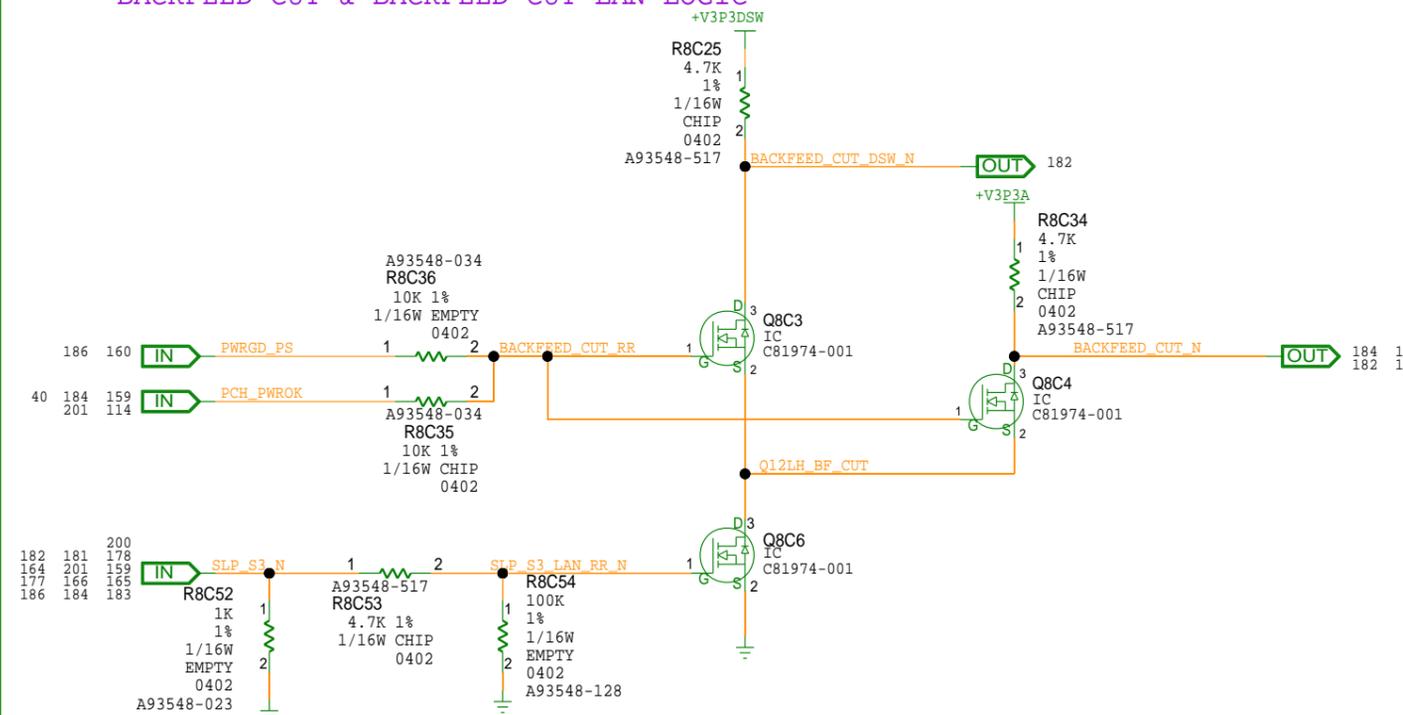
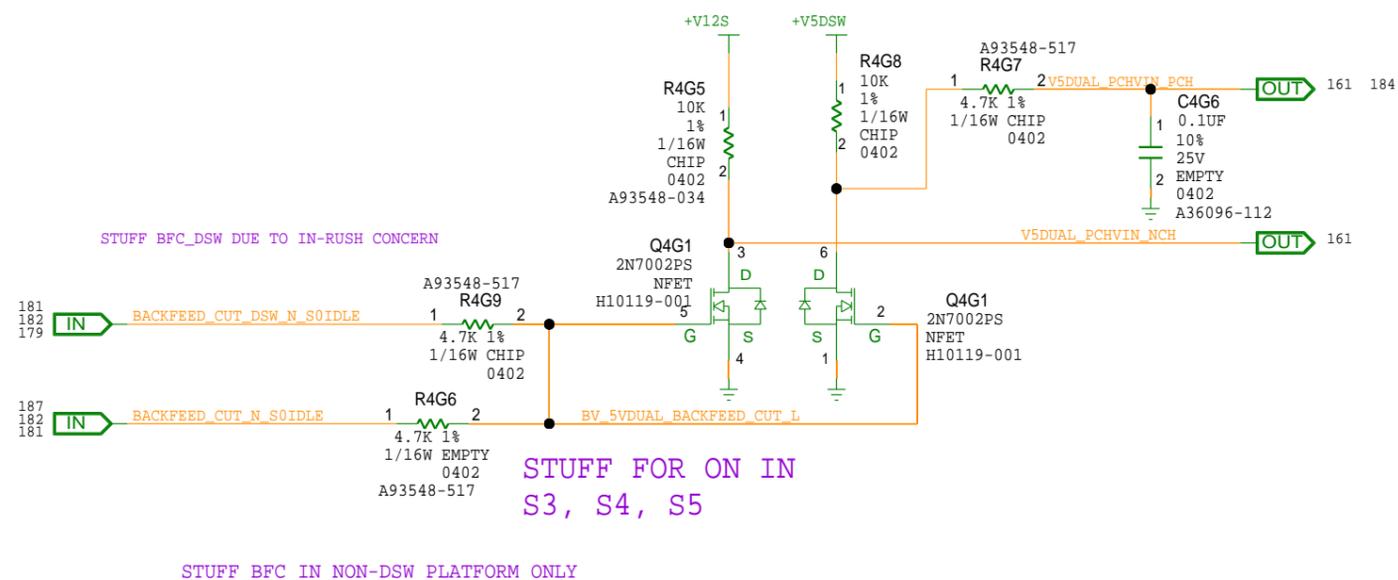
TRUTH TABLE:

	BFC	LBFC	BFC_DSW
S0	0	0	0
S3	1	1	1
S4/S5	1	0	1
DS4/DS5	0	0	1



DESIGN NOTE:

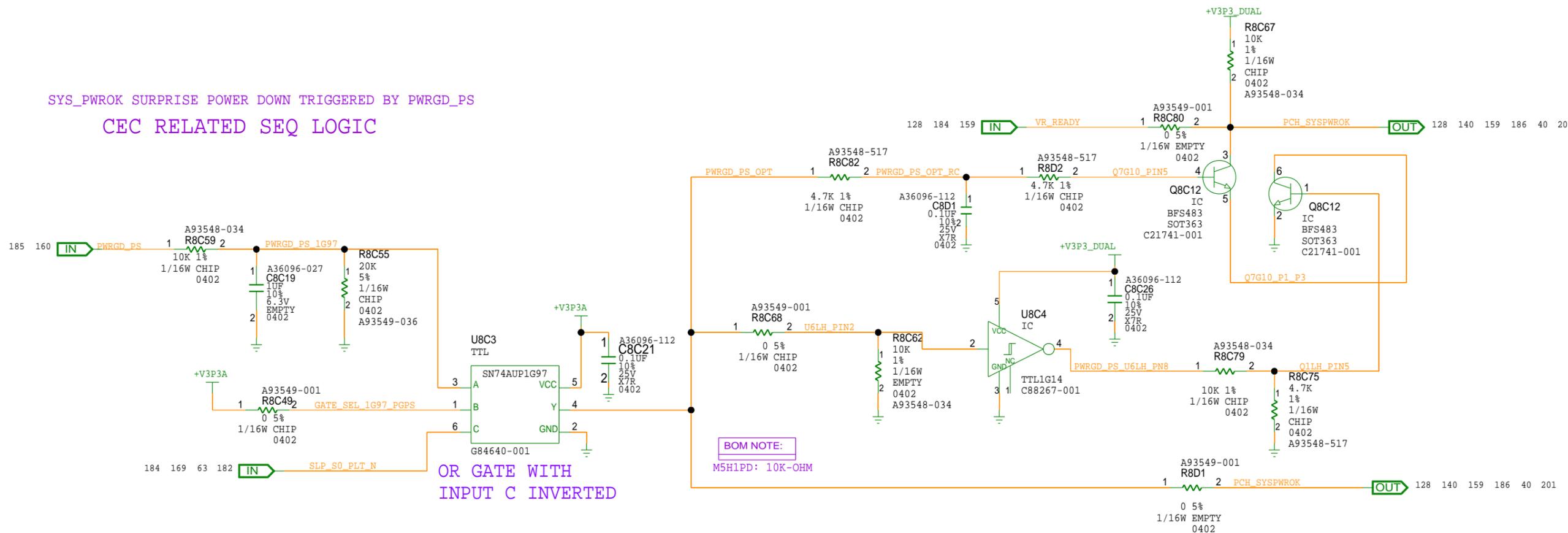
BACKFEED CUT & BACKFEED CUT LAN LOGIC



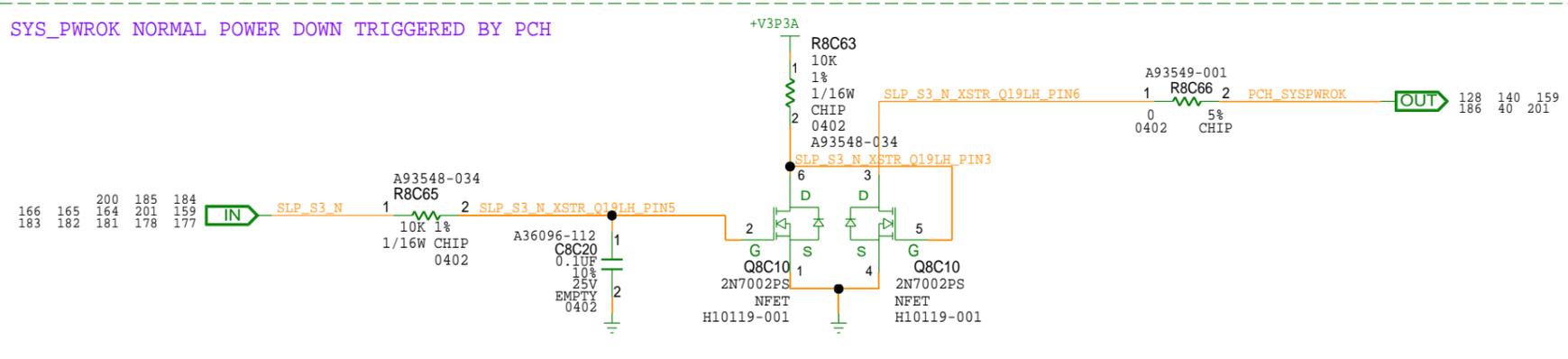
MODULE REV DETAILS

MODULE NAME	REV	DATE

SYS_PWROK SURPRISE POWER DOWN TRIGGERED BY PWRGD_PS
CEC RELATED SEQ LOGIC



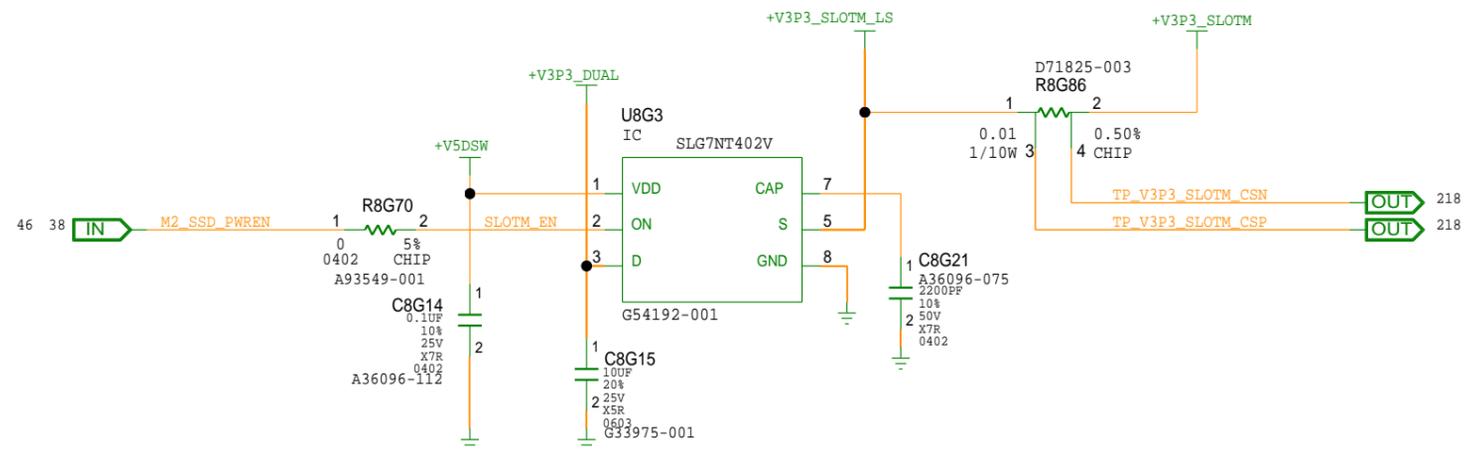
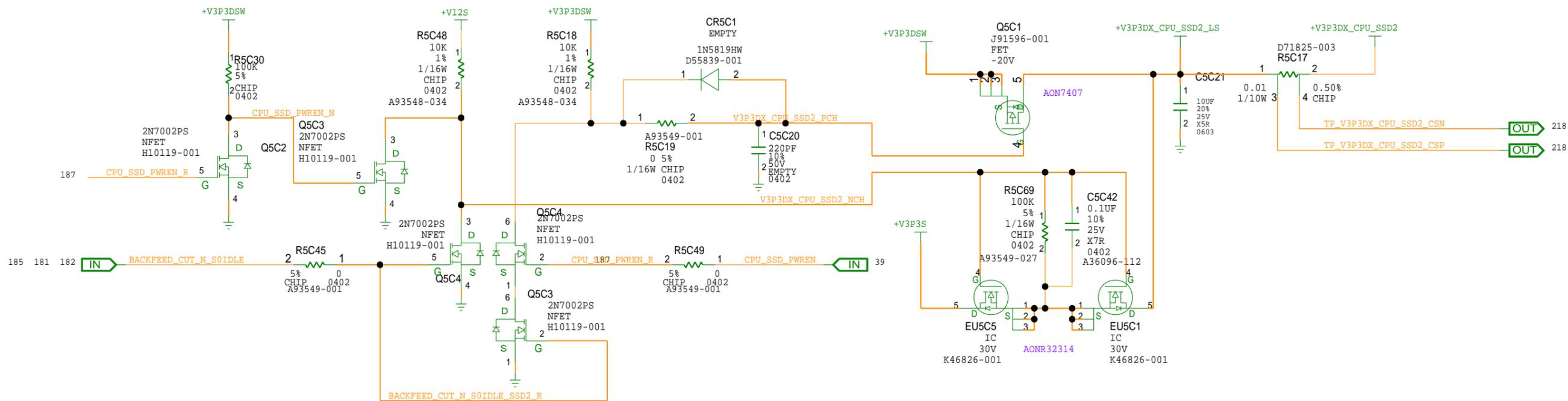
SYS_PWROK NORMAL POWER DOWN TRIGGERED BY PCH



MODULE REV DETAILS

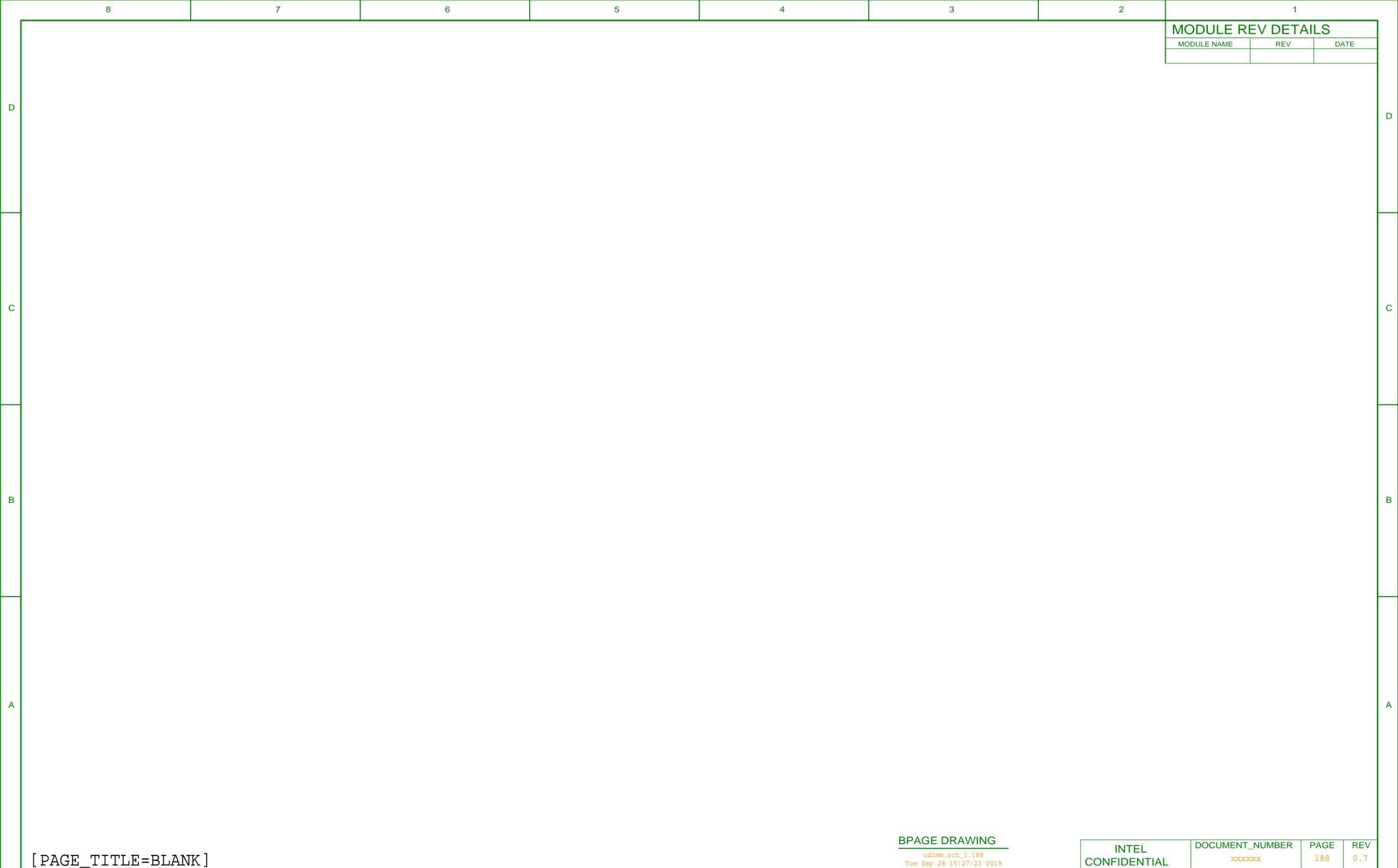
MODULE NAME	REV	DATE

V3P3DX_CPU_SSD2 GEN



MODULE REV DETAILS

MODULE NAME	REV	DATE



[PAGE_TITLE=BLANK]

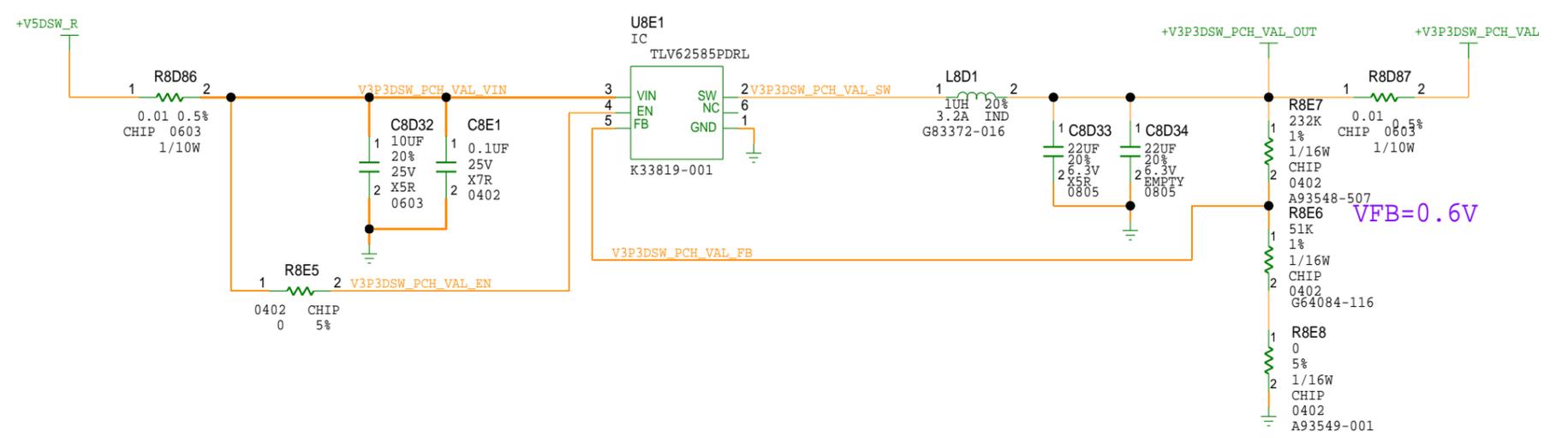
BPAGE DRAWING

udimm.sch_1.188
Tue Sep 24 15:27:23 2019

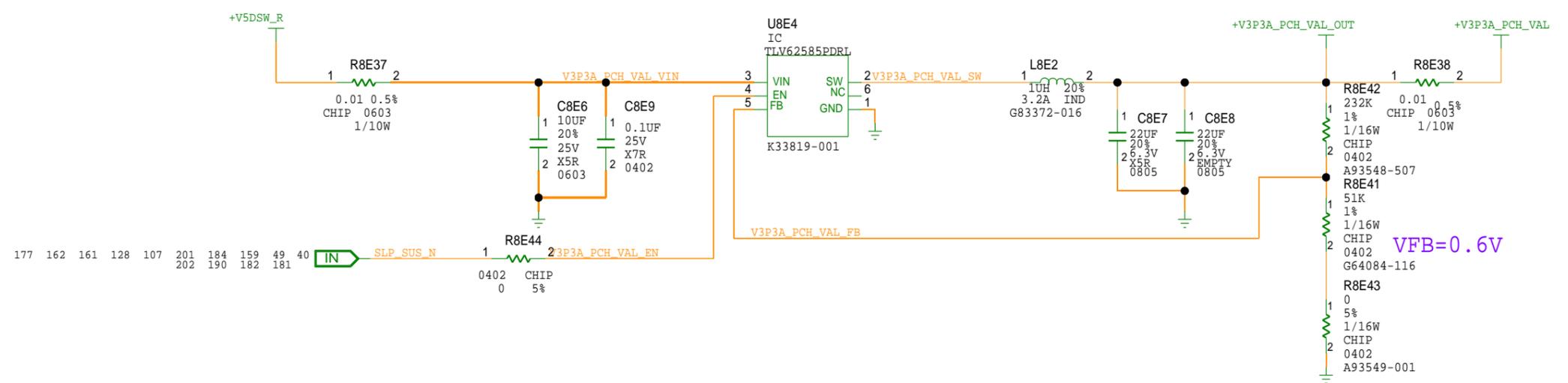
INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 188	REV 0.7
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MODULE REV DETAILS		
MODULE NAME	REV	DATE

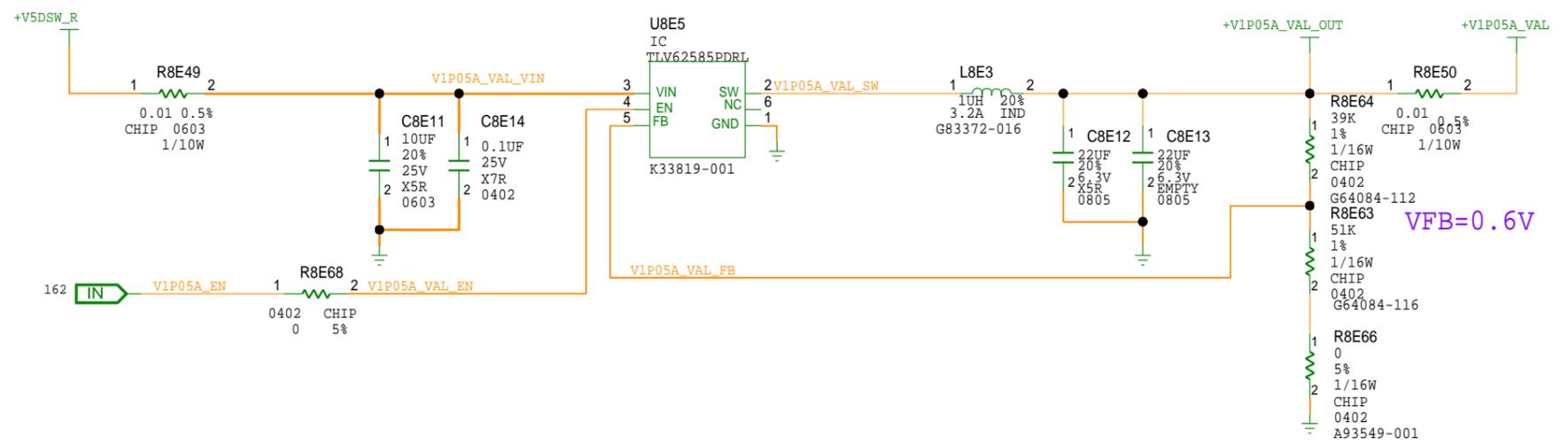
V3P3DSW_PCH_VAL RAIL - POWER CONVERSION



V3P3A_PCH_VAL RAIL - POWER CONVERSION



V1P05A_VAL RAIL - POWER CONVERSION



BPAGE DRAWING
 udimm.sch_1.189
 Fri Sep 27 16:42:16 2019

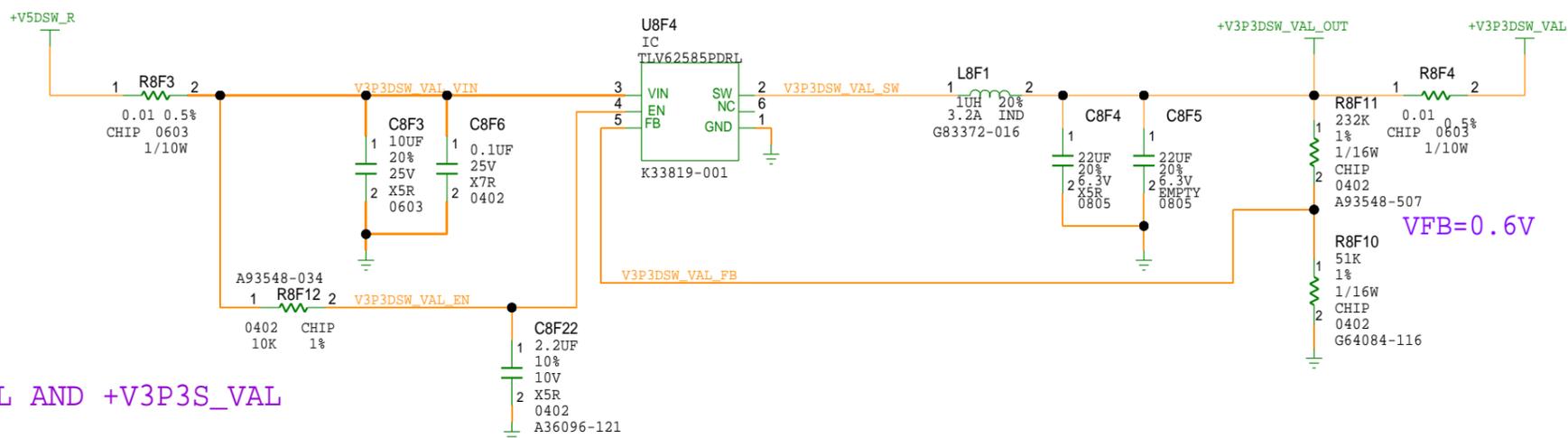
[PAGE_TITLE=V3P3DSW, V3P3A AND V1P05A VAL RAILS]

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 189	REV 0.7
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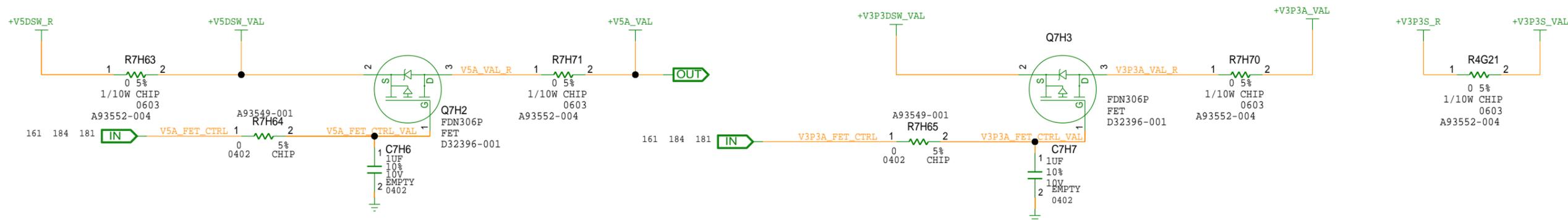
V3P3DSW VAL RAIL - POWER CONVERSION

MODULE REV DETAILS

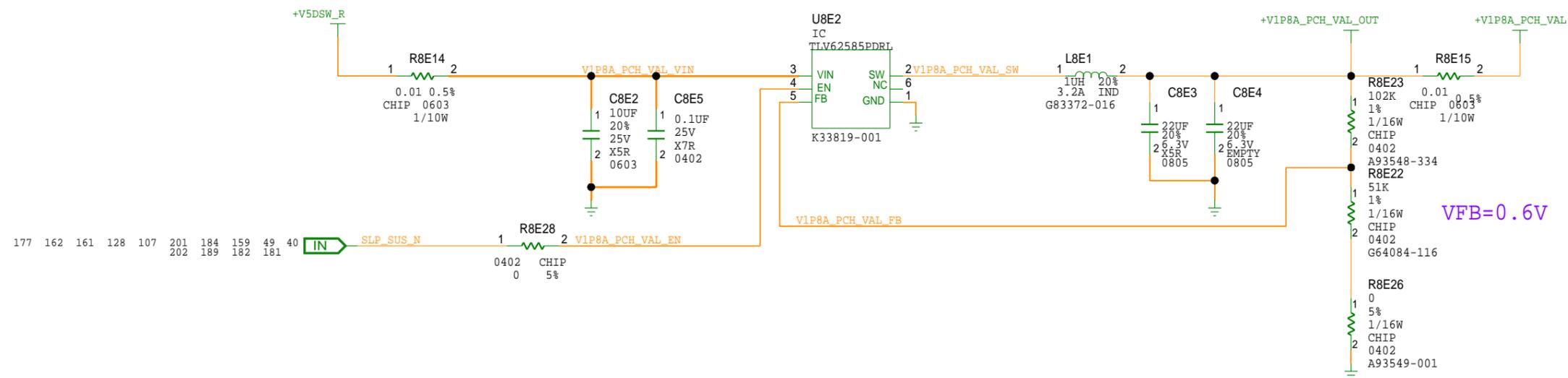
MODULE NAME	REV	DATE



+V5A_VAL, +V3P3A_VAL AND +V3P3S_VAL



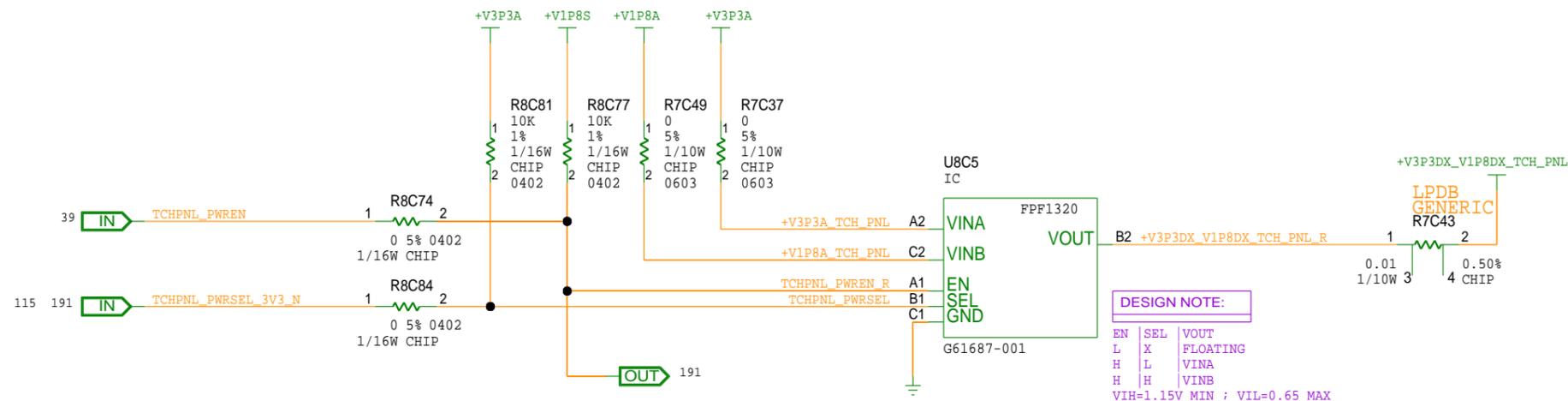
V1P8A_PCH_VAL RAIL - POWER CONVERSION



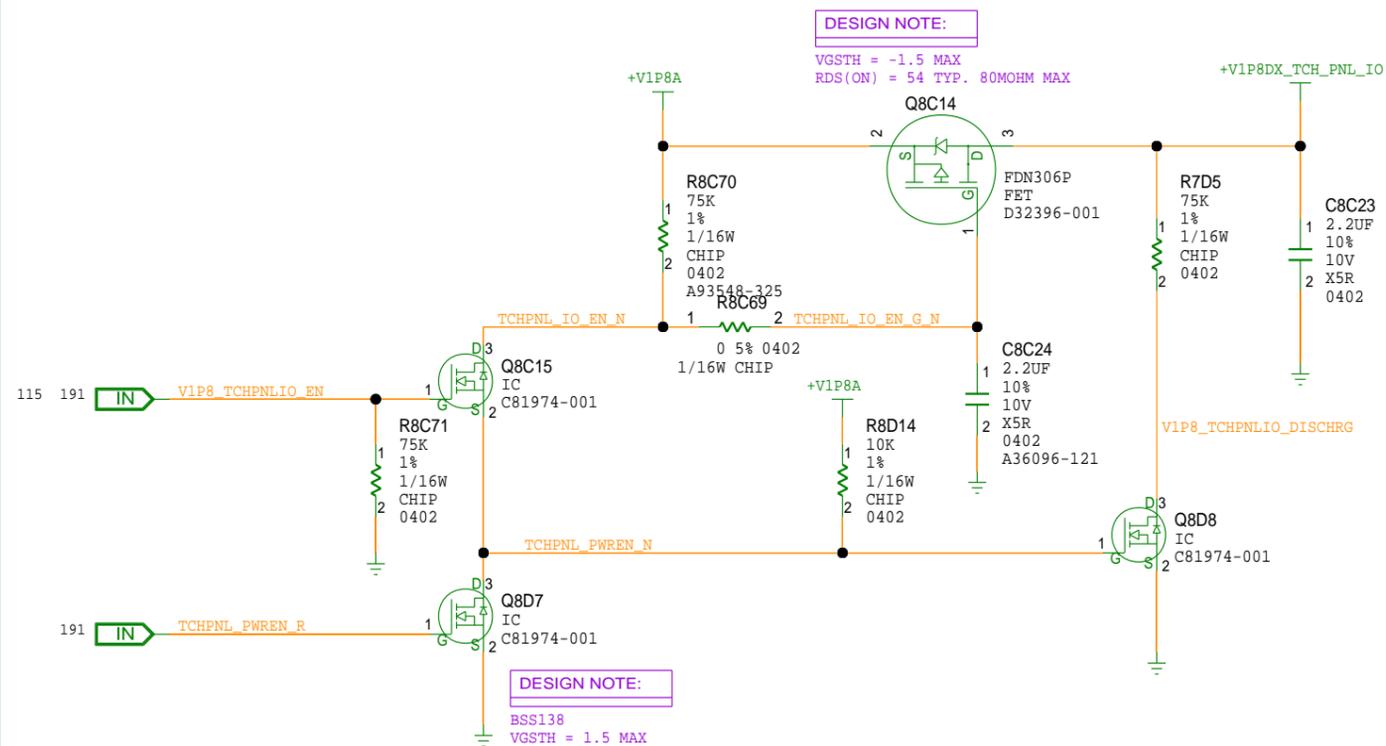
MODULE REV DETAILS

MODULE NAME	REV	DATE

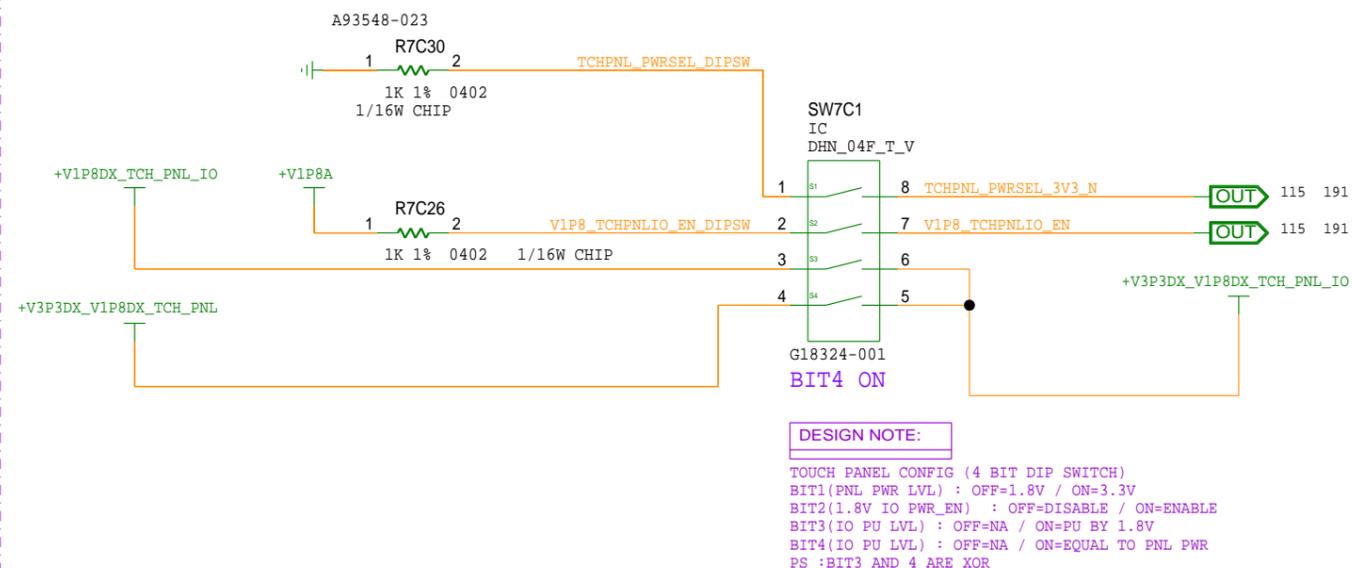
TOUCH PANEL POWER



TOUCH PANEL 1.8V IO POWER



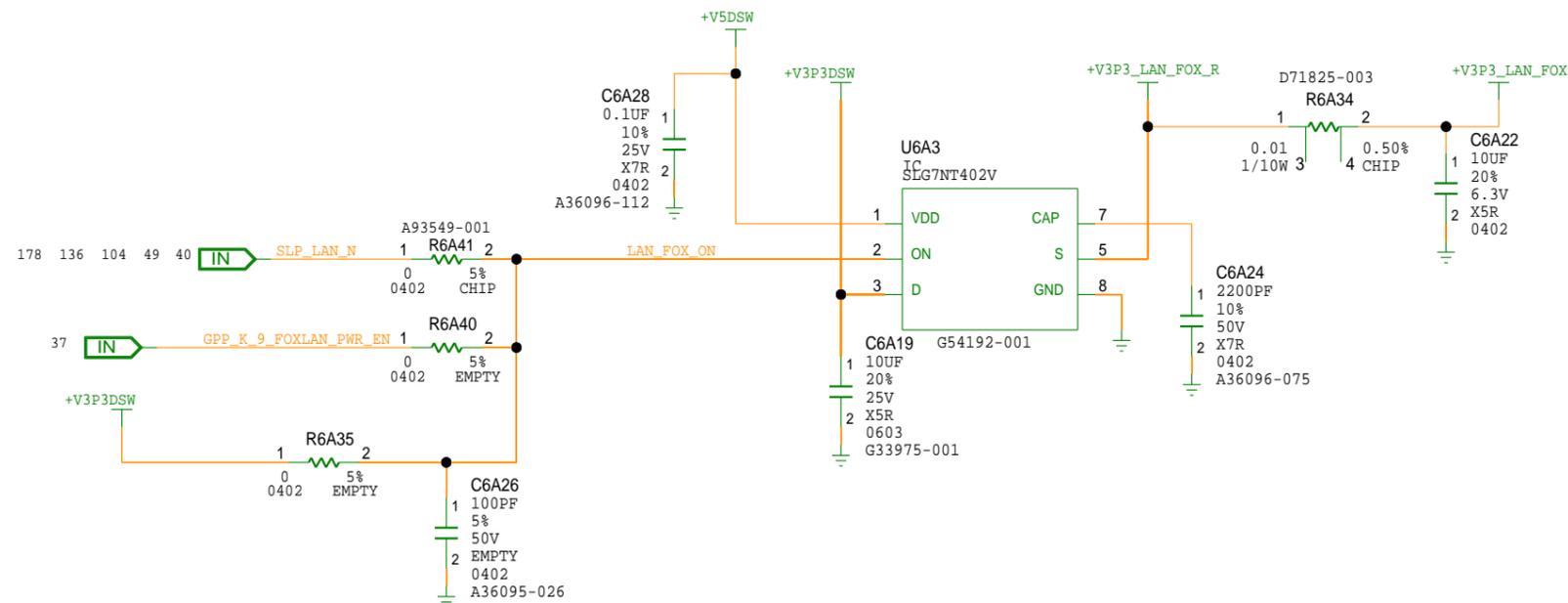
TOUCH PANEL POWER CONFIGURATION



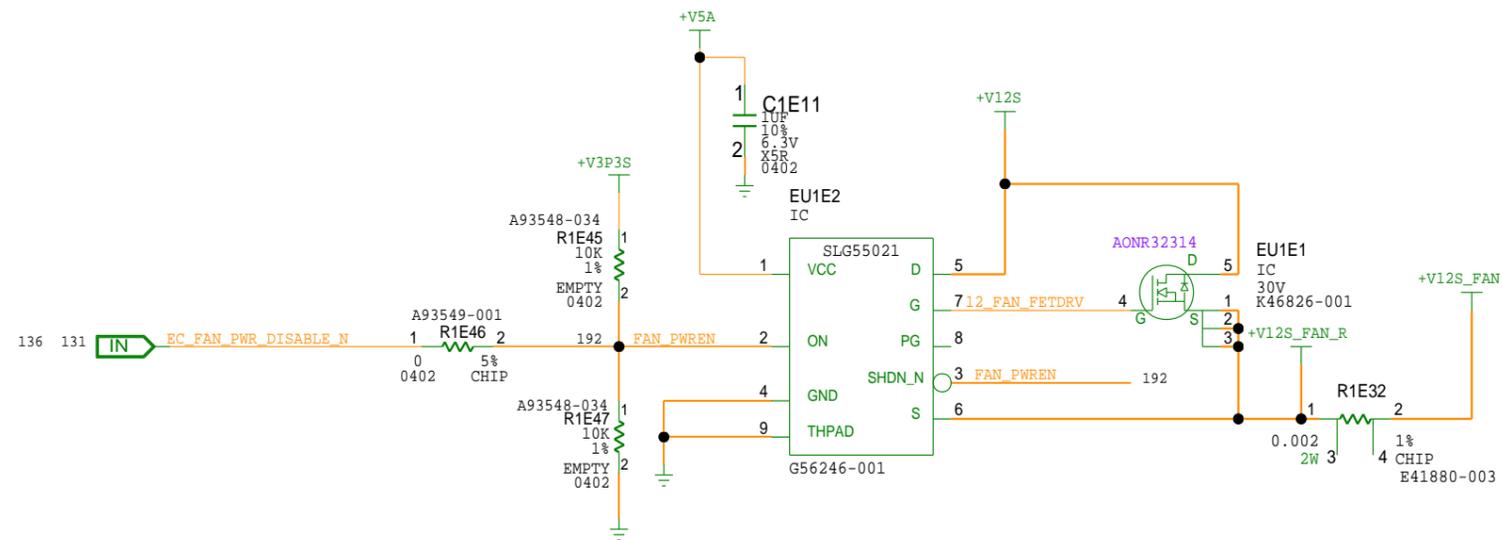
MODULE REV DETAILS

MODULE NAME	REV	DATE

FOXVILLE LAN POWER



12V FAN POWER



8

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MODULE REV DETAILS

MODULE NAME	REV	DATE

D

D

C

C

B

B

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A

[PAGE_TITLE= BLANK]

BPAGE DRAWING

udimm.sch_1.193
Fri Sep 20 11:44:44 2019

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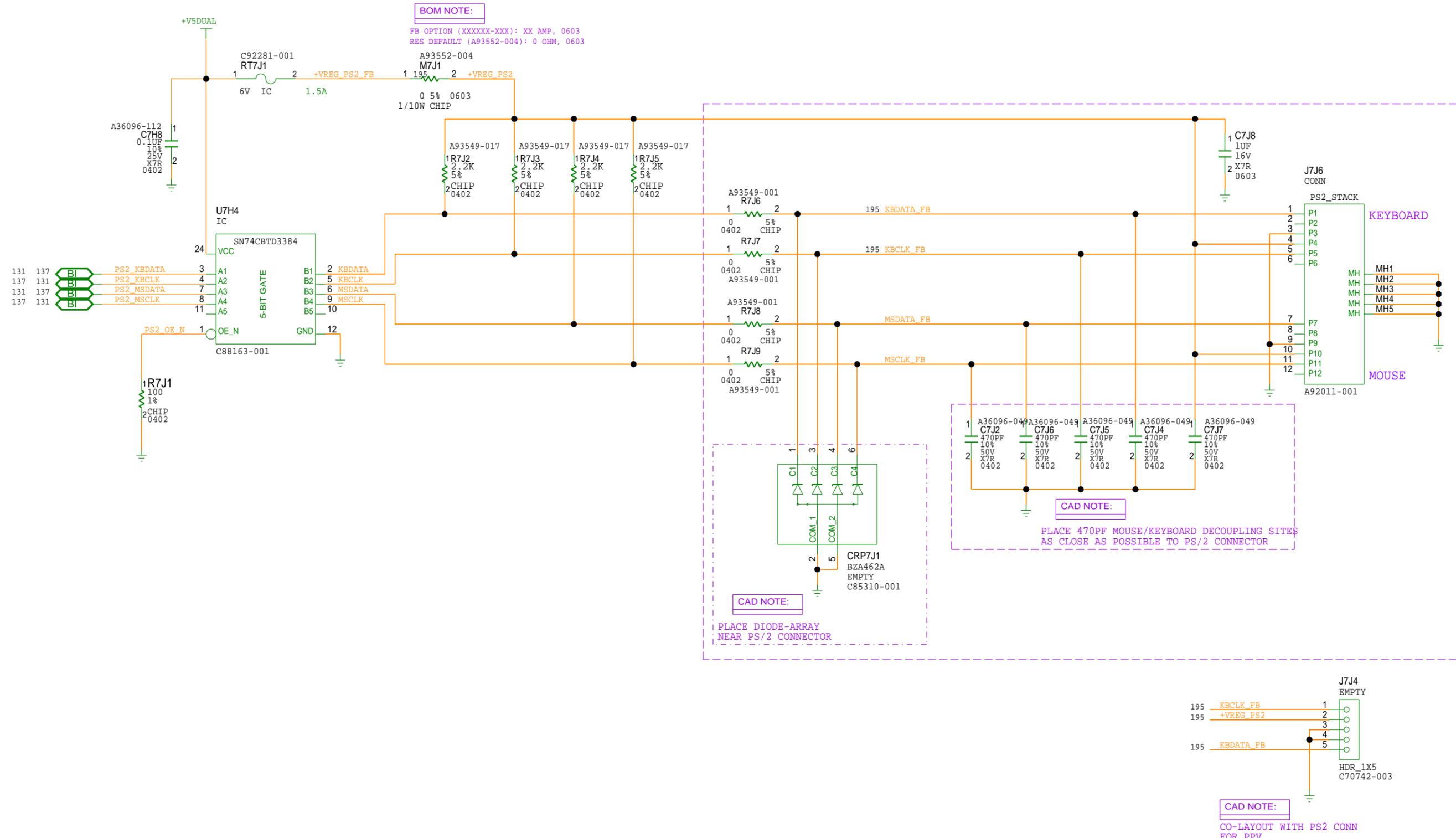
3

CUSTOM TEXT BPAGE

1

MODULE REV DETAILS

MODULE NAME	REV	DATE



[PAGE_TITLE=EV - PS\2]

BPAGE DRAWING
 udimm.sch_1.195
 Fri Sep 27 16:42:21 2019

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MODULE REV DETAILS

MODULE NAME	REV	DATE

D

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C

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A

[PAGE_TITLE=BLANK]

BPAGE DRAWING

udimm.sch_1.196
Tue Sep 24 14:57:30 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 196	REV 0.7
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8

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MODULE REV DETAILS

MODULE NAME	REV	DATE

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D

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A

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BPAGE DRAWING

udimm.sch_1.197
Fri Sep 20 11:34:45 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 197	REV 0.7
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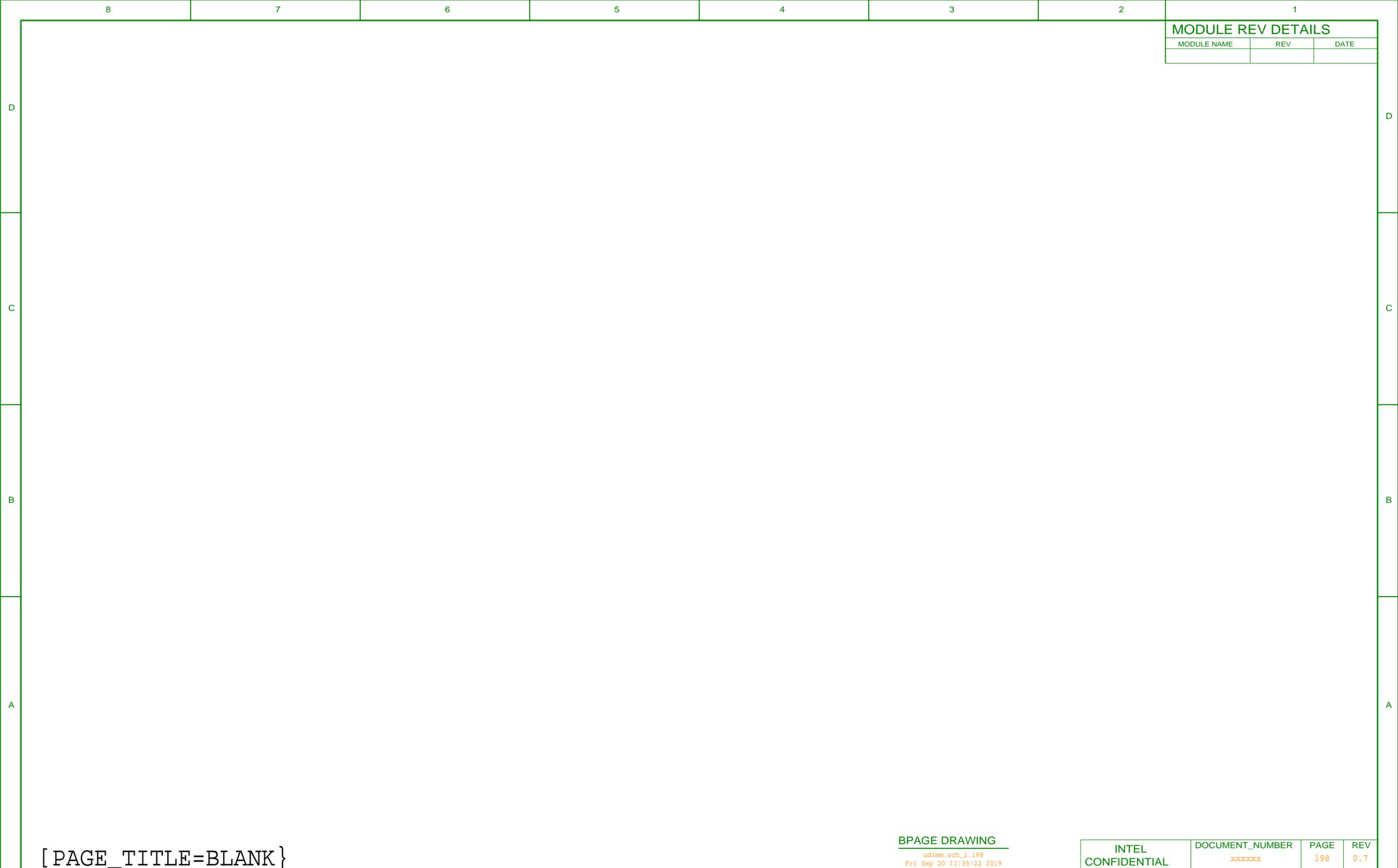
3

2

1

MODULE REV DETAILS

MODULE NAME	REV	DATE



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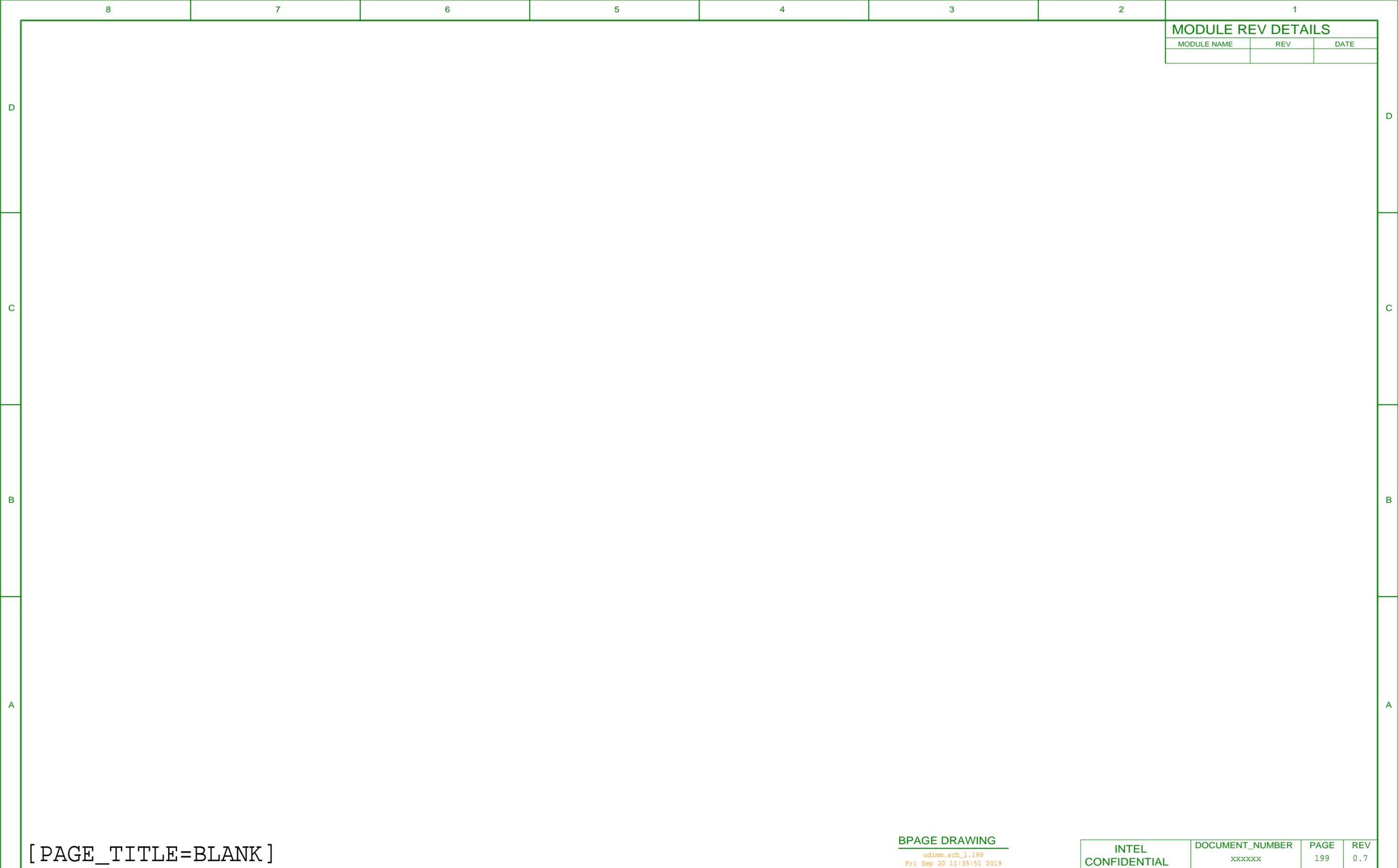
BPAGE DRAWING

udimm.sch_1.198
Fri Sep 20 11:35:22 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 198	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE



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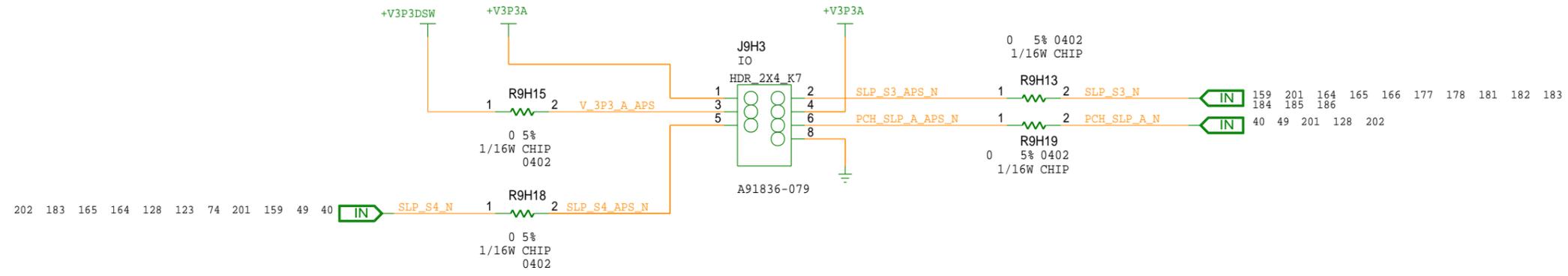
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udimm.sch_1.199
Fri Sep 20 11:35:51 2019

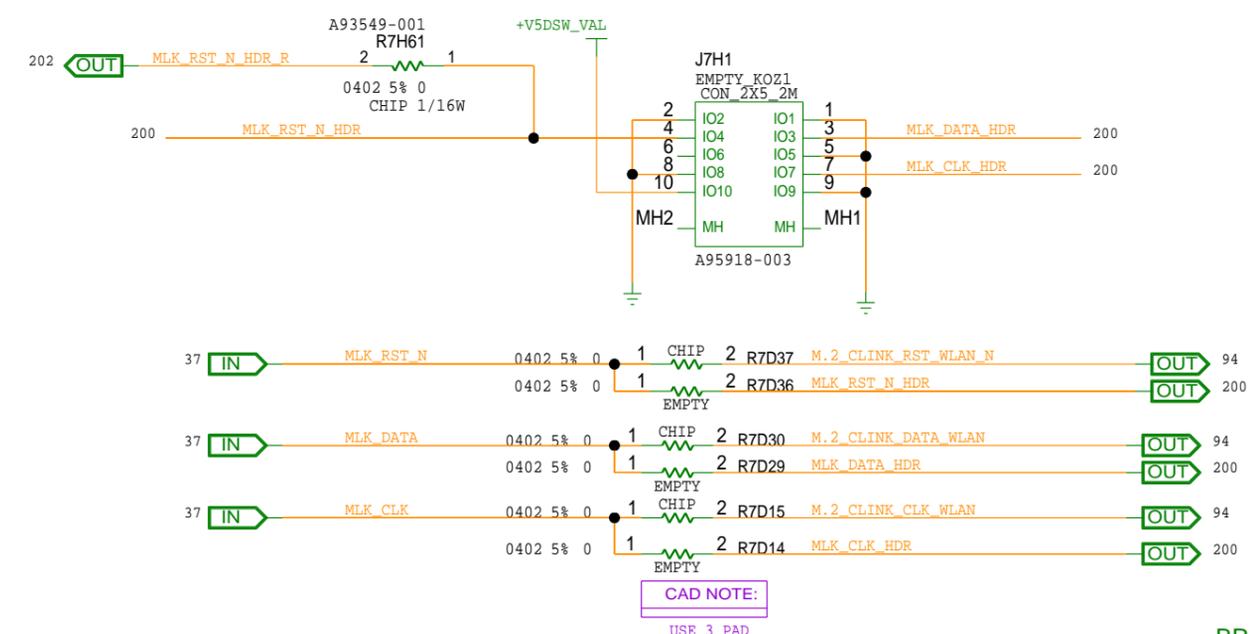
INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 199	REV 0.7
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MODULE REV DETAILS		
MODULE NAME	REV	DATE

APS HEADER



MLINK HEADER



CAD NOTE:
USE 3 PAD

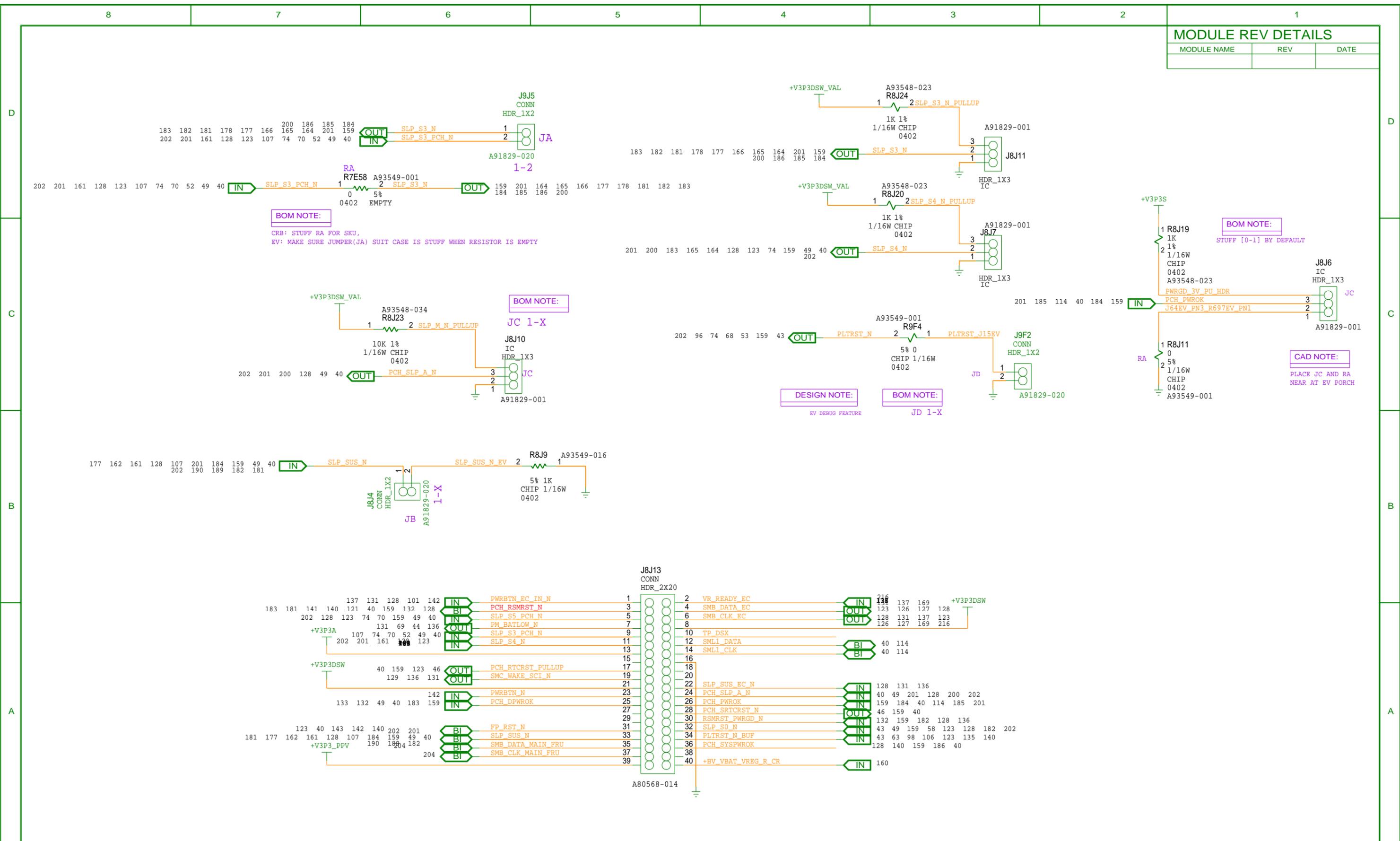
[PAGE_TITLE=EV - DEBUG HEADERS]

BPAGE DRAWING
udimm.sch_1.200
Fri Sep 27 16:42:23 2019

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MODULE REV DETAILS

MODULE NAME	REV	DATE



BOM NOTE:
 CRB: STUFF RA FOR SKU,
 EV: MAKE SURE JUMPER(JA) SUIT CASE IS STUFF WHEN RESISTOR IS EMPTY

BOM NOTE:
 JC 1-X

DESIGN NOTE:
 EV DEBUG FEATURE

BOM NOTE:
 JD 1-X

BOM NOTE:
 STUFF [0-1] BY DEFAULT

CAD NOTE:
 PLACE JC AND RA
 NEAR AT EV PORCH

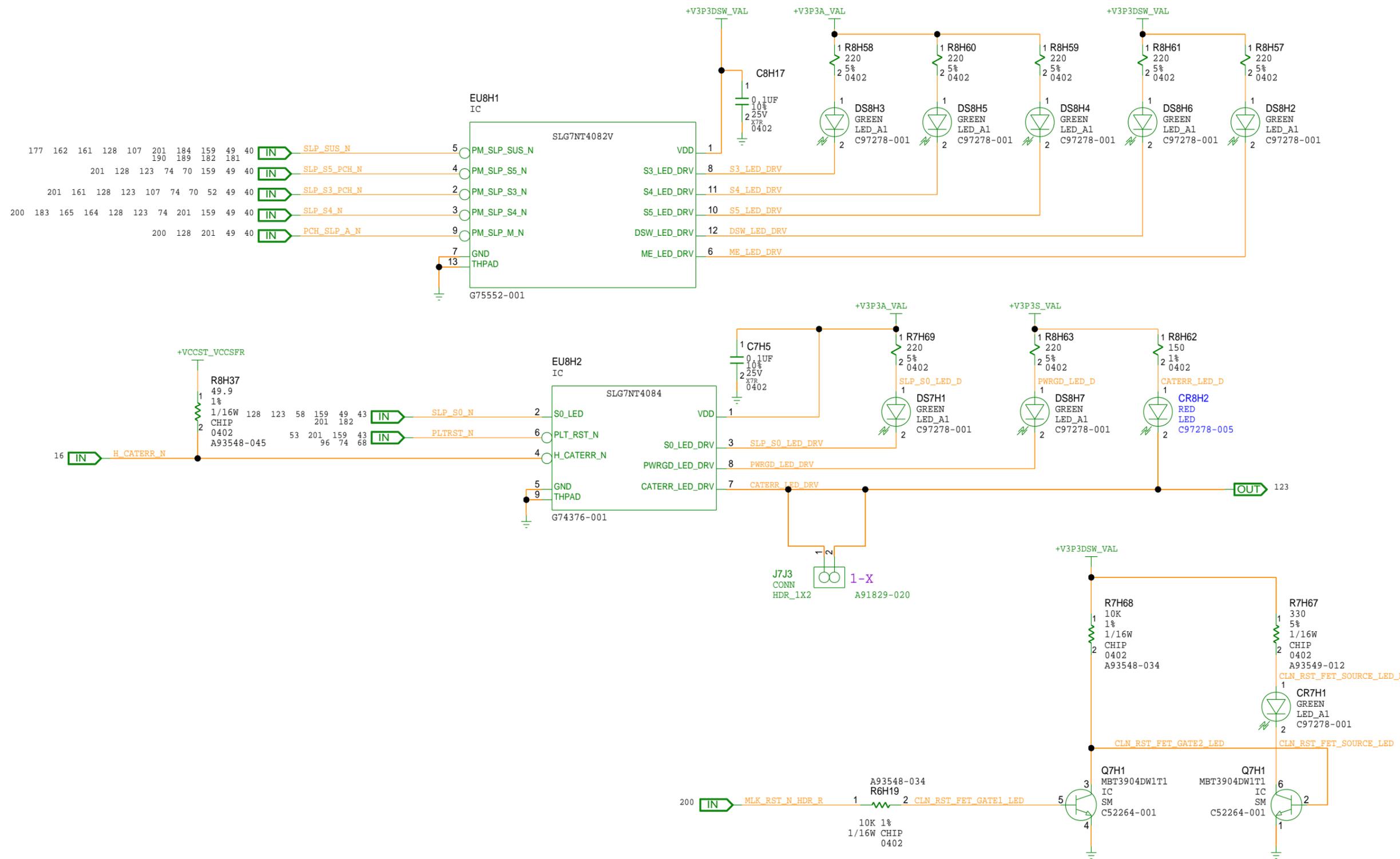
[PAGE_TITLE=EV - PM SIDEBAND HEADER]

BPAGE DRAWING
 udimm.sch_1.201
 Fri Sep 27 16:42:24 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 201	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE



[PAGE_TITLE=EV - LEDS]

BPAGE DRAWING
 udimm.sch_1.202
 Fri Sep 27 16:42:25 2019

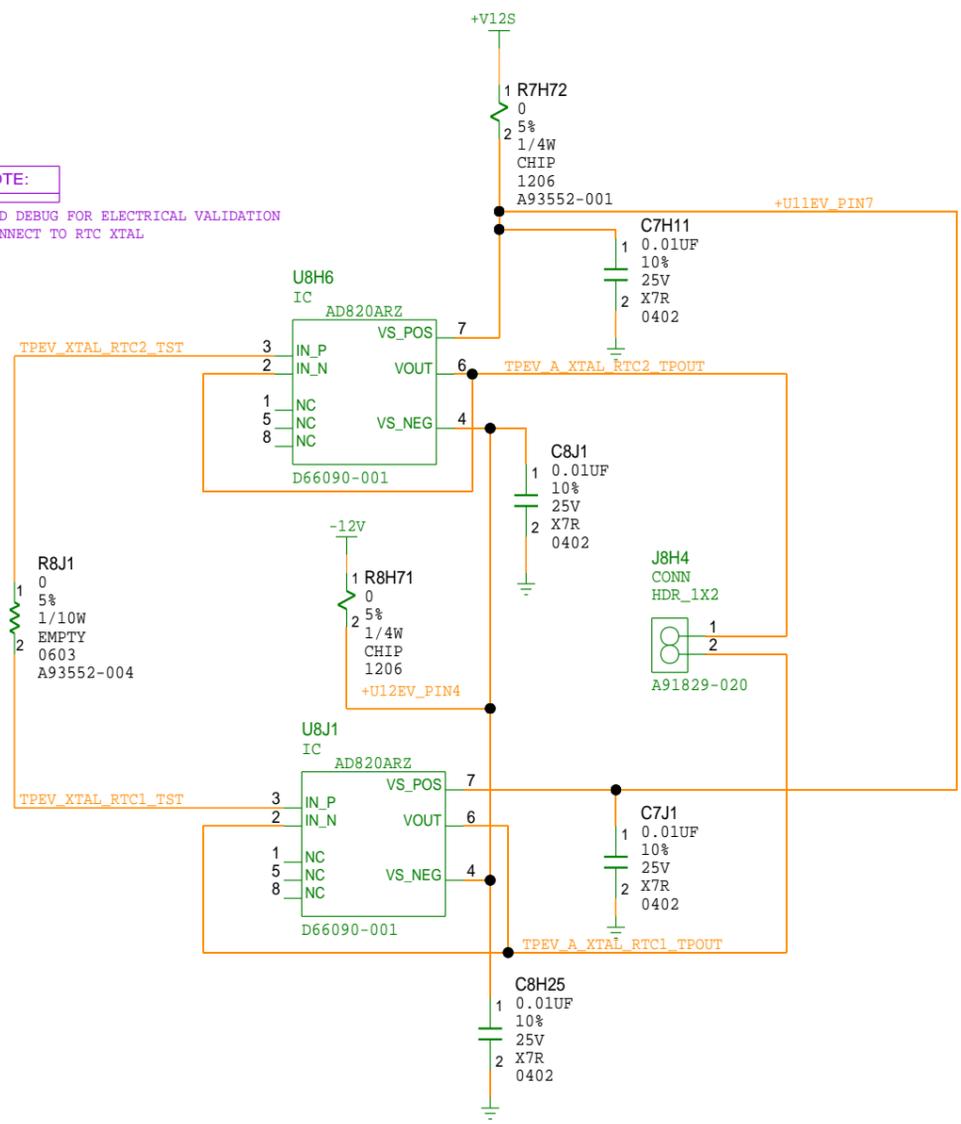
INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 202	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE

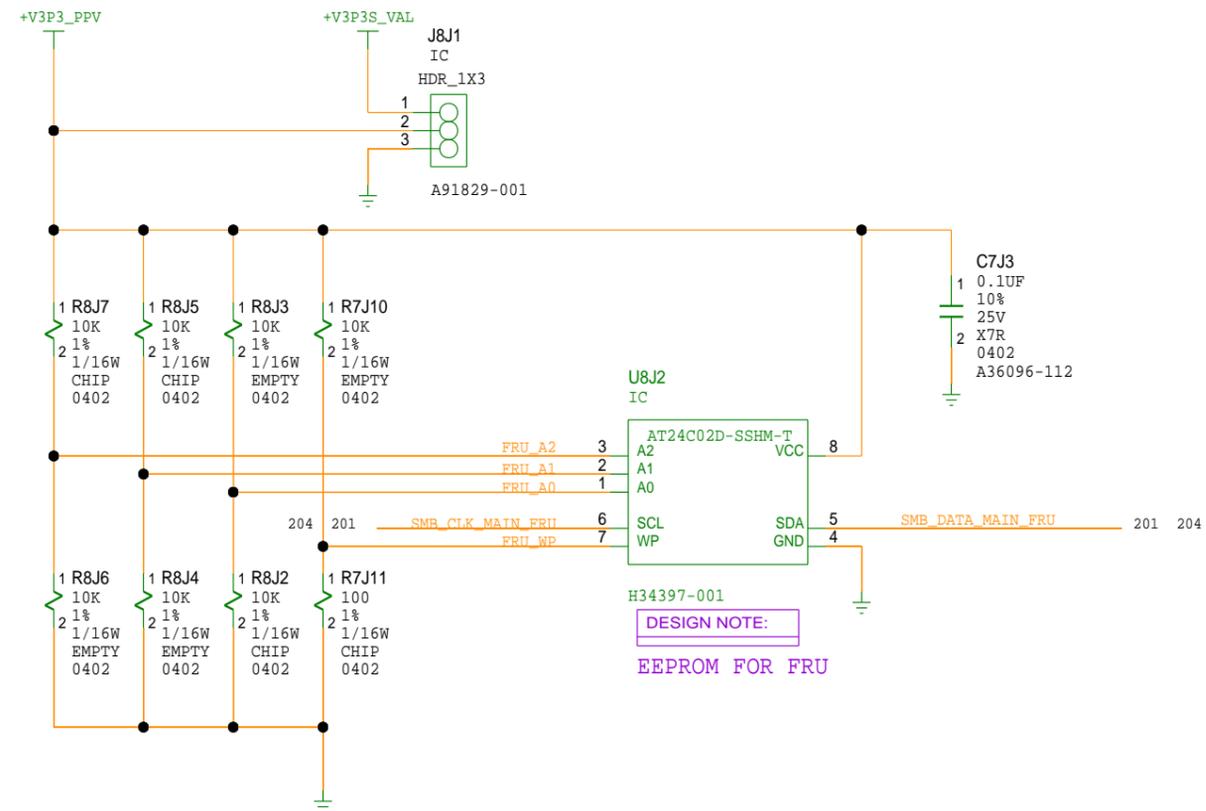
DESIGN NOTE:
 RTC CHECKING AND DEBUG FOR ELECTRICAL VALIDATION
 BLUE-WIRE TO CONNECT TO RTC XTAL

DESIGN NOTE:
 R4J5EV IS PAD FOR BLUE WIRE

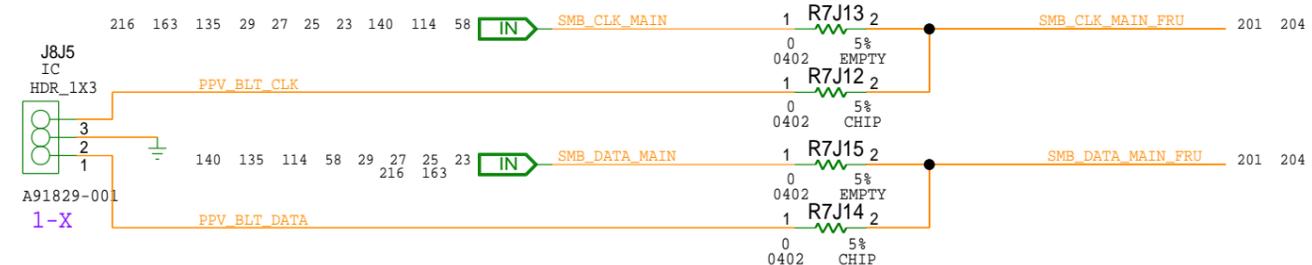


MODULE REV DETAILS

MODULE NAME	REV	DATE



DESIGN NOTE:
EEPROM FOR FRU



CAD NOTE:
3 PAD SHARING

MODULE REV DETAILS

MODULE NAME	REV	DATE



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BPAGE DRAWING

udimm.sch_1.205
Fri Sep 20 11:44:59 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 205	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE

D

D

C

C

B

B

A

A

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BPAGE DRAWING
 udimm.sch_1.206
 Fri Sep 20 11:39:59 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 206	REV 0.7
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8

7

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2

1

MODULE REV DETAILS

MODULE NAME	REV	DATE

D

D

C

C

B

B

A

A

[PAGE_TITLE=BLANK]

BPAGE DRAWING

udimm.sch_1.207
Fri Sep 20 11:40:10 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 207	REV 0.7
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CUSTOM TEXT BPAGE

8

7

6

5

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1

8

7

6

5

4

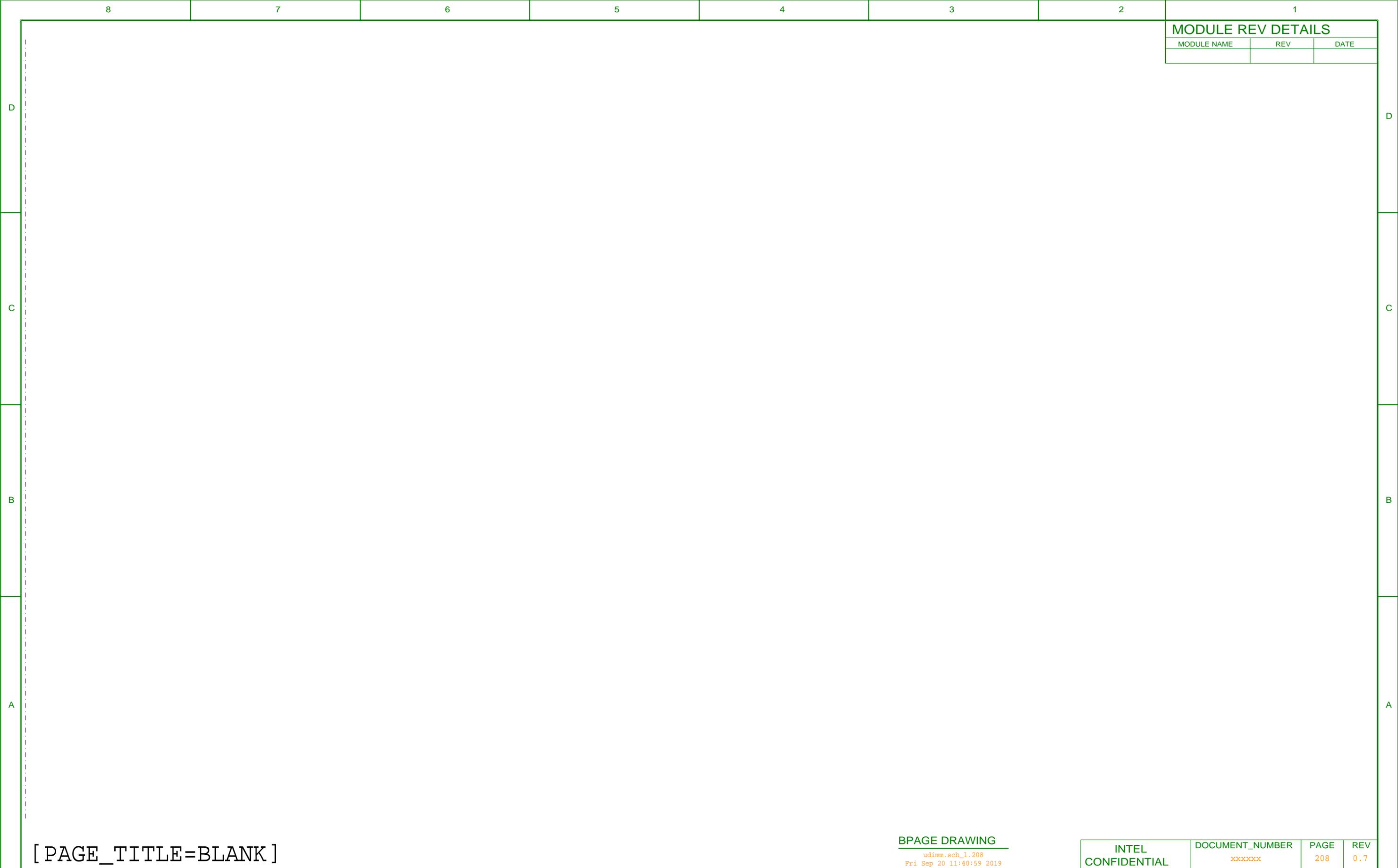
3

2

1

MODULE REV DETAILS

MODULE NAME	REV	DATE



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BPAGE DRAWING

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Fri Sep 20 11:40:59 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 208	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE



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BPAGE DRAWING

udimm.sch_1.209
Fri Sep 20 11:42:01 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 209	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE



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BPAGE DRAWING

udimm.sch_1.210
Fri Sep 20 11:42:29 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 210	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE



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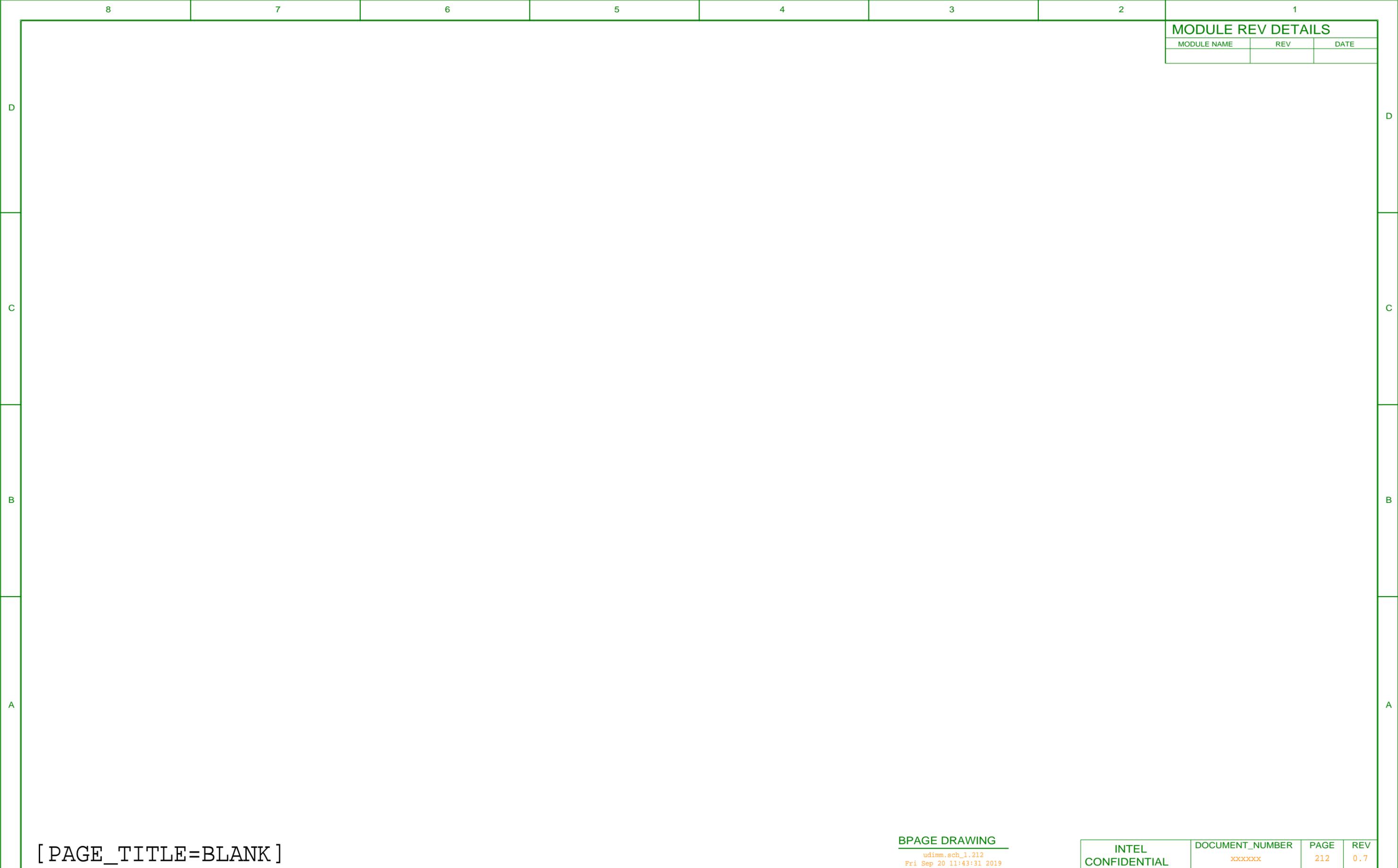
BPAGE DRAWING

udimm.sch_1.211
Fri Sep 20 11:43:04 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 211	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE



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BPAGE DRAWING

udimm.sch_1.212
Fri Sep 20 11:43:31 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 212	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE



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BPAGE DRAWING

udimm.sch_1.213
Fri Sep 20 11:44:06 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 213	REV 0.7
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MODULE REV DETAILS

MODULE NAME	REV	DATE



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BPAGE DRAWING

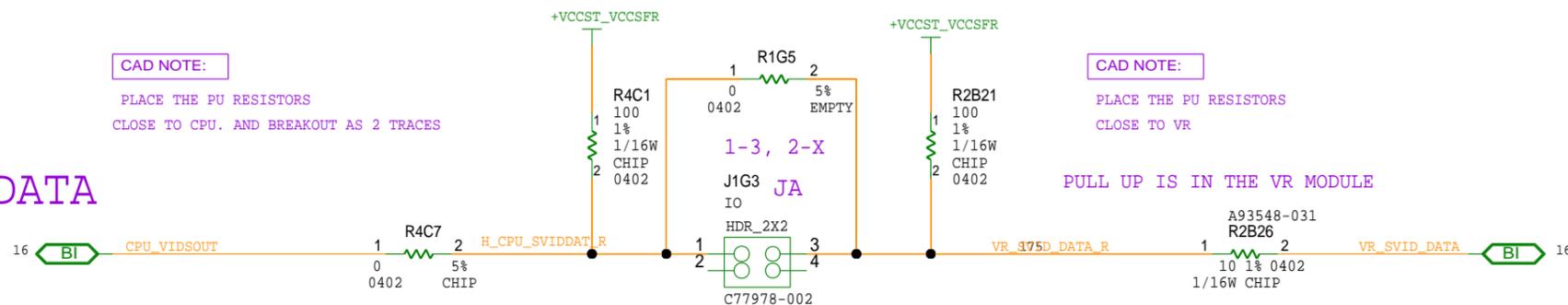
udimm.sch_1.214
Fri Sep 20 11:44:35 2019

INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 214	REV 0.7
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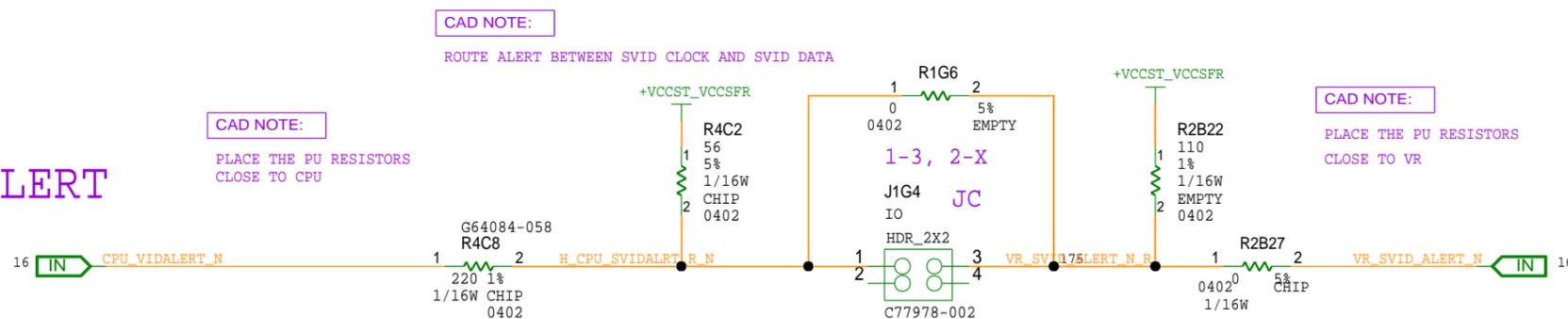
MODULE REV DETAILS

MODULE NAME	REV	DATE

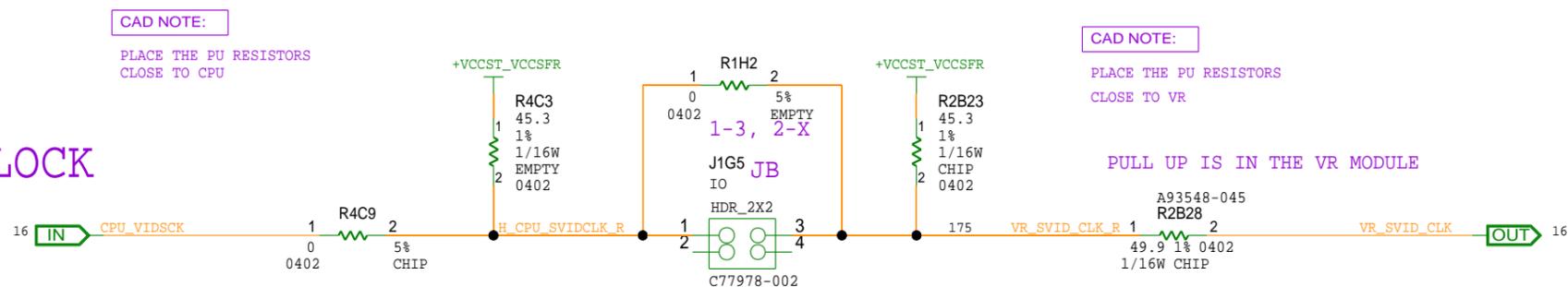
SVID DATA



SVID ALERT



SVID CLOCK



DESIGN NOTE:

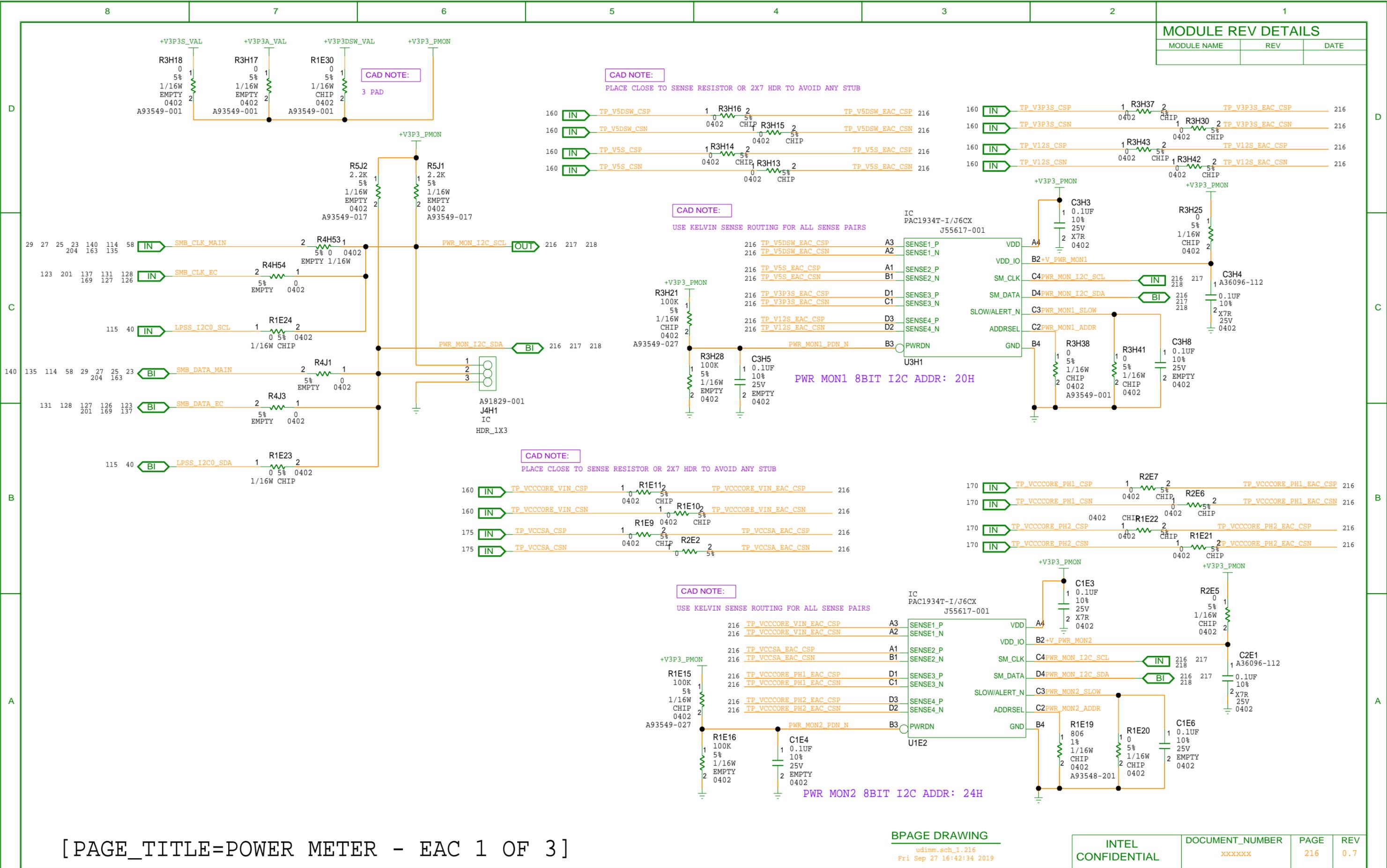
DEFAULT

STUFFING DETAILS ON THE BOARD

	JA	JB	JC
DEFAULT	1-3, 2-X	1-3, 2-X	1-3, 2-X

MODULE REV DETAILS

MODULE NAME	REV	DATE

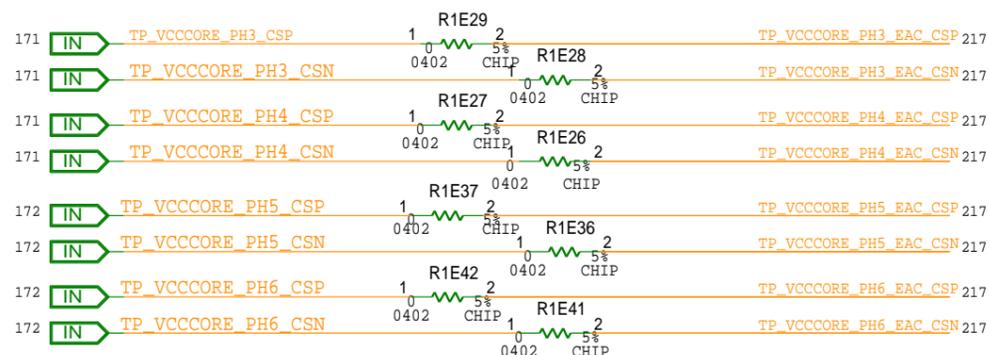


MODULE REV DETAILS

MODULE NAME	REV	DATE

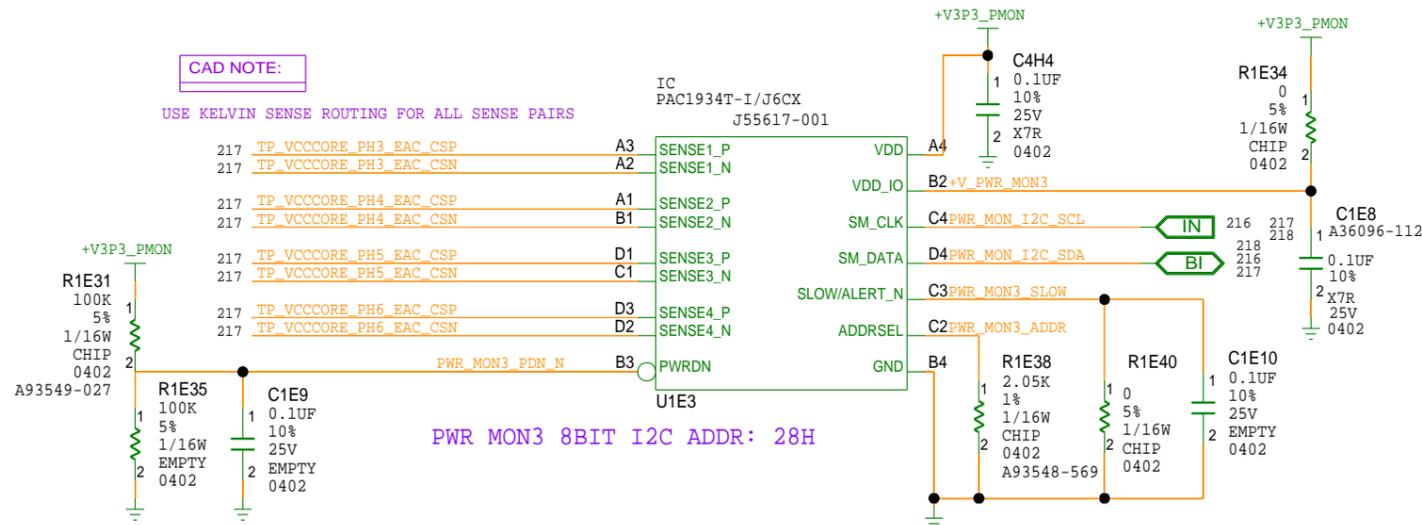
CAD NOTE:

PLACE CLOSE TO SENSE RESISTOR OR 2X7 HDR TO AVOID ANY STUB



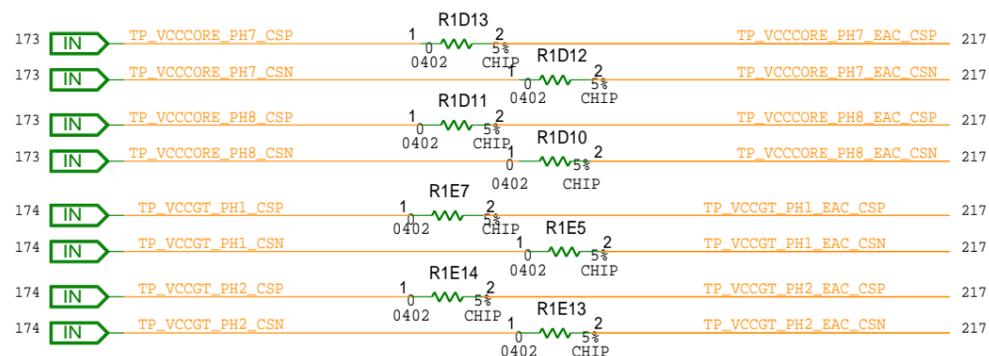
CAD NOTE:

USE KELVIN SENSE ROUTING FOR ALL SENSE PAIRS



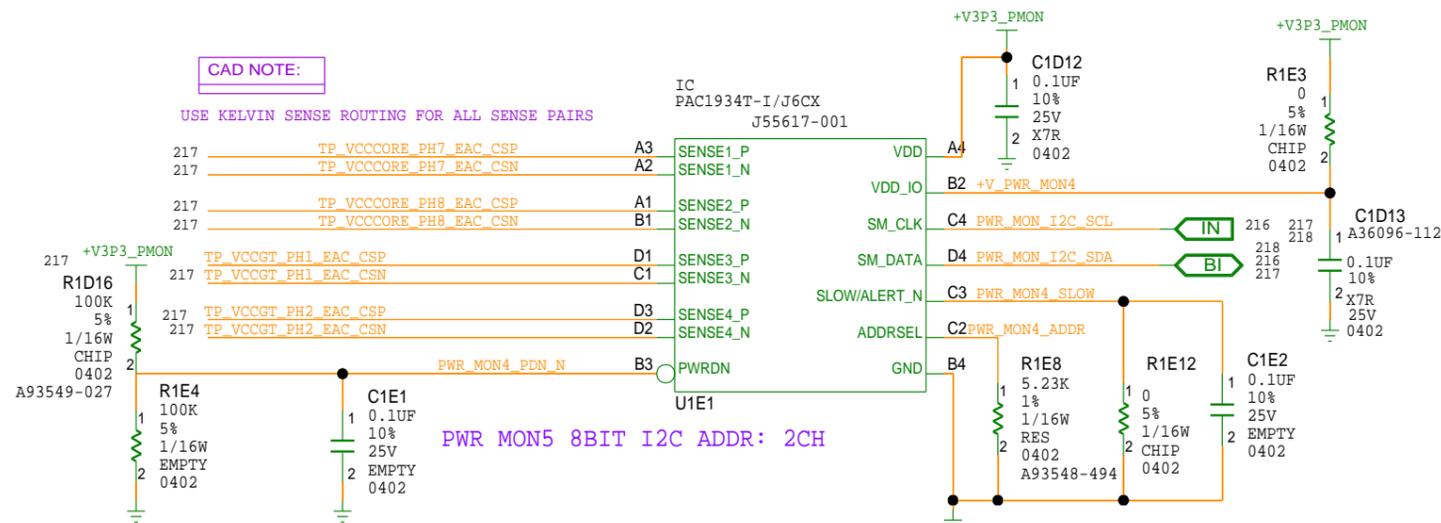
CAD NOTE:

PLACE CLOSE TO SENSE RESISTOR OR 2X7 HDR TO AVOID ANY STUB



CAD NOTE:

USE KELVIN SENSE ROUTING FOR ALL SENSE PAIRS

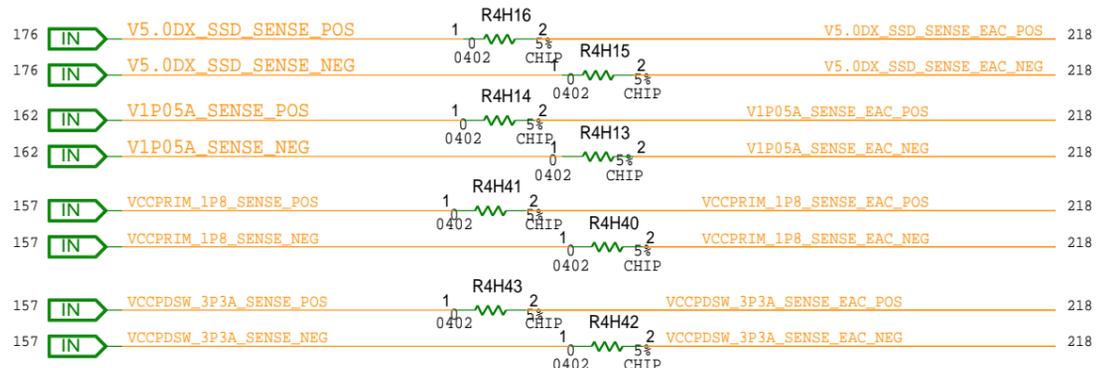


MODULE REV DETAILS

MODULE NAME	REV	DATE

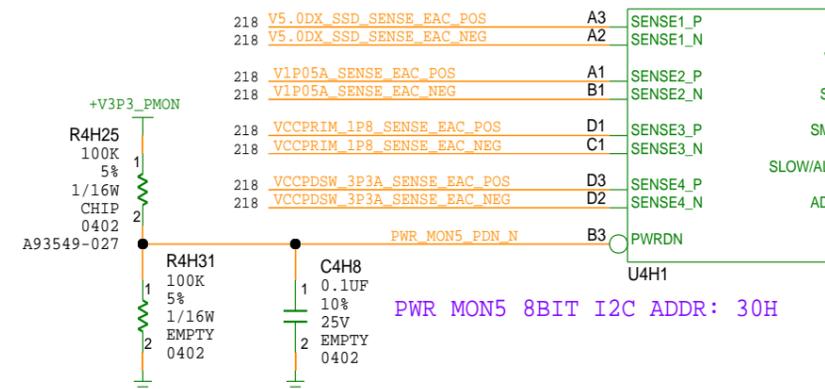
CAD NOTE:

PLACE CLOSE TO SENSE RESISTOR OR 2X7 HDR TO AVOID ANY STUB



CAD NOTE:

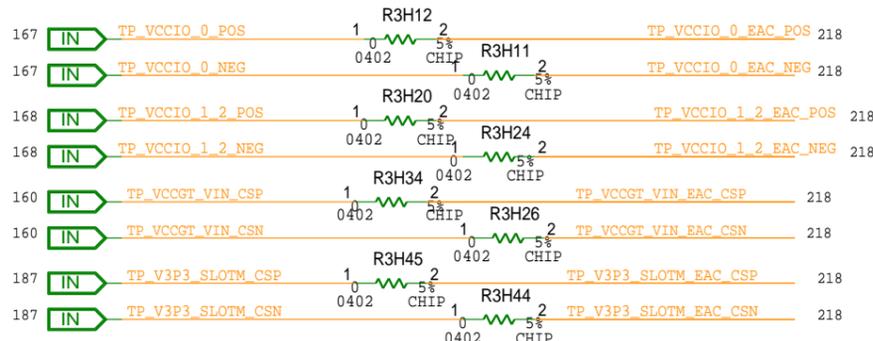
USE KELVIN SENSE ROUTING FOR ALL SENSE PAIRS



PWR MON5 8BIT I2C ADDR: 30H

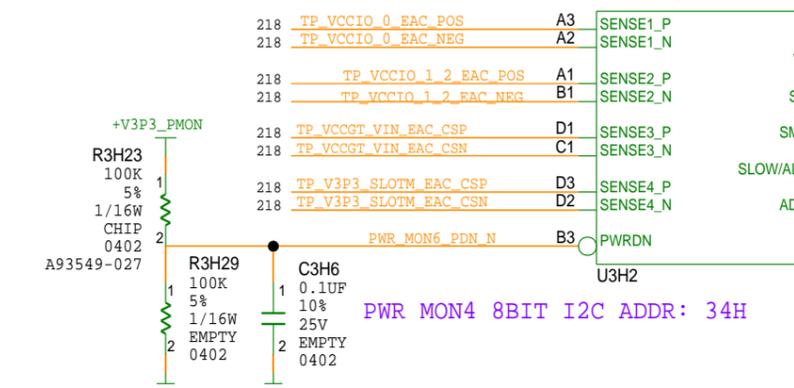
CAD NOTE:

PLACE CLOSE TO SENSE RESISTOR OR 2X7 HDR TO AVOID ANY STUB



CAD NOTE:

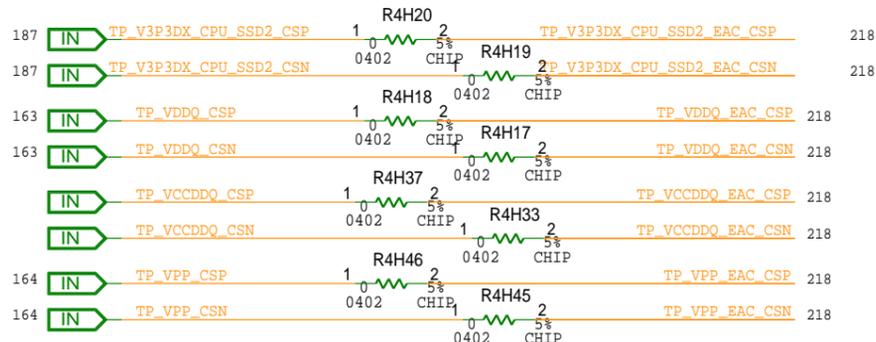
USE KELVIN SENSE ROUTING FOR ALL SENSE PAIRS



PWR MON4 8BIT I2C ADDR: 34H

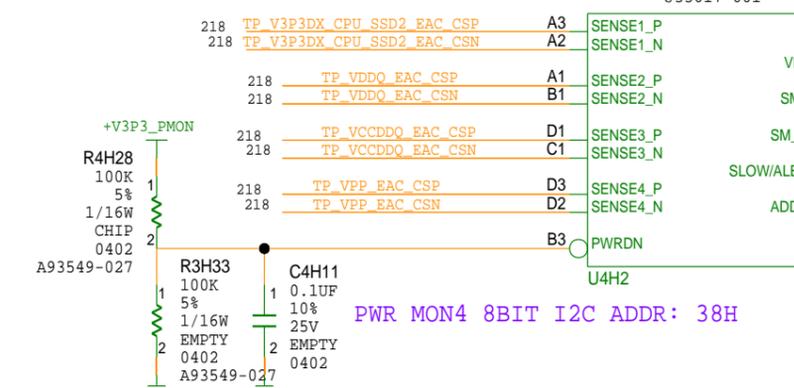
CAD NOTE:

PLACE CLOSE TO SENSE RESISTOR OR 2X7 HDR TO AVOID ANY STUB



CAD NOTE:

USE KELVIN SENSE ROUTING FOR ALL SENSE PAIRS



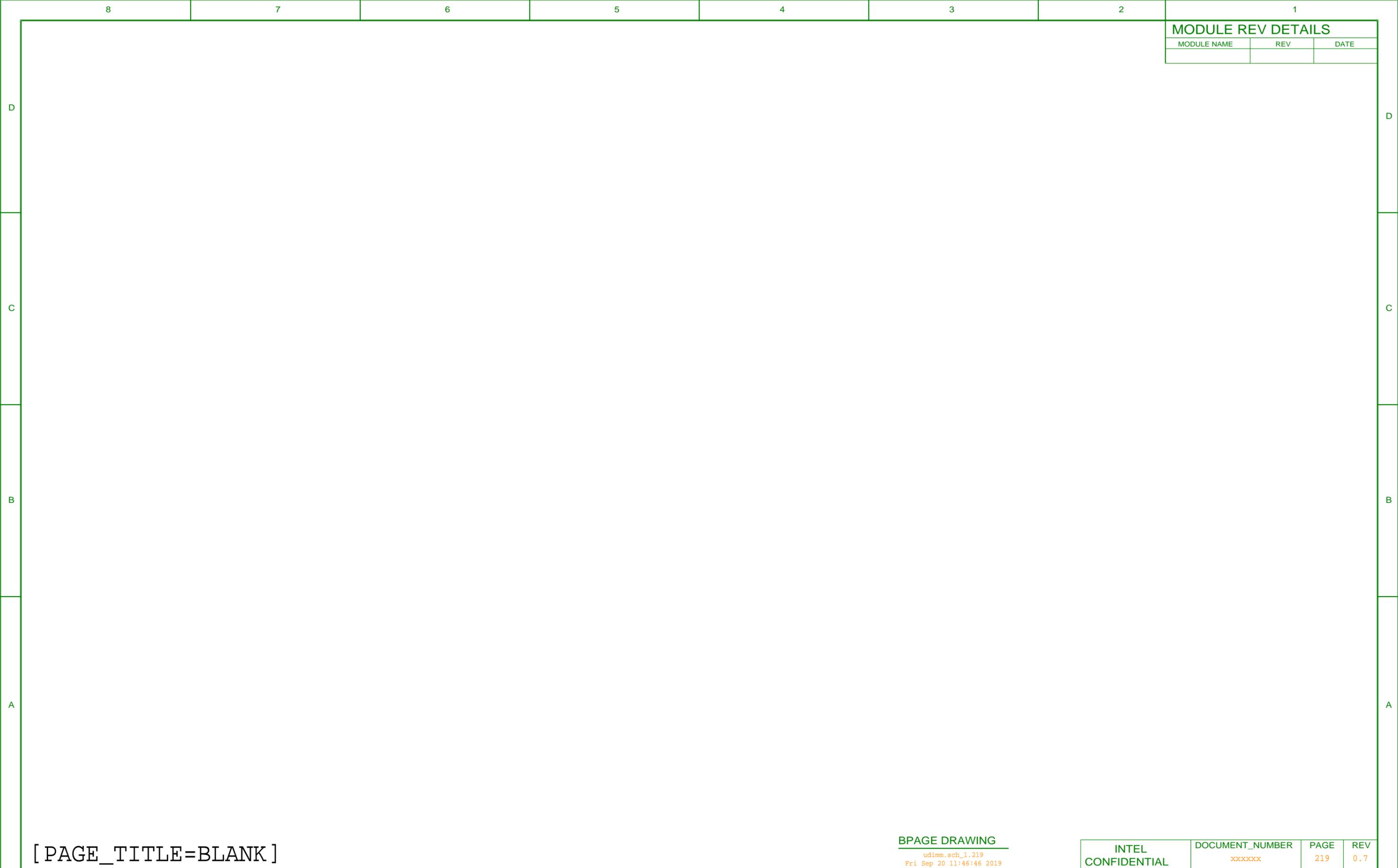
PWR MON4 8BIT I2C ADDR: 38H

BPAGE DRAWING

udimm.sch_1.218
Fri Sep 27 16:42:36 2019

MODULE REV DETAILS

MODULE NAME	REV	DATE



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BPAGE DRAWING

udimm.sch_1.219
Fri Sep 20 11:46:46 2019

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