Rework on Tiger Lake UP3 RVP for TSN AIC Phase 2

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Internet of Things Group

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Revision History

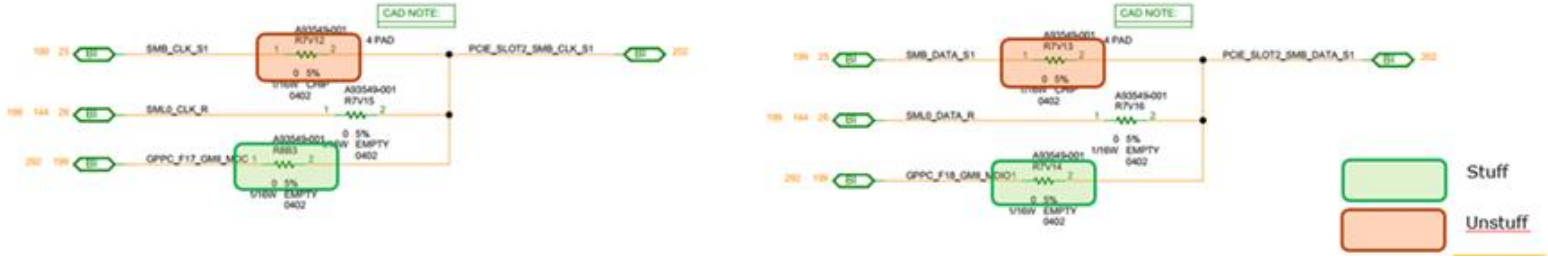
Date	Revision	Description
March 2020	1.05	Updated the platform name.
December 2019	1.0	Initial release.

Rework on Tiger Lake UP3 RVP for TSN AIC Phase 2

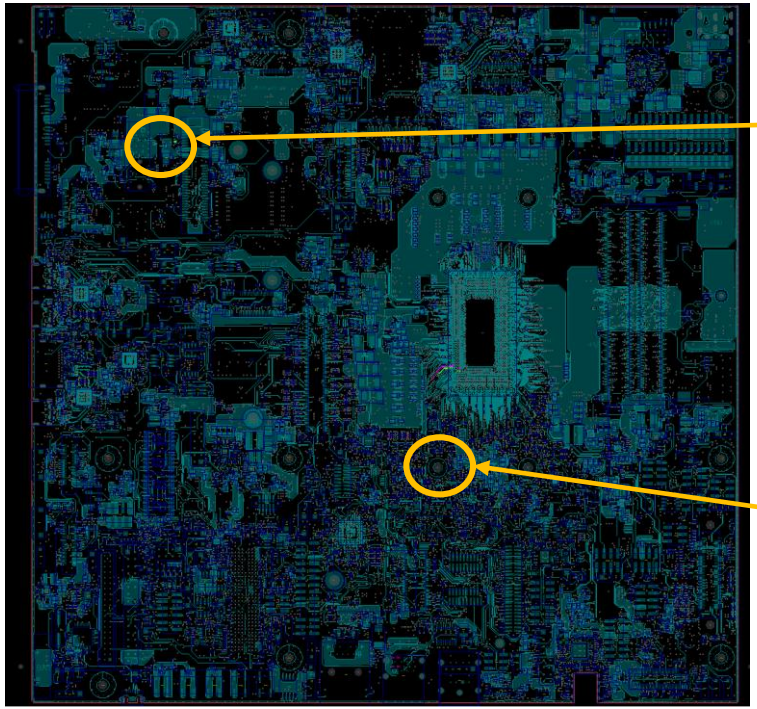
Rework title	**Rework on Tiger Lake UP3 RVP to enable MDC & MDIO signal**
Rework #	**WA-01: Workaround Rework**
Change log #	WW51p2Y19 - Initial release
Description	Workaround to enable MDC and MDIO for Tiger Lake UP3 design for compatibility with TSN AIC Ph2
Rework Implementation Impact	SMBus on PCIe connector will be replaced by MDC and MDIO signals
Reworks involved	Resistors
Applicable to (affected skus)	J91106-101 TGL U DDR4 SODIMM ERB
Contact for details	Intel representative

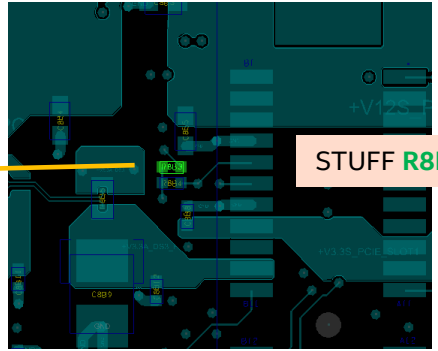
Materials Required to Carry Out the Rework

Action	Item	REFDES	Existing IPN	Description of existing part	New IPN	Description of new part	Implementation Impact
UNSTUFF	Res	R7V12, R7V13, R5G19, R4F72	A93549-001	RES D,0402,0 OHM,1.00%,1/16W			SMBUS CLK / DATA removed
STUFF	Res	R8B3, R7V14, R4G33, R4F71			A93549-001	RES D,0402,0 OHM,1.00%,1/16W	MDC / MDIO connected

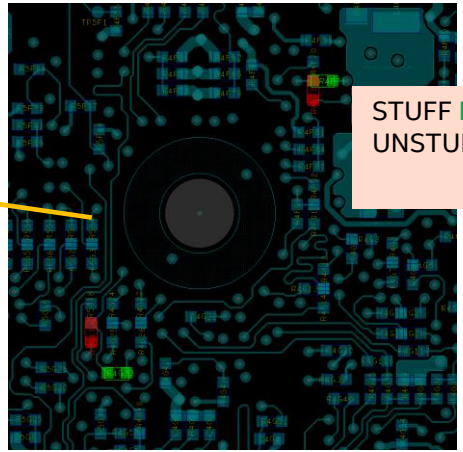


Layout Snapshot – Top Side



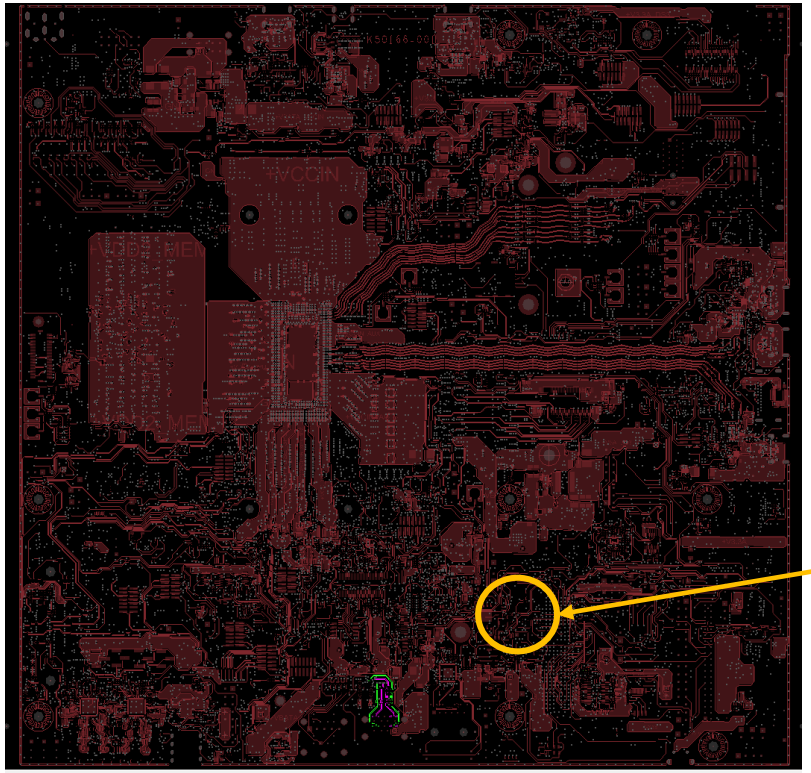


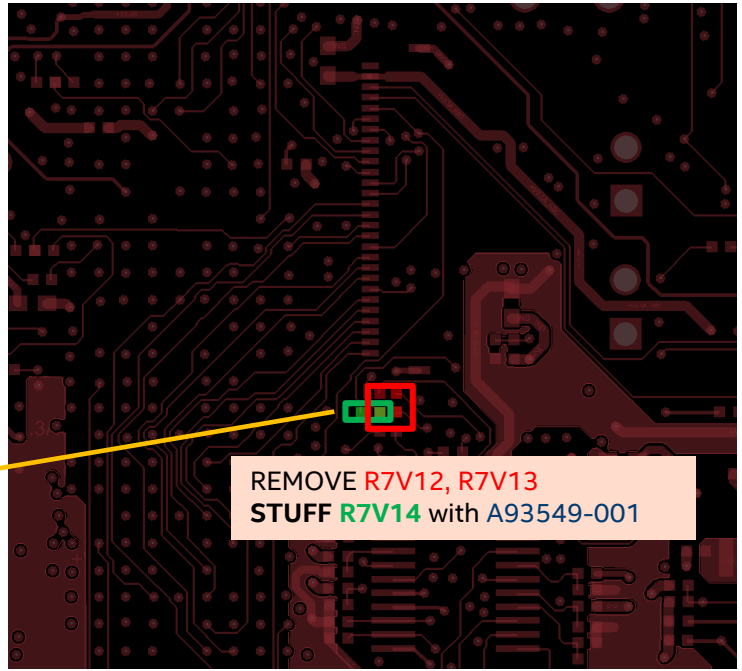
STUFF **R8B3** with A93549-001

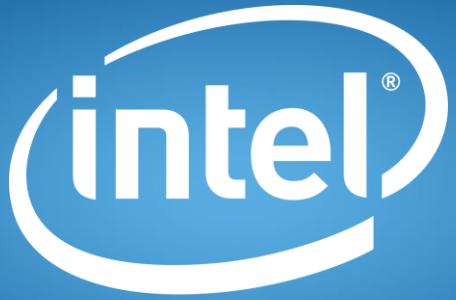


STUFF **R4G33 , R4F71** with A93549-001
UNSTUFF R5G19 , R4F72

Layout Snapshot – Bottom Side (Flipped)



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