Intel® Automated Power Switch (Intel® APS) Version 3

OEM - Specific Customization Guide

December 2019

Revision 2.3

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Revision History

Document Number	Revision Number	Description	Revision Date
443926	1.0	• Initial release.	February 2010
	1.2	• Updated Figure 17 - Pin Diagram (view from above) • S0 cable renamed as SUS cable	May 2010
	1.3	• Marked PC Power connector as "Do Not Use" and deleted instructions on using this connector • Added Safety and Regulatory Information • Added note: Do not modify the SUT power supply • Added: For 1.5MB SKUs which do not implement the SLP_A, the SLP_A connection from the Intel® APS should be connected to the same point as the SLP_S3 connection	February 2011
	1.4	• Added connection instructions for CRV EL2, Maho Bay CRB. • Added requirement of Intel® APS connector according to PDG • Added Intel® APS rework instructions for mobile platforms	May 2011
	1.5	• Added instructions for DS3 platform state detection	December 2011
	1.6	• Added connection instructions for Shark Bay Mobile and Desktop CRB.	June 2012
	1.7	• Added Shark Bay Intel® APS connector instructions.	March 2013
	1.8	• Added Grantley Aztec City Intel® APS connector instructions.	July 2013
	1.9	• Added chapter on connecting Intel® APS to SKL RVP	March 2015
575307	2.0	• Added instructions on connecting Intel® APS to the following platforms: ○ Basin Falls, Apollo Lake, Gemini Lake, Cannon Lake, Coffee Lake and Kaby Lake.	October 2017
	2.1	• Updated the Appendix with Intel® APS connector requirements according to the PDG's of the following platforms: ○ Skylake U/Y, Kaby Lake H/S, Cannon Lake U/Y, Coffe Lake U/H/S, and Gemini Lake	November 2017
	2.2	• Added instructions on connecting Intel® APS to Ice Lake Platform • Added Intel® APS connector requirements according to the PDG of Ice Lake U.	July 2018
	2.3	• Added instructions on connecting Intel® APS to Comet Lake and Tiger Lake Platforms (See CHAPTER 10 and 11) • Added Intel® APS connector requirements according to the PDG of Comet Lake and Tiger Lake (See Appendix T.10 and T.11) • Added instruction on how to simulate HW RF Kill using Intel® APS in APPENDIX E.	December 2019

§ §

1 Introduction

1.1 What is the Intel® APS?

The Intel® Automated Power Switch (Intel® APS) enables innovative and wide power state transition testing on platforms. The Intel® APS programmatic interface provides a simple and easy way to use it. The Intel® APS is compatible with mobile, desktop and workstations systems, and can be accessed by all validation platforms.

The Intel® APS is designed to switch between different types of power sources. The Intel APS effectively reduces the manual testing overhead and enables the exploration of multi-step power and system state flows.

The Intel® APS can provide the status of the following power state signals on the board of the system under test: ME (SLP_M), S0, S3, S4, S5, DSx, and 4 additional signals. The Intel APS reads the signal information via a flat cable that connects to the board of the system under test.

This document describes how to connect and set up the Intel® APS.

Note: Validation testing without connecting the Intel APS signal sampling cables is not supported and can result in unexpected behavior.

Note: You must be a platform hardware design engineer in order to connect the Intel® APS.

1.2 New in Intel® APS Rev. 3.0

The following features are new in this release of the Intel® APS:

- **Integral flash burning** (on CRB only): The device includes a SPI flash memory burner allowing programming via the Intel® APS Software. External flash burner no longer required.
- **BIOS POST code reader** (on CRB only): The Intel® APS retrieves the current Post code value and makes it available for display by the Intel® APS Software.
- **USB switching**: The device includes a USB switch allowing to connect 2 allowing to connect 2 computers to a USB device (using Intel® APS software to switch between the computers)
- **USB connection from management console**: parallel port is no longer required (or supported) on system under test
- **Additional external outputs** for opening and closing circuits (on External 1 cable): A total of 11 possible connections.

- **Intel® APS firmware is updatable** from the management console: Allows the user to update the Intel® APS firmware from the management console when new releases are made available.
- **LED indicators**: These display information on the current state of the system under test: ME, S0-S5, DSx, and 4 additional indicators for optional use.
- **Integrated Intel® SBD functionality**: No longer a need for the separate Intel APS SDB board.

§ §

2 Kit Contents

The Intel® APS Rev 3 kit contains the following components:

1 Intel® APS Rev 3 unit	N/A	FIGURE 1 FIGURE 2
1 USB data cable	(USB A<->B)	FIGURE 44
3 control cables	Main cable, EX1 cable, Feature cable	Main: FIGURE 29 EX1: FIGURE 37 Feature cable: FIGURE 31
1 battery cable	Do not use earlier versions of this cable with Intel APS Rev 3	FIGURE 41
1 mobile platform power cable	fits Intel mobile CRB power connectors – from extension cable to platform power in	FIGURE 39
Extension cable for the mobile platform power cable	Connects Intel® APS MB out to mobile platform power cable	FIGURE 40
1 mobile platform adapter board for Intel platforms	fits Intel mobile CRB power connectors – connects the mobile power brick to the Intel APS	FIGURE 45
1 Desktop unit (100v-220v) for desktop platform power control	N/A	FIGURE 5
12v power supply	compatible with 100v-220v input	N/A

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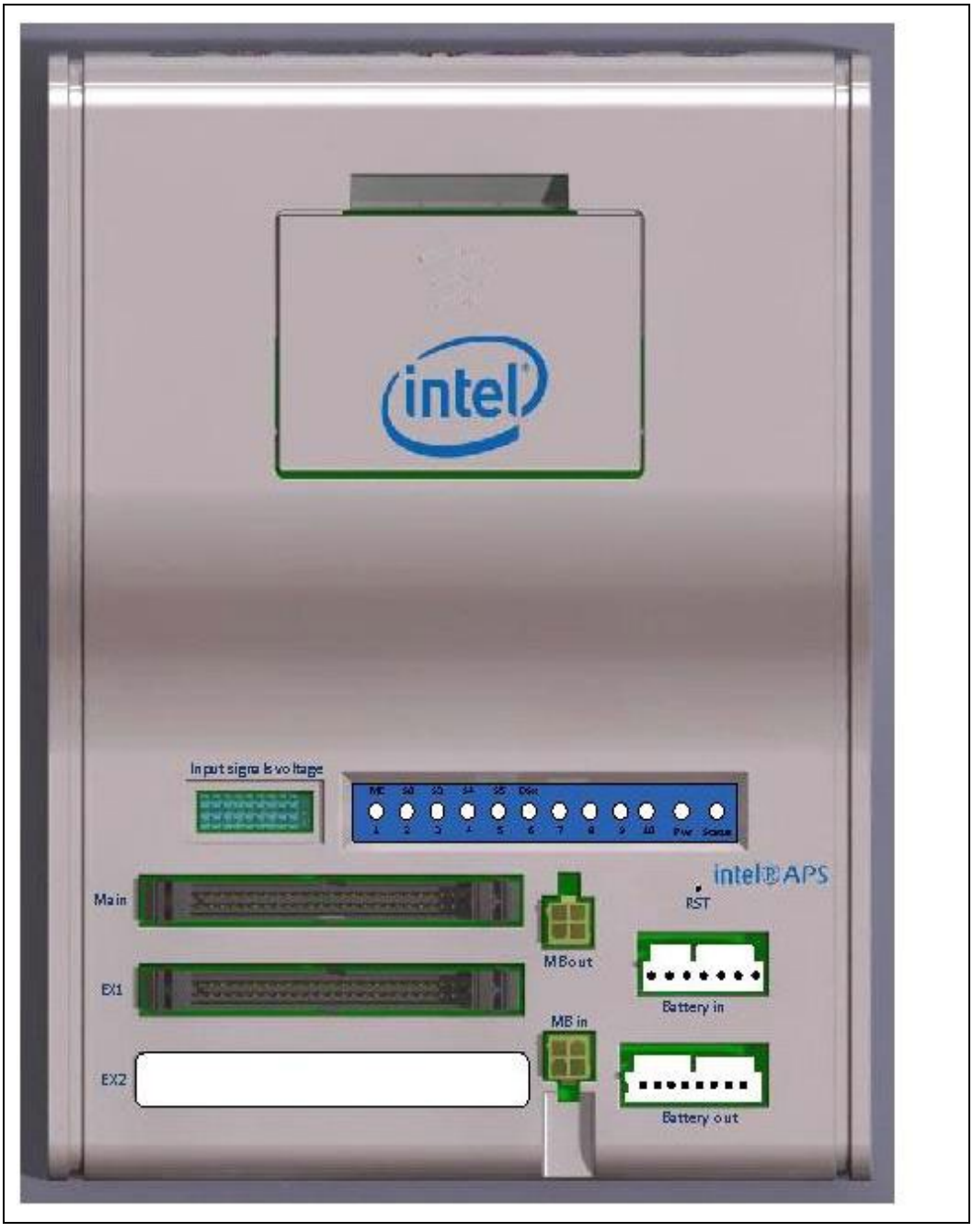
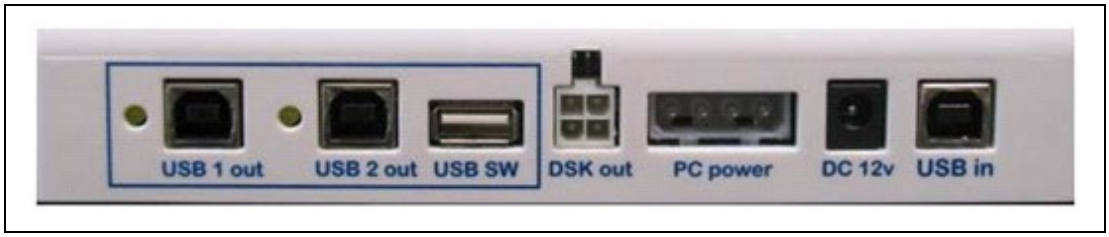
3 Intel® APS Connections

Figure 1. Intel® APS Front Panel



Legend:
Front panel Input signal voltage – Enables detection of 1.1V or 3V signals Main – Main connections flat cable connector EX1 – Extended connections flat cable connector EX2 – Reserved for future use MB in - Mobile: DC input from power brick - Molex_A-42404-04xx MB out - Mobile: DC power output to motherboard - Molex_A-42404-04xx Battery in - from battery, Molex_26-60-4080 Battery out - to platform battery connector, Molex_09-50-3071 Reset button for Intel® APS Rev 3 LED panel – Signals and Intel APS status LEDs J1 (Under the flip panel) – Extended capabilities flat cable connector J2 (Under the flip panel) – connector for connecting the feature cable J4 (Under the flip panel) – Extended capabilities flat cable connector

Figure 2. Intel® APS Rear Panel



Legend:
Back panel USB IN – Connects the Intel® APS to the management computer DC 12V - Supplies Power IN DC to Intel APS from PSU PC Power - Do Not Use DSK out – Connects to the Intel APS DSK unit to control AC power control on/off USB SW – USB SW controlled device USB1/2 out – connects the Intel APS USB SW to 2 computers

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4 Quick Connection Instructions for Mobile Platforms

This section provides a quick guide for connecting the Intel APS to a mobile platform. For help with locating components on the Intel® APS, see ERROR! REFERENCE SOURCE NOT FOUND. and **FIGURE 2. INTEL® APS REAR PANEL** as required. For more details on connection and setup, see the subsequent sections of this guide.

1. Plug one end of the USB data cable into the **USB in** socket on the rear panel of the Intel® APS. Plug the other end of the cable into a USB port on the management console computer.

2. Connect one end of the 12V APS power supply to the **DC 12v** socket on the rear panel. Plug the other end into an AC power source.

3. **If you are not connecting to an Intel CRB platform:**

   a. Cut the SUT's power supply cable and solder each cut end to an Intel® APS power jack connector. For details, see **CONNECTING THE POWER SUPPLY TO THE INTEL® APS**.
   NOTE: Do not modify the SUT power supply—modification of the SUT power supply will invalidate the safety approvals for the device. Figure 35, illustrates how you can construct an interface cable similar to the Intel mobile platform power cable using the SUT mating connectors.

   b. Take the jack connected to the power supply side and plug it into the **MB in** port on the front panel.

   c. Plug the jack connected to the SUT side into the **MB out** port on the front panel.

   d. Insert the other end of the cable into the SUT's power socket.

4. **If you are connecting to an Intel CRB platform:**

   a. Connect the mobile platform adapter board (see Figure 45) to the MB in socket on the Intel® APS front panel.

   b. Connect the mobile CRB's power brick to the mobile platform adapter board.

   c. Connect the extension cable (see Figure 40) to the MB out socket on the Intel APS front panel.

   d. Connect the other end of the extension cable to the mobile platform power cable.

   e. Connect the mobile platform power cable to the CRB's power in jack.

5. To connect the SUT's battery to the Intel® APS, you need to solder the battery to an SUT battery jack. Then plug the jack into the Battery in port. Plug a battery cable (provided with the Intel(R) APS kit) into the Battery out port and

solder the other end of the cable to the SUT battery socket. (See **CONNECTING THE MOBILE BATTERY TO THE INTEL® APS**.)

6. Connect the main Intel® APS cable to the Intel APS Main socket. Connect the individual wires to the correct headers on the SUT's board: Power, Reset, and Clear CMOS headers. (See **CONNECTING THE INTEL® APS TO SUT POWER BUTTON** on, **CONNECTING THE INTEL® APS TO THE RESET BUTTON**, and **CONNECTING THE INTEL® APS TO CLEAR CMOS ON THE PLATFORM**.)

7. To allow clearing CMOS via the Intel® APS, do the rework described in **CONNECTING THE INTEL® APS TO CLEAR CMOS ON THE PLATFORM**.

8. Connect the SUS, S3, S4, S5, GND, and ME cables to the relevant locations on the SUT's board. For details on locating the signals on the board, see **CONNECTING THE SIGNAL SAMPLING CABLES TO THE SYSTEM UNDER TEST**.

9. Use the Intel® APS Software to verify that the Intel® APS is connected properly. For details, refer to the Intel® APS Software Installation and User's Guide.

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5 Quick Connection Instructions for Desktop/Workstation Platforms

This section provides a quick guide for connecting the Intel APS to desktop and workstation platforms. For help with locating components on the Intel® APS, see **FIGURE 1** and **FIGURE 2. INTEL® APS REAR PANEL** as required. For more details on connection and setup, see the subsequent sections of this guide.

1. Plug one end of the USB data cable into the **USB in** socket on the rear panel of the Intel® APS. Plug the other end of the cable into a USB port on the management console computer.

2. Connect one end of the 12V APS power supply to the **DC 12v** socket on the back panel. Plug the other end into an AC power source.

3. Use the Desktop unit provided in the Intel® APS kit. (See **CONNECTING THE DESKTOP UNIT (DSK).**) Plug the 4-pin control cable into the **DSK out** port on the back panel. Connect the power cable into an AC socket. Plug the remaining cable of the desktop APS unit into the SUT's power supply. If the SUT has more than one power supply, plug the second power supply directly into a power source. If the system can run with only one power supply active, unplug the second power supply before tests that require transition to G3. If not, manually unplug/plug the second power supply during tests that require transition to/from G3.

4. Connect the main cable to the Intel® APS **Main** socket. Connect the individual wires to the correct headers on the SUT's board: Power, Reset, and Clear CMOS headers. (See **CONNECTING THE INTEL® APS TO SUT POWER BUTTON**, **CONNECTING THE INTEL® APS TO THE RESET BUTTON**, and **CONNECTING THE INTEL® APS TO CLEAR CMOS ON THE PLATFORM**.)

5. To allow clearing CMOS via the Intel® APS, do the rework described in **CONNECTING THE INTEL® APS TO CLEAR CMOS ON THE PLATFORM**.

6. Connect the SUS, S3, S4, S5, GND, and ME cables to the relevant locations on the SUT's board. For details on locating the signals on the board, see **CONNECTING THE SIGNAL SAMPLING CABLES TO THE SYSTEM UNDER TEST**.

7. Use the Intel® APS Software to verify that the Intel® APS is connected properly. For details, refer to the Intel APS Software Installation and User's Guide.

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6 USB Driver Installation

For instructions on installing the USB device drivers, refer to the Intel® APS Software Installation and User's Guide.

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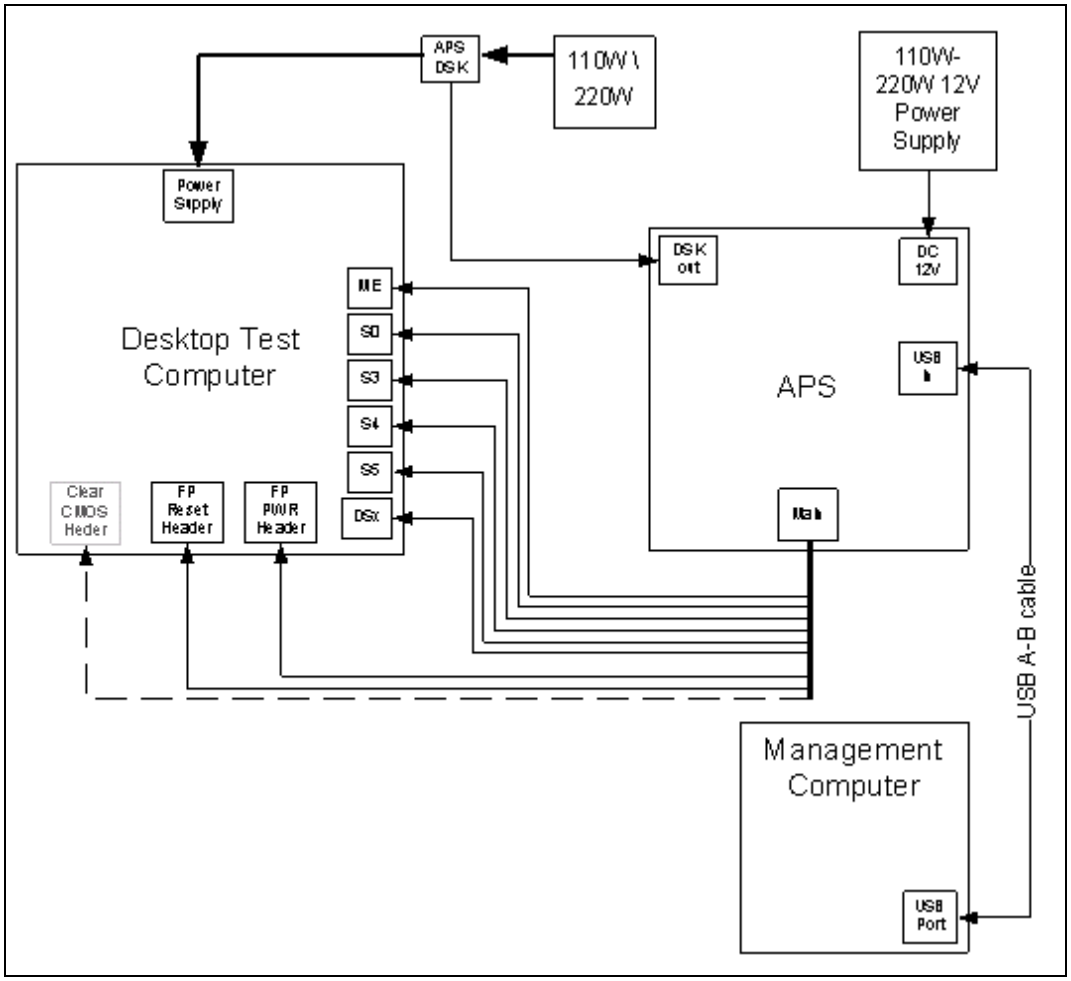
7 Connecting the Intel® APS to a Desktop/Workstation Platform

This section contains detailed instructions for connecting the Intel® APS to desktop and workstation platforms. Following are a high-level connection diagram and a picture of the connections on desktop and workstation platforms.

Figure 3. High-Level Desktop/Workstation Connection Diagram



7.1 Connecting the Desktop Unit (DSK)

This section describes how to connect the desktop unit to the Intel® APS and to the platform under test.

Figure 4. Desktop Unit Connection Diagram

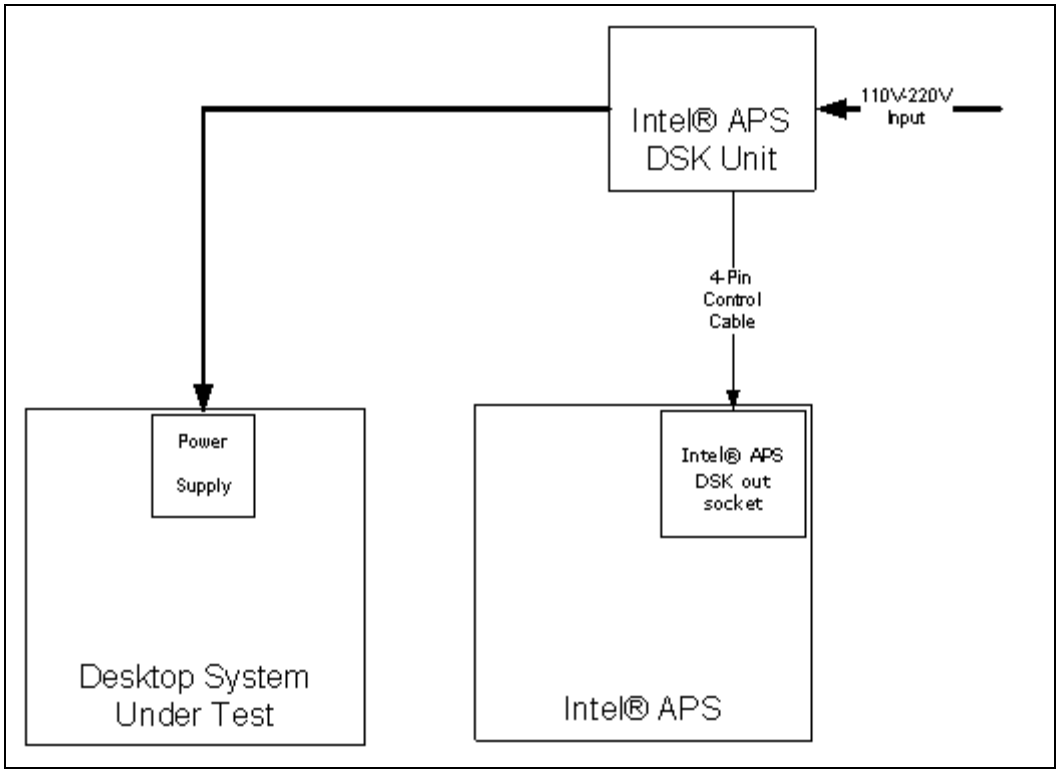


Figure 5. DSK (Desktop Intel® APS Unit)

To connect the Desktop Unit:

1. Connect the power cable coming out of the DSK to the platform's power supply.

2. Connect the DSK's 4-pin control cable to the DSK out connector on the rear panel of the Intel® APS.

Figure 6. Connecting the DSK's 4-pin control cable to the DSK out connector

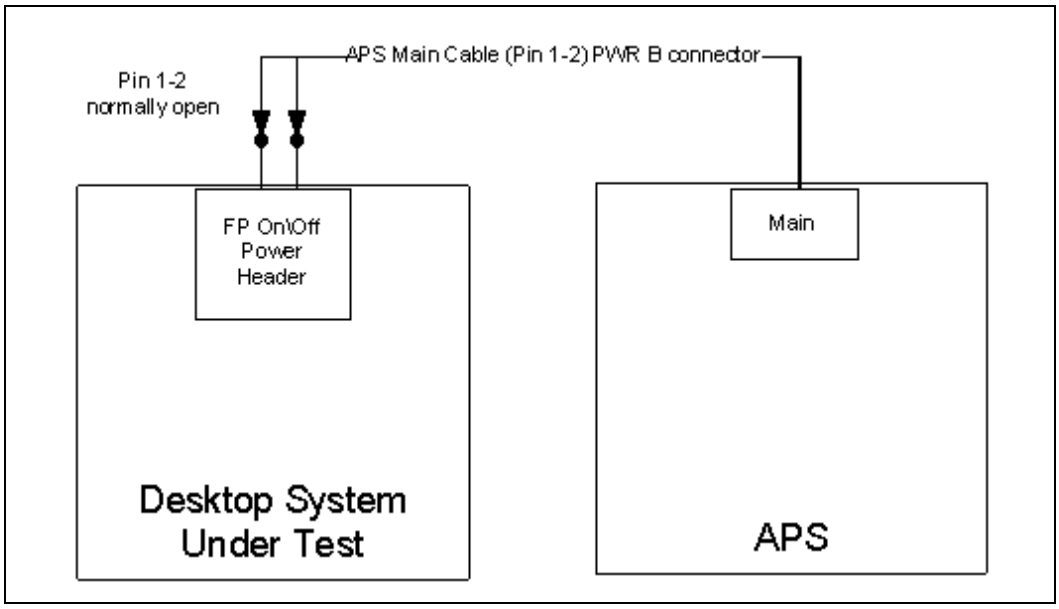
3. Connect the other end of the DSK's power cable to a 100v/220v electrical socket.

7.1.1 Possible Electrical Connectivity

- Connects -100220V power to the system under test.
- Disconnects -100220V power from the system under test.

7.2 Connecting the Intel® APS to the SUT's Power Button

Figure 7. Connecting to the SUT Power Button Diagram



To connect the Intel® APS to the SUT's power button:

Connect the PWR B connector (Main Pin 1-2) to the SUT's power button header on the motherboard (FP On/Off Power Header in the diagram).

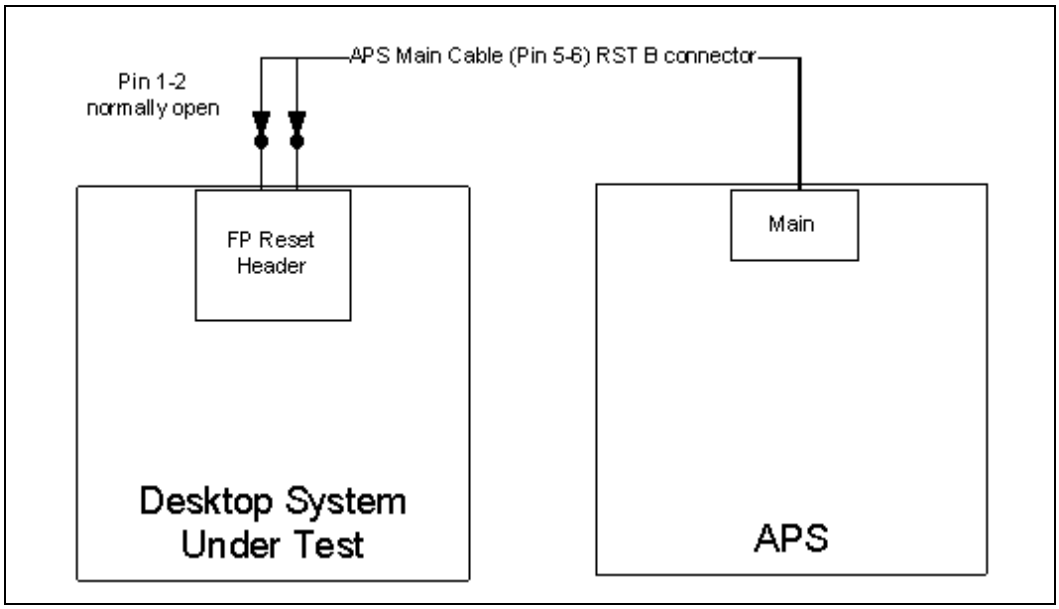
For details of how to connect to the power button on a CRB, see Connecting to Power Button on Piketon (Ibex Peak Desktop) CRB on Page 88, Connecting to SUT Power Button on a Sugar Bay (Cougar Point Desktop) CRB on Page 96, Connecting to SUT Power Button on a Maho Bay (Panther Point Desktop) CRB Page 98, and Connecting Signal Sampling Cables to Aztec City Workstation CRB on Page 119.

7.2.1 Possible Electrical Connectivity

- Connects Pin 1 to Pin 2
- Disconnects Pin 1 from Pin 2

7.3 Connecting the Intel® APS to the Reset Button

Figure 8. Connecting Intel® APS to Reset Button Diagram



To connect the Intel® APS to the reset button:

Connect the RST B cable (Main 5-6) to the SUT's Reset header on the motherboard.

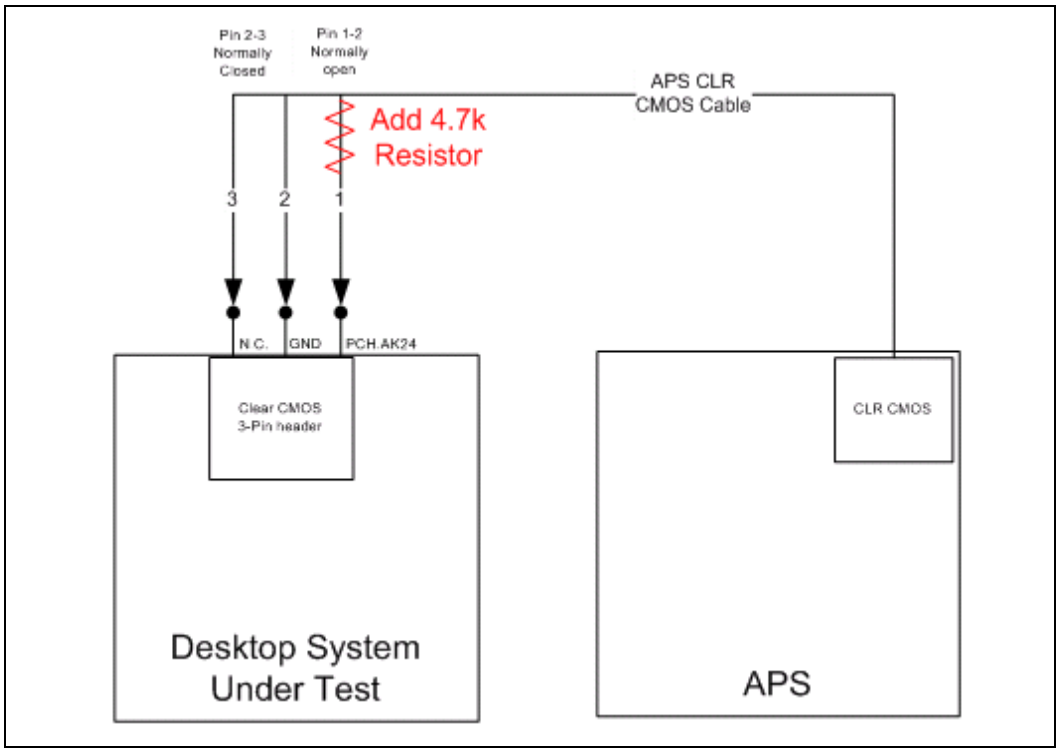
For details of how to connect to the reset button on a CRB, see Connecting to Reset Button on Piketon (Ibex Peak Desktop) CRB on Page 88, Connecting to SUT Reset Button on a Sugar Bay (Cougar Point Desktop) CRB on Page 99, Connecting to SUT Reset Button on a Maho Bay (Panther Point Desktop) CRB Page 111, and Connecting Signal Sampling Cables to Aztec City Workstation CRB on Page 119.

7.3.1 Possible Electrical Connectivity

- Connects Pin 1 to Pin 2
- Disconnects Pin 1 from Pin 2

7.4 Connecting the Intel® APS to Clear CMOS on the Platform

Figure 9. Connecting the Intel® APS to Clear CMOS Diagram



If there is a Clear CMOS header on the SUT board:
Connect the CLR CMOS cable (Main 9-11) to the header on the SUT.

If there is no Clear CMOS header on the SUT board :

1. Solder a 3-pin header (Samtec_TSW-103-07-T-S) to the following pins on the motherboard:

Pin1: PCH.AK24 (PCH_RTCRST_PULLUP) through a 4.7K resistor

Pin2: GND

Pin3: N.C.

2. Connect the CLR CMOS cable (Main 9-11) to the header on the SUT.

For details of how to connect to Clear CMOS on a CRB, see **Connecting to Clear CMOS on an Piketon (Ibex Peak Desktop) CRB** on Page 91 or **Intel® APS to Clear CMOS on a Sugar Bay (Cougar Point Desktop) CRB** on Page 101, or **Intel® APS to Clear CMOS on a Maho Bay (Panther Point Desktop) CRB** on Page 113, and Connecting Signal Sampling Cables to Aztec City Workstation CRB on Page 119.

7.4.1 Possible Electrical Connectivity

- Intel® APS connects Pin 1 to Pin 2
- Intel® APS disconnects Pin 1 from Pin 2

7.5 Powering the Intel® APS

Insert the 12v power supply into the Intel® APS **DC 12v** jack (see FIGURE 2. INTEL® APS REAR PANEL).

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8 Connecting the Intel® APS to a Mobile Platform

This section contains detailed instructions for connecting the Intel® APS to a mobile platform. Following are a high-level connection diagram and a picture of the connections on a mobile platform.

Figure 10. Mobile Connection Diagram

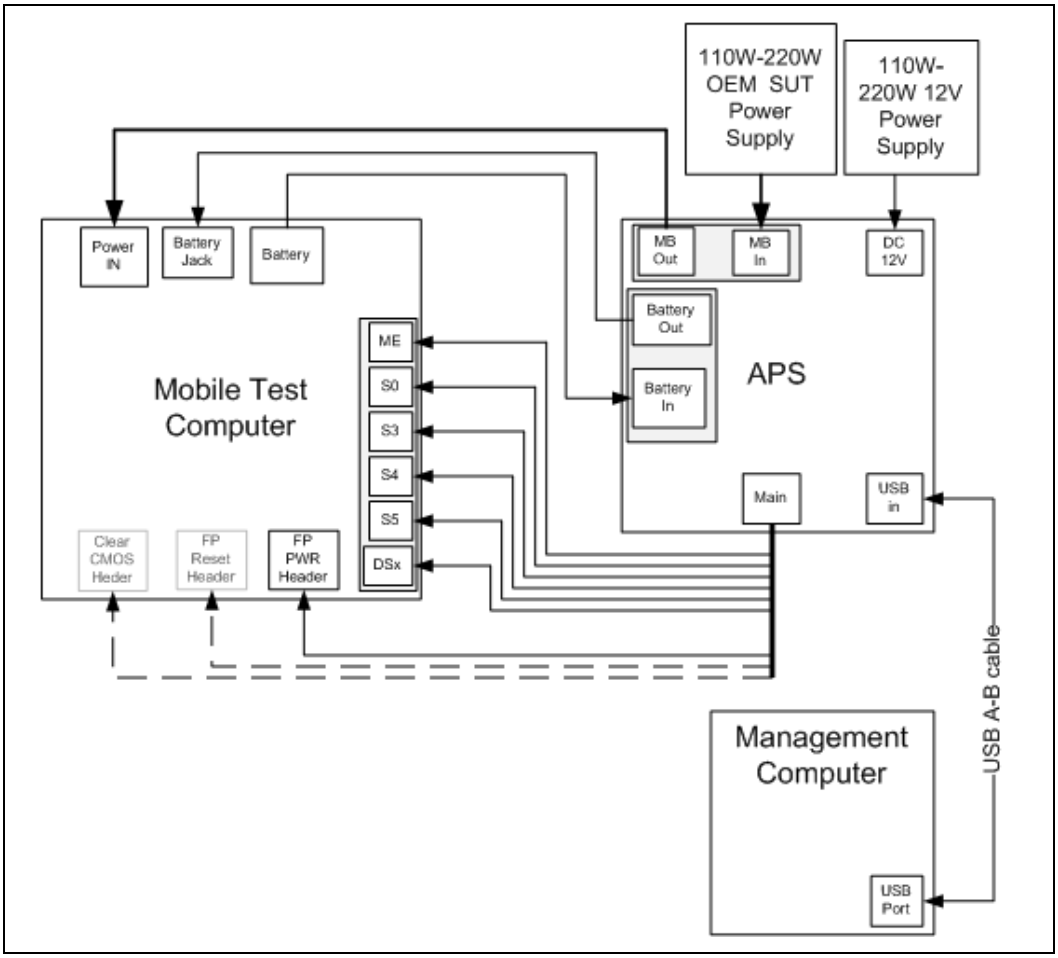


Figure 11. Intel® APS Connected to Huron River (Cougar Point mobile) CRB with Front Panel Power, Front Panel Reset, and CLR CMOS Connections

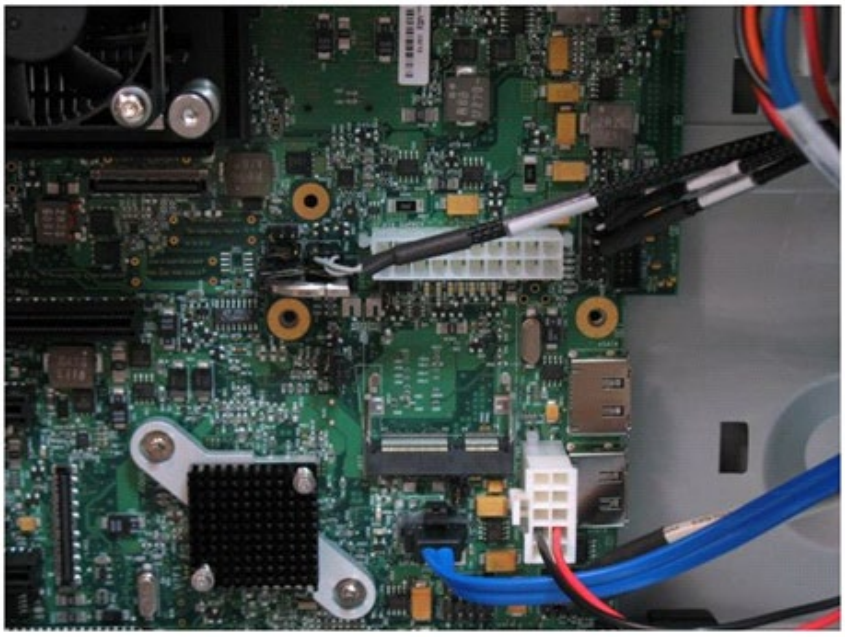
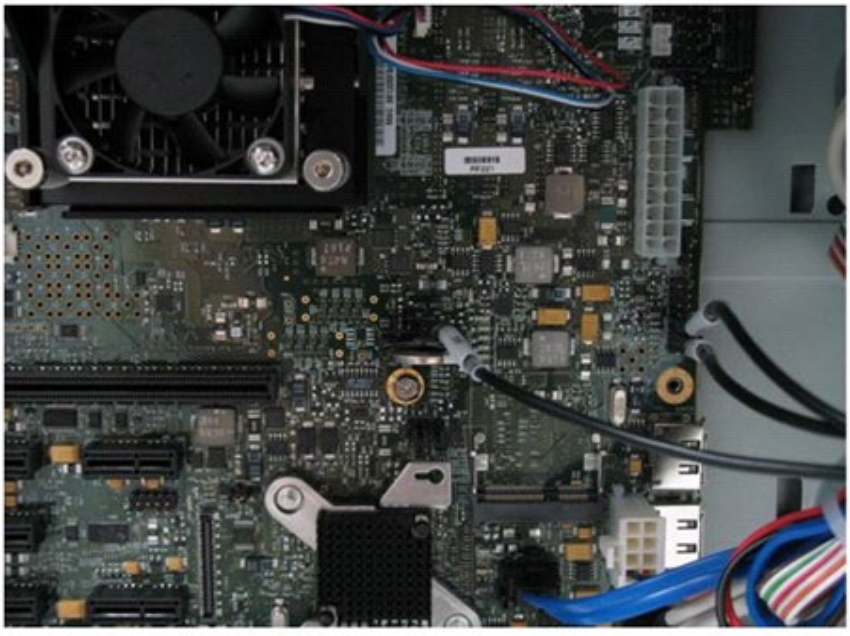


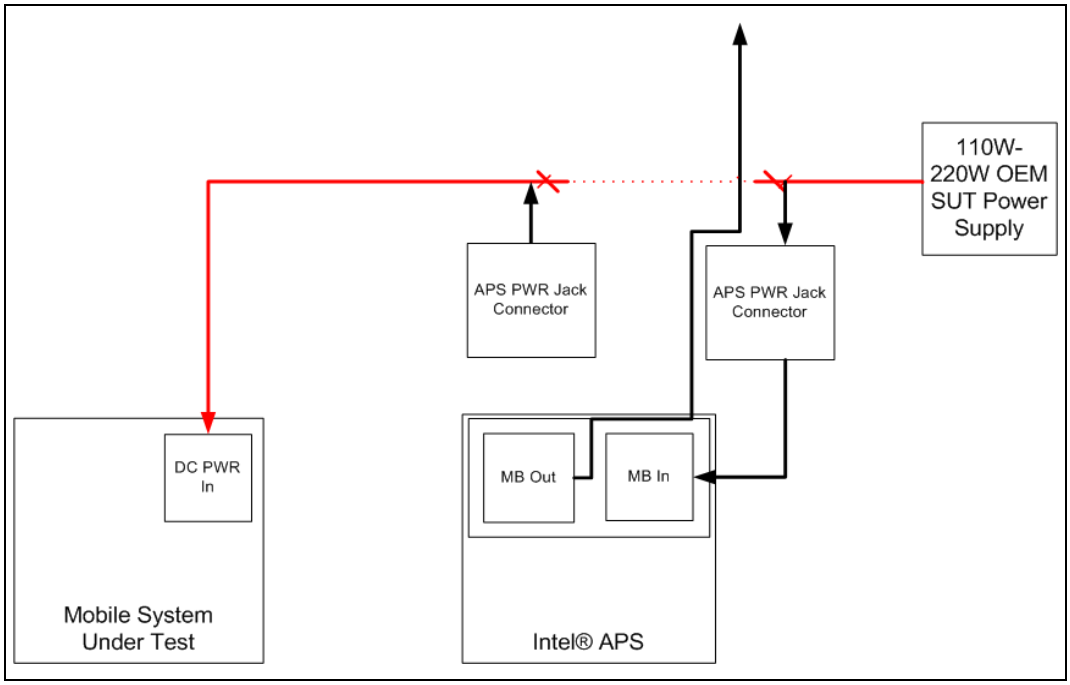
Figure 12. Intel® APS Connected to Calpella CRB (Ibex Peak mobile) with Front Panel Power, Front Panel Reset, and CLR CMOS Connections



8.1 Connecting the Power Supply to the Intel® APS

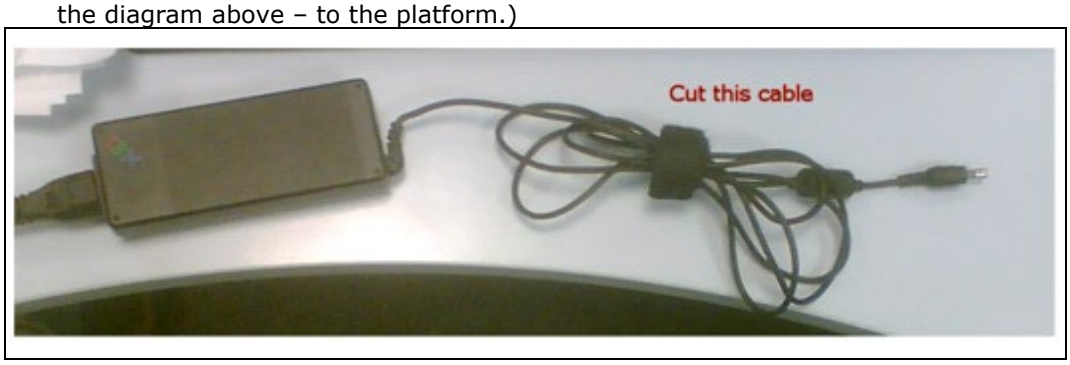
Note: The mobile system's power supply must not output more than 30V / 2A.

Figure 13. Connecting the Power Supply to the Intel® APS Diagram



To connect the power brick to a mobile board (not an Intel CRB) through the Intel® APS:

1. Cut the Power Brick DC cable into two pieces. (This is the cable that connects the mobile platform's power brick – marked **110V-220V OEM SUT Power Supply** in the diagram above – to the platform.)



2. Connect the ends of the cut Power Brick DC cable to 4-pin connectors. Following is an example of the modified cable section that connects to the platform's DC

power socket. (This cable – the **mobile platform power cable** - is supplied with the Intel® APS for use with Intel mobile CRB machines only).

Figure 14. Section of Cut Power Brick Cable (with 4-pin Connector) that Connects to the Platform's DC Power Socket

3. Plug the 4-pin connector on the cable that is still connected to the power brick into the Intel APS **MB in** jack.

4. Plug the 4-pin connector on the other cable (the cable that connects to the platform's power socket) into the Intel APS **MB out** jack. Insert the other end of the cable into the platform's DC power socket.

5. Insert the 12v power supply into the Intel® APS **DC 12V** jack (see Figure 2. Intel® APS Rear Panel).

To connect the power brick to an Intel mobile CRB through the Intel APS:

1. Connect the mobile platform adapter board to the MB in socket on the Intel APS front panel.

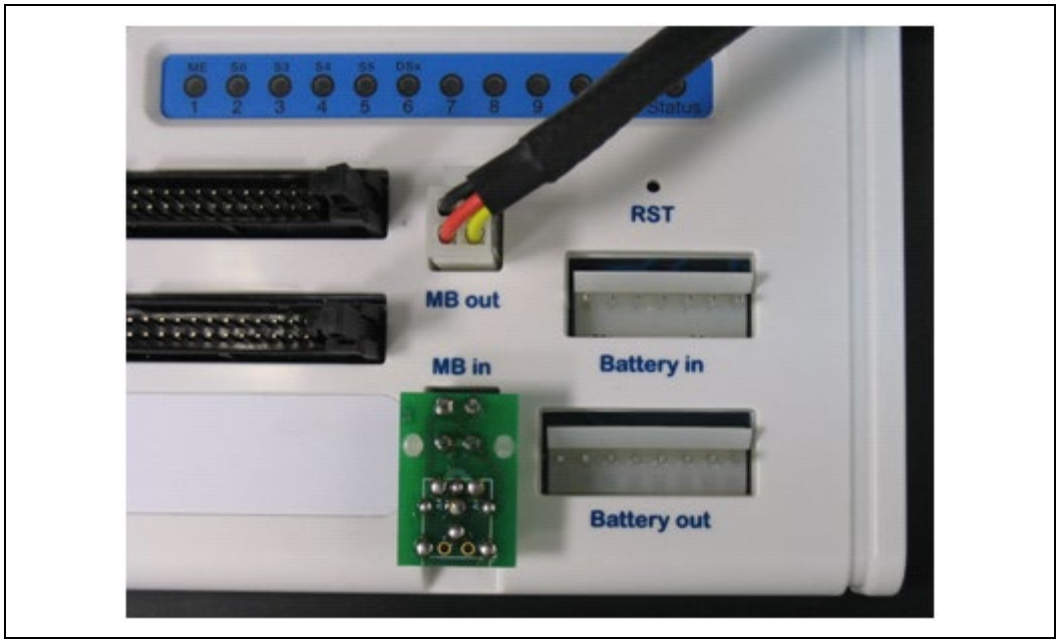
2. Connect the mobile CRB's power brick to the mobile platform adapter board.

3. Connect the extension cable to the MB out socket on the Intel APS front panel.

4. Connect the other end of the extension cable to the mobile platform power cable.

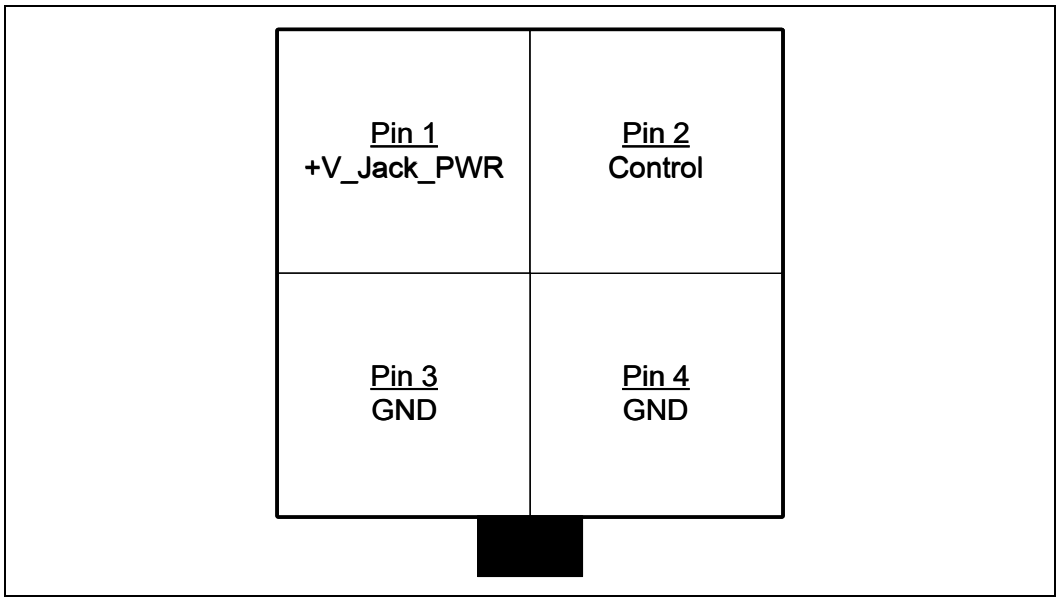
5. Connect the mobile platform power cable to the CRB's power in jack.

Figure 15. Mobile Platform Adapter Board Attached to MB In and Extension Cable Connected to MB Out (for connecting to mobile CRB)



8.2 Pin Definition

Figure 16. Pin Diagram (view from above)



Note: You only need to connect to one (not both) of the GND pins.

Table 1. Pins

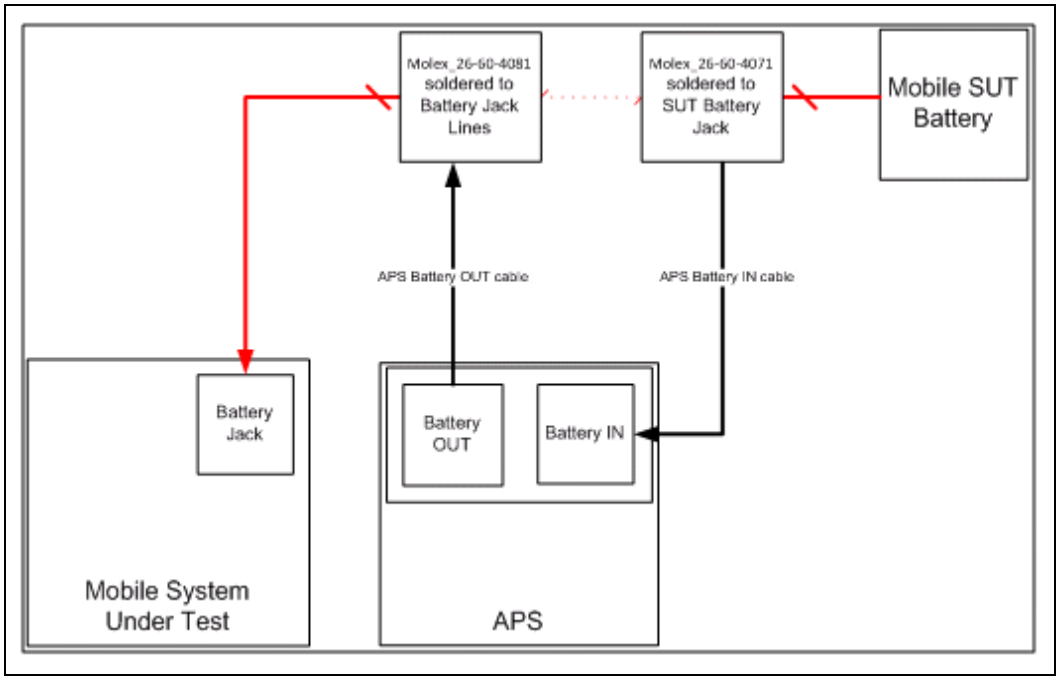
Warning: **Pin**	***Warning:*** **Name**
1	+V_JACK_PWR
2	Control
3	GND
4	GND

8.2.1 Electrical Characteristics

The Intel® APS connects/disconnects Pin 1 of the **MB in** connector to/from Pin 1 of the **MB out** connector.

8.3 Connecting the Mobile Battery to the Intel® APS

Figure 17. Connecting Mobile Battery to the Intel® APS Diagram



The Intel® APS supports connecting/disconnecting 7 battery signals that are expected to be routed through the Intel APS (**Battery IN**, **Battery OUT** connectors –

The mobile system's battery must not output more than 30V / 2A.

Note: Do not use earlier versions of the battery cable – use only the cable supplied with the Intel APS Rev 3!

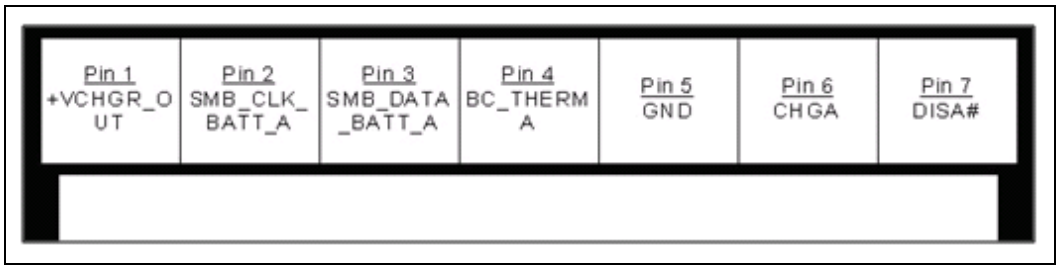
To connect/disconnect battery signals from the Intel APS:

1. Connect the Intel® APS Platform **Battery IN** socket (Battery Cable) to the battery's connector. (This can be done by replacing the existing connector on the Intel APS **Battery IN** cable with a connector that fits your battery.)
2. Connect the Intel® APS **Battery OUT** (Battery Cable) connector to Intel® APS **Battery IN** socket.
3. Connect one end of the Intel® APS **Battery OUT** cable to the battery jack on the motherboard. (This can be done by replacing the existing connector on the Intel® APS **Battery OUT** cable with a connector that fits your battery jack.)
4. Connect the other end of the Intel® APS **Battery OUT** Cable to the Intel® APS **Battery OUT** socket.

8.3.1 Electrical Characteristics

Intel® APS connects/disconnects pins 1 through 7 of Battery IN to/from pins 1 through 7 of Battery OUT

Figure 18. Intel® CRB Pins 1 through 7



As an example of how to connect the battery signals from the platform through the Intel® APS, the following table shows how to connect the battery signals on an Intel CRB:

Table 2. Battery Signals on Intel CRB Routed through the Intel® APS

Warning: **Pin**	***Warning:*** **Name**
1	+VCHGR_OUT
2	SMB_CLK_BATT_B
3	SMB_DATA_BATT_B
4	BC_THERMB
5	GND
6	CHGB
7	DISB#

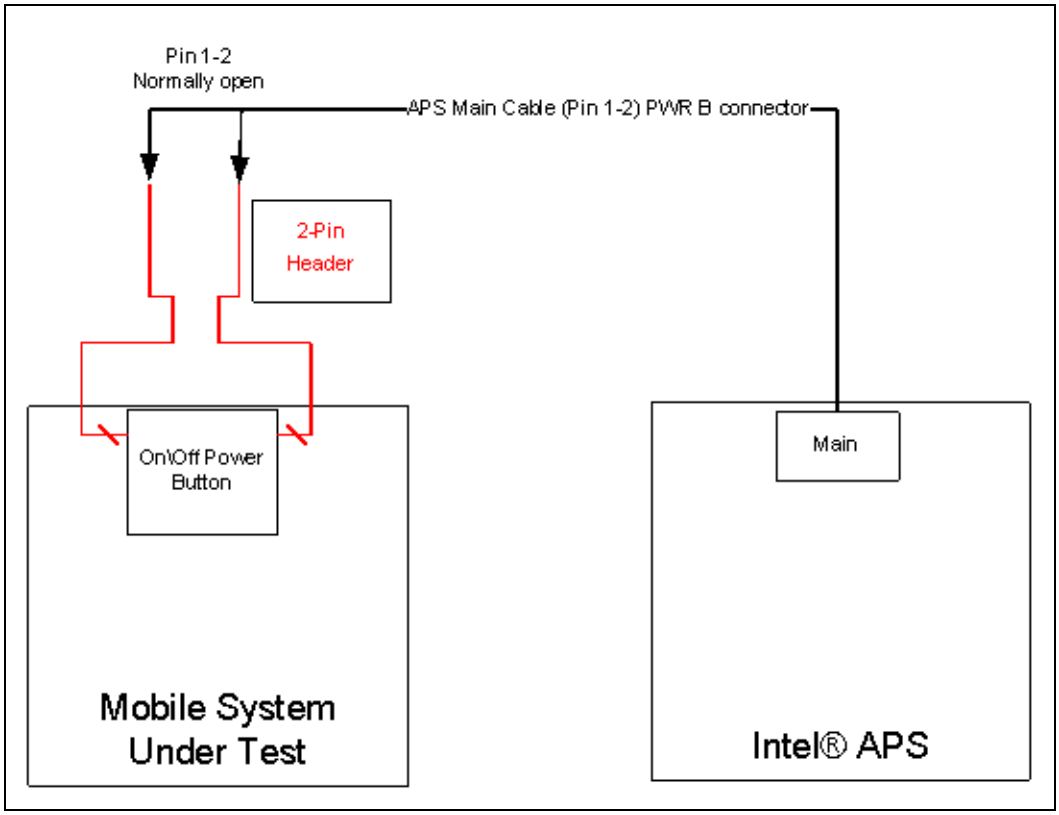
Note: Always connect VCC to Pin1 and GND to pin 5.

8.3.2 Additional Battery Signals

If the OEM has more than 7 signals on its battery connector, the 7 signals that are to be routed through the Intel® APS must be selected. These 7 signals, when disconnected, should cause the platform to detect that the battery is not present.

8.4 Connecting the Intel® APS to SUT Power Button

Figure 19. Connecting Intel® APS to SUT Diagram



To connect the Intel APS to the SUT power button:

Solder a 2-pin header (Samtec_TSW-102-07-T-S) to the two contacts of the power button (polarity unimportant) and connect it to the Intel® APS PWR B cable (Main Pin 1-2), or connect the two lines of the cable to the 2 contacts of the power button.

8.4.1 Possible Electrical Connectivity

- Intel® APS connects Pin 1 to Pin 2.
- Intel® APS disconnects Pin 1 from Pin 2.

For details on connecting the Intel® APS to the power button on a mobile CRB, see **INTEL® APS TO SUT POWER BUTTON ON A HURON RIVER (COUGAR POINT MOBILE)**

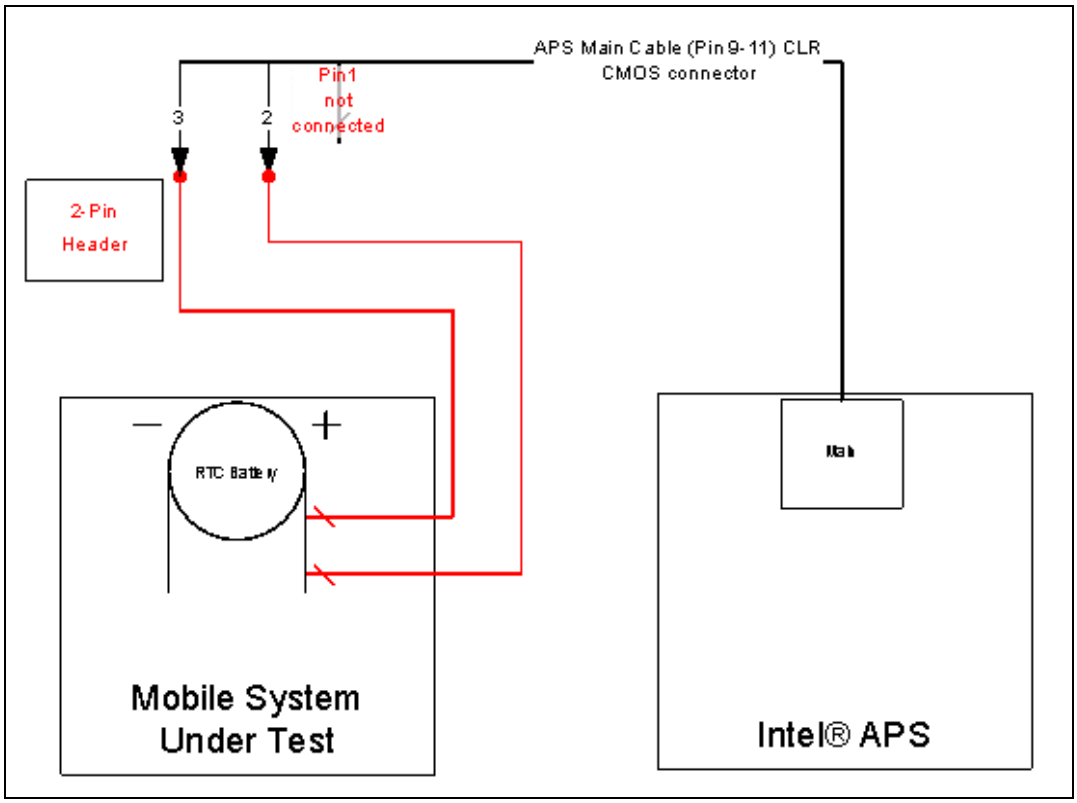
CRB and INTEL® APS TO SUT POWER BUTTON ON A CHIEF RIVER (PANTHER POINT MOBILE) CRB.

8.5 Connecting the Intel® APS to the Reset Button

For instructions on connecting the Intel® APS to a mobile CRB's reset button, see CONNECTING TO CALPELLA (IBEX PEAK MOBILE) CRB'S RESET BUTTON or CONNECTING TO RESET BUTTON ON A HURON RIVER (COUGAR POINT MOBILE) CRB ,and CONNECTING TO RESET BUTTON ON A CHIEF RIVER (PANTHER POINT MOBILE) CRB.

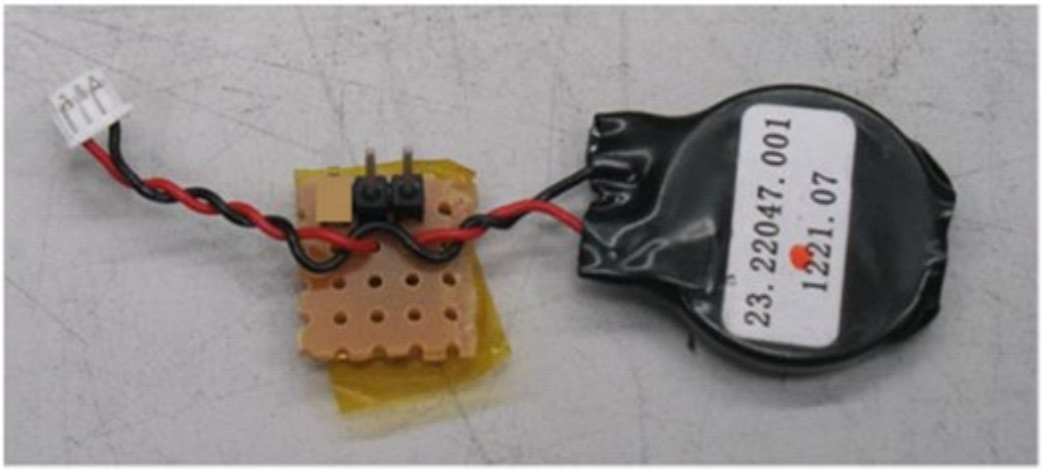
8.6 Connecting the Intel® APS to Clear CMOS on the Platform

Figure 20. Connecting the Intel® APS to Clear CMOS Diagram



To connect the Intel® APS to Clear CMOS on a mobile platform (not a CRB):

1. Cut either one of the RTC battery lines and solder the cut ends of the line to a 2-pin header (Samtec_TSW-102-07-T-S). In the following picture, the red wire has been cut.



2. Connect the Intel® APS CLR CMOS cable (Main Pin 9-11) to the 2-pin connector. Make sure you connect pins 2 and 3 of the cable to the 2-pin connector (polarity does not matter).

8.6.1 Possible Electrical Connectivity

- Intel® APS connects Pin 2 to Pin 3.
- Intel® APS disconnects Pin 2 from Pin 3.

8.7 Powering the Intel® APS

Insert the 12v power supply into Intel APS **DC 12V** jack (see Figure 2. Intel® APS Rear Panel).

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9 Connecting Intel® APS to the Management Computer

1. Connect the USB cable (A) to the management computer's USB port.
2. Connect the other end of the USB cable (B) to the **USB in** connector on the Intel® APS (see Figure 2. Intel® APS Rear Panel).

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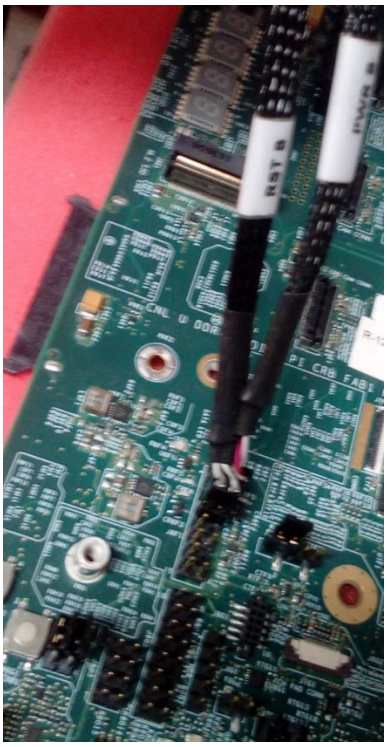
10 Connecting Intel® APS to Comet Lake Platforms

10.1 Connecting the Power and Reset Buttons on Comet Lake-U platforms

Connect the power button and reset button relays to J8F1 on the front panel header.

Figure 21. CML-U Power and Reset Button Relays Connected

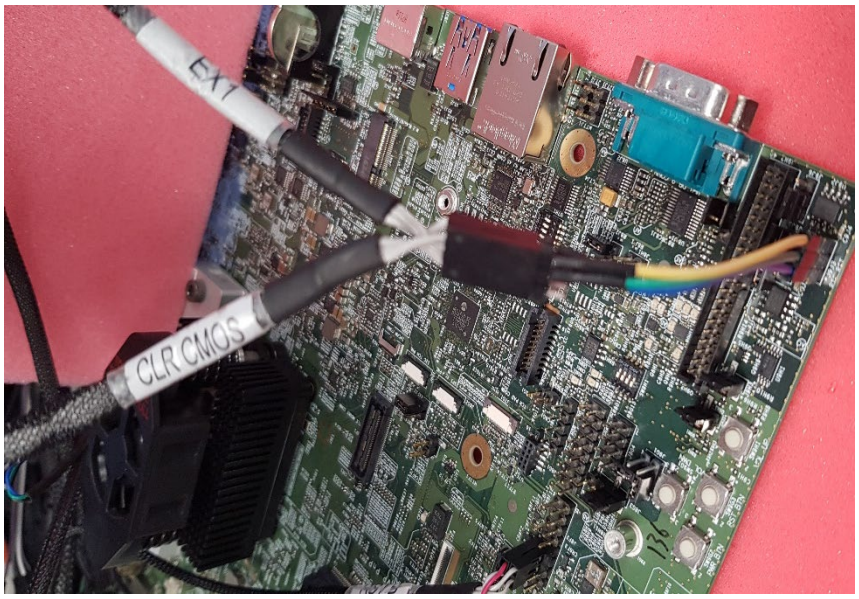


10.2 Connecting Clear CMOS and RTC on Comet Lake-U Platforms

Connect Clear CMOS and RTC to J9J3 connector.

Note: The user needs an additional adaptor seen in FIGURE 64.

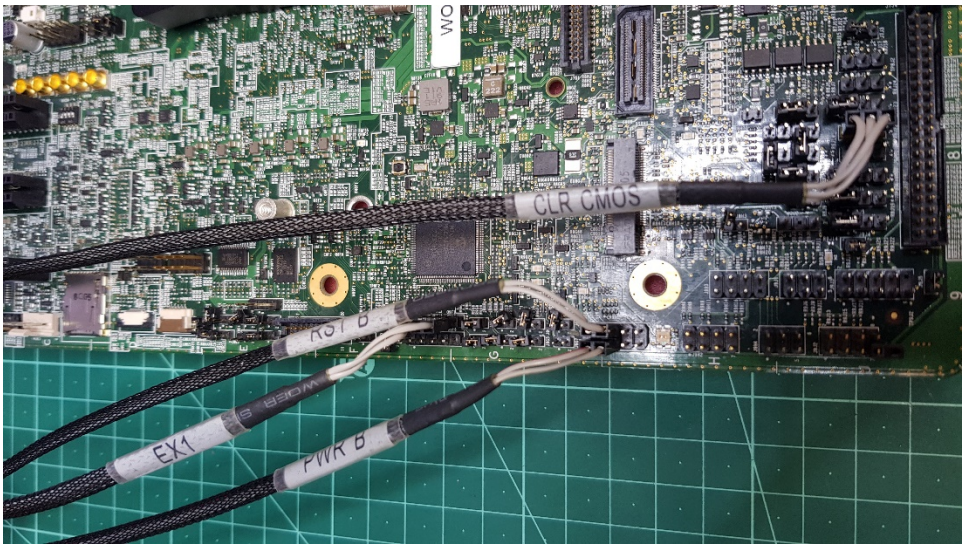
Figure 22.CML-U Platform with Clear CMOS and RTC Relays Connected



10.3 Connecting the Power and Reset Buttons on Comet Lake-S platforms

- Connect pins 6-8 of J9H1 on the front panel header for the **Power** button relay.
- Connect pins 5-7 of J9H1 on the front panel header for the **reset** button relay.

Figure 23. CML-S Power, Reset, Clear RTC and CMOS Connections



10.4 Connecting Clear CMOS and RTC on Comet Lake-S Platforms

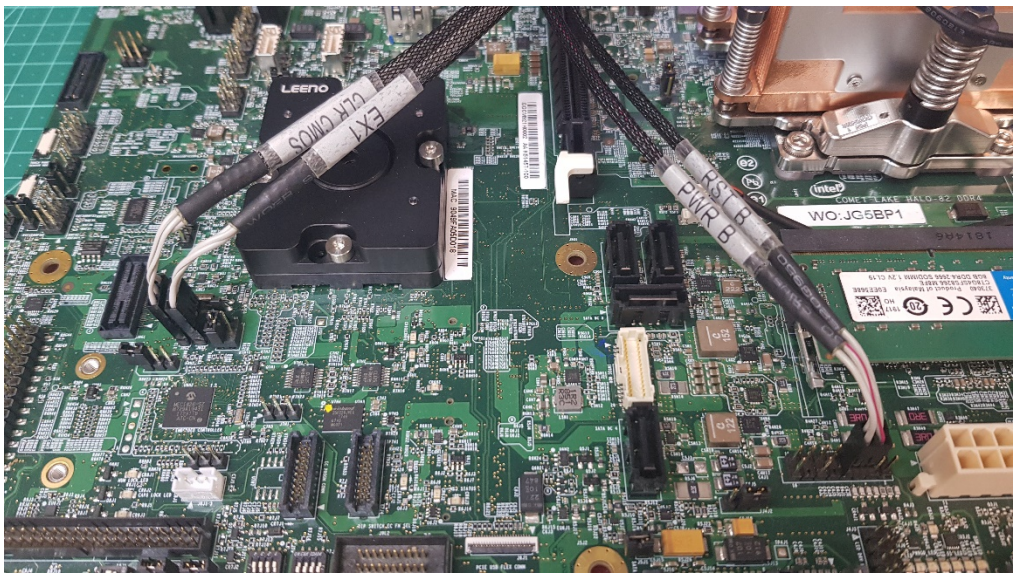
See **FIGURE 23** above for connecting CLR CMOS and RTC. Please note that Intel® APS does not have a cable for RTC CLR, EX1 cable can be used for that purpose after modifying the cable signal settings.

- Short pins 2-3 on J8J9 for CLR CMOS.
- Short pins 2-3 on J9E6 for CLR RTC.

10.5 Connecting the Power and Reset Buttons on Comet Lake-H platforms

- Connect pins 6-8 of J4J1on the front panel header for the **Power** button relay.
- Connect pins 5-7 of J4J1on the front panel header for the **reset** button relay.

Figure 24. CML-H Power, Reset, Clear RTC and CMOS Connections



10.6 Connecting Clear CMOS and RTC on Comet Lake-H Platforms

See **FIGURE 24** above for connecting CLR CMOS and RTC. Please note that Intel® APS does not have a cable for RTC CLR, EX1 cable can be used for that purpose after modifying the cable signal settings.

- Short pins 1-2 on J8G2 for CLR CMOS.
- Short pins 1-2 on J8G3 for CLR RTC.

10.7 Connecting Signal Sampling Cables to Comet Lake S/H/U Platforms

Connect the SML1 card seen in **FIGURE 57** on the LPC side band header.

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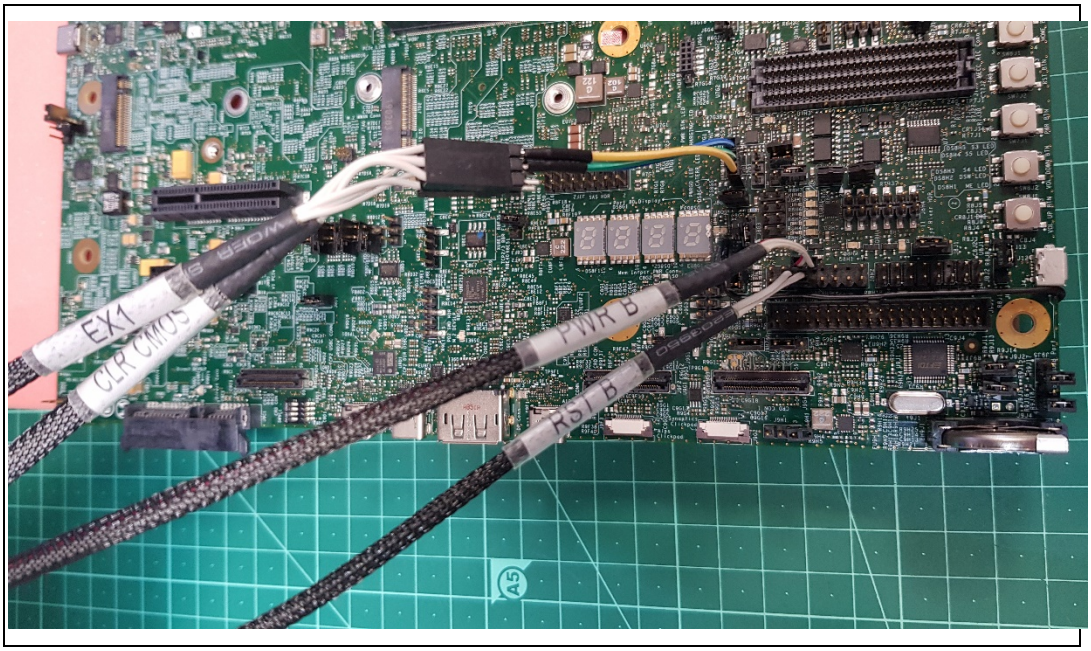
11 Connecting Intel® APS to Tiger Lake Platforms

11.1 Connecting the Power and Reset Buttons on Tiger Lake-UP3/UP4/Y Platforms

- Connect pins 6-8 of J8H2 on the front panel header for the **Power** button relay.
- Connect pins 5-7 of J8H2 on the front panel header for the **reset** button relay.

Figure 25. TGL-UP3/UP4/Y Power, Reset, Clear CMOS and RTC Connections



11.2 Connecting Clear CMOS and RTC on Tiger Lake-UP3/UP4 Platform

See FIGURE 25 above for connecting CLR CMOS and RTC. Please note that Intel® APS does not have a cable for RTC CLR, EX1 cable can be used for that purpose after modifying the cable signal settings.
Connect Clear CMOS and RTC to J7G1 connector, where pins 1-2 are for Clear RTC, and pins 2-3 are for Clear CMOS.

Note: The user needs an additional adaptor seen in FIGURE 64.

11.3 Connecting Clear CMOS and RTC on Tiger Lake-Y Platform

See FIGURE 25 above for connecting CLR CMOS and RTC. Please note that Intel® APS does not have a cable for RTC CLR, EX1 cable can be used for that purpose after modifying the cable signal settings.
Connect Clear CMOS and RTC to J7G3 connector, where pins 1-2 are for Clear RTC, and pins 2-3 are for Clear CMOS.

Note: The user needs an additional adaptor seen in FIGURE 64.

11.4 Connecting Signal Sampling Cables to Tiger Lake-UP3/UP4/Y Platforms

Connect the SML1 card seen in FIGURE 57 on the LPC side band header.

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12 Sampling Platform Signals with the Intel® APS

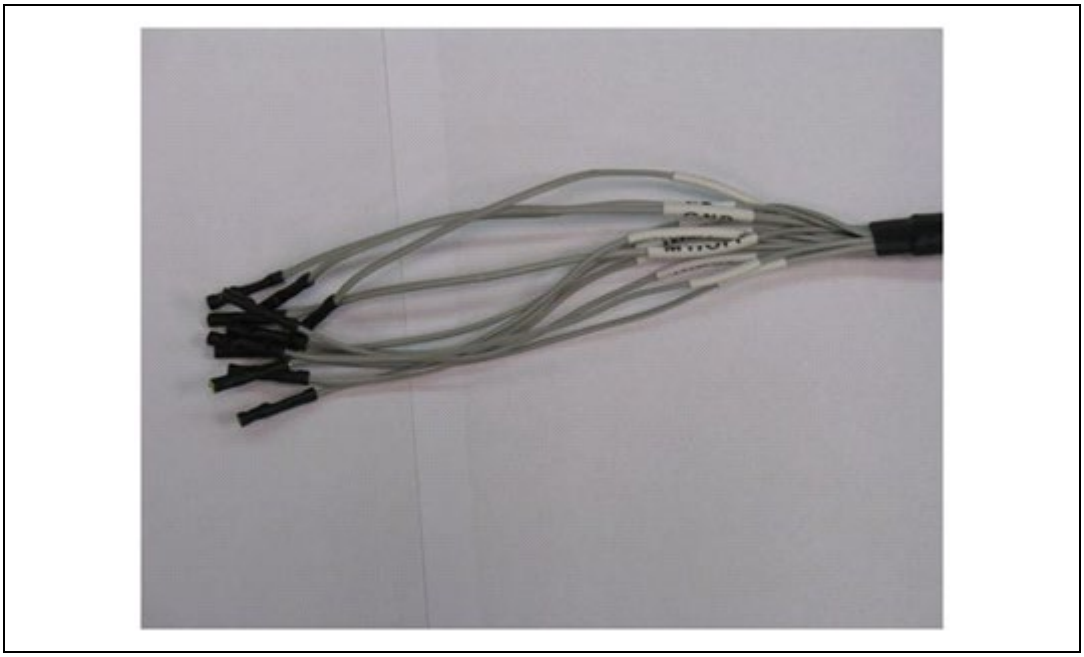
The Intel® APS samples the following signals on the system under test: S0 state, S3, S4, S5, ME (SLP_M).

12.1 Connecting the Signal Sampling Cables to the System under Test

To enable sampling signals on the system under test, you need to connect the Intel® APS to the system under test via 6 1-pin cables on the Intel® APS Main cable. You need to connect these cables to the relevant signals on the system under test. The 6 cables are labeled with the following signal names:

- **Sus** (Vcc_Sus/S0)
- **S3**
- **S4**
- **S5**
- **M1/OFF** (M1/M-OFF)
- **GND** (Ground)

Figure 26. Signal Sampling Cables



Note: Make sure you connect all 6 cables (**Sus, S3, S4, S5, M1/OFF, GND**) to the relevant signals on the SUT. Otherwise you will not be able to check the system's power state or perform power tests.

In addition to these signals, you can also sample additional signals on the platform by connecting them to the following cables on the main cable:

- **INEX1 (Deep S4/5)**
- **INEX2 (Deep S3)**
- **INEX3**
- **INEX4**
- **INEX5**

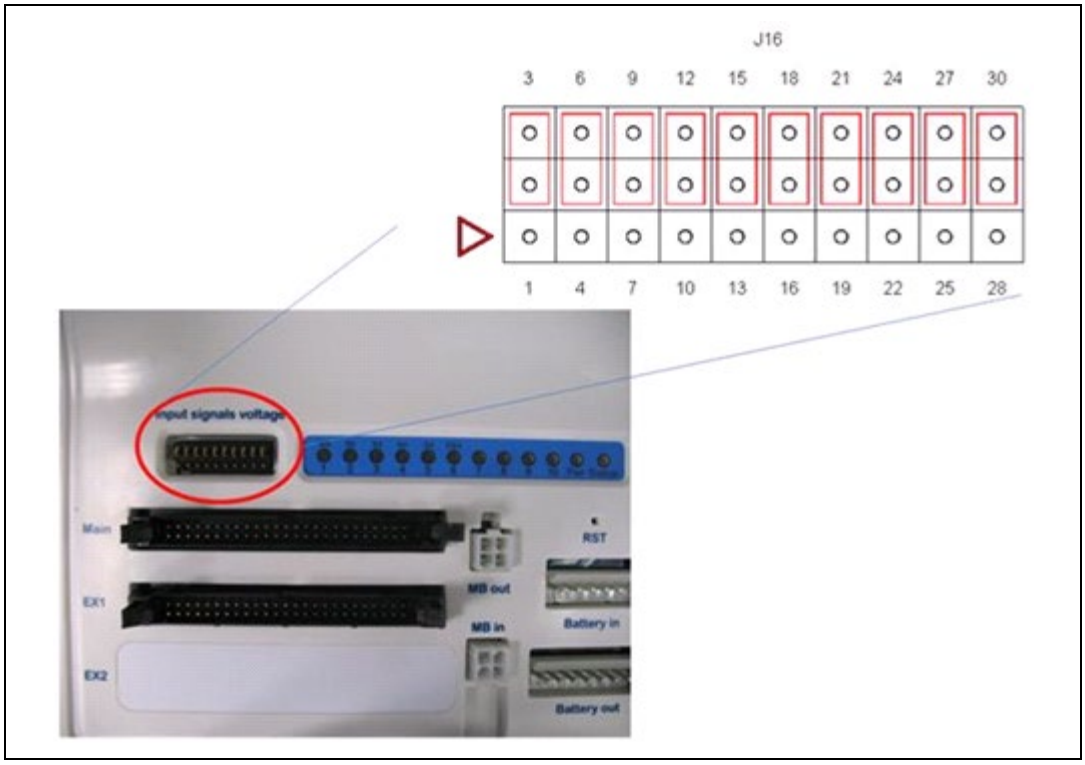
Note: If you do not connect all of the additional cables (**INEX1 (Deep S4/5)**, **INEX2 (Deep S3), INEX3, INEX4, INEX5**) to the relevant signals, **you must connect the unconnected cables to GND**; do not leave them unconnected. Unconnected cables may give unexpected results.

Note: On input signal voltages on the system under test:

1. **To avoid burning out circuits on the Intel APS, make sure that the voltages of the input signals do not exceed 4 volts.**

2. The Input signals voltage jumper block on the Intel® APS front panel contains jumpers that specify the voltages of the 10 input signals.

Figure 27. Input Signals Voltage Jumper Block with Default Settings (jumper position 2-3)



If a signal's input voltage level is 3.3V, the jumper for that signal should be set to position 2-3 (default). If the voltage is 1.1V, the signal's jumper should be set to

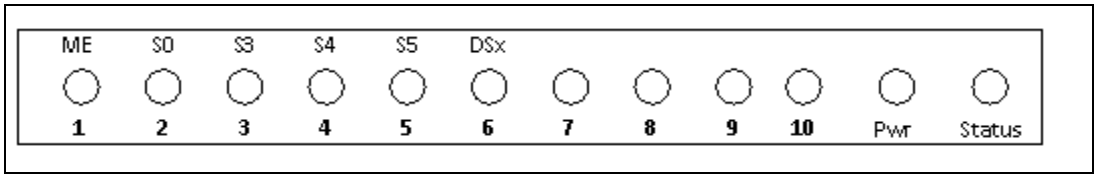
position 1-2. The following table identifies the jumper for each signal (jumper 1 is the leftmost jumper; jumper position 1 is the lower jumper position):

Signal	Jumper
Sus	1
S3	2
S4	3
S5	4
Me	5
Inex1	6
Inex2	7
Inex3	8
Inex4	9
Inex5	10

12.2 Understanding the Intel® APS LED Indicators

The Intel® APS includes twelve LED indicators. Six of the indicators allow the detection of the power state of the system under test.

The following figure shows the LEDs for each power state:



This LED…	Indicates Status of this Signal
LED 1	ME
LED 2	S0
LED 3	S3
LED 4	S4
LED 5	S5
LED 6	INEX1(Deep S4/5)
LED 7	INEX2 (Deep S3)
LED 8	INEX3
LED 9	INEX4
LED 10	INEX5
PWR	APS powered on and ready
Status	Red – APS not initialized by software or reset button is pressed Green – APS powered on and ready

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13 USB Switch

The Intel® APS includes the option to switch control of a USB device between 2 computers. This enables actions such as file transfer via USB key, USB Provisioning testing, etc.

The switching is performed via the Intel® APS Software.

13.1 Connecting the USB Switch

You set up the USB switching functionality by connecting a USB device and 2 computers to the USB sockets on the rear panel of the Intel® APS (see Figure 2. Intel® APS Rear Panel).

To set up USB switching functionality:

1. Connect the USB device to the Intel® APS **USB SW** socket.
2. Connect the first computer to the **USB 1 out** socket.
3. Connect the second computer to the **USB2 out** socket.

Figure 28. USB Disk on Key and 2 Computers Connected to Rear Panel

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14 SPI Flash Burning (CRB only)

To enable SPI flash burning on a CRB via the Intel® APS Software, you use the Feature cable.

1. Connect the Feature cable's 40-pin connector to the J2 connector under the lid of the Intel® APS.
2. Connect the Feature cable's SPI cable to the SPI PROGRAMMING header on the CRB.
3. Connect the Feature cable's CS connector to the SPI_CS# connector on the CRB.

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15 Reading Post Code from CRB

15.1 Reading Post Code from a Mobile CRB

To enable reading the Post code from a mobile CRB:

1. Connect the Feature cable's 40-pin connector to the J2 connector under the lid of the Intel® APS.
2. Connect the Feature cable's **Port 80** connector to the Port 80 mobile daughter card on the mobile CRB.

15.2 Reading Post Code from a Desktop CRB

To enable reading the Post code from a workstation CRB:

1. Connect the Feature cable's 40-pin connector to the J2 connector under the lid of the Intel® APS.
2. Connect the Port 80 mobile daughter card to the **LPC** connector on the workstation CRB. Note that the Port 80 mobile daughter card is not supplied with the Intel® APS kit and is not part of the workstation CRB. It must be purchased from Intel to enable reading the post code from a workstation CRB.
3. Connect the Feature cable's **Port 80** connector to the Port 80 mobile daughter card.

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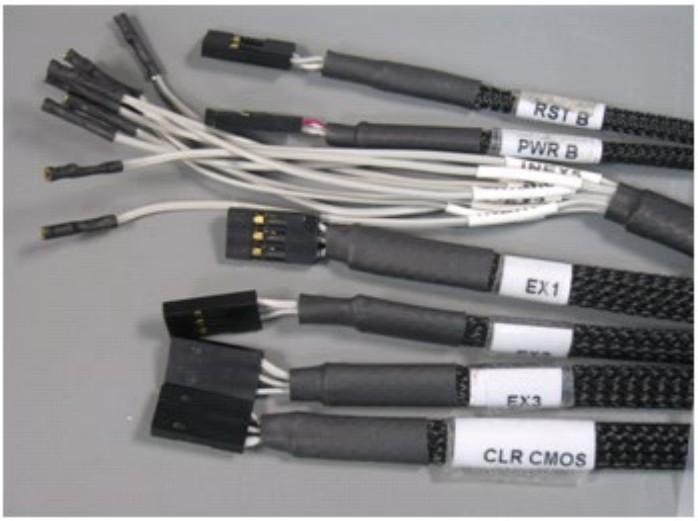
Appendix A Control Cables

A.1 Main Cable

Figure 29. Main Cable – Picture 1

Figure 30. Main Cable – Picture 2



A.2 Feature Cable

Figure 31. Feature Cable – Picture 1

Figure 32. Feature Cable – Picture 2

Figure 33. Feature Cable Connected to J2 (lid open)

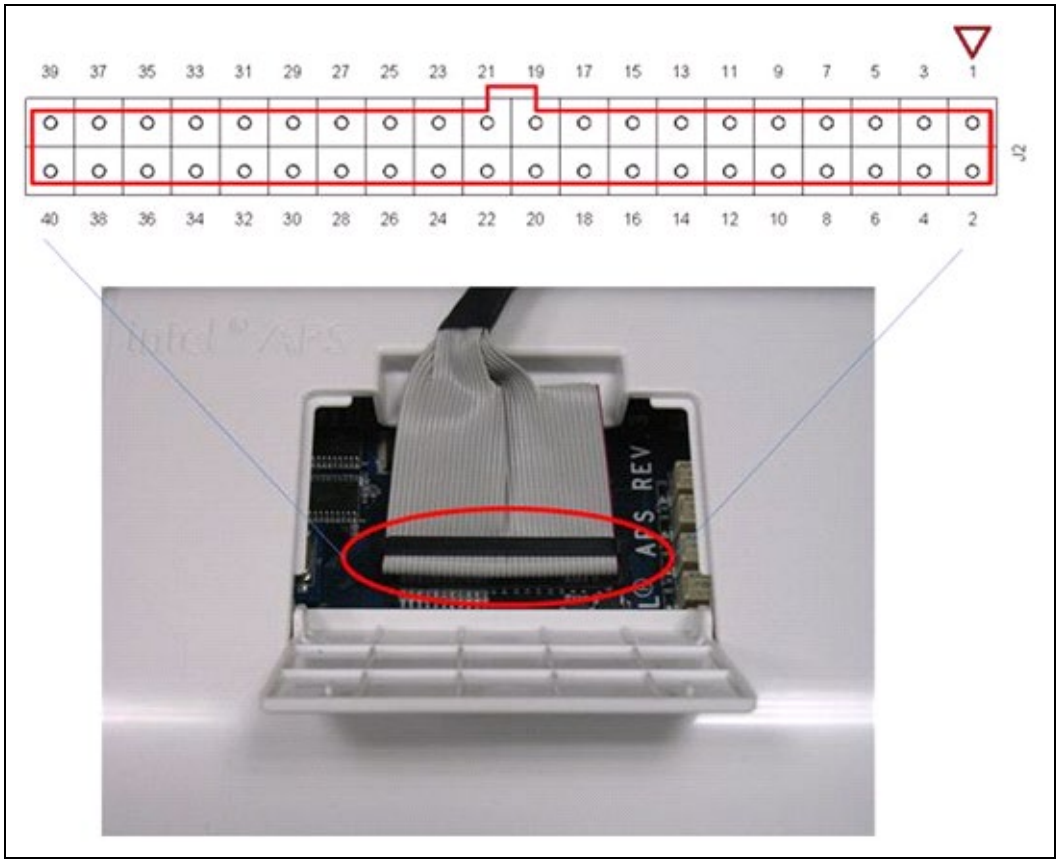


Figure 34. Feature Cable Connected to J2 (lid closed)

Figure 35. Feature Cable Connected to Port80 Daughter Card on Huron River

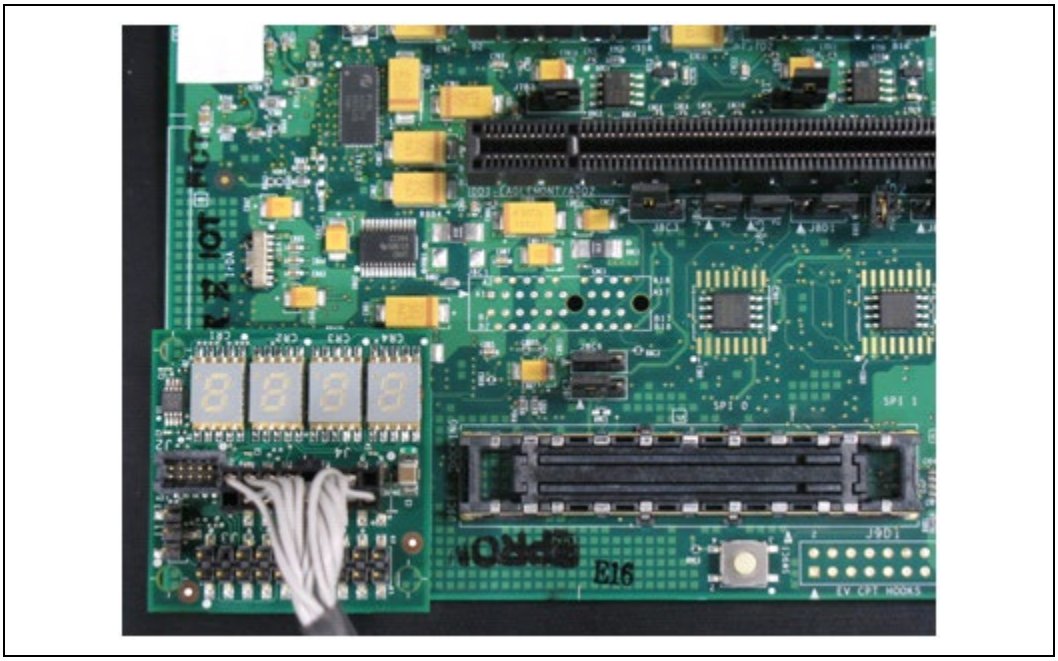
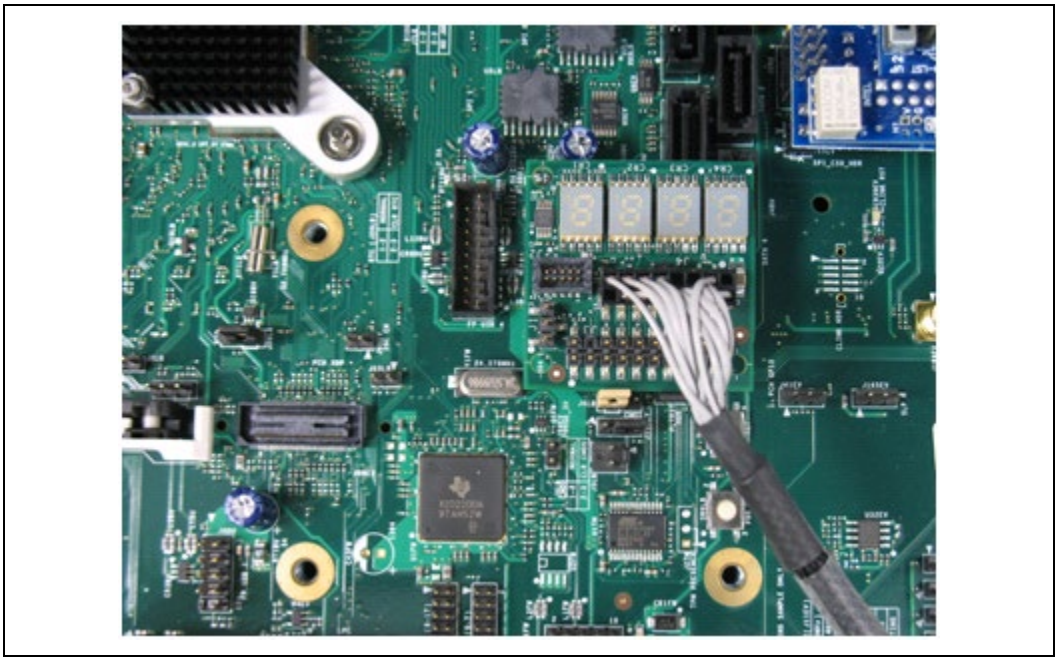


Figure 36. Feature Cable Connected to Port80 Daughter Card on Sugar Bay (J4LH)



A.3 EX1 Cable

Figure 37. EX1 Cable – Picture 1

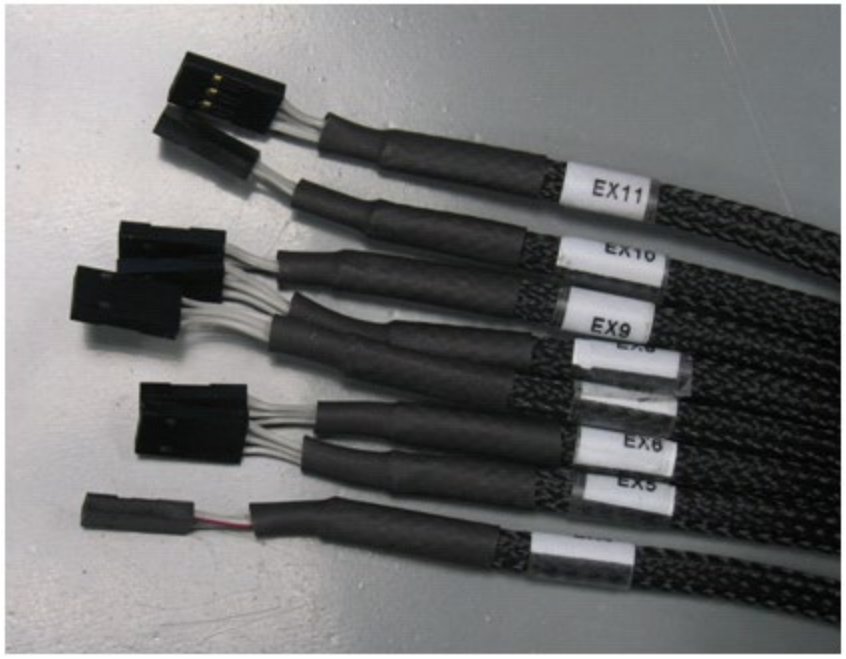


Figure 38. EX1 Cable – Picture 2

A.4 Mobile Platform Power Cable

Figure 39. Mobile Platform Power Cable

A.5 Mobile Power Extension Cable

Figure 40. Mobile Power Extension Cable

A.6 Battery Cable

Figure 41. Battery Cable

Figure 42. Molex_09-50-3071 (Intel® APS battery "OUT" connector)

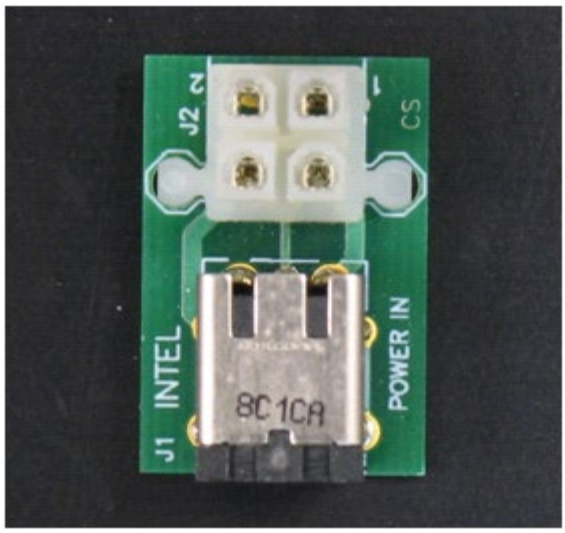
Figure 43. Molex_09-50-3081 (Intel® APS battery "IN" connector)

A.7 USB Data Cable

Figure 44. USB A-B (Data Cable)

A.8 Mobile Platform Adapter Board

Figure 45. Mobile Platform Adapter Board



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Appendix B Desktop Unit

The desktop unit provides the option to remotely disconnect/connect the platform's power cable (to transition to and from G3 state).

Figure 46. Desktop Intel® APS Unit

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Appendix C Part Number List

Description	Cable - Platform Connector (connector on the cable)- P/N	Required Platform Header P/N
PWR button (2- Pin)	Molex_70066-0176	Samtec_TSW-102-07-T-S
RST button (2- Pin)	Molex_70066-0176	Samtec_TSW-102-07-T-S
Clear CMOS (3- Pin)	Molex_70066-0177	Samtec_TSW-102/3-07-T-S
EX1-3 (3- Pin)	Molex_70066-0177	Samtec_TSW-103-07-T-S
Battery	Molex_09-50-3081	Molex_26-60-4070

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Appendix D Verifying Intel® APS Operation

After you have connected the Intel® APS, you should use the Intel® Automated Power Switch Software (Intel® APS Software) application to test its connectivity and functionality. For details, refer to the Intel® Automated Power Switch Software Installation and User's Guide.

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Appendix E Simulating HW Radio Frequency Kill Using Intel® APS

For cases where OEMs need to simulate hardware Radio Frequency Kill, Intel® APS EX3 can be used for this purpose.

E.1 RF Kill for Tiger Lake UP3/UP4/Y Platforms

Short pins 3-4 on connector J9J5 as shown in the figure below.

Figure 47: HW RF Kill for TGL UP3/UP4/Y Platforms

E.2 RF Kill for Comet Lake H Platform

Short pins 3-4 on connector J8A2 as shown in the figure below.

Figure 48: HW RF Kill for CML-H Platform

E.3 RF Kill for Comet Lake S Platform

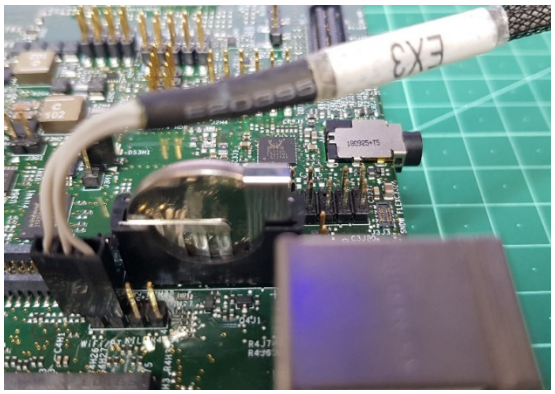
Short pins 3-4 on connector J8H5 as shown in the figure below.

Figure 49: HW RF Kill for CML-S Platform

E.4 RF Kill for Ice Lake U Platform

Short pins 3-4 on connector J4H2 as shown in the figure below.

Figure 50: HW RF Kill for ICL-U/WHL-U/CML-U/CFL-U Platforms



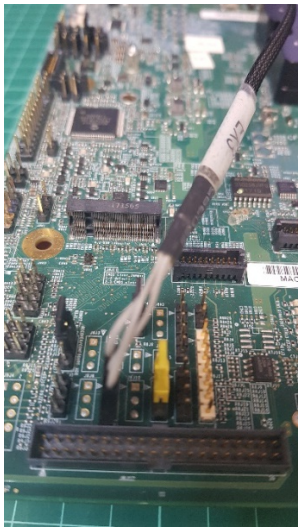
E.5 RF Kill for Whiskey Lake-U, Comet Lake-U, and Coffee Lake-U Platforms

Short pins 3-4 on connector J3H3 as shown in FIGURE 50.

E.6 RF Kill for Coffee Lake S Platform

Short pins 2-3 on connector J8J9 as shown in the figure below.

Figure 51: HW RF Kill for CFL-S Platform

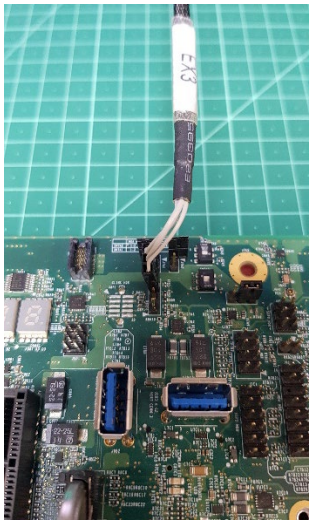


E.7 RF Kill for Coffee Lake H Platform

For Coffee Lake-H ERB, short pins 3-4 on connector J8A2 as shown in FIGURE 48.

For Coffee Lake-H CRB, short pins 3-4 on connector J8A2 as shown in the figure below.

Figure 52: HW RF Kill for CFL-H CRB Platform



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Appendix F Connecting Intel® APS to Basin Falls Platforms

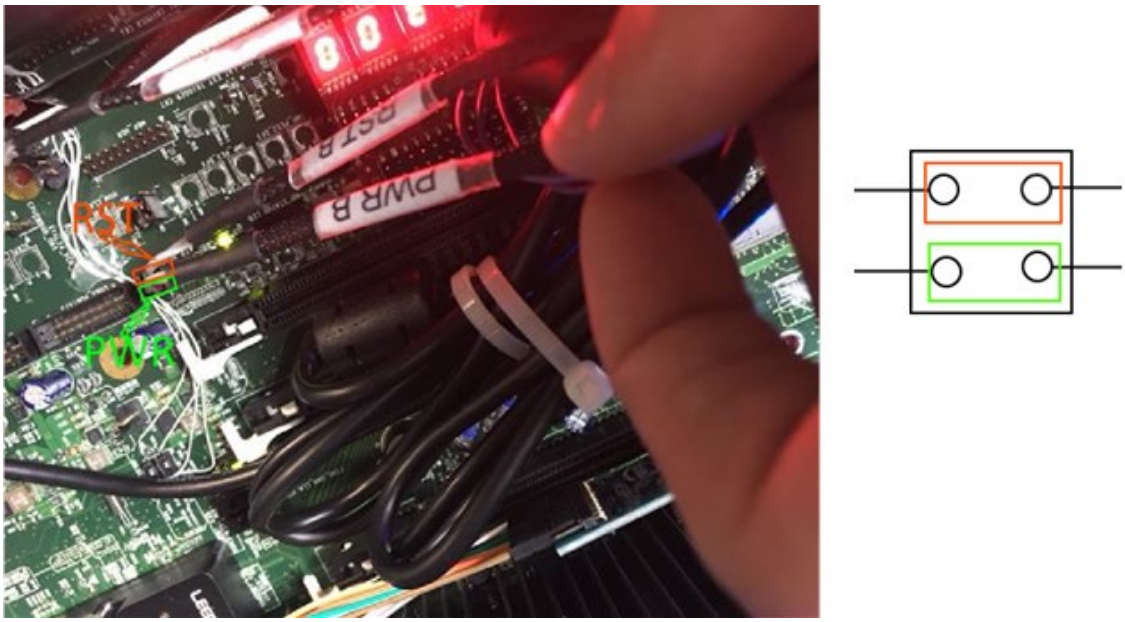
The following configuration is for BSF platforms. The user must configure APS-SW settings and choose "KabyLake-Mobile" platform.

F.1 Connecting the Power and Reset buttons on Basin Falls

Connect the **power-button** and **reset-button** relay to the connector (front panel header) as shown below.

- Connect the power button relay to J9E1 pins 6 and 8
- Connect the reset button relay to J9E1 pins 5 and 7

Figure 53. BSF platform with power and reset relays connected



F.2 Connecting to Clear CMOS on Basin Falls Platform

Connect the Clear CMOS cable from Intel® APS to the connector as shown in Figure 54 below.

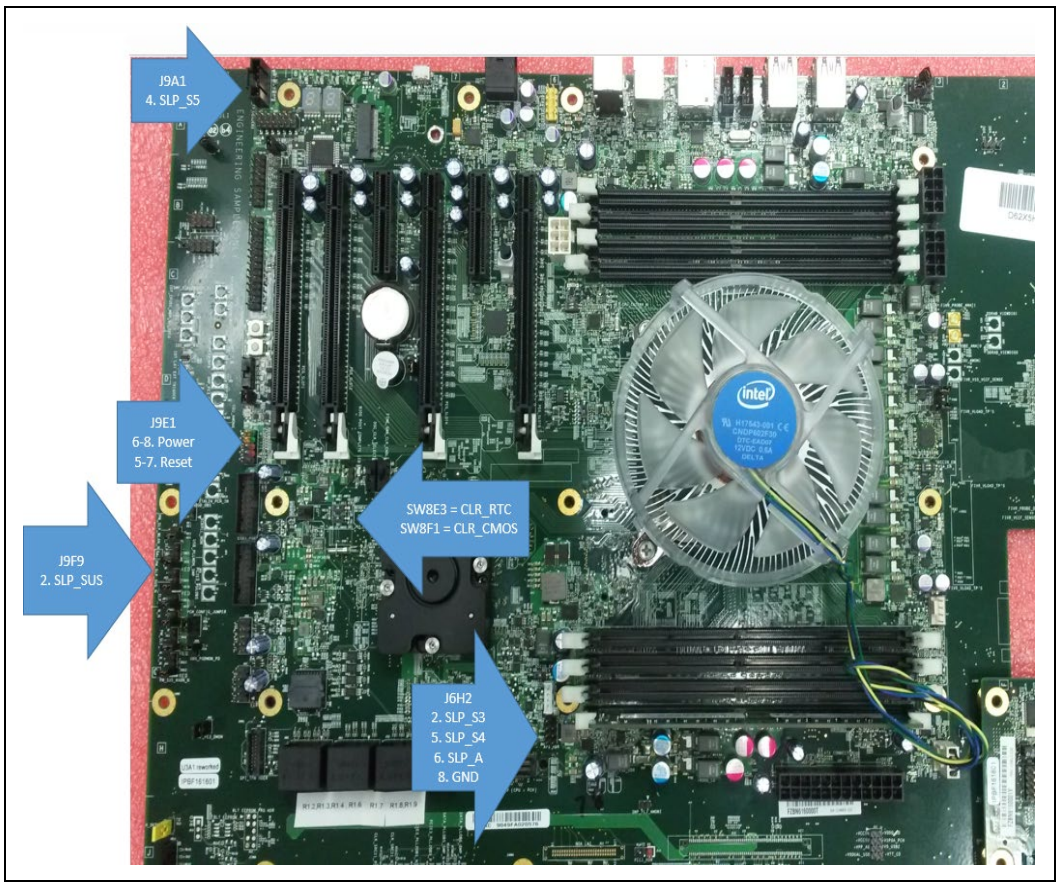
Note: The platform needs to have CMOS rework for automation. Remove the dipswitch and rework headers instead.

F.3 Connecting Signal Sampling Cables to Basin Falls Platform

See the picture below for pin locations on the board.

- Connect the **SUS** cable to J9F9 pin 2.
- Connect the **GND** cable to J6H2 pin8, **S4** cable to J6H2 pin 5, **S3** cable to J6H2 pin 2, and **SLP_A** cable to J6H2 pin 6.
- Connect the **S5** cable to J9A1 pin 4.

Figure 54 Connecting Signal Sampling Cables to BSF



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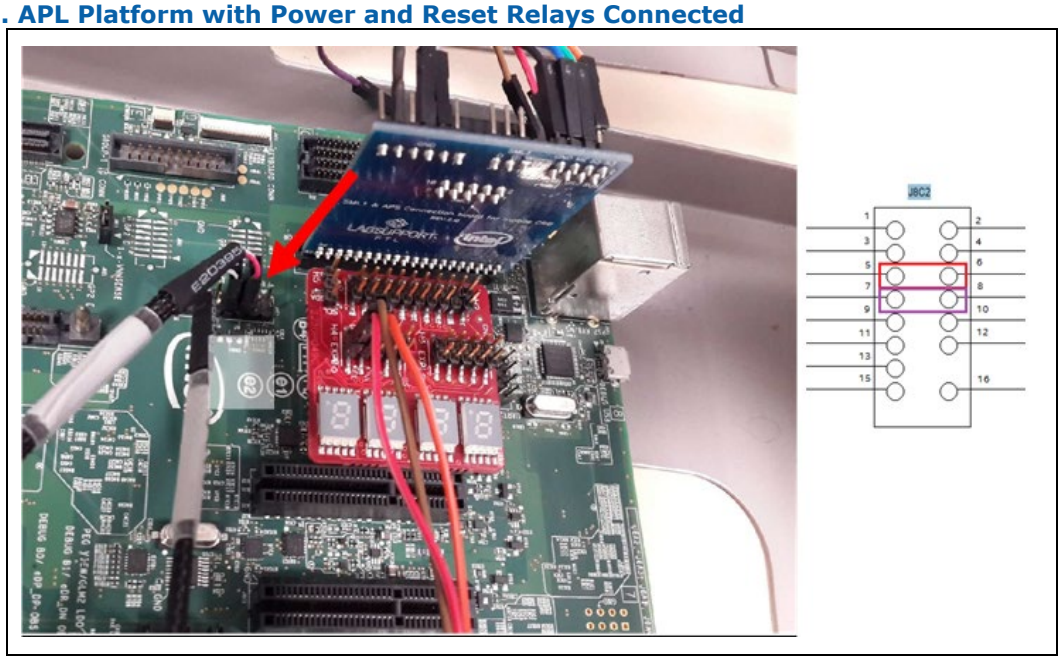
Appendix G Connecting Intel® APS to Broxton-P (Apollo Lake) Platforms

The following configuration is for BXT-P (APL) platforms. The user must configure APS-SW settings and choos “APL mobile” platform. “APL desktop” configuration is for a platform that doesn’t exist yet.

G.1 Connecting the Power and Reset Buttons on Apollo Lake Platforms

Connect the **power-button** relay and **reset-button** relays to the connector J8C2:

Figure 55. APL Platform with Power and Reset Relays Connected



G.2 Connecting to Clear CMOS and RTC on Apollo Lake Platform

See the picture below for connecting CLR CMOS and RTC on APL. Please note that Intel® APS does not have a cable for RTC CLR, EX1 cable can be used for that purpose after modifying the cable signal settings.

- Short pins 1-2 on J3B5 for CLR CMOS
- Short pins 1-2 on J3B4 for CLR RTC

Figure 56. CLR CMOS and RTC Cables Conected to APL

G.3 Connecting Signal Sampling Cables to Apollo Lake Platform

Connect the SML1 card seen below on the LPC side band header.

Figure 57. SML1 Card

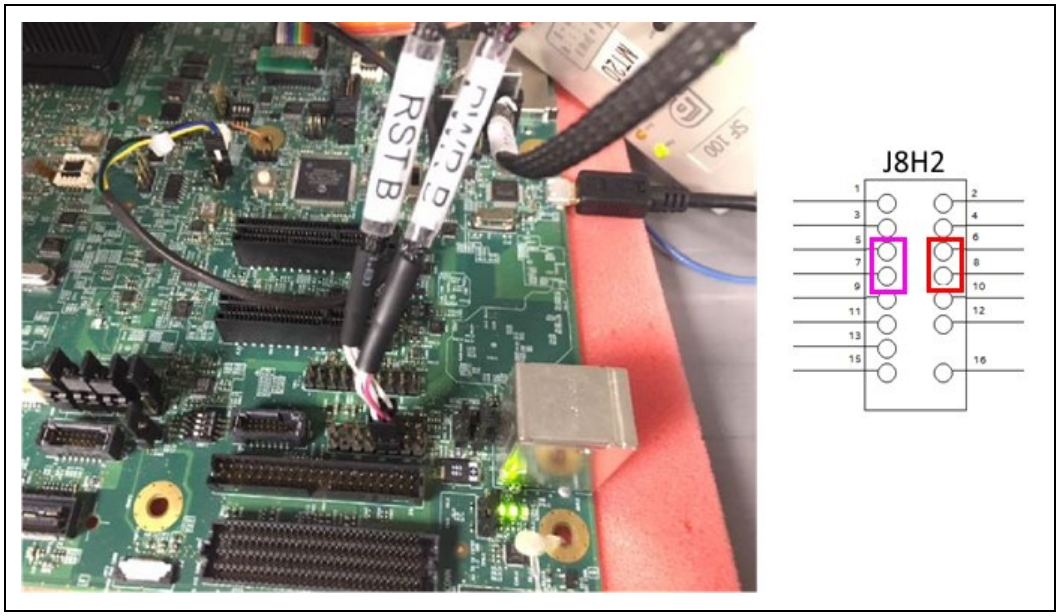
Appendix H Connecting Intel® APS to Gemini Lake Platforms

The following configuration is for GLK platforms. The user must configure APS-SW settings and choose “GeminiLake - Mobile” platform.

H.1 Connecting the Power and Reset Buttons on Gemini Lake Platforms

Connect the **power-button** relay and **reset-button** relay to the connector J8H2 on the front panel header:

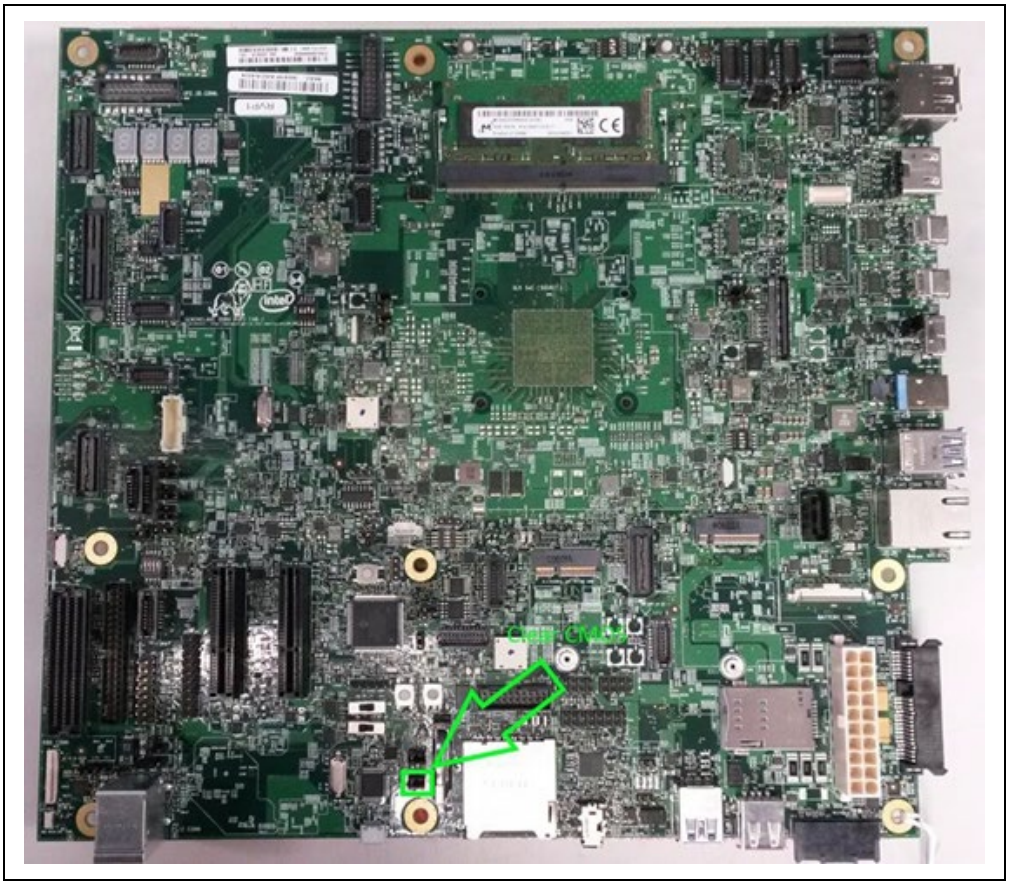
Figure 58. GLK Platform with Power and Reset Relays Connected



H.2 Connecting to Clear CMOS on Gemini Lake Platform

Connect the Clear CMOS cable from Intel® APS to the connector as shown below:

Figure 59. GLK Platform with CMOS Relay Connected



H.3 Connecting Signal Sampling cables to Gemini Lake Platform

Connect the SML1 card seen in FIGURE 57 on the LPC side band header.

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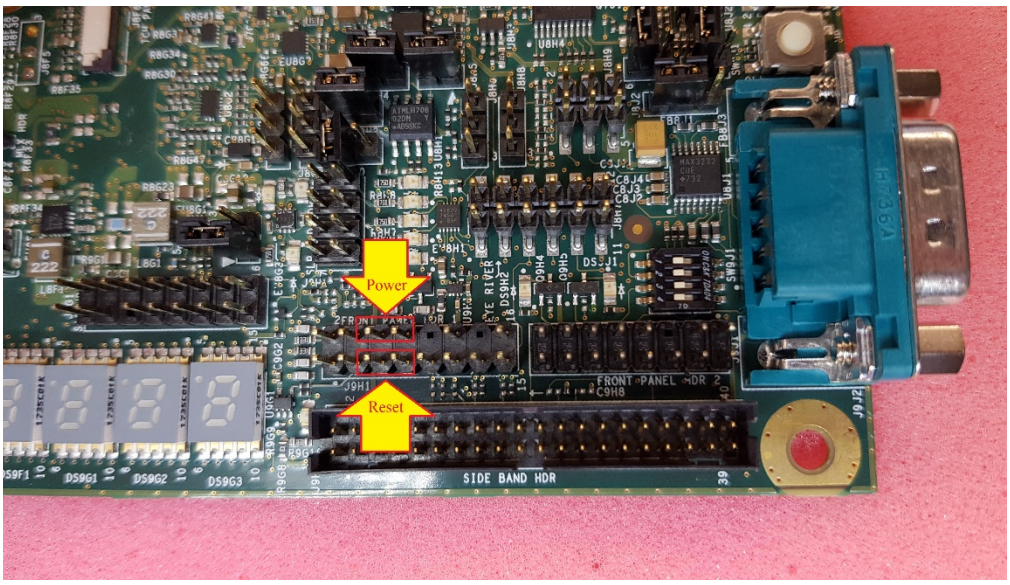
Appendix I Connecting Intel® APS to Ice Lake Platforms

I.1 Connecting the Power and Reset Buttons on Ice Lake-U Platform

- Connect pins 6-8 of J9H1 on the front panel header for the Power button relay.
- Connect pins 5-7 of J9H1 on the front panel header for the reset button relay

Figure 60: ICL-U Power and Reset Button Relays Connected

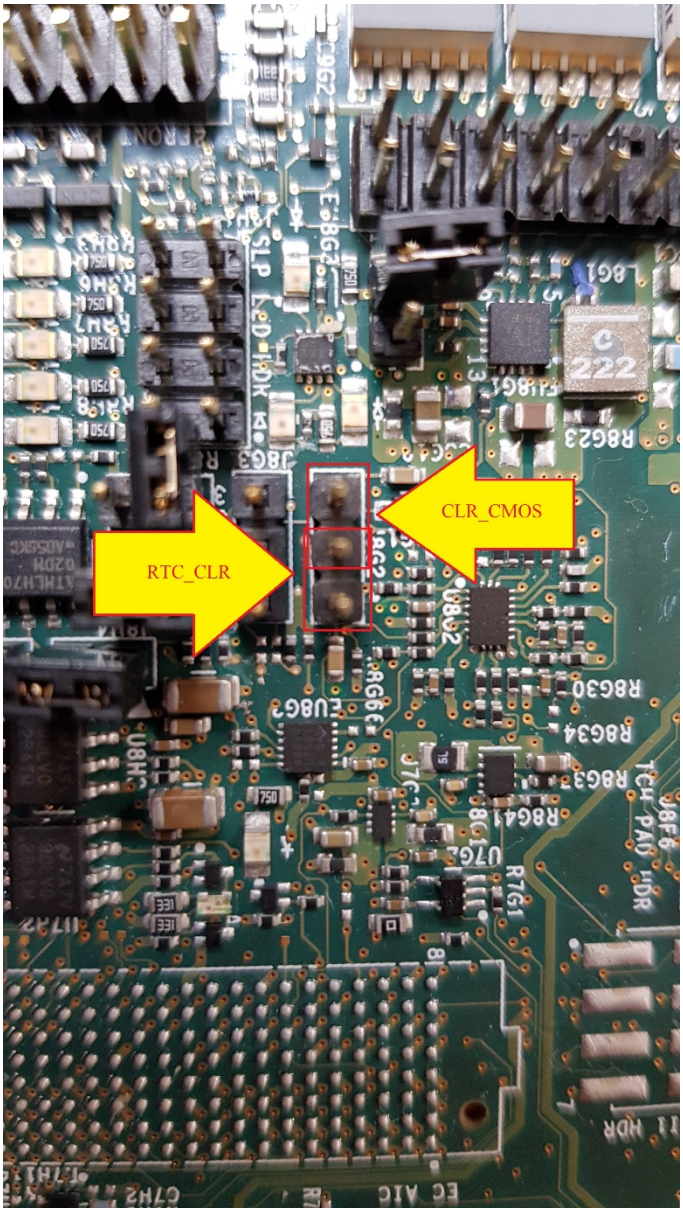


I.2 Connecting Clear CMOS and RTC on Ice Lake-U Platform

See the picture below for connecting CLR CMOS and RTC on ICL-U. Please note that Intel® APS does not have a cable for RTC CLR, EX1 cable can be used for that purpose after modifying the cable signal settings.

- Short pins 2-3 on J8G2 for CLR CMOS.
- Short pins 1-2 on J8G2 for CLR RTC.

Figure 61: ICL-U Platform with Clear CMOS and RTC Relays Connected



Appendix J Connecting Intel® APS to Cannon Lake Platform

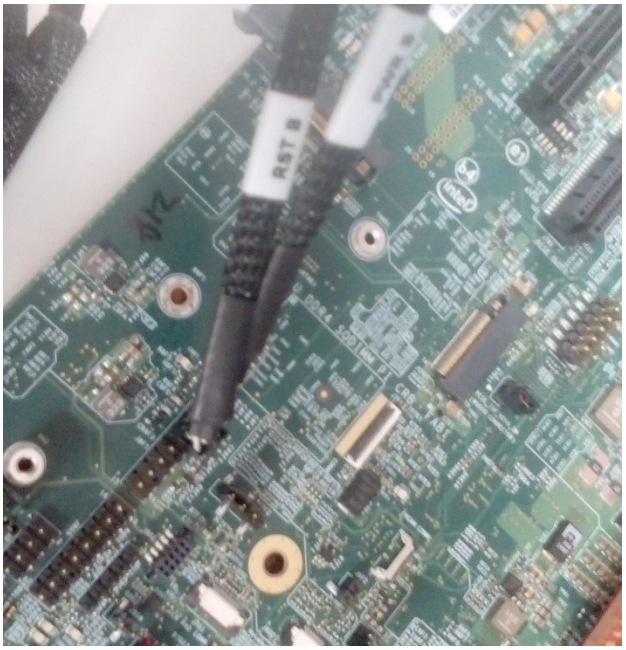
The following configuration is for CNL U/Y platforms. The user must configure APS-SW settings and choose "CanonLake - Mobile" platform.

J.1 Connecting the Power and Reset Buttons on Cannon Lake-U Platforms

For the power-button relay, rework should be done to the CNL platform (O-03 power button).

- Connect pins 6-8 of J8F1 on the front panel header for the **Power** button relay.
- Connect pins 5-7 of J8F1 on the front panel header for the **reset** button relay

Figure 62. CNL-U Power and Reset Button Relays Connected



J.2 Connecting Clear CMOS and RTC on Cannon Lake-U Platform

See the picture below for connecting CLR CMOS and RTC on CNL-U. Please note that Intel® APS does not have a cable for RTC CLR, EX1 cable can be used for that purpose after modifying the cable signal settings.

- Short pins 2-3 on J9J4 for CLR CMOS.
- Short pins 1-2 on J9J4 for CLR RTC.

Note: The user needs an additional adaptor seen in FIGURE 64 below.

Figure 63. CNL-U Platform with Clear CMOS and RTC Relays Connected

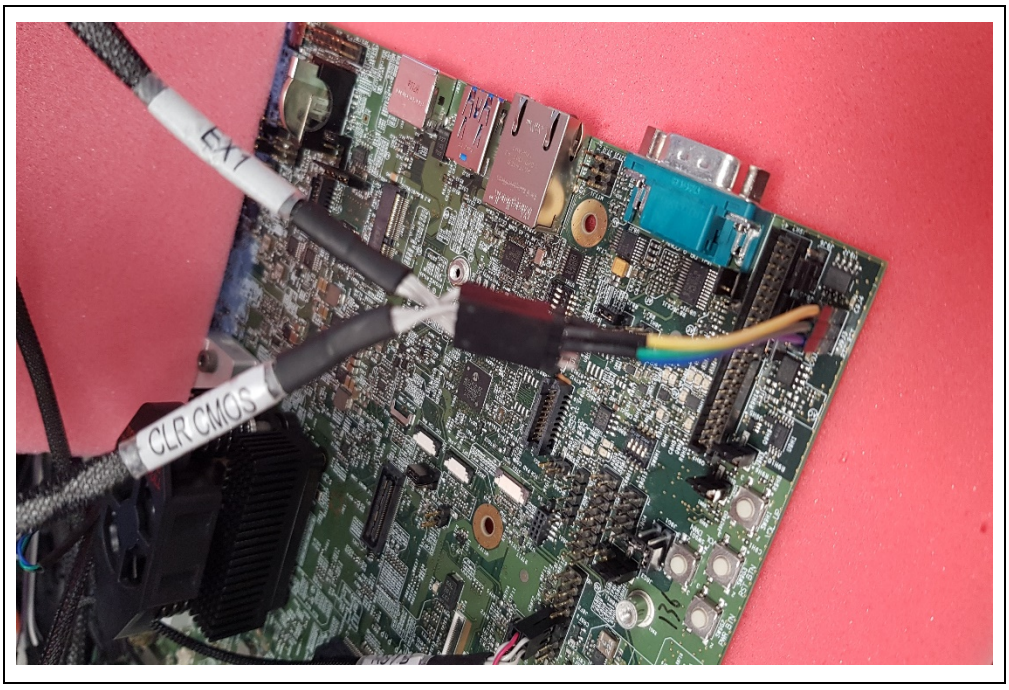
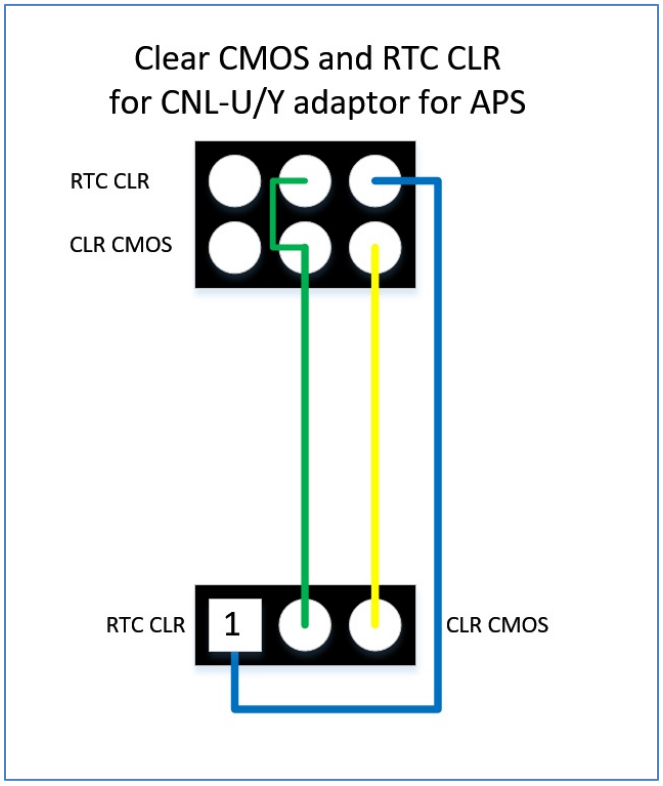


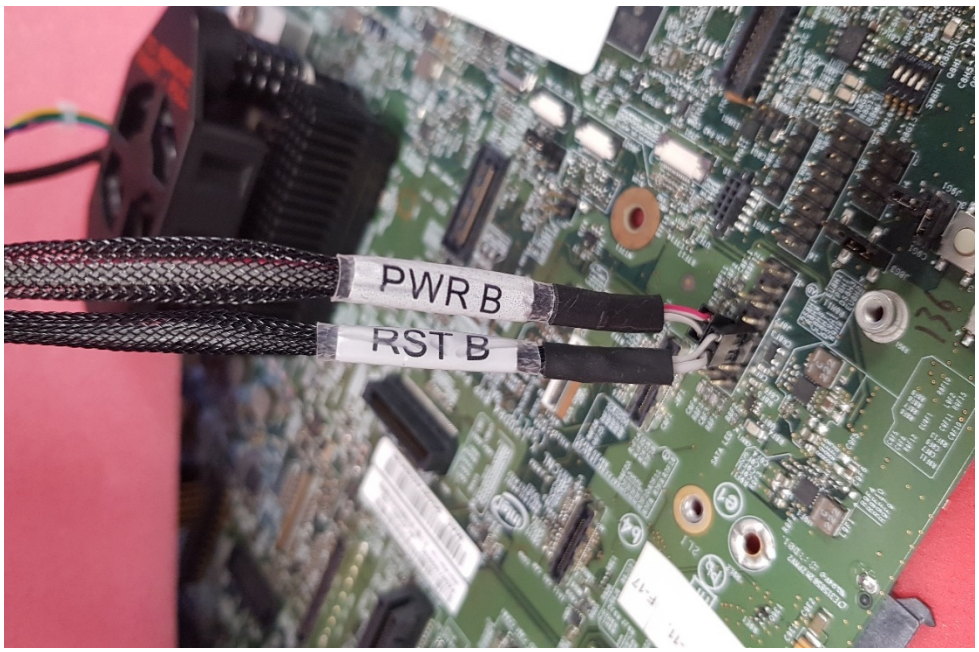
Figure 64. Adaptor Needed for CNL U/Y CLR CMOS and RTC Cable Connection



J.3 Connecting the Power and Reset Buttons on Cannon Lake-Y Platforms

For connector J8F2 on the front panel header, connect the **Power** relay to pins 6-8 and the **Reset** relay to pins 5-7 as seen below.

Figure 65. CNL-Y with Power and Reset Relays Connected



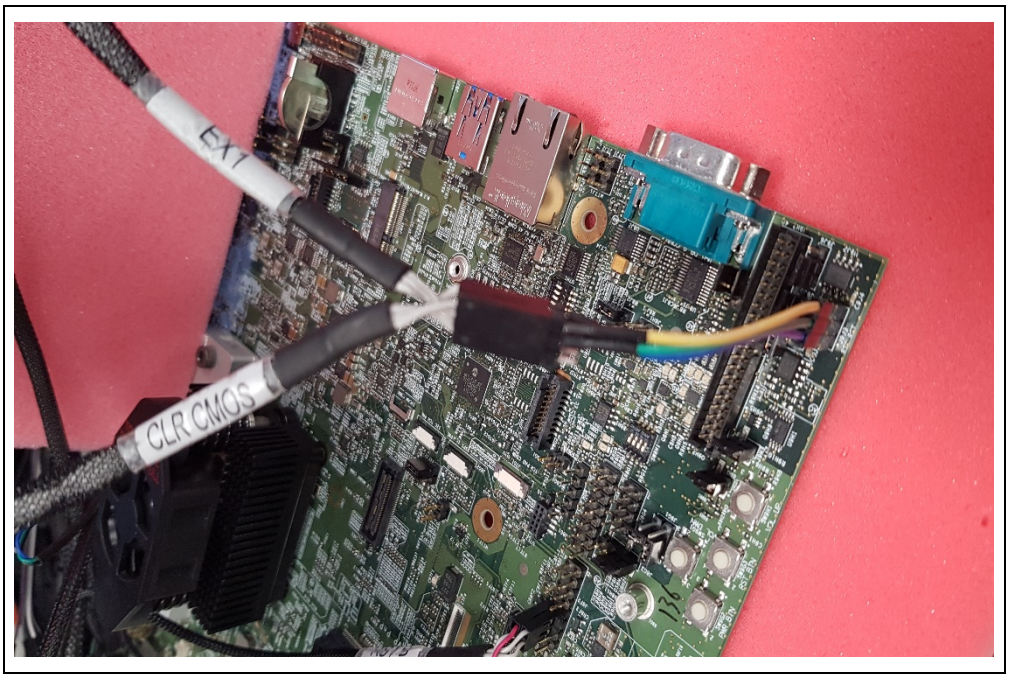
J.4 Connecting Clear CMOS and RTC on Cannon Lake-Y Platforms

See the picture below for connecting CLR CMOS and RTC on CNL-Y. Please note that Intel® APS does not have a cable for RTC CLR, EX1 cable can be used for that purpose after modifying the cable signal settings.

- Short pins 2-3 on J9J3 for CLR CMOS
- Short pins 1-2 on J9J3 for CLR RTC

Note: The user needs an additional adaptor seen in FIGURE 64.

Figure 66. CNL-Y Platform with CLR CMOS and RTC Connected



J.5 Connecting Signal Sampling Cables to CNL-U/Y platforms

Connect the SML1 card seen in FIGURE 57 on the LPC side band header.

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Appendix K Connecting Intel® APS to Coffee Lake Platform

The following configuration is for CFL-S platforms. The user must configure APS-SW settings and choose "CofeeLake - Desktop" platform.

K.1 Connecting the Power and Reset Buttons on Coffee Lake-S platforms

See Figure 68 below for Connecting the power and reset relays on CFL-S platform.

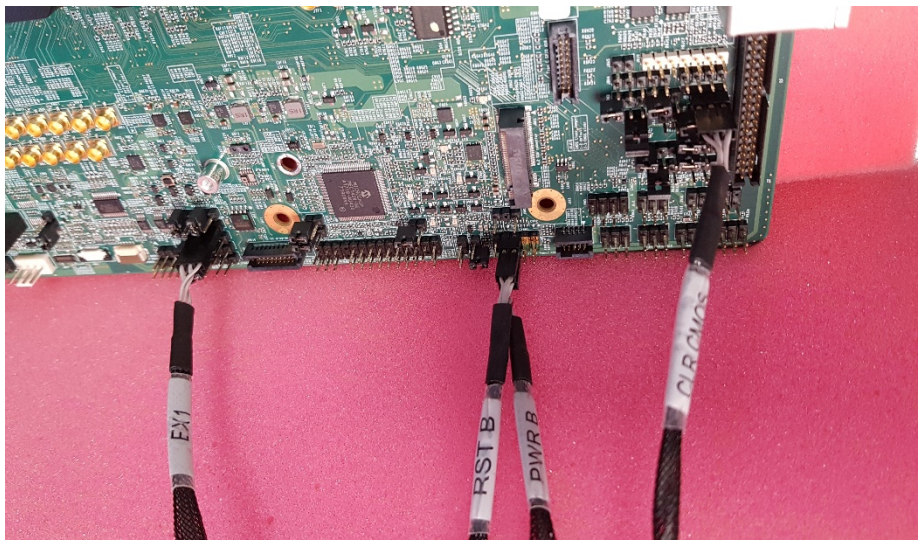
- Connect the power button relay to pin 6 of J9H2 on the front panel header.
- Connect the reset button relay to pin 7 of J9H2 on the front panel header.

K.2 Connecting Clear CMOS and RTC on Coffee Lake-S Platforms

See the picture below for connecting CLR CMOS and RTC on CNL-Y. Please note that Intel® APS does not have a cable for RTC CLR, EX1 cable can be used for that purpose after modifying the cable signal settings.

- Short pins 2-3 on J8J11 for CLR CMOS
- Short pins 2-3 on J9E5 for CLR RTC

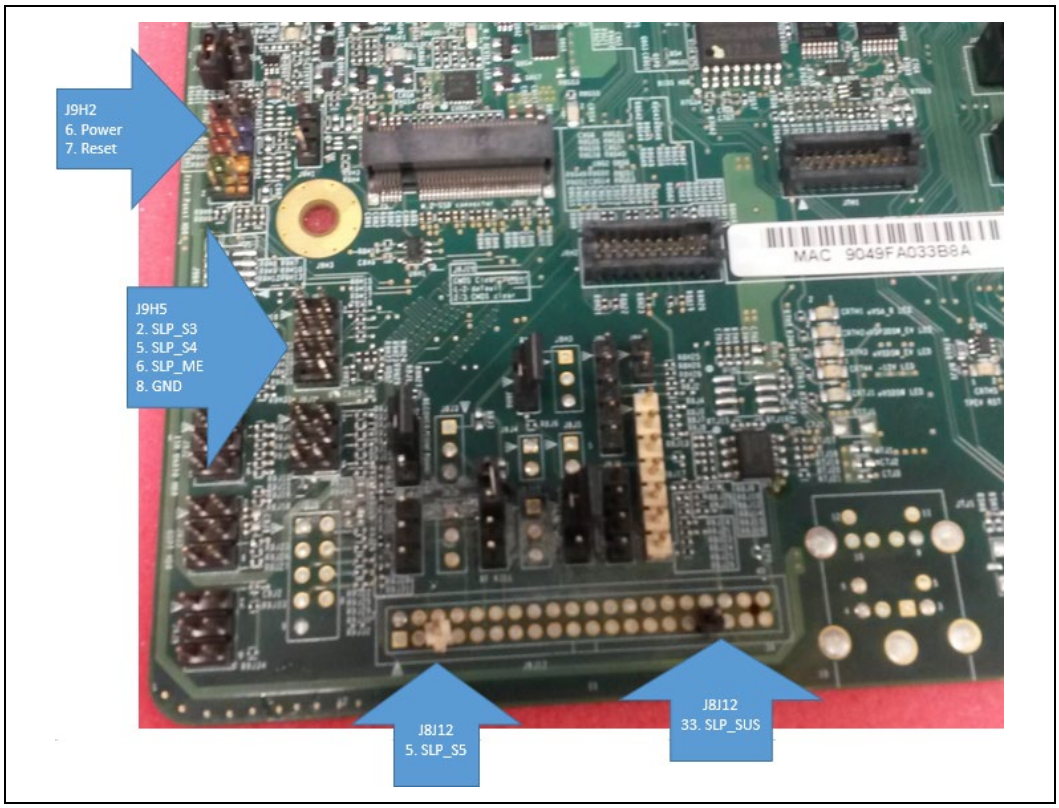
Figure 67. CFL-S platform with CLR CMOS, RTC, Power and Reset Relays Connected



K.3 Connecting Signal Sampling Cables to Coffee Lake-S Platform

Connect **SUS** cable to J8J12 pin 33, **S5** cable to j8j12 pin 5.
Connect **S3** cable to J9H5 pin 2,**S4** cable to J9H5 pin 5, **SLP_ME** cable to J9H5 pin 6, and **GND** to J9H5 pin 8.

Figure 68. CFL-S Connection for the Signal Sampling Cables and Power and Reset Button Relays

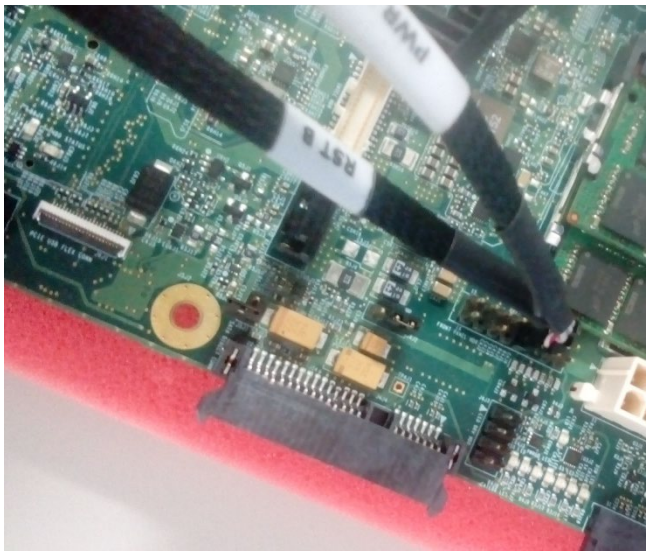


The following configuration is for CFL-H/U platforms. The user must configure APS-SW settings and choose "CofeeLake - Mobile" platform.

K.4 Connecting the Power and Reset Buttons on Coffee Lake-H platforms

Connect the power button and reset button to J4J1 on the front panel header. 5-7 for reset and 6-8 for power.

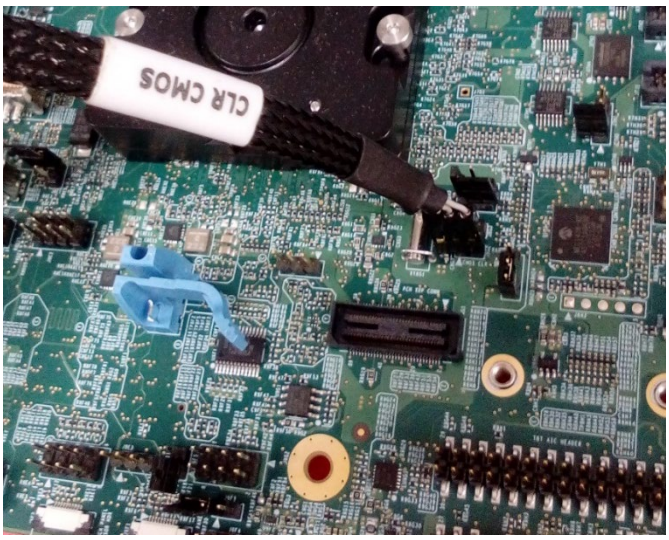
Figure 69. CFL-H power and Reset Button Relays Connected



K.5 Connecting Clear CMOS and RTC on Coffee Lake-H platforms

Connect the CMOS and RTC relays from Intel® APS to the connector as seen below. Short pins 2 and 3 on J8G1 for Clear CMOS, and short pins 1 and 2 on J8G1 for RTC Clear.

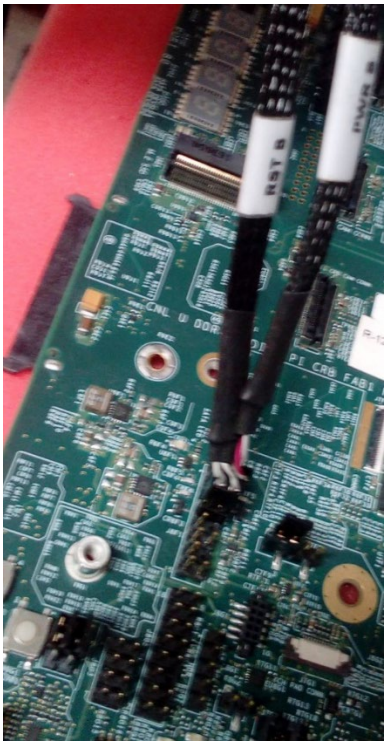
Figure 70. CFL-H Platform with CMOS Relay Connected



K.6 Connecting the Power and Reset Buttons on Coffee Lake-U platforms

Connect the power button and reset button relays to J8F1 on the front panel header.

Figure 71. CFL-U Power and Reset Button Relays Connected

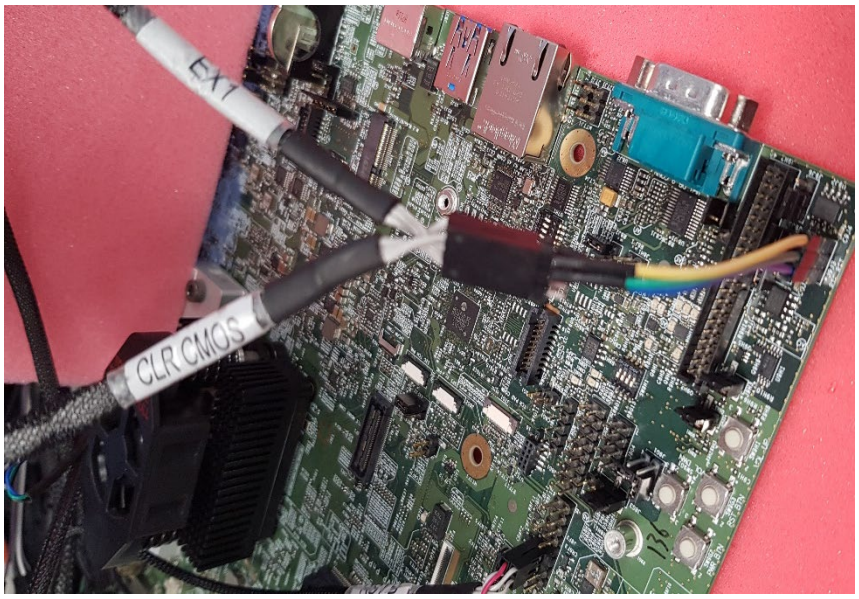


K.7 Connecting Clear CMOS and RTC on Coffee Lake-U Platforms

Connect Clear CMOS and RTC to J9J3 connector.

Note: The user needs an additional adaptor seen in FIGURE 64.

Figure 72.CFL-U Platform with Clear CMOS and RTC Relays Connected



K.8 Connecting Signal Sampling Cables to Coffee Lake H/U Platforms

Connect the SML1 card seen in Figure 57 on the LPC side band header.

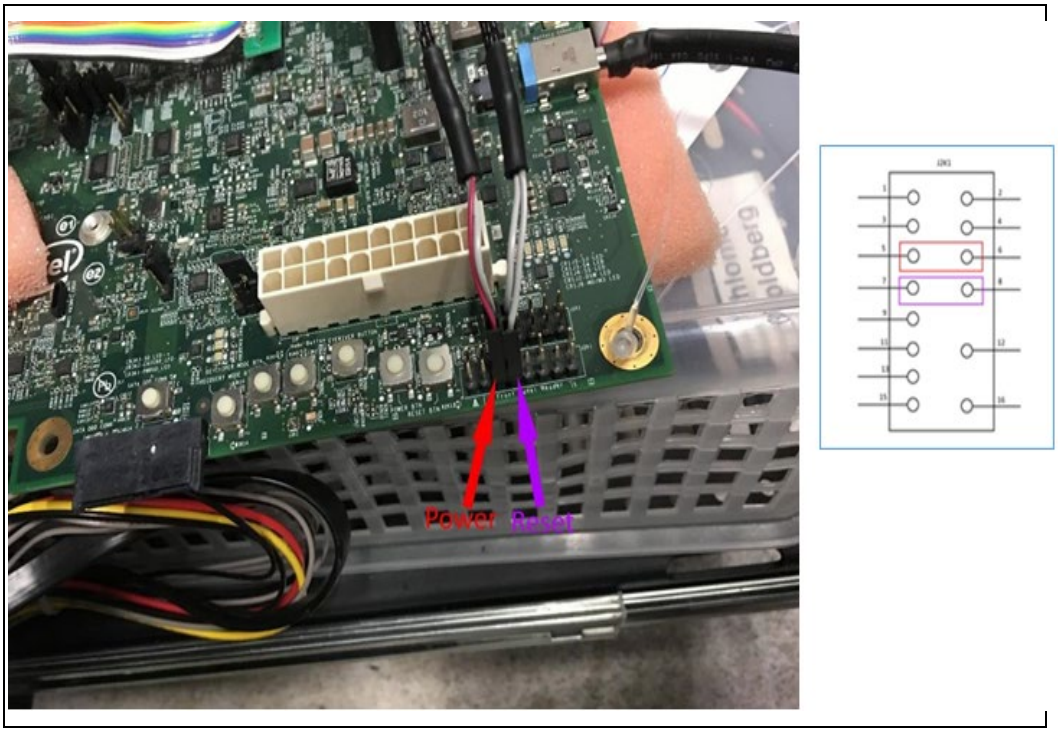
Appendix L Connecting Intel® APS to Kaby Lake Platforms

The following configuration is for KBL RVP3 and KBL RVP7 platforms. The user must configure APS-SW settings to "KabyLake-Mobile".

L.1 Connecting the Power and Reset buttons on Kaby Lake RVP3/7

Connect the **power-button** and **reset-button** relays to the connector J2K1 as seen below.

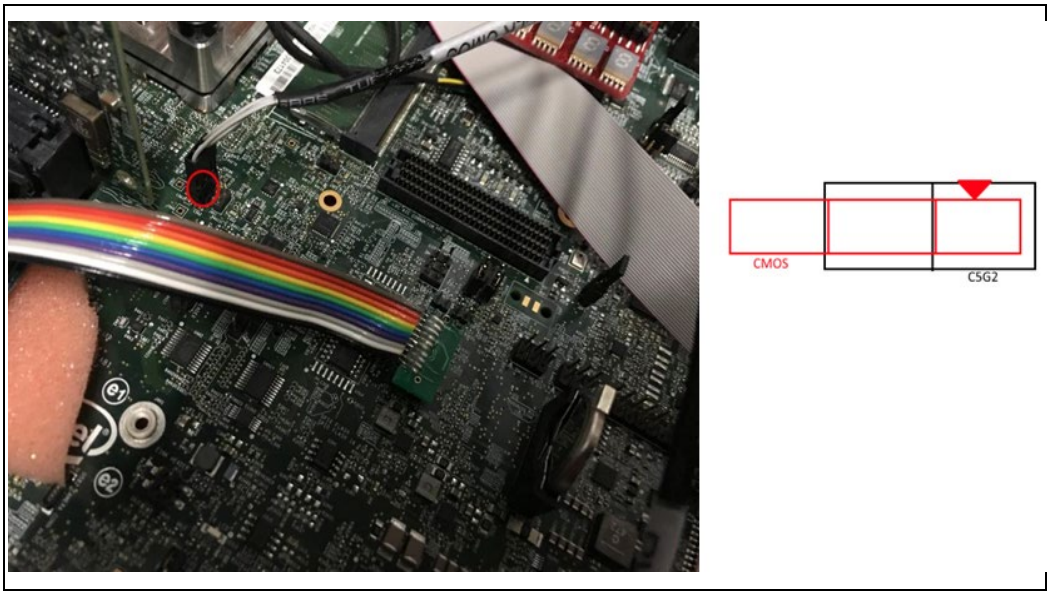
Figure 73. Kaby Lake platform with Power and Reset Relays Connected



L.2 Connecting to Clear CMOS on Kaby Lake RVP3/7

Connect the CMOS relay from Intel® APS to the connector C5G2 as seen below:

Figure 74. Kaby Lake Platform with CMOS Relay Connected



L.3 Connecting Signal Sampling Cables to Kaby Lake RVP3/7

To connect signal sampling cables, use the SML1 card (seen in Figure 57) on the LPC side band header.

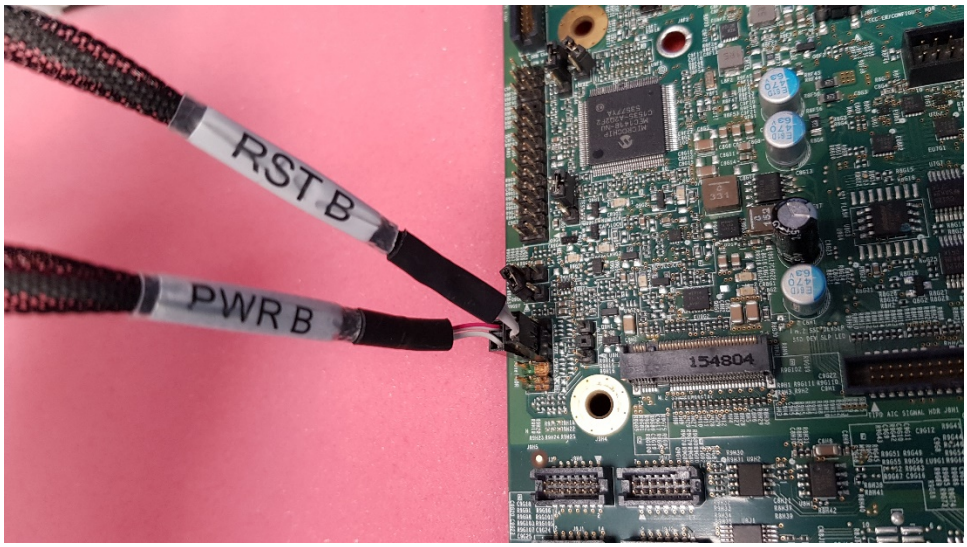
The following configuration is for KBL-S platforms. The user must configure APS-SW settings to “KabyLake-Desktop”.

L.4 Connecting the Power and Reset buttons on Kaby Lake-S platforms

Connect the power button to pins 6-8 of J9H6 on the front panel header.

Connect the reset button relay to pins 5-7 of J9H6 on the front panel header.

Figure 75. KBL-S with power and Reset Buttons Relay Connected

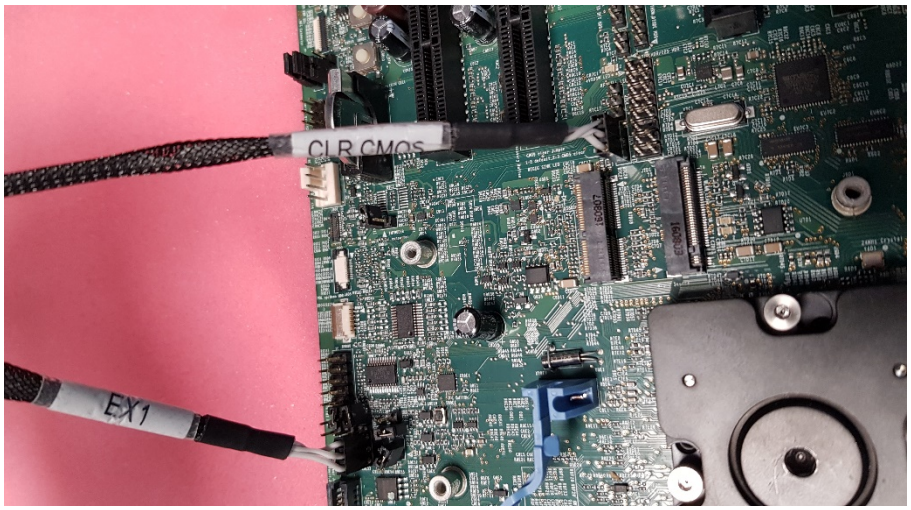


L.5 Connecting Clear CMOS and RTC to Kaby Lake-S Platforms

See the picture below for connecting CLR CMOS and RTC on KBL-S. Please note that Intel® APS does not have a cable for RTC CLR, EX1 cable can be used for that purpose after modifying the cable signal settings.

- Short pins 2-3 on J7D1 for CLR CMOS
- Short pins 2-3 on J9E7 for CLR RTC

Figure 76. KBL-S with CLR CMOS and RTC Connected



L.6 Connecting Signal Sampling Cables to KabyLake-S Platforms

- Connect **S3** cable to pin 2 on J8J1,**S4** cable to pin 5 on J8J1,**SLP_M** cable to pin 6 on J8J1, and **GND** cable to pin 8 on J8J1.
- Connect **SLP_5** cable to pin 7 on J9E2
- Rework required to connect **SUS** Cable.

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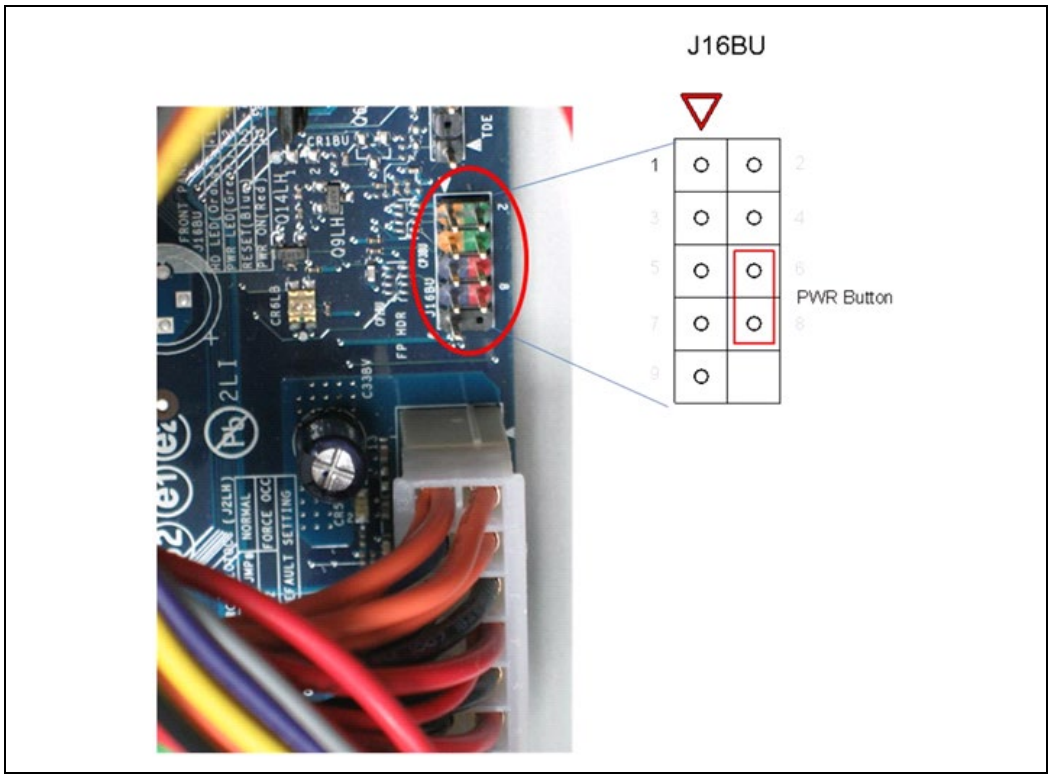
Appendix M Connecting to Intel® 5 Series Express Chipset [formerly Ibex Peak] CRBs

This section explains how to connect the Intel® APS to desktop and mobile Ibex Peak CRBs and includes photographs to facilitate connection.

M.1 Connecting to Power Button on Piketon (Ibex Peak Desktop) CRB

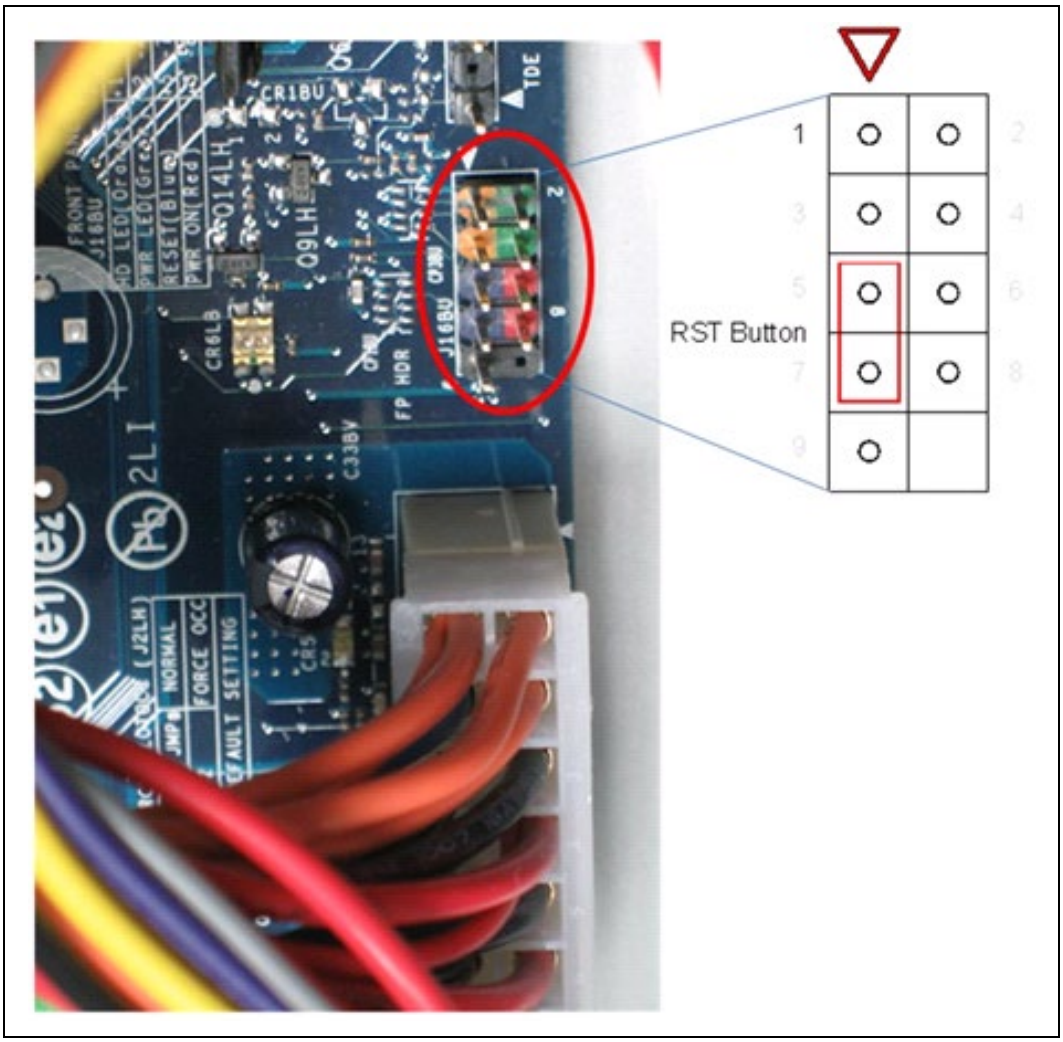
Connect the PWR B cable (Main 1-2) to the Piketon's power button header on the motherboard (FP On/Off Power Header J16BU).



M.2 Connecting to Reset Button on Piketon (Ibex Peak Desktop) CRB

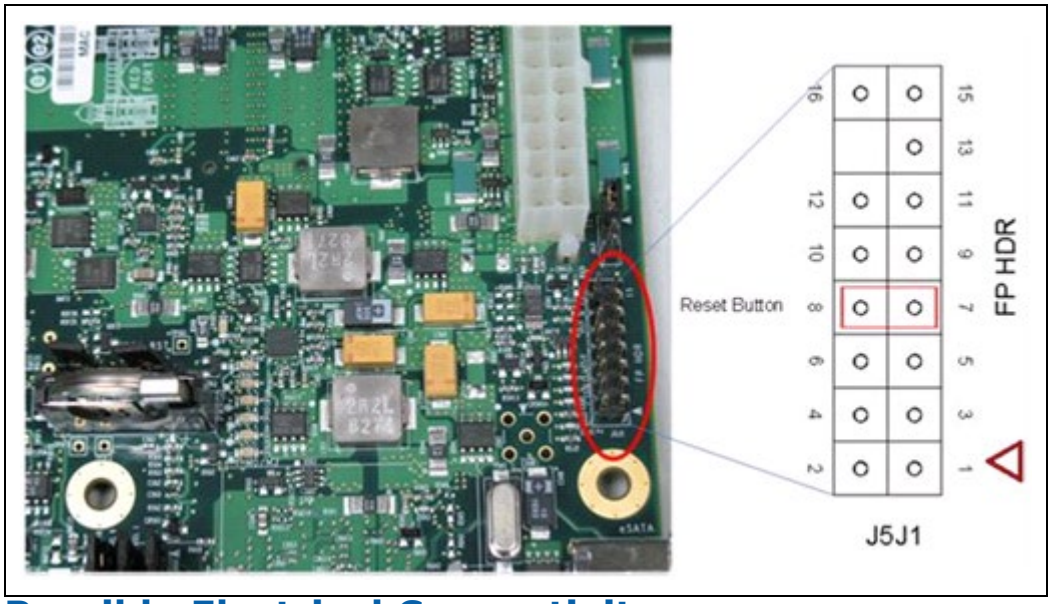
1. Connect the main cable to the Main socket on the Intel® APS front panel.

2. Connect the RST B cable (Main 5-6) to the Piketon's Reset header on the motherboard (FP Reset Power Header J16BU).



M.3 Connecting to Calpella (Ibex Peak Mobile) CRB's Reset Button

Connect the Intel® APS RST B cable (Main Pin 5-6) to the mobile CRB's Reset FP HDR header on the motherboard (FP Reset Power Header J5J1).

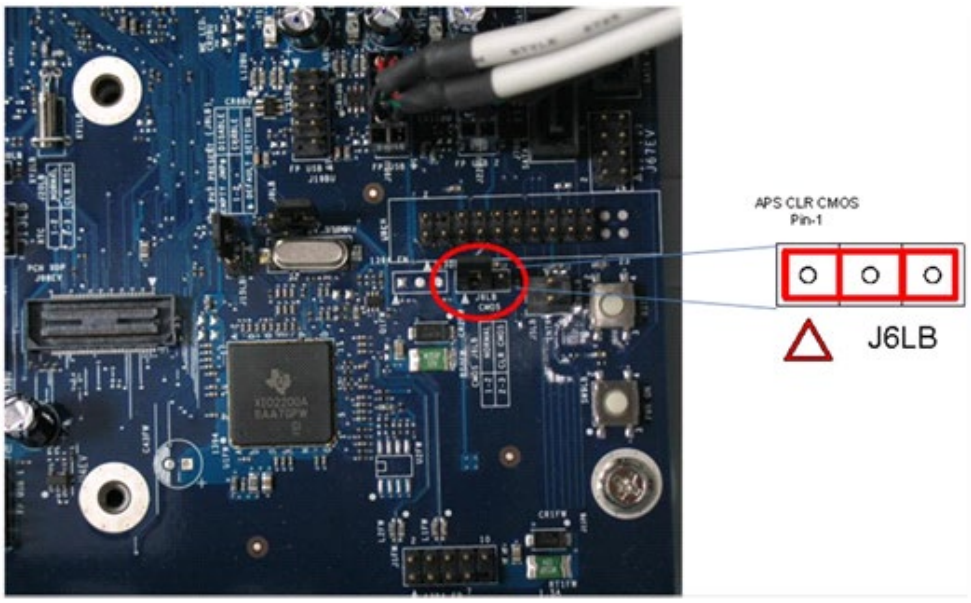


M.3.1 Possible Electrical Connectivity

- Intel® APS connects Pin 1 to Pin 2
- Intel® APS disconnects Pin 1 from Pin 2

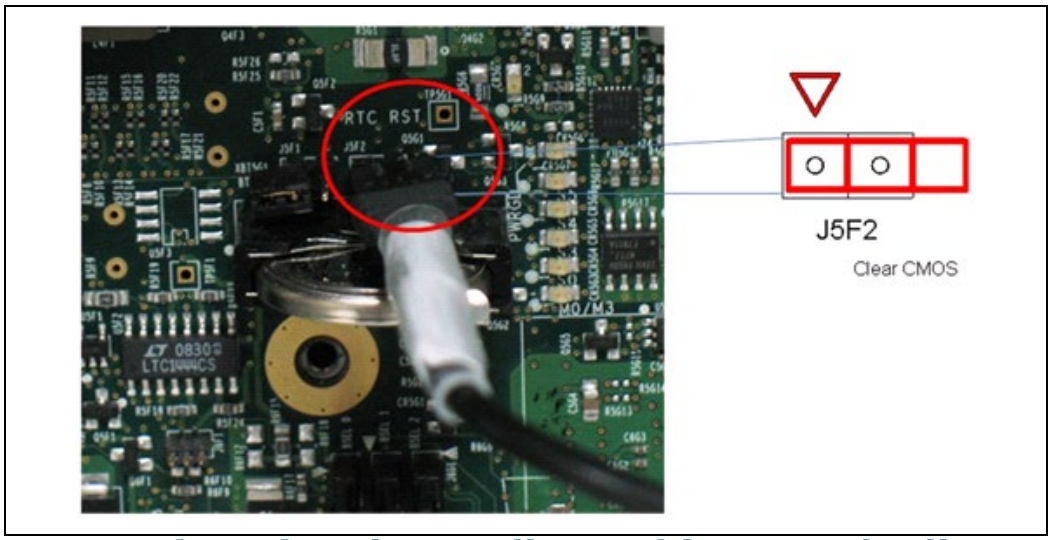
M.3.2 Connecting to Clear CMOS on an Piketon (Ibex Peak Desktop) CRB

Connect the CLR CMOS cable (Main 9-11) to the J6LB header on the Piketon.



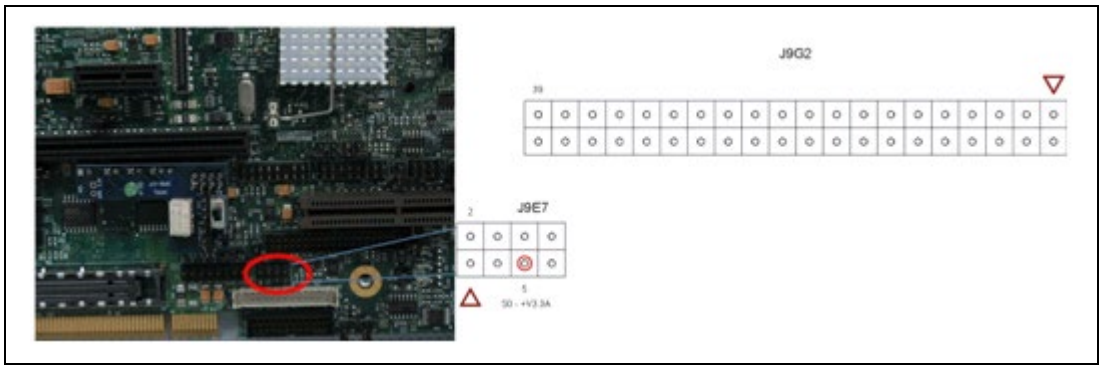
M.3.3 Connecting to Clear CMOS on Calpella (Ibex Peak Mobile) CRB

Connect the Intel® APS CLR CMOS cable (Main Pin 9-11) to the Calpella's CLR CMOS Header on the motherboard (FP Reset Power Header J5J1). Make sure you connect pins 1 and 2 of the cable.



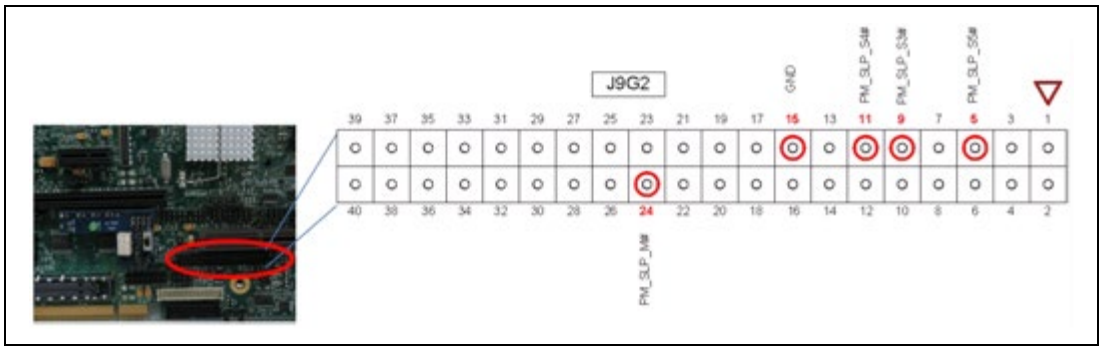
M.3.4 Connecting Signal Sampling Cables to Calpella (Ibex Peak Mobile) CRB

1. Connect the **Vcc_Sus** (Main Pin 33) wire to pin 5 on header J9E7.



2. Connect the **M1/OFF** (Main Pin 37) wire to pin 24 on header J9G2

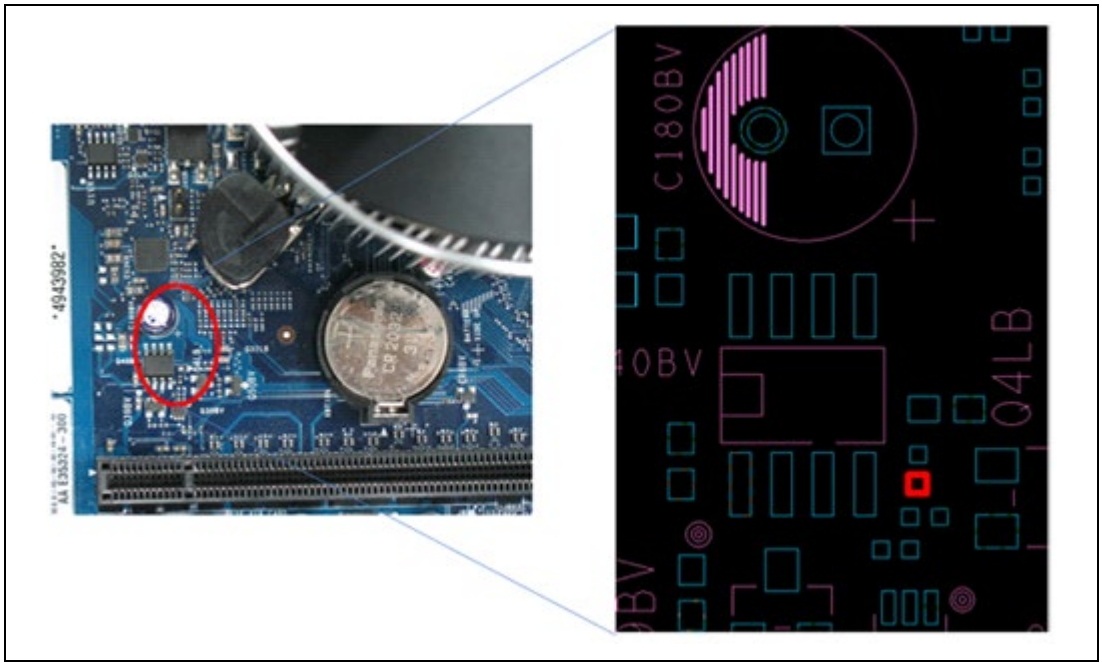
3. Connect the **GND** (Main Pin 38) wire to pin 15 on header J9G2
4. Connect the **S3** (Main Pin 34) wire to pin 9 on header J9G2
5. Connect the **S4** (Main Pin 35) wire to pin 11 on header J9G2
6. Connect the **S5** (Main Pin 36) wire to pin 5 on header J9G2



Note: For 1.5MB SKUs which do not implement the SLP_A, the SLP_A connection from the Intel® APS should be connected to the same point as the SLP_S3 connection.

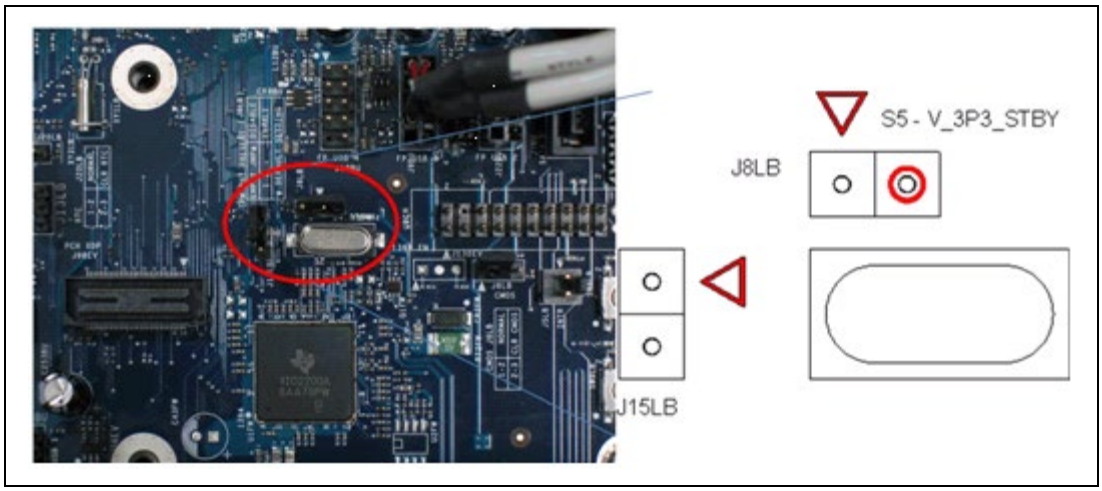
M.3.5 Connecting Signal Sampling Cables to Piketon (Ibex Peak Desktop) CRB

1. Solder the **M1/OFF** (Main Pin 37) wire to R98LB.2.

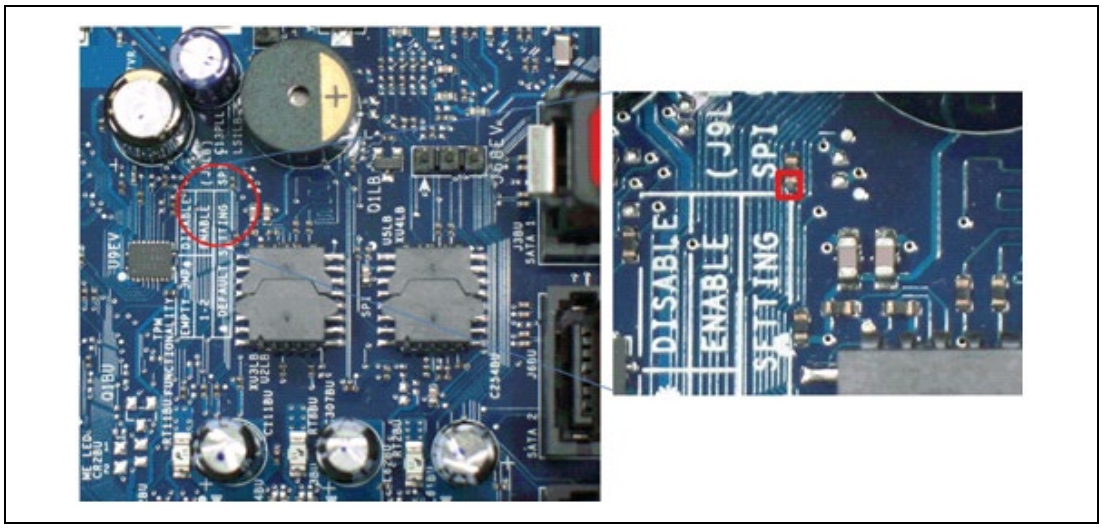


Note: For 1.5MB SKUs which do not implement the SLP_A, the SLP_A connection from the Intel® APS should be connected to the same point as the SLP_S3 connection.

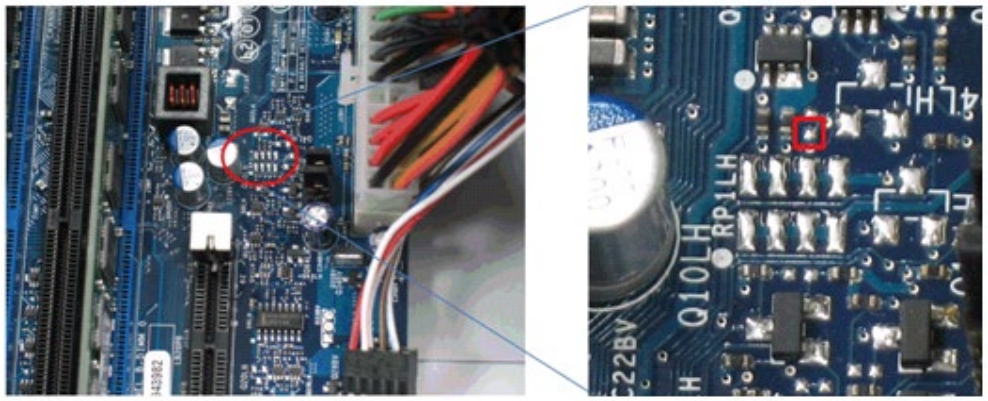
2. Connect the **S5** (Main Pin 36) wire to pin 1 on header J8LB.



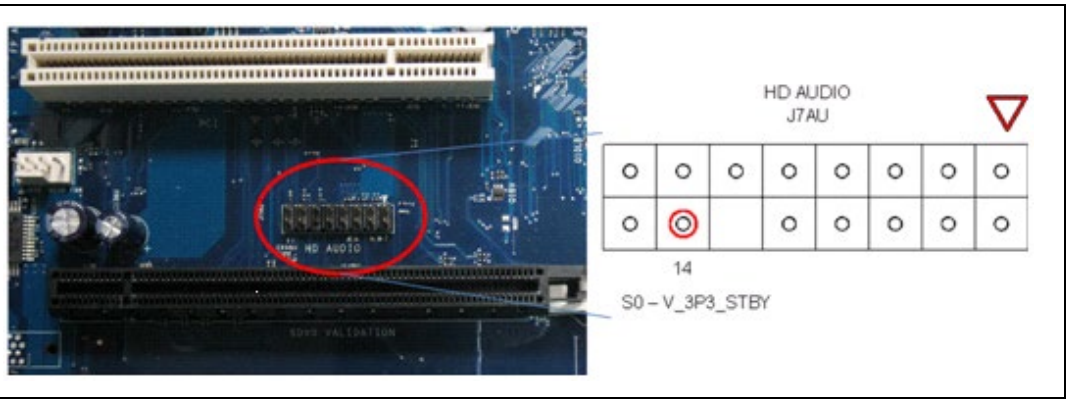
3. Solder the **S3** (Main Pin 34) wire to R11LB.1.



4. Solder the **S4** (Main Pin 35) wire to R65LH.1.



5. Connect the **Vcc_Sus** (Main Pin 33) wire to pin 14 on header J7AU.



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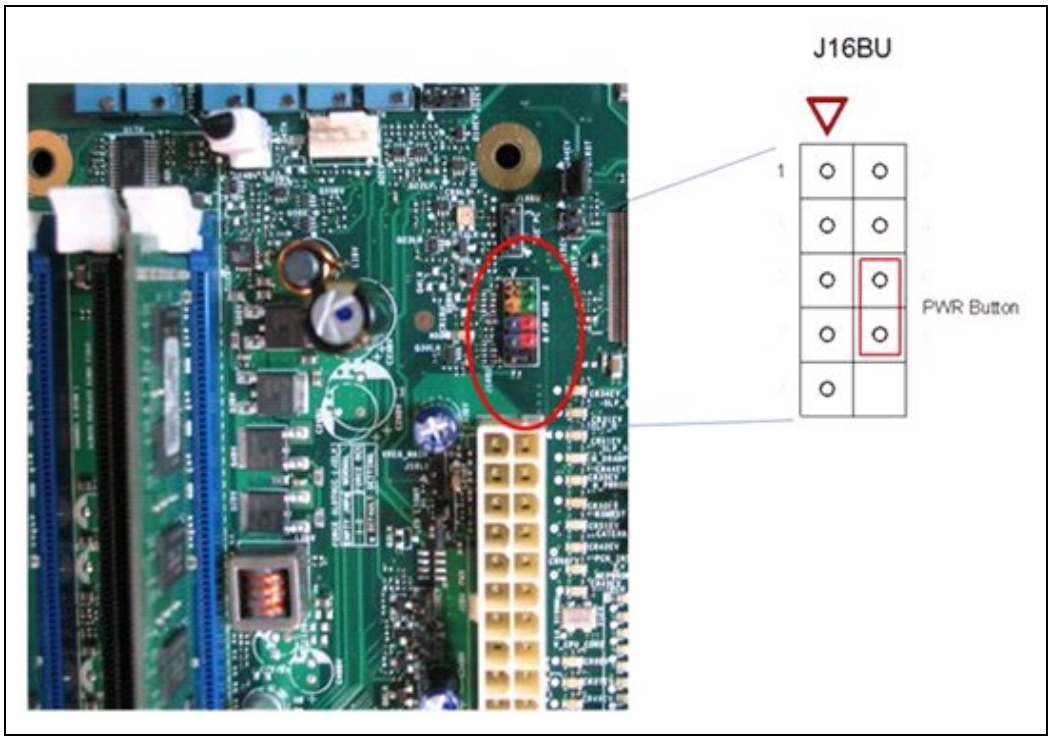
Appendix N Connecting to Intel® 6 Series Express Chipset [formerly Cougar Point] CRBs

This section explains how to connect the Intel® APS to Cougar Point desktop and mobile CRBs and includes photographs to facilitate connection.

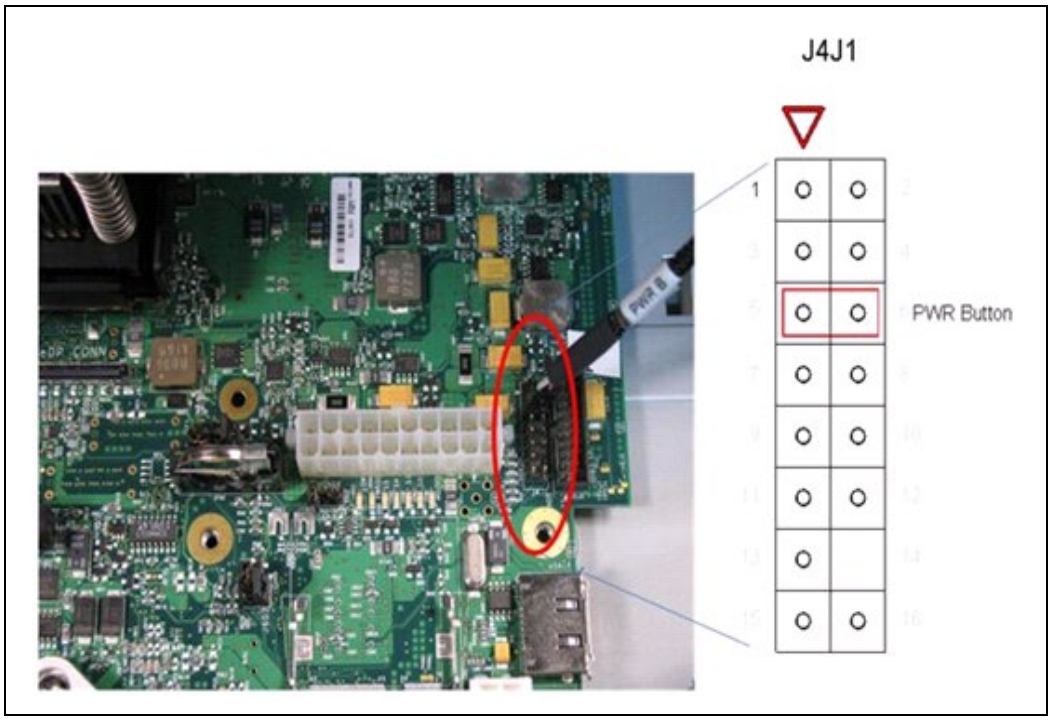
N.1 Connecting to SUT Power Button on a Sugar Bay (Cougar Point Desktop) CRB

Connect the Power button cable to J16BU pins 6-8.



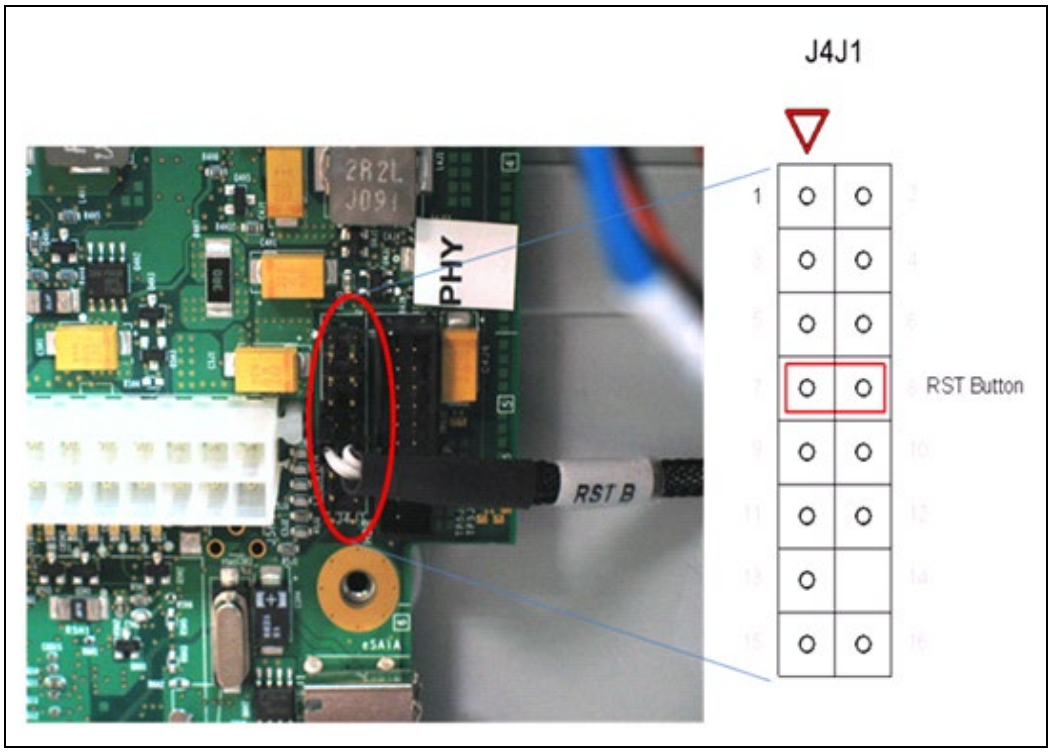
N.2 Intel® APS to SUT Power Button on a Huron River (Cougar Point Mobile) CRB

Connect the Power button cable to J4J1, pins 5-6.



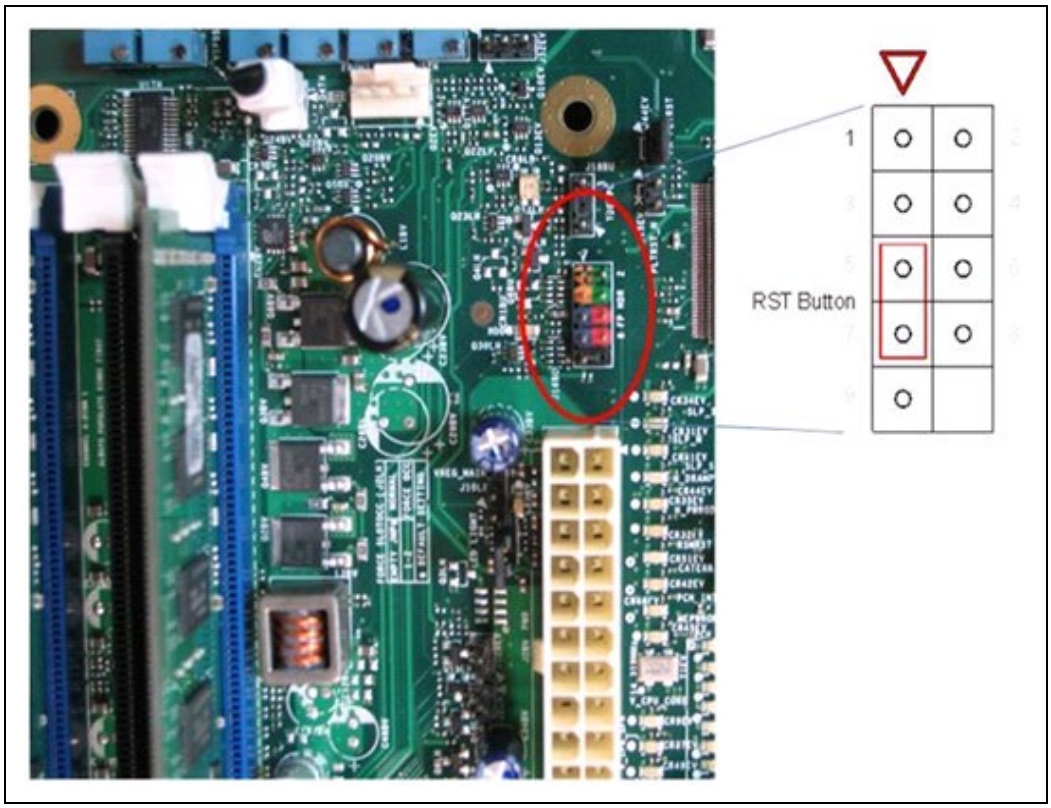
N.3 Connecting to Reset Button on a Huron River (Cougar Point Mobile) CRB

Connect the Reset cable to J4J1 pins 7-8.



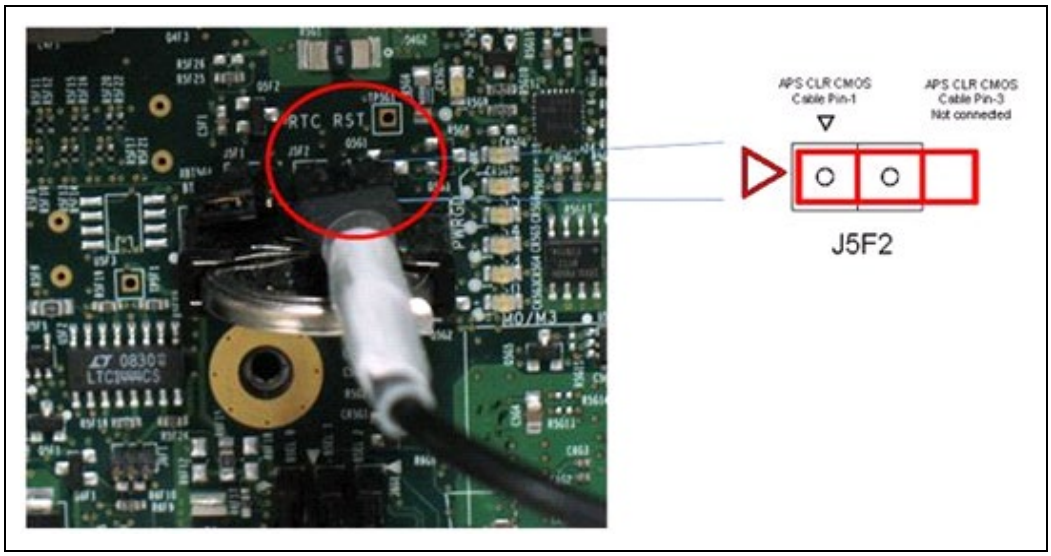
N.4 Connecting to Reset Button on a Sugar Bay (Cougar Point Desktop) CRB

Connect the Reset cable to J16BU pins 5-7.



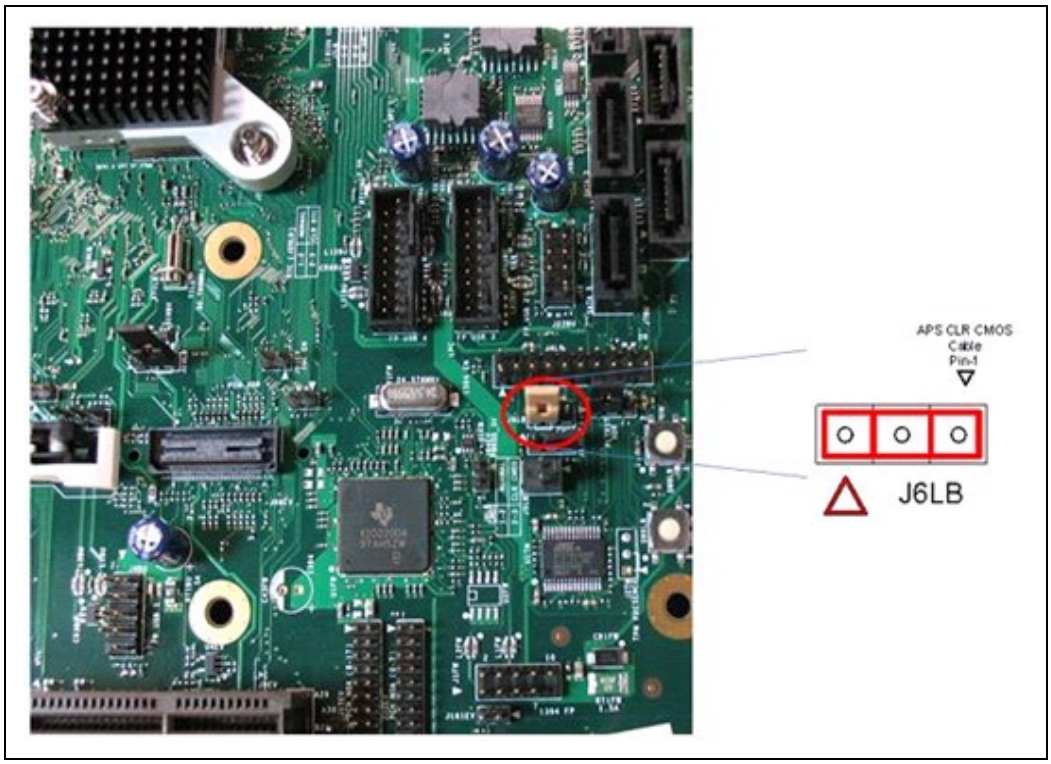
N.5 Connecting to Clear CMOS on a Huron River (Cougar Point Mobile) CRB

Connect the Clear CMOS cable to J5F2, pins 1-2.



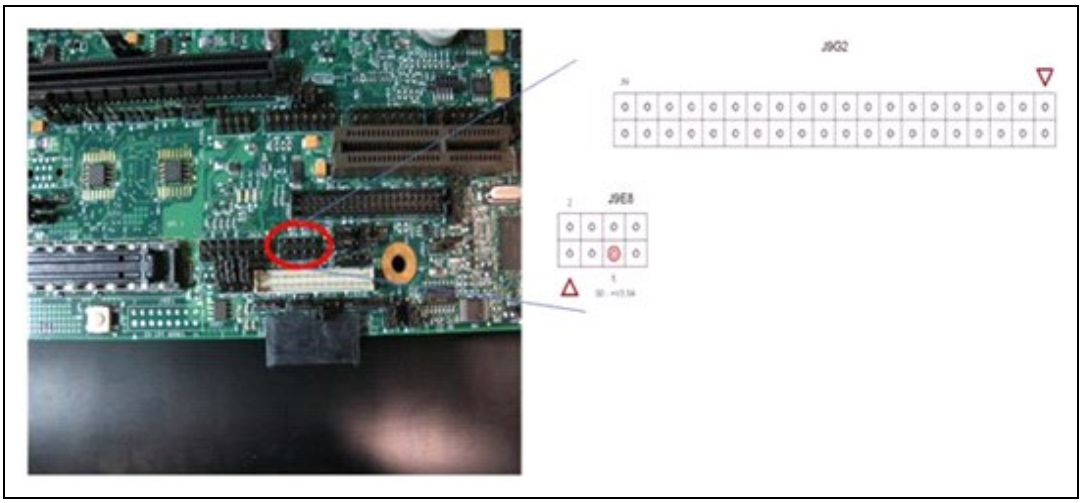
N.6 Intel® APS to Clear CMOS on a Sugar Bay (Cougar Point Desktop) CRB

Connect the Clear CMOS cable to J6LB.

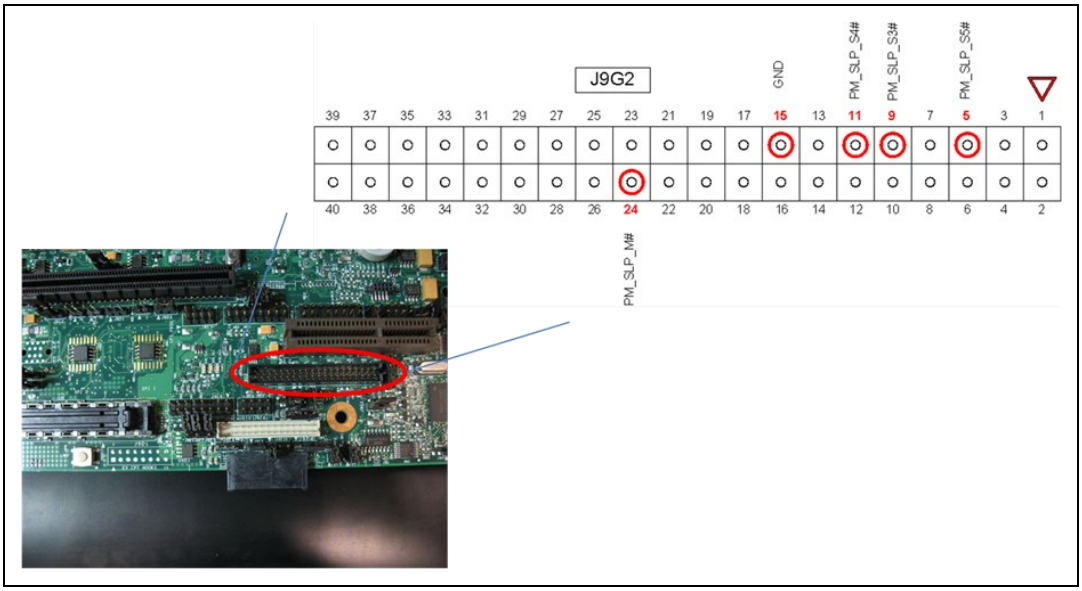


N.7 Connecting Signal Sampling Cables to Huron River Mobile CRB

Connect the **SUS** cable to J9E8 pin 5.

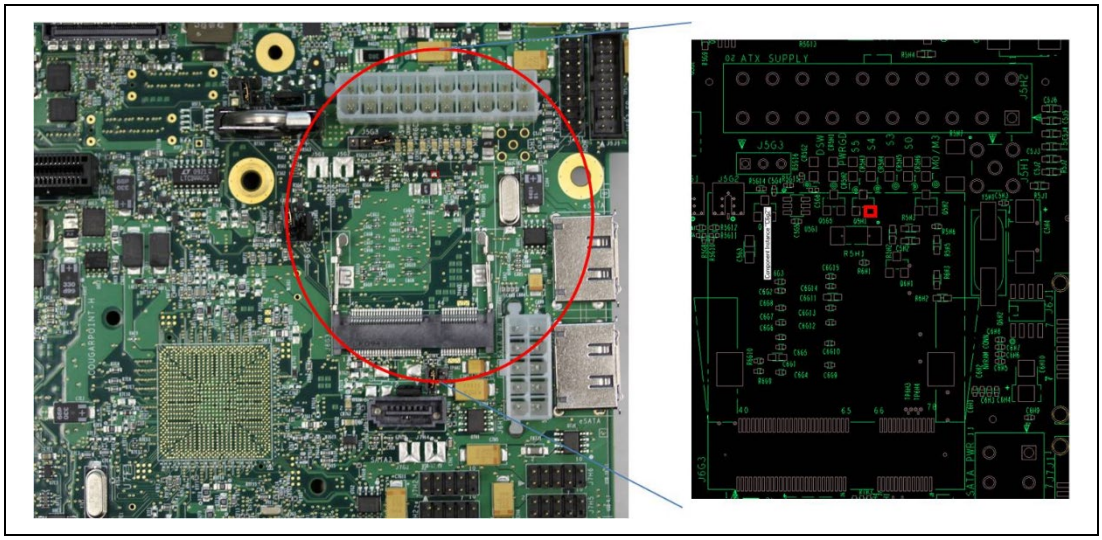


Connect the **GND** cable to J9G2 pin 15, **S4** cable to J9G2 pin 11, **S3** cable to J9G2 pin 9, **S5** cable to J9G2 pin 5, **M1/Off** cable to J9G2 pin 24.



Note: For 1.5MB SKUs which do not implement the SLP_A, the SLP_A connection from the APS should be connected to the same point as the SLP_S3 connection.

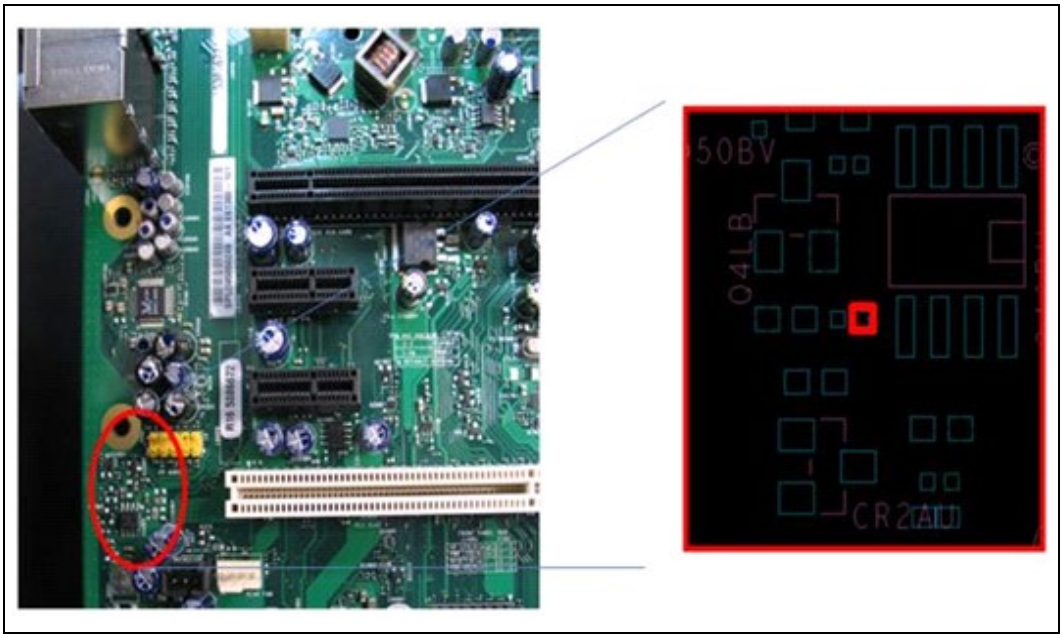
Connect the **INEX1(Deep S4/5)**cable to Q5H1 pin 2.



Note: If you do not connect this cable to the platform (because the connection point is missing from the platform, or for some other reason), make sure you connect it to GND. Note also that if this cable is not connected to Q5H1 pin 2, tests that depend on reading the Deep Sx states will fail.

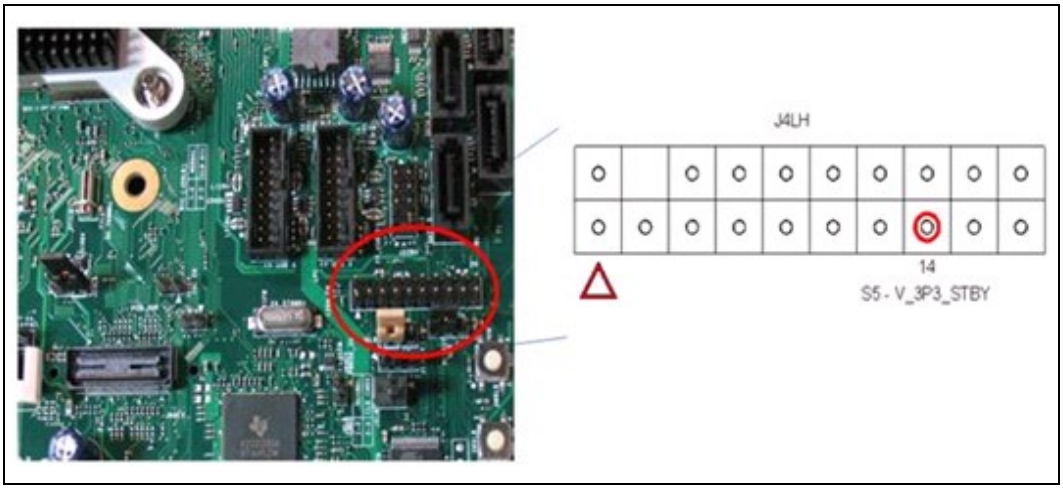
N.8 Connecting Signal Sampling Cables to Sugar Bay Desktop CRB

Connect the **M1/Off** cable to R98LB pin 2.

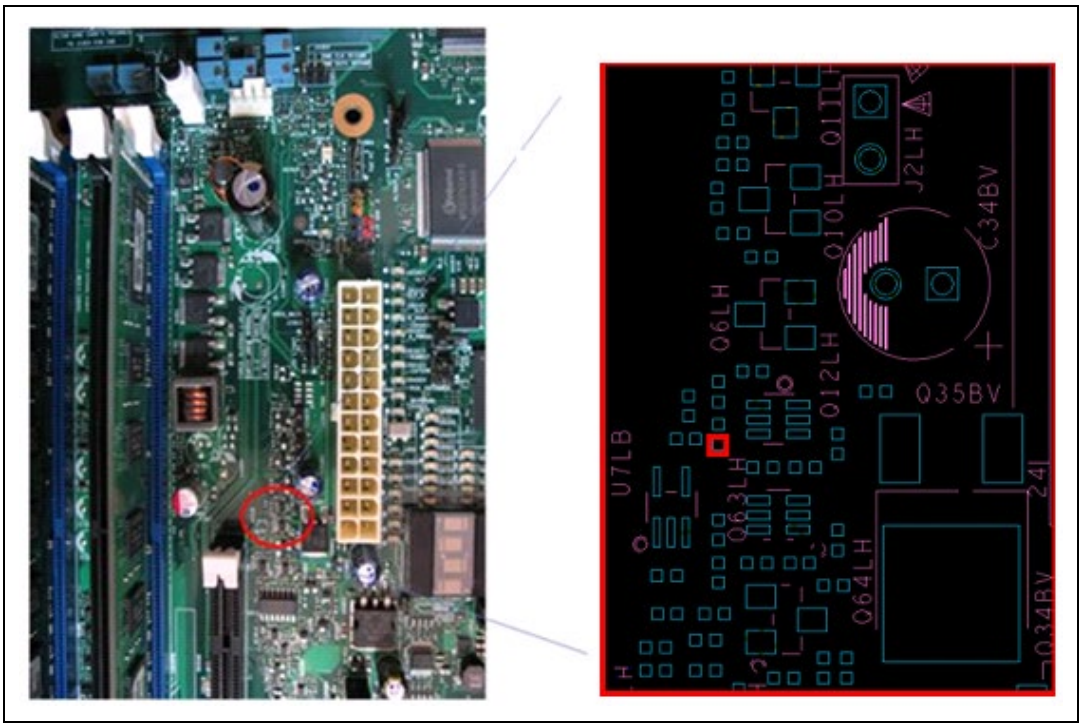


Note: For 1.5MB SKUs which do not implement the SLP_A, the SLP_A connection from the Intel® APS should be connected to the same point as the SLP_S3 connection.

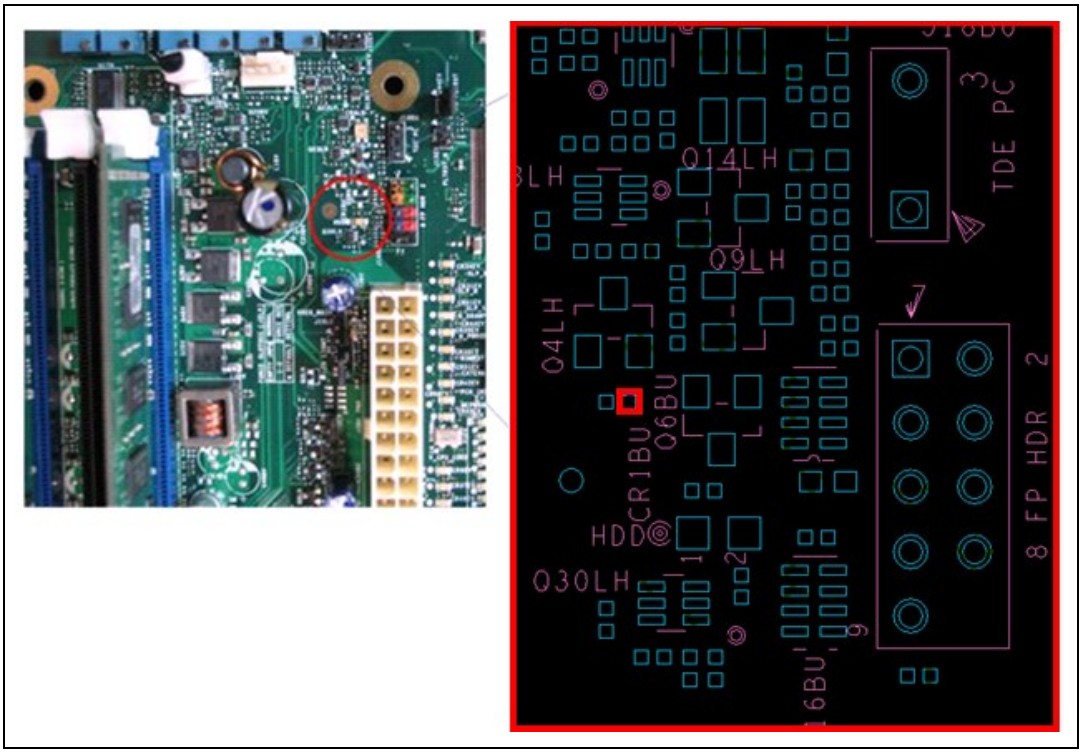
Connect the **S5** cable to J4LH pin 14.



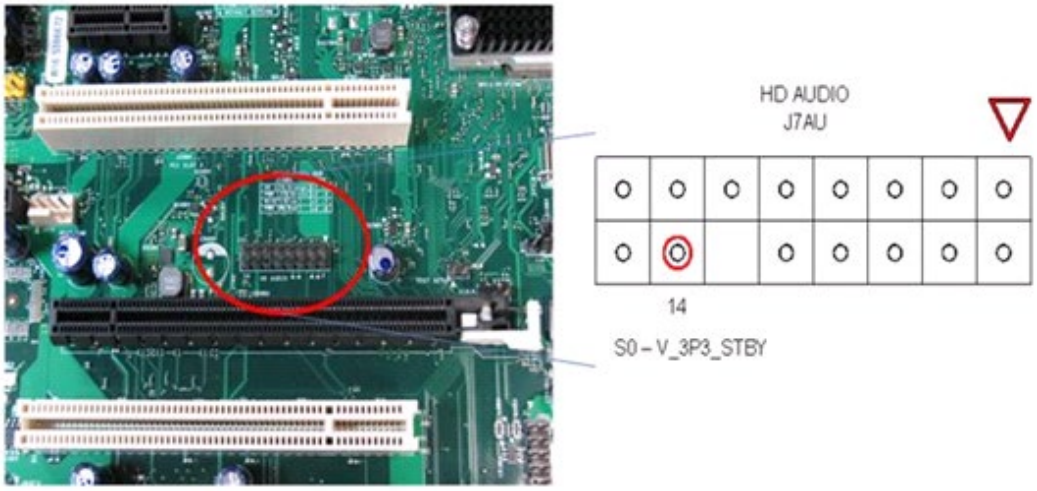
Connect the **S3** cable to R11LB pin 1.



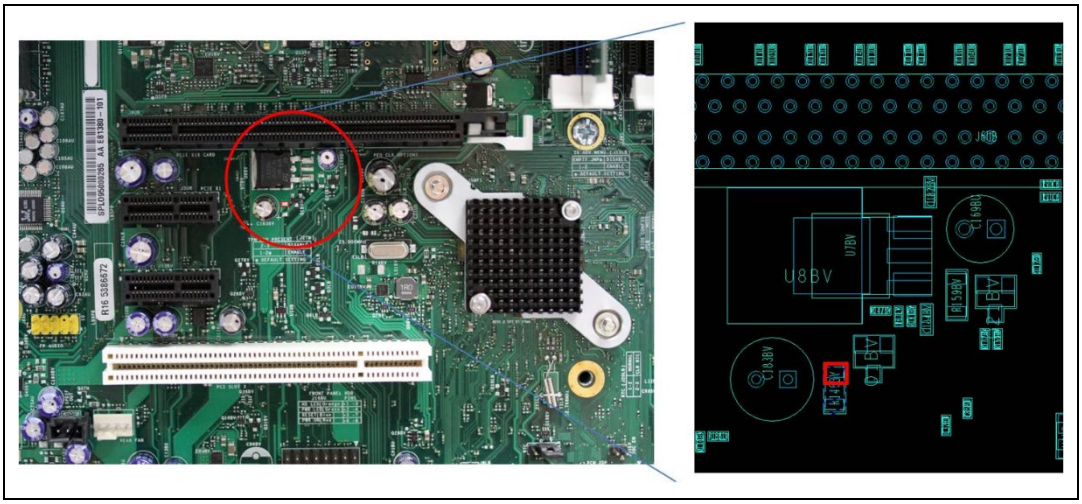
Connect the **S4** cable to R65LH pin 1.



Connect the **SUS** cable to J7AU pin 14.



Connect the **INEX1(Deep S4/5)** cable to R146BV pin 1. **Note:** If you do not connect this cable to the platform (because the connection point is missing from the platform, or for some other reason), make sure you connect it to GND. Note also that if this cable is not connected to R146BV pin 1, tests that depend on reading the Deep Sx states will fail.



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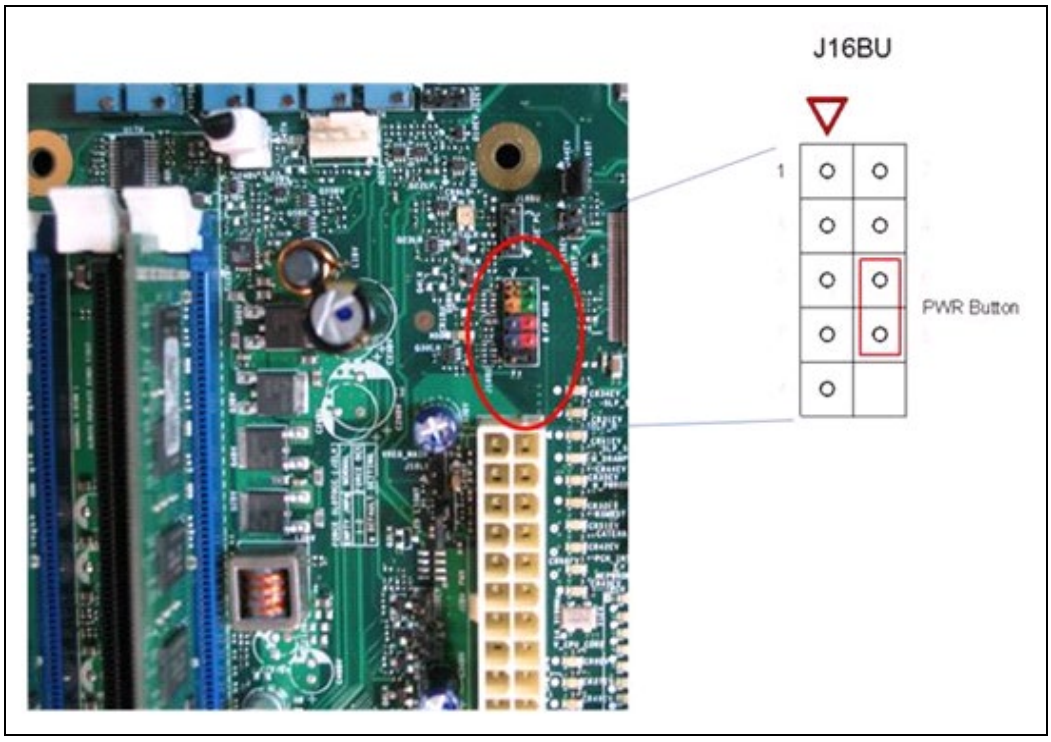
Appendix O Connecting to Intel® 7 Series Express Chipset [formerly Panther Point] CRBs

This section explains how to connect the Intel® APS to Panther Point desktop and mobile CRBs. It includes photographs to illustrate all connections.

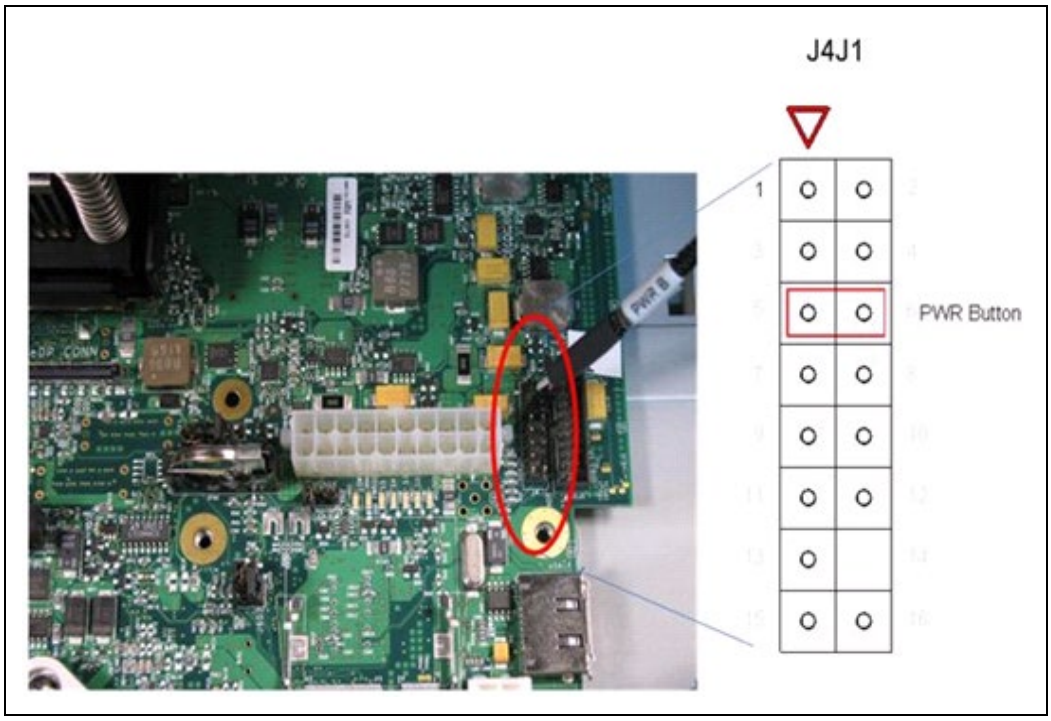
O.1 Connecting to SUT Power Button on a Maho Bay (Panther Point Desktop) CRB

Connect the Power button cable to J16BU pins 6-8.



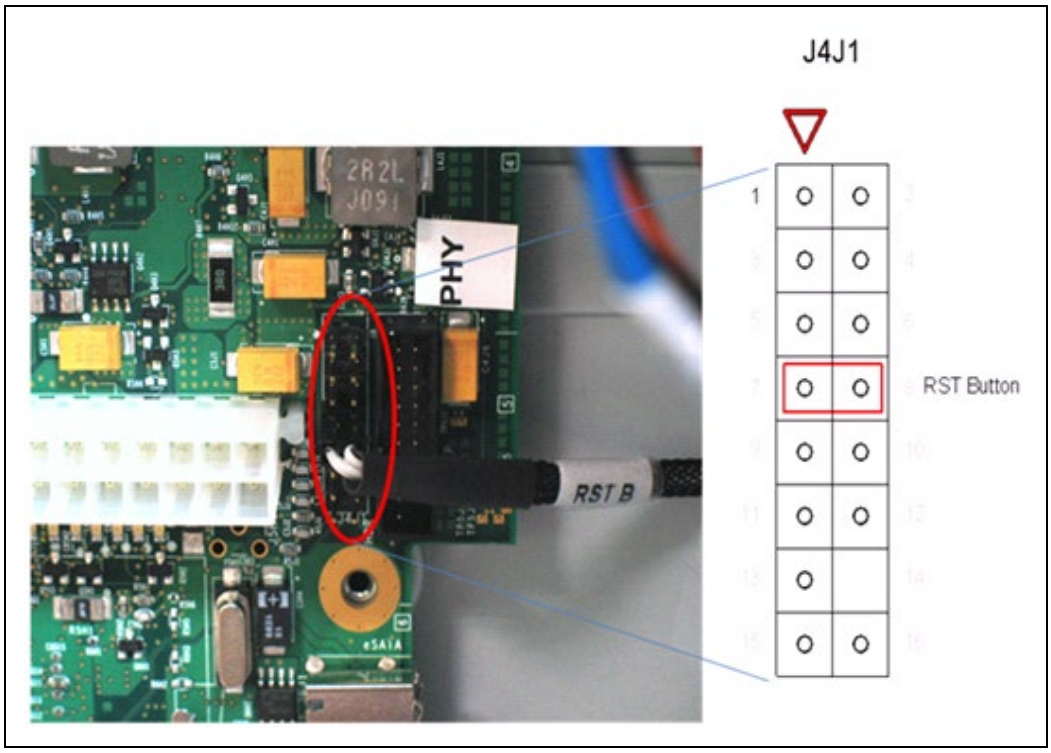
O.2 Intel® APS to SUT Power Button on a Chief River (Panther Point Mobile) CRB

Connect the Power button cable to J4J1, pins 5-6.



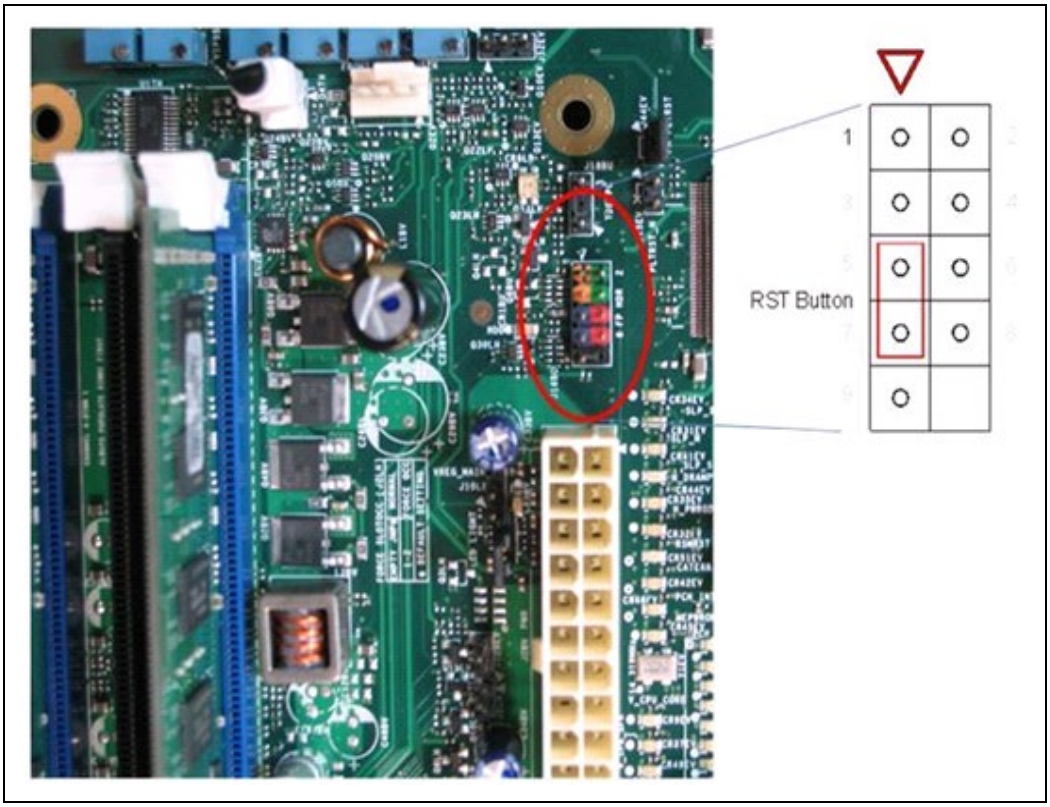
O.3 Connecting to Reset Button on a Chief River (Panther Point Mobile) CRB

Connect the Reset cable to J4J1 pins 7-8.



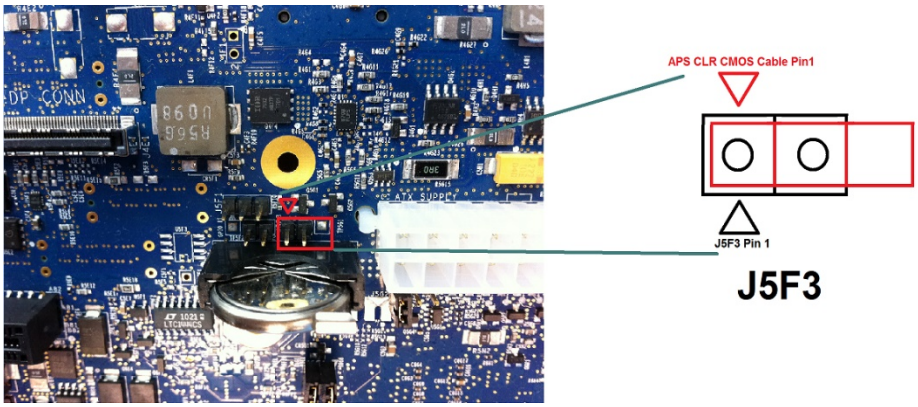
O.4 Connecting to Reset Button on a Maho Bay (Panther Point Desktop) CRB

Connect the Reset cable to J16BU pins 5-7.



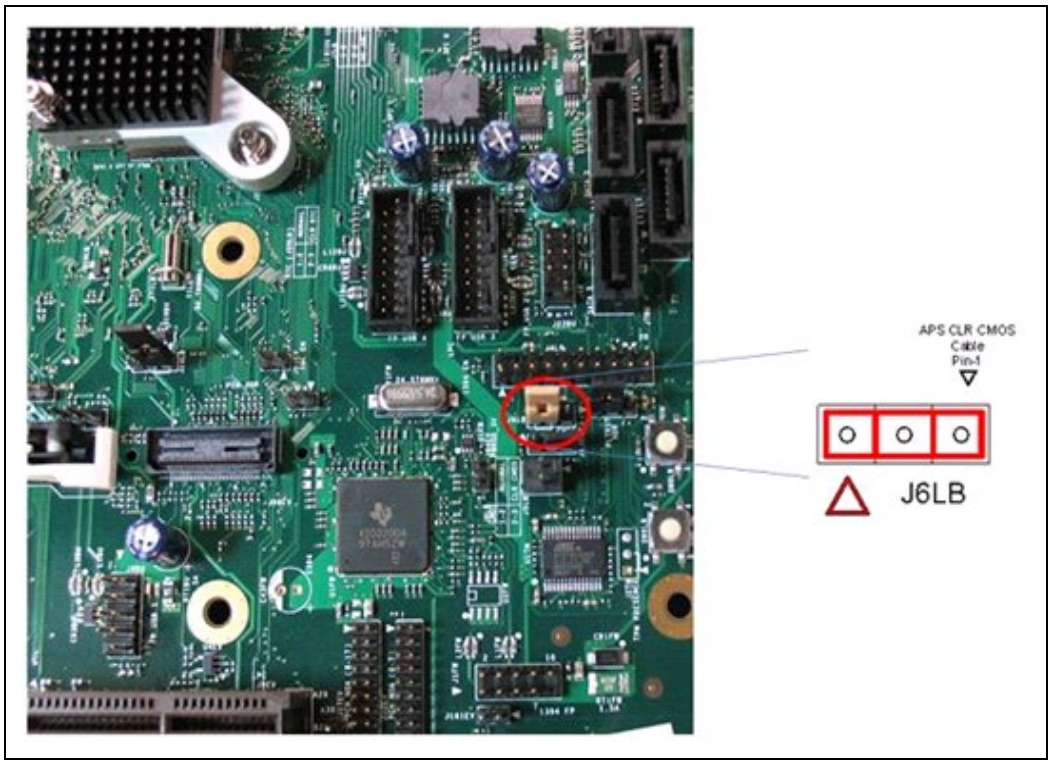
O.5 Connecting to Clear CMOS on a Chief River (Panther Point Mobile) CRB

Connect the Clear CMOS cable to J5F3, pins 1-2.



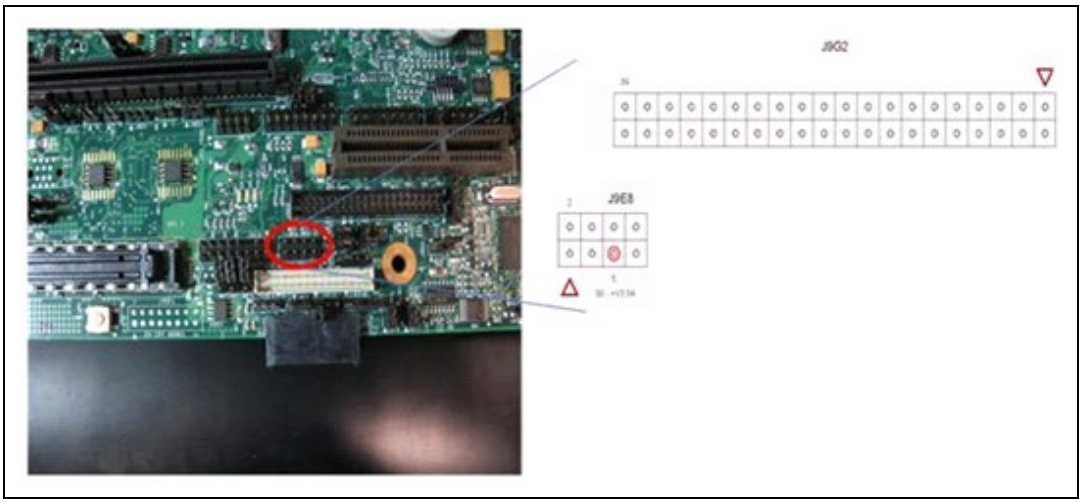
O.6 Intel® APS to Clear CMOS on a Maho Bay (Panther Point Desktop) CRB

Connect the Clear CMOS cable to J6LB.

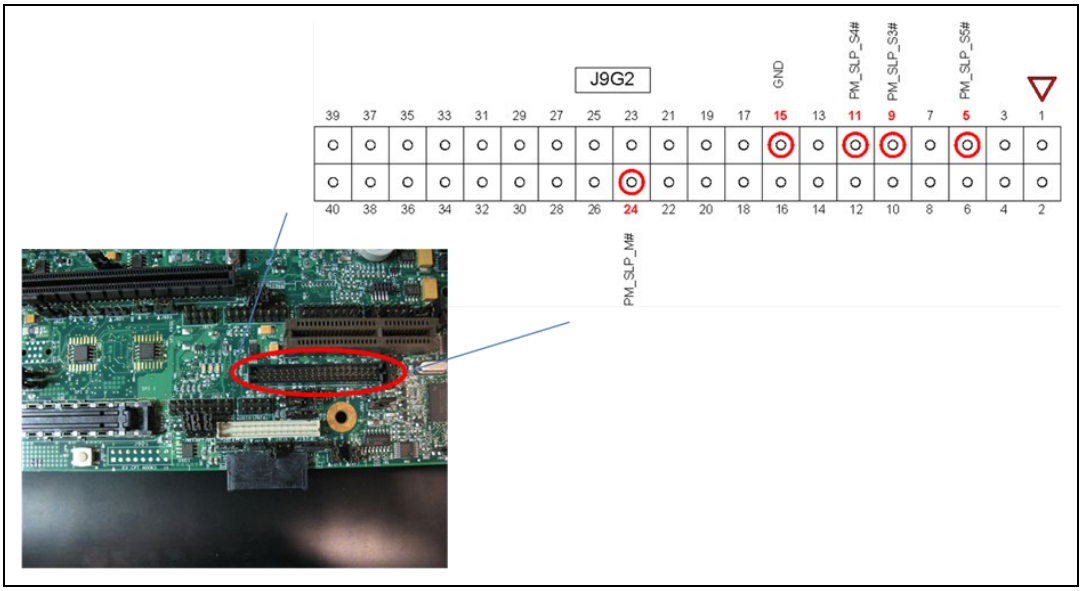


O.7 Connecting Signal Sampling Cables to Chief River Mobile CRB

Connect the **SUS** cable to J9E8 pin 5.

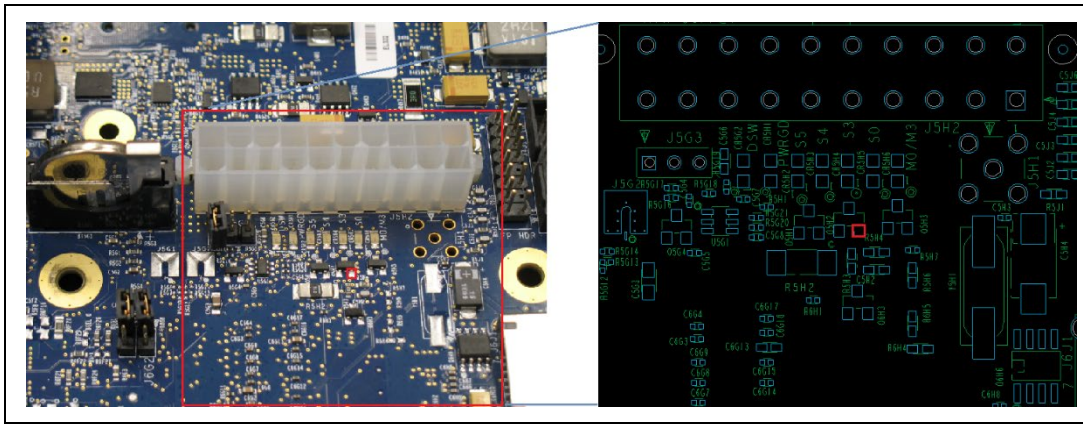


Connect the **GND** cable to J9G2 pin 15, **S4** cable to J9G2 pin 11, **S3** cable to J9G2 pin 9, **S5** cable to J9G2 pin 5, **M1/Off** cable to J9G2 pin 24.



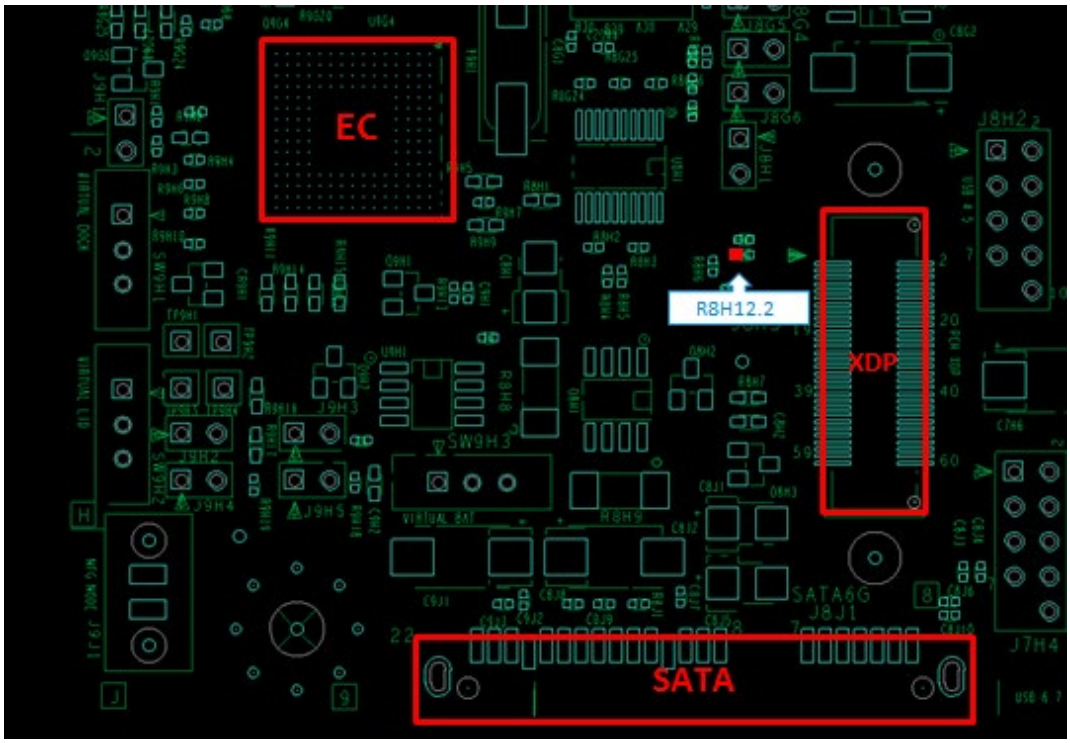
Note: For 1.5MB SKUs which do not implement the SLP_A, the SLP_A connection from the Intel® APS should be connected to the same point as the SLP_S3 connection.

Connect the **INEX1(Deep S4/5)**cable to Q5H2 pin 2.



Note: If you do not connect this cable to the platform (for example, because the connection point is missing from the platform, or for some other reason), make sure you connect it to GND. Note also that if this cable is not connected to Q5H2 pin 2, tests that depend on reading the Deep Sx states will fail.

Connect the INEX2 (Deep S3) cable to R8H12 pin 2 (Emerald Lake2 Fab2 platform only).

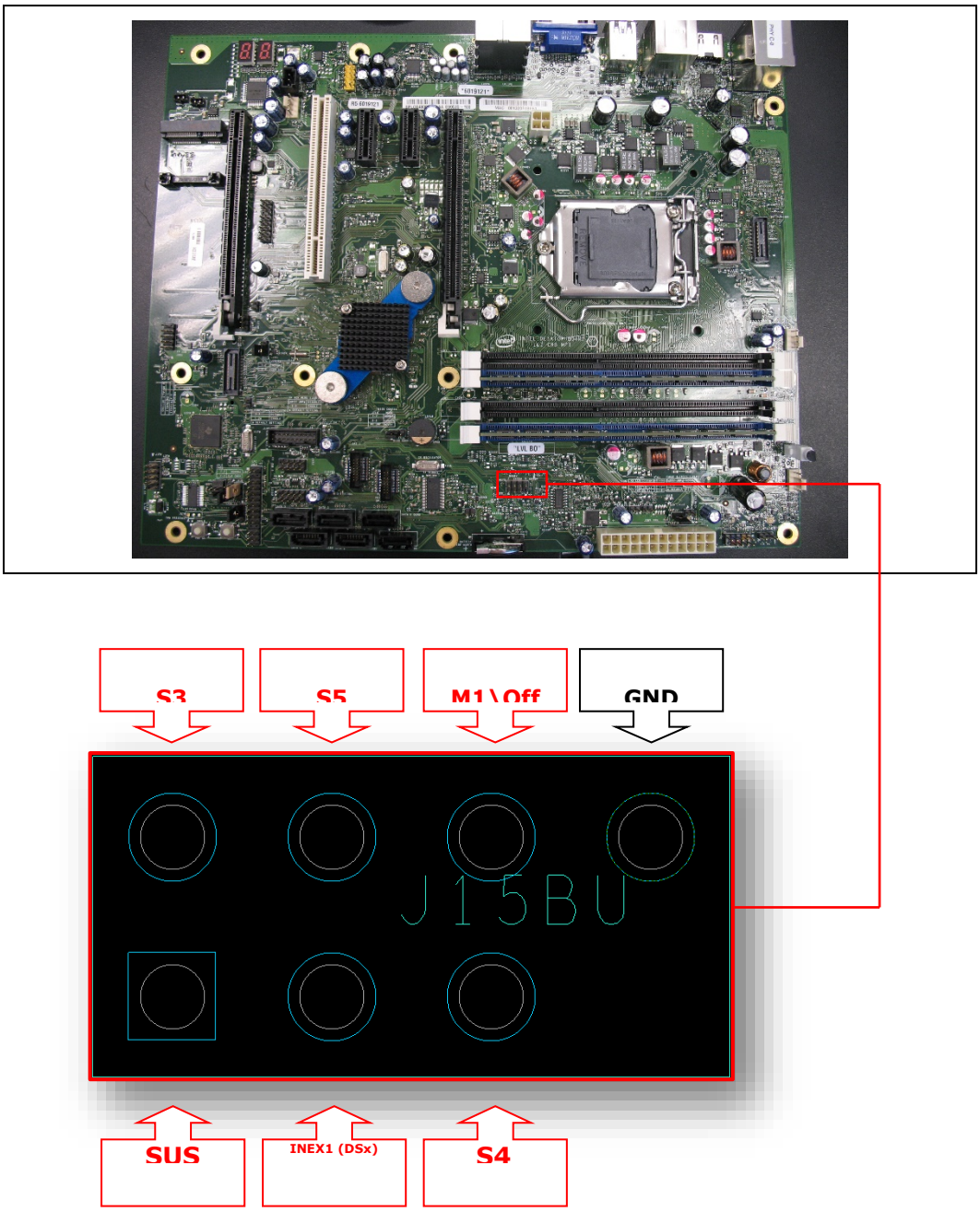


Note: If you do not connect this cable to the platform (for example, because the connection point is missing from the platform, or for some other reason), make sure you connect it to GND. Note also that if this cable is not connected to R8H12 pin 2, tests that depend on reading the Deep S3 states will fail.

Note: DS3 state detecting requires connection of both INEX1 and INEX2 wires.

O.8 Connecting Signal Sampling Cables to Maho Bay Desktop CRB

Connect the signals cables to J15BU as follows:



Note: For 1.5MB SKUs which do not implement the SLP_A, the SLP_A connection from the Intel® APS should be connected to the same point as the SLP_S3 connection.

Note: If you do not connect this cable to the platform (for example, because the connection point is missing from the platform, or for some other reason), make sure you connect it to GND. Note also that if this cable is not connected to J15BU pin 3, tests that depend on reading the Deep Sx states will fail.

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Appendix P Connecting Signal Sampling Cables to Aztec City Workstation CRB

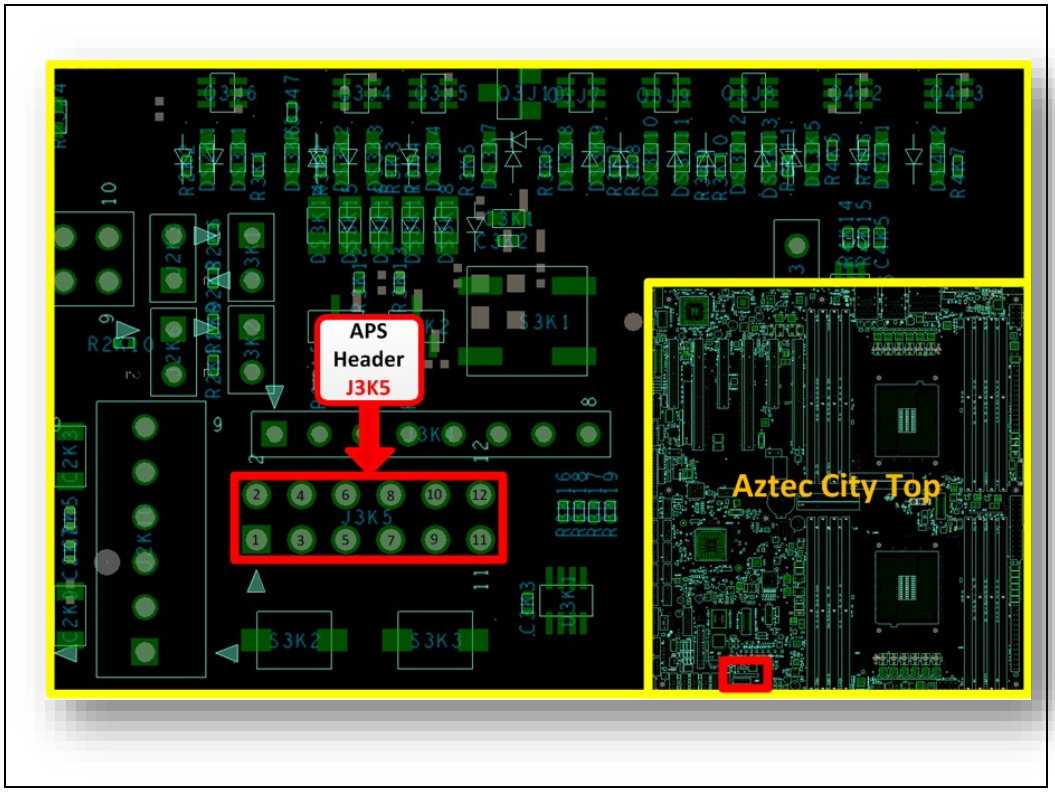
This chapter is intended to help users connect the Intel® Automatic Power Switch (Intel® APS3) device to the Intel® Aztec City platform.

P.1 Intel® APS Connection Scheme

This section provides figures for the Intel APS connection scheme.

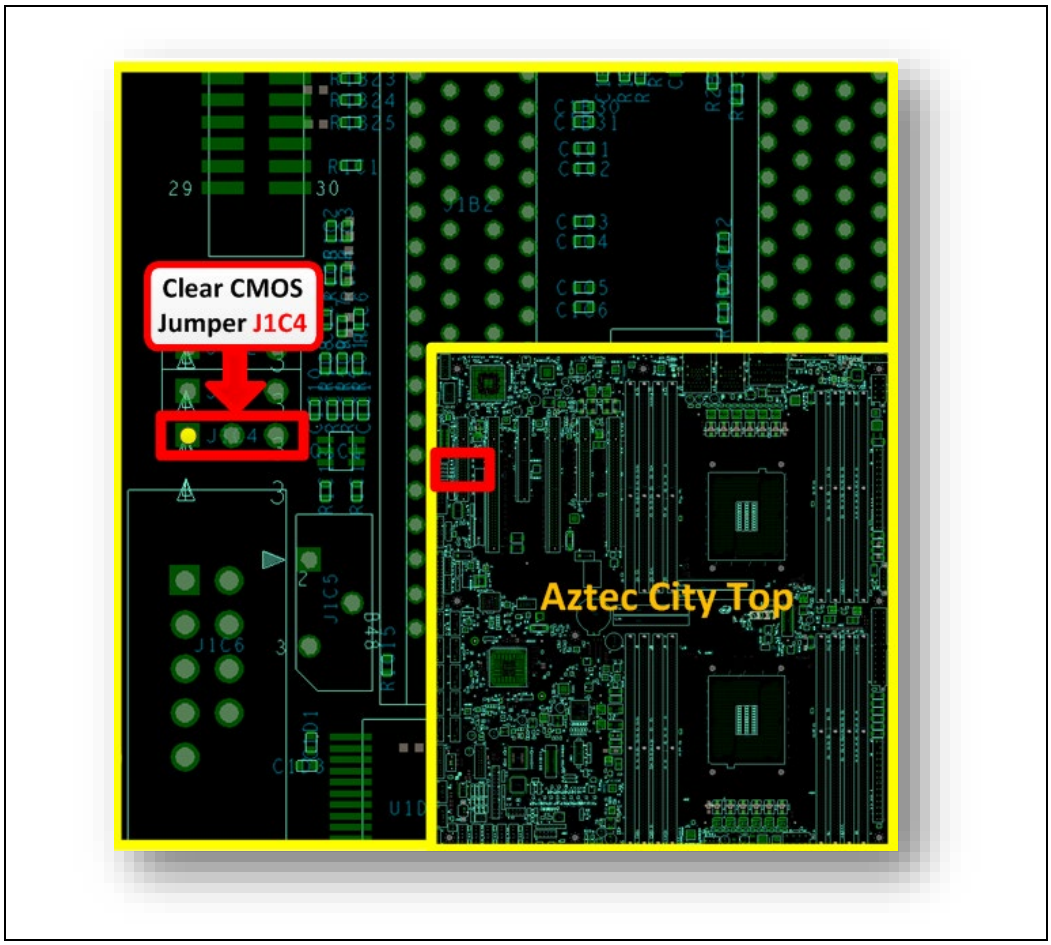
P.1.1 Intel® APS Header (J3K5) Connection

Figure 77. Header Connection



P.1.2 Clear CMOS (J1C4) Connection

Figure 78. Clear CMOS Diagram



P.2 Connection Steps

Connect the APS Main cable to the Intel Aztec City platform according to the following table.

Table 3. Connection Steps

APS Cable	Aztec City pin	Aztec City Signal Name
SUS	J3K5 pin 1	P3V3_AUX
S3	J3K5 pin 2	FM_SLPS3_N
INEX2	J3K5 pin 7	NC_APS_DS3 (not connected)
S5	J3K5 pin 4	FM_SLPS5_N
S4	J3K5 pin 5	FM_SLPS4_N
M1/OFF	J3K5 pin 6	FM_SLPA_N
INEX1	J3K5 pin 3	P3V3_STBY_DSW
GND	J3K5 pin 8	GND
PWR B	J3K5 pins 9-10	FP_PWR_BTN_N
RST B	J3K5 pins 11-12	FP_RST_BTN_N
CLR CMOS	J1C4 pins 1-2-3	RST_RTCRST_N

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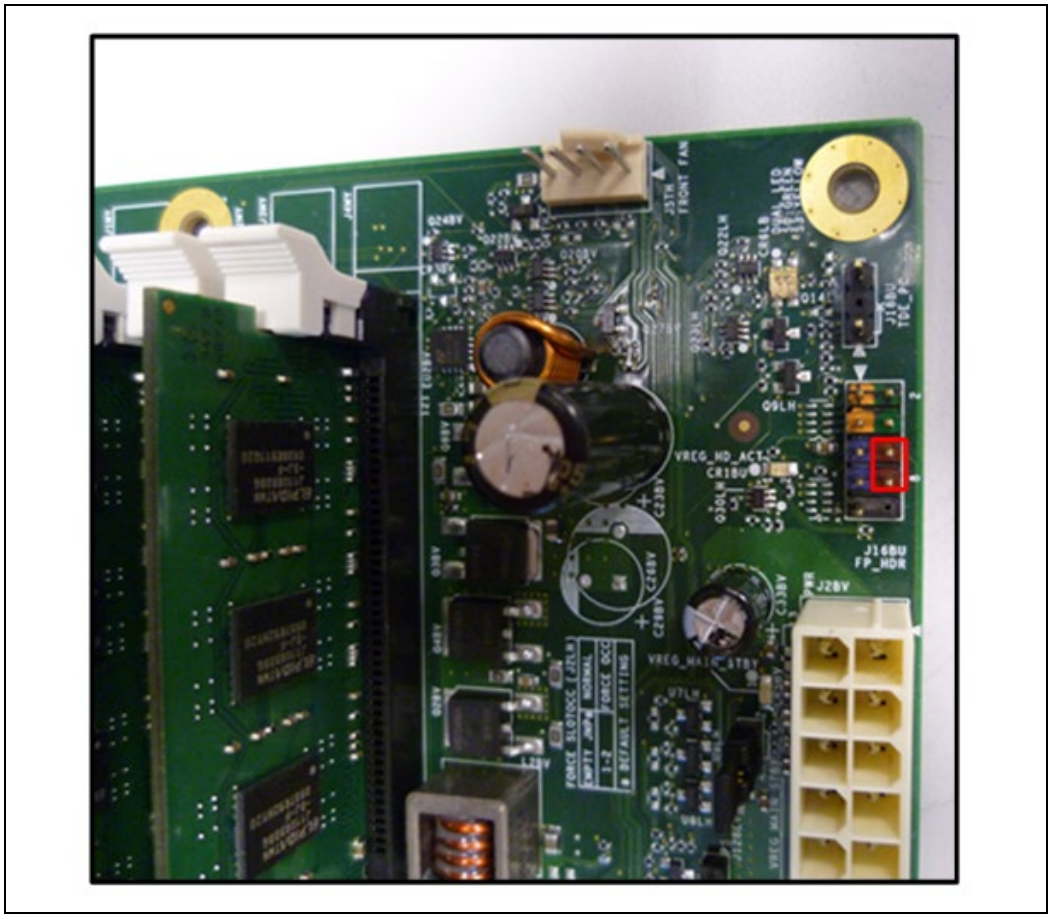
Appendix Q Connecting to Intel® 8 Series Express Chipset [formerly Lynx Point] CRBs

This section explains how to connect the Intel® APS to Lynx Point desktop and mobile CRBs. It includes photographs to illustrate all connections.

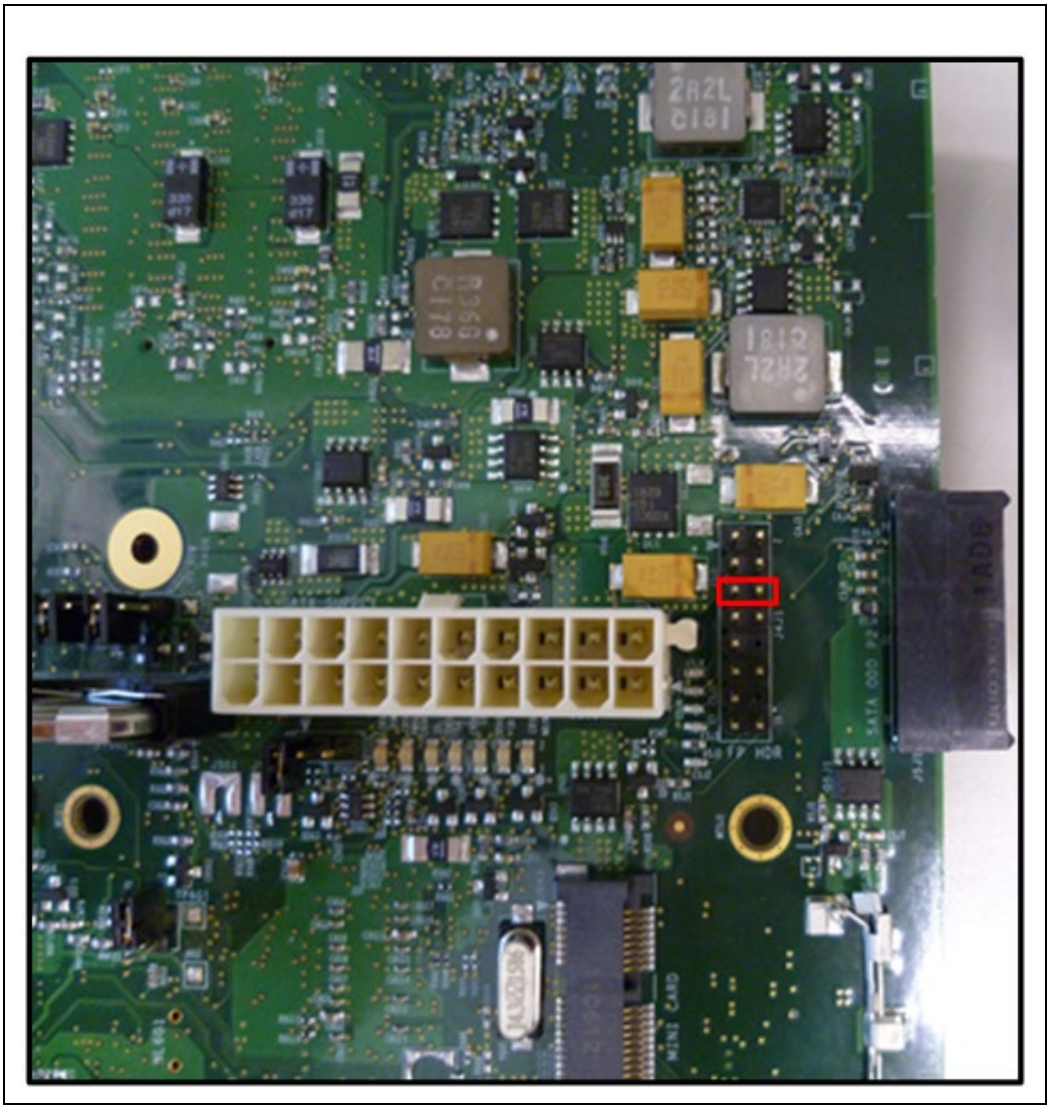
Q.1 Connecting to SUT Power Button on a Shark Bay DT (Lynx Point Desktop) CRB

Connect the Power button cable to J16BU pins 6-8.



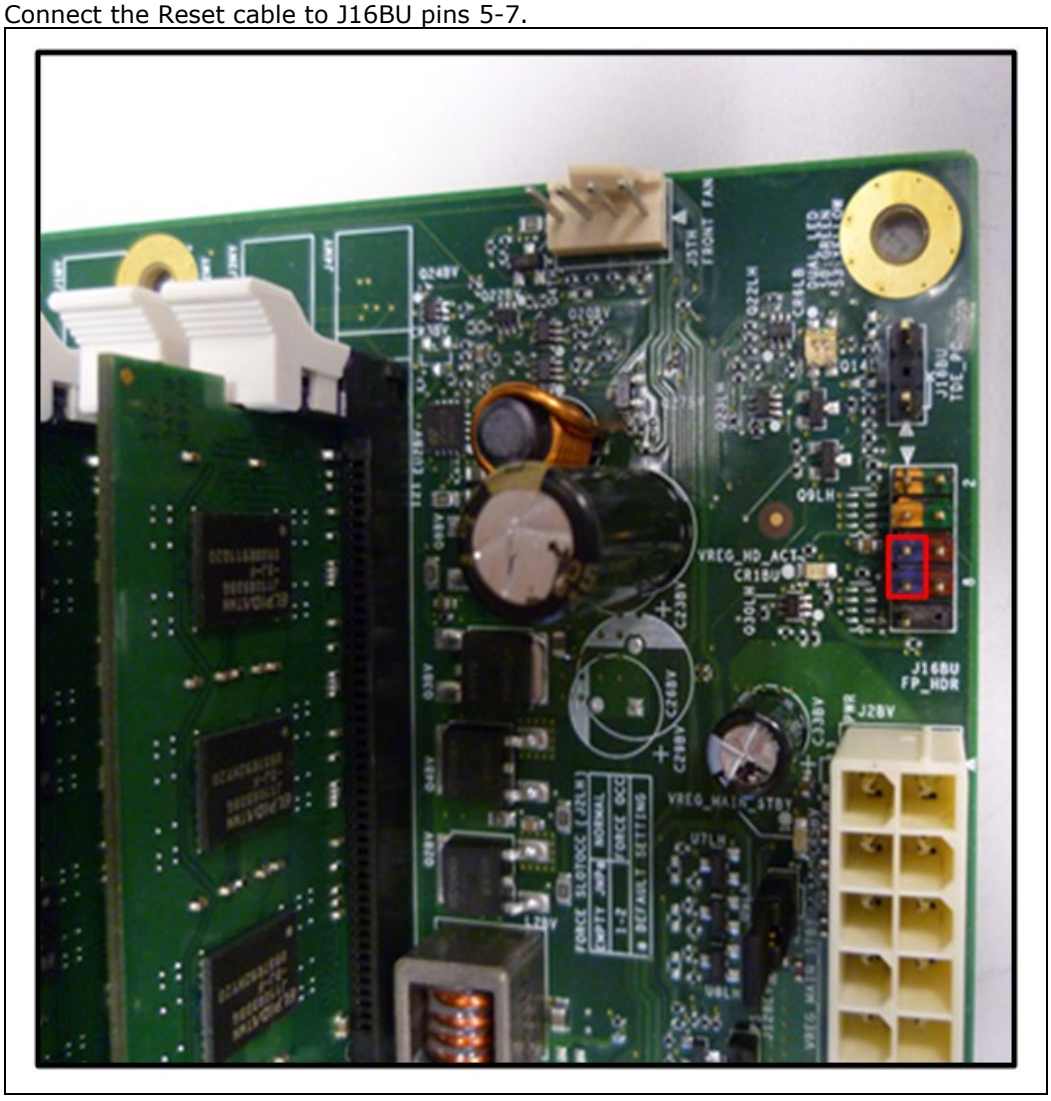
Q.2 Connecting to SUT Power Button on a Shark Bay MB (Lynx Point Mobile) CRB

Connect the Power button cable to J4J1, pins 5-6.



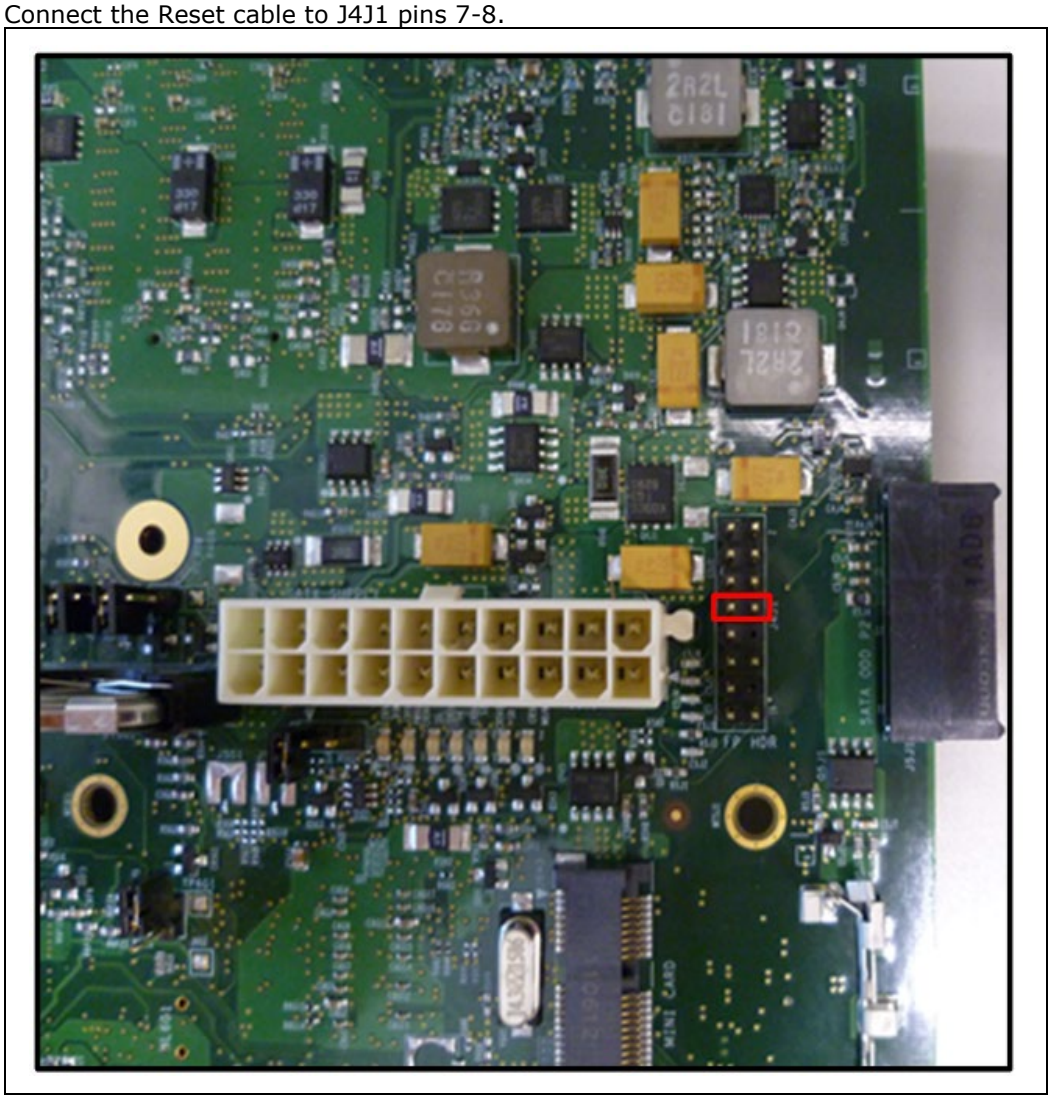
Q.3 Connecting to SUT Reset Button on a Shark Bay DT (Lynx Point Desktop) CRB

Connect the Reset cable to J16BU pins 5-7.



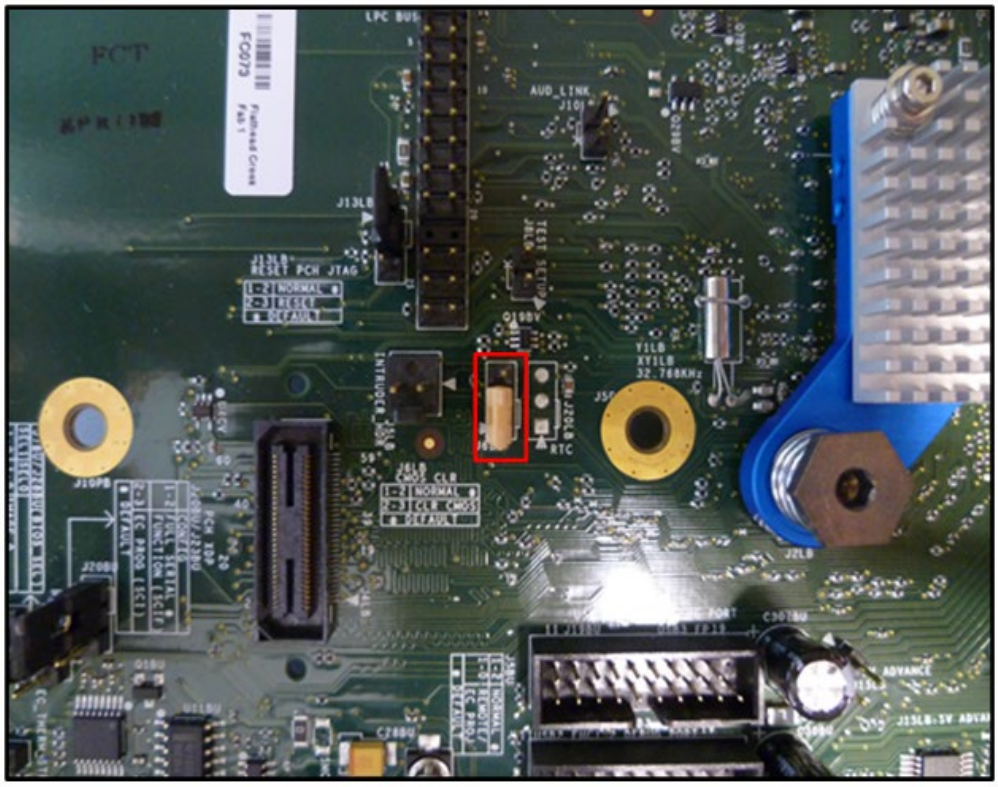
Q.4 Connecting to SUT Reset Button on a Shark Bay MB (Lynx Point Mobile) CRB

Connect the Reset cable to J4J1 pins 7-8.



Q.5 Connecting to SUT Clear CMOS on a Shark Bay DT (Lynx Point Desktop) CRB

Connect the Clear CMOS cable to J6LB.

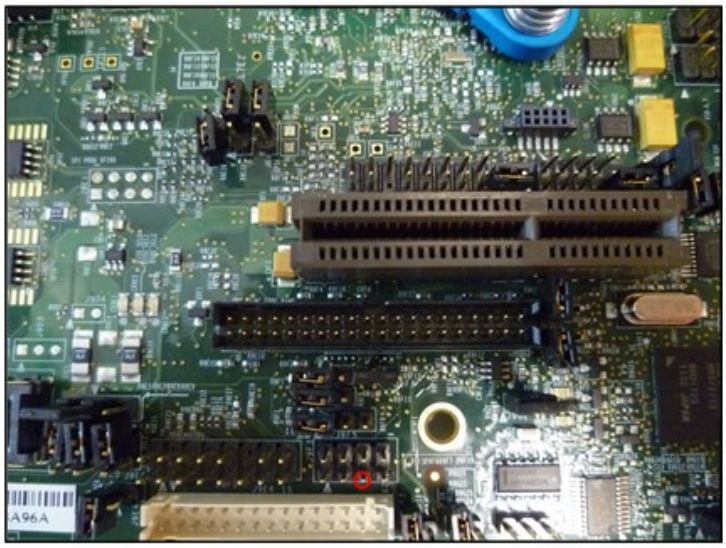


Q.6 Connecting to SUT Clear CMOS on a Shark Bay MB (Lynx Point Mobile) CRB

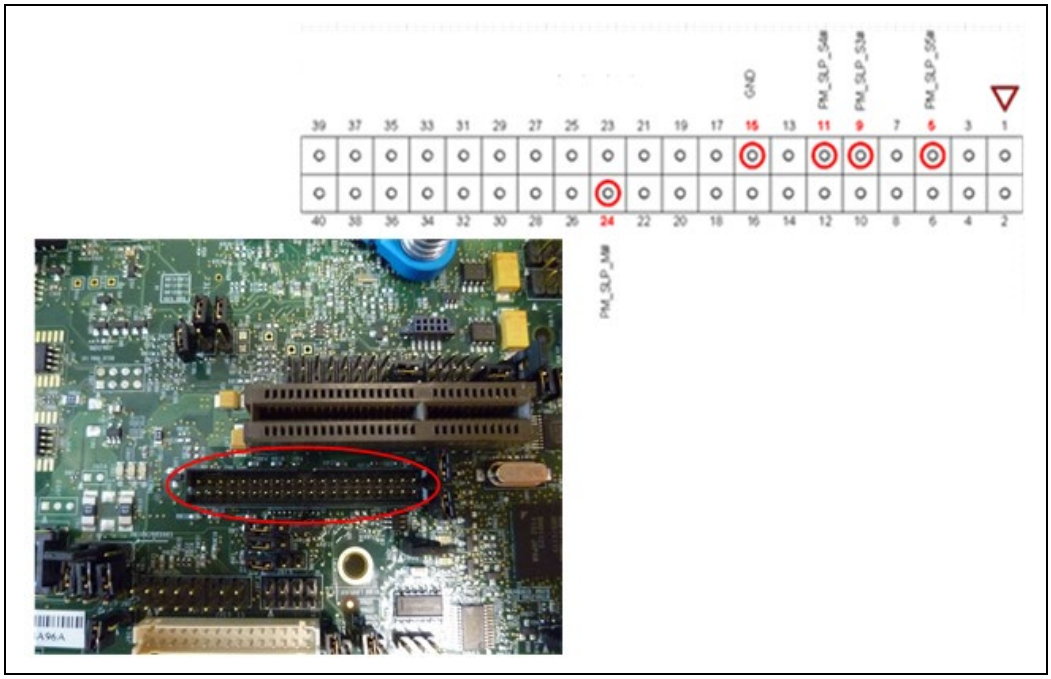
Connect the Clear CMOS cable to J5F2, pins 1-2.

Q.7 Connecting Signal Sampling Cables to Shark Bay Mobile CRB

Connect the **SUS** cable to J9F3 pin 5.

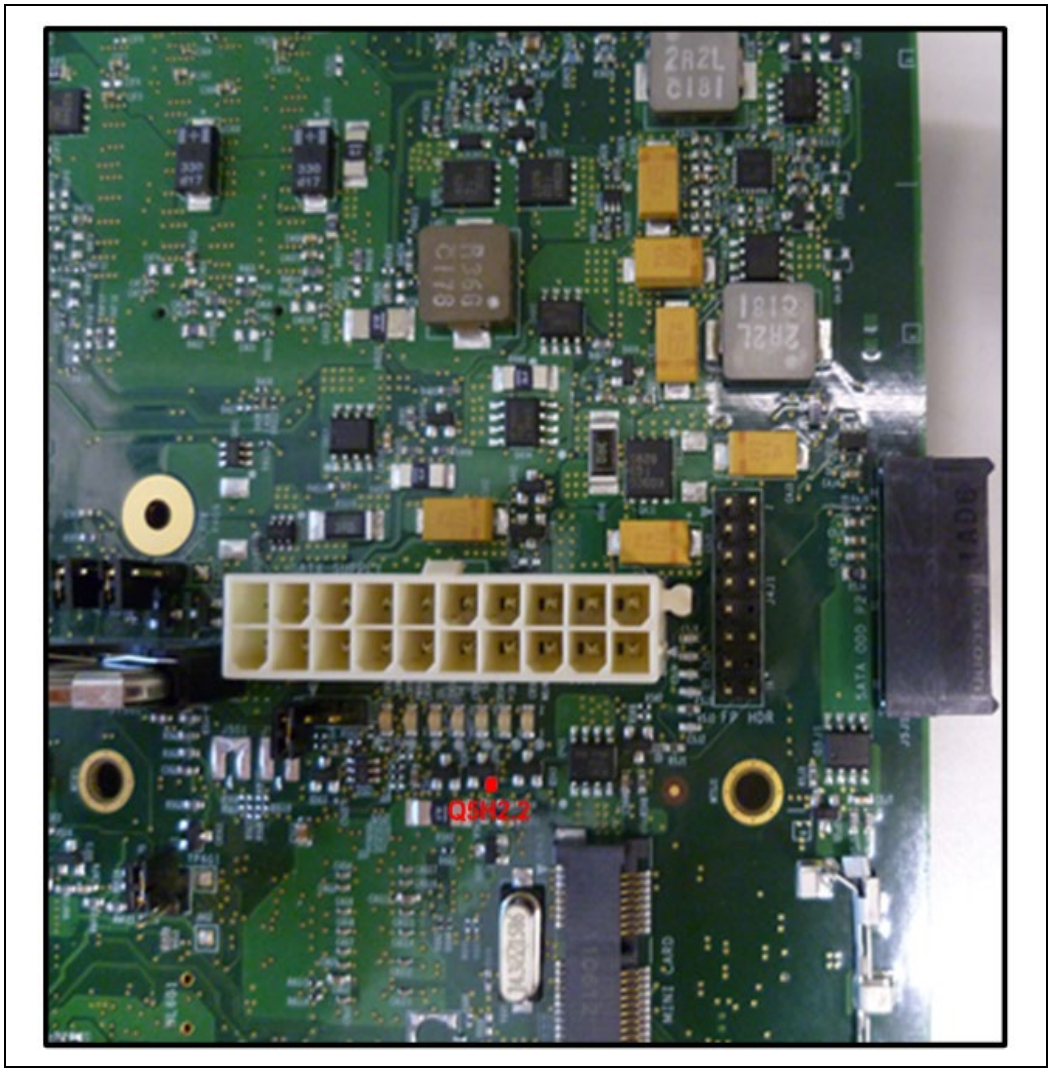


Connect the **GND** cable to J9G3 pin 15, **S4** cable to J9G3 pin 11, **S3** cable to J9G3 pin 9, **S5** cable to J9G3 pin 5, **M1/Off** cable to J9G3 pin 24.



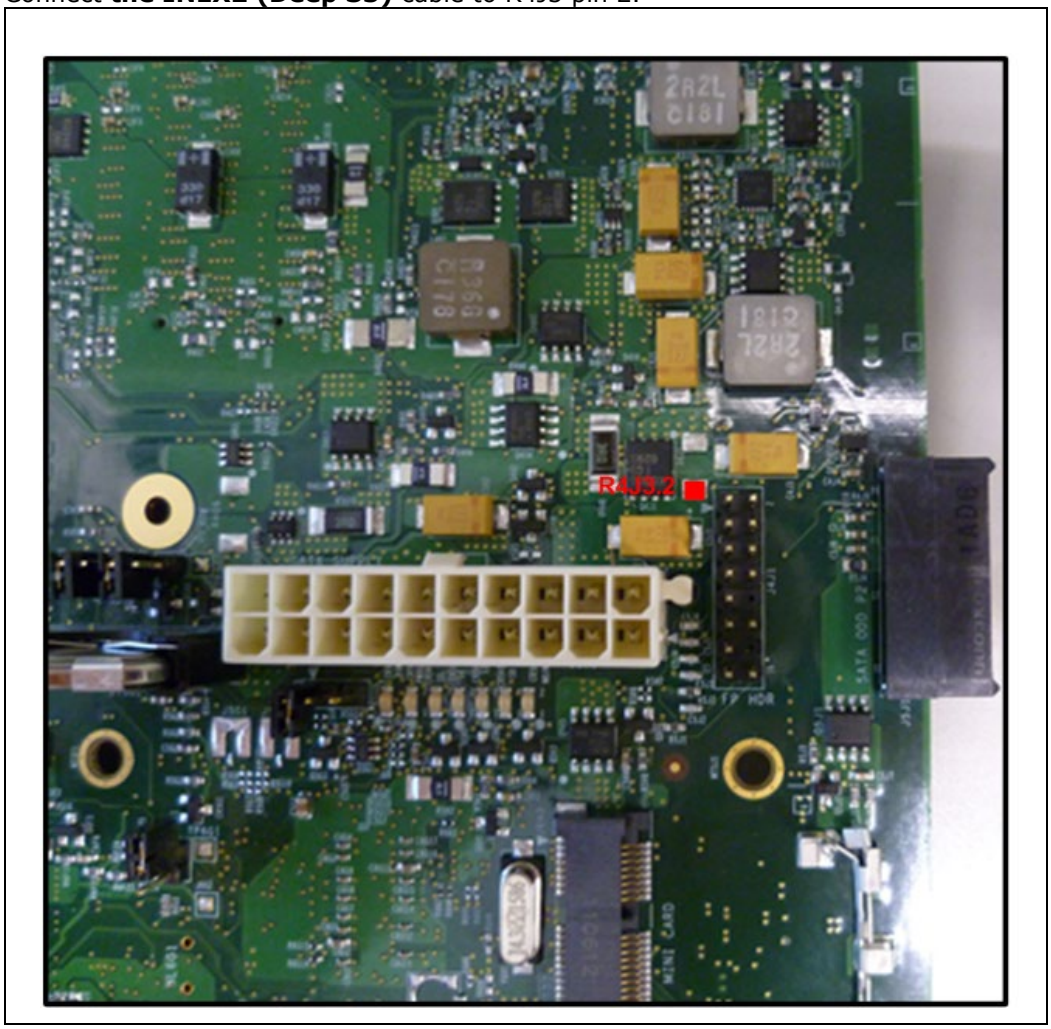
Note: For 1.5MB SKUs which do not implement the SLP_A, the SLP_A connection from the APS should be connected to the same point as the SLP_S3 connection.

Connect the **INEX1(Deep S4/5)**cable to Q5H2 pin 2.



Note: If you do not connect this cable to the platform (for example, because the connection point is missing from the platform, or for some other reason), make sure you connect it to GND. Note also that if this cable is not connected to Q5H2 pin 2, tests that depend on reading the Deep Sx states will fail.

Connect **the INEX2 (Deep S3)** cable to R4J3 pin 2.

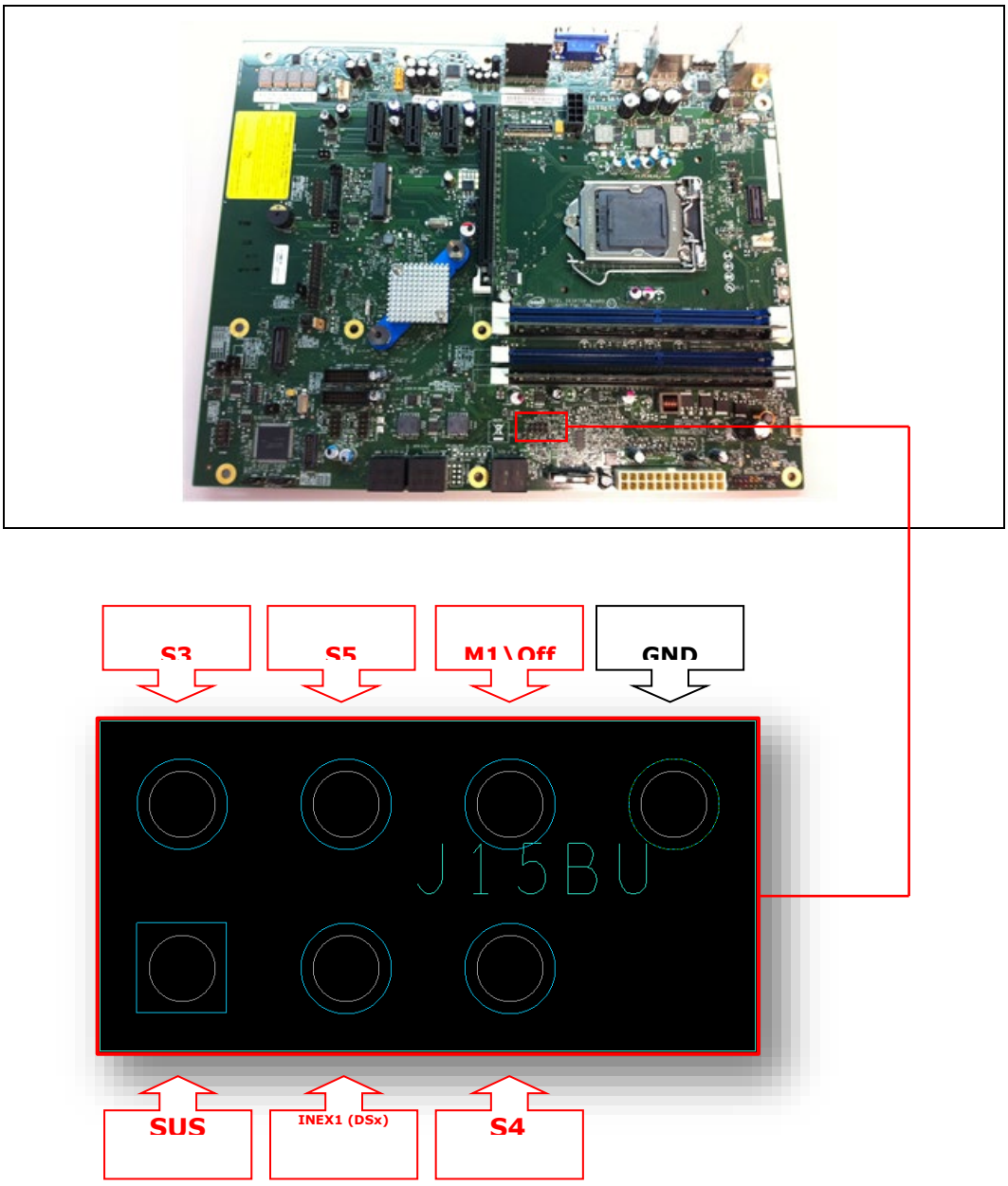


Note: If you do not connect this cable to the platform (for example, because the connection point is missing from the platform, or for some other reason), make sure you connect it to GND. Note also that if this cable is not connected to R4J3 pin 2, tests that depend on reading the Deep Sx states will fail.

Note: DSx states detecting requires connection of both INEX1 and INEX2 wires.

Q.8 Connecting Signal Sampling Cables to Shark Bay Desktop CRB

Connect the signals cables to J15BU as follows:



Appendix R Connecting Intel® APS to SKL Platforms

This section contains detailed instructions for connecting the Intel® APS to SKL RVP3 and RVP8 platforms. Following are high-level connection diagrams and picture of the connections.

R.1 RVP3

Figure 79. Intel® APS Connected to RVP3 via LPC Side Band HDR

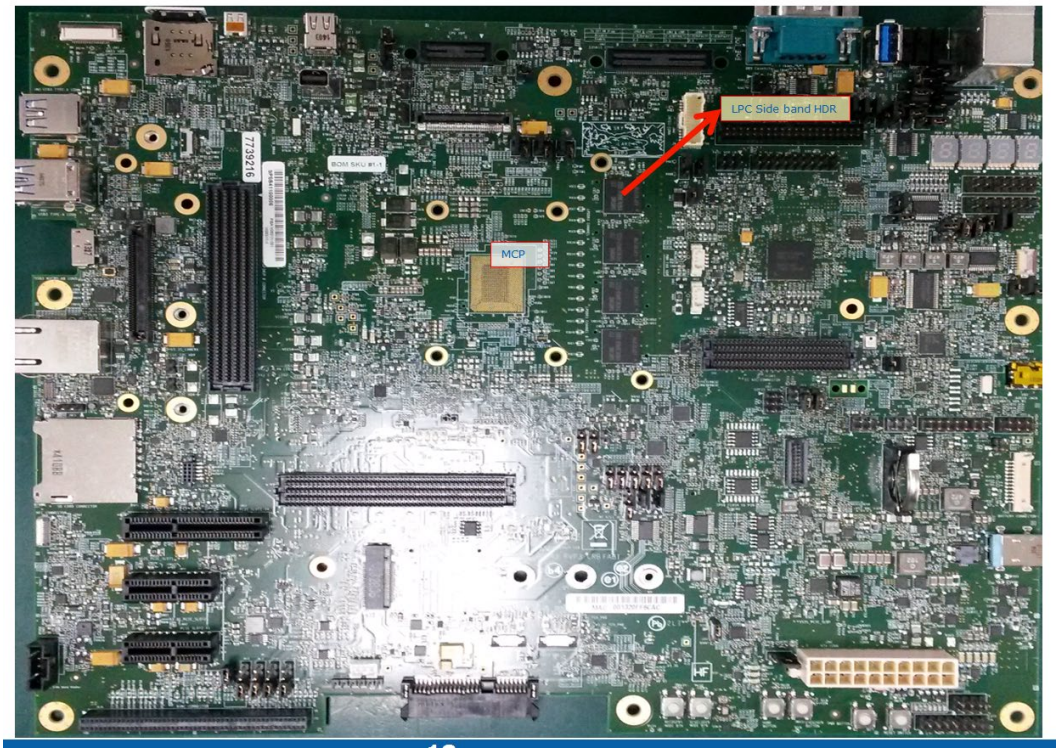


Figure 80. LPC Side Band HDR

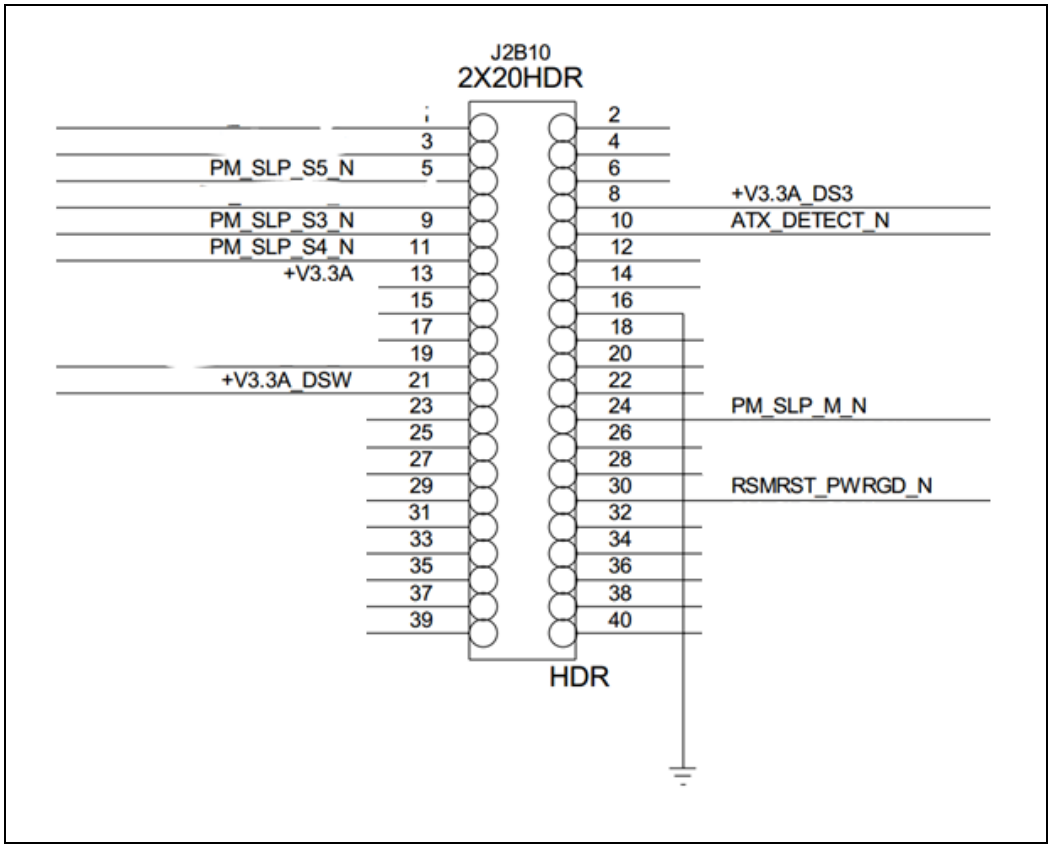


Table 3. SKL Platform LPC Side Band HDR – Pin-Out Description

Number	Name	Intel®APS3 Sampling Wire Labels
13	+V3.3A	VCC_Sus/S0
9	PM_SLP_S3_N	S3
11	PM_SLP_S4_N	S4
5	PM_SLP_S5_N	S5
24	PM_SLP_M_N	M1/MOFF
21	+V3.3A_DSW	INEX1(Deep S4/5)
8	+V3.3A_DS3	INEX2(Deep S3)

R.2 RVP8

Figure 81. Intel® APS Connected to RVP8 via LPC Side Band HDR

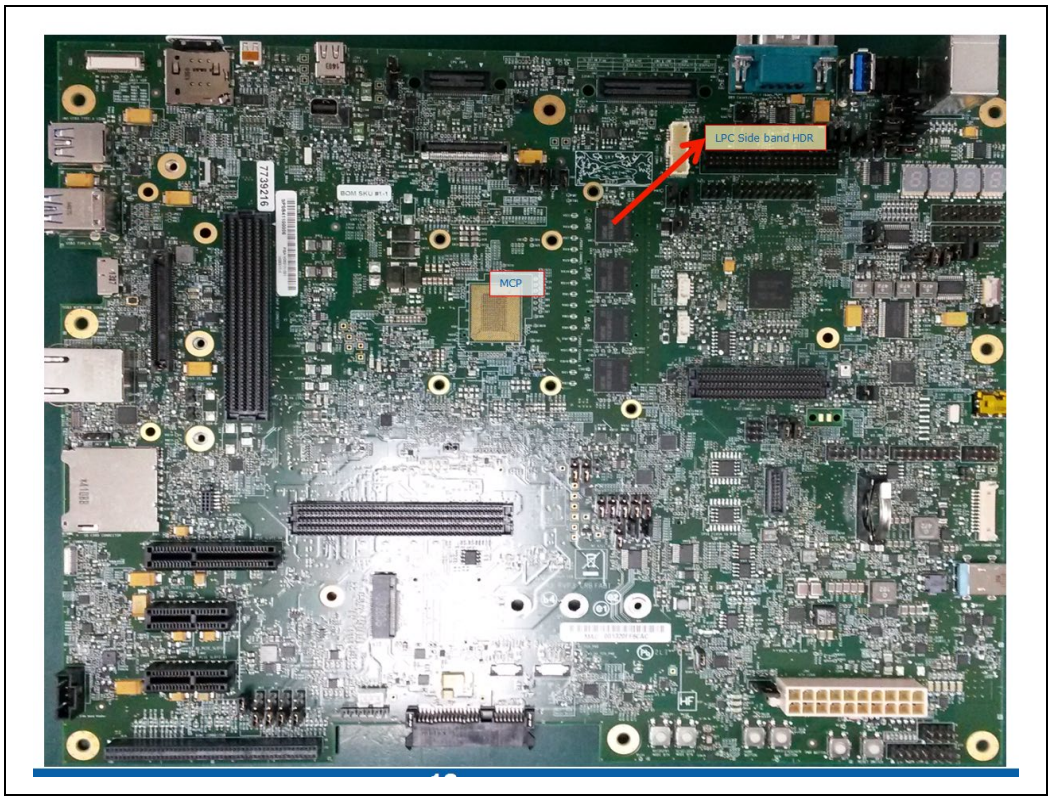
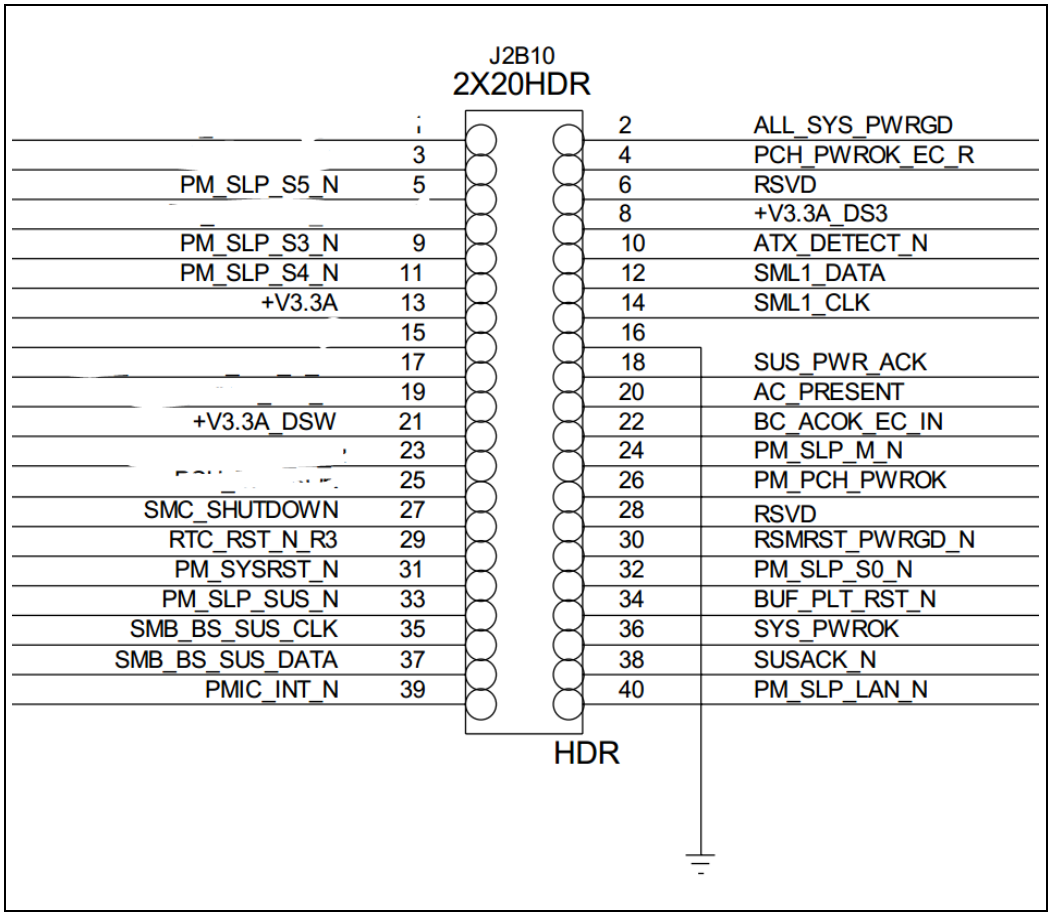


Figure 82. LPC Side Band HDR



Appendix S Locating Signals for Sampling on CRBs

To assist OEMs in locating the correct signals on the system under test, this section provides details of the signal names as they appear in the Cougar Point Desktop MPI Board schematic diagram, Cougar Point Mobile CRB schematic diagram, Panther Point Desktop MPI Board schematic diagram, Panther Point Mobile CRB schematic diagram, Lynx Point Desktop MPI Board schematic diagram, Lynx Point Mobile CRB schematic diagram and Aztec City CRB schematic diagram:

Intel® APS3 Sampling wire labels	CPT DT MPI Board schematic diagram signal names	PPT DT MPI Board schematic diagram signal names	LPT-H DT MPI Board schematic diagram signal names	Comments
Vcc_Sus/ S0	v_3p3_stby	v_3p3_stby	v_3p3_stby	
S3	SLP_S3_PCH_N	SLP_S3_PCH_N	SLP_S3_PCH_N	
S4	SLP_S4_N	SLP_S4_N	SLP_S4_N	
S5	v_3p3_stby	v_3p3_stby	v_3p3_stby	* On Desktop boards, the S5 wire needs to be connected to the same signal as the Vcc_Sus/S0 wire (labeled Sus in the diagram).
M1/M-OFF	PCH_SLP_A_N	PCH_SLP_M_N	PCH_SLP_M_N	
INEX1 (Deep S4/5)	V_3P3_A	V_3P3_A	V_3P3_A	

Intel® APS3 Sampling wire labels	CPT Mobile CRB schematic diagram signal names	PPT Mobile CRB schematic diagram signal names	LPT-H Mobile CRB schematic diagram signal names	Aztec City Signal Name	Comments
Vcc_Sus/ S0	+V3.3A	+V3.3A	+V3.3A	P3V3_AUX	VCC 3.3A is always present, except in G3 state.
S3	PM_SLP_S3#	PM_SLP_S3#	PM_SLP_S3#	FM_SLPS3_N	
S4	PM_SLP_S4#	PM_SLP_S4#	PM_SLP_S4#	FM_SLPS4_N	
S5	PM_SLP_S5#	PM_SLP_S5#	PM_SLP_S5#	FM_SLPS5_N	
M1/M-OFF	PM_SLP_A#	PM_SLP_M#	PM_SLP_M#	FM_SLPA_N	
INEX1 (Deep S4/5)	+VREG3	+VREG3	+V3.3DS	P3V3_STBY_DSW	
INEX2 (Deep S3)		+V3.3A_DS3*	+V3.3A_DS3	NC_APS_DS3	*Refers to Emerald Lake2 FAB2 platform. DS3 state detecting requires connection of both INEX1 and INEX2 wires.

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Appendix T Intel® APS Connector Requirements According to PDG

Intel® Automatic Power Switcher (Intel® APS) is a tool that interfaces with the Intel® Platform Enablement Test Suite (Intel® PETS) used to test compliancy to Intel® ME requirements and is a validation vehicle to assist with the reproduction of power management and power sequencing issues. The Intel® APS signals are required to be present at an accessible location on the board. Routing these signals to a connector is strongly recommended and will contribute significantly to accelerating debug and verification of system Intel® ME compliancy. If Intel® PETS tests are run on a pre-production SUT (System Under Test), the Intel® APS connector may be removed from the production system board layout.

An Intel® APS header allows for easy connection to a platform without extensive rework and/or intrusion by grouping signals required by the Intel® APS to a common connector.

Note: It is strongly recommended that the name 'Intel® APS' or 'Intel® PETS' be labeled in silk screen next to the connector and/or pads, and each pin name clearly marked in silk screen on the PCB.

T.1 Intel® APS Connector Requirements According to Maho Bay PDG

It is strongly recommended to use a 14 (2 rows of 7 pins) male header with pin width of.64mm, pin height of 5.84mm and a 2.54 mm distance (pitch) between pins.

The required signals from the PCH as well as the recommended signal routing to the connector are provided below. Each name in the 'Pin' column refers to the signal or rail defined in the PCH External Design Specification (EDS).

APS Connector	Pin	Comments
Pin 1	VccSus3_3	3.3 V Suspend Power Well
Pin 2	SLP_S3#	When asserted (0) system is in S3
Pin 3	VccDSW3_3	Used to determine if system is in Deep Sx

APS Connector	Pin	Comments
Pin 4	VccSus3_3	When off (0) system is in S5
Pin 5	SLP_S4#	When asserted (0) system is in S4
Pin 6	SLP_A#	When asserted (0) ME is in Moff
Pin 7	Unused	
Pin 8	GND	Ground
Pin 9	RSTRST#	When asserted (0) CMOS is cleared
Pin 10	GND	Ground for RTCRST#
Pin 11	PWRBTN#	When asserted (0) Power Button Pushed
Pin 12	GND	Ground for PWRBTN#
Pin 13	SYS_RESET#	When asserted (0) Reset Button Pushed
Pin 14	GND	Ground for SYS_RESET#

T.2 Intel® APS Connector Requirements According to Chief River PDG

It is recommended to use a single 14 pin (2 rows of 7 pins) male header with pin width of .64 mm, pin height of 5.84 mm and a 2.54 mm distance (pitch) between pins.

On mobile platforms the signals should be routed to pads or a connector with pins near the memory slots so that the required signals on a laptop form factor can be easily accessed through the self-service DIMM exchange door on the bottom of a platform.

The required signals from the PCH as well as the recommended signal routing to the connector are provided below. Each name in the 'Pin' column refers to the signal or rail defined in the PCH External Design Specification (EDS).

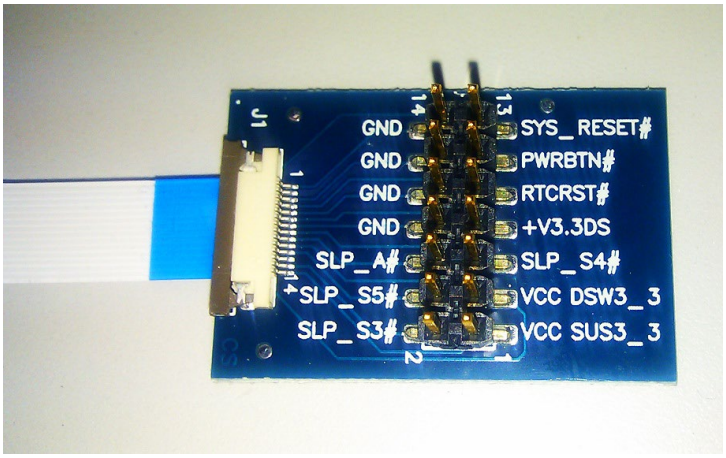
APS Connector	Pin	Comments
Pin 1	VccSus3_3	3.3 V Suspend Power Well
Pin 2	SLP_S3#	When asserted (0) system is in S3
Pin 3	VccDSW3_3	Used to determine if system is in Deep Sx
Pin 4	SLP_S5#	When asserted (0) system is in S5
Pin 5	SLP_S4#	When asserted (0) system is in S4
Pin 6	SLP_A#	When asserted (0) ME is in Moff
Pin 7	Unused	
Pin 8	GND	Ground
Pin 9	RSTRST#	When asserted (0) CMOS is cleared
Pin 10	GND	Ground for RTCRST#
Pin 11	PWRBTN#	When asserted (0) Power Button Pushed
Pin 12	GND	Ground for PWRBTN#
Pin 13	SYS_RESET#	When asserted (0) Reset Button Pushed
Pin 14	GND	Ground for SYS_RESET#

T.3 Intel® APS Connector Requirements According to Shark Bay Haswell 2-Chip PDG

It is strongly recommended to use one of the two proposed connector types. For more information on the 14-pin through-hole header and the Intel® APS 14-pin connector, please refer to the Shark Bay Mobile Platform Design Guide.

The following table applies to the 14-pin Intel® APS Connector used on Chief River and Haswell 2-Chip designs pictured in the figure below:

Figure 83. 14-Pin Intel® APS Adapter



Note: The signals in the **Signal Name** column may be labeled differently on the CRB.

Pin	Signal Name	APS Signal Sampling and Control Lines	Description
1	VccSus3_3	Sus (Vcc_Sus/S0)	3.3 V Suspend Power Well
2	SLP_S3#	S3	When asserted (0) system is in S3.
3	VccDSW3_3	INEX2 (DeepS3)	Used to determine if the system is in DeepS3.
4	SLP_S5#	S5	When asserted (0) system is in S5.

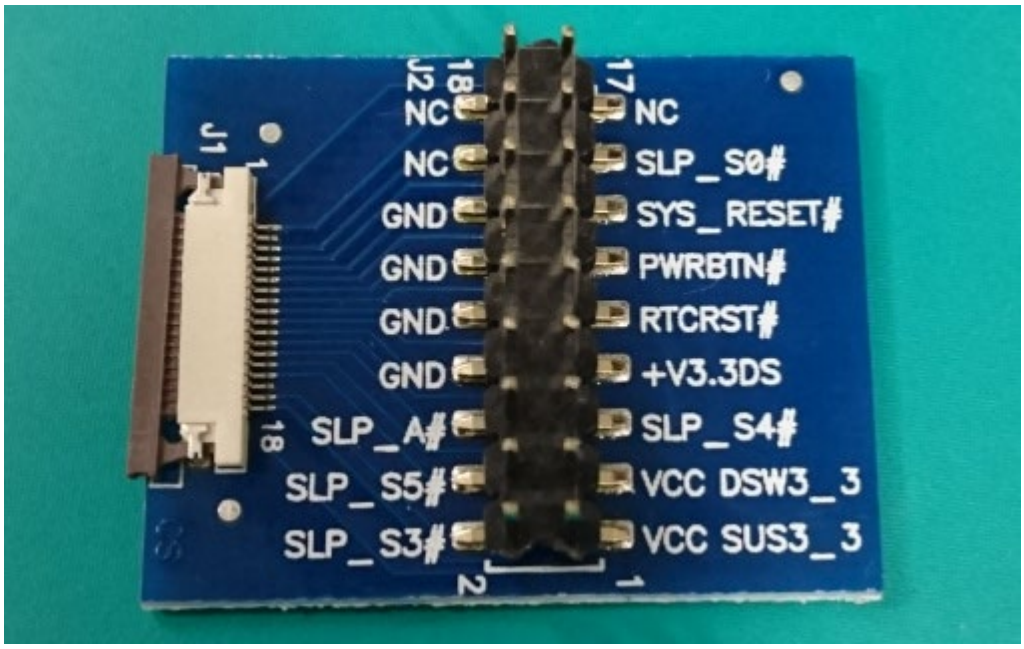
5	SLP_S4#	S4	When asserted (0) system is in S4.
6	SLP_A#	M1/OFF (M1/M-OFF)	When asserted (0) Intel ME is in Moff.
7	+V3.3DS	INEX1(DeepS4/5)	Used to determine if the system is in DeepS4/S5.
8	GND	GND (Ground)	Ground
9	RTCRST#	CLR CMOS (Clear CMOS)	When asserted (0) CMOS is cleared
10	GND		Ground for RTCRST#
11	PWRBTN#	PWR B (Power Button)	When asserted (0) Power Button Pushed
12	GND		Ground for PWRBTN#
13	SYS_RESET#	RST B (Reset Button)	When asserted (0) Reset Button Pushed
14	GND		Ground for SYS_RESET#

T.4 Intel® APS Connector Requirements According to Haswell U/Y PDG

It is strongly recommended to use one of the two proposed connector types. For more information on the 18-pin through-hole header and the Intel® APS 18-pin connector, please refer to the Haswell U/Y Platform Design Guide.

The following table applies to the 18-pin Intel® APS Connector used on Haswell ULT designs shown below

Figure 84. 18-Pin Intel® APS Adapter



Note: The signals in the **Signal Name** column may be labeled differently on the CRB.

Table 4. Signal names of Intel® APS Adapter Pins

Pin	Signal Name	Intel® APS Signal Name	Description
1	VccSus3_3	SUS (Vcc_Sus/S0)	3.3 V Suspend Power Well
2	SLP_S3#	S3	When asserted (0) system is in S3.
3	VccDSW3_3	INEX2 (DeepS3)	Used to determine if the system is in DeepS3.
4	SLP_S5#	S5	When asserted (0) system is in S5.
5	SLP_S4#	S4	When asserted (0) system is in S4.
6	SLP_A#	M1/OFF (M1/M-OFF)	When asserted (0) Intel ME is in Moff.
7	+V3.3DS	INEX1(DeepS4/5)	Used to determine if the system is in DeepS4/S5.

8	GND	GND (Ground)	Ground
9	RTCRST#	CLR CMOS (Clear CMOS)	When asserted (0) CMOS is cleared
10	GND		Ground for RTCRST#
11	PWRBTN#	PWR B (Power Button)	When asserted (0) Power Button Pushed
12	GND		Ground for PWRBTN#
13	SYS_RESET#	RST B (Reset Button)	When asserted (0) Reset Button Pushed
14	GND		Ground for SYS_RESET#
15	SLP_S0		When asserted (0) system is in deterministic idle state.
16	NC		No connection.
17	NC		No connection.
18	NC		No connection.

T.5 Intel® APS Connector Requirement according to Sky Lake U/Y PDG

It is strongly recommended to use one of the two proposed connector types. For more information on the 18-pin through-hole header and the Intel® APS 18-pin connector, please refer to the Sky Lake-U/Y Platform Design Guide CDI doc ID 543016.

Refer to FIGURE 84 and TABLE 4.

T.6 Intel® APS Connector Requirement according to Kaby Lake H/S PDGs

For KBL-S: more information on Intel® APS 18-pin connectoris available in Kaby Lake-S Platform Design Guide CDI doc ID 564041.

For KBL-H: It is strongly recommended to use one of the two proposed connector types. For more information on the 18-pin through-hole header and the Intel® APS

18-pin connector, please refer to Kaby Lake-H Platform Design Guide CDI doc ID 575232.

Refer to FIGURE 84 and TABLE 4.

T.7 Intel® APS Connector Requirement according to Coffee Lake U/H/S and Cannon Lake U/Y PDGs

It is strongly recommended to use one of the two proposed connector types. For more information on the 18-pin header and the Intel® APS 18-pin connector, please refer to the Cannon Lake U/Y PDG CDI doc ID 566468, Coffee Lake-H PDG CDI doc ID 571391,and Coffee Lake-S PDG CDI doc ID 571264.

The following table applies to the 18-pin Intel® APS Connector shown in FIGURE 84.

Table 5. Signal names of Intel® APS Adapter Pins For CFL H/S Platforms

Pin	Signal Name	Intel® APS Signal Name	Description
1	VCCPRIM_3P3	SUS	3.3 V Suspend Power Well
2	GPD_4_SLP_S3	S3	When asserted (0) system is in S3.
3	No connection.	No connection.	No connection.
4	GPD_10_SLP_S5#	S5	When asserted (0) system is in S5.
5	GPD_5_SLP_S4#	S4	When asserted (0) system is in S4.
6	GPD_6_SLP_A#	M1/OFF	When asserted (0) Intel ME is in Moff.
7	VCCDSW_3P3	INEX1(DeepS4/5)	Used to determine if the system is in DeepS4/S5.
8	GND	GND (Ground)	Ground
9	RTCRST#		When asserted (0) CMOS is cleared
10	GND		Ground for RTCRST#
11	PWRBTN#	PWR B (Power Button)	When asserted (0) Power Button Pushed
12	GND		Ground for PWRBTN#

13	SYS_RESET#	RST B (Reset Button)	When asserted (0) Reset Button Pushed
14	GND		Ground for SYS_RESET#
15	GPP_B12_SLP_S0		When asserted (0) system is in deterministic idle state.
16	NC	No connection.	No connection.
17	NC	No connection.	No connection.
18	NC	No connection.	No connection.

T.8 Intel® APS Connector Requirement according to Gemini Lake PDG

It is strongly recommended to use one of the two proposed connector types. For more information on the 18-pin header and the Intel® APS 18-pin connector, please refer to the Gemini Lake Platform Design Guide CDI doc ID 567247.

The following table applies to the 18-pin Intel® APS Connector shown in FIGURE 84.

Table 6. Signal names of Intel® APS Adapter Pins For GLK Platforms

Pin	Signal Name	Intel® APS Signal Name	Description
1	Power well such as V3P3A	SUS	Power well indication that the system is in S0 power state
2	PMU_SLP_S3_N	S3	When asserted (0) system is in S3, S4 & S5.
3	No connection.	No connection.	No connection.
4	No connection.	No connection.	No connection.
5	PMU_SLP_S4_N	S4	When asserted (0) system is in S4 & S5.

6	No connection.	No connection.	No connection.
7	No connection.	No connection.	No connection.
8	GND	GND (Ground)	Ground
9	RTC_TEST_N		When asserted (0) CMOS is cleared
10	GND		Ground for (for RTC_TEST_N)
11	PMU_PWRBTN_N	PWR B (Power Button)	When asserted (0) Power Button Pushed
12	GND		Ground for (for PMU_PWRBTN_N)
13	PMU_RSTBTN_N	RST B (Reset Button)	When asserted (0) Reset Button Pushed
14	GND		Ground (for PMU_RSTBTN_N)
15	PMU_SLP_S0_N		When asserted (0) system is in deterministic idle state.
16	No connection.	No connection.	No connection.
17	RTC_RST_N		When asserted (0) all register bits in the RTC well are reset and system is reset.
18	GND		Ground (for RTC_RST_N)

T.9 Intel® APS Connector Requirement according to Ice Lake U/Y PDG

It is strongly recommended to use one of the two proposed connector types. For more information on the 18-pin header and the Intel® APS 18-pin connector, please refer to the Ice Lake U/Y PDG CCL doc ID 572907.

The following table applies to the 18-pin Intel® APS Connector shown in FIGURE 84.

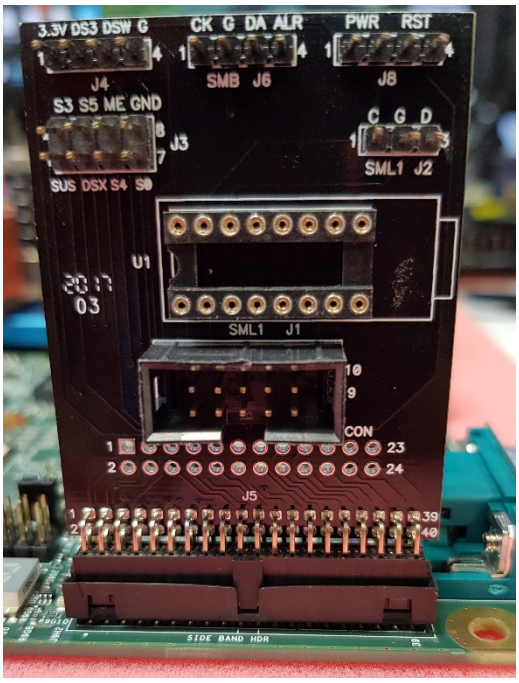
Table 7. Signal names of Intel® APS Adapter Pins For ICL-U/Y Platforms

Pin	Signal Name	Intel® APS Signal Name	Description
1	VCCPRIM_3P3	SUS	3.3 V Suspend Power Well
2	GPD_4_SLP_S3	S3	When asserted (0) system is in S3.

Pin	Signal Name	Intel® APS Signal Name	Description
3	No connection.	No connection.	No connection.
4	GPD_10_SLP_S5#	S5	When asserted (0) system is in S5.
5	GPD_5_SLP_S4#	S4	When asserted (0) system is in S4.
6	GPD_6_SLP_A#	M1/OFF	When asserted (0) Intel® CSME is in Moff.
7	VCCDSW_3P3	INEX1(Deep S4/S5)	Used to determine if the system is in Deep S4/S5.
8	GND	GND (Ground)	Ground
9	RTCRST#		When asserted (0) CMOS is cleared
10	GND		Ground for RTCRST#
11	GPD_3_PWRBTN#	PWR B	When asserted (0) Power Button Pushed
12	GND	PWR B GND	Ground for PWRBTN#
13	SYS_RESET#	RST B	When asserted (0) Reset Button Pushed
14	GND	RST B GND	Ground for SYS_RESET#
15	GPP_B12_SLP_S0		When asserted (0) system is in deterministic idle state.
16	NC	No connection.	No connection.
17	NC	No connection.	No connection.
18	NC	No connection.	No connection.

In case the customer is using an Intel RVP, Version 0.5 of SML1 Card is recommended to be used and connected on the side band header J9H2. See **FIGURE 85** below.

Figure 85 : SML-1 Card for Intel RVP's



The following table applies to the SML1 card shown in FIGURE 85

Table 8. Signal names of Intel® APS Adapter Pins For ICL-U/Y Platforms

SML 1 Card Pin	Intel® APS Signal Name	Description
3J-1	SLP_SUS	3.3 V Suspend Power Well
J3-2	SLP_S3	When asserted (0) system is in S3.
J3-5	SLP_S4	When asserted (0) system is in S4.
J3-4	SLP_S5	When asserted (0) system is in S5.
J3-6	ME	When asserted (0) Intel® ME is in Moff.
J4-3	INEX1(Deep S4/S5)	Used to determine if the system is in Deep S4/S5.
J4-2	No Connection	No Connection

J3-8	GND (Ground)	Ground

T.10 Intel® APS Connector Requirement according to Comet Lake U PDG

It is strongly recommended to use one of the two proposed connector types. For more information on the 18-pin header and the Intel® APS 18-pin connector, please refer to the Comet Lake U PDG CCL doc ID 607109.

TABLE 7 applies to the 18-pin Intel® APS Connector shown in FIGURE 84.

In case the customer is using an Intel RVP, Version 0.5 of SML1 Card is recommended to be used and connected on the side band header J9H2. See FIGURE 85 above.

T.11 Intel® APS Connector Requirement according to Tiger Lake UP3/UP4 PDG

It is strongly recommended to use one of the two proposed connector types. For more information on the 18-pin header and the Intel® APS 18-pin connector, please refer to the Tiger Lake UP3/UP4 PDG CCL doc ID 607872.

TABLE 7 applies to the 18-pin Intel® APS Connector shown in FIGURE 84.

In case the customer is using an Intel RVP, Version 0.5 of SML1 Card is recommended to be used and connected on the side band header J9H2. See FIGURE 85 above.

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Appendix U Intel® APS3 Rework Instructions

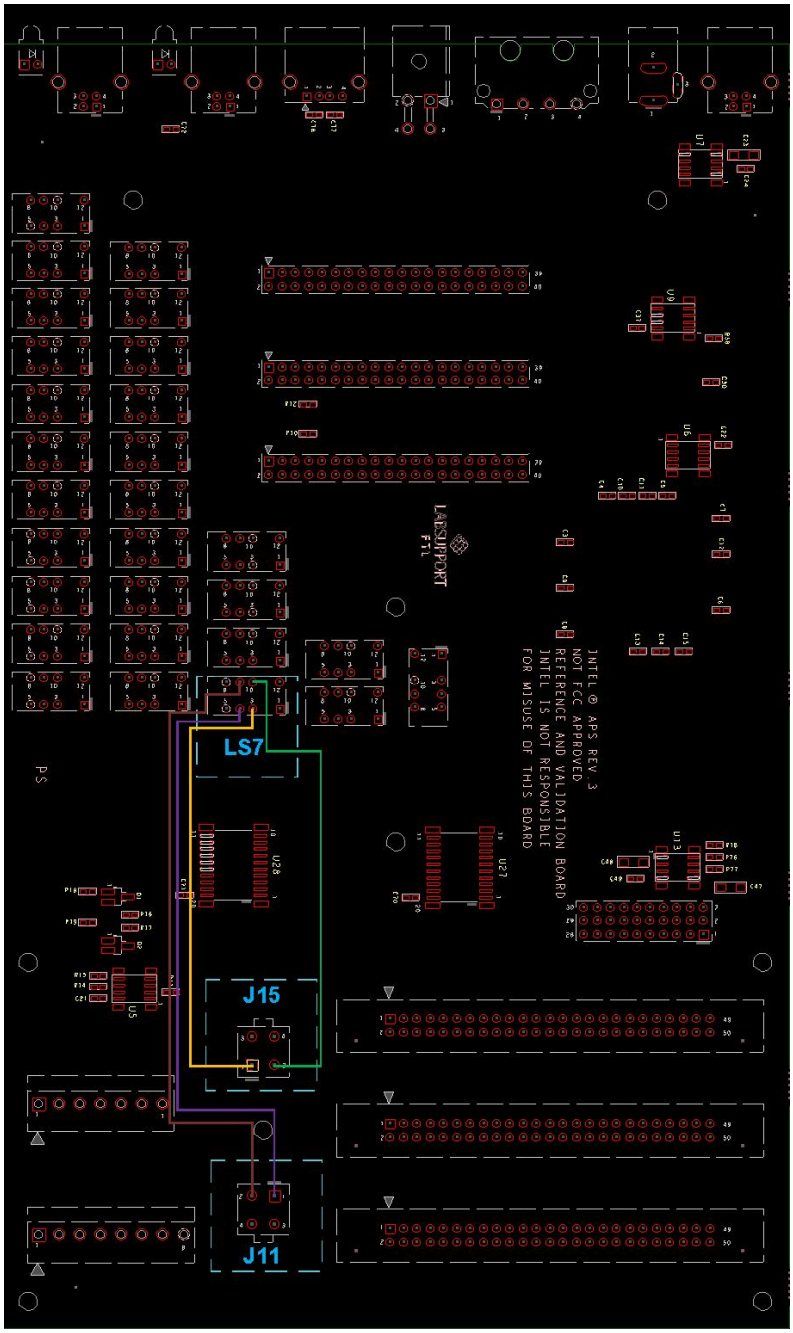
U.1 Issue Description

Issue was found on Intel® APS3 AC and DC switches of mobile platforms. Some mobile platforms can work not properly when DC /AC power supply is connected to SUT via Intel® APS3 due to current limitation of Intel® APS3. Customers which are using this capability should rework their Intel® APS3 device.

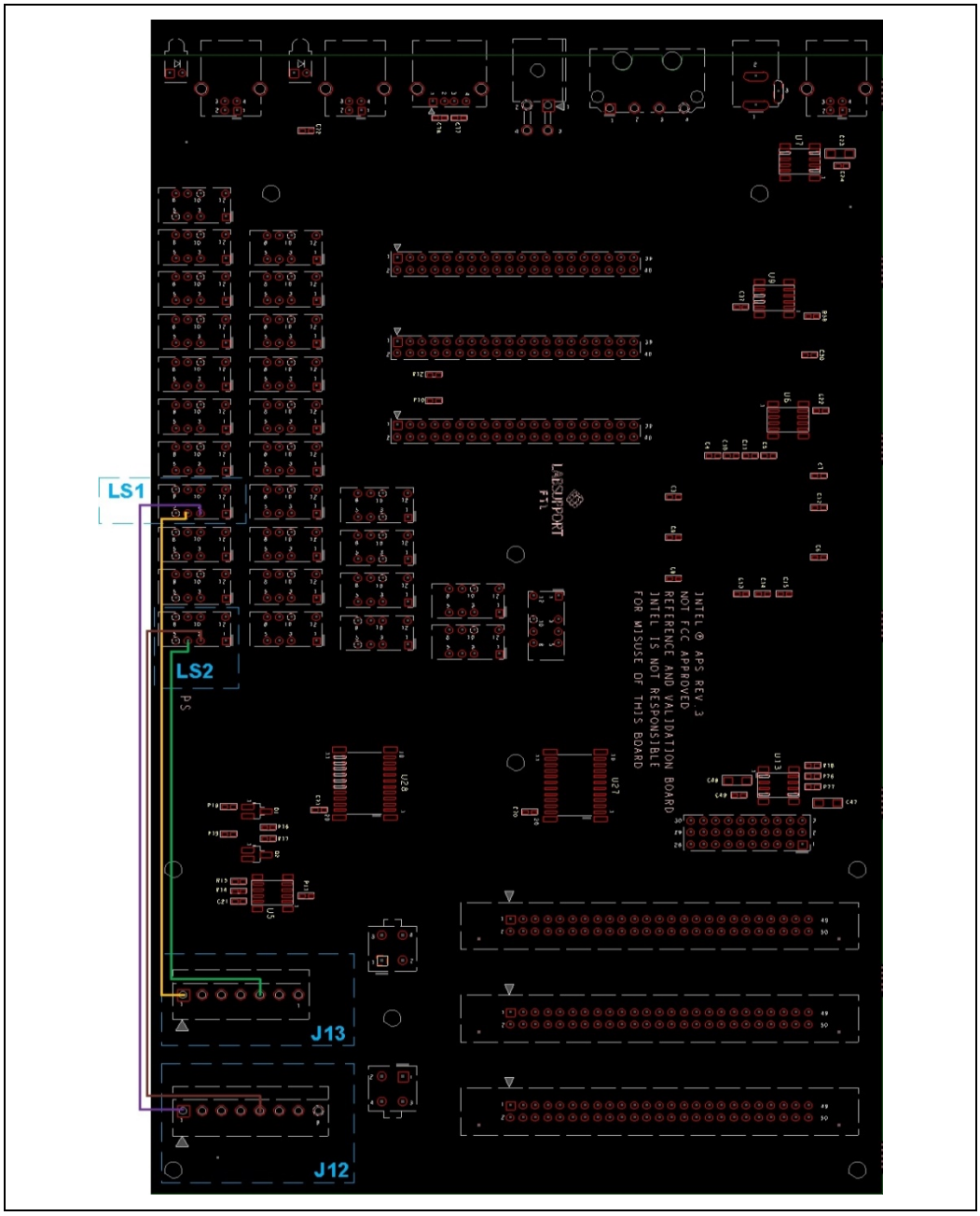
U.2 Rework Instructions

Connect the following parts on the bottom of the Intel® APS3 board by soldering 24” AWG wires:

1. **J15.1, LS7.3.**
2. **J15.2, LS7.10**
3. **J11.1, LS7.4**
4. **J11.2, LS7.9**


LS7
J15
J11
INTEL ® APS REV 3
NOT FCC APPROVED
REFERENCE AND VALIDATION BOARD
INTEL IS NOT RESPONSIBLE
FOR MISUSE OF THIS BOARD

5. **J13.1, LS1.4**
6. **J13.5, LS2.4**
7. **J12.1, LS1.3**
8. **J12. , LS2.3**


LS1
LS2
J13
J12

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Appendix V IMPORTANT SAFETY & REGULATORY INFORMATION

V.1 DO NOT DISCARD – DOCUMENT MUST REMAIN WITH PRODUCT

This symbol on the DSK indicates that the user shall refer to the documentation for important information regarding potential hazards and actions to be taken.

Mains (AC power), DSK input and output: 100-240 V~ 50/60Hz 5A maximum

Mains installation (overvoltage) category II (1500 V impulse)

Voltage fluctuation of +/- 10% maximum

V.2 General Operating Conditions

Indoor Use only, commercial or industrial locations

Ambient temperature: 5°C to 40°C

Relative Humidity: 80% up to 31°C, decreasing linearly to 50% at 40°C

Altitude 0 to 2000m

Pollution Degree 2 (normally only non conductive pollution occurs (dust, moisture) however temporary conductivity may occur)

To ensure safety connect APS3 Input/Output ports ONLY to devices which are Listed, Approved, or Certified as required for use in your region

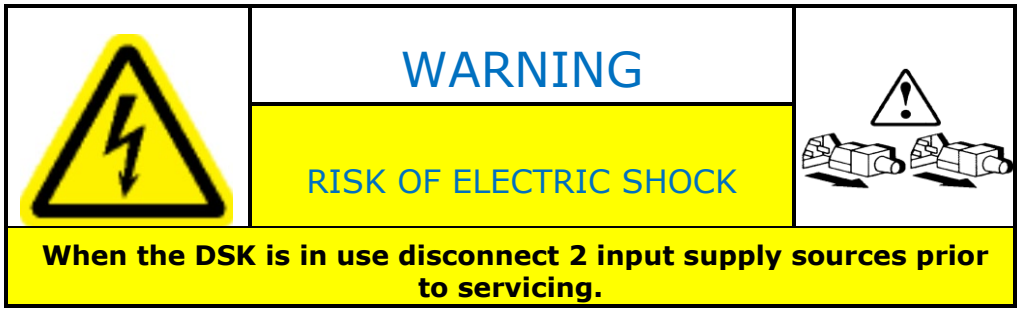
Mains Power Input/Output: Some types of Desk Top Systems (the System Under Test, SUT) may require more than 5 Amps. Prior to connecting the DSK to a SUT verify that the input current required is less than 5A at the mains voltage that will be used.

V.3 SAFETY WARNINGS

This symbol indicates risk of electric shock.

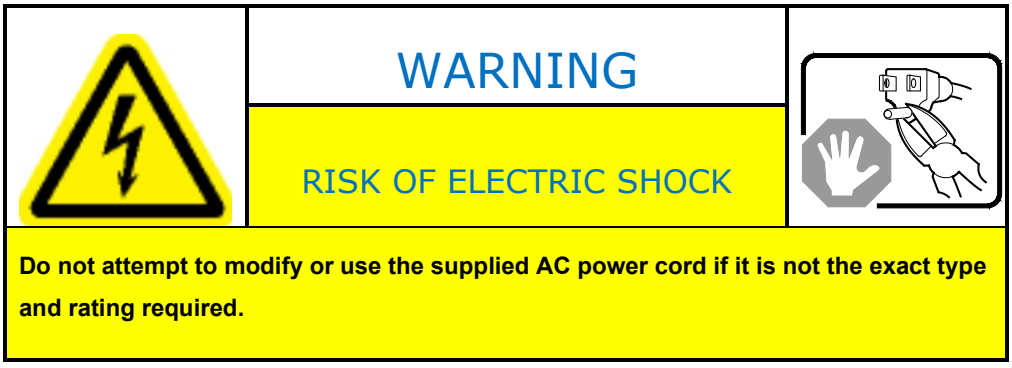
WARNING *Risk of electric shock*

No user serviceable parts inside. AC mains voltages are present within the power supply and the DSK assembly.



Power Connect and Disconnect: The mains (AC power) cords (APS3 Power Supply and DSK) are the primary disconnect device from mains (AC power) and to remove all DC power from the ASP 3 and SUT. The socket outlets shall be installed near the equipment and shall be readily accessible.

System Earthing (Grounding): To avoid shock, ensure that the power cords are connected to properly wired and earth grounded socket outlets. Ensure that any equipment to which this product will be attached is also connected to properly wired and earth grounded socket outlets.



Power Cord Requirements: The connector that plugs into the socket outlet must be a grounding-type male plug designed for use in your region. It must have certification marks showing certification by an agency in your region. The connectors that plug into the Appliance Inlets (AC receptacle) on the Intel® APS 3 must be an IEC 320, sheet C13, female connector. If the power cord supplied with the system does not meet requirements for use in your region discard the cord, do not use with adapters.

Lightning/Electrical Storm: Do not connect or disconnect any cables or perform installation or maintenance of this product during an electrical storm.

Risk of Fire: Cooling Requirements, Maintain a minimum clearance area of 5 centimeters (2 inches) around the side, front, and back of the product for cooling purposes; do not block ventilation openings in the front and rear panels.

V.4 FCC Statement

This equipment complies with FCC regulations by exemption as Industrial, Commercial or Medical test equipment (47 CFR 15.103) it is not intended for use in a residential location. This equipment generates uses and can radiate radio frequency energy which may result in harmful interference to radio communications. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment on and off, the user is required to take measures to eliminate the interference.

V.5 Electrostatic Discharge Warning

A properly grounded ESD wrist strap must be worn during installation of the system, connection of cables to the SUT. Failure to do so may damage components within APS or the SUT.

Lithium Battery: Risk of explosion if the lithium battery is replaced by an incorrect type. Observe proper polarity when replacing battery. Dispose of used batteries according to local regulations.

Perchlorate Material: Lithium Battery contains perchlorate material, special handling may apply. See www.dtsc.ca.gov/hazardouswaste/perchlorate. This notice is required by California Code of Regulations, Title 22, Division 4.5, Chapter 33: Best

Management Practices for Perchlorate Materials. This product includes a battery which contains perchlorate material.

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