Production Release Qualification Report

Intel® Core™ i3 Processor series
Intel® Pentium® Processor series

14nm Technology
1151 Lands FC-LGA12 Package
S step 4/3 MB Cache

Products included in this Production Release Qualification Report

Stepping	Product Name	S-SPEC	MM#	Core Freq	GT Freq
S	CM8066201927102	R2HE	945206	3.2 GHz	0.35 GHz
S	CM8066201927104	R2HF	945207	3.3 GHz	0.35 GHz
S	CM8066201927408	R2HN	945300	3.7 GHz	0.35 GHz
S	CM8066201927407	R2HM	945298	3.6 GHz	0.35 GHz
S	CM8066201926904	R2H9	945192	3.9 GHz	0.35 GHz
S	CM8066201926905	R2HA	945193	3.8 GHz	0.35 GHz
S	CM8066201927511	R2HR	945363	3.1 GHz	0.35 GHz
S	CM8066201927512	R2HS	945382	3 GHz	0.35 GHz
S	CM8066201927004	R2HD	945205	3.3 GHz	0.35 GHz
S	CM8066201927003	R2HC	945195	3.4 GHz	0.35 GHz
S	CM8066201927319	R2HJ	945269	3.5 GHz	0.35 GHz
S	CM8066201927204	R2HH	945261	3.8 GHz	0.35 GHz
S	CM8066201927202	R2HG	945208	3.7 GHz	0.35 GHz

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1.0 INTRODUCTION

This report covers the data collected to fulfill Production Release Qualification (PRQ) requirements for the Intel® Core™ DT Processor.

The Intel® Core™ DT Processor has been validated against the PRQ Quality and Reliability Verification requirements set forth in the Intel® Product Qualification System for the use-conditions that Intel has determined to represent the target usage segment(s) for Desktop PC.

1.1 Product Description

The 6th Generation Intel® Core™ Processor family on 14nm process is the next generation 64-bit, multi-core processor built on 14-nanometer process technology. The processor is designed for a two-chip platform. The two-chip platform consists of a processor and a Platform Controller Hub (PCH) and enables higher performance, lower cost, and easier validation. The processor includes Integrated Display Engine, Processor Graphics, PCI Express ports, and an Integrated Memory Controller. Intel® 6th Generation Core Processor enables improved CPU and graphics performance with significant power reduction and increased battery life.

2.0 QUALITY AND RELIABILITY VERIFICATION

The Intel Quality and Reliability Verification (QRV) Process starts by defining the correct requirements early in the product design. It involves comprehensive product design and technology development integration, implementation of robust and controlled manufacturing processes and systems, and ultimately leads to Quality and Reliability Verification testing on the finished product.

This report documents the product QRV testing results. During QRV testing Intel uses both standards-based and knowledge-based qualification strategies to insure that Intel products are shipped with the highest quality while considering cost and practicality of these requirements. Intel uses industry accepted standards such as JEDEC and internally developed stress methodologies so that the products conform to the product quality and reliability requirements.

QRV stress tests were conducted on units that have completed the full manufacturing flow. In all cases, a failure is defined as a failure to meet datasheet parameters as measured by the appropriate production and/or engineering tester. QRV results are summarized in the following section with supporting experimental results in the subsequent pages.

3.0 SUMMARY OF QUALIFICATION RESULTS

Intel® Core™ DT Processor

3.1 Use Reliability

Active & Inactive Operation→	0-1 Year	0-3 Years	0-5 Years
	FIT	FIT	FIT
Estimated	262	110	74

3.2 Outgoing Quality

Indicator	Results
Outgoing Quality Assurance	873

3.3 Qualification Summary

Stress	Spec #	Stress Condition	Results
ESD – Human Body Model	JS-001-2014	±1000 V	0/9 units
ESD – Charged Device Model (Non-Performance Pins)	JESD22-C101	±500 V	0/9 units
ESD – Charged Device Model (Performance Pins)	JESD22-C101	±250 V	0/9 units
Latch-up – Vcc	JESD78	1.5x VCC max DC	0/9 units
Latch-up – I/O	JESD78	±100 mA	0/9 units

3.4 Operating Reliability

Stress	Spec #	Stress Condition	Readout 1	Readout 2	Readout 3
Infant Mortality Evaluation	JESD94	105c, 1.35v	12/1882 units @ 0.083 hrs	12/1430 units @ 1 hrs	16/1230 units @ 10 hrs
Extended Life Test	JESD94	105°C, 1.35 V	0/340 @ 1 hrs	0/340 @ 10 hrs	0/340 @ 25 hrs

3.5 Thermal Mechanical

Stress	Spec #	Stress Condition	Readout 1	Readout 2	Readout 3
Temperature Cycling	JESD22-A104	-55°C to 125°C (Condition B)	0/138 units @ 50 cyc	0/138 units @ 250 cyc	0/138 units @ 750 cyc
High Temperature Storage (Bake)	JESD22-A103	150°C (Condition B)	0/150 units @ 500 hrs	0/150 units @ 1,000 hrs	
Accelerated Moisture Resistance – Unbiased HAST	JESD22-A118	110°C / 85%RH (Condition B)	0/137 units @ 25 hrs	0/137 units @ 50 hrs	0/137 units @ 100 hrs

4.0 USE RELIABILITY ASSESSMENT METHODOLOGY

4.1 Overview

This section provides a basic explanation of Intel's use reliability assessment methodology.

Intel follows a consistent and robust methodology for validating our products and delivering them to the market. This process begins with Technology Certification and reaches completion after product qualification when we grant Production Release Qualification (PRQ). Technology Certification focuses on validation of the package and silicon building blocks for our products. During this phase, the focus is on identifying possible failure mechanisms and risks associated with the technology. Evaluations are performed on package test vehicles and circuit level test structures to drive changes to material selection and the overall silicon and assembly process flow. During this phase very detailed failure models are developed for potential mechanisms that might be observed on the product. Upon completion of Technology Certification each product is required to execute a detailed Product Qualification in order to achieve PRQ. The product qualification focuses on validating that the product quality & reliability performance matches the technology model or baseline. This includes targeted evaluations to assess numerous product specific targets and goals, examples include Electrical Overstress (EOS), time-zero quality, and reliability failure characteristics.

Reliability failure characteristics are a function of time and usage. A technology baseline for each failure mechanism is derived using failure-mechanism testing, also known as knowledge-based testing as described in JEDEC Standard JESD94. This testing uses specific stresses that accelerate known failure mechanisms. The acceleration factors and time dependent (TTF) parameters are derived by including targeted use based evaluations in addition to unique accelerated stress conditions. Each failure mechanism type has a unique failure characteristic as a function of time and acceleration relative to use conditions as shown in Figure 1.

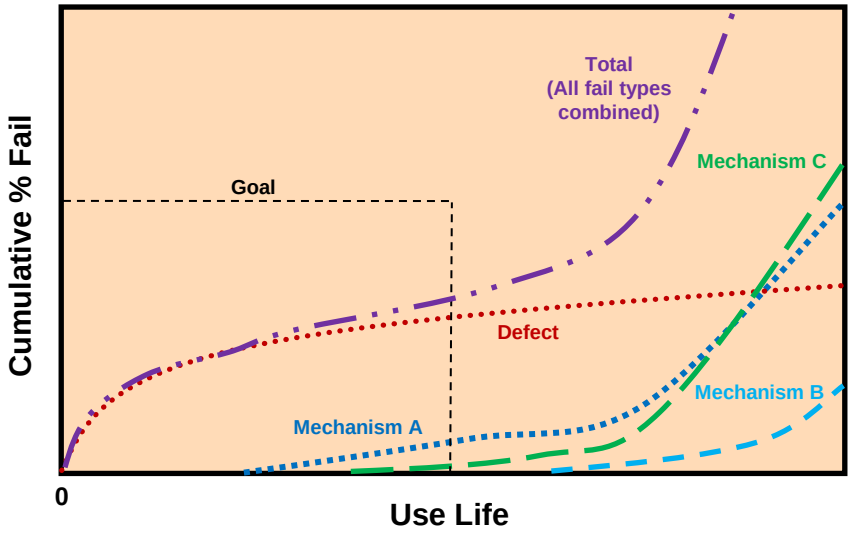


Figure 1: Example Failure Characteristics for Typical Defect and Intrinsic Failure Mechanisms.

As stated previously, this approach requires knowledge of the specific failure mechanisms and details on the target use conditions. Intel's long term product reliability is estimated by assessing each of the failure mechanisms at a reference use condition. The use condition consists of parameters associated with platform design, environmental conditions, and end-user behavior. The platform design parameters are outlined in the product datasheet. It is expected that the system meets all electrical and thermal requirements in the

datasheet since this bounds the operating region and defines the range of operating conditions assumed for the reliability assessment. For the environmental and end-user parameters, Intel has generated assumptions based on extensive data models of ambient conditions and component activity established by data acquisition projects under actual use environment.

The reference use model can vary depending on targeted usage and market segment. For the products included in this quality and reliability report, the reference use assumptions noted in Table 1 (section 4.2) are associated with compliance to the datasheet requirements. The reference use conditions are Intel's best estimate of operation variables within the datasheet representing a time averaged scenario. Operation of a population of units at or below these reference use conditions on average will ensure the product will continue to meet Intel's quality and reliability goals.

4.2 Use Condition Definition

Use Condition Segment: Desktop PC

Product: Intel® Core™ DT Processor

Category	Parameter	Value
Durations	Operating Time[3]	5 years (43800 hours)
Active Operation[1]	Time (%)	30%
	Junction Temperature[4], T_j (°C)	66
Inactive Operation[2]	Time (%)	70%
	Junction Temperature[4], T_j (°C)	40

Table 1: Product Reference Use Conditions[5]

Notes:

1. Active Operation means executing instructions; for multi-core product, equal core usage is assumed.
2. Inactive Operation equates to time spent in idle and/or standby states.
3. Operating Time is the accumulated modeled time in years that a product spends in either active operation (i.e., executing instructions) or inactive operation (i.e., time spent in idle and/or standby states).
4. The Junction Temperature T_j (°C) is the estimated weighted average die temperature based on the operating conditions (Active or Inactive) and the component within a system at the target use condition.
5. Reference Use Condition values are intended to represent the integration over time of reliability-related conditions seen over the life of the product in typical use, and are not the same as Product Datasheet limits. Sustained exposure to extreme use environments that significantly deviate from the use environment described in Table 1 may affect long-term component reliability.

The reference use conditions described in Table 1 are used in the Intel® Core™ DT Processor and are based on a Desktop PC environment that comprehends various types of computing models and form factors (e.g., blade, tower, notebook). These reference use conditions are used in conjunction with the reliability models to assess the product's reliability during use in a system.

4.3 Use Reliability

Use Reliability[1] Results:

Active & Inactive Operation→	0-1 Year	0-3 Years	0-5 Years
	FIT	FIT	FIT
Estimated[2]	262	110	74

Notes:

1. "Use Reliability" is based on a statistically meaningful population of devices operating continuously for the "Active & Inactive Operation" duration. Failure rates are not constant, so they are not linear functions of time.
2. The estimated Average Fail Rate (FIT) values represent projected component best estimates for a population of units, comprehending latent reliability defects and intrinsic failure mechanisms accelerated by the test evaluations documented in PRQ report. The first year of continuous operation is dominated by latent reliability defect failures.

The projected Average Failure Rate (FIT) for a given use time is provided to aid in system failure rate calculations. For system reliability budgets, the concept of failure rate budgets is valid for constant or time varying failure rates. It should be noted that Mean-Time-To-Failure or MTTF is computed from the reciprocal of failure rate as a reliability figure of merit. Generally MTTF and FIT are only valid for constant failure rates; however, Intel component failure rates are not constant nor are the resultant system failure rates.

5.0 OUTGOING ELECTRICAL QUALITY VALIDATION DPM

Description:
Outgoing Electrical Quality Validation measures the outgoing quality level by testing the electrical functionality and performance of the product before shipment. It is performed on material that has completed the standard production flow including assembly and electrical test.

Test Methodology:
The units are electrically tested using content and conditions which are comprehensive and specific to the product, which can include functional, structural and parametric content, as well as SKU-specific configuration testing.

Results:
Outgoing Electrical QV was completed on 13736 units across 48 production lots.

Outgoing Electrical Quality Validation

# of Lots	Product Name	Package	Results	DPM
48	CM806620192xxxx	FC-LGA12	12/13736	873

Failure Summary:
1) 12 functional failures

6.0 QUALIFICATION STRESS DETAILS

6.1 Electrostatic Discharge

Stress Description:

Electrostatic Discharge (ESD) testing is done to measure a device's sensitivity to electrostatic damage during handling. Human handling is simulated using the Human Body Model (HBM). This type of event occurs when a person transfers a charge from their body into a device. Intel uses ESDA/JEDEC joint standard JS-001-2014 in determining the appropriate HBM test conditions for each product. Mechanical handling is simulated using the Charged Device Model (CDM). This type of event occurs when a device accumulates charge during automated handling and is discharged to a low resistance, low inductance ground plane. Intel uses JEDEC Standard JESD22-C101 to establish the appropriate non-socketed CDM test conditions for each product.

Stress Conditions:

HBM ESD testing is done using an automated ESD tester. A 100pF capacitor is discharged into the device through a 1.5 kΩ resistor. The units are stressed to both polarities and are zapped once for each polarity. Pin combinations used are consistent with Tables 2A or 2B in JS-001-2014.

CDM ESD testing is done using an automated ESD tester. The device is charged via induction, and the device is discharged to a ground plane through the pin under test which is contacted with a robotic driven probe. Each pin under test is discharged one time when the device is charged positively with respect to ground and one time when the device is charged negatively with respect to ground.

Parts are functionally and parametrically tested after stress using an automated tester. A failure is defined as any device failing to meet datasheet specifications.

Stress Results:

HBM ESD (JS-001-2014)
Classification Level: Class 1C

Lot ID	Product Name	Package	Step	Stress Voltage	Results
Y508093S	CM806620192xxxx	FC-LGA12	R	±1000 V	0/3
Y511035S	CM806620192xxxx	FC-LGA12	R	±1000 V	0/3
Y514046S	CM806620192xxxx	FC-LGA12	R	±1000 V	0/3
TOTALS:					**0/9**

CDM ESD (JESD22-C101)
Classification Level: Class C1
CDM ESD – Non-Performance Pins

Lot ID	Product Name	Package	Step	Stress Voltage	Results
Y508094S	CM806620192xxxx	FC-LGA12	R	±500 V	0/3
Y511036S	CM806620192xxxx	FC-LGA12	R	±500 V	0/3
Y514047S	CM806620192xxxx	FC-LGA12	R	±500 V	0/3
TOTALS:					**0/9**

CDM ESD –Performance Pins [A]

Lot ID	Product Name	Package	Step	Stress Voltage	Results
Y508094S	CM806620192xxxx	FC-LGA12	R	±250 V	0/3
Y511036S	CM806620192xxxx	FC-LGA12	R	±250 V	0/3
Y514047S	CM806620192xxxx	FC-LGA12	R	±250 V	0/3
TOTALS:					**0/9**

A. The performance pins are all I/O pins. For more information on the CDM ESD target levels please refer to JEDEC publication JEP157 (www.jedec.org)

6.2 Latch-up

Stress Description:

Latch-up testing is performed on CMOS technologies to check the sensitivity of the product to parasitic bipolar action, often referred to as Silicon-Controlled Rectifier (SCR) latch-up. Two basic tests are completed to evaluate latch-up on a product: Vcc latch-up and I/O latch-up. Vcc Latch-up checks the product's sensitivity to Vcc over voltage while I/O latch-up checks the product's sensitivity to voltage over and undershoot on device pins.

Stress Conditions:

Latch-up is performed on a functional tester in accordance to JEDEC Standard JESD78. The stress is performed at hot and room temperatures that meets the datasheet operating temperature. Icc measurements are taken before and after applying the stress, but without removing power. Post stress Icc measurements are compared to the pre-test results to check for latch-up conditions. Parts are functionally and parametrically tested after stress using an automated tester. A failure is defined as any device failing to meet datasheet specifications.

Stress Results:

Vcc Latch-up

Lot ID	Product Name	Package	Step	Trigger Vcc	Hot (temp°C)	Room (temp°C)
Y516039L	CM806620192xxxx	FC-LGA12	R	1.5x VCC max DC	0/3	0/3
Y514253L	CM806620192xxxx	FC-LGA12	R	1.5x VCC max DC	0/3	0/0
Y516017L	CM806620192xxxx	FC-LGA12	R	1.5x VCC max DC	0/3	0/0
TOTALS:					**0/9**	**0/3**

I/O Latch-up

Lot ID	Product Name	Package	Step	Trigger Icc	Hot (temp°C)	Room (temp°C)
Y515053L	CM806620192xxxx	FC-LGA12	R	100 mA	0/3	0/3
Y516017L	CM806620192xxxx	FC-LGA12	R	100 mA	0/3	0/0
Y516039L	CM806620192xxxx	FC-LGA12	R	100 mA	0/3	0/0
TOTALS:					**0/9**	**0/3**

Clamping voltage(s) for I/O Latch-up are VIH+0.5*(VIH-VIL) for positive trigger and VIL-0.5*(VIH-VIL) for negative trigger.

6.3 Infant Mortality Evaluation

Stress Description:

An Infant Mortality Evaluation (IME) is performed to assess the latent defect portion of the operating reliability failure rate. The IME uses burn-in stressing, which is also used to monitor and control production material. Data from the IME is used to establish the required production burn-in time and control limits and to assess the individual product's latent defect Early-Life health on its process technology. IME results and fail mechanisms are statistically compared to model predictions to validate that the product is predictable to the technology baseline model.

Stress Conditions:

Units are stressed using dynamic patterns running in a controlled environmental chamber at an elevated Vcc and junction temperature. Actual stress Vcc and junction temperature for a given unit depends on the unit's power and position in the environmental chamber. The mean and variation are set to provide the necessary acceleration relative to the datasheet specifications. Parts are functionally and parametrically tested during readouts using an automated tester. A failure is defined as any device failing to meet datasheet specifications.

Stress Results:

Infant Mortality Evaluation

Number of lots	Product Name	Package	Step	Tj target	Vcc target	0.083 hrs	1 hrs	10 hrs
9	FJ80662019xxxxx[B]	FC-PGA4	D	105°C	1.35 V	12/1882[1]	12/1430[2]	16/1230[3]
TOTALS:								

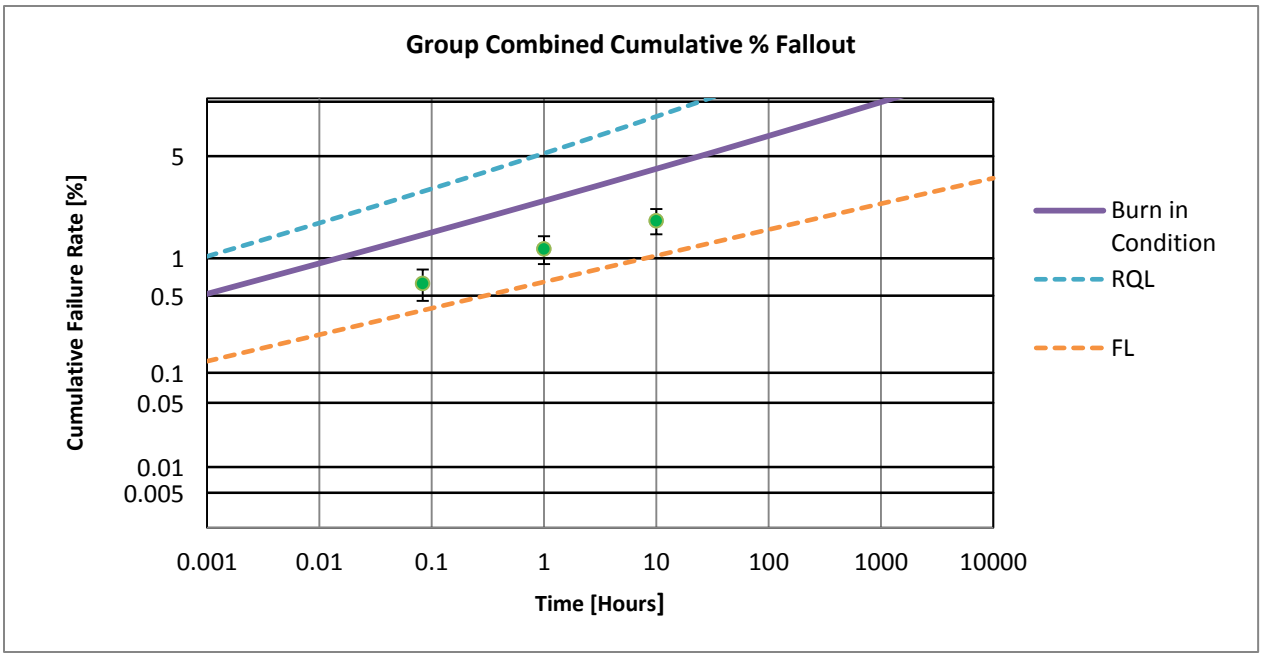
A. Material of SKL dual core was used, from 3 different fablots. Sample size reduction between readouts is caused by testing issues unrelated to Si failure modes.

B. This stress was performed on FJ80662019xxxxx processor and the results are being shared with CM806620192xxxx Processor quality and reliability verification. FJ80662019xxxxx and CM806620192xxxx processors share the same design and test coverage.

Failure Summary:

1) 3 functional, 9 parametrical failures
2) 2 functional, 10 parametrical failures
3) 4 functional, 12 parametrical failures

Infant Mortality Evaluation: Results Model Comparison



6.4 Extended Life Test

Stress Description:

Extended Life Test (ELT) is used to assess the intrinsic electrical portion of the operating reliability failure rate.

Stress Conditions:

Units are stressed using dynamic patterns running in a controlled environmental chamber at an elevated Vcc and junction temperature. Actual stress Vcc and junction temperature for a given unit depends on the unit's power and position in the environmental chamber. The mean and variation are set to provide the necessary acceleration relative to the datasheet specifications. Parts are functionally and parametrically tested during readouts using an automated tester. A failure is defined as any device failing to meet datasheet specifications.

Stress Results:

Extended Life Test

Lot ID	Product Name	Package	Step	Tj target	Vcc target	1hr	10hrs	25hrs
Y516232E	CM806620192xxxx	LGA	R[A]	105°C	1.35 V	0/170	0/170	0/170
Y516233E	CM806620192xxxx	LGA	R[A]	100°C	1.35 V	0/170	0/170	0/170
TOTALS:						**0/340**	**0/340**	**0/340**

A. This stress was performed on R-step processor and the results are being shared with S-step Processor quality and reliability verification-step and S-step processors share the same design and test coverage.

6.5 Temperature Cycling

Stress Description:

Temperature Cycling (T/C) is performed to evaluate the mechanical integrity portion of the intrinsic operating reliability failure rate. Mechanical failure mechanisms such as solder joint fatigue, package cracking, and ILD (Interlayer Dielectric) cracking in the die and package are accelerated by this stress.

Stress Conditions:

This test is conducted in conformance with the procedures defined in JEDEC Standard JESD22-A104. The devices are alternately exposed to -55°C to 125°C (Condition B) with a ramp rate of 15°C to 30°C per minute and a dwell time of 15 minutes. Heating and cooling are done by convection using temperature cycling chambers. Parts are functionally and parametrically tested during readouts using an automated tester. A failure is defined as any device failing to meet datasheet specifications.

Stress Results:

Temperature Cycling

Lot ID	Product Name	Package	Step	50 cycles	250 cycles	750 cycles
D438A803	CM806620192xxxx	FC-LGA12	P	0/36	0/36	0/36
D438A803A	CM806620192xxxx	FC-LGA12	P	0/102	0/102	0/102
TOTALS:				**0/138**	**0/138**	**0/138**

A. This stress was performed on P-step and the results are being shared with the S-step processor quality and reliability verification. P and S stepping's mechanical designs and materials are equivalent.
B. Material sampled from multiple fab and assembly lots.

6.6 High Temperature Storage (Bake)

Stress Description:

A High Temperature Bake, with no applied electrical bias, is performed to evaluate the thermal integrity portion of the intrinsic operating reliability failure rate. The bake evaluation accelerates failure mechanisms such as single bit charge loss, bond degradation, ionic contamination, contact integrity, and metal void propagation.

Stress Conditions:

This test is conducted in conformance with the procedures defined in JEDEC Standard JESD22-A103 at an elevated temperature of 150°C (Condition B). Parts are functionally and parametrically tested during readouts using an automated tester. A failure is defined as any device failing to meet datasheet specifications.

Stress Results:

High Temperature Storage (Bake)

Lot ID	Product Name	Package	Step	500 hrs	1000 hrs
D438A805	CM806620192xxxx	FC-LGA12	P	0/66	0/66
D438A805A	CM806620192xxxx	FC-LGA12	P	0/84	0/84
TOTALS:				**0/150**	**0/150**

A. This stress was performed on P-step and the results are being shared with the S-step processor quality and reliability verification. P and S stepping's mechanical designs and materials are equivalent.
B. Material sampled from multiple fab and assembly lots.

6.7 Accelerated Moisture Resistance – HAST

Stress Description:

Highly Accelerated Stress Test (HAST) is a high temperature/high humidity stress performed on non-hermetic devices to evaluate the moisture reliability portion of the intrinsic operating failure rate. Typical failure mechanisms from this stress include corrosion of metal and contamination induced threshold shifts due to moisture.

Stress Conditions:

This test is conducted in conformance with the procedures defined in JEDEC Standard JESD22-A118 (Unbiased) . The devices are placed in an 110°C / 85%RH (Condition B) environment with no bias supplied. Parts are functionally and parametrically tested during readouts using an automated tester. A failure is defined as any device failing to meet datasheet specifications.

Stress Results:

Unbiased HAST

Lot ID	Product Name	Package	Step	25 hrs	50 hrs	100 hrs
D438A804	CM806620192xxxx	FC-LGA12	P	0/55	0/55	0/55
D438A804A	CM806620192xxxx	FC-LGA12	P	0/82	0/82	0/82
TOTALS:				**0/137**	**0/137**	**0/137**

A. This stress was performed on P-step and the results are being shared with the S-step processor quality and reliability Verification. P and S stepping's mechanical designs and materials are equivalent.

B. Material sampled from multiple fab and assembly lots.

7.0 ADDITIONAL REFERENCES

Product Datasheet

Document Title: Desktop 6th Generation Intel® Core™ Processor Family Datasheet, Volume 1 of 2

This document is available post product launch at www.intel.com and can be found by performing a generic search on the web page using the products S-Spec. The document is found under Product Documentation and then under Technical Documents.

Thermal and Mechanical Design Guidelines

Document Title: Document Title: SkyLake-S Thermal Mechanical Design Guide

This document is available post product launch at www.intel.com and can be found by performing a generic search on the web page using the S-Spec. The document is found under Product Documentation and then under Technical Documents.

Process certification document

Document Title: Intel® P1272 14nm Logic Technology Process Certification Report

The goal of this report is to provide customers with a reliability overview of Intel's CMOS logic processes used in the fabrication of the processor and platform controller hub. This will be relevant to the customer's Implementation of internal quality and reliability programs for products containing components manufactured using this technology.

This document is available upon request.

Package certification document

Document Title: Intel® FCLGA12 Package and Assembly technology Certification report

This report documents the results of the Intel FC-LGA12package-assembly technology reliability certification. Intel® FCLGA12package assembly technology consists of a functional silicon die that is flip-chip attached to an organic land grid array package

This document is available upon request.

MAS Document

Document Title: Manufacturing with Intel® Desktop Platforms Code Named SKYLAKE

Intel(R) Manufacturing Advantage Service program (MAS) is designed to enable manufacturing customers and mitigate customer manufacturing risks. The MAS program shares Intel learning and BKMs, and deploys customer training materials in presentation, video, webinar and other formats. The MAS training materials are published through Intel Learning Network (http://learn.intel.com) and other websites. Please consult with your Intel field representatives or visit http://www.intel.com/design/quality/, Discover Customer Manufacturing Enabling and/or, refer to Resources to view and download the ESD/EOS prevention, rework BKMs, board flexure and component strain limit, shipping and handling, or other manufacturing videos or presentations topics.

8.0 REVISION HISTORY

Version	Date	Comments
0	/28/2015	Initial release

Appendix A

PRODUCT CHARACTERISTICS

General Information

Product Name	Intel ® Core™ Processor
Device Description	Intel ® Processor in 1151 pin FC-LGA12 Package
Die Size	93.48 mm^2
Transistor Count	1.18 billion transistors
Memory	3/4 MB
I/O Count	Refer to datasheet
Vcc	Refer to datasheet
Icc	Refer to datasheet

PROCESS CHARACTERISTICS

General Information

Base Process Number	P1272
Process Name	14nm Logic
Fab Plant(s)[1]	Hillsboro, Oregon, USA; Ocotillo, Arizona, USA
Wafer Size	300 mm
Wafer Type	P –Epitaxially grown thin film on a P+ Si crystal substrate
Well Type	Dual well
Final Wafer/Die Thickness	370 um
Metal Layer Count	13 + 1 local contact routing

Gate Level Attributes

Gate Material	Dual work function metal stack
Gate Thickness	Not publicly disclosed
Thin Gate Oxide Thickness	Not publicly disclosed
Thick Gate Oxide Thickness	N/A
Minimum Gate Width	14 nm
Minimum Gate Pitch	Not publicly disclosed

Passivation Attributes

Passivation Material	Silicon nitride
Passivation Thickness	450 nm
Passivation Deposition	RECVD deposition technique
Die Overcoat Material	WPR (Wafer Passivation Resist)
Die Overcoat Method	Wafer Level

[1]Intel uses Copy Exactly methodologies to enable a Virtual Factory approach for Fab and Assembly/Test processes. Production sites may change during a product's manufacturing life, once appropriate certification and qualification have been accomplished to demonstrate output equivalence and compliance with applicable Quality & Reliability goals.

PACKAGE CHARACTERISTICS

General Information

Package Type	FC-LGA12
Assembly Plant(s)[1]	Penang, Malaysia and Vietnam
Ball Land or Lead Count	1151
Package Dimensions	37.5 nm x 37.5 nm
Lead Finish Material	NiPdAu
Land or Solder Ball Pitch	0.91
Flame Retardant Used	Package and Underfill Compliant with (UL94-V0)

[1]Intel uses Copy Exactly methodologies to enable a Virtual Factory approach for Fab and Assembly/Test processes. Production sites may change during a product's manufacturing life, once appropriate certification and qualification have been accomplished to demonstrate output equivalence and compliance with applicable Quality & Reliability goals.