Thunderbolt™ Release Notes For Maple Ridge (JHL8540, JHL8340)

Release Notes - NDA

May 2020

Revision 5.0

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Audience

This document intended for use by OEM developers, test and validation engineers, and system integrators.

Contents

Revision History

Revision Number	Description	Revision Date
4.0	Initial release for MR FW rev 4	March, 2020
5.0	MR FW rev 5	May, 2020

1   *Introduction*

1.1   Scope of Document

This document provides component level details of the downloaded release and the contents of each folder in the release.

1.2   Acronyms

Term	Description
TBT	Thunderbolt™
HR	Host Router
EP	End Point
AIC	Add In Card
PR	Port Ridge (Thunderbolt™)
FR	Falcon Ridge (Thunderbolt™ 2)
AR	Alpine Ridge (Thunderbolt™ 3)
TR	Titan Ridge (Thunderbolt™ 3)
MR	Maple Ridge (Thunderbolt™ 4)
GR	Goshen Ridge (Thunderbolt™ 4 Hub)
DP	Display Port
CM	Connection Manager
LC	Link Controller
HDCP	High-bandwidth Digital Content Protection
DB	Delta Bridge – TBT Retimer
BB	Burnside Bridge – TBT Retimer

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1.3 Naming Convention:

<project name>_<mode>_<Si stepping>_<image rev>.bin

For example
   <project name>:
      AR, TR, etc.
   <mode>:
      HR = Host Router
      EP = Endpoint
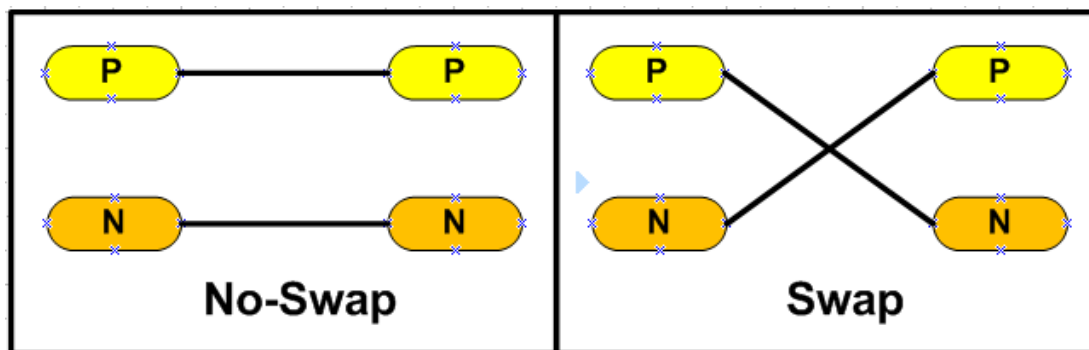   4C = 4 TBT channels (2 ports)
      2C = 2 TBT channels (1 port)

MR_HR_4C_A0_Rev10.bin - Maple Ridge Host Router Dual Port A0 stepping Revision 10

1.4 Lane N/P Swap Configuration

Note: Each revision might have different instructions on how to control board-dependent channels lanes N/P swap configuration.

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1.5 DP Sink Selection Preferences

1. For redrive of direct attach display, the preferred sink is selected by 0x51[0] for PA and 0x52[0] for PB. '0' - prefer sink 0. '1' - prefer sink 1

2. For DP tunneling over Thunderbolt to a remote display on the Thunderbolt cloud, the presence of the sinks is determined by writes in the CIO_EE2TAR section:

   a. The pointer for this section is located at offset 0xBF-C1 (relatively to active region)

   b. The structure of each write is described in the Maple Ridge datasheet

   c. In the DP-in ports (0x5, 0x6), register VSEC_DP_CS_50 (offset 0x81) bit 23 define GPU presence. If cleared the sink will not be used

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2   *Release Summary*

This document covers the following Thunderbolt™ Firmware for the Maple Ridge:

- Maple Ridge DP
- Maple Ridge SP

2.1   Release Overview

The release can be downloaded from **Intel VIP** (https://platformsw.intel.com/).

Note: Please use **Imaginarium2** latest version from **My Intel**.

Note: A username and password are required to access the website and to log in. User must have an account created for access.

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3 Features Supported

Supported = ✓ Limited Support = ⚠ Not Supported = ✗

Technology	Support
Thunderbolt™ Link 20/40G	✓
Thunderbolt™ Link Power Management (CLx)	✓
DP Redrive	✓
DP Tunnel	✓
MFDP out	✓
LTTPR	✓
DSC/FEC	✓
HDCP1.4	✓
HDCP2.2	✓
USB4	✓
USB 3 10G/5G	✓
USB2.0	✓
USB Wake	✓
PCIe traffic	✓
TBT Wake	✓
Sx	✓
RTD3	✓
Peer-to-Peer (P2P)	✓

3.1 Hardware Configurations

This release supports the following HW configurations:
- **MR DP:**
  o Sign default settings
- **MR SP:**
  o Sign default settings

3.2 Best Known Configuration

For the latest Client Based Platforms Best Known Configuration (BKC), please contact your platform CE.

4   *New Features–RCRs*

RCR #	Title	Change Info	Status

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5   *Issue Status Definitions*

This document provides sightings and bugs report for Thunderbolt™ Maple Ridge SKUs. At the time of a milestone release, this report will be distributed with the Intel® TBT Release and will provide information on new issues and the status of old issues (replacing the Release Notes document).

Closed Issues: This category will only display closed issues within the current Intel® Thunderbolt™ release. After each release, old issues will be dropped down to the "Archive" section and then new closed issues will take its place back up top for the next release. If an issue is posted in this section, it will indicate that the issue has been verified and fixed within the one that is being released.

Known Issues: This category will display all Known Issues since the initial release and will remain in this section until fixed or noted otherwise. "Known Issues" are still under investigation and may or may not be root caused.
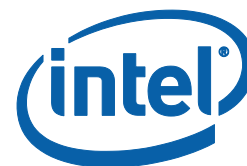
Archive – Fixes in Previous releases: This category will display all closed issues that were closed in their respected release#. This section will serve as a history of fixed issues.

Sightings listed in this document apply to the Thunderbolt™ Maple Ridge SKU's unless noted otherwise in this document or in the sightings tracking systems.

5.1 Closed Issues in this Release

Issue Closed in Release #	Title	Details	Affected SKUs
5	**YB after Sx**	**Sighting #:** 1307411108 **Affected Component:** USB **Impact**: GR gets YB after reboot/S4/S5 when TBT3 device is connected to GR Down Stream port **Workaround: none**	**All**
5	**YB after Sx**	**Sighting #:** 1307382339 **Affected Component:** USB **Impact**: MR gets YB after reboot/S4/S5 when TBT3 device is connected to Down Stream port **Workaround: none**	**All**
5	**CLx**	**Sighting #:** 1307067272 **Affected Component:** TBT **Impact:** Link is in CL0 after disconnected from Port A and B in CLx **Workaround:** none	**All**

5.2 Known Issues–To Date

Title	Details	Affected SKUs
Sx support with Cactus Ridge	**Sighting #:** 1307096350 **Affected Component:** LC **Impact:** After exit from Sx, there is no link with Cactus Ridge **Workaround:** none	**All**
Flashless is not supported	**Sighting #:** 1306729247, 1306731585 **Affected Component:** PCIe **Impact:** PCIe is not functional in flashlaess mode **Workaround:** none, will be fixed in B0 step	**All**
PERST INACTIVE indication over CIO to align USB4 spec	**Sighting #:** 1306856377 **Affected Component:** PCIe **Impact:** no functional failure , when PERST# is de-asserted the tunneled link goes back up. The PCIe upstream adapter on the other side gets TSs and exits the reset state but the USB4 spec calls for PERST inactive packets (PDF 0x6) on this state. **Workaround:** none, will be fixed in B0 step	**All**

5.3   Archive−Fixes in Previous Releases

Issue Fixed in Release #	Title	Details	Affected SKUs

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