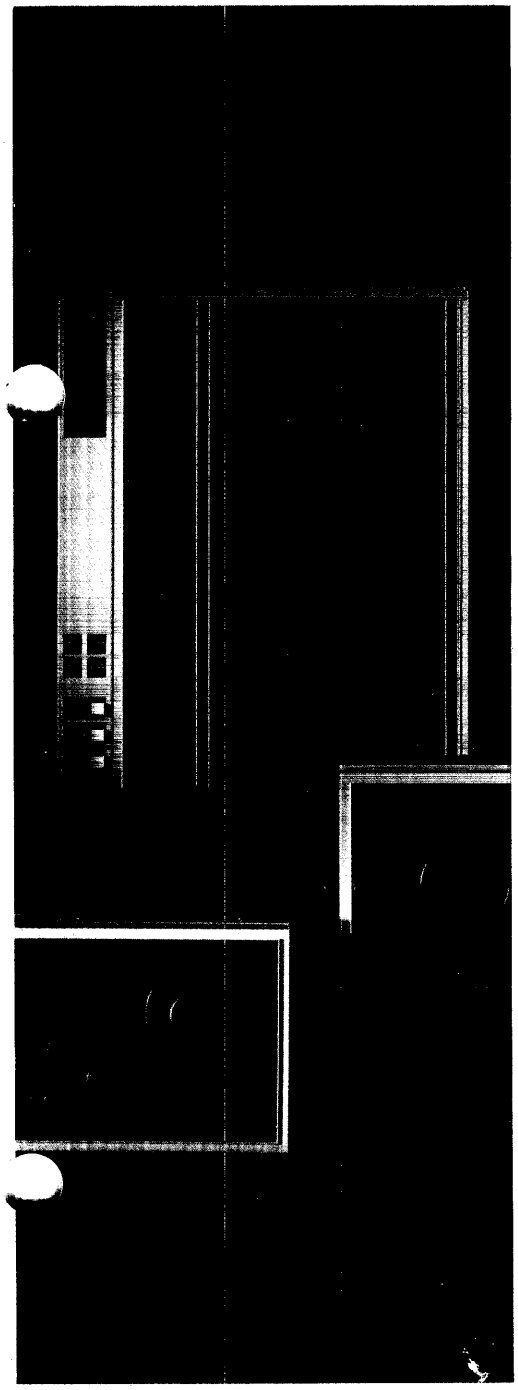
Operation and Maintenance Manual

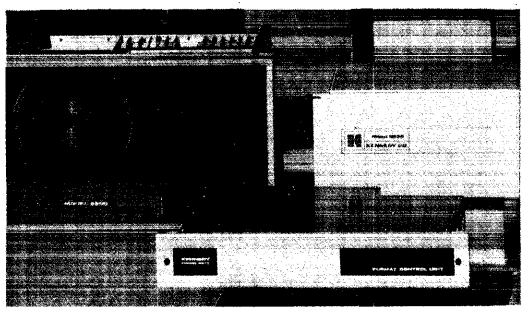
Model 9000

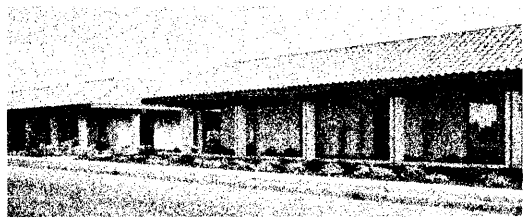
Digital Tape Transport

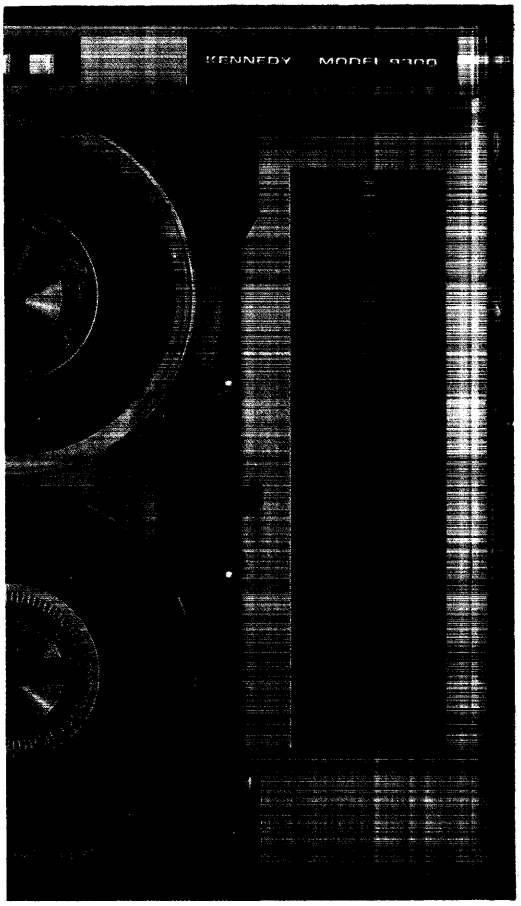
KENNEDY

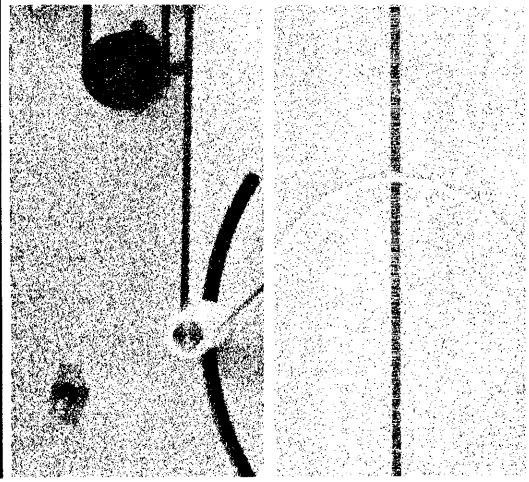
MODEL	PART NO.	INTERFACE
9000	192-9000-147	STD
SPEED	**DENSITY**	**TRACKS**
45 IPS	800/1600 CPI	9
MODIFICATIONS		
DENSITY SELECT SWITCH		

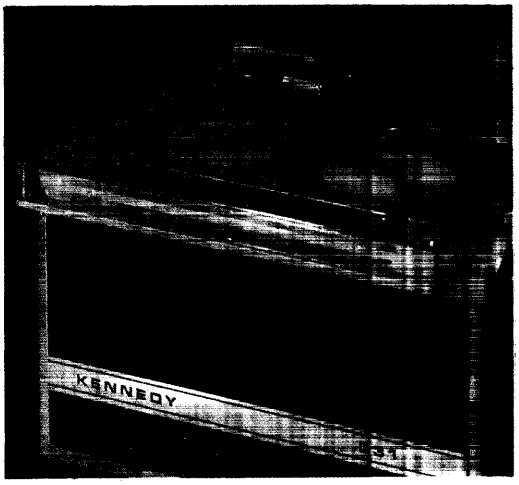












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ILLUSTRATIONS

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FCC CERTIFIED COMPUTER EQUIPMENT

Warning: This equipment generates and uses radio frequency energy and if not installed and used in accordance with the instruction manual may cause harmful interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment.

Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

SECTION I
APPLICATION DATA

SECTION I

APPLICATION DATA

1.1 INTRODUCTION

The Kennedy Model 9000 is a synchronous digital magnetic tape unit that with proper external formatting control is capable of reading and writing IBM compatible tapes, and is used in applications requiring high reliability at moderate tape speeds. Typical applications include operation with mini computers, high speed data collection systems, and computer peripherals.

The Model 9000 is equipped with the electronics necessary for reading and writing tapes and for controlling the tape motion. The head specifications and the mechanical and electrical tolerances of the Model 9000 meet the requirements for IBM compatibility. However, the formatting electronics, parity generator, cyclic redundancy check character(CRCC) generator, gap control, etc., are not included and must be provided by the tape control and formatter in order to generate properly formatted IBM compatible tapes.

The standard Model 9000 is available in 7 or 9 track NRZI and 9 track phase encoded recording configurations. Standard data recording densities are: 200/556 cpi or 556/800 cpi for 7 track NRZI, 800 cpi for 9 track NRZI, 1600 cpi for 9 track phase encoded and 800/1600 cpi for 9 track NRZI.

The standard tape speed is 25 ips; however, tape speeds from 10-45 ips are available. The data transfer rate at 25 ips, 800 cpi is 25 kHz.

The seven-track units are normally equipped for dual density, 556/800 bpi operation. Other combinations can be specified.

1.2 ELECTRICAL AND MECHANICAL SPECIFICATIONS

Tape (computer grade)
- Width . . . . . 0.5 inch (1.27 cm)
- Thickness . . . . . 1.5 mil (.038 mm)
- Tension . . . . . 8.0 ounces (227 gm)
- Reel diameter . . . . . to 10.5 inches (26.6 cm)
- Capacity . . . . . 2400 feet (731.5 meters)
- Reel hub . . . . . 3.69 inches (9.37 cm) dia per IBM standards

Reel braking . . . . . Dynamic
Recording mode (IBM compatible) NRZ1
Tape drive . . . . . Single capstan
Tape speed . . . 10-45 ips (25.4-114.3 cm/sec) 25 ips (63.5 cm/sec) standard

Instantaneous speed variation . . . . . ±3%
Long term speed variation . . . . . ±1%
Start/stop displacement 0.1875 inch (0.476 cm)
Start/stop time @ 25 ips . . . . . 15 ms
Rewind speed . . . . 150 ips (381 cm) (nominal)

Magnetic head assembly
(Write to read gap displacement)
- Dual gap 7 track read after write . . . . . 0.30 inch (0.76 cm)
- Dual gap 9 track read after write . . . . . 0.15 inch (0.38 cm)
- Interchannel displacement error . . (measured with IBM master skew tape PN 432362)
- Write (maximum) . . . . . 150 μinches (3.8 μm)
- Read (maximum) . . . . . 150 μinches (3.8 μm)

Erase head . . . . . Full width

Load point and end of tape reflective strip detection . . . . . Photoelectric (IBM compatible)

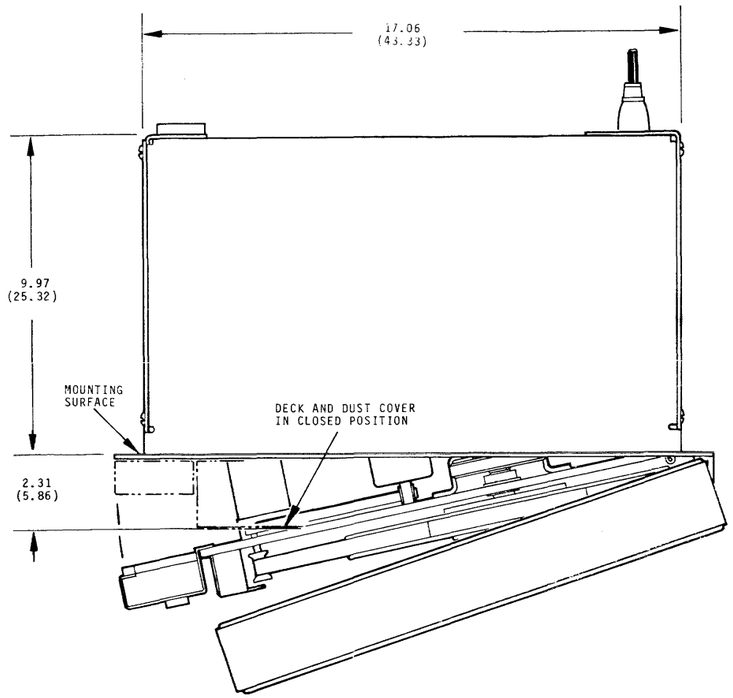
Broken tape detection . . . . . Photoelectric

Dimensions (see Figure 1-1)
- Transport mounting (vertical) . . . . . Standard 19-inch (48.26 cm) RETMA rack
- Height . . . . . 24.47 inches (62.15 cm)
- Width . . . . . 19.00 inches (48.26 cm)
- Depth (from mounting surface) . . . . . 10.62 inches (26.97 cm)
- Depth (overall) . . . 13.00 inches (33.02 cm)
- Weight . . . . . 90 pounds (40.77 kgm)
- Shipping weight . . . . . 105 pounds (48 kgm)

Operating environment
- Ambient temperature . . . . . $+2^{o}$ to $+50^{o}$C
- Relative humidity (noncondensing) . . 15% to 95%
- Altitude . . . . . to 30,000 feet (9120 m)

Power requirements . . . 115 or 230 vac (10%) 50 to 500 Hz, single phase
- Volt amps nominal 325
- Volt amps maximum 480

Table 1-1. Model 9000 Electrical and Mechanical Specifications

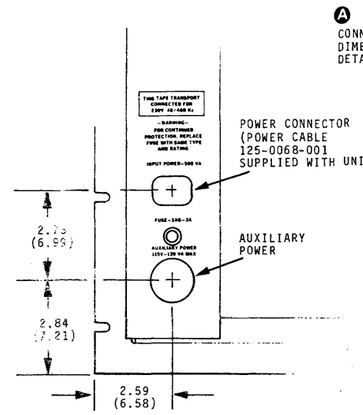


DUST COVER OPENS TO APPROX 120°
FOR ACCESS TO TAPE REELS

WARNING

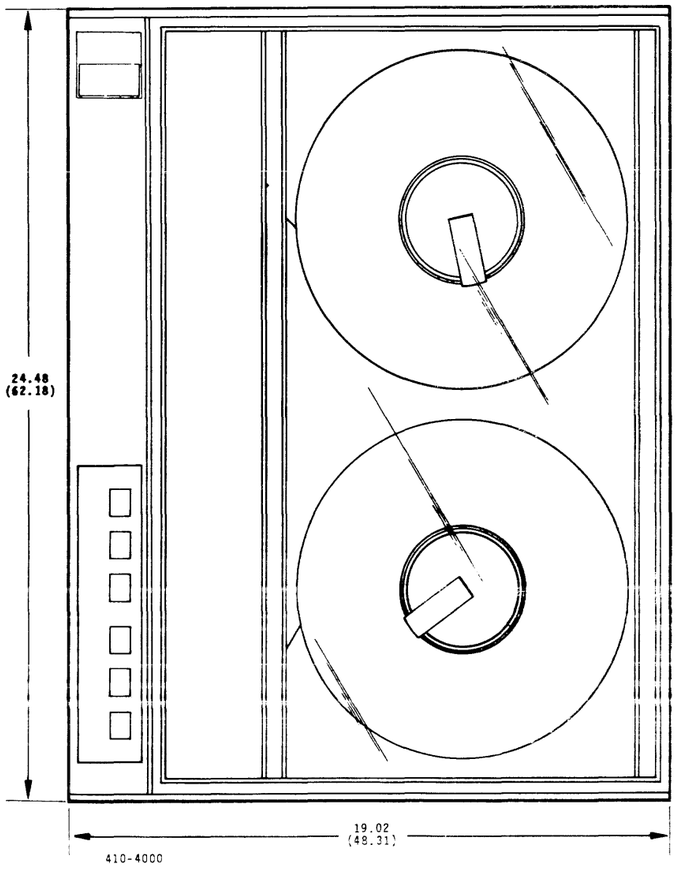
DUST COVER MUST BE FULLY OPENED
BEFORE OPENING DECK ASSEMBLY

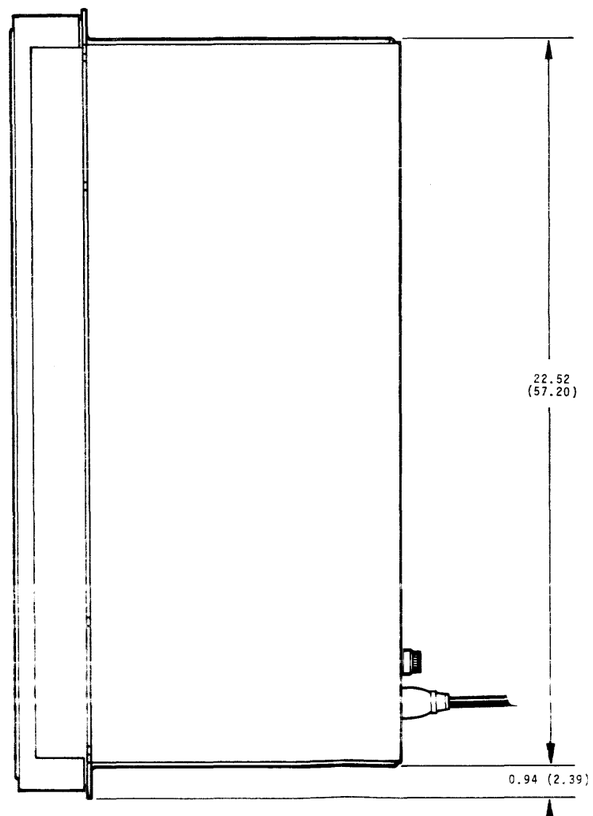
DECK ASSEMBLY OPENS TO APPROX 90°
FOR ACCESS TO TRANSPORT & ELECTRONICS



Ⓐ CONNECTOR LOCATION
DIMENSIONS (TYPICAL)
DETAILS FOR 230V OPERATION

FIRST DIMENSIONS SHOWN ARE IN INCHES.
DIMENSIONS IN PARENTHESES ARE IN CENTIMETERS.
UNLESS OTHERWISE SPECIFIED
DIMENSIONS SHOWN ARE NOMINAL.





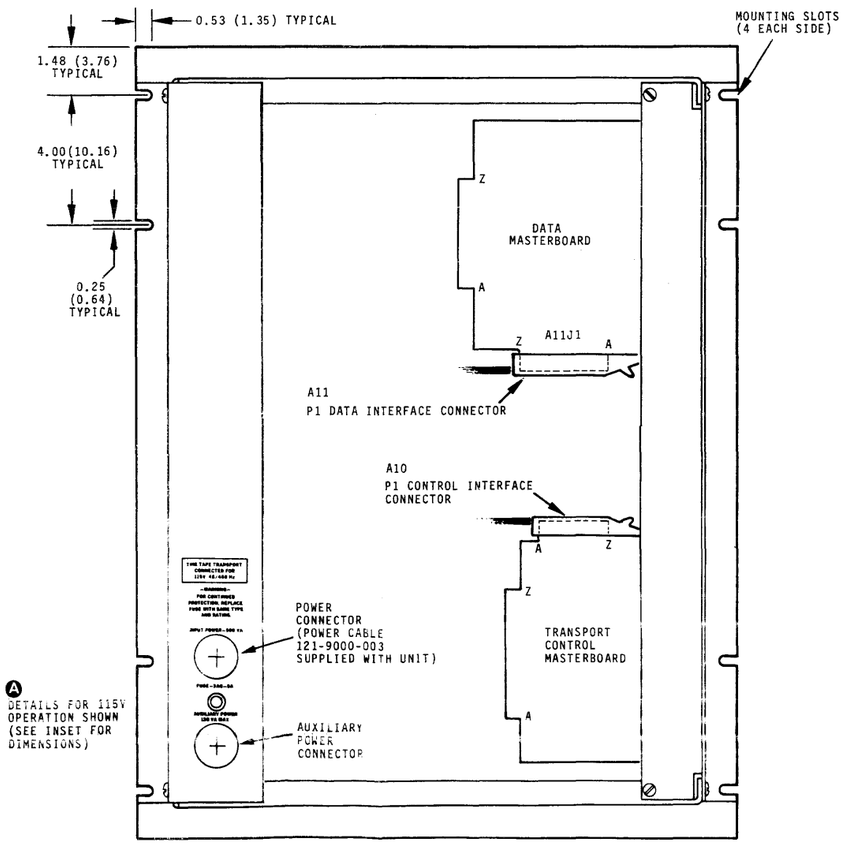
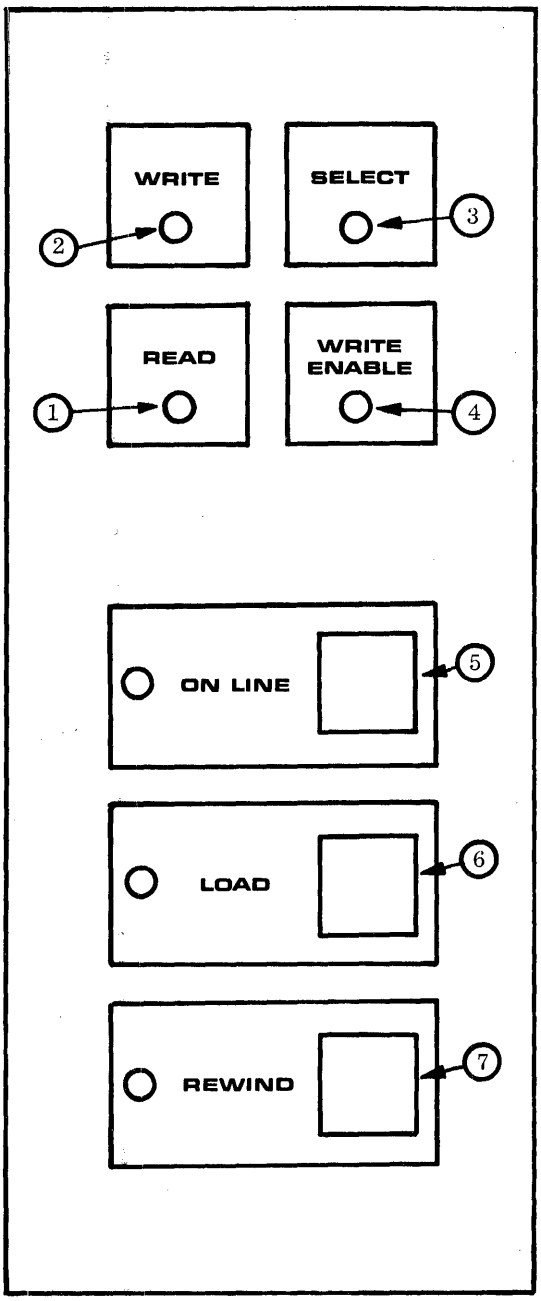


Figure 1-1.
Outline and Installation Drawing,
Model 9000

1.3 CONTROLS AND INDICATORS

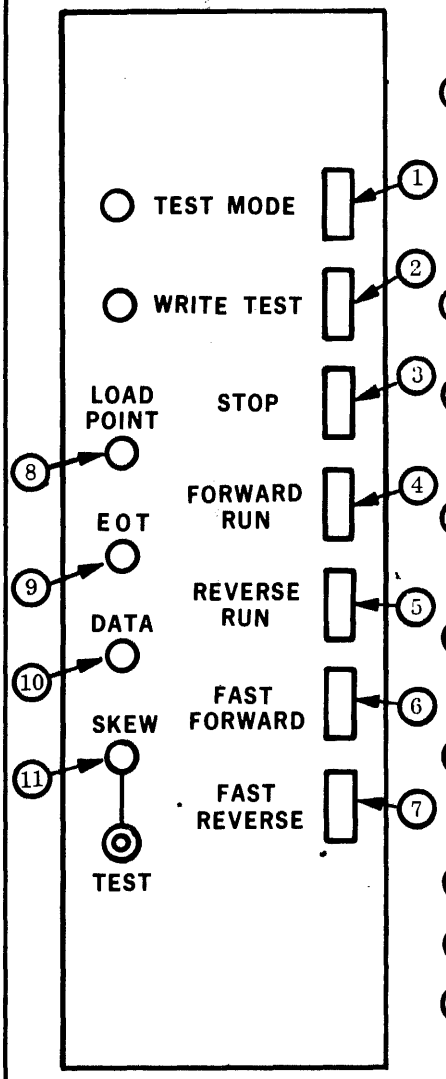
Controls and indicators provided on the Model 9000 formatted transports are shown in Figure 1-2. Each control function is explained in the figure. Model 9000 also contains a test panel, which is accessible by sliding the front panel nameplate. The control functions performed by the test panel are shown in Figure 1-3.



1. READ INDICATOR. Illuminated when tape unit is on line, selected, and read selected.
2. WRITE INDICATOR. Illuminated when tape unit is on line, selected, and write status selected.
3. SELECT INDICATOR. Illuminated when tape unit is on line and selected.
4. WRITE ENABLE INDICATOR. Illuminated whenever a reel with a write enable ring is mounted on the supply hub.
5. ON LINE. A momentary pushbutton, which functions as alternate action. When first activated the tape unit is placed in an on-line condition; when the tape unit is on line it can be remotely selected and will be ready if tape is loaded to or past the load point. When activated again it takes the tape unit off line. The indicator is illuminated in the on-line condition.
6. LOAD. The momentary pushbutton activates the reel servos (tensions tape) and starts the load sequence. The indicator is illuminated when the reel servos are activated and tape is tensioned.
7. REWIND. The momentary pushbutton activates a rewind operation. This control is enabled only when tape is tensioned and unit is off line. The indicator is illuminated during either a local or remote rewind operation.

LOAD and REWIND pushbuttons are disabled when the tape unit is on line.

Figure 1-2. Controls and Indicators



Note

Tape transport must be off line and STOP pushbutton depressed before test panel can become functional.

(1) TEST MODE pushbutton and indicator. A momentary pushbutton selects test mode and activates test panel. When indicator (LED) is illuminated, test panel is active. (Tape unit must be off line and STOP pushbutton depressed before test panel will function.)

(2) WRITE TEST pushbutton and indicator. A momentary pushbutton which programs 1's to be written on all channels in order to facilitate write skew adjustment. WRITE TEST remains active in FORWARD RUN mode only. (STOP pushbutton must be depressed and TEST MODE selected to actuate this feature.) The indicator (LED) will remain illuminated while unit is in this mode.

(3) STOP pushbutton. An interlocked pushbutton switch which terminates all tape motion.

(4) FORWARD RUN pushbutton. An interlocked pushbutton switch that allows tape unit to proceed forward at normal speed. Depressing STOP pushbutton or EOT marker will terminate this operation.

(5) REVERSE RUN pushbutton. An interlocked pushbutton switch which allows tape unit to run in reverse at normal speed. Depressing STOP pushbutton or BOT marker will terminate this operation.

(6) FAST FORWARD pushbutton. An interlocked pushbutton switch that allows tape unit to run forward at high speed. Depressing STOP pushbutton or EOT marker will terminate this operation.

(7) FAST REVERSE pushbutton. An interlocked pushbutton switch that allows tape unit to run in reverse at 150 ips. Depressing STOP pushbutton or BOT marker will terminate this operation.

(8) LOAD POINT indicator (LED). Indicates when tape is at load point.

(9) EOT indicator (LED). Indicates when tape is at EOT.

(10) DATA indicator (LED). Indicates when data is being processed by read/write electronics.

(11) SKEW indicator (LED) and TEST point. Indicator lights if tape skew exceeds the appropriate skew (read or write) gate setting. An oscilloscope TEST point is available for monitoring all read pulse outputs simultaneously, displaying total bit scatter.

Figure 1-3. Test Panel Controls and Indicators

1.4 INTERFACE CONNECTIONS

The interface connectors on the Model 9000 are designed for twisted pair inputs and outputs. For each active pin there is a ground pin. Two 44-pin edge mating connectors are supplied with the tape unit for interface connections. Connector P1 mates with A10J1, and P2 mates with A11J1.

1.5 INTERFACE SIGNAL CHARACTERISTICS

The tape unit responds to zero true inputs and provides zero true outputs. Each signal input is terminated in such a manner as to provide matching for twisted pair cables. See Figure 1-4. Each output line is driven with an open collector driver. For best results the typical interfacing circuit configurations shown in Figure 1-5 should be used. The recommended twisted pair cable will reduce the magnitude of intercable crosstalk. Unless otherwise specified all wires should be 24 AWG minimum, with a minimum insulation thickness of 0.01 inch. Each pair should have not less than one twist per inch and the input-output cables should not exceed 20 feet in length.

1.6 INPUT SIGNAL DESCRIPTION

The input receiver circuits, due to zero true current sinking logic design, will interpret a disconnected wire or removal of power at the transmitter as a logic zero or false condition. The logic 1, or true state, requires 25 ma current sink with less than 0.4v. The logic 0, or false state, will be 3v due to the input matching resistors (see Figure 1-4). The recommended input pulse width is 2 microseconds. The rise and fall times for pulses and levels must be less than 0.5 microsecond. Each input is enabled when the tape transport is on line and selected.

1.7 OUTPUT SIGNAL DESCRIPTION

Each output line is driven with an open collector current sinking logic driver which is capable of sinking up to 40 ma in the true state. All outputs are disabled (false) when the tape unit is not on line and selected.

1.8 TAPE MOTION COMMANDS

The tape transport capstan servo accelerates the tape to the required speed with a linear ramp. The tape is also decelerated to a stop with a linear ramp. Start and stop occurs within the interrecord gaps. The ramp time is 15 ms for 25 ips and varies inversely with tape speed. The amount of tape travel during the ramp up or ramp down is always 0.1875 inch.

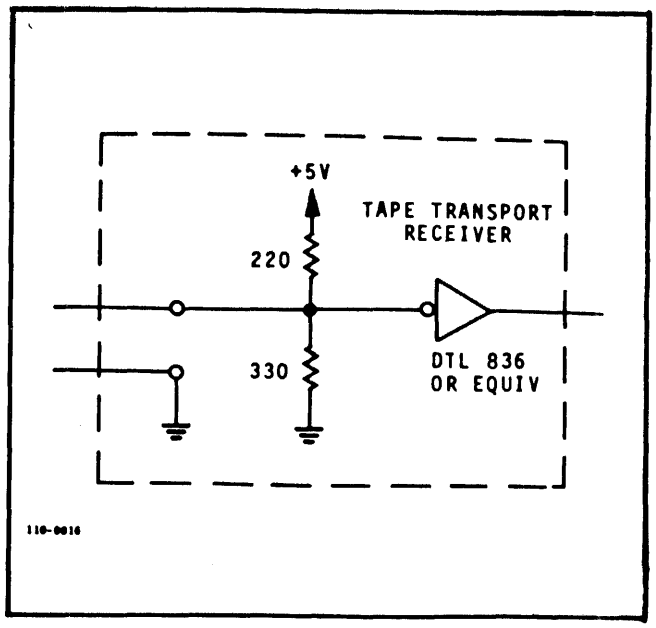


Figure 1-4. Typical Receiver Circuit

These two factors are to be taken into consideration when writing and gapping. A delay is required before writing to insure that tape is up to speed and to allow read after write. Timing diagrams for pertinent commands to provide properly formatted tapes are shown in Figures 1-6, 1-7, and 1-8.

Figure 1-6 shows the timing requirements for writing a block in a read after write system (dual gap head) in the write mode with read occurring immediately after writing. Figure 1-7 shows the timing requirements for reading a block on a read after write system in the forward direction. Figure 1-8 shows the timing requirements for reading a block on a read after write system in the reverse direction.

1.9 INTERFACE INPUT SIGNALS

All commands from and to the input/output connector are preconditioned by loading the machine and placing it on line using the front panel controls. The next commands set up the recorder.

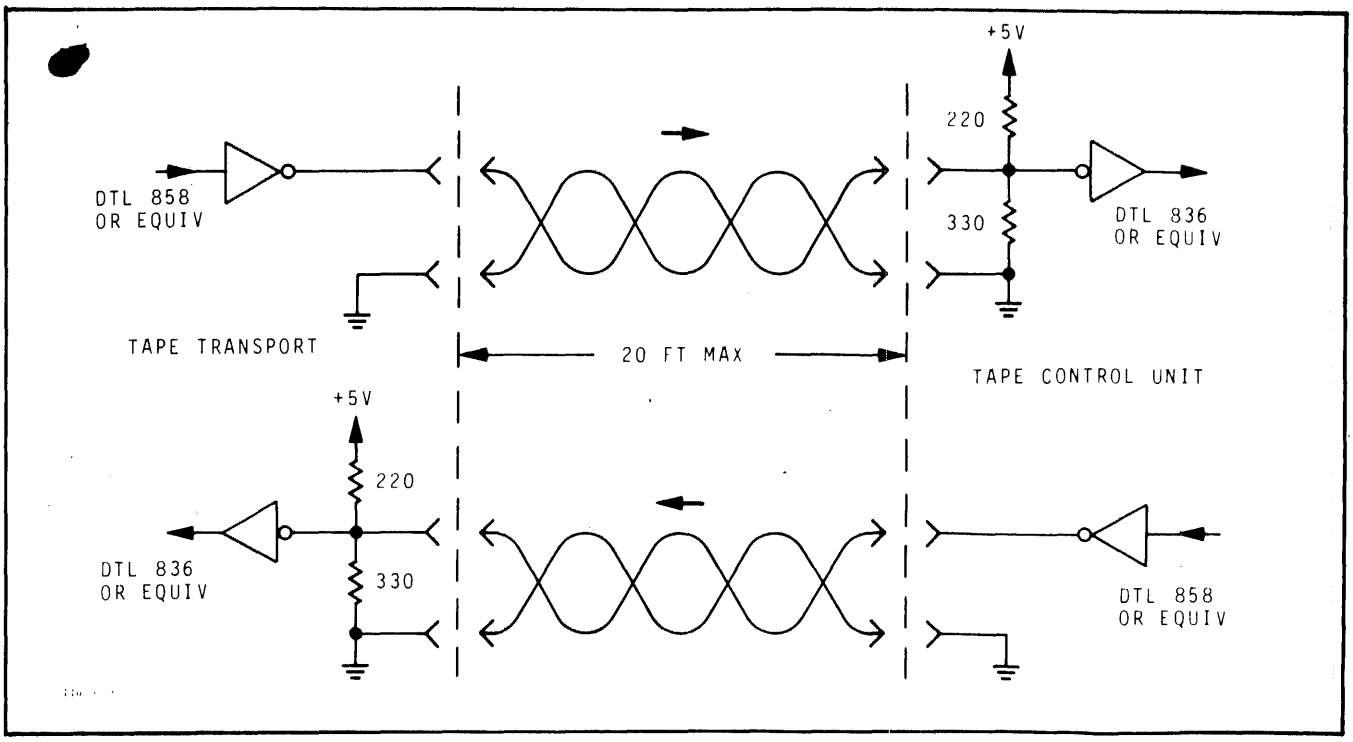


Figure 1-5. Typical Interface Configuration

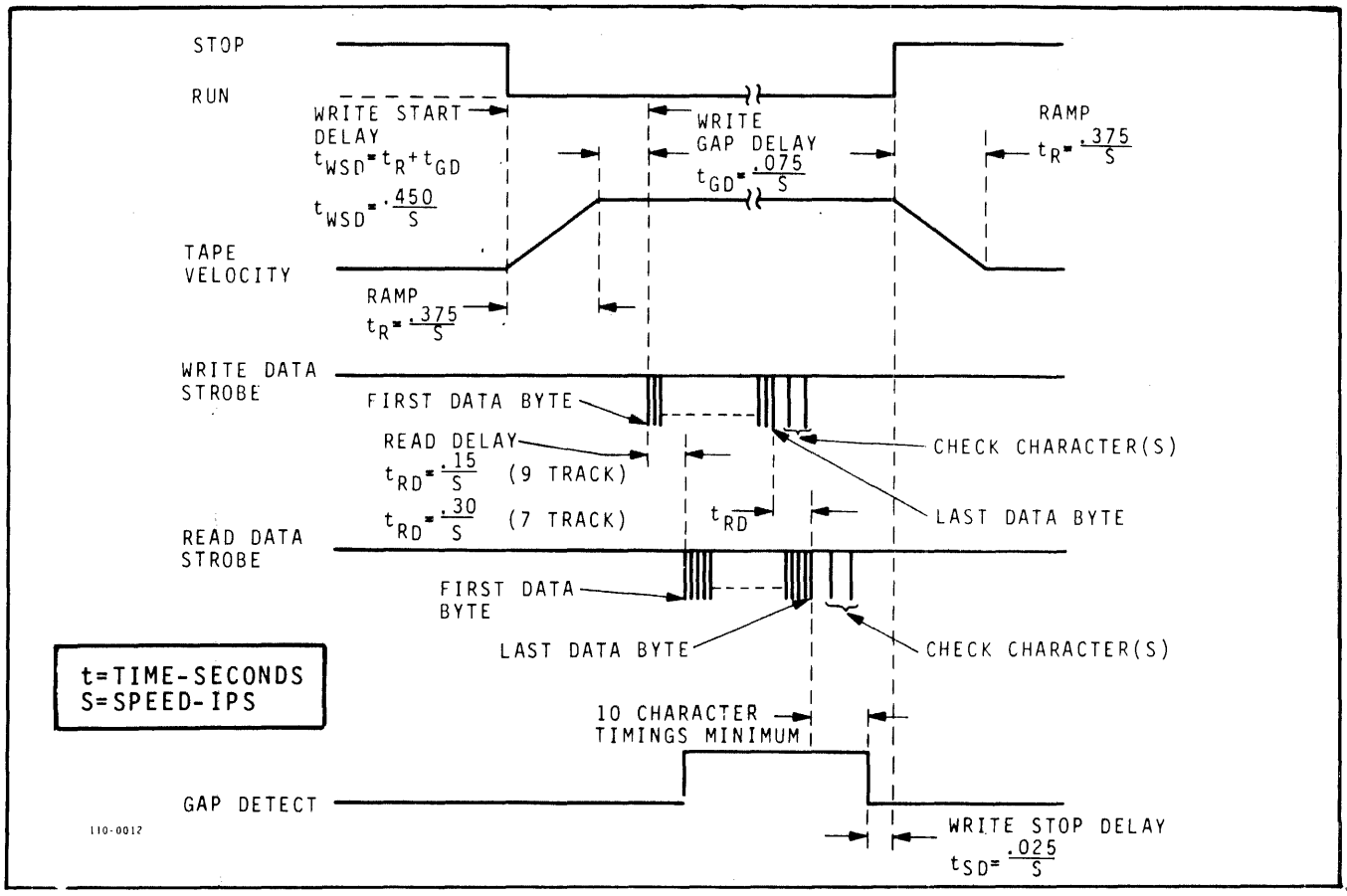


Figure 1-6. Read after Write Tape Transport Write Start and Stop Delays

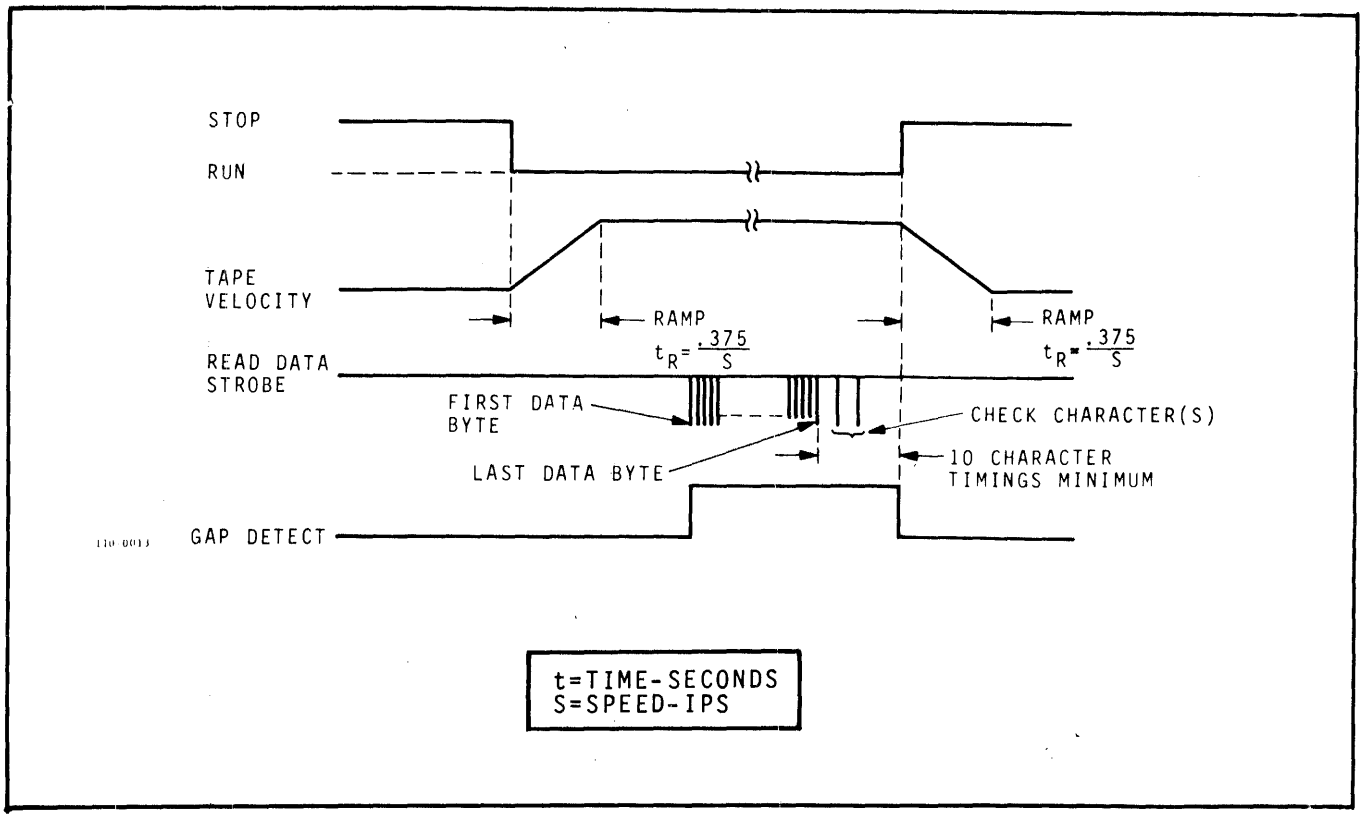


Figure 1-7. Read after Write Tape Transport Reading Forward

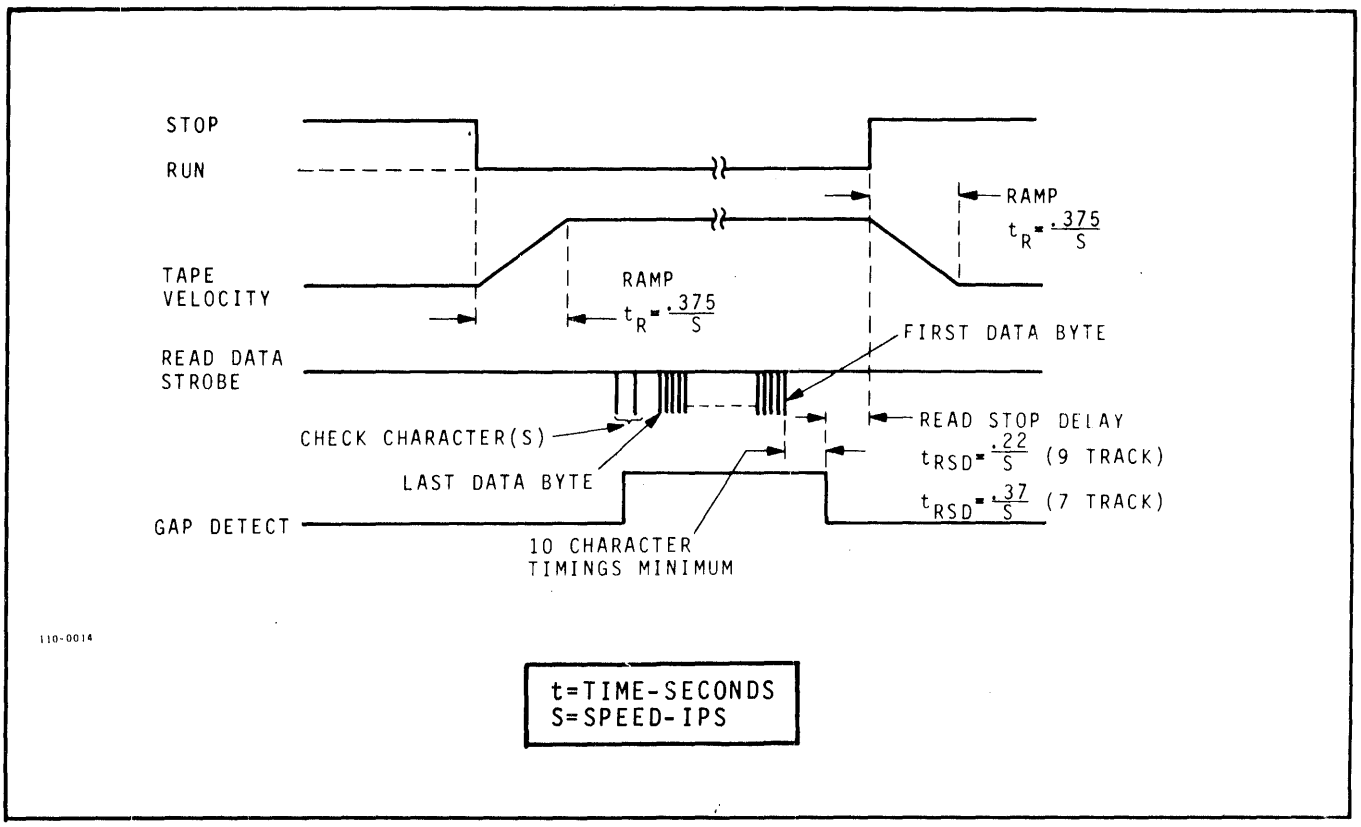


Figure 1-8. Read after Write Tape Transport Reading in Reverse

1.9.1 CONTROL COMMANDS

TRANSPORT SELECT

SLT	Level	P1-J

A level that when true enables all the interface drivers and receivers in the transport, thus connecting the transport to the controller. Transport must also be on line, and SLT must be true for the entire write sequence (until tape motion stops). The SLT level may be removed to disconnect the machine from the system. The machine will remain in the last condition established by SWS.

HIGH DENSITY SELECT

(7 track only)

HDS	Level	P1-D

Used when the TRANSPORT DENSITY SELECT switch is in the remote position. When true, this level selects the high read density (dual density).

OVERWRITE

OVW	Level	P1-B

A level that when true conditions appropriate circuitry in the transport to allow updating (rewriting) of a selected record. The transport must be in the write mode of operation to utilize the OVW feature.

SYNCHRONOUS FORWARD COMMAND

SFC	Level	P1-C

A level that when true, and the transport is ready and on line, causes tape to move forward at the specified speed. When the level goes false, tape motion ramps down and ceases.

SYNCHRONOUS REVERSE COMMAND

SRC	Level	P1-E

A level that when true, and the transport is ready and on line, causes tape to move in a reverse direction at the specified speed. When the level goes false, tape motion ceases. If the load point marker is detected during an SRC, the SRC will be terminated. If an SRC is given when the tape is at load point, it will be ignored.

REWIND COMMAND

RWC	Pulse	P1-H

A pulse input will rewind the tape past the load point and stop. The transport will then initiate a load forward sequence and return the tape to the load point marker. This input will be accepted only if the load point output is false. The transport may be taken off line while rewind is still in process. Rewind will continue normally.

1.9.2 WRITE COMMANDS

SET WRITE STATUS

SWS	Level	P1-K

A level that must be true at the leading edge of an SFC (or RUN and FWD) when the write mode of operation is required, and must remain true for a minimum of 10 μsec after the leading edge of the SFC (or RUN and FWD). SWS is sampled at the leading edge of the SFC or SRC (or RUN and FWD), toggling the read/write flip-flop to the appropriate state. Internal interlocks in the 9000 will prevent writing in the reverse direction, when the write enable ring is missing, when the tape unit is off line, when loading to a load point, and during a rewind.

WRITE DATA INPUTS

Nine Track	Seven Track	
WDP	WDC	P2-R
WD0		P2-S
WD1		P2-T
WD2	WDB	P2-U
WD3	WDA	P2-V
WD4	WD8	P2-W
WD5	WD4	P2-X
WD6	WD2	P2-Y
WD7	WD1	P2-Z

Nine lines are for nine-track operation, seven lines for seven-track operation. These are levels that if true at WDS time will result in a flux transition being recorded on tape (transport is in the write mode). Data inputs must have settled 0.5 μsec before the leading edge of the WDS pulse and must remain quiescent 0.5 μsec beyond the trailing edge of the WDS pulse. The CRCC is written by providing the correct data character together with a WDS four character times after the last data character of the record.

The LRCC is written using the WARS signal. The LRCC can also be written by providing the correct data character together with a WDS. If the LRCC is written (DATA WDS) in this manner a WARS should be given one character time after the LRCC to insure proper IRG erasure in case of DATA input error.

WRITE DATA STROBE

WDS	Pulse	P2-N

A pulse of 2 μsec nominal width for each character to be written. Writing occurs on the leading edge of

the WDS. WDS may be a 1 μsec minimum, 3 μsec maximum pulse. Data inputs must have settled for at least 0.5 μsec before the leading edge of WDS and remain quiescent for at least 0.5 μsec beyond the trailing edge.

WRITE AMPLIFIER RESET
WARS Pulse P2-P

A pulse of 2 μsec nominal width that, when true, resets the write amplifier circuits on the leading edge. The purpose of this line is to enable writing of the longitudinal redundancy check character (LRCC) at the end of a record. This insures that all tracks are properly erased in an interrecord gap (IRG).

In a seven-track system, the leading edge of the WARS pulse should be four character times after the leading edge of the WDS associated with the last data character in the block. In a nine-track system, the leading edge of the WARS pulse should be eight character times after the leading edge of the WDS associated with the last data character in the block (four character times after the CRCC is written).

1.9.3 READ COMMANDS

A read after write machine will always have read selected. When write is selected (SWS) the data just written will be read back using a high threshold level on the read amplifiers. When SWS is false the normal threshold is applied to the read amplifiers.

CLIPPING LEVEL DEFEAT
CLD Level P2-1

A level that when true overrides the automatic clipping level electronics and holds the read electronics in the normal clipping level mode.

1.9.4 SHUTDOWN COMMANDS

The use of a given magnetic tape unit may be terminated by an off line command. Once this command is given the tape unit may be returned to interface command only by operating the front panel ON LINE switch.

OFF LINE COMMAND
OFFC Pulse P1-L

A level or pulse (minimum width 2 μsec) that resets the on-line flip-flop to the zero state, placing the transport under manual control. It is gated only by SELECT in the transport logic, allowing an OFFC to be given while a rewind is in progress. An OFFC should be separated from a rewind command by at least 2 μsec.

1.10 INTERFACE OUTPUT SIGNALS

All output signals are enabled only when the tape transport is on line and selected.

1.10.1 STATUS OUTPUTS

ON LINE
ONL Level P1-M

A level that is true when the on-line flip-flop is set. When true, the transport is under remote control. When false, the transport is under local control.

TRANSPORT READY
RDY Level P1-T

A level that is true when the tape transport is on tape; that is, when the initial load sequence is complete and the transport is not rewinding. When true, the transport is ready to receive a remote command.

HIGH DENSITY INDICATOR
(7 track only)
HDI Level P1-F

A level that is true only when the high-density mode of operation is selected.

FILE PROTECT
FPT Level P1-P

A level that is true when a reel of tape without a write-enable ring is mounted on the transport supply reel.

WRITE ENABLE
WEN Level P1-S

A level that is true when a reel of tape with a write-enable ring is mounted on the transport supply reel. Opposite of file protect.

LOAD POINT
LDP Level P1-R

A level that is true when the load point marker is under the photosensor and the transport is not rewinding. After receipt of an SFC, the signal will remain true until the load point marker leaves the photosense area. (Circuitry using this output should not use the transitions to and from the true state.)

TAPE RUNNING
RNG Level P1-V

This is a level that is true when tape is being moved under capstan control and remains true until tape motion has ceased. (Includes forward, reverse, and rewind tape motion.)

END OF TAPE

EOT	Level	P1-U

A level that is true when the EOT marker is detected in the forward direction. Output remains true until the EOT marker is detected in the reverse direction.

REWINDING

RWD	Level	P1-N

A level that is true only when the transport is engaged in a rewind operation or returning to the load point. (Goes true approximately 5 μsec after a rewind command is given.)

1.10.2 READ OUTPUTS

Read outputs are present at all times in tape units when a dual gap head is used (read after write). The high threshold level is selected internally when SWS is selected.

READ DATA STROBE

RDS	Pulse	P2-A

A pulse of 0.5 μsec minimum width for each data character read from tape. Although the average time between two read data strobes is

$$\tau_1 \text{ (sec)} = \frac{1}{s \cdot d}$$

where

s = tape speed in inches per second

d = density characters per inch

the minimum time between consecutive read data strobes is less than this figure due to skew and bit crowding effects. A guaranteed safe value for the minimum time is $1/2\tau_1$.

READ GAP DETECT

RGAP	Level	P2-M

A level that is true approximately two character spacings after the last data byte, and remains true until the first data byte of subsequent data block. Note: This level will be true whenever tape motion is at rest.

READ DATA LEVEL

Nine Track	Seven Track	
RDP	RDC	P2-B
RD0		P2-C
RD1		P2-D
RD2	RDB	P2-E
RD3	RDA	P2-F
RD4	RD8	P2-H
RD5	RD4	P2-J
RD6	RD2	P2-K
RD7	RD1	P2-L

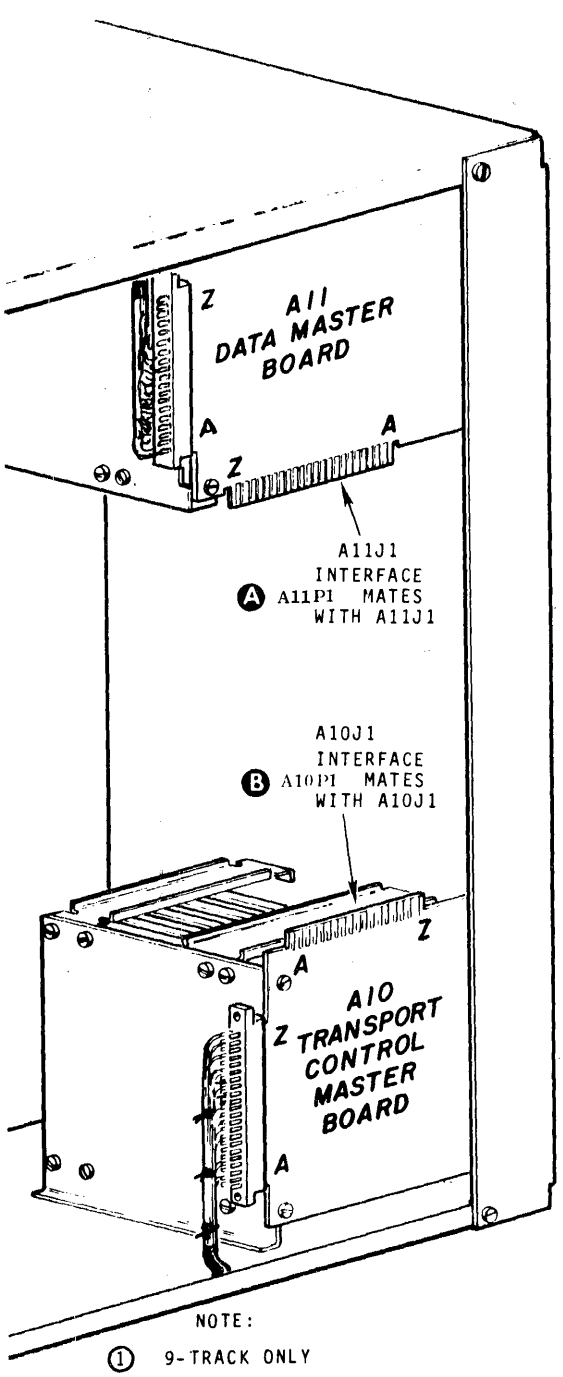
Nine lines, nine track; seven lines, seven track. Nine (or seven) staticisers are provided, which act as a one-stage read deskewing buffer. Each output is a level that changes to the appropriate state approximately 1 μsec before the read data strobe and remains in that state until 1 μsec before the next read data strobe. Data lines return to false condition in the IRG when tape motion stops regardless of the last character read.

It is recommended that read data strobes and the read gap detect be ignored during the first read or write operation from load point for τ_2 ms after the load point output goes false, where $\tau_2 = 1000/s$ (s = speed of tape unit).

The read gap in a read after write tape unit is downstream from the write gap. Thus, when the write gap is initially energized the read gap may detect a flux change depending on the initial state of magnetism on the tape.

1.11 SUMMARY OF INTERFACE

Figure 1-9 shows the location of connectors and pin numbers with signal names.



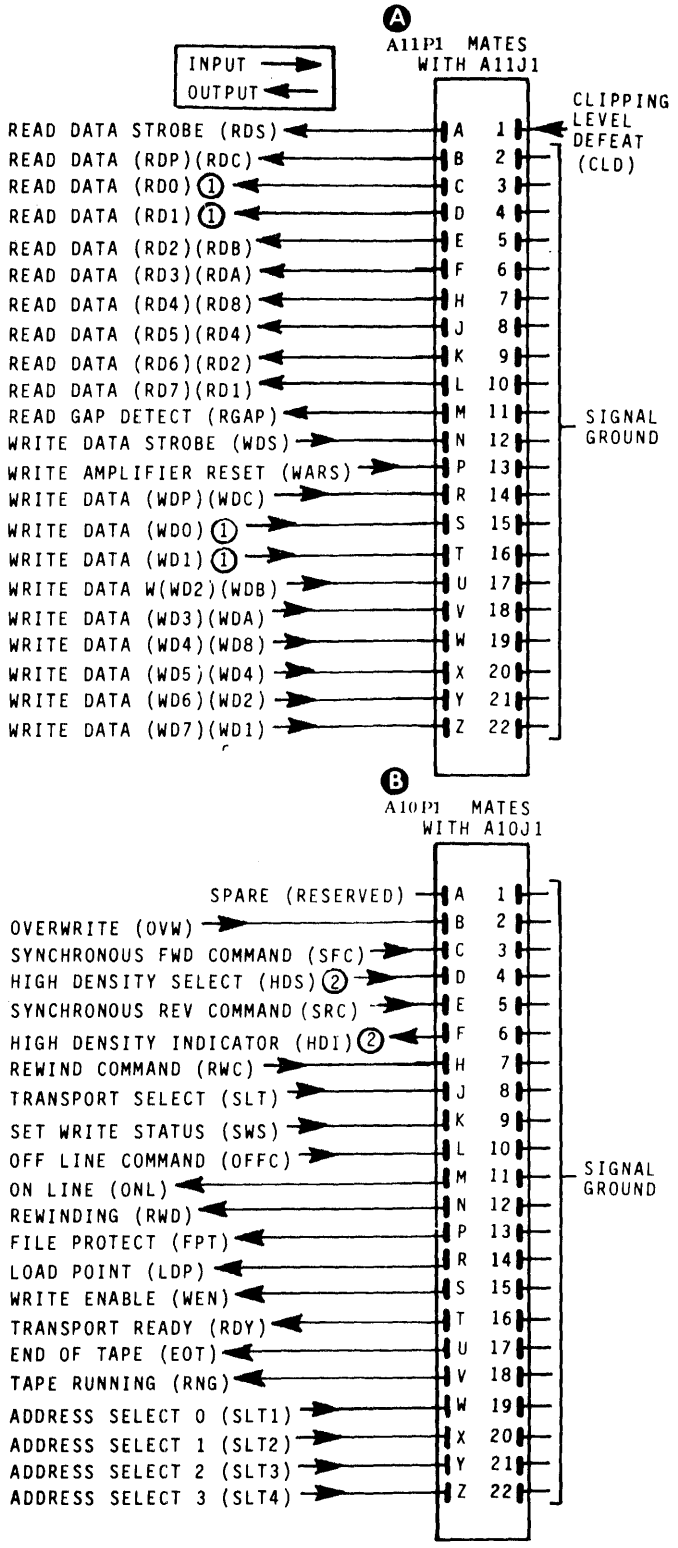


Figure 1-9. Interface Connection Summary

1.12 TAPE TRANSPORT DENSITY SELECT SWITCH

The Model 9000 now includes a density select switch as standard equipment. It is wired as indicated in Figure 1-10. This switch allows the generator to choose one of two tape character densities, such as 800/1600 cpi for 9 track, or 200/556 cpi for 7 track. The densities desired should be specified when ordering. The Dual Density Control Panel Assembly is numbered 190-2512-012. The slide switch is numbered 151-0033-001.

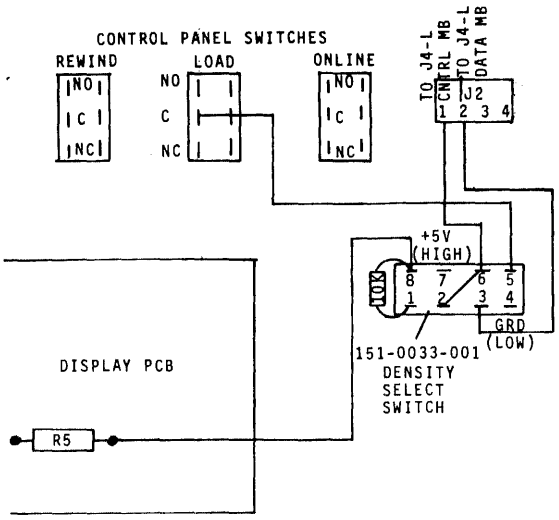


Figure 1-10

1.13 TAPE TRANSPORT ADDRESS SELECT SWITCHES

This option is essential in daisychain applications, where each transport in the chain must be assigned an address. Two address variations are currently available: 0-3 and 1-4. Kennedy part numbers for entire control panel assemblies and individual thumbswitches are:

0-3 Control Panel Assembly: 190-2512-011
0-3 Thumbswitch only: 151-0034-006
1-4 Control Panel Assembly: **190-2512-009**
1-4 Thumbswitch only: 151-0034-001

Switch wiring is indicated in Figures 1-11 and 1-12.

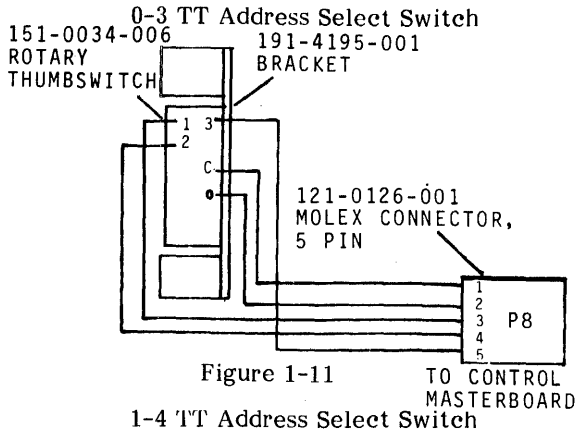


Figure 1-11

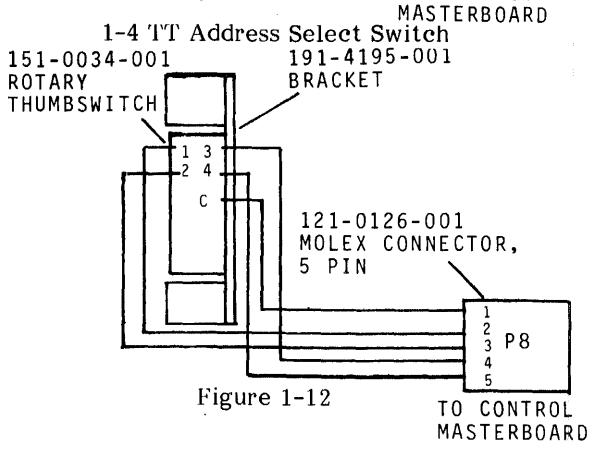


Figure 1-12

SECTION II
INSTALLATION AND OPERATION

SECTION II

INSTALLATION AND OPERATION

2-1 INSTALLATION

2.1.1 INSPECTION

Prior to installation, open the tape transport deck (paragraph 2.1.3) and inspect thoroughly for foreign material that may have become lodged in the tension arms, reel hubs, and other moving parts. After inspection, secure the deck and close the dust cover.

2.1.2 MOUNTING

Physical dimensions and outline of the tape transport are shown in Figure 1-1. The transport requires 24.5 inches of vertical mounting space in a standard 19 inch rack. Transports in a system configuration should be located so that there is no more than 20 feet of cabling between the Format Control Unit and farthest tape unit.

2.1.3 SERVICE ACCESS

CAUTION

The dust cover must be fully opened before opening deck.

The tape transport dust cover and deck are hinged at the right-hand edge (Figure 1-1). Open the dust cover and loosen the captive screw on the deck for access to all plug-in cards, control electronics, and the transport.

The power supply, voltage selection switch, fuse, power connector, interface connectors, and servo power amplifiers are accessible from the rear of the unit. For servicing the electronics, test points are provided by standoff pins on circuit boards and are identified by upper case letters near each test point.

2.1.4 INTERCABLING REQUIREMENTS

Installation of the tape transport requires fabrication of interconnection cables between the Format Control Unit and the tape transport. Cable connectors that mate with the card edge connectors on the units are supplied with the system. In units using a Multiple Transport Adapter three 36-pin edge connectors are supplied. In units without this option two 44-pin edge connectors are supplied.

The connector pin assignments are shown in Figure 1-9. Twisted pair cabling should be used to reduce intercable crosstalk. All wires should be 24 AWG, minimum, with a minimum insulation thickness of 0.01 inch. Each pair should have not less than one twist per inch, and maximum cable length should not exceed 20 feet.

2.1.5 POWER CONNECTIONS

A detachable power cord is supplied with the tape unit. The power cord is 7.5 feet long and has a NEMA three-prong (two power, one chassis) ground plug for connection to the power source.

CAUTION

Before connecting the unit to the power source, make certain that the power source voltage matches the voltage for which the transport is connected (115 vac or 230 vac). The transport voltage connection is indicated on a label located on the rear of the transport, near the power plug connection. Also ascertain that the proper fuse has been installed (5A 3AG for 115 vac, 3A 3AG for 230 vac).

2-2 OPERATION

2.2.1 INTERFACE

Before placing the unit in operation, make certain that the interface connection procedures outlined in Section I have been performed.

2.2.2 CONTROLS AND INDICATORS

Paragraph 1.3 lists the controls and indicators for the tape transport and describes the functions of each.

2.2.3 PRELIMINARY PROCEDURES

Before placing the unit in operation, proceed as follows:

a. Clean the tape transport read/write head, capstan, and idlers to prevent degradation of magnetic tapes.

b. Check for correct connection of line voltage on rear flange, and that correct fuse is installed (paragraph 2.1.5).

c. Set primary power switch on transport deck (behind dust cover) to ON.

2.2.4 TAPE THREADING

To thread the tape on the transport, proceed as follows:

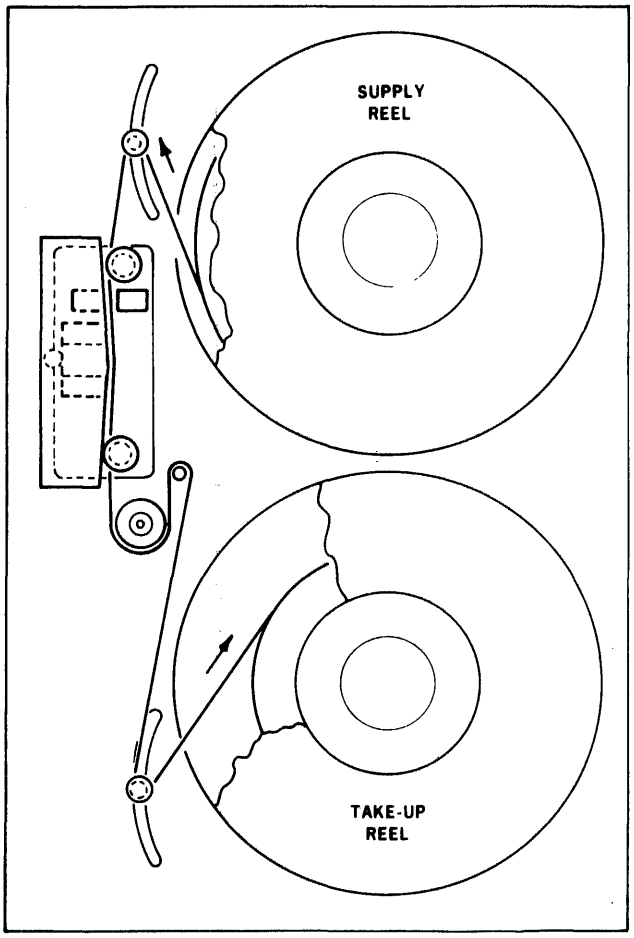


Figure 2-1. Tape Threading

a. Place the tape file reel to be used on the upper or supply hub (Figure 2-1) with the write-enable ring side next to the transport deck. Make certain the reel is all the way against the hub flange.

b. Secure the reel by rotating the hub knob clockwise while holding the reel.

c. Thread the tape along the path as shown by the threading diagram (Figure 2-1).

d. Holding the end of tape with a finger, wrap a few turns clockwise around takeup reel.

2.2.5 TAPE LOADING

Pressing the LOAD pushbutton energizes the reel servos and initiates a load sequence. Tape advances to the load point marker and stops.

If for some reason the load point marker is already past the sensor as, for example, in restoring power after a shutdown, tape will continue to move. Under these conditions, press REWIND and tape will rewind to load point.

Once pressed, the LOAD switch is illuminated and is inactive until power has been turned off or tape is removed from machine.

2.2.6 PLACING TAPE UNIT ON LINE

After the tape is properly threaded and has been loaded and brought to the load point, press the ON LINE pushbutton and check that ON LINE indicator illuminates. (LOAD and REWIND pushbuttons are disabled when the tape unit is on line.) On-line status enables the tape unit to be remotely selected and to perform all normal operations under remote control.

2.2.7 TAPE UNLOADING AND REWIND

Provision is made in the 9000-series transports for rewinding a tape to the load point under remote control. However, this operation may also be performed manually. Proceed as follows.

a. If the ON LINE indicator is illuminated, press the ON LINE pushbutton. Check that the indicator extinguishes.

b. Press the REWIND pushbutton. The tape will now rewind to the load point marker.

c. After the tape has been positioned at the load point under remote or local control, press the REWIND pushbutton to rewind the tape past the load point to the physical beginning of the tape.

NOTE

The rewind sequence cannot be stopped until the tape has rewound either to the load point or until tension is lost at the physical beginning of the tape.

2.2.8 POWER SHUTDOWN

A tape transport should not be turned off when tape is loaded and is past the load point marker. Kennedy 9000-series transports are designed to prevent physical damage to the tape in the event of power failure, and to minimize operator error which could destroy recorded data. In the event of a power failure during tape unit operation, manually wind the tape forward several feet before restoring power. When power has been restored, press the LOAD pushbutton, then the REWIND pushbutton. This will rewind the tape to the load point. If desired, the tape can then be advanced to the data block nearest the point at which the power failure occurred, by initiating the appropriate control commands.

Although it is possible to develop procedures which would allow power shutdown between files or record blocks on a tape, this is not recommended. Where data files are short, it is preferable to use smaller tape reels.

SECTION III
THEORY OF OPERATION

SECTION III

THEORY OF OPERATION

3.1 INTRODUCTION

This section describes the tape transport on a functional basis. The description applies to the standard model using the 800 cpi NRZI data electronics and covers all tape speeds. Models using the 1600 cpi phase encoded electronics, the dual density 800/1600 cpi electronics, or the seven-track NRZI electronics include a different set of data electronics, and these are described in special supplements that accompany the standard manual.

Each circuit card schematic is preceded by a detailed circuit description that explains the operation of the card on the component level. The description offered in this section is more in the nature of a block diagram description, and divides the transport into three main functional subsections – control logic, servo system, and data electronics.

3.2 CONTROL LOGIC

3.2.1 INTRODUCTION

The control logic section of the tape transport generates the appropriate internal tape motion commands in response to input commands from the transport interface, the main pushbutton panel, and from the test panel pushbuttons. The control electronics receive these commands and generate transport motion if all internal interlocks are satisfied. In addition, the control electronics return the transport status outputs to the interface and illuminate the respective indicators on the main panel and on the test panel.

Five plug-in circuit cards constitute the control section logic: Control Terminator Type 3841, Interface Type 3842, Pushbutton Control Type 3843/4843, Ramp Generator Type 3645, and Sensor Amplifier/Driver Type 3844. The modules are housed in the control card cage assembly and plug into the control master board. Figure 3-1 is a simplified block diagram of the control logic, showing the signal flow between the control modules. As can be seen, the input signals from the interface are supplied, after being terminated on the Control Terminator module, to the Control Interface module, where these signals are acknowledged if certain interlocks are satisfied. The motion commands are then supplied to the Pushbutton Control module; this card also includes the interlocks for the main panel pushbuttons and for the test panel pushbuttons. If the interlocks are satisfied, the Pushbutton Control module encodes all tape motion commands onto three command lines: RUN NORMAL (RNN1), RUN FAST (RNFST1), and REVERSE SELECT (RVS1). The three command lines are then supplied to the Ramp Generator module which produces accurate analog voltage output. The output of the Ramp Generator is then supplied to the Capstan Servo Amplifier module in the servo system, described below. The voltage output of the Ramp Generator in conjunction with the feedback from the capstan tachometer is used to energize the capstan motor and to advance the tape in the desired speed and direction. The Ramp Generator provides linear ramp-ups to speed and linear ramp-downs to standstill in order to minimize the stress on the tape and maintain accurate speeds.

The Sensor Amplifier Driver module receives the inputs from the file protect switch, the load point sensor, end of tape sensor, and broken tape sensor. These signals are amplified and supplied to the other modules in the control section where they provide the inputs to the interlocks. The Sensor Amplifier Driver module also contains the drivers for the front panel indicators, the driver for the file protect solenoid, and the write and erase head drivers.

3.2.2 CONTROL LOGIC OPERATION DURING A WRITE SEQUENCE

A write operation will be used as an example to demonstrate the interaction of the different components of the control logic. The whole operation is described, showing the flow of commands and the required control interlocks.

The main pushbutton panel is used to prepare the transport for operation. After the power is turned on and the tape is properly threaded, the front panel LOAD pushbutton is pressed. This sets the LOAD flip-flop on the Pushbutton Control modules, generating a RUN NORMAL (RNN1) true to the Ramp Generator card. The Ramp Generator outputs a linear ramp voltage to the Capstan Servo Amplifier card, initiating forward tape motion at normal running speed. The Ramp Generator also supplies TAPE RUNNING status true through the Interface Control card to the transport interface. When the load point reflector marker is detected by the respective photo cell, the signal is amplified by the Sensor Amplifier Driver card and is supplied as LOAD POINT DETECT (LP) true to the Pushbutton Control module. LOAD POINT true sets the ON TAPE flip-flop to the true condition which terminates the synchronous forward motion by setting RUN NORMAL (RNN1) false. The tape is stopped at load point and is properly loaded. Pressing the front panel ON LINE pushbutton now places the transport on line, preparing the transport to respond to interface commands once it is selected by the interface. When the transport is selected (input line SELECT going

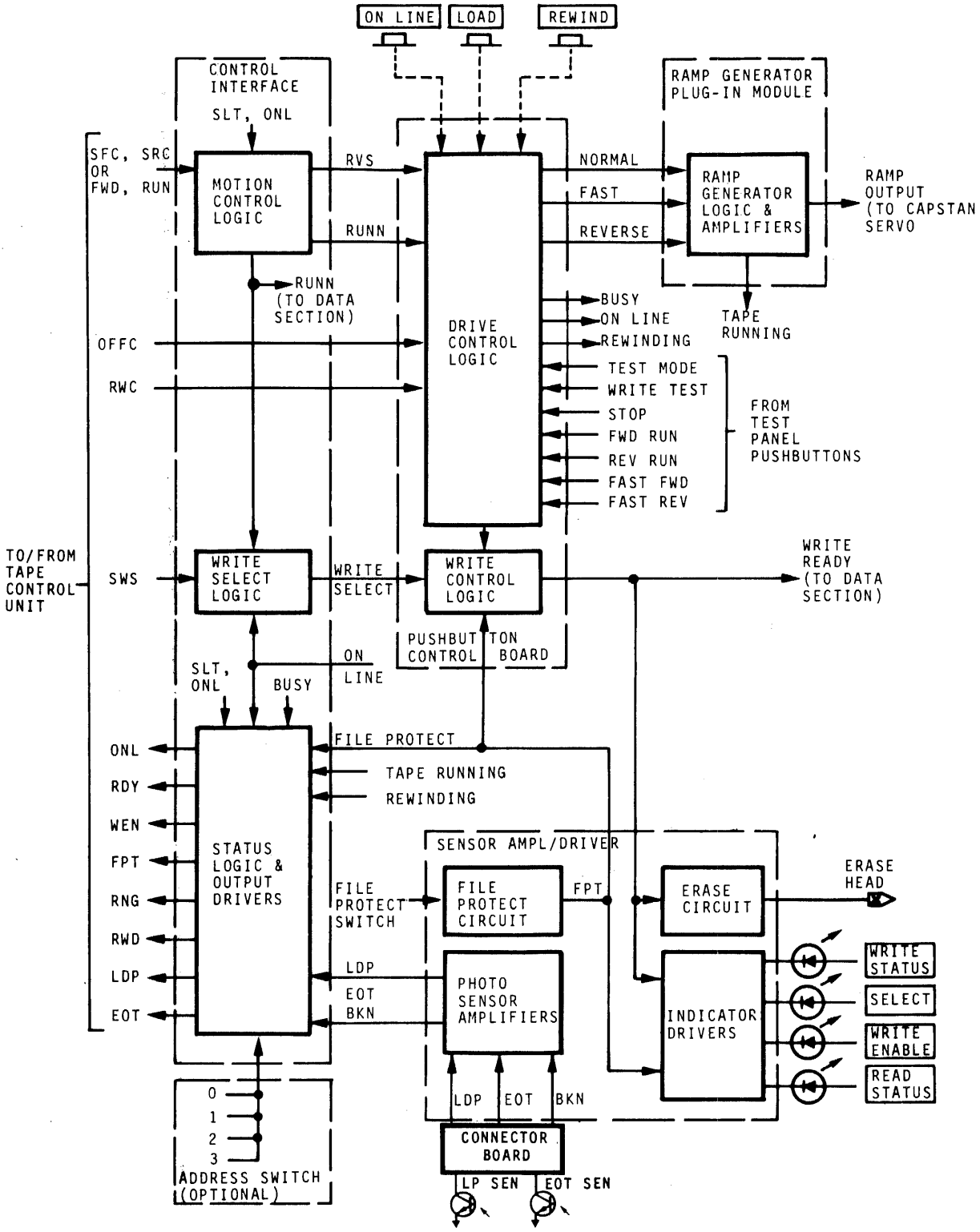


Figure 3-1. Control Section

true) the transport can accept commands from the interface and return the transport status outputs back to the interface. At this time the transport status lines would be in the states shown in Table 3-1.

In addition to the status lines, the front panel ON LINE and SELECT indicators are illuminated, as is the WRITE ENABLE indicator if the supply reel contains a write enable ring.

If the write operation is to be initiated, the interface now supplies SET WRITE STATUS level true and then a SYNCHRONOUS FORWARD COMMAND. The SET WRITE STATUS (SWS) level is sampled on the leading edge of the SYNCHRONOUS FORWARD COMMAND. If the level is true this sets a flip-flop on the Interface Control module and generates WRITE SELECT (WSEL/) true. WRITE SELECT is supplied to the Pushbutton Control module where it generates WRITE READY true provided that FILE PROTECT is false (supplied from the Sensor Amplifier/Driver module), BUSY is false (this signal is generated on the Pushbutton Control and is true whenever the transport is searching for load point and is rewinding), and no reverse command is given. These interlocks ensure that the transport writes data on tape only when the tape is properly loaded, the reel has a write enable ring, and the tape is moving forward at normal running speed. WRITE READY true is supplied to the Sensor Amplifier/Driver module where it turns on write and erase head current drivers and illuminates the WRITE indicator on the front panel. WRITE READY and SELECT 1 (combining ON LINE true and SELECT true) are also supplied to the data electronics card cage where they enable the write and read amplifier stages.

When the tape is properly loaded and not rewinding the WRITE READY is false, a read operation is selected and the Sensor Amplifier/Driver module illuminates the front panel READ indicator.

If WRITE READY does go true the interface supplies the properly formatted data to be written on tape. The write operation can be interrupted in case of broken tape; when the BROKEN TAPE signal is supplied from the Sensor Amplifier/Driver module, all servos are disabled immediately. Note that an END OF TAPE indication does not terminate a write operation, but leaves it up to the interface to do so. When the write operation is terminated by the interface, the tape is rewound to load point when the interface issues a REWIND COMMAND. Note that the tape cannot be rewound past the load point by a command from the interface. In order to rewind the tape off the takeup reel the transport must be taken off line, either through an interface command or by pressing the front panel ON LINE pushbutton again. Once the transport is off line the front panel REWIND pushbutton can be activated to rewind the tape completely off the takeup reel.

3.2.3 TEST PANEL

The test panel provides a means of exercising, testing, and adjusting the tape transport while it is off line, eliminating the need for a separate test fixture or for the use of valuable computer time. The test panel can initiate forward and reverse tape motions at either normal or high tape speeds. It can also initiate a write test, generating a crystal controlled all-1 test pattern on tape. The test panel also provides indicators for load point, end of tape, and data available. An additional indicator monitors excessive skew, and is used in the aligning of the read/write head and when using an 800 cpi skewmaster tape. When the head is properly aligned and the data is written on tape properly the SKEW indicator is extinguished.

The controls and interlocks for the test panel are located on the Pushbutton Control card. The skew detect network is located on the Delay Timing module in the read logic section of the transport. The test panel becomes operational only when the transport is OFF LINE, with the test panel STOP pushbutton depressed. If these conditions are satisfied the test panel pushbuttons are enabled when the TEST MODE pushbutton is pressed.

3.2.4 CONTROL LOGIC ADJUSTMENTS

The Kennedy tape transport requires very few adjustments. These are preset in the factory and should not be changed unless there is a very strong reason to believe that they are required. The following adjustments are made on the control logic modules:

Adjustment	Location
Normal running speed	Ramp Generator
Ramp-up time	Ramp Generator
Ramp-down time	Ramp Generator
End of Tape/Beginning of Tape Sensor Adjustment	Sensor/Amplifier Driver

The adjustment procedures are outlined in the maintenance section of the manual and in the circuit descriptions of the individual schematics.

3.3 SERVO SYSTEM

3.3.1 INTRODUCTION

The transport servo system consists of the electronics and electromechanical components that are required to advance the tape past the magnetic head at accurately controlled speeds while maintaining constant tape tension. The servo system includes two subsections -- the capstan servo system, whose function is to drive the tape at accurately controlled speed, and the reel servo system that maintains constant tape tension. High performance servos are

STATUS LINE	STATE	POINT OF ORIGIN
ON LINE	true	Supplied from the load point flip-flop on the Pushbutton Control module, routed through the Interface Control module.
TRANSPORT READY	true	This signal, generated on the Interface Control module, combines BUSY false (meaning the transport is loaded and not rewinding or searching for load point) and SELECT 1 true (meaning the transport is ON LINE and SELECT is true).
TAPE RUNNING	false	This signal goes true on the Ramp Generator when tape motion is initiated.
REWINDING	false	At this time the Rewind flip-flop on the Pushbutton Control module is in the cleared state.
FILE PROTECT		This signal is true if the reel of tape mounted on the supply hub does not contain a write enable ring. It is false if the reel does contain the ring and is available for writing. The signal originates on the Sensor Amplifier/Driver module.
LOAD POINT	true	Since the tape is at load point the Sensor Amplifier/Driver supplies this signal true. When LOAD POINT is true the transport does not acknowledge a REWIND command or a SYNCHRONOUS REVERSE COMMAND from the interface, but must be taken off line and rewound off tape by using the front panel pushbutton.
WRITE ENABLE		This signal is equivalent to the inverse of the FILE PROTECT signal and is true whenever the other is false; e.g., whenever the supply reel contains a write enable ring. The signal originates on the Interface Control module.
END OF TAPE	false	This signal goes true only when the end of tape reflective marker is detected by the respective photosensor. The signal is supplied to the Sensor Amplifier/Driver module.

Table 3-1. Transport Status

required to drive the reel motors and the capstan drive motor. Considerable power is required, resulting in substantial heat dissipation. This requires the use of heatsinks which are mounted for optimum cooling. All servo components are modular in nature and may be replaced with minimum effort.

Two types of servo systems are employed: One is used in transports with running speeds of up to and including 25 inches per second; the other system is used in transports with running speeds exceeding 25 inches per second. Both systems are described below.

3.3.2 REEL SERVOS (for transport speeds of 25 ips or less)

Two identical reel servos are employed for the supply and the takeup reels. A block diagram is shown in Figure 3-2. Each reel servo includes a spring loaded buffer arm, a magnetic position sensor coupled to the buffer arm shaft, a Servo Preamplifier Type 2683 module, a Servo Power Amplifier Type 3191 module, and a high power dc motor. The dc motors operate from +/-24 volt supplies capable of providing up to 30 amperes peak output current. Belt drives are used with a gear ratio of 4.8 to 1 to couple the motors to the reel hubs.

The tape tension is maintained by the interaction of the spring loaded buffer arms and the respective reel motors. The magnetic position sensors, called magpots, produce a corrective voltage whenever the buffer arm swings away from the center of its arc. The magpot consists of an oscillator circuit, a stationary transformer with a rotating flux linkage, and a discriminator circuit. When the buffer arm is in the center of its arc the rotating flux linkage

coupled to the buffer arm shaft is adjusted so that the oscillation induces equal voltages into the two stationary secondary coils of the transformer. When equal voltage is induced to both coils the voltage of each cancels out the other and the output of the position sensor is 0 volt. When the buffer arm swings away from the center of its arc the rotating flux linkage induces more voltage into one of the secondary coils than the other, generating either a positive or negative corrective voltage to the Servo Preamplifier module of the respective reel. This module amplifies the corrective voltage and supplies it to the Servo Power Amplifier whose output energizes the reel motor. The reel motor then produces the proper torque to return the buffer arm to the center of its arc, where the position sensor output is again reduced to zero.

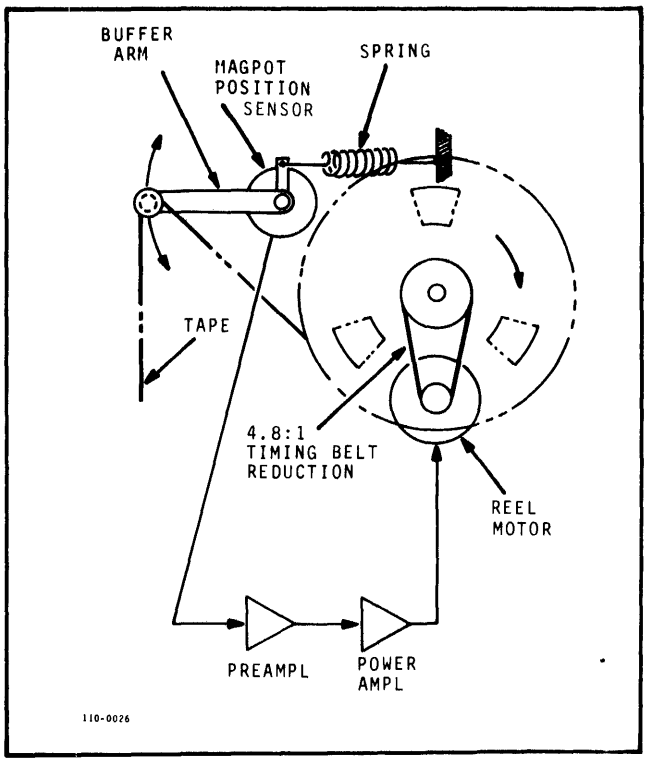


Figure 3-2. Reel Servo System

3.3.3 CAPSTAN SERVO (25 ips or less)

The capstan servo system includes the Capstan Servo Amplifier Type 3264, the capstan motor, and the capstan tachometer. The analog voltage output by the Ramp Generator card (in the control logic section) is supplied to the Capstan Servo Amplifier module where it is compared with the feedback supplied from the tachometer coupled to the capstan motor. Any resulting difference is amplified and energizes the capstan motor.

3.3.4 HIGH SPEED SERVO SYSTEM (for transport speeds exceeding 25 ips)

In transports with synchronous running speeds exceeding 25 inches per second the response of the reel motors to the capstan motion is more critical. Since the ramp times are shorter for higher tape speeds (ramp times are determined by the formula, ramp time 0.375/ tape speed, and are consequently inversely proportional to tape speed) it is necessary for the reel motors to be energized as soon as capstan motion is initiated. This quicker response is accomplished by modifying the capstan tachometer output on the Capstan Servo Amplifier Type 4181 module and supplying it as MODIFIED TACHOMETER OUTPUT to the Servo Preamplifier Type 4105 modules, where it is summed with the corrective voltage supplied from the magpot position sensors to produce the energizing output for the reel motors. The effect of the MODIFIED TACHOMETER OUTPUT on the reel motor response is adjusted by potentiometers on the Servo Preamplifier Type 4105 modules. The adjustment is made so that the buffer arm travel is minimized during ramp-ups to normal running speed, thus optimizing the interaction of the MODIFIED TACHOMETER OUTPUT and the magpot corrective voltage.

In addition to the MODIFIED TACHOMETER OUTPUT the high speed Capstan Servo Amplifier supplies a FIELD DRIVE output to the reel motors. The FIELD DRIVE cuts off the current to the reel motor windings in speeds exceeding approximately 65 inches per second. This increases the speed during the high speed rewind, while during normal running speeds the FIELD DRIVE supplies the current to the reel motor windings to increase the torque, as required for normal speed ramp-ups and ramp-downs.

Other than the MODIFIED TACHOMETER OUTPUT and the FIELD DRIVE signals the operation of the high speed servos is identical to that of the normal speed servos. The same ramp generator is used in both systems to supply the input voltage to the Capstan Servo Amplifier, where it is compared with the tachometer output to energize the capstan motor.

3.3.5 SERVO SYSTEM ADJUSTMENTS

The following adjustments are preset in the factory and should not be changed unless there is a strong reason to believe that they are required. The adjustment procedures are outlined in the maintenance section of the manual and in the circuit descriptions of the particular schematics.

Adjustment	Location
Capstan servo offset (to prevent capstan creep)	Capstan Servo Preamplifier
Buffer arm position	Magpot Type 4210 Magpot with Tension Arm Limit Detector Type 4537 (optional)
Buffer arm travel	Only in the high speed Servo Preamplifier

3.4 DATA SECTION

3.4.1 INTRODUCTION

The data section includes read and write amplifiers and interface cards providing output drivers and timing controls. Block diagrams are shown in Figures 3-3 and 3-4.

The data section consists of eight circuit cards that plug into the data master board. These include a Timing Delay module, a Read Amplifier/Clipping Control card, a pair of Quad Read Amplifier modules, a four channel Write Amplifier Card, a five channel Write Amplifier card, and a Data Terminator card.

3.4.2 WRITE ELECTRONICS

A write amplifier channel is provided for each tape channel. Four such channels and the circuitry common to all write amplifiers are contained on Write Amplifier Type 3848, and the five remaining write amplifier stages are located on Write Amplifier Type 3849. These cards plug into the data master board, from which the necessary head connections are made. Two of the channels on Write Amplifier Type 3848 are not used in seven-track operation.

Each write amplifier channel consists of an input buffer, a digitally adjustably deskewing circuit, a clocked flip-flop, and a head driver. The skew characteristics of each read/write head are tested at the factory and the write amplifier switches are set to compensate for the skew, using channel P as the fixed reference channel. Normally the write deskew switch settings should never be changed. When a new head is installed the factory furnishes a tag displaying the new deskew switch settings required to compensate for the characteristics of the new head.

The write electronics section also includes the write data strobe buffer which clocks the write amplifier flip-flops, and a write amplifier reset circuit to clear all write amplifier flip-flops. The write amplifier reset is used to write the longitudinal redundancy check character. During a write test mode, initiated by the test panel with the recorder off line, the write electronics generates an all-1 test pattern on tape derived from a crystal controlled reference frequencey F_R, supplied from the Delay Timing module in the read electronics. The test pattern can be used to test the write deskewing, as well as the other functions of the data electronics.

3.4.3 READ ELECTRONICS

The function of the read electronics is to convert the data recovered from the tape into digitized waveforms, deskew it and supply it to the interface with its respective read clock. The read electronics also detect the interrecord gap and excessive skew. The components comprising the read section include the magnetic read head, the Read Preamplifier module, Delay Timing module, Read Amplifier/Clipping Control module, and a pair of Quad Read Amplifier modules. Figure 3-4 is a functional block diagram of the read section, showing the general signal flow between the cards. A detailed circuit description of each circuit card accompanies the schematic of the card.

The low level analog signals, on the order of tens of millivolts, are supplied from the read head to the Read Preamplifier module where they are linearly amplified to an output voltage (adjusted by a potentiometer for each Read Preamplifier stage) of approximately 9 volts peak to peak in 800 cpi NRZI read operation. The amplified analog signals are then supplied to the nine read amplifier stages, eight of which are located on the Quad Read Amplifier modules while that of channel P is located on the Read Amplifier/Clipping Control module. Each Read Amplifier stage includes a peak detection circuit, a filtering network, an output data register, and a pulse generator.

The analog signals from the preamplifier are detected only when they exceed the positive or negative clipping levels provided by the Read Amplifier/ Clipping Control module. They are then rectified and peak detected, with the resulting digitized waveforms containing negative-going transitions corresponding to the peaks of the input analog signals, e.g., one bits in the NRZI code. The digitized waveforms are supplied to a filtering network which eliminates spurious pulses between transitions. The data of each channel is then stored in a register and generates a PULSE OUT to the Delay Timing module. Following the skew delay the Delay Timing card supplies a DATA TRANSFER output to clock the data registers of all nine channels simultaneously, supplying the data character to the interface.

When an error is detected, and the transport is commanded by the interface to reread a block, the read amplifier clipping levels are switched automatically by the Read Amplifier/Clipping Control module to maximize the recoverability of marginally

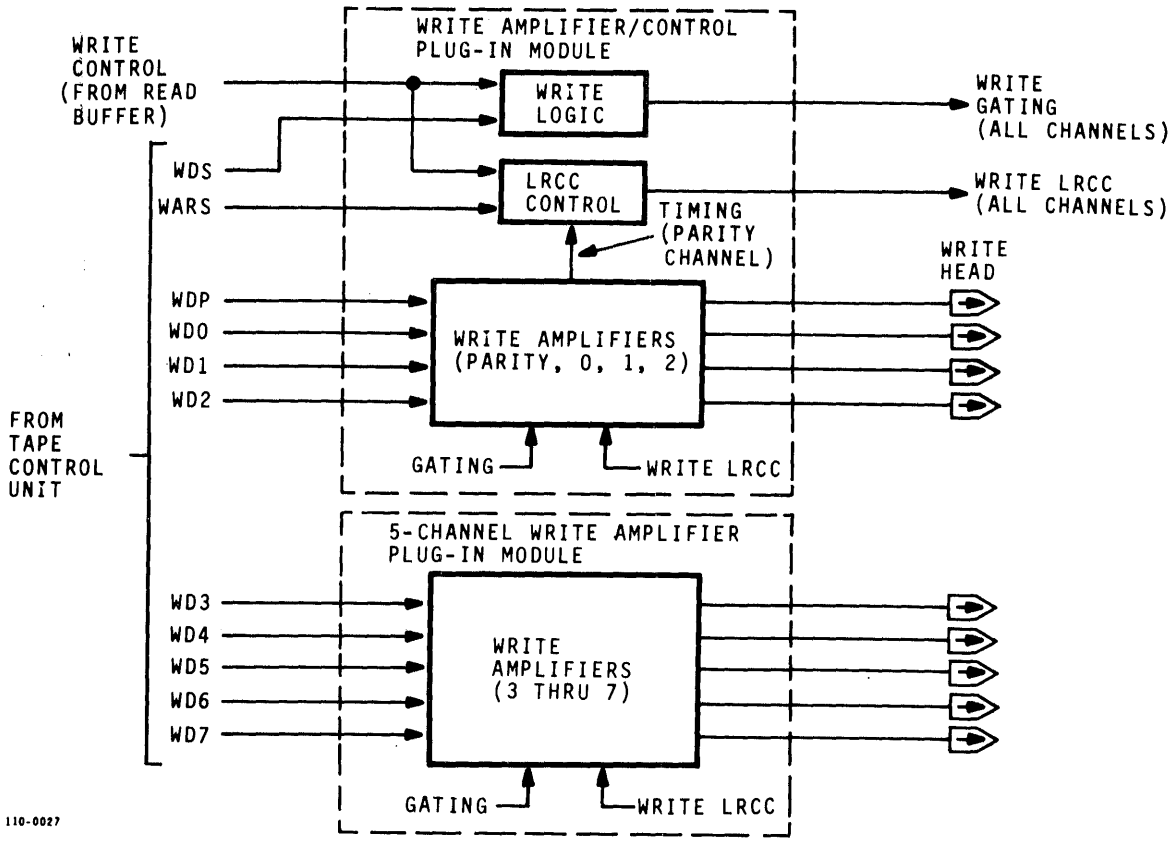


Figure 3-3. Write Data Section

recorded data. The clipping levels are kept normal on the first reread; on the second reread are switched to lower levels in order to recover possible partial dropouts. If the block is still in error and a third reread is commanded the clipping levels are switched to higher levels to eliminate possible baseline spikes. During read-after-write operations higher clipping levels are used.

The Delay Timing module contains circuitry common to all nine channels. It includes a crystal controlled oscillator and divider network which produce the synchronous clocks used in the skew delay network, the data strobe generation, the gap detect network, and are also supplied to the Write Amplifier Type 3848 module to generate the write test pattern. The crystal controlled clocks ensure high precision in the performance of all data synchronized functions.

3.4.4 DATA SECTION ADJUSTMENTS

The following adjustments are made in the data electronics section:

Adjustment	Location
Read preamplifier amplitude	Read Preamplifier Type 3935
Skew alignment	Read/write head, write amplifiers

These adjustments are preset at the factory and should not be changed unless there is a strong reason to believe that a readjustment is required. The adjustment procedures are outlined in the maintenance section of the manual and in the circuit description of the individual schematics.

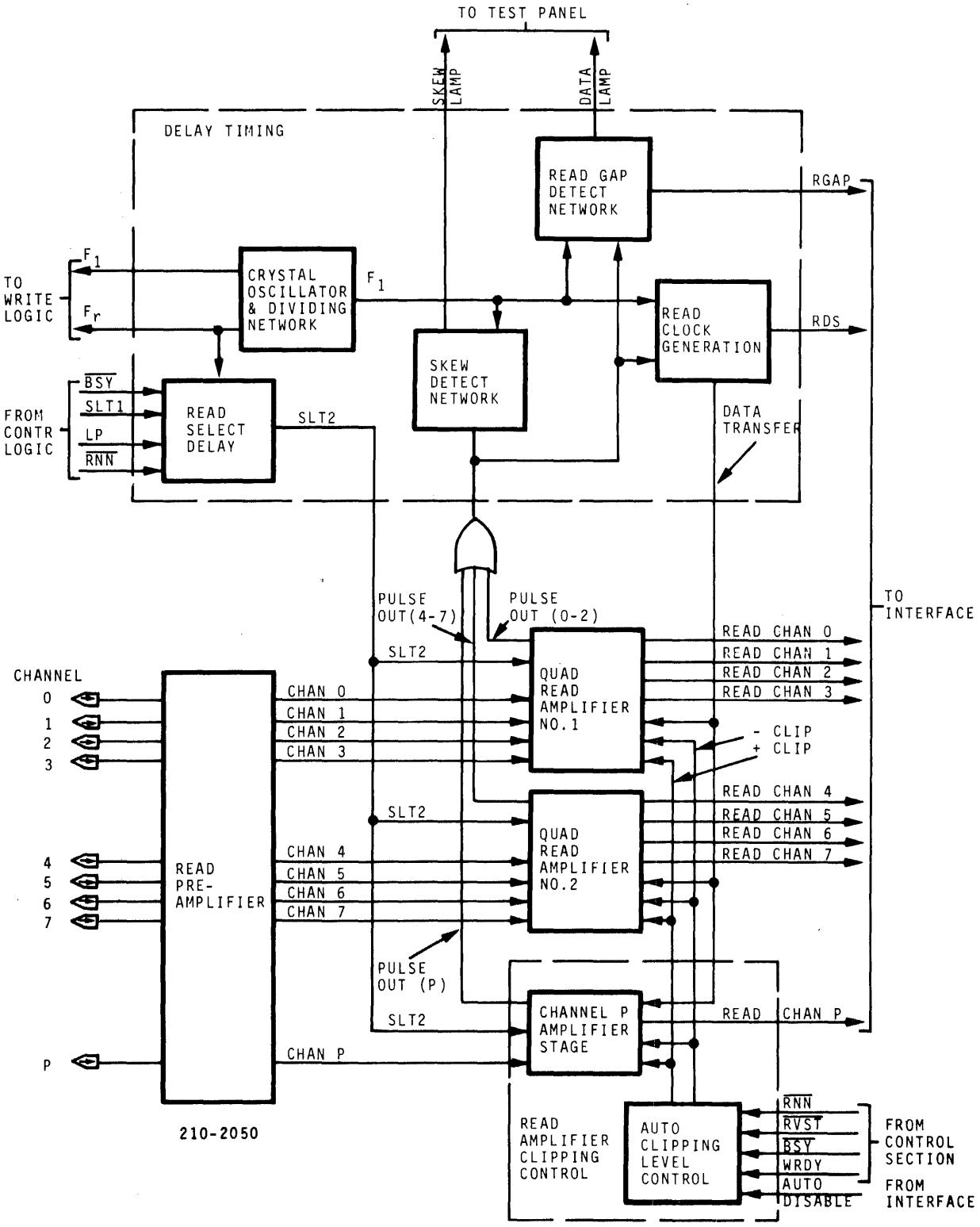


Figure 3-4. Read Data Section

SECTION IV
MAINTENANCE INSTRUCTIONS

SECTION IV

MAINTENANCE INSTRUCTIONS

4.1 GENERAL

Kennedy Company tape transports are highly reliable precision instruments which will provide years of trouble-free performance when properly maintained. A planned program of routine inspection and maintenance is essential for optimum performance and reliability. The units require very few adjustments and these should not be performed unless there is strong reason to believe they are required. All electrical adjustments are preset at the factory and should not require readjustment except after long periods of time.

4.2 PREVENTIVE MAINTENANCE

To assure continuing trouble-free operation a preventive maintenance schedule should be kept. The items involved are few and simple but very important to proper tape transport operation. The frequency of performance will vary somewhat with the environment and degree of use of the transport so a rigid schedule applying to all machines is difficult to define. The recommended periods below apply to units in constant operation in ordinary environments. They should be modified if experience shows other periods are more suitable.

4.2.1 DAILY CHECK

Visually check the machine for cleanliness and obvious misadjustment. If items in the tape path show evidence of dirt or oxide accumulation, clean thoroughly.

4.2.2 CLEANING

All items in the tape path must be kept scrupulously clean. This is particularly true of the head and guides. The inside of the dust cover must not be allowed to accumulate dirt since transfer to the tape will cause malfunction.

In cleaning it is important to be thorough yet gentle and to avoid certain dangerous practices.

4.2.2.1 Head Cleaning

Oxide or dirt accumulations on the head surfaces are removed using a mild organic solvent and a swab. Q tips are convenient for this but must be used with caution. Be sure the wooden portion does not contact head surfaces. Figure 4-1 shows access to the head by lifting the face shield.

An ideal solvent is 1.1.1 trichlorothane contained in the Kennedy K21 maintenance kit. However, others such as isopropyl alcohol will do.

DO NOT USE - acetone or lacquer
- aerosol spray cans
- rubbing alcohol

Do not use an excess of any solvent, and be extremely careful not to allow solvent to penetrate ball bearings of tension rollers, capstan motor, etc., since it will destroy their lubrication.

4.2.2.2 Tape Path Cleaning

Other items in the tape path should be cleaned at the same time as the magnetic head. These include:

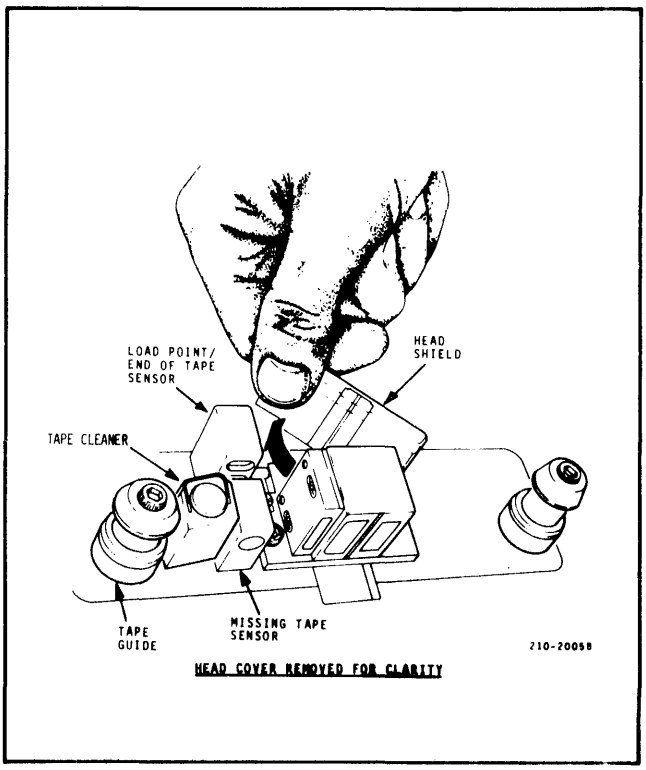


Figure 4—1. Opening of Head Shield

Tension rollers
Tape guides
Capstan

The techniques are similar to those outlined above for head cleaning.

4.2.2.3 Other Cleaning

Use a vacuum cleaner to remove accumulations of dust inside the dust cover or elsewhere in the unit. Compressed air may be used if caution is exercised to avoid blowing dirt into bearings. Antistatic cleaners are available for cleaning the plexiglass dust cover window.

4.2.3 VISUAL CHECK

Check visually to determine if all appears to be right with the machine. It is helpful to run tape forward and reverse observing smooth tape motion, proper tension arm operation, etc. It is well to remember that if things look right they probably are right, and the converse.

4.3 ROUTINE ADJUSTMENT

There are no routine adjustments. Need for adjustment will be manifest if malfunction occurs. Under normal circumstances adjustment will be more likely to cause trouble than prevent it.

4.4 LUBRICATION

No bearing lubrication is required. All bearings are lubricated for life and introduction of oil may destroy their lubrication.

4.5 WEAR

Magnetic tape is an abrasive and in time wear will be noted on items over which the oxide surface slides.

4.5.1 HEAD WEAR

Head wear is generally signaled by an increase in error rate. Confirmation is a sizable increase in output voltage from the read head as measured at the read preamplifier. When the head becomes worn it must be replaced. Head replacement is described in paragraph 4.16.

Worn heads usually can be resurfaced at least once if returned to the factory. This is more economical than replacement with a new head. Consult Section V for details of head return.

4.5.2 GUIDE WEAR

Guides wear principally at the point of contact with the front guide surface. Although guides are hard anodized with a coating equivalent to sapphire, in time grooves will appear. Since guides are symmetrical it is only necessary to loosen the guide mounting screw, rotate the guide, and tighten to present an unworn surface to the tape.

4.5.3 REEL HUB WEAR

Quick release hubs are adjustable to assure a firm clamping action. They are designed to make it impossible to mount a reel in a wrong or cocked position. If the locking action should become weak, the hub may be adjusted by tightening the nut at the read end of the shaft. O ring clamps used in the hub may tend to hang up after long periods of use. This can be corrected as follows:

a. Remove O ring from hub.

b. Clean thoroughly with mild solvent.

c. Lubricate ring with silicone grease. Wipe off as thoroughly as possible, leaving a light lubricating film.

d. Snap O ring back in place.

4.6 PERIODIC INSPECTION

At regular intervals, approximately every two months, it is advisable to make a more thorough check of machine operating parameters. This will insure that no progressive degradation will go unnoticed. Of great assistance in making these checks is the test panel which is standard equipment on Model 9000. It allows control of tape motion off line for test purposes and provides certain useful indicators and test signals as well. Using the test panel or other appropriate means, check the following periodically.

Tape speed
Ramp times
Read level
Skew
Photosensor adjustment

4.7 CAPSTAN AND REEL SERVO ADJUSTMENTS

Procedures for checking these and other items are given in paragraph 4.11 and a suggested sequence of adjustments is shown in Table 4-1.

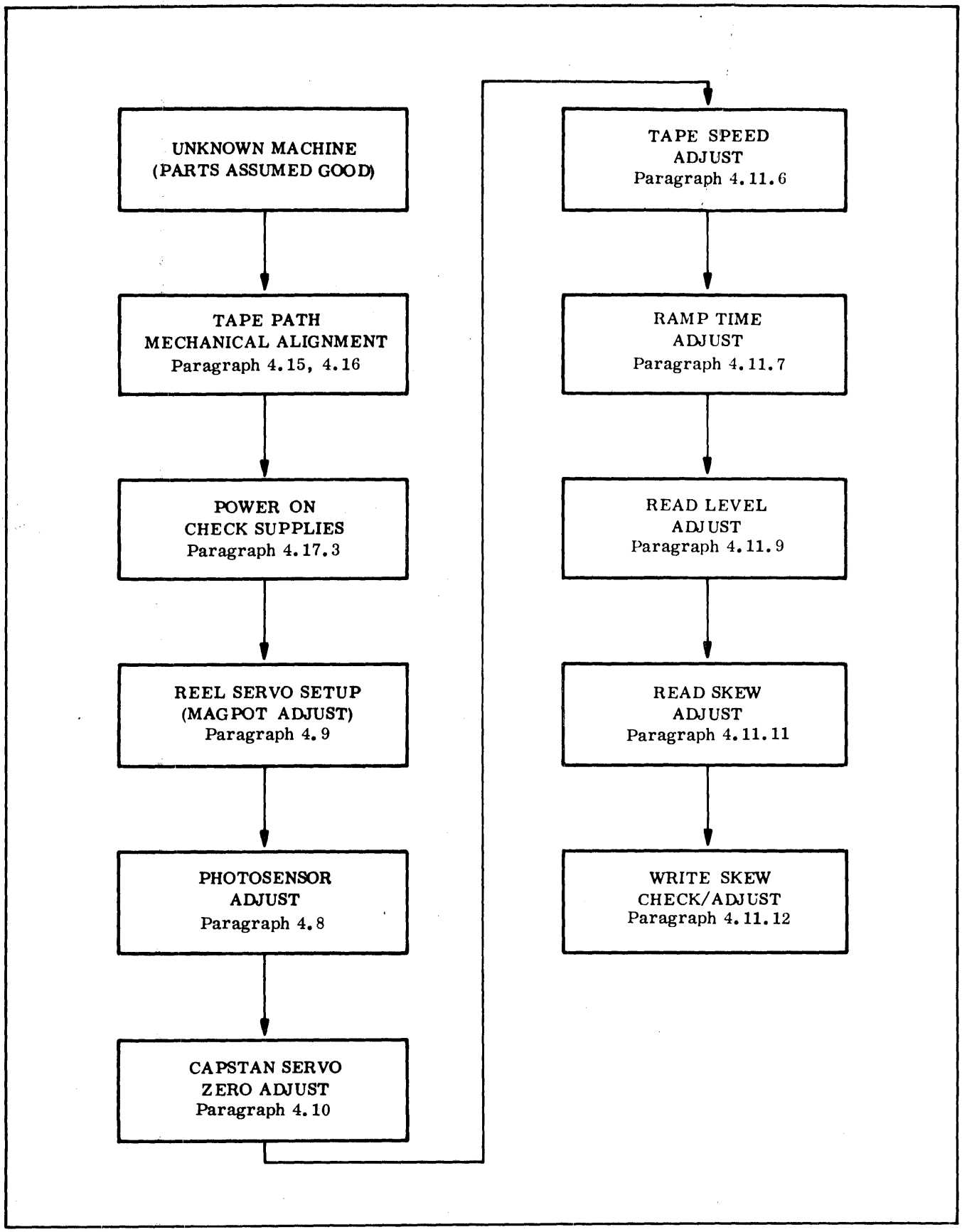


Table 4-1. Adjustment Sequence

4.8 EOT/BOT SENSOR ADJUSTMENT

Infrared emitting diodes and sensor transistors are used to detect the EOT and BOT markers. These semiconductor elements display long term stability and high resistance to ambient light conditions. The sensor amplifier bias has to be initially adjusted to balance the input to the amplifier stages. Once this adjustment is performed in the factory there is usually no need for readjustment unless the amplifier module or the sensing elements are replaced. When readjustment is required, follow the procedure outlined below.

a. Place blank tape over the sensors.

b. Connect a dc voltmeter between test points E and F on the Sensor Amplifier/Driver module.

NOTE

These test points are both off ground. If an oscilloscope is used to measure the voltage instead of a voltmeter, it must be isolated from ground, or the two inputs should be added with one channel inverted.

c. Adjust potentiometer R16 for 0v between test points E and F.

4.9 MAGPOT ADJUSTMENT

Magpots which provide position feedback to the reel servos should not require adjustment since only passive components and their geometry determine their zero settings. If one is moved by severe damage to the machine or if replacement is necessary, refer to the detailed circuit description in the schematic section for adjustment details.

4.10 CAPSTAN ZERO ADJUSTMENT

The capstan should be absolutely stationary at the zero speed setting. A zero adjustment is provided on the Capstan Servo Amplifier to nullify effects of component tolerances. To determine if adjustment is required, observe the following:

a. If capstan rotates slowly when it should be standing still, grasp capstan with tape loaded and turn first clockwise, then counterclockwise. Capstan will show a reluctance to turn. If turned gently a small dead zone can be detected. This dead zone should be approximately the same for either direction of motion. If adjustment is required, connect a voltohmmeter or scope probe to test point A of the Capstan Servo Amplifier.

b. Load tape and advance to load point.

c. Rotate zero adjust pot to obtain 0 volt at test point A.

4.11 TEST PANEL USE

The test panel is standard equipment in Model 9000, and is used to check the machine when it is off line and completely isolated from the operating system. The controls provided are useful under these circumstances. Under normal operation, however, they would be confusing and invite possible operator error. For this reason the test panel is mounted behind the deck assembly on Model 9000.

A diagram of the controls and indicators, together with brief descriptions of their functions, is given in Figure 4-2. Note that the box allows tape to be moved in either direction at normal speed or fast speed. Motion is interlocked to prevent tape from running off the reels.

Because of the special nature of the phase encoded and dual density transports, use of the test panel is slightly modified. The above discussion applies to NRZ1 only. Test panel use with other units is discussed in portions of the manual applicable to these types.

4.11.1 TEST PANEL OPERATION

The test panel becomes operational only in test mode, selected by pressing the alternate action TEST MODE pushbutton. For the TEST MODE button to be operational the machine must be:

a. Off line

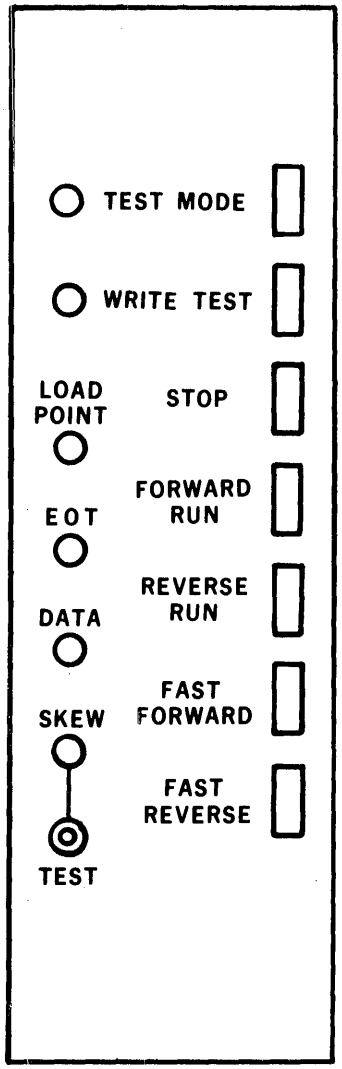
b. STOP must be depressed

Test mode is terminated by either:

a. Pressing alternate action TEST MODE button

b. Pressing ON LINE pushbutton

A characteristic of Series 9000 electronics is that when LOAD is pressed the machine feeds forward to load point. If tape is already wound on the machine and the load point marker has been passed, search will continue to end of tape unless REWIND is pressed. This characteristic is sometimes troublesome when servicing the machine. However, pressing TEST MODE will terminate search and induce an ON TAPE status in the control electronics. If ON LINE is



NOTE

Tape transport must be off line and STOP pushbutton depressed before test panel can become functional.

TEST MODE pushbutton and indicator. A momentary pushbutton selects test mode and activates test panel. When indicator (LED) is illuminated, test panel is active. (Tape unit must be off line and STOP pushbutton depressed before test panel will function.)

WRITE TEST pushbutton and indicator. A momentary pushbutton which programs 1's to be written on all channels to facilitate write skew adjustment. WRITE TEST remains active in FORWARD RUN mode only. (STOP pushbutton must be depressed and TEST MODE selected to actuate this feature.) The indicator remains illuminated while unit is in this mode.

STOP pushbutton. An interlocked pushbutton switch that terminates all tape motion.

FORWARD RUN pushbutton. An interlocked pushbutton switch that allows tape unit to proceed forward at normal speed. Depressing STOP pushbutton or EOT marker terminates this operation.

REVERSE RUN pushbutton. An interlocked pushbutton switch that allows tape unit to run in reverse at normal speed. Depressing STOP pushbutton or load point marker terminates this operation.

FAST FORWARD pushbutton. An interlocked pushbutton switch that allows tape unit to run forward at fast speed. Depressing STOP pushbutton or EOT marker terminates this operation.

FAST REVERSE pushbutton. An interlocked pushbutton switch that allows tape unit to run in reverse at fast speed. Depressing STOP pushbutton or load point marker terminates this operation.

LOAD POINT indicator. Indicates when tape is at load point.

EOT indicator. Indicates when tape is at end of tape.

DATA indicator. Indicates when data is being processed by read/write electronics.

SKEW indicator and TEST point. Indicator lights if tape skew exceeds the appropriate skew (read or write) gate setting. An oscilloscope test point is available for monitoring all read pulse outputs simultaneously, displaying total bit scatter.

Figure 4-2. Test Panel Controls and Indicators

subsequently pressed, the ON TAPE status is retained. This feature can be employed to allow power turn-off while tape is loaded.

When using tape motion pushbuttons the STOP button should be pressed between changes in motion speed or direction. No harm will result if this is not done, but occasionally switch bounce will cause the command not to be recognized and the last motion signaled will be retained.

4.11.2 SKEW INDICATOR

An LED indicator is provided which flashes if skew is encountered. Logic in the data section detects skew by two different criteria and lights the indicator. The skew gate in the NRZ1 read electronics is normally open for 50 percent of one character time (see discussion of read electronics). If pulses fall outside the skew gate they trigger the indicator. In test mode the skew gate is narrowed to 6/32 of a character time. An all 1's pattern on a properly adjusted machine should fall inside the shortened gate. A tape with random data suffers from pulse crowding effects and will not, in general, fall inside the gate. Thus in test mode the skew indicator is valid for all 1's data pattern only. In normal operation it is valid for all data patterns.

4.11.3 DATA INDICATOR

The DATA INDICATOR is illuminated when the tape being read has data written on it of a level sufficient to activate the read electronics. Naturally it blinks when reading gapped data.

4.11.4 LOAD POINT INDICATOR

This LED lights when load point is sensed.

4.11.5 EOT INDICATOR

EOT is indicated when the end of tape marker is sensed in the forward direction and remains true until it is passed in the reverse direction. All indicators operate whether or not TEST MODE is selected.

4.11.6 TAPE SPEED ADJUSTMENT

Normal speed of the unit is determined by setting the NORMAL SPEED pot (R14) on the Ramp Generator card. This control is set at the factory and should not normally require adjustment. To check speed:

a. Mount skewmaster tape on machine as in read skew adjustment.

b. Observe waveform at one preamplifier test point.

c. Set the time for one complete sine wave cycle (two bits) at a value determined by

$$\text{Time in } \mu s = 100 \times \frac{25}{\text{speed (ips)}}$$

by adjusting R14. Note that the waveform will not be entirely stationary on the scope owing to small rapid speed variations. These should be visually averaged.

d. If speed adjustment was made, check read preamp gain settings (paragraph 4.11.9).

4.11.7 RAMP TIME ADJUSTMENT

To assure accurate tape gap generation, the tape must linearly accelerate to running speed and linearly decelerate to stop. The start and stop ramp voltages required are controlled by potentiometers R3 and R4 on the Ramp Generator PC Board. Issue a series of rapid start/stop commands to the transport. Ramp timing is the same for both reverse and forward operations.

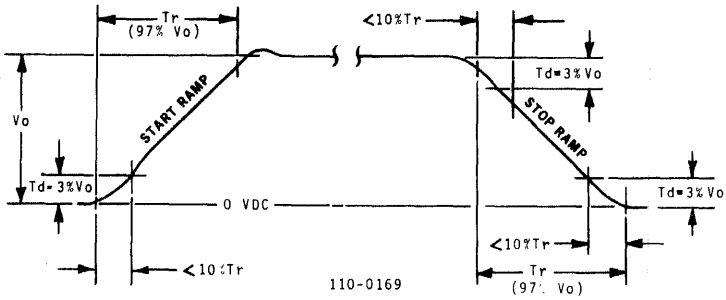
4.11.7.1 START RAMP ADJUSTMENT

a. Connect dual trace oscilloscope to resistor R20 of the 3264 Capstan Servo, or Test Point B of 5181 Board in high speed units.

2. Trigger oscilloscope on the control input to the formatter.

3. Adjust potentiometer R3 on ramp generator for Tr, the ramp time in milliseconds, where:

$$\text{Tr } (-5\% \ +0\%) = \frac{375}{\text{TAPE SPEED}}$$



NOTES: 1. Tr equals 97% of the total ramp voltage, Vo; 2. Ramp voltage should be at ground at beginning of ramp.

d. After adjustment, make certain Td, which is defined as 3% of ramp voltage Vo, is less than 10% of ramp time Tr.

4.11.7.2 STOP RAMP ADJUSTMENT

a. Connect oscilloscope to resistor R20, 3264 Board or Test Point B of 5181 Board.

b. Trigger scope on the trailing edge of the synchronous control command to the tape transport.

c. Adjust potentiometer R4 on the Ramp Generator PC Board for ramp time Tr. Start and stop ramp times should be equal.

d. Make certain Td, which is 3% of ramp voltage Vo, occurs in less than 10% of ramp time Tr.

4.11.8 REWIND SPEED

Rewind speed rewind ramp times are not adjustable. They are determined by fixed values on the Ramp Generator card.

4.11.9 READ LEVEL ADJUSTMENT

This adjustment sets gain of the Read Preamplifiers to the correct level. Too much gain will introduce noise and too little will aggravate dropouts.

a. Load a reel of scratch tape on the transport, write enable ring in place.

b. Select TEST MODE.

c. Select WRITE TEST, FORWARD RUN.

d. Observe waveforms at test point for each channel on Read Preamplifier.

e. Signal seen should appear as an approximate sine wave. Noise introduced by crosstalk from write head will be present but waveform should not be badly distorted by this.

f. Measure peak to peak amplitude. Set for 8 (+/-0.5) volts for dual density units or 9 (+/-0.5) volts for single density units, using channel gain control on Read Preamplifier. Repeat for each channel. Note that the read level is about 10 percent higher when the machine is operating in read-after-write mode than when in the read mode. This effect is caused by small unavoidable magnetic remanence in the write head and erase head. Skewmaster tapes should NOT be used as amplitude reference for this reason.

4.11.10 SKEW ADJUSTMENT

Skew is one of the most important parameters in reading NRZI data. Since, in a read-after-write head, data is read with one gap and written in a second gap, read and write skew are in general different and must be compensated separately. Only when both are properly set can the machine be said to be deskewed. In Series 9000 transports the read gap is deskewed mechanically while digitally controlled delays are used to deskew the write gap.

4.11.11 READ SKEW ADJUSTMENT

In deskewing the read gap the head is mechanically tilted to have its gap at an exact right angle to the tape. This is accomplished using a skewmaster tape (see maintenance tools).

a. Load skewmaster on transport. Be sure write enable ring is missing.

b. Press TEST MODE button.

c. Press FORWARD RUN.

d. Observe SKEW indicator and adjust skew adjusting screw on the head mounting plate (Figure 4-3) until indicator does not come on.

For greater precision a scope probe may be connected to the TEST terminal on the test panel. (This signal is also available at pin 8 of the test panel connector on the Pushbutton Control module.) At this point the pattern will be a grouping of nine pulses as each channel "reports in." The optimum skew setting is the one at which these pulses occupy the minimum spread.

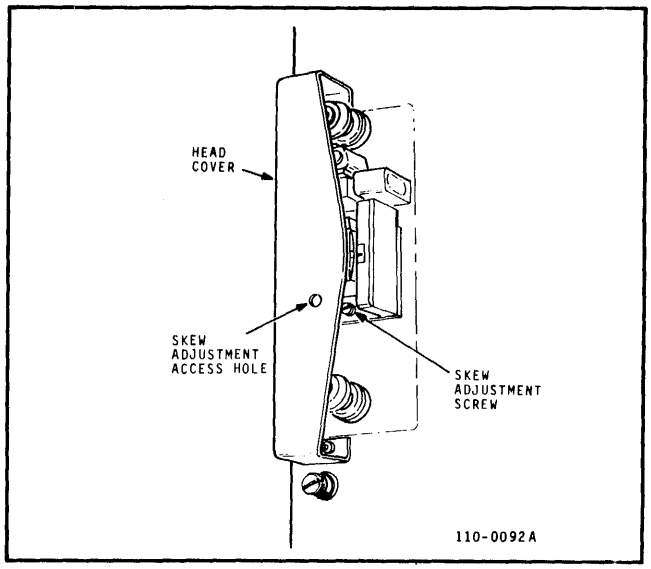


Figure 4—3. Read Skew Adjustment

4.11.12 WRITE SKEW ADJUSTMENT

Series 9000 transports feature a unique digital deskewing arrangement for deskewing the write head. Since write-read skew is a function of head geometry and does not change, write deskewing delays are determined at the factory and each head has a deskewing chart showing the appropriate write amplifier deskew switch settings for that head. All channels are referenced to the P channel (or C in seven-track units.)

If for some reason it is necessary to deskew the write head in the field the procedure is as follows:

a. Proceed as in read level adjustment, paragraph 4.11.9.

b. Connect a dual channel scope channel 1 to the P channel test point on the Read Preamplifier. Set alternate sweep, trigger channel 1 internal.

c. Connect scope channel 2 to test point for tape channel 5 and observe pattern. Set sweep speed to display one half sine wave cycle.

d. Observe separation of peaks displayed. Note that because of small variations in speed and skew the pattern will not be entirely stationary.

e. Set channel 5 skew switch for minimum peak separation.

f. Repeat for each of the remaining seven channels.

4.12 CHECKS AND ADJUSTMENTS

4.12.1 TAPE TENSION CHECK

a. Turn power off and remove tape from machine.

b. Using a spring scale, measure return force of tension arm at the approximate center of its arc. Force should be 16 ±2 ounces (450 ±55 grams) corresponding to tape tension of 8 ± 1 ounces (225 ± 27 grams).

NOTE

Spring anchor adjustment can be varied to produce small corrections. If a large correction is required, tension arm spring should be replaced.

c. To adjust spring tension, loosen anchor lug nut slightly and adjust anchor for correct reading on spring scale.

4.12.2 REEL SERVO TORQUE

CAUTION

Tape reels are equipped with drive servos that produce powerful torque forces. Caution must be exercised to avoid injury in making servo checks.

To check reel servo torque, an empty reel and a spring scale are required. Proceed as follows:

a. Drill a hole in the reel flange 3 inches (76 mm), measured radially, from the outside of the hub hole (see Figure 4-4).

b. Mount test reel on the transport.

c. With tension arm fully down, supply reel will turn clockwise. Hook spring scale in the hole.

d. Press LOAD button and restrain reel motion by holding spring scale. Scale reading should be 3 ±0.5 lb (1.36 kg ±225 g).

e. Repeat the check for opposite direction with buffer arm fully up. Scale reading should be the same as in step d.

4.12.3 TENSION ARM POSITION CHECK

When the transport is at rest with a tape loaded, the tension arms should be located in the approximate center of their respective arcs. If the arms drift away from their proper position they may hit the end of their arcs when the tape ramps up to running speed. The magpot position sensors coupled to the buffer arms as shown in Figure 4-5 control the position of the arms. When the tension arms drift away from their proper position the magpots should be adjusted according to the procedure described in the magpot circuit description, which is found in the schematic section.

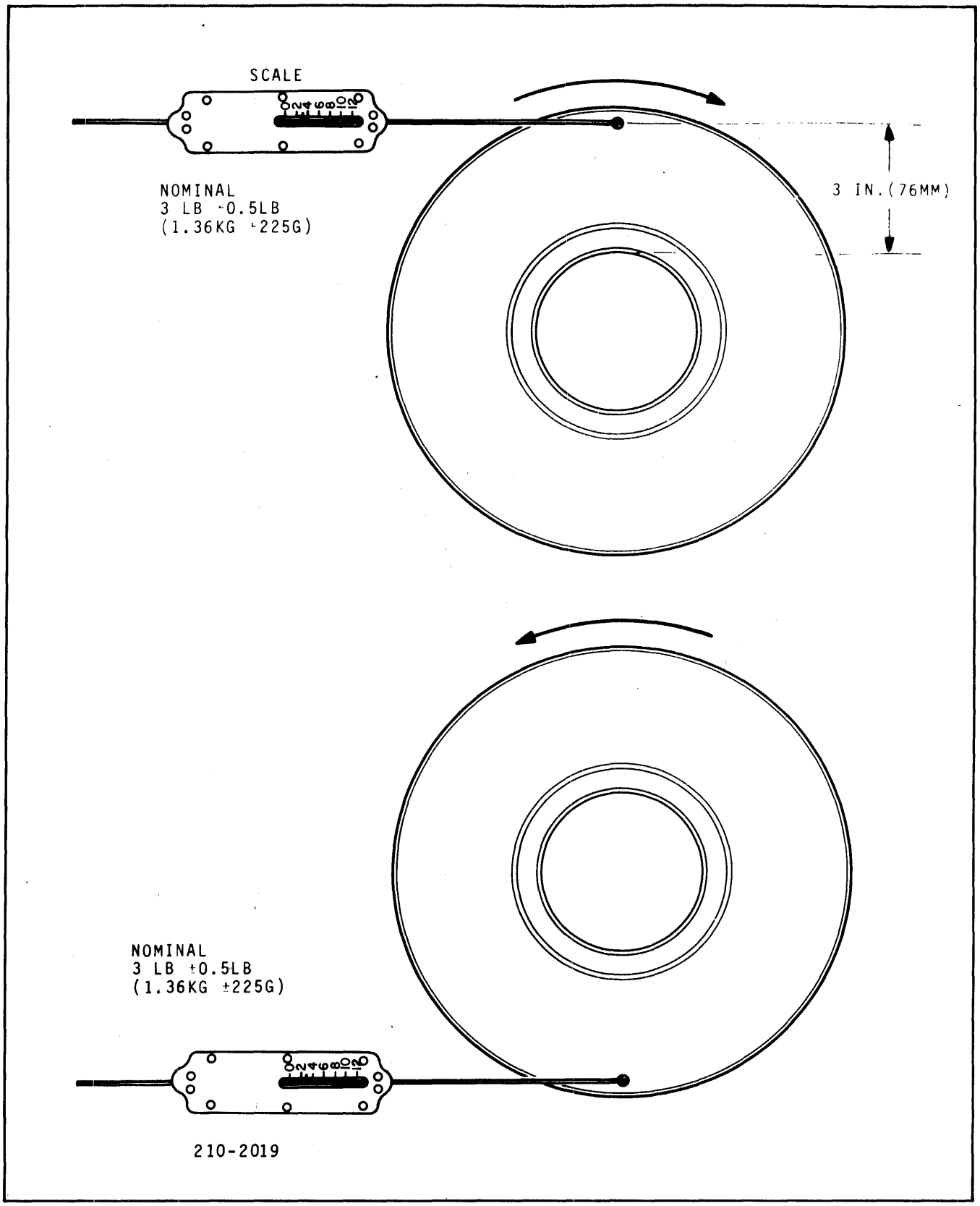


Figure 4—4. Reel Servo Torque Check

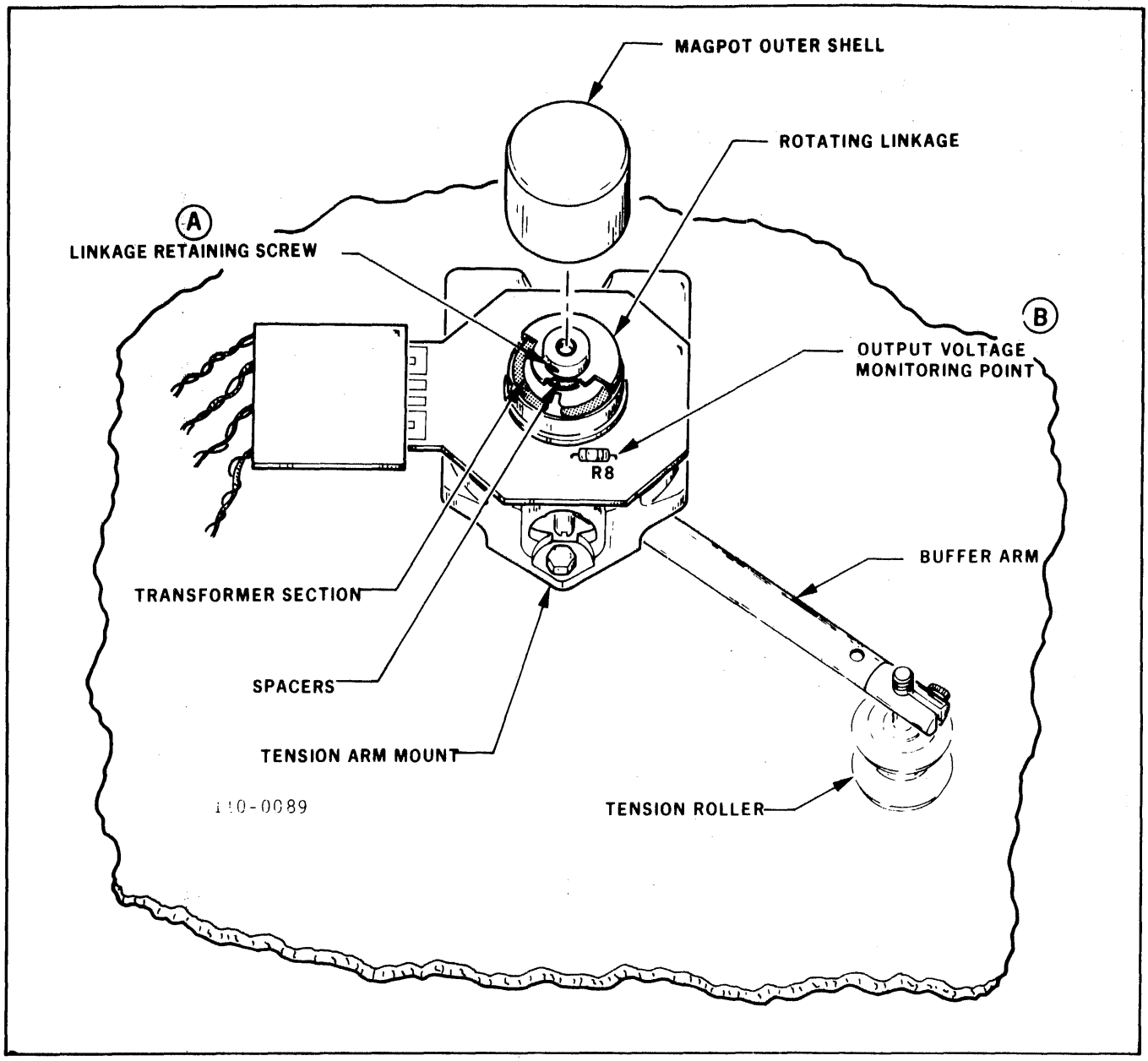


Figure 4-5. Magpot Assembly

4.12.4 HIGH SPEED BUFFER ARM ADJUSTMENT

This adjustment is performed only in transports with running speeds exceeding 25 inches per second. The adjustment is performed on the high speed Servo Preamplifier Type 4105 module, and is required when the buffer arms exhibit excessive travel during ramp-ups to running speed. In that case potentiometer R17 on the Servo Preamplifier Type 4105 should be adjusted to minimize buffer arm travel during the ramps, preventing the arm from bottoming and overshooting. To adjust, follow these steps:

a. Load a full reel of tape on the supply reel.

b. With the transport OFF LINE, press the Test Panel TEST MODE pushbutton, placing the transport under the test panel control.

c. Alternately press the FORWARD RUN and then the REVERSE RUN pushbuttons on the test panel, initiating synchronous forward and reverse tape motions.

d. Adjust potentiometer R17 on the SUPPLY Servo Preamplifier Type 4105 until the travel of the SUPPLY buffer arm is at a minimum during ramp-ups and ramp-downs.

e. Repeat the above procedure for the TAKE-UP Servo Preamplifier.

4.13 DATA SECTION ADJUSTMENTS

The data read/write deskewing adjustments are described in paragraph 4.11 of this section. The only other adjustment required is the output voltage adjustment of the read preamplifier stages. This adjustment should be made after the transport speed has been checked and, if necessary, adjusted (see paragraph 4.11.6). The output voltage of each read preamplifier stage should then be adjusted, using the potentiometer associated with that stage, until the output voltage is 9 volts peak to peak in 800 cpi operation.

4.14 POWER SUPPLY ADJUSTMENT

Power supply voltage regulation is handled by two regulator boards. Potentiometer R4 on the 3810 regulator board is the +5 volt adjustment; R5 on the 3414 board is the -10 volt adjustment.

Plus 5 volts should measure between +5 and 5.1 volts as measured at P2-2 of the 3810 board. Use chassis ground. Plus 10 volts regulated should measure between +10 and 10.1 volts as measured at J2 on the 3414 board.

4.15 TAPE PATH ALIGNMENT

For proper transport operation the items in the tape path must be accurately aligned. Tape guides are fixed in location and are not shimmed or adjusted in any way. The tension roller guides must be:

a. In alignment with tape guides;

b. Exactly at right angles to the tape.

4.15.1 ROLLER GUIDE ALIGNMENT

a. Remove roller guide to be aligned and replace with a length (approximately 4 inches) of 0.1875 inch stainless steel ground stock. Clamp in place.

b. Loosen roller guide lockscrew slightly so that with moderate pressure the roller guide rod can be rotated.

c. Thread tape over the rod.

d. While holding rod, run tape forward. Tilt rod back and forth until a position is found at which tape runs with equal tension on inside and outside and tape enters tape guides correctly, or in the case of the take-up roller guides, winds correctly on the center of the takeup reel.

e. When correct position is found, tighten lockscrew securely.

f. Replace roller guide and adjust height (paragraph 4.18.1).

g. Check alignment as described above and revise alignment if required.

NOTE

After completing all servo adjustments, correct spring tension should be checked by loading a full reel of tape and advancing it until equal amounts of tape are on both reels. Detach capstan connector plug J2 from the capstan servo amplifier; then rotate the capstan in both directions. Tension should feel equal. If it does not, readjust spring tension.

4.15.2 IDLER ALIGNMENT

With roller guides aligned as described above, only one critical item remains in the tape path - the idler. Its surface must be precisely at right angles to the tape surface. To determine whether idler adjustment is required, run tape forward and reverse about 1 foot in either direction. Observe whether tape maintains the same position on the capstan while it is in motion. If tape position varies more than 1/32 inch, idler adjustment is required.

To adjust idler:

a. Loosen locknut on idler adjusting screw (see Figure 4-6).

b. Loosen idler collar setscrew.

c. Run tape forward and reverse. Adjust idler adjusting screw until tape maintains the same position on the capstan and idler while it is in motion.

d. Retighten idler collar setscrew and locknut on the idler adjusting screw.

4.16 HEAD FACE SHIELD ADJUSTMENT

A shield is located over the magnetic head surface to reduce write-read crosstalk. Its spacing, determined by a spring stop, is important. The spring stop is adjustable as follows:

a. Loosen stop screw with tape removed from machine.

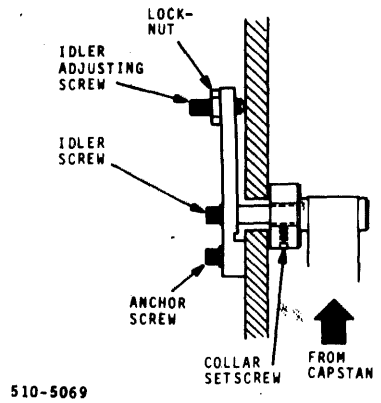


Figure 4-6. Idler Adjustment

b. Insert three thicknesses of tape (0.006 inch) between shield surface and top surface of head. Do not use feeler gauges, since they may scratch the head surface.

c. Press shield against tape firmly and tighten stop screw.

d. Remove tape pieces by lifting shield.

4.17 TROUBLESHOOTING

Trouble that can arise in the Model 9000 can usually be classified as either mechanical or electrical but often the classification may be confusing because a basically mechanical problem can cause what appears to be an electronic malfunction and vice versa. In any case the problem should be thoroughly analyzed before adjustments are changed.

Electronic troubleshooting is greatly facilitated by the modular construction - a new card may be substituted and the effect observed. Most difficult, of course, are subtle problems and those of an intermittent nature.

Visualizing solution (Magnasee) is useful under certain conditions for troubleshooting. At high densities the data cannot be satisfactorily resolved but such problems as a dead track, improper gap length, etc., can be isolated rapidly by its use.

If a tape has had visualizing solution applied to it DO NOT reuse that portion of the tape as it will contaminate the head. Cut the visualized portion off and discard.

To use visualizing solution, shake the can thoroughly, remove top and pass portion to be visualized through the solution. Snap the tape vigorously to remove excess solution and let dry. Iron powder will be left in magnetized areas. This can be picked off using Scotch tape and applied to a sheet of paper for a permanent record.

4.17.1 HIGH ERROR RATE

Usually the more difficult problems involve a higher than permissible error rate for which, at first glance, there is no obvious reason. If operating properly with good tape the transport should make very few errors in writing and if rewriting is included in the program it should make no read errors.

Useful clues are:

a. In what mode - read or write - are many errors occurring?

b. At what point in the block does the error occur?

c. What is the nature of the error: VRC, CRC, LRC?

d. Are the errors pattern related?

The first thing to be done is to inspect head and other items in the tape path for dirt accumulations. Be sure everything is clean. Check the tape being used and try a new reel if tape is doubtful. Check interface connections for broken wires or bad contacts. Table 4-2 is a trouble shooting chart concerned with high error rate.

4.17.2 COMPATIBILITY

Model 9000 accepts and produces tapes conforming to the ANSI standards. Occasionally compatibility problems can arise:

a. Tapes written by and acceptable to the 9000 are not acceptable to another transport.

b. Foreign tapes cannot be read by the 9000 but its own tapes can be.

Three items may be involved: skew, speed, ramp times. These should be checked as described in the adjustment procedures.

4.17.3 OTHER MALFUNCTIONS

Normal trouble shooting procedures are involved in finding electronic malfunctions. The first things to check are the supply voltages:

±24 volts nominal unregulated will normally be about ±26 volts under light load.

±10 volts ±0.5 volt

+5 volts ±0.25 volt

The test points for measuring supply voltages are:

+24v - case of Q9 (MJ802) on heatsink

-24v - case of Q10 (MJ4502) on heatsink

+10v - Sensor Amplifier/Driver TPA

-10v - Sensor Amplifier/Driver TPB

+5v - Sensor Amplifier/Driver TPC

Voltages are measured to chassis (ground).

NOTE

TURN POWER OFF WHEN REMOVING OR INSERTING CARDS.

If the voltages are not correct the trouble is either in the power supply or in the fact that the malfunction is loading the supply excessively. Pulling cards from their sockets can help isolate an overloaded condition. The power supply is short-circuit protected on the regulated voltages. A short circuit on +24 volts should blow the fuse. Assuming the voltages are correct. Table 4-3 should help in isolating malfunctions.

4.18 REPLACEMENT OF PARTS

In most instances assembly methods for parts replacement are obvious. Electronic parts are nearly all on plug-in modules. Items in the tape path may require machine realignment if replaced. If only one item is replaced at a time the complete alignment procedure usually may be avoided. Examples follow.

4.18.1 SUPPLY TENSION ARM ROLLER GUIDE

If alignment tool is available follow procedure given in tape path alignment. If not available, the following procedure will generally suffice.

a. Loosen roller guide split clamp screw (C) and remove roller shaft from tension arm. Do not loosen the adjustment lockscrew (A).

b. Insert new roller guide shaft and clamp lightly by tightening split clamp screw (C).

c. The shaft end is threaded to allow use of a nut for fine adjustment. The thread does not enter the clamp area. Place several No. 10 flat washers over the threaded end and install a 10-32 nut as shown in Figure 4-7.

Observed: High error rate — clean machine, good tape

Symptom	Possible Cause	Indication	Action	Reference
Continuous errors, every block (read mode)	Broken connection to interface or internally	Continuity	Correct connection.	
	Bad preamp channel	No output at test point on write test	Replace preamp.	
	Bad quad read amp channel	No data at test point	Replace quad read amplifier.	
	Tape speed grossly wrong	Visual or skewmaster	Adjust speed.	4.10.6
	Bad head channel	No output at preamp test point on write test	Replace head.	4.14.7
Continuous errors, write mode only	Broken connection on write data or WDS lines	Continuity	Correct connection.	
	Bad write amp channel	Wrong or no signal at write amp test point in write test mode	Replace write amp.	
Frequent write errors, few or no read errors	Write-read crosstalk	Noisy signal at preamp test point	Check preamp gain. Check face shield spacing.	4.10.9 4.12
Frequent CRC, LRC errors, no VRC errors	Wrong CRC generation in interface	Wrong data at input	Correct interface.	
Read or write errors only at start of block	Ramp time wrong	Read signals appear before ramp is complete	Adjust ramp time.	4.10.7
Read errors on long blocks only	Tape path misaligned	Tape bears heavily on one guide surface	Mechanical alignment.	4.11
Pattern related errors	Write-read crosstalk	Noisy signal at preamp test point	Check preamp gain. Check face shield spacing.	4.10.9

Table 4-2. Troubleshooting

Control Malfunctions

Symptom	Possible Cause	Location	Action	Reference
LOAD pushbutton activates servos when pressed but does not hold	Broken tape signal clears LOAD flip-flop			
	a. Sensor Amp/Driver module	Card cage	Replace module.	
	b. Pushbutton Control module	Card cage	Replace module.	
	c. Photosensor (BKN) malfunction	Deck	Replace sensor.	4.14.8
After load, tape runs and does not stop	Tape feeds forward after load point marker is sensed			
	a. Marker strip missing from tape	Tape	Apply reflective strip.	
	b. Misadjustment of photosensor on Sensor Amp/Driver module	Card cage	Adjust photosensor.	4.7
No EOT signal	Same as load point above but for EOT			4.7
REWIND pushbutton inoperative	Logic malfunction, Pushbutton Control module	Card cage	Replace module.	
Rewind does not stop at LP but continues until tape is wound off reel	a. Same as above			
	b. Photosensor adjustment wrong Sensor Amp/Driver module	Card cage	Adjust photosensor.	4.7
Reels rotate uncontrolled when power is turned on	a. Servo preamp malfunction	Card cage	Remove preamp. If reels stop, replace preamp module.	
	b. Servo power amplifier (bad power transistors)	Heatsink	Replace heatsink assembly or locate and replace bad power transistors.	
Arms badly off center of arc at rest	Magpot adjustment	Deck	Adjust magpot setting.	4.8

Table 4-3. Troubleshooting

Control Malfunctions

Symptom	Possible Cause	Location	Action	Reference
Arms bottom when starting or stopping. Weak reel torque, otherwise normal	a. Servo preamp malfunction	Card cage	Replace module.	
	b. Magpot adjustment (spacing)	Deck	Check adjustment.	4.8
	c. Bad reel motor	Deck	Replace reel motor.	
Tape moves erratically, slips on capstan	a. Head face shield touching tape	Deck	Adjust face shield setting.	4.12
	b. Defective tension roller	Deck	Replace roller.	4.14.1
Capstan turns slowly when it should be stopped	Capstan zero adjustment Servo Preamplifier module	Card cage	Adjust zero.	4.9

Table 4-3. Troubleshooting

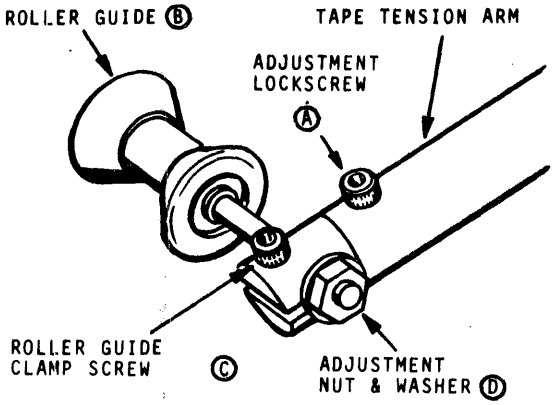


Figure 4–7. Roller Guide Adjustment

4.18.2 TENSION ARM REPLACEMENT

Tension arms are replaced by removing roller guides and disassembling. Do not attempt to remove the pin holding the arm to its shaft; replacement assemblies are supplied pinned. Reassemble the arm mechanism.

It will be necessary, if tension arms are replaced, to perform the complete tape path alignment procedure (see paragraph 4.15).

4.18.3 REEL MOTOR OR BELT REPLACEMENT

a. Open deck panel to expose motor. Disconnect motor power plug. Remove four nuts fastening motor and its mounting plate to chassis.

b. Unscrew four screws fastening motor to mounting plate to chassis. Replace with new motor.

c. Hook drive belt over motor pulley. Reposition motor assembly onto its mounting studs.

d. Check belt tension prior to tightening mounting plate nuts. When pressed, it should deflect about 1/4 inch. Position motor assembly for proper belt tension and tighten motor mounting nuts. Reconnect motor power plug.

4.18.4 CAPSTAN MOTOR REPLACEMENT

a. Remove capstan lockscrew.

b. Remove capstan. Capstan fits a taper on the motor shaft so it may be readily removed once loosened. It may require considerable force to break loose, however. Pullers are available for this use but a screwdriver properly protected to prevent marring may be used to pry against the panel.

c. Remove the four capstan motor mounting screws. Unplug motor and remove.

d. Install new motor. Check tape path when tape is in motion.

e. Adjust capstan position as described under tape path alignment, paragraph 4.15.

4.18.5 HUB REPLACEMENT

After long use components in the quick locking mechanism may become worn to the point that adjustment of locking pressure cannot securely hold the tape reel. It is not necessary to replace the entire hub assembly; a hub repair kit, Kennedy PN 198-0100-002, may be installed instead.

Repair kits consist of replacement lock lever, thrust washer, and O ring. (See Replaceable Parts List.)

To install:

a. Remove lock adjusting nut.

b. Pull lock lever out.

c. Remove thrust washer.

d. Replace thrust washer.

e. Install new lock lever and replace adjusting nut.

f. Install new O ring.

g. Reinstall hub adjustment nut. Tighten it until O ring presses firmly against reel when reel is locked. Check adjustment by installing and removing several reels.

4.18.6 MAGNETIC HEAD REPLACEMENT

Replacement heads are supplied as complete assemblies together with mounting plate and face shield. A write deskewing chart is supplied with each head.

a. Unplug head connectors.

b. Remove head mounting screw and remove head, passing connectors through the panel hole provided.

c. Be sure adjusting screw on replacement head is almost completely unscrewed.

d. Mount new head with mounting screw fairly loose. Screw in adjusting screw until point protrudes enough to engage its conical locating hole. Tighten mounting screw.

4.18.7 PHOTOSENSOR REPLACEMENT

a. Remove photosensor assembly by unplugging and removing mounting screws. Since it will not pass through the hole provided, the connector must be removed by cutting the cable. Retain the connector.

b. Replacement sensors are provided with connector pins crimped to wires but with connector shell not installed.

c. Replace assembly, passing wires through hole provided. Replace screws.

d. Snap pins into connector shell in same color sequence as in the shell removed and plug in.

e. Adjust as described in adjustment procedure.

4.18.8 MAGPOT REPLACEMENT (refer to Figure 4-8)

a. Unplug magpot cable.

b. Remove outer shell of magpot.

c. Using an Allen wrench, loosen linkage retaining screw and slip linkage retainer off shaft.

d. Detach two Phillips screws securing the magpot board to the tension arm mount.

e. Slide magpot assembly off shaft and install replacement magpot.

f. Consult magpot circuit description in the schematic portion for realignment procedures.

4.18.9 TAPE CLEANER REPLACEMENT

a. Remove circular snap-in plug cover.

b. Remove mounting screw and tape cleaner.

c. Mount new cleaner assembly with mounting screw finger tight.

d. Adjust cleaner surface so that it just touches the tape and is parallel to the tape surface.

e. Tighten mounting screw and install snap-in plug cover.

4.19 MODULE REPAIR

If in troubleshooting the difficulty is traced to a plug-in module it will usually not be too difficult to find the component at fault and repair the module. All parts used in the electronics are standard commercially available units and may be replaced by others of like type and rating. Normal good practice and workmanship should be exercised.

4.20 MAINTENANCE TOOLS

In addition to normal electronic tools and test gear: an oscilloscope, a voltohmmeter, etc., the following items should be available for service and repair.

Skewmaster Tape, PN 154-0036-001

Set of nut drivers or open end wrenches

Phillips and standard screwdrivers

Capstan puller, Kennedy PN 154-0001-001

Maintenance kit, Kennedy PN 190-2324-001, containing:

- Head cleaner
- Hex socket keys - 7/64, 5/32, 1/8, 3/32
- Lint-free swabs
- Reflective marker strips
- Magnasee visualizing solution
- Loctite grade H

Card extender, Kennedy PN 190-2224-001

Speed tester, Kennedy PN 190-4536-001

Alignment tool, Kennedy PN 154-0006-001

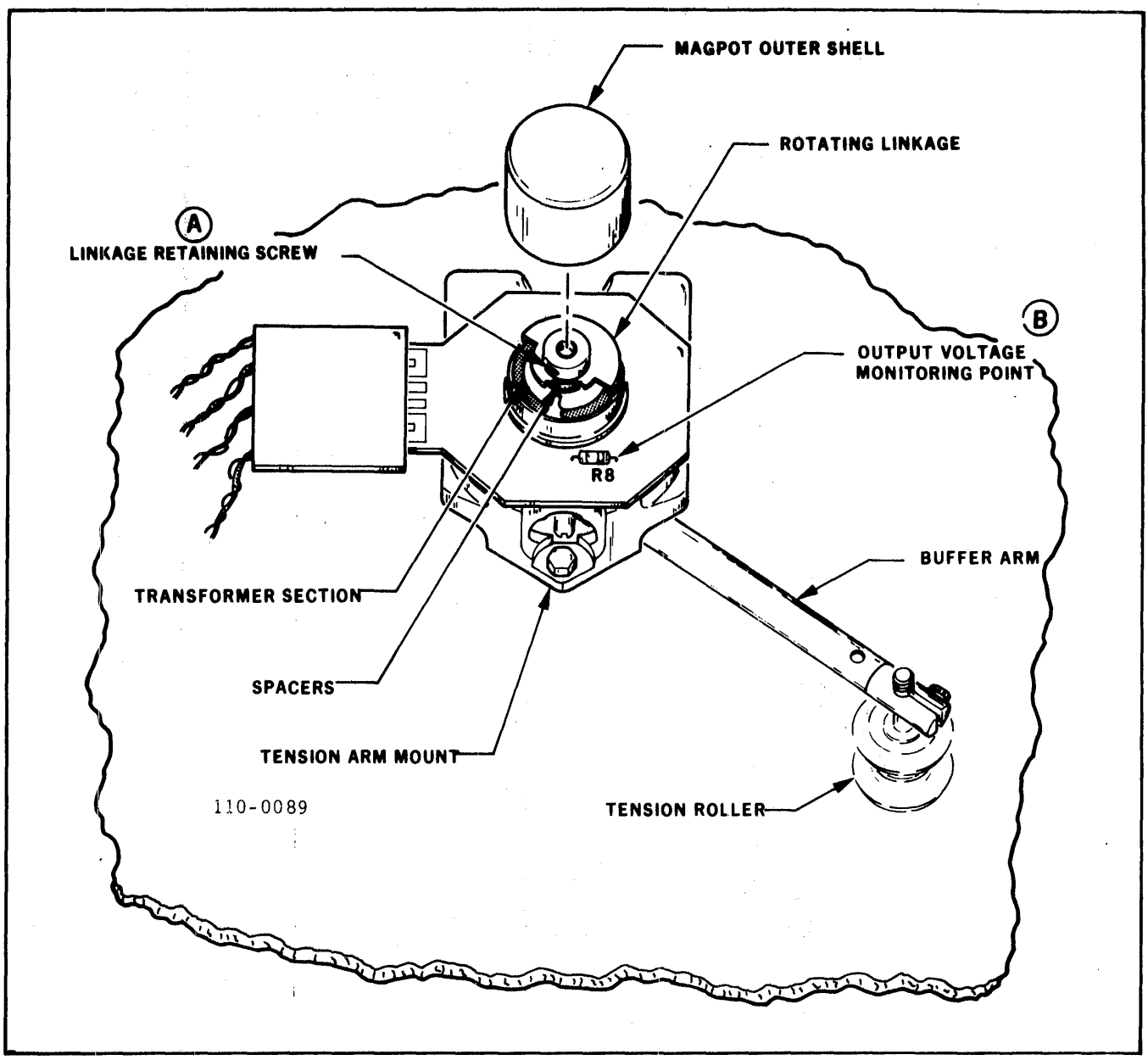


Figure 4–8. Magpot Assembly

SECTION V
PARTS IDENTIFICATION

SECTION V
PARTS IDENTIFICATION

5.1 SPARE PARTS ORDERING INFORMATION

This section describes the replaceable parts in your unit which are available only from Kennedy Company. Many parts of the unit are common commercial parts and can be obtained locally from the manufacturer. These parts are marked with the manufacturer's name and part number and are not listed herein.

The serial number and part number are the keys to numerous engineering details applying to your unit. These numbers are on the serial number tag located on the rear panel of the unit.

Changes to Kennedy units are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest circuit improvements developed in our Engineering Department. If a part you have ordered has been replaced by a new part, a Kennedy representative will advise you concerning any change in part number.

All parts orders should be addressed directly to Kennedy Company, Spare Parts Order Department, 1600 Shamrock Avenue, Monrovia, California 91016, telephone (213) 357-8831 or (213) 681-9314, TWX 910-585-3249.

5.2 IN-WARRANTY REPAIR PARTS ORDERING INFORMATION

Repair parts for in-warranty units are made available on an exchange basis through the Kennedy Company Spare Parts Department. The serial number and part number of the tape unit are necessary to insure shipment of the proper replacement parts.

All inquiries should be directed to Kennedy Company, Spare Parts Department, 1600 Shamrock Avenue, Monrovia, California 91016, telephone (213) 357-8831 or (213) 681-9314, TWX 910-585-3249.

5.3 EXPORT ORDERS

Customers outside the United States and Canada are served by Kennedy Company international sales agents. All correspondence regarding your unit should be directed to your sales agent. If you prefer, correspondence may be addressed directly to Kennedy Company, Spare Parts Department, 1600 Shamrock Avenue, Monrovia, California 91016, telephone (213) 357-8831 or (213) 681-9314, TWX 910-585-3249, cable KENNEDYCO.

5.4 ILLUSTRATED PARTS LIST

To assist in parts identification, an illustrated parts list is included in this section with references to photographs of the machine. Part numbers beginning with 198 are listed again in the Recommended Spare Parts list at the end of this section. Kennedy Company recommends that these parts be ordered as spares to minimize machine downtime due to equipment failure. Certain parts on this list have no quantity indicated. We recommend ordering one of each such parts for remote installations where delivery is time consuming.

5.5 FIELD KITS

Some replacement components may be supplied in the form of repair or field change kits. The repair kits contain parts that are matched or assembled and adjusted at the factory because of complexity or to aid the field technician. The components ordered as field kits either by correspondence with Kennedy service engineers or by direct order will be supplied with complete installation instructions. The change kits are intended for standard or special options not originally included in the unit.

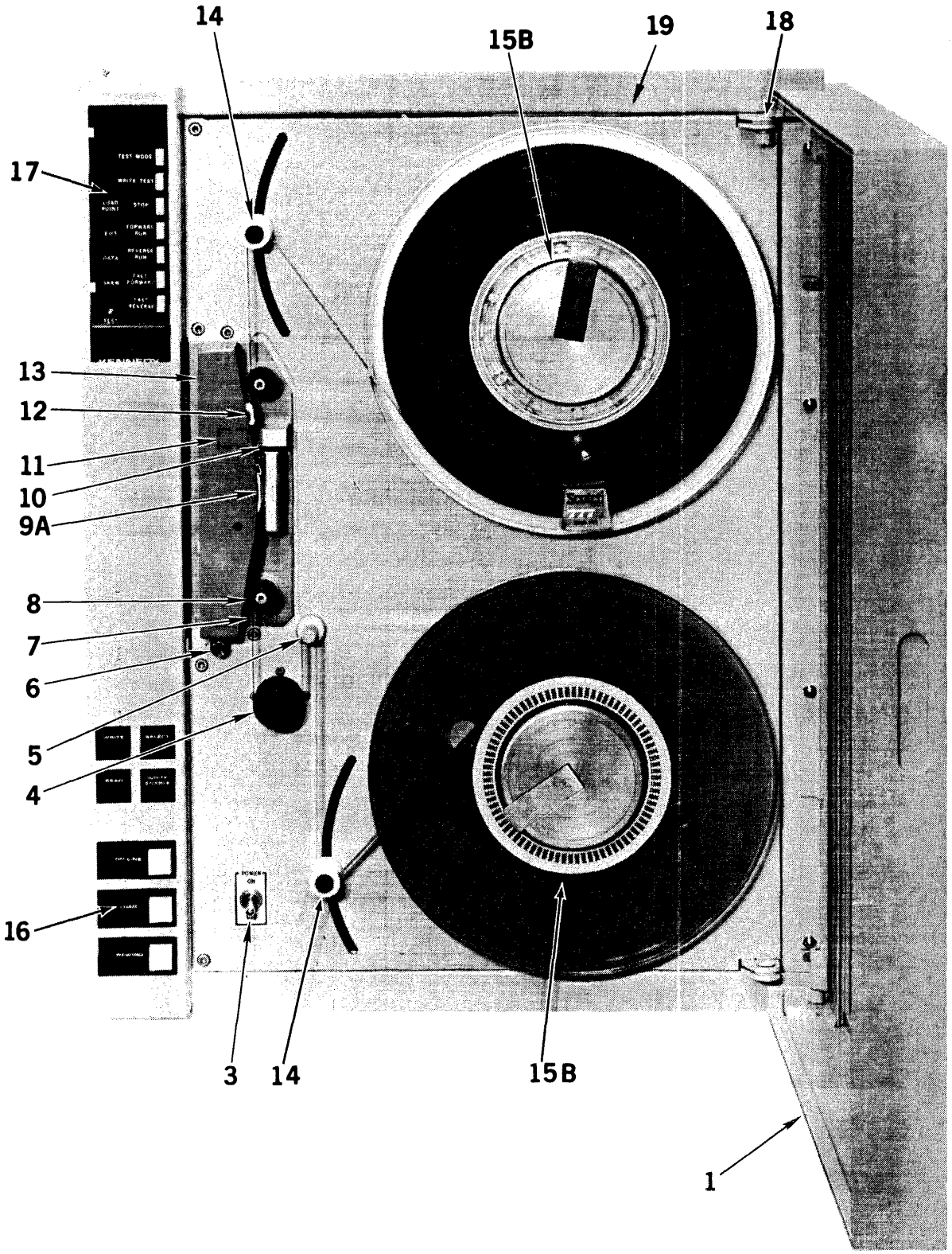


Figure 5-1. Parts Identification

ILLUSTRATED PARTS BREAKDOWN FOR FIGURE 5-1

Item No.	Part No.	Description	Notes
5-1-1	190-2609-011	Door Assy	
5-1-3	151-2001-201	Switch, DPST, AC Power (S4)	
5-1-4	190-2605-001	Capstan	
	128-0074-001	Screw, Hex Head, 6-32 x 3/16, Stl, B	
5-1-5	190-2627-001	Idler Assy	
5-1-6	128-0008-001	Screw, Captive	
5-1-7	391-3976-001	Plate, Guide	
5-1-8	190-1509-001	Split Tape Guide Assy	
5-1-9A	198-2399-010	Head and Head Mount Assy, Read After Write, 9 track	
5-1-9A	198-2399-003	Head and Head Mount Assy, Read After Write, 7 track	
5-1-9A	190-4420-001	Head Shield only	
5-1-10	*198-5906-001	IR Sensor EOT/BOT	
5-1-12	190-5858-001	Tape Cleaner Assy	
5-1-13	198-0056-006	Magnetic Head Cover Assy	
5-1-14	190-2647-002	Tension Roller Assy (25 ips)	
5-1-14	198-0012-001	Tension Roller Assy (37.5/45 ips)	
5-1-15B	190-2744-001	Quick Release Hub Bearing and Pulley Assy	
5-1-16	491-3820-xxx	Control Panel Cover only (single density models)	1
	491-3820-xxx	Control Panel Cover only (dual density models)	1
5-1-16	190-2512-012	Control Panel Assy (with density select switch panel)	
	190-2512-005	Control Panel Assy	
5-1-17	190-2817-001	Test Panel	
5-1-18	391-2909-007	Hinge, Dust Cover	
5-1-18	191-2939-001	Hinge Pin	
5-1-18	291-3980-001	Deck Hinge	
5-1-19	291-3980-002	Deck Hinge	
5-1-19	190-2249-011	Frame Assy	

*Replaces 198-1138-001, LP/EOT Photosensor, and 198-1139-001, BT Photosensor, after SN 10823. (198-5906-001 includes 190-5303-001 Connector board.)

NOTE 1: The last three dash numbers of these modules vary, depending on machine specifications. These dash numbers are stamped on the module, or may be found on the circuit card identification strip.

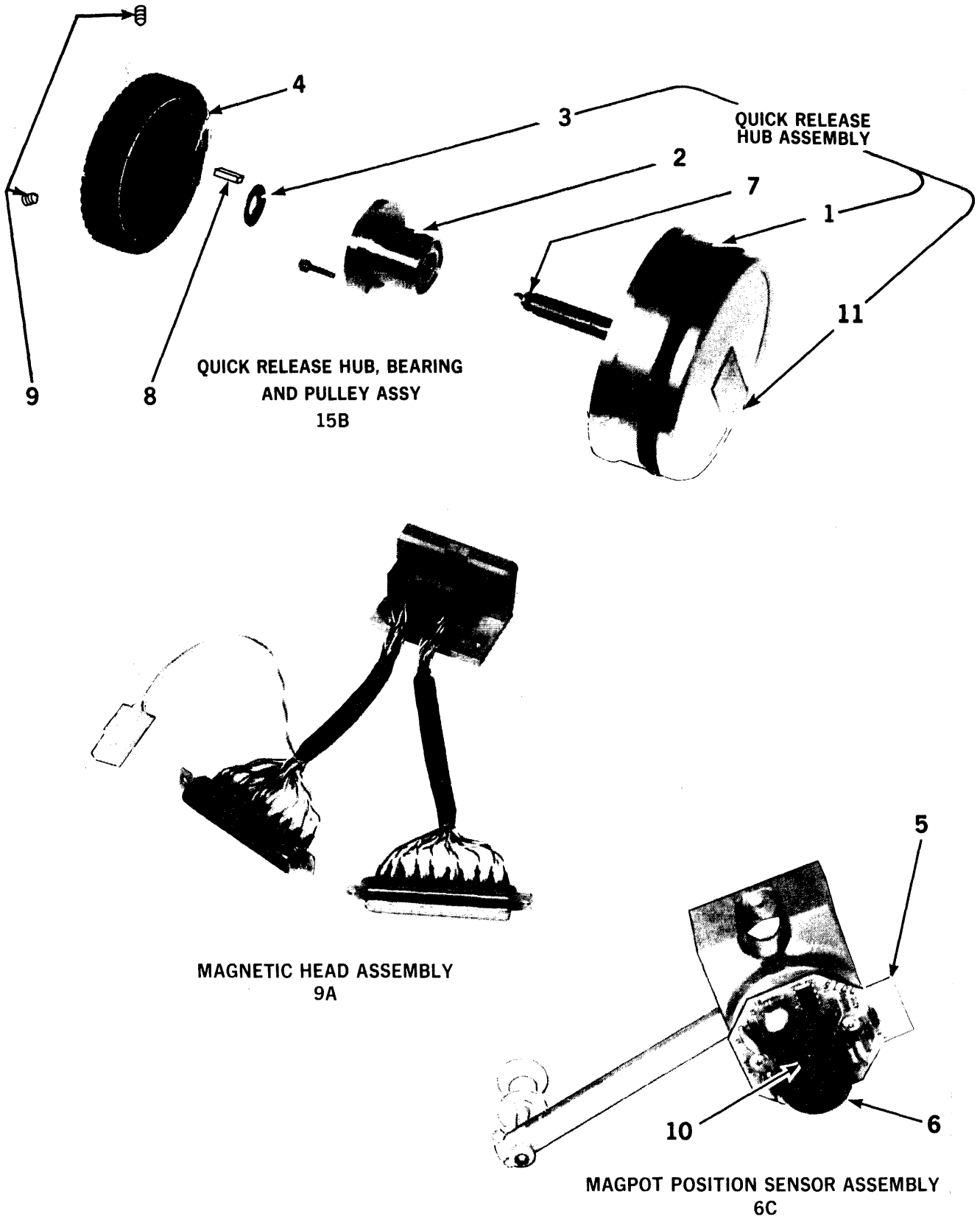


Figure 5-2. Parts Identification

ILLUSTRATED PARTS BREAKDOWN FOR FIGURE 5-2

Item No.	Part No.	Description	Qty	Notes
5-2-1	125-0030-006	O Ring (part of hub assy)		
5-2-2	198-0010-001	Hub Bearing Assy		
5-2-3	128-0090-001	Spring Washer, Belleville (part of hub assy)		
5-2-4	191-2643-002	Reel Drive Pulley		
5-2-5	190-4210-001	Magpot PC Board		
	190-4537-001	Magpot PC Board (for magpots w/optional limit sensor)		
5-2-6	191-4198-001	Cover		
5-2-7	128-0104-001	Nut, Hex, self-locking (part of hub assy)		
5-2-8	191-4274-001	Key		
5-2-9	128-1010-086	Setscrew, Allen 10-32 x $\frac{1}{2}$"		
5-2-10	190-4204-001	Rotor Assy (under cover)		
5-2-11	291-3446-003	Reel Drive Latch Assy (part of hub assy)		
5-2-11	191-3451-001	Thrust Washer (under latch, part of hub assy)		
Not shown	128-1090-001	Shim (.001" thick)	10	1
Not shown	128-1090-003	Shim (.003" thick)	10	1
Not shown	128-1090-005	Shim (.005" thick)	10	1

NOTE 1: These hub spacer shims are not normally required.

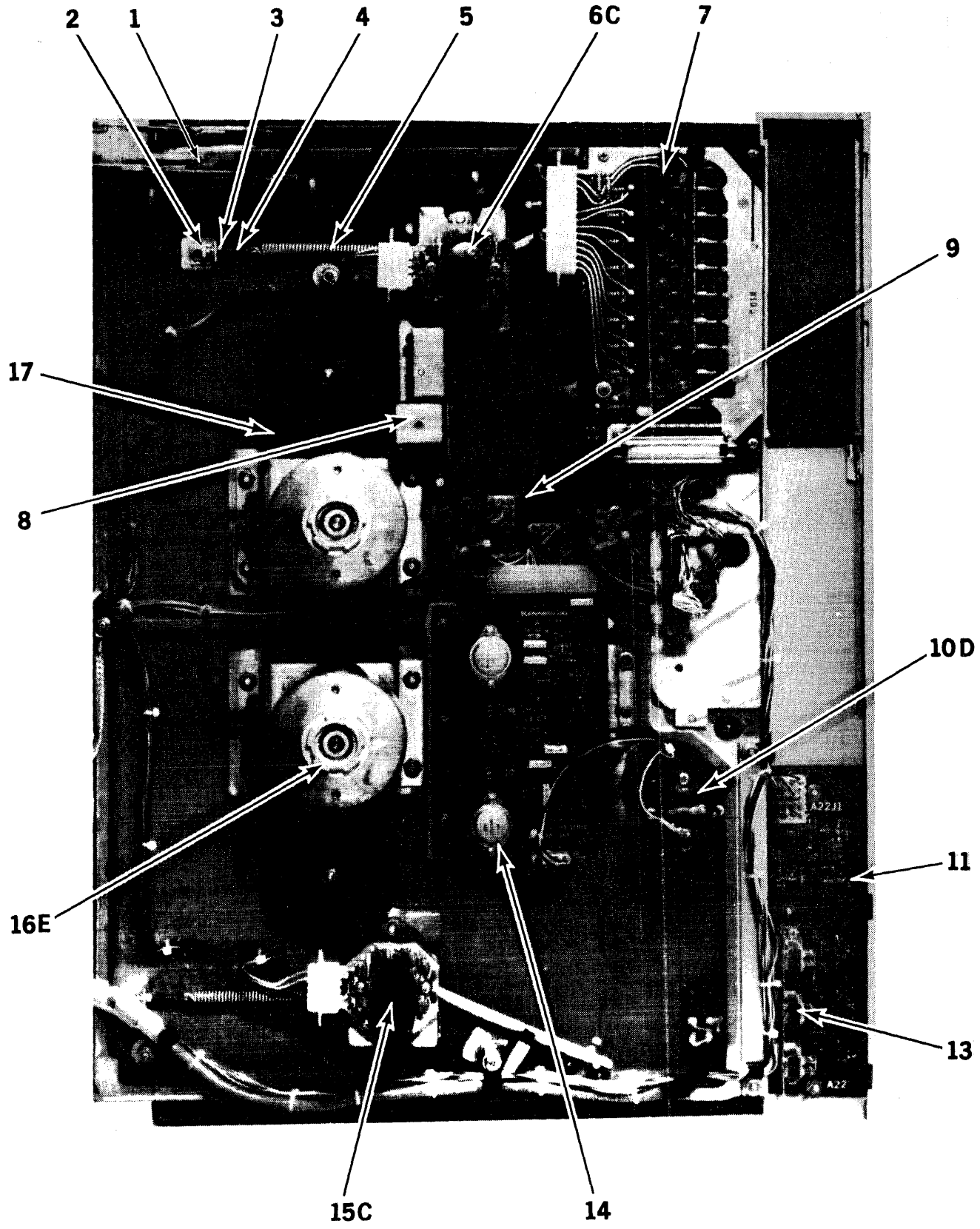


Figure 5-3. Parts Identification

ILLUSTRATED PARTS BREAKDOWN FOR FIGURE 5-3

Item No.	Part No.	Description
5-3-1	128-0033-001	Deck Latch, Left Hand
5-3-2	128-1064-001	Thumb Nut
5-3-3		Nut, Keps, 6-32
5-3-4	191-3982-001	Spring Tension Adjuster
5-3-5	125-0072-001	Extension Spring
5-3-6C	198-0009-003	Supply Magpot Sensor
	198-0009-005	Supply Magpot Sensor (w/optional limit sensor)
5-3-7	190-3935-001	Read Preamplifier Assy (25 ips 9 tk) (18.75 ips 7 tk)
5-3-7	190-3935-002	Read Preamplifier Assy (37.5 ips 9 tk) (25 ips 7 tk)
5-3-7	190-3935-003	Read Preamplifier Assy (45 ips 9 tk) (37.5 ips 7 tk)
5-3-7	190-3935-004	Read Preamplifier Assy (18.75 ips 9 tk) (10-15 ips 7 tk)
5-3-7	190-3935-005	Read Preamplifier Assy (10-15 ips 9 tk)
5-3-7	190-3935-006	Read Preamplifier Assy (45 ips 7 tk)
5-3-8	190-2641-001	File Protect Assy
5-3-9	*190-5303-001	Connector Board Assy
5-3-10	190-2710-003	Capstan Motor Tachometer Assy
5-3-11	198-3855-001	Control Pushbutton/Indicator Assy
5-3-13	151-0052-001	Switch, Pushbutton, 3 Station
	151-0053-001	Cover, Pushbutton Switch
	190-5181-001	Capstan Servo Amplifier
5-3-15C	198-0009-004	Takeup Magpot Sensor
	198-0009-006	Takeup Magpot Sensor (w/optional limit sensor)
5-3-16	198-0002-001	Reel Motor and Mounting Assy
5-3-17	125-0015-001	Reel Drive Belt
5-3-17	191-2644-001	Reel Drive Belt Pulley

*Replaces 190-4013-001 Connector board after SN 10823.

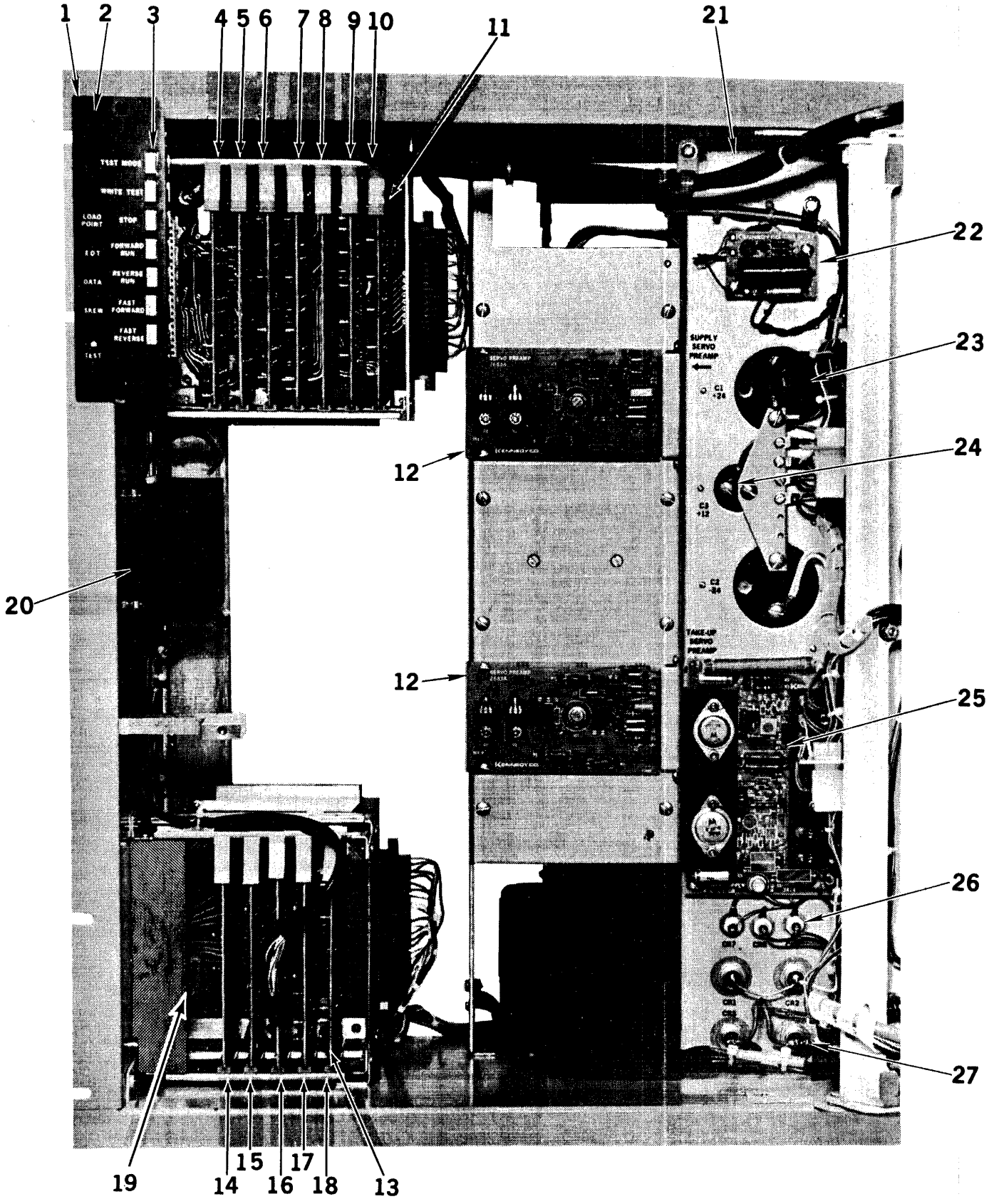


Figure 5-4. Parts Identification

ILLUSTRATED PARTS BREAKDOWN FOR FIGURE 5-4

Item No.	Part No.	Description	Notes
5-4-1	190-2817-001	Pushbutton/Indicator Test Panel Assy	
5-4-2	190-3864-001	Indicator Assy	
5-4-3	151-0054-001	Pushbutton Switch Assy, 7 Station	
5-4-4	190-3845-xxx	Delay Timing	1
	190-4118-xxx	Delay Timing (7 tk models)	1
	190-4209-xxx	Read Control Logic (PE models)	1
	190-4365-xxx	Dual Density Control (dual density models)	1
	190-4845-xxx	Delay Timing (Pertec compatible models)	1
5-4-5	190-4179-xxx	Read Amplifier/Clipping Control	1
	190-4188-xxx	Read Amplifier/Clipping Control (PE models)	1
	190-4367-xxx	Replaced by:	
	190-6367-xxx	Dual P Channel Clipping Control (dual density models)	1
5-4-6	190-4178-xxx	Quad Read Amplifier	1
	190-4139-xxx	Quad PE Read Detector (PE models)	1
	190-4385-xxx	Replaced by:	
	190-6385-xxx	Quad Read Amplifier (dual density models)	1
5-4-7	190-4178-xxx	Quad Read Amplifier	1
	190-4139-xxx	Quad PE Read Detector (PE models)	1
	190-4385-xxx	Replaced by:	
	190-6385-xxx	Quad Read Amplifier (dual density models)	1
5-4-8	190-3860-xxx	Data Terminator	1
5-4-9	190-3848-xxx	Four Channel Head Driver	1
	190-4207-xxx	Four Channel PE Write Amplifier (PE models)	1
	190-4366-xxx	Four Channel Write Amplifier (dual density models)	1
5-4-10	190-3849-xxx	Five Channel Head Drive	1
	190-4208-xxx	Five Channel PE Write Amplifier (PE models)	1
	190-4368-xxx	Five Channel Write Amplifier (dual density models)	1
5-4-11	190-4373-001	Dual Data Masterboard	
5-4-12	190-2683-002	Reel Servo Preamplifier Assy (25 ips)	
	190-4105-001	Reel Servo Preamplifier Assy (37.5 ips)	
	190-4905-045	Reel Servo Preamplifier Assy (45 ips)	
5-4-13	190-3858-001	Control Masterboard	
5-4-14	190-3841-xxx	Control Terminator	1
5-4-15	190-3842-xxx	Control Interface	1
	190-5002-xxx	Interface Control (TMZ compatible models)	1
5-4-16	190-3843-xxx	Pushbutton Control	1
	190-4843-xxx	Pushbutton Control	1
5-4-17	190-3645-xxx	Ramp Generator	1
5-4-18	190-3844-xxx	Sensor Amplifier/Driver	1
5-4-19	151-0034-001	Thumbwheel Switch, 1 to 4	
	151-0034-006	Thumbwheel Switch, 0 to 3	
5-4-20	190-6810-001	Voltage Regulator Assy, +5 vdc	
5-4-21	190-2379-002	Power Supply Assy	
5-4-22	190-3067-001	Time Delay Assy	
5-4-23	115-3625-559	Capacitor, Electrolytic, 55,000 mfd, 25v (C1 and C2)	
5-4-24	115-0020-209	Capacitor, Electrolytic, 20,000 mfd, 15v (C3)	
5-4-25	190-6414-001	Voltage Regulator Assy, +10 vdc	
5-4-26	148-0063-001	Rectifier, 1N1200A (CR5,6, and 7)	
5-4-27	148-0085-001	Rectifier, 1N1183 (CR1,2,3, and 4)	
	148-0162-001	Rectifier, 1N3900 (DC units)	

NOTE 1: The last three dash numbers of these modules vary, depending on machine specifications. These dash numbers are stamped on the module, or may be found on the circuit card identification strip.

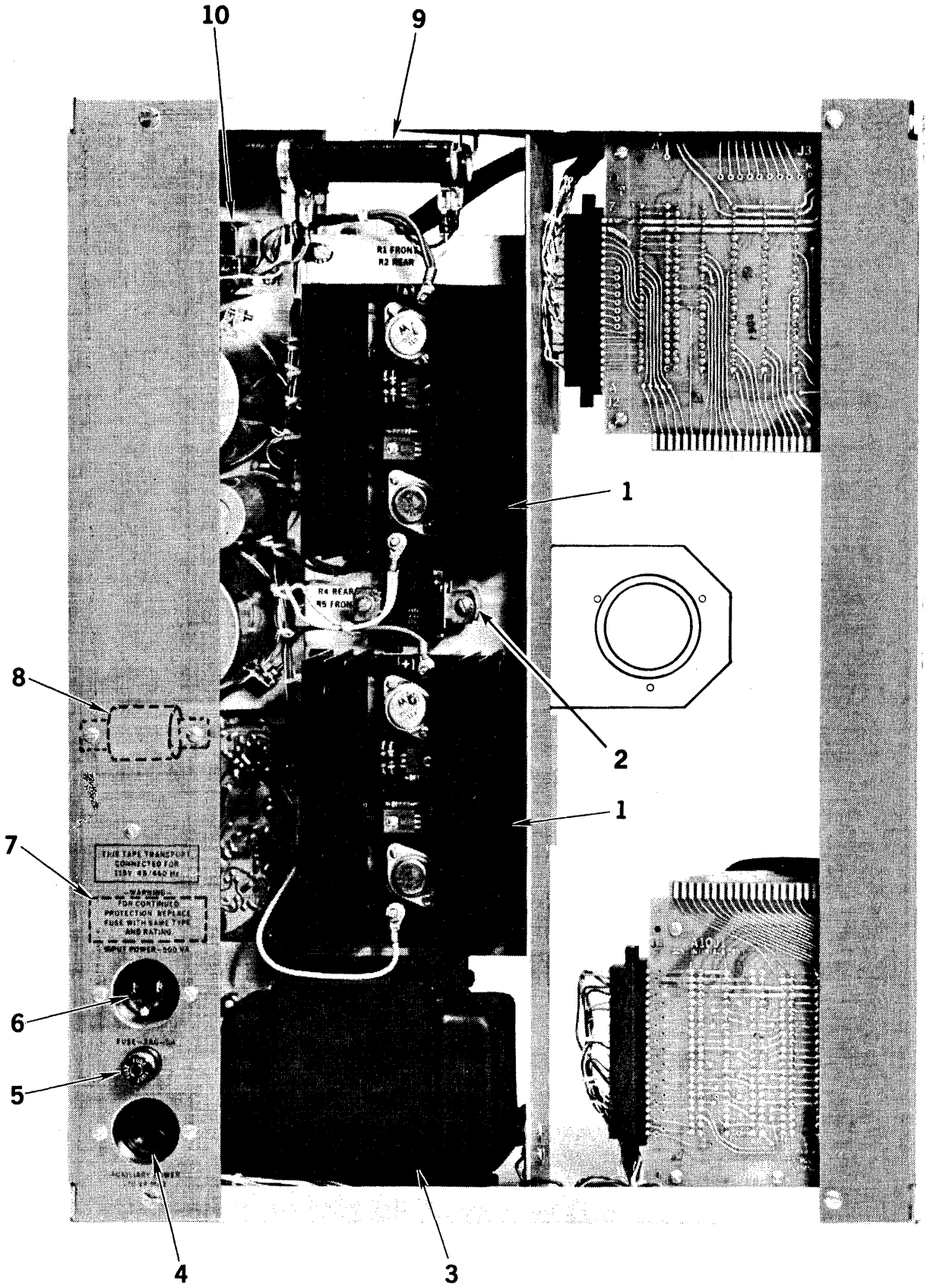


Figure 5-5. Parts Identification

ILLUSTRATED PARTS BREAKDOWN FOR FIGURE 5-5

Item No.	Part No.	Description
5-5-1	190-3191-001	Reel Servo Power Amplifier Assy (25 ips)
	190-4111-001	Reel Servo Power Amplifier Assy (37.5 ips)
	190-4911-001	Reel Servo Power Amplifier Assy (45 ips)
5-5-2	147-1530-250	Resistor, Wire Wound, 25 ohm, 30w (R4 & R5)
5-5-3	198-0001-001	Transformer (T1)
5-5-4	121-9001-002	Receptacle, Female, Auxiliary Output
5-5-5	151-0802-001	Fuseholder
5-5-5	198-0133-050	Fuse, 3AG, 5A (115v use) (5 per pkg)
5-5-5	198-0133-030	Fuse, 3AG, 3A (230v use) (5 per pkg)
5-5-6	121-9001-003	Receptacle, Male, AC input (115v use)
5-5-6	121-9000-003	Power Cord (115v use) (not shown)
5-5-6	127-0003-001	Receptacle, Male, AC Input (230v use) (Not shown; includes RFI line filter)
	121-0198-004	Power Cord (230v/240v use) (not shown)
5-5-7	127-0004-001	115v RFI Line Filter
5-5-8	147-1530-030	Resistor, Wire Wound, 3 ohm, 30w (R3)
5-5-9	147-0022-002	Resistor, Wire Wound, 5 ohm, 100w (R1 & R2)
5-5-9	147-0022-001	Resistor, Wire Wound, 2 ohm, 30w (R3) (45 ips models only)
5-5-10	145-0005-001	Relay K1

RECOMMENDED SPARE PARTS

(Certain parts in this list have no quantity indicated. For remote installations where parts delivery is time consuming we recommend ordering one of each of these parts as required for your machine in addition to the recommended quantities of the regular spares.)

Item No.	Part No.	Description	Qty	Notes
5-1-4	190-2605-001	Capstan	1	
5-1-5	190-2627-001	Idler Assy	1	
5-1-8	190-1509-001	Split Tape Guide Assy	1	
5-1-9	198-2399-010	Head and Head Mount Assy	1	
5-1-9	198-2399-003	Head and Head Mount Assy, RAW (7 tk)	1	
5-1-10	*198-5906-001	IR Sensor EOT/BOT	1	
5-1-13	198-0056-006	Magnetic Head Cover Assy		
5-1-14	190-2647-002	Tension Roller Assy (25 ips)	2	
5-1-14	198-0012-001	Tension Roller Assy (37.5 ips/45 ips)	2	
5-2-2	198-0010-001	Hub Bearing Assy	1	
5-3-5	125-0072-001	Extension Spring	1	
5-3-6C	190-4210-001	Magpot PC Board	2	
5-3-6C	190-4537-001	Magpot PC Board (used in magpots w/limit sensors)	2	
5-3-7	190-3935-001	Read Preamplifier Assy (25 ips)	1	
5-3-7	190-3935-002	Read Preamplifier Assy (37.5 ips)	1	
5-3-7	190-3935-003	Read Preamplifier Assy (45 ips)	1	
5-3-7	190-3935-004	Read Preamplifier Assy (556/800 cpi)	1	
5-3-7	190-3935-005	Read Preamplifier Assy (12.5 ips)	1	
5-3-7	190-3935-006	Read Preamplifier Assy (7 tk, 45 ips)	1	
5-3-8	190-2641-001	File Protect Assy	1	
5-3-9	190-5303-001	Connector Board	1	
5-3-10	190-2710-003	Capstan Motor Tachometer Assy	1	
5-3-11	198-3855-001	Control Pushbutton/Indicator	1	
5-3-14	190-5181-001	Capstan Servo Amplifier	1	
5-3-16	198-0002-001	Reel Motor Assy and Mounting Assy	1	
5-3-17	125-0015-001	Belt, Reel Drive	2	
5-4-1	190-2817-001	Pushbutton/Indicator Test Panel Assy	1	
5-4-4	190-3845-xxx	Delay Timing	1	1
5-4-4	190-4118-xxx	Delay Timing (7 tk models)	1	1
5-4-4	190-4209-xxx	Read Control Logic (PE models)	1	1
5-4-4	190-4365-xxx	Dual Density Control (dual density models)	1	1
5-4-4	190-4845-xxx	Delay Timing (Pertec compatible models)	1	1
5-4-5	190-4179-xxx	Read Amplifier/Clipping Control	1	1
5-4-5	190-4188-xxx	Read Amplifier/Clipping Control (PE models)	1	1
5-4-5	190-4367-xxx	Replaced by:		
	190-6367-xxx	Dual P Channel/Clipping Control (dual density models)	1	1
5-4-6	190-4178-xxx	Quad Read Amplifier	1	1
5-4-6	190-4139-xxx	Quad PE Read Detector (PE models)	1	1
5-4-6	190-4385-xxx	Replaced by:		
	190-6385-xxx	Quad Read Amplifier (dual density models)	1	1
5-4-7	190-4178-xxx	Quad Read Amplifier	1	1
5-4-7	190-4139-xxx	Quad PE Read Detector (PE models)	1	1
5-4-7	190-4385-xxx	Replaced by:		
	190-6385-xxx	Quad Read Amplifier (dual density models)	1	1
5-4-8	190-3860-xxx	Data Terminator		1

*Replaces 198-1138-001, LP/EOT Photosensor, and 198-1139-001, BT Photosensor, after SN 10823. (198-5906-001 includes 190-5303-001 Connector board.)

See last page for notes)

RECOMMENDED SPARE PARTS

Item No.	Part No.	Description	Qty	Notes
5-4-9	190-3848-xxx	Four Channel Head Driver	1	1
	190-4207-xxx	Four Channel PE Write Amplifier (PE models)	1	1
	190-4366-xxx	Four Channel Write Amplifier (dual density models)	1	1
5-4-10	190-3849-xxx	Five Channel Head Driver	1	1
	190-4208-xxx	Five Channel PE Write Amplifier (PE models)	1	1
	190-4368-xxx	Five Channel Write Amplifier (dual density models)	1	1
5-4-12	190-2683-002	Reel Servo Preamplifier Assy (25 ips)	1	
	190-4105-001	Reel Servo Preamplifier Assy (37.5 ips)	1	
	190-4905-045	Reel Servo Preamplifier Assy (45 ips)	1	
5-4-14	190-3841-xxx	Control Terminator		1
5-4-15	190-3842-xxx	Control Interface	1	1
	190-5002-xxx	Interface Control (TMZ compatible models)	1	1
5-4-16	190-3843-xxx	Pushbutton Control	1	1
	190-4843-xxx	Pushbutton Control	1	1
5-4-17	190-3645-xxx	Ramp Generator	1	1
5-4-18	190-3844-xxx	Sensor Amplifier Driver	1	1
5-4-19	151-0034-001	Thumbwheel Switch, 1 to 4 (optional)		
5-4-20	190-6810-001	Voltage Regulator Assy, +5v	1	
5-4-22	190-3067-001	Time Delay Assy	1	
5-4-23	115-3625-559	Capacitor, Electrolytic, 55,000 mfd, 25 vdc	1	
5-4-24	115-0020-209	Capacitor, Electrolytic, 20,000 mfd, 15 vdc	1	
5-4-25	190-6414-004	Voltage Regulator Assy, +10 vdc	1	
5-4-26	148-0063-001	Rectifier, 1N1200A (CR5, 6, 7)	2	
5-4-27	*148-0085-001	Rectifier, 1N1183 (CR1, 2, 3, 4)	4	
5-5-1	190-3191-001	Reel Servo Power Amplifier (25 ips)	2	
5-5-1	190-4111-001	Reel Servo Power Amplifier (37.5 ips)	2	
5-5-1	190-4911-001	Reel Servo Power Amplifier (45 ips)	2	
5-5-5	198-0133-050	Fuse, 3AG, 5A (115v use)		
5-5-5	198-0133-030	Fuse, 3AG, 3A (230v use)		
	198-0057-001	Brush Replacement Kit, Capstan Motor	1	
	198-0059-001	Brush Replacement Kit, Reel Motor	1	
5-5-6	121-9000-003	Power Cord (115v use) (not shown)	1	
5-5-6	125-0068-001	Power Cord (230v use) (not shown)	1	
	198-0100-001	Hub Repair Kit (includes O ring, latch and thrust washer)	1	
Not shown	190-4147-001	Multiple Transport Adapter PC Board	1	
	*148-0162-001	Rectifier, 1N3900 (DC units)	1	

TOOLS

	154-0001-001	Capstan Puller	1
	190-2324-001	Maintenance Kit	1
	190-2224-001	Card Extender	1
	198-4536-001	Speed Tester	1
	154-0006-001	Alignment Tool	1

NOTE 1: The last three dash numbers of these modules vary, depending on machine specifications. These dash numbers are stamped on the module, or may be found on the circuit card identification strip.

SECTION VI
WIRING AND SCHEMATIC DIAGRAMS

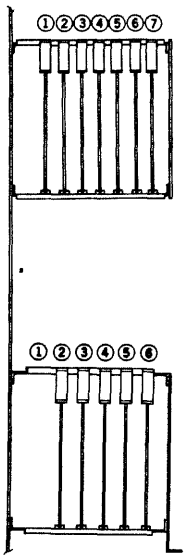
SECTION VI

WIRING AND SCHEMATIC DIAGRAMS

This section contains the wiring diagrams, schematic diagrams, and circuit descriptions for the individual circuit cards used in the transport. The schematics are arranged by functional group as shown below.

Electronics symbols used in the drawings conform to MIL-STD-15. Abbreviations conform to MIL-STD-12 unless otherwise specified.

Functional Group	Module Name and Type
Overall	System Wiring Diagram
	Control Masterboard Assembly
	Data Masterboard Assembly
	Power Supply
Control Electronics	Control Terminator
	Interface Control
	Tape Motion Controls including Pushbutton Control, Main Control, and Test Panel Control
	Ramp Generator
	Sensor Amplifier/Driver
	Connector Board
Servo System	Capstan Servo Amplifier
	High Speed Capstan Servo Amplifier
	Reel Servo System
	High Speed Reel Servo Preamplifier
	High Speed Servo Power Amplifier
	Magpot
Read Electronics	Data Terminator
	Read Preamplifier
	Read Control Logic including Delay Timing
	Quad Read Amplifier
	Read Amplifier/Clipping Control
Write Electronics	Write Amplifier, Four Channel
	Write Amplifier, Five Channel



CIRCUIT CARD IDENTIFICATION		
LOC	**TYPE**	**FUNCTION**
READ/WRITE SECTION		
1	4365-003	DUAL DENSITY CONTROL
2	6367-003	DUAL P CHANNEL/CLIPPING
3	6385-003	QUAD READ AMPLIFIER
4	6385-003	QUAD READ AMPLIFIER
5	3860-001	DATA TERMINATOR
6	4366-003	4 CHANNEL WRITE AMPL
7	4368-001	5 CHANNEL WRITE AMPL
CONTROL SECTION		
2	3841-001	CONTROL TERMINATOR
3	3842-001	CONTROL INTERFACE
4	3843-001	PUSHBUTTON CONTROL
5	3645-010	RAMP GENERATOR
6	3844-001	SENSOR AMPLIFIER/DRIVER

MODEL	**PART NO.**	**INTERFACE**
9000	192-9000-147	STD
SPEED	**DENSITY**	**TRACKS**
45 IPS	800/1600 CPI	9
MODIFICATIONS		
DENSITY SELECT SWITCH		

NOTES TO SCHEMATIC SECTION

Certain conventions have been observed in preparing schematics for this manual:

1. Resistor values are given in ohms. If wattage is unspecified the resistor may be either 1/4 or 1/2 watt.

2. Capacitor values may be given in picofarads or microfarads. Those values for which neither designation is provided are assumed to be obvious from circuit function. Filter capacitors on certain supply lines do not have logic significance. In general, they are not shown on schematics. On PC board silkscreens they are designated as CF.

3. Normally, IC power connections are on pins 14 (+5v) and 7 (ground) for 14 pin packages, and 16 (+5v) and 8 (ground) for 16 pin packages. Some ICs — 7476, 7492, 7493 for example — have power connections on pin 5 (+5v) and pin 10 (ground). Operational amplifiers in the 8 pin package have power connections on pin 4 (-Vcc) and pin 7 (+Vcc). Power connections are not shown unless they are nonstandard.

4. Where multiple inputs are tied together only one pin may be designated on the schematic.

5. Unused inputs that are tied high are not normally indicated unless the connection has logic significance.

6. From and to designations are intended to describe inputs and outputs only. The same signal may be connected to several other points not shown on a particular drawing.

7. Abbreviations used in from and to designations are as follows:

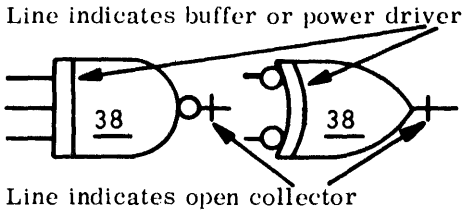
CI	Control Interface
PBC	Pushbutton Control
RG	Ramp Generator
SA	Sensor Amplifier/Driver
DT	Delay Timing
RA/CL	Read Amplifier/Clipping Level
RA	Quad Read Amplifier
WA1	Four Channel Write Amplifier
WA2	Five Channel Write Amplifier

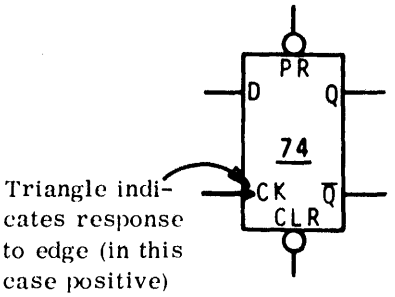
8. Positive logic is shown for all internal connections. Interface connections are zero true but the bar is omitted.

9. Integrated circuit symbols contain a circuit designator that corresponds to the number silkscreened onto the circuit module above an underlined number representing the IC type.

   The IC type number is abbreviated and omits the portions of the manufacturer's type number pertaining to case and vendor identification. Further, since the TTL 7400 series makes up most of the circuitry, the 74 is omitted on these. Thus a 00 designation indicates a 7400 quad two input NAND gate. T.I.'s complete part number is SN7400N. In multifunctional units in close proximity to each other the type designation may be omitted. The type designation may appear outside the symbol if the symbol is too small.

   Military Standard 806C is the base for logic symbols. Additional conventions are shown below.



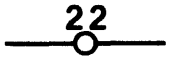


10. Semiconductor types on schematics may be replaced by their functional equivalents. If not indicated, diodes are 1N914, NPN transistors are 2N2714, and PNP transistors are MPS6517.

11. Unless otherwise specified, light emitting diodes are FLV102 or equivalent.

12. Module connector pins are shown as

where no further connection is shown on the schematic, and as



when there is a connection shown.

13. Where an input is represented by an arrow instead of a complete line, the input source is designated. Where outputs are so shown their destinations may not be shown.

14. Some schematics of modules include certain external elements which aid in understanding the circuit function. In this case all the connections to the element may not be shown in the interest of clarity.

15. 

designates a test point provided on the module. Letters proceed from top to bottom of card with the ground test point, if present, as the bottommost terminal.

16. Socket terminals are designated with numbers for component side connections and letters for circuit side connections when a double sided socket is used. These are the designations on the socket. When a single sided socket is provided, all connections are designated by letters regardless of which side of the board they lie on the etch. Letters follow the 22 pin alphabet, ABCDEFHJKLMNPRSTUVWXYZ; numbers are 1 through 22.

MODEL 9000 TAPE TRANSPORT

SIGNAL ORIGIN/DESTINATION LIST

Signal	From	To
A.SLT1	A10J1-W Control Masterboard Interface Connector	J8-0 Address Select Connector; Rotary Thumbswitch, Front Panel
A.SLT2	A10J1-X Control Masterboard Interface Connector	J8-1 Address Select Connector; Rotary Thumbswitch, Front Panel
A.SLT3	A10J1-Y Control Masterboard Interface Connector	J8-2 Address Select Connector; Rotary Thumbswitch, Front Panel
A.SLT4	A10J1-2 Control Masterboard Interface Connector	J8-3 Address Select Connector; Rotary Thumbswitch, Front Panel
BKN	Pin W, Sensor Amplifier/Driver PCB	Pin 18, Sensor Amplifier Driver PCB; Pin U, Pushbutton Control PCB; Pin X, Interface Control PCB
BKNSENS	A7J2-1, 5303 Connector PCB	A1073-D, Control Masterboard; Pin W, Sensor Amplifier Driver PCB
BSY/	Pin 13, Pushbutton Control PCB	1. Pin 13, Sensor Amplifier Driver PCB 2. Pin N, Interface Control PCB 3. A10J4P, Control Masterboard; A11J4P, Data Masterboard; Pin Z, Delay Timing PCB; Pin Y, P Channel Amplifier/Clipping PCB
CURRENT SENSOR+	J1-1, 4911 Servo Power Amplifier PCB	J1-2, 4905 Reel Servo Preamplifier PCB
CURRENT SENSOR-	J1-4, 4911 Servo Power Amplifier PCB	J1-1, 4905 Reel Servo Preamplifier PCB
+CLIP	Pin P, P Channel Read Amplifier/Clipping Control PCB	Pin P, Quad Read Amplifier PCB
-CLIP	Pin R, P Channel Read Amplifier/Clipping Control PCB	Pin R, Quad Read Amplifier PCB
CLIPPING LEVEL DEFEAT/	A11J1-1, Data Masterboard Interface Connector	Pin N, P Channel/Clipping PCB
DATA LAMP	Pin Y, Delay Timing PCB	A11J4-F, Data Masterboard; A10J4-F, Control Masterboard; Pin E, Pushbutton Control PCB; J1-6 Test Connector; A23J1-H, Test Panel
DATA TRANSFER	Pin M, Delay Timing PCB	Pin U, P Channel/Clipping Control PCB; Pin U, Quad Read Amplifier PCB
EOT SENSOR	A7J3-1, 5303 Connector PCB	A7J2-10, 5303 Connector PCB; A10J3-B, Control Masterboard; Pin Z, Sensor Amplifier Driver PCB; (becomes EOT)
EOT	Pin 20 Interface Control PCB	A10J1-U, Control Masterboard (to Interface)
EOT1	Pin X, Sensor Amplifier/Driver PCB	Pin Z, Interface Control PCB (becomes EOT2)
EOT2	Pin E, Interface Control PCB	Pin 22, Pushbutton Control PCB
ERS HD DR	Pin J, Sensor Amplifier/Driver PCB	A10J3-S, Control Masterboard; A7J2-2, 4013 Connector PCB
FPT CONTACT	A7J2-6, 5303 Connector PCB	A10J3-H, Control Masterboard; Pin T, Sensor Amplifier Driver PCB
FPT/	Pin 9, Sensor Amplifier/Driver PCB	Pin J, Interface Control PCB; A10J1-P, Control Masterboard

Signal	From	To
FPTSOL	Pin P, Sensor Amplifier/Driver PCB	A10J3-L, Control Masterboard; A7J2-9, 4013 Connector PCB
f_R	Pin F, Delay Timing PCB	Pin 5, 4 Channel Write Amplifier PCB; A11J4-Y, Data Masterboard, A10J4-Y, Control Masterboard; Pin N, Ramp Generator PCB
f1	Pin J, Delay Timing PCB	Pin F, 4 Channel Write Amplifier PCB; Pin F, 5 Ch Amplifier PCB
GAP DETECT	Pin H, Delay Timing PCB	A11J1-M, Data Masterboard; Data Interface Connector
HDI	Pin B, Delay Timing PCB	A11J4-M, Data Masterboard; A10J4-M, Control Masterboard; A10J1-F, Control Masterboard; Control Interface Connector
HDS	Pin A, Delay Timing PCB	A11J4-L, Data Masterboard; A10J4-L, Control Masterboard; A10J1-D, Control Masterboard; Control Interface Connector
LDP/	Pin 15, Interface Control PCB	Pin 5, Control Terminator PCB; A10J1-R, Control Masterboard
LOAD/	Pin V, Pushbutton Control PCB	Pin U, Sensor Amplifier Driver PCB; A10J3-F, Control Masterboard
LP	Pin 19, Sensor Amplifier/Driver PCB	1. A10J4-V, Control Masterboard; A11J4-V, Data Masterboard; Pin W, Delay Timing PCB 2. Pin 21 Pushbutton Control PCB 3. Pin Y, then Pin 17 Interface Control PCB; A10J1-R, Control Masterboard
LP SENS	A7J3-2, 5303 Connector PCB	A7J2-7, 5303 Connector PCB, A10J3-C, Control Masterboard; Pin Y, Sensor Amplifier Driver PCB (becomes LP PULSE)
LP PULSE	Pin 8, Sensor Amplifier/Driver PCB	Pin H, Pushbutton Control PCB
MAGPOT OUTPUT	J1-4 Magpot PCB (supply or takeup)	J1-9, Reel Servo Preamplifier PCB (supply or takeup)
MODIFIED TACHOMETER OUTPUT	J1-3 Capstan Servo Amplifier PCB	J1-5, 6 Reel Servo Preamplifier
MTR GRD	R4-A, Terminal Block	J1-2, Servo Power Amplifier PCB
OFFC	Control Interface Connector	A10J1-L, Control Masterboard; Pin 13, Interface Control PCB
OFFC1/	Pin M, Interface Control PCB	Pin 12, Pushbutton Control PCB
ONL/	Pin 14, Pushbutton Control PCB	Pin R, Interface Control PCB; A10J1-M, Control Masterboard
ONL INHIBIT	A22J1-4, Main Control Panel	A10J3-J Control Masterboard; Pin T, Pushbutton Control PCB
ONL LAMP	Pin P, Pushbutton Control PCB	A10J3-V, Control Masterboard; A22J1-11, Main Control Panel
OVW	A10J1-B, Control Interface Connector	Pin B, Interface Control PCB
PEAK PULSE	Pin V, Quad Read Amplifiers; P Channel/Clipping PCB	Pin R, Delay Timing PCB
POWER SERVO DRIVE	J1-11, 4905 Reel Servo Preamplifier PCB	J1-3, 4911 Servo Power Amplifier PCB
+POWER SERVO DRIVE	J1-2, 4105 Reel Servo Preamplifier PCB	J1-1, 4111 Servo Power Amplifier PCB
-POWER SERVO DRIVE	J1-1, 4105 Reel Servo Preamplifier PCB	J1-4, 4111 Servo Power Amplifier PCB

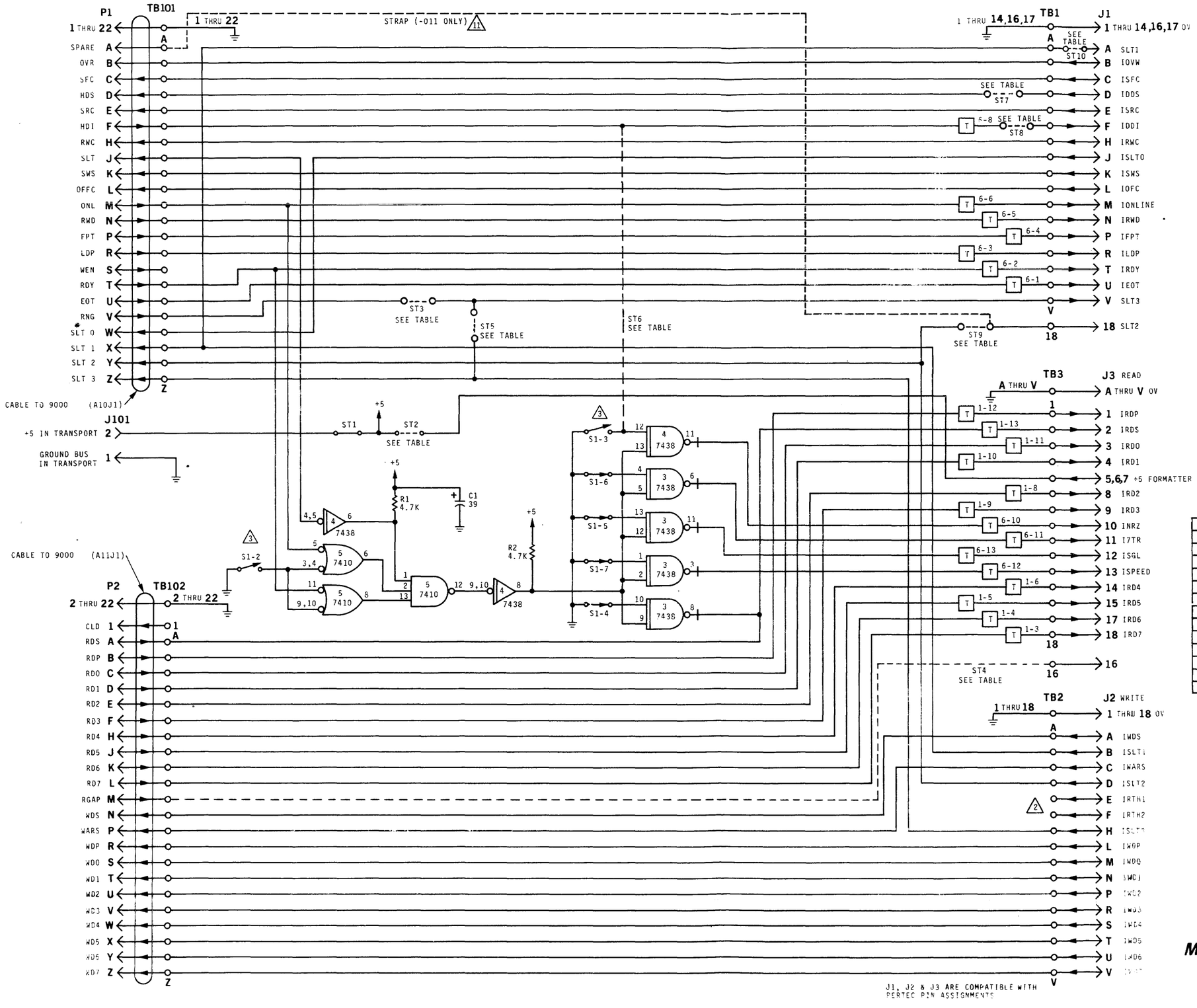
Signal	From	To
RAMP OUT	Pin L, Ramp Generator PCB	Pin 1, Capstan Servo PCB
RDP(C)1	Pin Z, P Channel/Clipping Control PCB	A11J1-B, Data Masterboard Interface Connector
RDS	Pin P, Delay Timing PCB	A11J1-A, Data Masterboard Interface Connector
RDY	Pin 9, Interface Control PCB	A10J1-T, Control Masterboard (derived from TNG/)
RD0/	Pin W, Quad Read Amplifier PCB (Location 3, Data Masterboard)	A11J1-C, Data Masterboard Interface Connector
RD1/	Pin X, Quad Read Amplifier PCB (Location 3, Data Masterboard)	A11J1-D, Data Masterboard Interface Connector
RD2/(B)	Pin Y, Quad Read Amplifier PCB (Location 3, Data Masterboard)	A11J1-E, Data Masterboard Interface Connector
RD3(A)/1	Pin Z, Quad Read Amplifier PCB (Location 3, Data Masterboard)	A11J1-F, Data Masterboard Interface Connector
RD4(8)/1	Pin W, Quad Read Amplifier PCB (Location 4, Data Masterboard)	A11J1-H, Data Masterboard Interface Connector
RD5(4)/1	Pin X, Quad Read Amplifier PCB (Location 4, Data Masterboard)	A11J1-J, Data Masterboard Interface Connector
RD6(2)/1	Pin Y, Quad Read Amplifier PCB (Location 4, Data Masterboard)	A11J1-K, Data Masterboard Interface Connector
RD7(7)/1	Pin Z, Quad Read Amplifier PCB (Location 4, Data Masterboard)	A11J1-L, Data Masterboard Interface Connector
RD LAMP/	Pin K, Sensor Amplifier Driver PCB	A10J3-R, Control Masterboard; A22J1-15, Main Control Panel
REEL MOTOR VOLTAGE SENSE	J1-3, 4111 Servo Power Amplifier PCB	J1-11, 4105 Reel Servo Preamplifier PCB
READ SIG P(C)1	Read Head Winding	A15J3-32, 13, Read Preamplifier PCB; A15J1-3, Read Preamplifier PCB; A11J3-T, Data Masterboard; Pin E, P Channel/Clipping PCB
READ SIG0	Read Head Winding	A15J3-36, 17, Read Preamplifier PCB; A15J1-1, Read Preamplifier PCB; A11J3-S, Data Masterboard, Pin J, Quad Read Amplifier PCB (lLocation 3, Data Masterboard)
READ SIG1	Read Head Winding	A15J3-34, 15, Read Preamplifier; A15J1-2, Read Preamplifier PCB; A11J3-R, Data Masterboard; Pin H, Quad Read Amplifier PCB (Location 3, Data Masterboard
READ SIG2(B)2	Read Head Winding	A15J3-30, 11, Read Preamplifier PCB; A15J1-4, Read Preamplifier PCB; A11J3-P, Data Masterboard; Pin F, Quad Read Amplifier PCB (Location 3, Data Masterboard)
READ SIG3(A)/2	Read Head Winding	A15J3-20, 1, Read Preamplifier PCB; A15J1-9, Read Preamplifier PCB; A11J3-N, Data Masterboard; Pin E, Quad Read Amplifier PCB (Location 3, Data Masterboard)
READ SIG4(8)/2	Read Head Winding	A15J3-28, 9 Read Preamplifier PCB; A15J1-5, Read Preamplifier PCB; A11J3-M, Data Masterboard; Pin J, Quad Read Amplifier PCB (Location 4, Data Masterboard)
READ SIG5(4)/2	Read Head Winding	A15J3-22, 3, Read Preamplifier PCB; A15J1-8, Read Preamplifier PCB; A11J3-L, Data Masterboard; Pin H, Quad Read Amplifier PCB (Location 4, Data Masterboard)

Signal	From	To
READ SIG6(2)/2	Read Head Winding	A15J3-26, 7, Read Preamplifier PCB; A15J1-6, Read Preamplifier PCB; A11J3-K, Data Masterboard; Pin F, Quad Read Amplifier PCB (Location 4, Data Masterboard)
READ SIG7(1)/2	Read Head Winding	A15J3-24, 5, Read Preamplifier PCB; A15J1-7, Read Preamplifier PCB; A11J3-J, Data Masterboard, Pin E, Quad Read Amplifier PCB (Location 4, Data Masterboard)
-REEL MOTOR VOLTAGE SENSE	J1-3, 4111 Servo Power Amplifier	J1-11, 4105 Reel Servo Preamplifier PCB
RESET/	Pin K, Delay Timing PCB	Pin T, P Channel Read Amplifier/Clipping PCB; Pin T, Quad Read Amplifier PCB
REWIND LAMP	Pin L, Pushbutton Control PCB	1. Pin K, Interface Control PCB 2. A10J3-N, Control Masterboard; Pin N, Ramp Generator PCB
RNF1	Pin Z, Pushbutton Control PCB	Pin Z, Ramp Generator PCB
RNN/	Pin V, Interface Control PCB	1. A10J4-T, Control Masterboard; A11J4-T, Data Masterboard; Pin X, Delay Timing PCB; Pin H, P Channel/Clipping Control PCB 2. Pin 18, Pushbutton Control PCB (becomes RNN1)
RNN1	Pin Y, Pushbutton Control PCB	Pin Y, Ramp Generator PCB
RVS/	Pin T, Interface Control PCB	A10J4-S, Control Masterboard, A11J4-S Data Masterboard; Pin W, P Channel/Clipping Control PCB
RVS1	Pin X, Pushbutton Control PCB	Pin V, Ramp Generator PCB
RWC/	A10J1-H, Control Masterboard Interface Connector	Pin 10, Interface Control PCB
RWC1/	Pin L, Interface Control PCB	Pin M, Pushbutton Control PCB
RWDCOM	Pin R, Pushbutton Control PCB	A10J2-K, Control Masterboard; A22J1-6, Main Control Panel
RWDG	Pin 15, Interface Control PCB	A10J1-N, Control Masterboard Interface Connector
SERVO DISABLE	A21J-2, Main Control Panel	J1-4, Reel Servo Preamplifier PCB
SFC/	A10J1-C, Control Masterboard Interface Connector	Pin D, Control Terminator PCB; Pin 5, Interface Control PCB
SKEW LAMP	Pin N, Delay Timing PCB	A11J4-E, Data Masterboard; A10J4-E, Control Masterboard; Pin F, Pushbutton Control PCB; Test Connector J1-1; Pin F, Test Panel PCB
SLT/	A10J1-J, Control Masterboard Interface Connector	Pin 11, Interface Control PCB
SLT1	Pin F, Interface Control PCB	1. A10J4-W, Control Masterboard; A11J4-W, Data Masterboard, Pin V, Delay Timing PCB; Pin 9, 4 Channel Write Amplifier PCB 2. Pin 12, Sensor Amplifier Driver PCB
SLT2	Pin L, Delay Timing PCB	Pin S, P Channel/Clipping Control PCB; Pin S, Quad Read Amplifier PCB
SLT LAMP/	Pin V, Sensor Amplifier/Driver PCB	A10J3-E, Control Masterboard; Pin 10 Main Control Panel
SRC/	A10J1-E, Control Masterboard Interface Connector	Pin 8, Interface Control PCB

Signal	From	To
SWS/	A10J1-K, Control Masterboard Interface Connector	Pin 12, Interface Control PCB
TEST MODE	Test Mode Switch, Test Panel	A23J1-B, Test Panel; Pin 1, Pushbutton Control PCB; A10J4-H, Control Masterboard; A11J4-H, Data Masterboard; Pin U, Delay Timing PCB; Pin K, 4 Channel Write Amplifier PCB
TEST PULSES	Pin E, Delay Timing PCB	A11J4-J, Data Masterboard; A10J4-J, Control Masterboard; Pin 5, Pushbutton Control PCB; Pin J, Test Panel (Skew Test)
TNG/	Pin Z, Ramp Generator PCB	Pin 10, Interface Control PCB; Pin 21, Interface Control PCB, A10J1-V Control Masterboard
TS/	Pin 2, 5 Channel Write Amplifier PCB	Pin B, 4 Channel Write Amplifier PCB
WARS/	A11J1-P, Data Masterboard Interface Connector	Pin J, Data Terminator PCB; Pin J, 4 Channel Write Amplifier PCB
WARS1/	Pin M, 4 Ghannel Write Amplifier PCB	A11J4-N, Data Masterboard; A10J4-N, Control Masterboard; Pin K, Control Terminator PCB
WARS2/	Pin H, 4 Channel Write Amplifier PCB	Pin H, 5 Channel Write Amplifier PCB
WDP(C)/3	A11J1-R, Data Masterboard Interface Connector	Pin M, Data Terminator PCB; Pin 11, 4 Channel Write Amplifier PCB
WDO/	A11J1-S, Data Masterboard Interface Connector	Pin N, Data Terminator PCB; Pin 12, 4 Channel Write Amplifier PCB
WD1/	A11J1-T, Data Masterboard Interface Connector	Pin P, Data Terminator PCB; Pin 13, 4 Channel Write Amplifier PCB
WD2(B)/3	A11J1-U, Data Masterboard Interface Connector	Pin R, Data Terminator PCB; Pin 14, 4 Channel Write Amplifier PCB
WD3(A)/3	A11J1-V, Data Masterboard Interface Connector	Pin Z, Data Terminator PCB; Pin J, 5 Channel Write Amplifier PCB
WD4(8)3	A11J1-W, Data Masterboard Interface Connector	Pin Y, Data Terminator PCB; Pin K, 5 Channel Write Amplifier PCB
WD5(4)3	A11J1-X, Data Masterboard Interface Connector	Pin X, Data Terminator PCB; Pin L, 5 Channel Write Amplifier PCB
WD6(2)3	A11J1-Y, Data Masterboard Interface Connector	Pin W, Data Terminator PCB; Pin M, 5 Channel Write Amplifier PCB
WD7(1)3	A11J1-Z, Data Masterboard Interface Connector	Pin V, Data Terminator PCB; Pin N, 5 Channel Write Amplifier PCB
WDS	A11J1-N, Data Masterboard Interface Connector	Pin H, Data Terminator PCB, Pin 7, 4 Channel Write Amplifier PCB
WDS1	Pin E, 4 Channel Write Amplifier PCB	Pin E, 5 Channel Write Amplifier PCB
WEN/	Pin P, Interface Control PCB	A10J1-S, Control Masterboard Interface Connector
WEN LAMP/	Pin H, Sensor Amplifier Driver PCB	A10J3-T, Control Masterboard; Pin 13, Main Control Panel
WRDY	Pin J, Pushbutton Control PCB	1. Pin S, Interface Control PCB 2. Pin 7, Sensor Amplifier Driver PCB 3. A10J4-R, Control Masterboard; A11J4-R, Data Masterboard; Pin T, Delay Timing PCB; Pin J, P Channel/Clipping PCB; Pin 10, 4 Channel Write Amplifier PCB
WRITE CHAN P(C)4	Pins Z, Y, 4 Channel Write Amplifier PCB	A11J2-K, L, Data Masterboard; P2-13, 14, Write Head Connector

Signal	From	To
WRITE CHAN0	Pins X, W, 4 Channel Write Amplifier PCB	A11J2-M, N, Data Masterboard; P2-15, 16 Write Head Connector
WRITE CHAN1	Pins V, U, 4 Channel Write Amplifier PCB	A11J2-P, R, Data Masterboard; P2-11, 12, Write Head Connector
WRITE CHAN2(B)4	Pins T, S, 4 Channel Write Amplifier PCB	A11J2-S, T, Data Masterboard; P2-9, 10, Write Head Connector
WRITE CHAN3(A)4	Pins Z, Y, 5 Channel Write Amplifier PCB	A11J2-C, D, Data Masterboard; P2-7, 8, Write Head Connector
WRITE CHAN4(8)4	Pins X, W, 5 Channel Write Amplifier PCB	A11J2-E, F, Data Masterboard; P2-5, 6, Write Head Connector
WRITE CHAN5(4)4	Pins V, U, 5 Channel Write Amplifier PCB	A11J2-H, J, Data Masterboard; P2-17, 18, Write Head Connector
WRITE CHAN6(2)4	Pins T, S, 5 Channel Write Amplifier PCB	A11J2-U, V, Data Masterboard; P2-3, 4, Write Head Connector
WRITE CHAN7(1)4	Pins R, P, 5 Channel Write Amplifier PCB	A11J2-W, X, Data Masterboard; P2-1, 2, Write Head Connector
WRITE HEAD DRIVE	Pin 22, Sensor Amplifier Driver PCB	A10J4-X, Control Masterboard; A11J4-X, Data Masterboard; A11J2-Y, Data Masterboard; P2, Write Head Connector
WRT LAMP	Pin N, Sensor Amplifier Driver PCB	A10J3-M, Control Masterboard; Pin 12, Main Control Panel
WSEL	Pin H, Interface Control PCB	Pin 7, Pushbutton Control PCB

401-4147-001E4



REPRESENTS RESISTOR TERMINATOR NETWORK IN A 14 PIN DIP PACKAGE. PIN 7, GRD; PIN 14, +5V KENNEDY PART NO 149-0043-002. BECKMAN INST. PART NO 899-5R-220/330 OR EQUIV.

NOTES:
1. -001 IS A PLUG BOARD (ALL COMPONENTS OMITTED)
   -002 IS A "LAST TRANSPORT" MULTIPLE TRANSPORT ADAPTER. THE CABLES ATTACHED TO TB1, 2 & 3 ARE OMITTED. THIS VERSION MAY ALSO BE USED FOR SINGLE TRANSPORT SYSTEMS;
   -003 IS THE MULTIBLE TRANSPORT ADAPTER. A 5FT. CABLE IS ATTACHED TO THE ADAPTER. AT TB1, TB2 & TB3 TO GO TO THE NEXT TRANSPORT SIGNAL TERMINATOR BOARDS ARE IN THE TRANSPORT AND SHOULD BE REMOVED FROM ALL EXCEPT THE "LAST TRANSPORT". WHEN THE MTA IS USED AN OPTIONAL PUSH BUTTON ADDRESS ASSEMBLY MUST BE INSTALLED IN THE TRANSPORT.
   PROVISION IS MADE FOR TERMINATING SIGNALS FROM THE TRANSPORT, ALTHOUGH THESE SIGNALS SHOULD PROPERLY BE TERMINATED IN THE FORMATTER. IF THE FORMATTER DOES NOT HAVE PROPER TERMINATIONS, TERMINATING NETWORKS (KENNEDY PART NO. 149-0043-002, 2 REQ,D PER SYSTEM) MAY BE INSTALLED IN IC1 &IC6.

55X SERIES, STRAP ST4 AS SHOWN
-005 SAME AS -003 BUT 15' OF CABLE

2 RTH1 AND RTH2 SIGNALS ARE NOT REQUIRED WHEN USING A KENNEDY 9000 SERIES TRANSPORT. AUTOMATIC THRESHOLD CHANGES ARE MADE ON READ RETRIES BETWEEN THREE THRESHOLD LEVELS.

3 S1-3 OPEN, ALL OTHER CLOSED (SEE NOTE 1)

4 +5V FROM TRANSPORT REQUIRES ST1
+5V FROM FORMATTER REQUIRES ST2

5 QANTEL SPECIAL

TABLE

	ST1	ST2	ST3	ST4	ST5	ST6	ST7	ST8	ST9	ST10	
-001	4	4	USED	OMIT	OMIT	OMIT	USED	USED	OMIT	USED	SEE NOTES
-002			OMIT	OMIT	USED	USED	OMIT	OMIT	USED	USED	
-003			OMIT	OMIT	USED	USED	OMIT	OMIT	USED	USED	
-004			USED	OMIT	OMIT	OMIT	USED	USED	OMIT	USED	5
-005			OMIT	OMIT	USED	USED	OMIT	OMIT	USED	USED	6
-551			USED	USED	OMIT	OMIT	USED	USED	OMIT	USED	7
-006			USED	OMIT	OMIT	OMIT	USED	USED	OMIT	OMIT	SPECIAL
-007	4	4	USED	OMIT	OMIT	OMIT	USED	USED	OMIT	OMIT	
-009	4	4	USED	OMIT	OMIT	OMIT	USED	USED	USED	USED	9
-010	4	4	OMIT	OMIT	USED	USED	OMIT	OMIT	USED	OMIT	10
-011	4	4	USED	OMIT	OMIT	OMIT	USED	USED	OMIT	USED	11

6 15' CABLE TYPE-003

7 ITT (DOM) SPECIAL

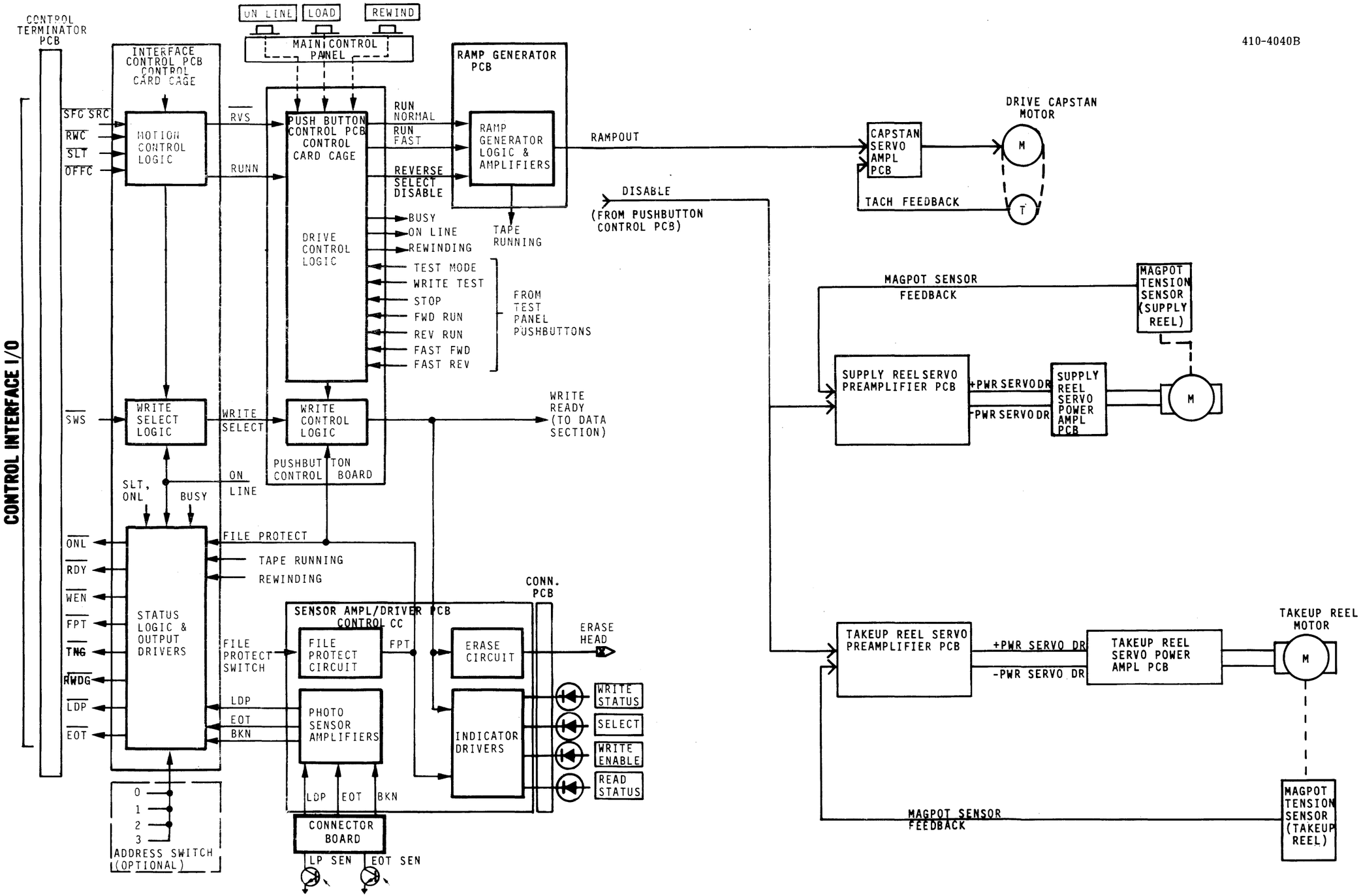
9 WESTERN PERIPHERALS CONTROLLER

10 ON LINE LOCK IS STRAPPED FROM J1-A TO P1-A

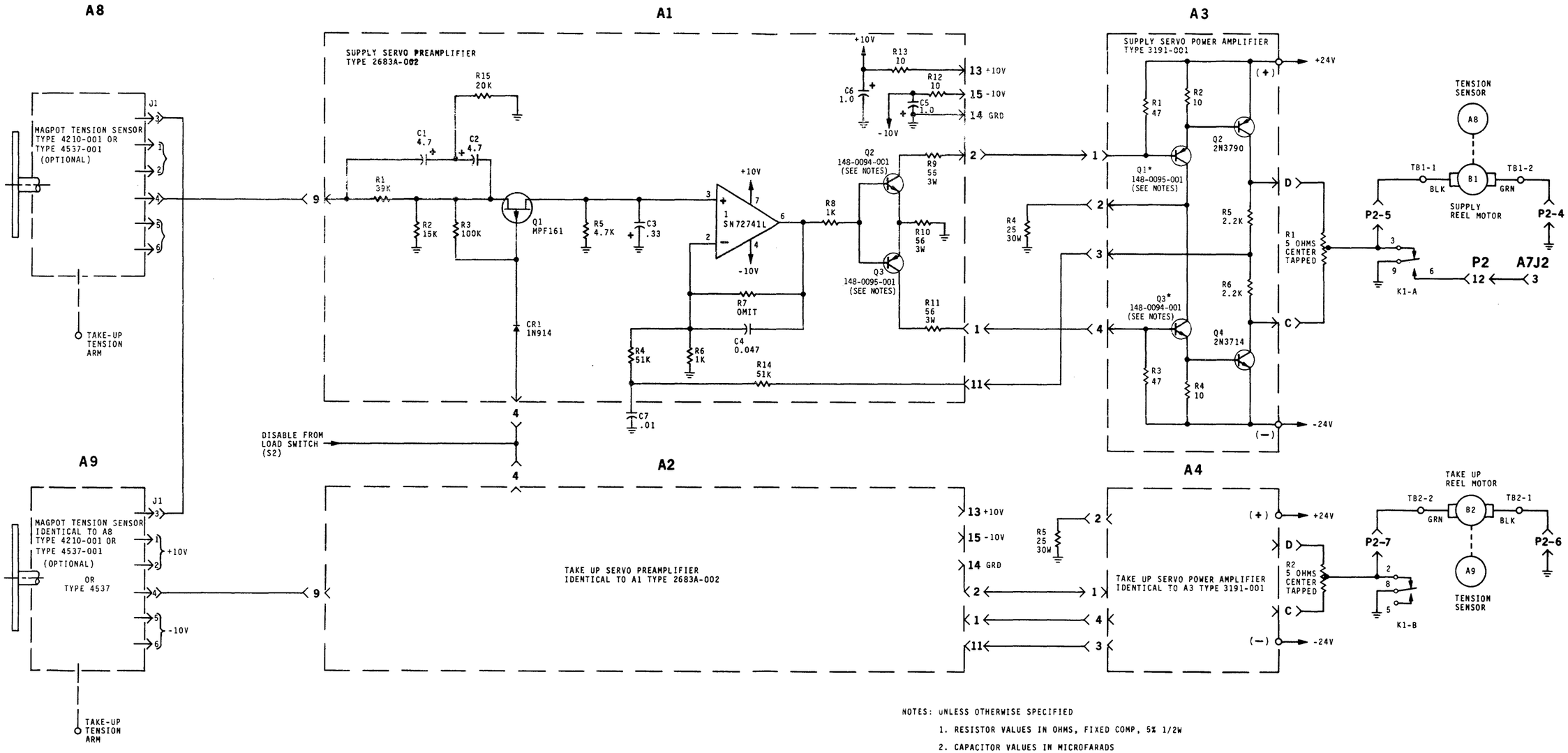
11 SPECIAL

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Multiple Transport Adapter, Type 4147
Optional Connector Configuration
For Industry Standard



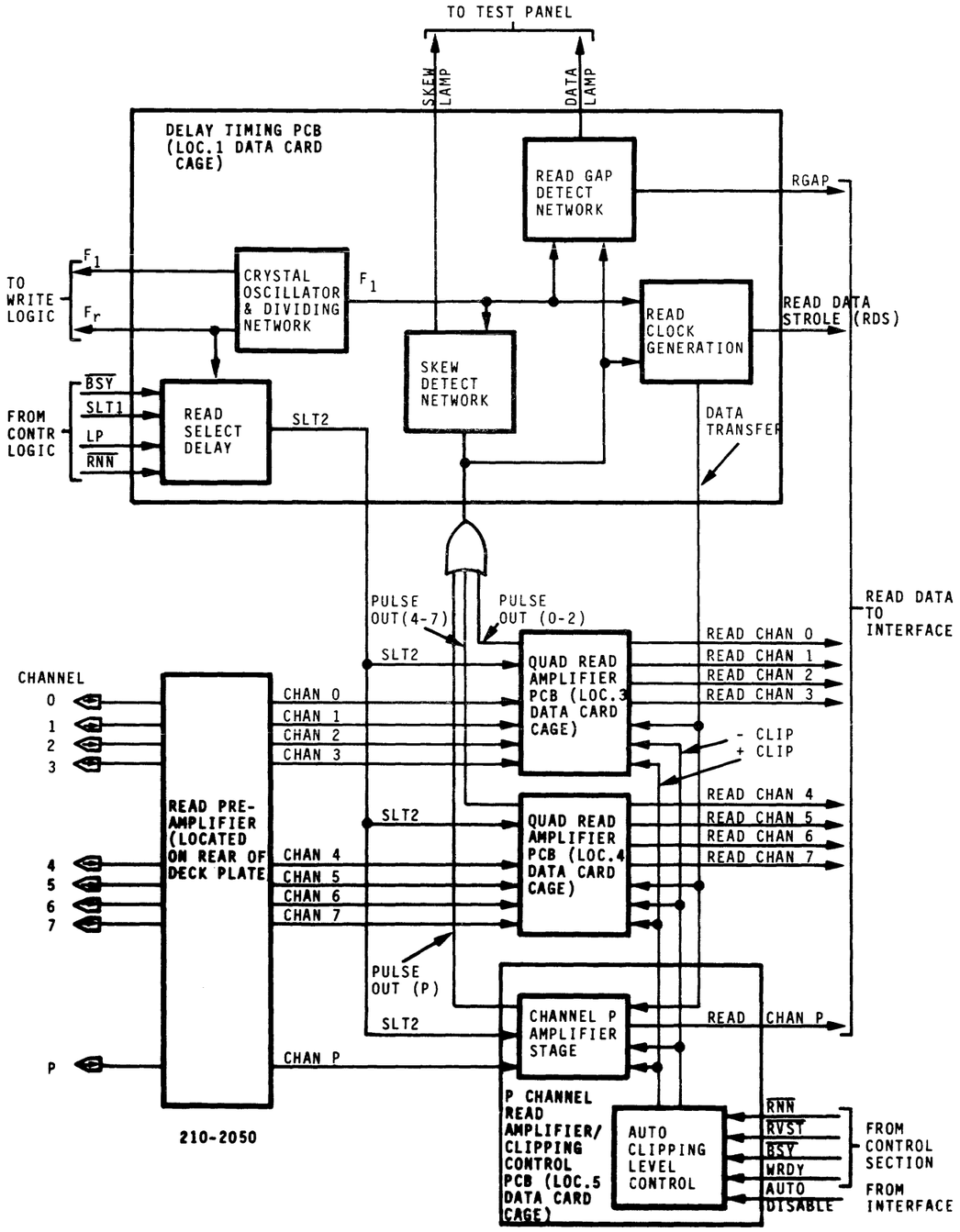
Control Section



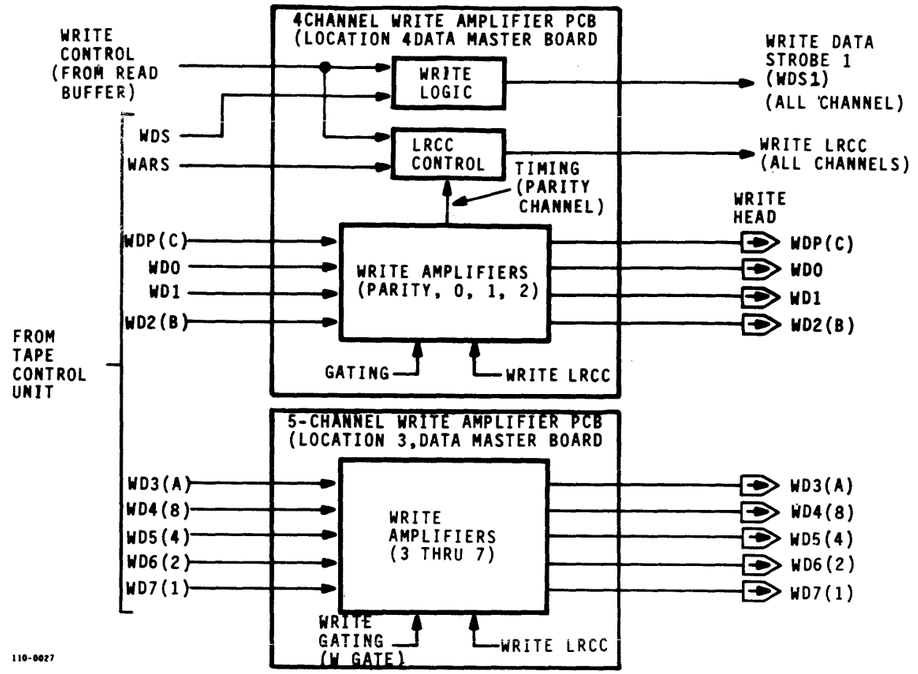
NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES IN OHMS, FIXED COMP, 5% 1/2W
2. CAPACITOR VALUES IN MICROFARADS
3. (*) DENOTES SELECTED VALUE OR TYPE TYPICALLY USED
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATIONS, PREFIX WITH ASSEMBLY DESIGNATION
5. EQUIVALENT TRANSISTORS
   148-0094-001 EQUALS MJE4922, MJE2523, SJE5052K, TIP31A.
   148-0095-001 EQUALS MJE2491, SJE5053K, TIP32A.

Reel Servo System, Schematic Diagram



Read Section



Write Section

Data Section

DELAY TIMING CARD TYPE 3845

401-9000-002 F

TO CONTROL M. BOARD

TEST PULSES

PEAK PULSES FROM PIN R

TEST MODE

WRDY

SKEW LAMP

DATA LAMP

BSY

SLT1

LP

RNN

SEE TABLE

(TO IC6-8)

(TO IC5-11)

(TO IC3-10)

(TO IC17-4)

(TO IC14-13)

(TO PIN N)

(TO PIN V)

(NOT USED)

TO IC3-5

IC11-6

IC15-5

SKEW LAMP

DATA LAMP

READ DATA STROBE

DATA TRANSFER

GAP DETECT

PEAK PULSE INPUT

RESET

SLT 1 (PIN V)

SLT2

DASH NO.	-001B	-002B	-004B	-005B	SWITCH POSITION 1 2 3 4 5 6 7	-011B
SPEED IPS	75.00		30.00		● ●	
	37.50	45.00	15.00	18.75	● ● ●	
	25.00		10.00		● ● ●	24.00
	12.50		5.00		● ● ●	
Y1	3.84MHz	4.608MHz	1.336MHz	1.92MHz		3.84MHz
C9	.047	.047	.047	.047		220PF

UNLESS OTHERWISE SPECIFIED:
- RESISTOR VALUES ARE IN OHMS ±5%
- CAPACITOR VALUES ARE IN PICOFARADS ±5%
- NPN TRANSISTORS ARE 2N2714
- PNP TRANSISTORS ARE MPS6517
- DIODES ARE 1N914
- IC ARE TTL, 7400 SERIES
-- NUMBER IN LOGIC SYMBOL IS REFERENCE DESIGNATOR, UNDERLINED NUMBER IS IC TYPE. (IF 7400 SERIES, 74 IS OMITTED)
-- IC PIN 7 IS CONNECTED TO GROUND
-- IC PIN 14 IS CONNECTED TO +5V
-- UNUSED INPUTS OF IC MAY BE TIED TOGETHER OR TO +5V THROUGH RESISTOR (+V)
- (*) DENOTES FACTORY SELECTED VALUE. TYPICAL VALUE IS SHOWN
- FILTER CAPACITORS ARE NOT SHOW' BUT ARE IDENTIFIED BY CF ON PC BOARD

ANALOG SIGNALS FROM PREAMP

A11J3 PREAMP CONN

A11J1 DATA INTERFACE CONN

(POSITION 2)

P CHAN READ AMP/CLIP CONTROL

SEE SCHEMATIC FOR CLIPPING CONTROL LOGIC

TOP (POSITION) TOP

TAPE CHANNEL LOCATIONS ON QUAD READ AMPLIFIERS

QUAD READ AMP

4179

4178

4178

POS CLIP LEVEL

NEG CLIP LEVEL

CLIPPING LEVEL DEFEAT

RDS

GAP DET

READ DATA OUTPUTS

9 Track Read Control Logic, Schematic Diagram

DELAY TIMING P.C. BOARD TYPE 4118 (POSITION NO.1)

401-9000-005J

AIU4 TO CONTROL MASTER BOARD

TEST PULSES J

TEST MODE H

WRDY R

SKEW LAMP E

DATA LAMP F

SLT 1 W

BUSY P

LP V

RNN T

Y1 SEE TABLE

R1 470

C1 OMIT

R2 470

R3 1K

C2 2200

R12 1K

(FROM IC5-8) f_{IN}

PEAK PULSES FROM PIN R

f_{R2} (FROM IC1-11)

C3 SEE TABLE

(FROM IC13-6)

(FROM IC16-5)

CR1 1N914

R11 SEE TABLE

C6 SEE TABLE

R15 SEE TABLE

R14 SEE TABLE

C4 4700

R5 470

R6 680

R7 1K

R8 2.2K

R4 1K

R13 1K

R14 4.7K

R9 2.2K

R10 1K

S1 S2 S3 S4 S5 S6 S7

f_{R2} f_{IN}

SKEW LAMP

DATA LAMP

f_1 f_{IN} HDI HDS f_R (NOT USED)

READ DATA STROBE RDS

DATA TRANSFER RNN J4-T

WRDY J4-R

RVS J4-X

BSY J4-P

PEAK PULSE INPUT

GAP DETECT

RESET

SLT 2

ANALOG SIGNALS FROM PREAMPLIFIER

PREAMP CONNECTOR AMJ3

C CHANNEL READ AMP /CLIPPING CONTROL

QUAD READ AMP

POSITION 2

POSITION 3

POSITION 4

TAPE CHANNEL LOCATIONS ON QUAD READ AMPLIFIERS

POSITIVE CLIPPING LEVEL

NEGATIVE CLIPPING LEVEL

DATA INTERFACE CONNECTOR AMH

READ DATA OUTPUTS

CLIPPING LEVEL DEFEAT

READ DATA STROBE

GAP DETECT

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

● INDICATES CLOSED POSITION OF SWITCH * DASH -103 TO USE THE SAME SWITCHING ARRANGEMENT AS -003

DENSITY	200/556														556/800															
DASH NO.	-001D			-002D				-003D				-001D				-002D				*-003D				-004F						
Y1	3.840 MHZ			2.304 MHZ				1.920 MHZ				3.840 MHZ				2.304 MHZ				1.920 MHZ				3.840 MHZ						
SWITCH POSITION	1	2	3	4	5	6	7	1	2	3	4	5	6	7	1	2	3	4	5	6	7	1	2	3	4	5	6	7	1	2	3	4	5	6	7
SPEED (IPS) 12.50																																			
15.00																																			
18.75																																			
25.00																																			
37.50																																			
45.00																																			
75.00																																			

C3	.047	220PF
R11	2.2K	680
R14	OMIT	1.2K
R15	OMIT	1K
C6	OMIT	1000

7 Track Read Control Logic, Schematic Diagram

TYPE 3194/3645 RAMP GENERATOR

CIRCUIT DESCRIPTION

The ramp generator produces the proper analog signal inputs to the capstan servo system to control the direction and velocity of tape motion. The outputs are voltages that rise and fall linearly at controlled rates to highly stable levels. These analog signals are controlled by digital logic outputs from the control section. Waveforms produced are shown with the schematic.

Two similar ramp generator circuits are provided: one for normal speed operation and one for high speed operation. IC4 is an operational amplifier in the RUN NORMAL SPEED circuit. The amplifier output is normally saturated in the negative direction. When its positive input at pin 5 is high, the output saturates at +10 volts. This occurs when the RUN NORMAL input sets flip-flop IC7. IC4 feeds FETs Q1, Q2 which are connected in a constant-current circuit. The magnitude of current flow in the circuit is controlled by R3 and R4. R3 controls current in the positive-going direction, or start ramp, while R4 controls the negative-going stop ramp.

Since C1 is charged by a constant current, its voltage rises linearly until clamped by CR1 to a value one diode drop below +5 volts. Q3 is an emitter follower whose output rises to a value of +5 volts, since the emitter can rise one diode drop higher than the base. When the input from IC7 to IC4 drops, the voltage fed to Q1, Q2 goes to -10 volts and C1 is discharged linearly until clamped by the base-collector diode of Q3. Since Q3 base goes one diode drop negative, and the emitter is at zero, a positive-going ramp has been generated.

The ramp voltage output from Q3 is fed to the FET switches Q4 and Q5. If forward direction has been selected, Q4 is on and Q5 is off. The ramp is then amplified by unity gain operational amplifier IC3, without inversion, and appears as a positive-going ramp at test point A. If reverse is selected, Q5 is on and Q4 is off. The ramp is then fed to the inverting input of IC3 and appears as a negative-going ramp at test point A. Forward/reverse selection is controlled by flip-flop IC6 and Q9, Q10.

Ramp amplitude and, therefore, tape speed is controlled by normal speed control R14 and output summing resistor R15. The fast forward and reverse ramps are produced by a similar circuit involving amplifiers IC1 and IC2. However, since rewind speed and ramp time need not be precisely controlled, resistors are used instead of FETs to charge and discharge C4 and produce an approximate 0.5 sec rise/fall time. CR9 and CR10 isolate the ramp output from any small offsets that may be present in IC2. Rewind speed is controlled by summing resistor R16. Operational amplifier IC5 at zero ramp output has a slight bias produced by R37 and R38, keeping its output negative. When the ramp rises above the bias, IC5 switches to positive output, indicating that the tape is running. This output is used to gate off the input circuits through IC10 and IC9. Flip-flops IC7 and IC8 may be reset by run normal or run fast inputs going false, but cannot be set again until the tape comes to a stop. This prevents damage from illegal commands and reduces timing requirements.

Type 3645 Ramp Generator includes an additional flip-flop, IC11-8, whose function is to enable consecutive RUN NORMAL commands to be received without requiring the tape to ramp down to a stop following each normal speed operation. Following a RUN FAST command, however, flip-flop IC11 is set by IC8, inhibiting any RUN NORMAL commands until the tape comes to a stop, at which point IC9-6 clears IC11-9, and the 0 output at IC11-8 enables IC7-2.

ADJUSTMENT PROCEDURE

Start/stop time adjustment:

a. Arrange input signals to the tape transport to start and stop machine. Rate must be such as to allow full ramp time.

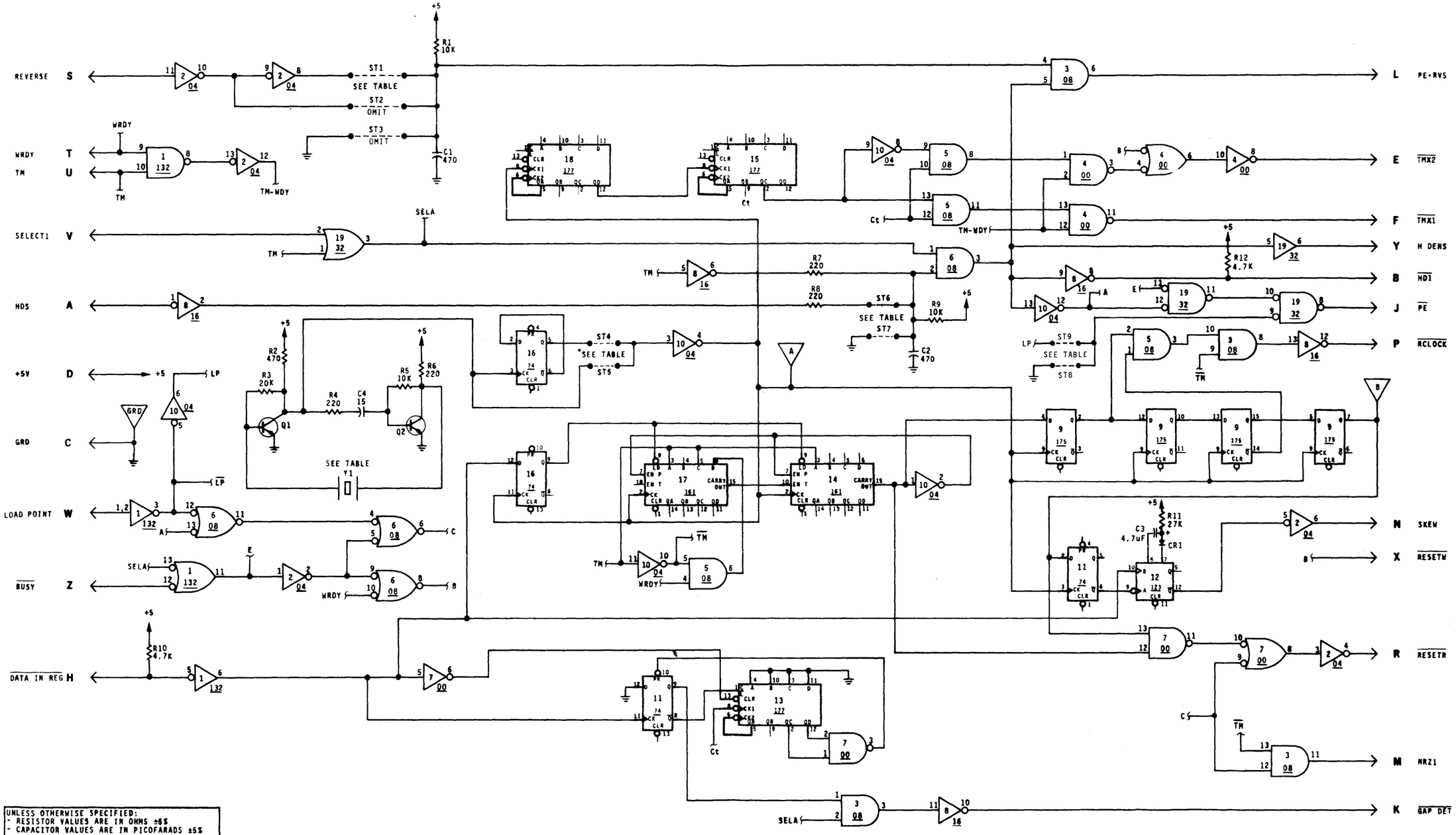
b. Adjust start ramp (R3) for required time, observing with oscilloscope at test point A.

c. Adjust stop ramp (R4) for required time. Time is measured from maximum volts to zero volts.

Speed adjustment:

a. Using a master skew tape, drive the transport in a forward direction at normal speed.

b. Observe data rate at read amplifiers and adjust R14 for correct timing.



UNLESS OTHERWISE SPECIFIED:
- RESISTOR VALUES ARE IN OHMS ±5%
- CAPACITOR VALUES ARE IN PICOFARADS ±5%
- NPN TRANSISTORS ARE 2N2714
- PNP TRANSISTORS ARE MPS6517
- DIODES ARE 1N914
- IC ARE TTL, 7400 SERIES
-- NUMBER IN LOGIC SYMBOL IS REFERENCE DESIGNATOR, UNDERLINED NUMBER IS IC TYPE. (IF 7400 SERIES, 74 IS OMITTED)
-- IC PIN 7 IS CONNECTED TO GROUND
-- IC PIN 14 IS CONNECTED TO +5V
-- UNUSED INPUTS OF IC MAY BE TIED TOGETHER OR TO +5V THROUGH RESISTOR (+V)
- (*) DENOTES FACTORY SELECTED VALUE. TYPICAL VALUE IS SHOWN
- FILTER CAPACITORS ARE NOT SHOWN BUT ARE IDENTIFIED BY CF ON PC BOARD

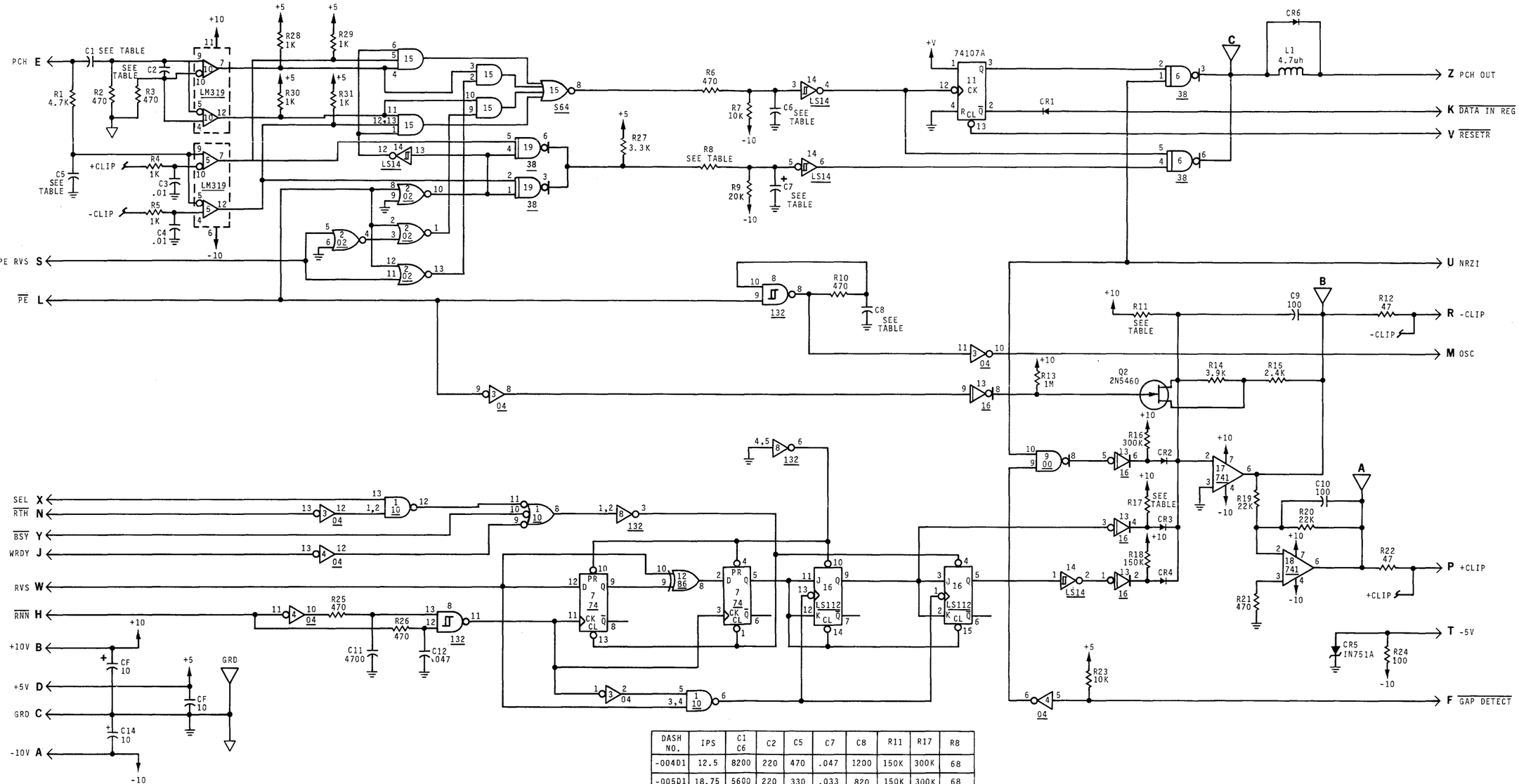
NOTE: DASH NUMBERS 10X ARE THE SAME AS 00X WITH ST6 OMITTED AND ST7 IN. 20X ARE THE SAME AS 00X WITH ST6 AND ST7 OMITTED.

*

DASH NO.	-004F	-005F	-001H	-002F	-003F	-006F	-013C		
IPS	12.5	18.75	25	37.5	45	75	45		
Y1	1.28	1.92	1.28	1.92	2.306	3.840	2.306		
ST4	STRAP	STRAP	OMIT	OMIT	OMIT	OMIT	OMIT		
ST5	OMIT	OMIT	STRAP	STRAP	STRAP	STRAP	STRAP		
ST1	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	STRAP		
ST6	STRAP	STRAP	STRAP	STRAP	STRAP	STRAP	STRAP		
ST7	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT		
ST8	STRAP	STRAP	STRAP	STRAP	STRAP	STRAP	STRAP		
ST9	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT		

NOTE. ST1 IS IN FOR READ REVERSE CAPABILITY WITH 9217 ONLY

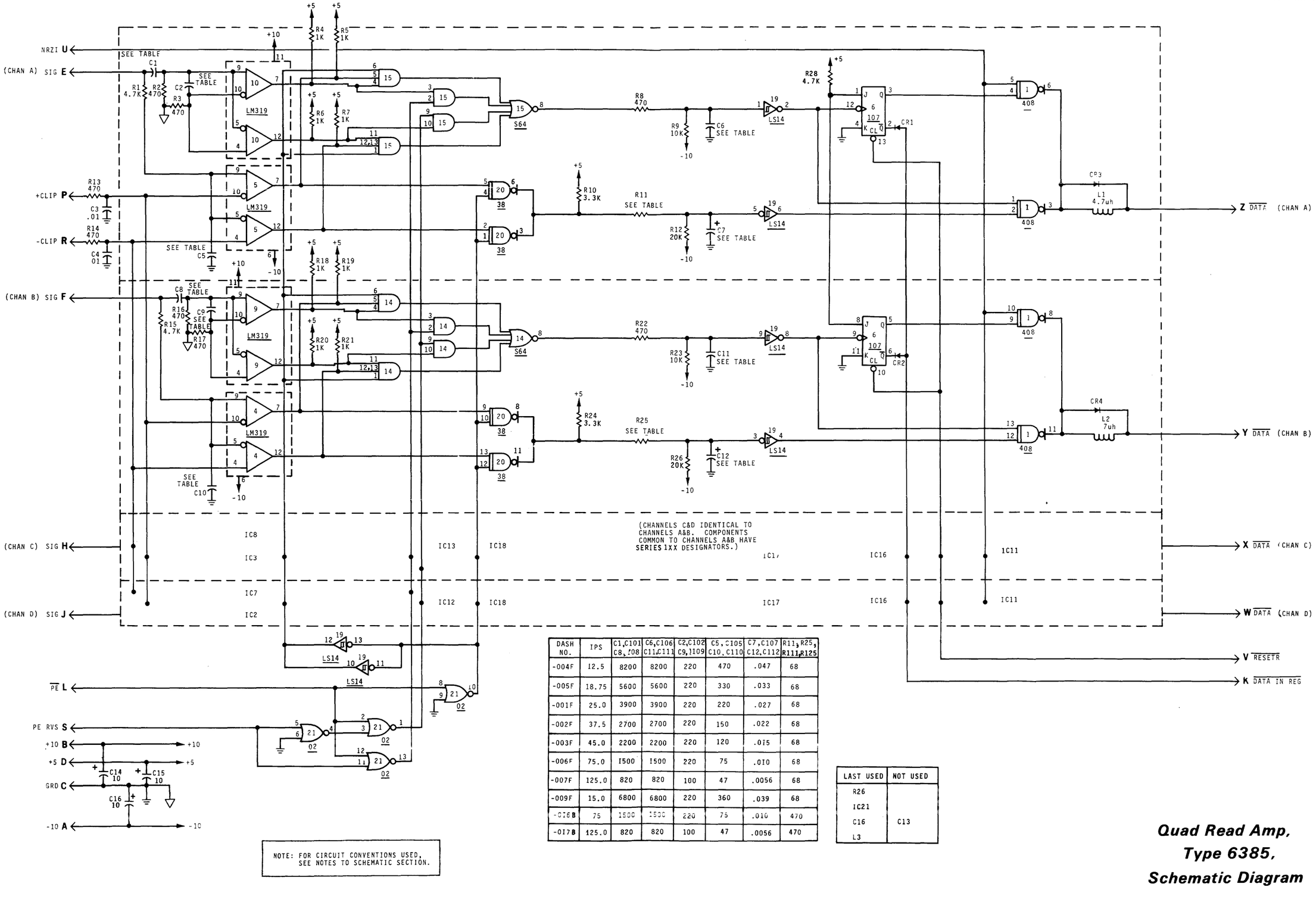
Dual Density Control, Type 4365A
Schematic Diagram



DASH NO.	IPS	C1 C6	C2	C5	C7	C8	R11	R17	R8
-004D1	12.5	8200	220	470	.047	1200	150K	300K	68
-005D1	18.75	5600	220	330	.033	820	150K	300K	68
-001D1	25.0	3900	220	220	.027	560	150K	300K	68
-002D1	37.5	2700	220	150	.022	390	150K	300K	68
-003D1	45.0	2200	220	120	.015	330	150K	300K	68
-006D1	75.0	1500	220	75	.010	180	100K	1M	68
-007D1	**125.0**	**820**	**100**	**47**	**.0056**	**100**	**100K**	**1M**	**68**
-009D1	15.0	6800	220	360	.039	1000	150K	300K	68
-016A	75	1500	220	75	.010	180	100K	1M	470
-017A	125.0	820	100	47	.0056	100	100K	1M	470

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Dual P Chan/Clipping, Type 6367, Schematic Diagram



DASH NO.	IPS	C1,C101 C8,108	C6,C106 C11,C111	C2,C102 C9,1109	C5,C105 C10,C110	C7,C107 C12,C112	R11,R25, R111,R125
-004F	12.5	8200	8200	220	470	.047	68
-005F	18.75	5600	5600	220	330	.033	68
-001F	25.0	3900	3900	220	220	.027	68
-002F	37.5	2700	2700	220	150	.022	68
-003F	45.0	2200	2200	220	120	.015	68
-006F	75.0	1500	1500	220	75	.010	68
-007F	125.0	820	820	100	47	.0056	68
-009F	15.0	6800	6800	220	360	.039	68
-016B	75	1500	1500	220	75	.010	470
-017B	125.0	820	820	100	47	.0056	470

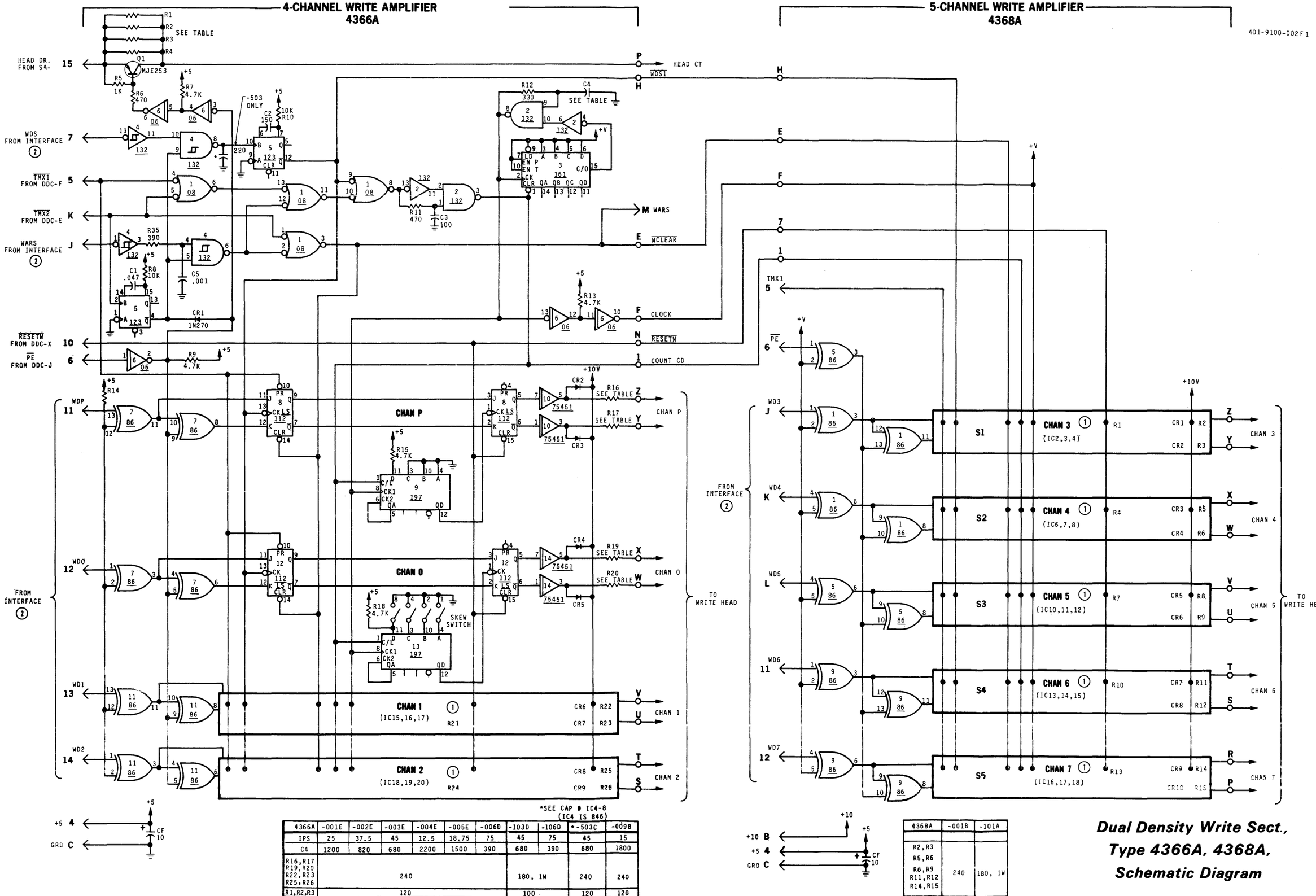
LAST USED	NOT USED
R26	
IC21	
C16	C13
L3	

Quad Read Amp, Type 6385, Schematic Diagram

4-CHANNEL WRITE AMPLIFIER 4366A

5-CHANNEL WRITE AMPLIFIER 4368A

401-9100-002F1



*SEE CAP @ IC4-8 (IC4 IS 846)

4366A	-001E	-002E	-003E	-004E	-005E	-006D	-103D	-106D	*-503C	-009B
IPS	25	37.5	45	12.5	18.75	75	45	75	45	15
C4	1200	820	680	2200	1500	390	680	390	680	1800
R16,R17 R19,R20 R22,R23 R25,R26	240						180, 1W		240	240
R1,R2,R3	120						100		120	120
R4	180						100		180	180

4368A	-001B	-101A
R2,R3 R5,R6 R8,R9 R11,R12 R14,R15	240	180, 1W

Dual Density Write Sect., Type 4366A, 4368A, Schematic Diagram

MODEL 9000 SYSTEM WIRING DIAGRAM

The system wiring diagram displays the entire transport's wiring, including the wiring from the control and data masterboards to the various mechanical and electrical components of the deck, the interconnections between the two masterboards, as well as the servo, motor and power supply interconnections.

The source of each wire is clearly identified by the number of the source, the connector number, and the connector pin number, all displayed at the wire's destination. Where relevant, the mnemonic designation of the signal is also given.

The system wiring diagram is followed by actual prints of the two masterboards, the control masterboard, and the data masterboard. These prints show the printed circuits which interconnect the individual modules.

POWER SUPPLY
E2
TO E1-A
1
A1P1-14
A5-J1
J2-3
2
J2-13
R4-B
3
J2-4
J2-12
J2-6
4
J2-8
K1-9
5
6
K1-3 R1CT SM
K1-2 R2CT TM
K1-9 E2-4 GRD
C3(+) +12 J3-5 +12
J2-14 +24
C1(+) +24 A5-A +24
A3 + +24
C2(-) -24 J2-15 -24
A5-B -24
A3 - -24
POWER SUPPLY (FOR INTERNAL WIRING SEE SCHEMATIC DIAGRAM)
A5
VOLTAGE REGULATOR
+24V A PSC1 +24
J3-1 +24
+10V J1 J2-1 +10
J3-3 +10
A1P1-13 +10
-24V B J3-2 -24
PSC2 -24
-10V J2 J2-2 -10
J3-4 -10
A1P1-15 -10
GRD J4 J3-6 GRD
E2-1 GRD
LF1
LINE FILTER
INPUT
LOAD
F1
TO T1 ON POWER SUPPLY
P1 J1
7 S4-3
4 S4-2
1 S4-1
2 S4
A5-J1
A5-J2
E2-2 GRD
E2-3 GRD
R1CT SM
E2-4 GRD
R2CT TM
GRD
E2-4
E2-3 LITE GRD
E2-2
PSC1 +24
PSC2 -24
A1P1-9
A2P1-9
A1P1-4
A1P1-5
J2
1 2 3 4 5 6 7 8 12 13 14 15 9 10 11
P2
P2A J2A
A8J1-1 +10
A8J1-6 -10
A22J1-14 GRD
TB1-1 SM
TB1-2 SM
TB2-2 TM
TB2-1 TM
A6J1-15 GRD
A7J2-3 GRD
A7J2-11 GRD
A7J2-12
A24-4+24
A6J1-10
A8J1-4 SUP POT
19J1-4 TU POT
A6J1-9 DISABLE
J3
1 2 3 4 5 6
P3
A5-A +24
A5-B -24
A5-J1 +10
A5-J2 -10
PSC3 +12
A5-J4 GRD
A10J3-U +24
A10J3-V +10
A10J3-7 10
A24J1-1 -12
A10J3-X GRD REG
A13 FILE PROTECT SOLENOID
C
NC
A
B
IN
RING
MISSING
GRN GRD
WHT FPT
BLK
BLK
J1
1 2 3 4
A7
CONNECTOR BOARD 5303
J1
J2
8 3 11 12 4 5 1 2 6 7 9 10
J3
1 2 3 4
J5
1 2
BLK
WHT
PU2 ERASE HEAD
A8J1-3
P2-12 GRD
P2-13
P2-14 +24
+24
+10
A22J1-1
A22J1-2 DISABLE
A10J3-D BKN SEN
A10J3-S ERASE HD
A10J3-H FPT
A10J3-C LP SEN
A10J3-L FP SOL
A10J3-B EOT
GRN EOT
RED LP
YEL
WHT
A7J3-2 RED
A7J3-1 GRN
A7J3-3 YEL
A7J3-4 WHT
LP SEN
EDT SEN
J1
1 2 4 5 6 3
P2-1 +10
A9J1-2 +10
P2-9 OUTPUT
A9J1-5 -10
P2-2 -10
A7J2-8 LITE
A9J1-3
A8
SUPPLY TENSION SENSOR MAGPOT
A9J1-6 -10
P2-15 -24
P2-8 CM PWR GRD
+24
A9J1-1
+10
P2-11
SERVO DISABLE
A10J3-P RAMP
A10J3-20 GRD
P2A-1 TACH SIG
6 10 15 12 8 9 1 4 3
J1
CAPSTAN SERVO AMPLIFIER 3264
A6
J2
1 2 3 4
GRN
BLK
WHT
BLK
B3
G1
TB1
P2-4 GRD
1 GRN
B1
SUPPLY REEL MOTOR
P2-5
2 BLK
TB2
P2-7
1 GRN
B2
TAKEUP REEL MOTOR MAGPOT
P2-6 GRD
2 BLK
A6J1-8 +10
A8J1-2 +10
A8J1-3 LITE
P2-10 OUTPUT
A8J1-5 -10
A6J1-6 -10
A9
J1
TAKEUP TENSION SENSOR
S4
AC POWER SWITCH
ON
OFF
3 2
4 1
J1-7
J1-2
J1-1
J1-4
A22
MAIN CONTROL PANEL
A10J3-A ON LINE NC
A10J3-J ON LINE NO
A7J2-5 DISABLE
A7J2-4 +10
A10J3-V ON LINE LITE
A10J3-F LOAD LITE
A10J3-N REWIND LITE
A10J3-K REWIND SW
A10J3-W +5
A10J3-E SELECT LITE
A10J3-T WRITE EN LITE
A10J3-R READ LITE
A10J3-M WRITE LITE
P2-3 GRD
J1
7 4 2 1 11 3 14 9 6 5 10 13 15 12 14
1K
220
ON LINE
LOAD
REWIND
SELECT
WRITE ENABLE
READ
WRITE
MAIN CONTROL PANEL 3855

System Wiring Diagram

A15

READ PREAMPLIFIER PCB

J1

A11J3-S CHAN 0 — 1
A11J3-R CHAN 1 — 2
A11J3-T CHAN P — 3
A11J3-P CHAN 2 — 4
A11J3-M CHAN 4 — 5
A11J3-K CHAN 6 — 6
A11J3-J CHAN 7 — 7
A11J3-L CHAN 5 — 8
A11J3-N CHAN 3 — 9
A11J3-C +10 — 13
A11J3-B -10 — 14
A11J3-A SIG GRD — 15

J3: 1 20 3 22 5 24 7 26 9 28 11 30 13 32 15 34 17 36

CHAN 3 SIG GRD
CHAN 3 R OUTPUT
CHAN 5 SIG GRD
CHAN 5 R OUTPUT
CHAN 7 SIG GRD
CHAN 7 R OUTPUT
CHAN 6 SIG GRD
CHAN 6 P OUTPUT
CHAN 4 SIG GRD
CHAN 4 R OUTPUT
CHAN 2 SIG GRD
CHAN 2 R OUTPUT
CHAN P SIG GRD
CHAN P R OUTPUT
CHAN 1 SIG GRD
CHAN 1 R OUTPUT
CHAN 0 SIG GRD
CHAN 0 R OUTPUT

P3: 1 20 3 22 5 24 7 6 9 28 11 30 13 32 15 34 17 36

READ HEAD

E1 GROUND STRAP (A, R)

A15J1-3 CHAN P
A15J1-1 CHAN 0
A15J1-2 CHAN 1
A15J1-4 CHAN 2
A15J1-9 CHAN 3
A15J1-5 CHAN 4
A15J1-8 CHAN 5
A15J1-6 CHAN 6
A15J1-7 CHAN 7
+10
-10
SIG GRD

A11: T S R P N M L K J C B A

J4 — J3

STD NRZI ONLY DAUGHTER BOARDS

LOCATION	TYPE	NAME
1	3845	TIMING DELA
2	4179	READ AMPL./CLIPPING
3	4178	QUAD READ AMPL.
4	4178	QUAD READ AMPL.
5	3860	DATA TERMINATOR
6	3848	4 CHANNEL WRITE AMP
7	3849	5 CHANNEL WRITE AMP

STD DUAL DENSITY DAUGHTER BOARDS

LOCATION	TYPE	NAME
1	4365	
2	6367	
3	6385	
4	6385	
5	3860	
6	4366	
7	4368	

1600BPI STD PE DAUGHTER BOARD

1	4209	5	3860
2	4188	6	4207
3	4139	7	4208
4	4139		

J1: 1 A B C D E F H J K L M N P R S T U V W X Y Z

CLD RDS RDP N00 R01 R02 R03 R04 R05 R06 R07 RGAP WDS WARS WDP WD0 WD1 WD2 WD3 WD4 WD5 WD6 WP7

TO DATA INTERFACE INPUT

A10J2-A -10
A10J2-B +10
A10J2-C GRD
A24J2-2 +5
A10J2-E SKEW LITE
A10J2-F DATA LITE
A10J2-H TEST MODE
A10J2-J TEST PULSES
A10J2-L HDS
A10J2-M HDI
A10J2-N WARS
A10J2-P BSY
A10J2-R WR RDY
A10J2-S RVS
A10J2-T RNN
A10J2-U TNG
A10J2-V LP
A10J2-W SLT1
A10J2-X HD DRIVE
A10J2-Y FWR

A16 P2 — J2

37 36 35 34 33 32 31 30 29 2 1 4 3 10 9 12 11 16 15 14 13 18 17 6 5 8 7

Z SIG GRD (SHIELD)
Y WRITE HD DRIVE
X CHAN 7
W CHAN 7
V CHAN 6
U CHAN 6
T CHAN 2
S CHAN 2
R CHAN 1
P CHAN 1
N CHAN 0
M CHAN 0
L CHAN P
K CHAN P
J CHAN 5
H CHAN 5
F CHAN 4
E CHAN 4
D CHAN 3
C CHAN 3

WRITE HEAD

A24

E1 C — GRD

J2: 1 — A10J2-D +5; 2 — A11J4-D +5

+5V REGULATOR

J1: 2 1 4 — P3-5 +12 — P2-14 +24

E1 D

E2 GRD (E)

CONTROL INTERFACE INPUT

Z Y X W V U R S P N M L K J H F E D C B

SLT4 SLT3 SLT2 SLT1 RNG EOT ROV WEN LOP FPT RWD UNL OFFC SWS SLT RWC HDI SRC HDS SFC OVW

A11J4-A -10
A11J4-B +10
A11J4-C SIG GRD
A24J2-2 +5V
A11J4-E SKEW LITE
A11J4-F DATA LITE
A11J4-H TEST MODE
A11J4-J TEST PULSES
A11J4-L HDS
A11J4-M HDI
A11J4-N WARS
A11J4-P BSY
A11J4-R WRDY
A11J4-S RVS
A11J4-T RNN
A11J4-U TNG
A11J4-V LP
A11J4-W SLT1
A11J4-X W HD DRIVE
A11J4-Y FWR

J2: A B C D E F H J K L M N P R S T U V W Z

J3: Z Y X W V U T S R P N M L K J H F E D C B

P3-4 -10
P3-3 +10
P3-6 SIG GRD
A22J1-6 +5
A22J1-11 ONL LITE
P3-1 +24
A22J1-13 W EN LITE
A7J2-2 ERASE HD
A22J1-15 READ LITE
A6J1-1 RAMP
A22J1-9 REWIND LITE
A22J1-12 WRITE LITE
A7J2-9 FPT SOL
A22J1-6 REWIND SW
A22J1-4 ONL SW
A7J2-6 FPT
A22J1-3 LOAD SW
A22J1-10 SLT LITE
A7J2-1 BKN SEN
A7J2-7 LP SEN
A7J2-10 EOT SW
A7J2-4 [illegible] SW

PUSHBUTTON CONTROL PLUG IN MODULE 3843

STOP SW GRD	10 L		F REV SW
+5	9 K		F FWD SW
TEST PT	8 J		STOP SW
DATA LITE	6 H		T MODE SW
SKEW LITE	5 F		W TEST SW
W TEST LITE	4 E		W TEST SW
T MODE LITE	3 D		STOP SW
LOP LITE	2 C		F FWD SW
EOT LITE	1 B		R REV SW
	A		R FWD SW

J4 ADDRESS SELECT: 1 2 3 4 (OPTION) — 0 1 2 3

STD DAUGHTER BOARDS

LOCATION	TYPE	NAME
2	3841	CONTROL TERMINATOR
3	3842	INTERFACE CONTROL
4	3843	PUSHBUTTON CONTROL
5	3645	RAMP GENERATOR
6	3844	SENSOR AMPL./DRIVER

A10

A23

TEST PANEL

J1: W X T B C U Y D V P A R E H F J M L S

P2-10 STOP SW GRD
P2-D STOP SW GRD
P2-J T MODE SW
P2-3 T MODE LITE
P2-4 W TEST LITE
P2-E W TEST SW
P2-F W TEST SW
P2-2 LOP LITE
P2-J STOP SW
P2-K FWD SW
P2-9 +5
P2-A R FWD SW
P2-1 EOT LITE
P2-6 DATA LITE
P2-5 SKEW LITE
P2-8 SKEW TEST
P2-C F FWD SW
P2-B R REV SW
P2-F REV SW

TEST MODE
TEST MODE
WRITE TEST
WRITE TEST
STOP
LOAD POINT
FORWARD RUN
EOT
REVERSE RUN
DATA
FAST FORWARD
SKEW
FAST REVERSE
SKEW TEST

A3

SUPPLY REEL POWER AMPLIFIER

+ PSC1 +24
A4+ +24
– PSC2 -24
A4- -24
C R1-B
D R1-A

J1: 4 1 3 2 — A4-A

A1 P1 — SUPPLY REEL SERVO PREAMP

5 9 4 13 14 15 1 2 11

J2A-1
A2P1-6
J2-9 SUP POT
J2-11 DISABLE
A2JP-4
A5-J1+10
A2P1-13
E2-1 GRD
A2P1-14
A5-J2-10
A2P1-15

A4

TAKEUP REEL POWER

+ A3+ +24
– A3- -24
C R2-B
D R2-A

J1: 2 4 1 3 — R2-A

A2 P1 — TAKEUP REEL SERVO PREAMP

6 4 9 13 14 15 1 2 11

A1P1-5
A1P1-4 DISABLE
J2-10 TU POT
A1P1-13 +10
A1P1-14 GRD
A1P1-15 -10

A3-D A4-D PSK1-3 J2-5 PSK1-2 J2-7 A3-C A4-[illegible]

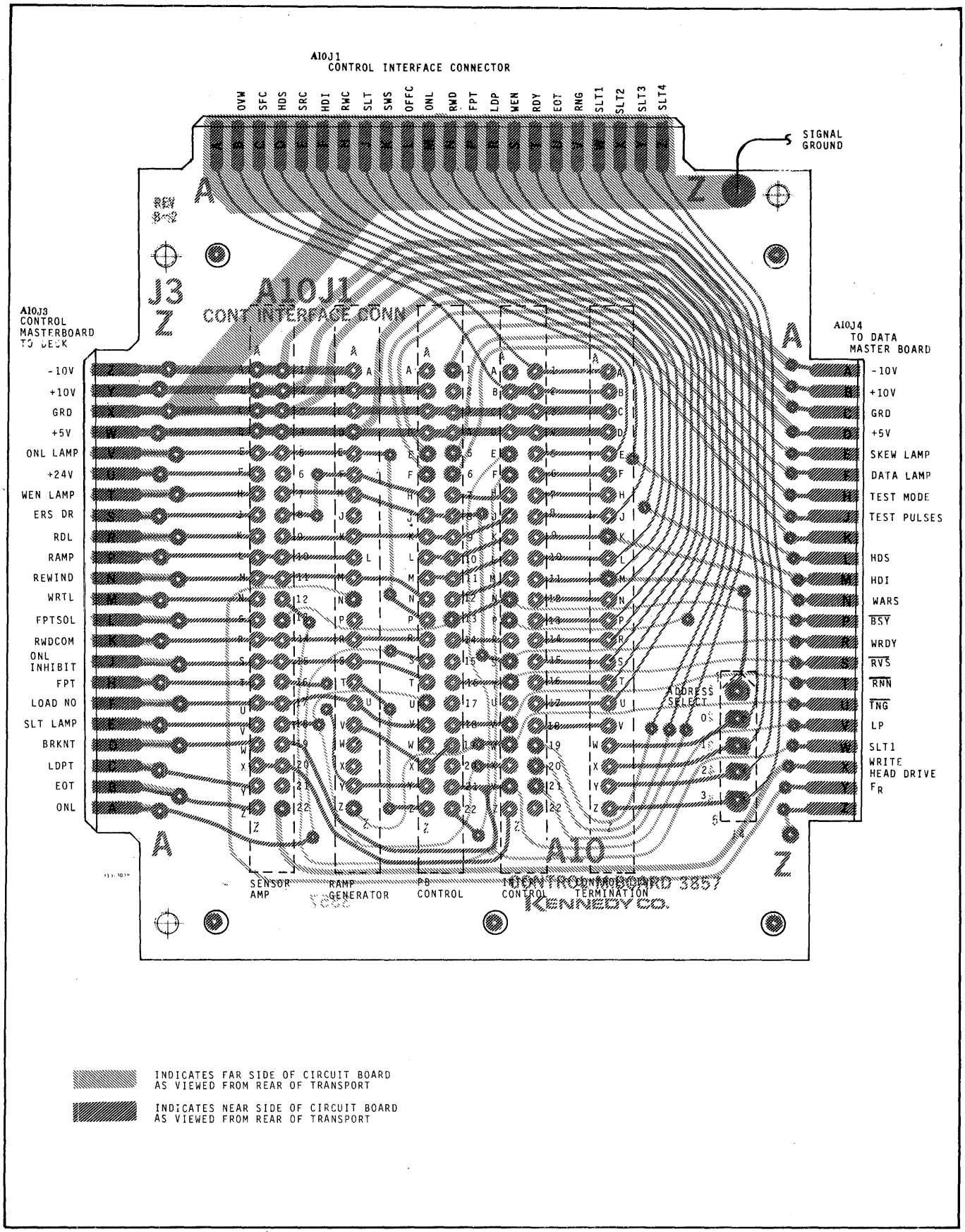
R2: A CT B / A CT B

R1: A CT B / A CT B

E2-3 A3J1-2 A4J1-2

R5: B B A

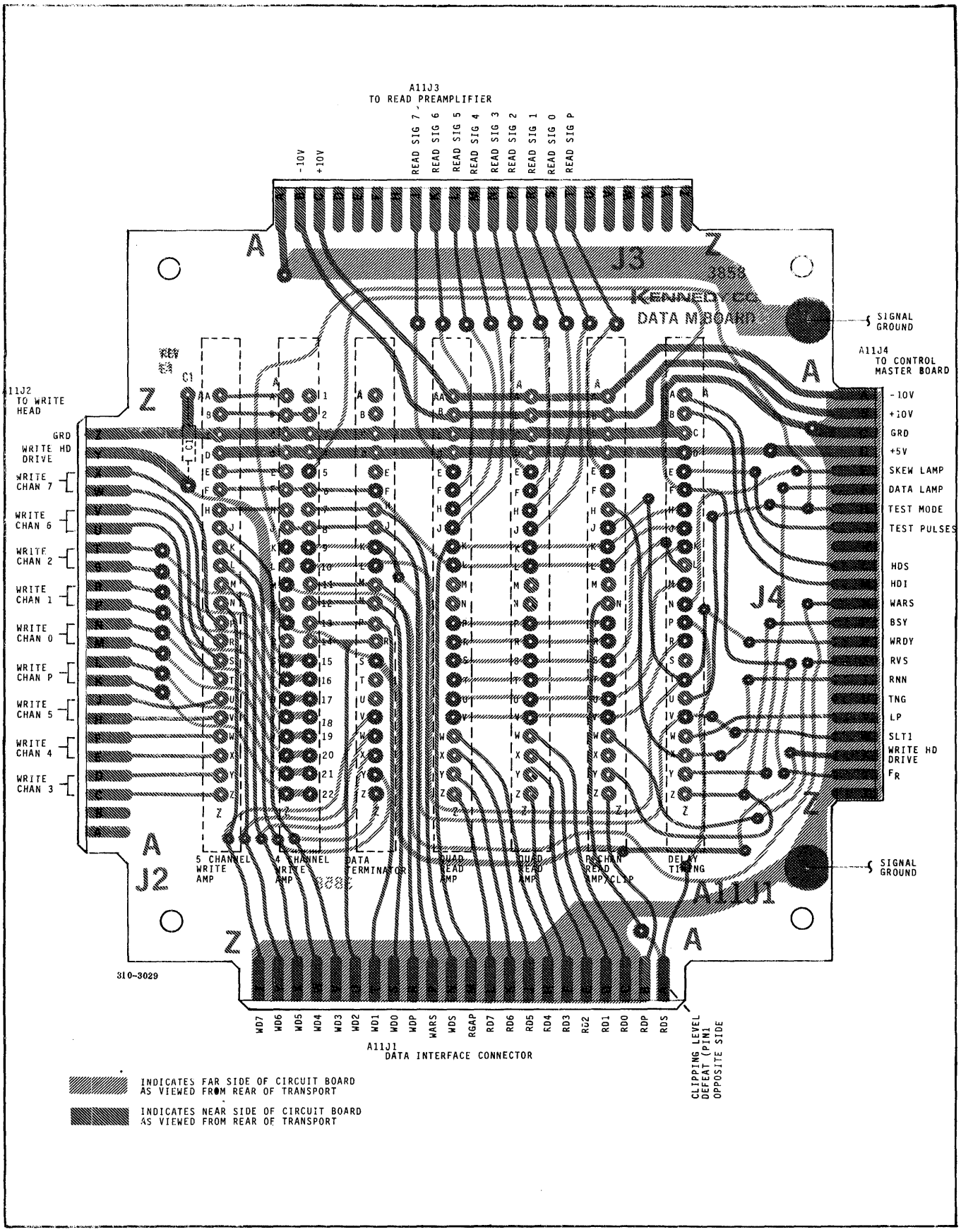
R4: B A



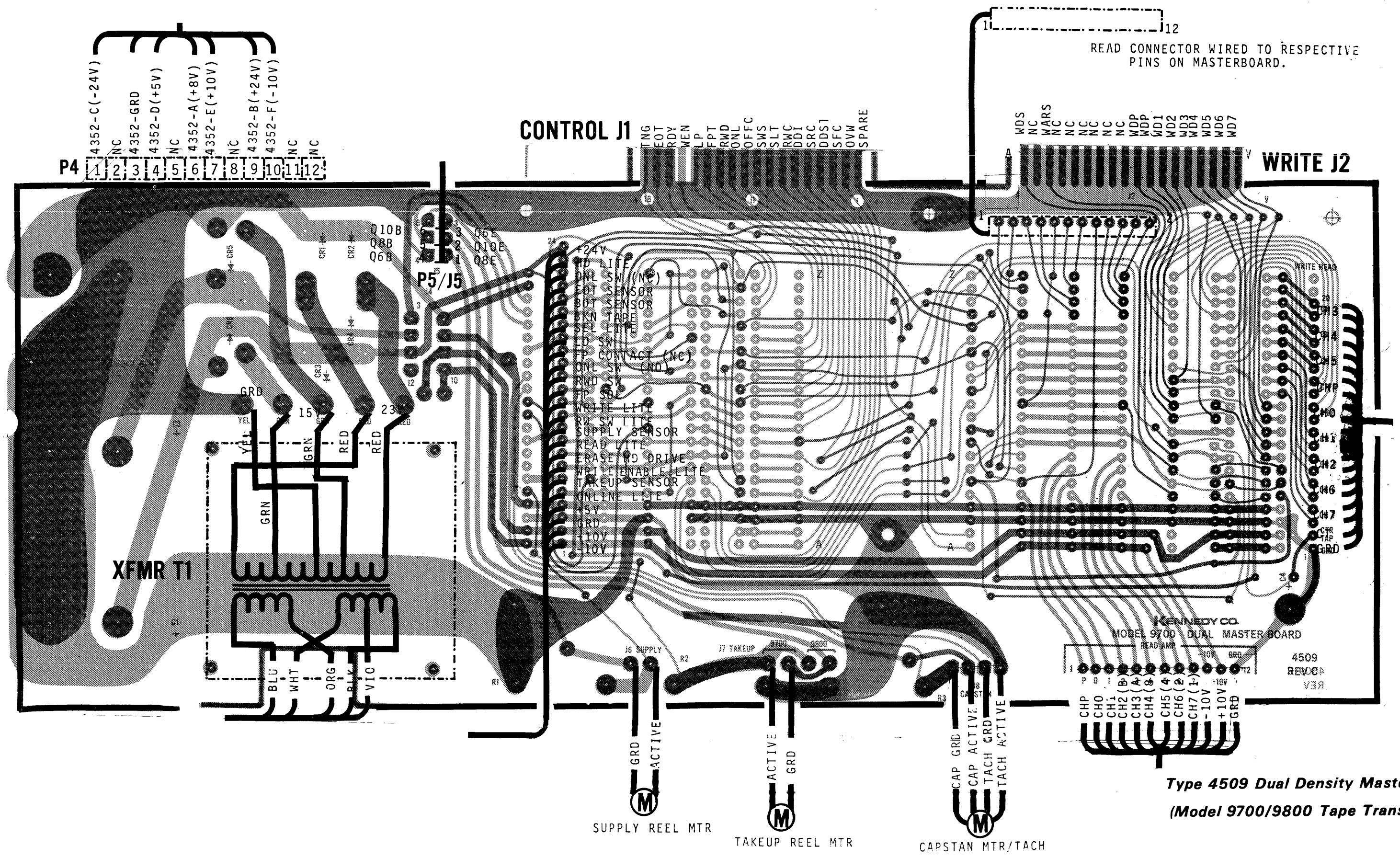
INDICATES FAR SIDE OF CIRCUIT BOARD AS VIEWED FROM REAR OF TRANSPORT

INDICATES NEAR SIDE OF CIRCUIT BOARD AS VIEWED FROM REAR OF TRANSPORT

Control Master Board Assembly



Type 3858 Data Master Board Assembly



Type 4509 Dual Density Master Board

(Model 9700/9800 Tape Transports)

MODEL 9000 SERIES

POWER SUPPLY CIRCUIT DESCRIPTION

The Model 9000 series power supply produces the unregulated and regulated voltages required to operate the motors and electronics. The unregulated voltages are +24 vdc and -24 vdc. Regulated voltages include +10 vdc, -10 vdc and +5 vdc. The Type 6414 PC Board outputs regulated +10 vdc and -10 vdc, while the Type 6810 PC Board outputs regulated +5 vdc.

TYPE 6414 REGULATOR (+10 vdc/-10 vdc)

Pass transistor Q1 is controlled by output from pin 10 of the uA723 regulator, IC1. Voltage output from the PC board is determined by resistors R6, R10 and adjustment pot R7 or R5 and R9 for nonadjustable versions. Resistors R4 and R8, together with sense resistors R2 and R3 and the regulator circuitry connected to IC1-2 and IC1-3, form a current limiting foldback circuit for protection against shorts on the +10 vdc line. To assure accurate voltage tracking, the regulated -10 vdc is referenced to the regulated +10 vdc through resistor R11, temperature compensating diodes CR2 and CR3 and resistor R12. Transistors Q2 and Q3 form an error amplifier that drives the node between CR2 and CR3 to virtually ground, thus assuring that the -10 vdc supply will track that of the +10 vdc. Similar foldback current limiting for the -10 vdc supply is performed by resistors R15 through R18 and transistor Q4.

TYPE 6810 REGULATOR (+5 vdc)

Pass transistor Q1 is controlled by pin 10 of regulator IC1. As in the case of the +10 vdc supply, shorting protection is accomplished by the foldback current limit circuit composed of bias resistors R10, R11, sense resistors R7, R8 and R9, and the regulator IC's internal circuitry connected to pins 2 and 3. Voltage output is controlled by optional potentiometer R3 and resistors R1 and R4, or R2 and R5 for nonadjustable versions. (R3 is the +5 vdc adjustment.)

POWER SUPPLY VOLTAGE ADJUSTMENTS
(Applies to 890-6414-001 and 890-6810-001 boards only)

Potentiometer R7 on Type 6414 Regulator PC Board is the +10 vdc voltage adjustment. Potentiometer R3 on the Type 6810 Regulator PC Board is the +5 vdc adjustment. Regulated -10 vdc supply voltage is not adjustable as it tracks the +10 vdc supply.

Regulated +10 vdc should measure between 10 vdc and 10.3 vdc at test point TPB on the 3844 or 4844 Sensor Amplifier/Driver in the control card cage. (PE transports may require +10.3 vdc for normal operation.) Regulated -10 vdc should measure approximately -10 vdc at TPA on the same PC board. Plus 5 vdc regulated should measure +5 vdc at TPC and the GRD test point on the same Sensor Amplifier/Driver PC Board.

A12 TIME DELAY	3067-001	3067-002	6067-001	6067-002
R1, R2, R3 C2, Q1, CR2	AS SHOWN	OMIT	AS SHOWN	OMIT
CR2	OMIT	AS SHOWN	OMIT	AS SHOWN
R4, CR3	OMIT	OMIT	- AS SHOWN -	

401-9001-001B1

K1 2 8 5

K1 3 9 6

J2 7 — FROM R2 CENTER TAP

FROM R1 CENTER TAP — J2 5

TO REEL MOTORS

TO OPTIONAL 4843 PIN A

A12
TIME DELAY (SEE TABLE)

R1 2.2K, C1 500, CR2, Q1 2N4990, CR1 C6B, R3 470, R4 4.7K, CR3, C2 100, R2 470

A B K1

(6067 ONLY) BKN 3844 PIN W

115VAC POWER INPUT — RFI FILTER LFI — F1 5A — S4 — P1/J1 — ON/OFF

115V AUX POWER OUTPUT (OPTIONAL) — WHT, GRN, BLK

T1 156-0002-001

RED — 5 9V — 6BLUE — CR5 1N1200A

WHT 1 — 8

BLK 2 — 6

7 9V BRN

ORN — 9

9V 8BLUE — CR6 1N1200A

VIO — 3

9 RED

R3 A 3 B

J8

J1 1 2

K1 1 7 4

CR4 CR1 CR3 CR2 — 1N1184(4) — +24V — -24V

C2 55,000uF

C1 55,000uF

A B C

A3(+24) — J3-1

CR1 OMIT — Q1 MJ1000 — R2 1.5 2W — R3 1.5 2W

C3 1 — R1 2K — R4 510 — C4 100

J1 — +10V (@ 1.4A) — J2-1, J3-3, AIPI-13

11 Vc 12 Vcc — 5 Vr 1 — 6 NI — 13 Comp — 10 Vo — 2 CL — 3 CS — 4 I — 7 Vcc-

C1 4700 — R8 8.2K — R5 SEE TABLE — R6 1.8K — R7 SEE TABLE CW — R9 SEE TABLE — R10 5.6K — R11 2.10K

CR2 — CR3

DASH	-001	-002
	ADJ	FIXED
R5	OMIT	3.32K
R7	2K	OMIT
R9	OMIT	8.25K

A3(-) — J3-2 — -24V

CR4 OMIT — Q2 MJ900 — R17 1.5 2W — R18 1.5 2W — R12 2.10K

R13 2K — R15 510 — R16 8.2K — Q4 2N4403 — R14 100 — C2 4700 — Q3 2N4403

J2 — -10V (@ 1.4A) — J2-2, J3-4, AIPI-15

C5 100 — J4

POWER SUPPLY REGULATOR 190-6414-001

CR7 1N1200A — TO OPTIONAL 4843 PIN 15

J1-1 — +8V — C3 20,000uF

J1-4 — +24V — C1 1

J1-2

Q1 MJ1000 — R7 0.75 2W — R8 0.75 2W — R9 0.75 2W — R6 2K — R10 750

P2-2 — +5V (@ 3.5A)

P2-1

11 Vc 12 Vcc — 5 Vr 1 — 6 NI — 13 Comp — 10 Vo — 2 CL — 3 CS — 4 I — 7 Vcc-

R1 2K — R2 SEE TABLE — R3 SEE TABLE CW — R4 5.6K — R5 SEE TABLE — C2 4700 — R11 10K — C3 33

DASH	-001	-002
	ADJ	FIXED
R2	OMIT	2.10K
R3	2K	OMIT
R5	OMIT	4.99K

POWER SUPPLY REGULATOR 190-6810-001

230VAC POWER INPUT — RFI FILTER — F1 3A — 2 1 4 7 8 6 9 3 J8 J1 1 2

115V AUX POWER OUTPUT (OPTIONAL) — WHT, GRN, BLK

R3 A 6 B

FOR EXPORT WIRING ONLY

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Power Supply, Model 9000, Schematic and Wiring Diagram

MODEL 9000 POWER SUPPLY WITH DC-DC CONVERTER CIRCUIT DESCRIPTION

(6414/6810 Regulators)

PRIMARY POWER

The DC-DC Power Supply, type 7288, converts the input DC power to the equivalent AC input that would normally be supplied to the power supply regulator. The converter includes an input voltage regulator, a switching regulator used to generate the switching wave forms, and current limiting circuitry. These circuits are described below.

Upon power turn on, relay K2 pulls in, supplying the input DC power to the DC-DC power supply. Adjustable regulator CR1, transistor Q1 and the associated resistors regulate the incoming voltage. Voltage divider R2/R3 provides the reference voltage to regulator CR1, which in turn supplies the regulated output voltage as tabulated on the schematic.

In this application switching regulator IC2 is used to generate the required switching outputs only. The internal components of IC2 used for this purpose are an oscillator, a steering flip-flop and a pair of open collector transistors. The oscillator frequency is set by external components C4, R14 and R34.

Normally the switching frequency is 500 cycles; during initial turn-on transistor Q11 adds resistor R34 to the timing network, quadrupling the frequency. The internal oscillator pulses are stretched using external circuitry including transistors Q8 and Q9 and associated components. The oscillator pulses provide a dead zone during the output switching, preventing both output stages from turning on at once, and the pulse stretching provides additional protection. The two complementary collector outputs of IC2 at pins 12 and 13 are applied to a push-pull amplifier stage including Q4 and Q5, whose outputs drive complementary Darlington power stages including Q2, Q3, Q6 and Q7. The outputs of the power stages are connected to opposite terminal of the transformer, while the input DC voltage is applied to the transformer center tap. Current limiting is provided by sensing the voltage across a solder trace used as a 20 milliohm resistor.

When current through the output power stages reaches approximately 20 amp, the output of comparator IC1-1 goes high, causing IC1-7 to go high as well. This causes transistor Q10 to be turned on, grounding the switching outputs at IC2-9.

SECONDARY POWER

TYPE 6414 REGULATOR (+10 vdc/-10 vdc)

Pass transistor Q1 is controlled by output from pin 10 of the uA723 regulator, IC1. Voltage output from the PC board is determined by resistors R6, R10 and adjustment pot R7, or R5 and R9 for nonadjustable versions. Resistors R4 and R8, together with sense resistors R2 and R3 and the regulator circuitry connected to IC1-2 and IC1-3, form a current limiting foldback circuit for protection against shorts on the +10 vdc line. To assure accurate voltage tracking, the regulated -10 vdc is referenced to the regulated +10 vdc through resistor R11, temperature compensating diodes CR2 and CR3 and resistor R12. Transistors Q2 and Q3 form an error amplifier that drives the node between CR2 and CR3 to virtually ground, thus assuring that the -10 vdc supply will track that of the +10 vdc. Similar foldback current limiting for the -10 vdc supply is performed by resistors R15 through R18 and transistor Q4.

TYPE 6810 REGULATOR (+5 vdc)

Pass transistor Q1 is controlled by pin 10 of regulator IC1. As in the case of the +10 vdc supply, shorting protection is accomplished by the foldback current limit circuit composed of bias resistors R10, R11, sense resistors R7, R8 and R9, and the regulator IC's internal circuitry connected to pins 2 and 3. Voltage output is controlled by optional potentiometer R3 and resistors R1 and R4, or R2 and R5 for nonadjustable versions. (R3 is the +5 vdc adjustment.)

POWER SUPPLY VOLTAGE ADJUSTMENTS
(Applies to 190-6414-001 and 190-6810-001 boards only)

Potentiometer R7 on type 6414 Regulator PC board is the +10 vdc voltage adjustment. Potentiometer R3 on the type 6810 Regulator PC board is the +5 vdc adjustment. Regulated -10 vdc supply voltage is not adjustable as it tracks the +10 vdc supply.

Regulated +10 vdc should measure between 10 vdc and 10.3 vdc at test point TPB on the 3844 or 4844 Sensor Amplifier/Driver in the control card cage. (PE transports may require +10.3 vdc for normal operation.) Regulated -10 vdc should measure approximately -10 vdc at TPA on the same PC board. Plus 5 vdc regulated should measure +5 vdc at TPC and the GRD test point on the same Sensor Amplifier/Driver PC board.

401-7288-001 E

A12 TIME DELAY	3067-001	3067-002	6067-001	6067-002
R1, R2, R3 C2, Q1, CR2	AS SHOWN	OMIT	AS SHOWN	OMIT
CR2	OMIT	AS SHOWN	OMIT	AS SHOWN
R4, CR3	OMIT	OMIT	- AS SHOWN -	

DASH NO.		R15	F1	T1	L1
190-7651-001		100,3W	25A	156-4561-001	190-3950-003
190-7651-002		150,3W	20A	156-3909-001	190-3950-004
190-7651-003		400,10W	10A	156-3626-001	190-3950-005

A12
TIME DELAY (SEE TABLE)
R1 2.2K
C1 500
CR2 OMIT
CR1 C6B
R3 470
R4 4.7K
C2 100
Q1 2N4990
R2 470
CR3
TO OPTIONAL 4843 PIN A
(6067 ONLY) BKN 3844 PIN W

P4
RUSSEL AND STOOL 8943R
POWER CONNECTOR
FRONT VIEW

F1, 3AB SEE TABLE
L1 SEE TABLE
VDC
K2-A
K2-C
K2-D
S1 POWER
R15 SEE TABLE
CR7 1N2070
C4 .33
K2 P.D. PM17DY 4PDT
C5 .33
C6 2400
RED
BRN
V_{IN}
V_{IN+}
$V_{IN\,R}$
Q1 2N6038
R1 SEE TABLE
CR1 TIL 4301
R2 SEE TABLE
R3 SEE TABLE
C2 .1 35V
+V
R

+5V
R6 4.7K
R9 4.7K
C3 1
C4 .068
R14 17.8K 1%
SG3524
VCC
CL+
CL-
II
NI
CT
RT
GRD
OSC
COMP
SH
5V
R4 3K
CR2 SEE TABLE
R5 SEE TABLE
Q2 SEE TABLE
Q3 SEE TABLE
Q4 2N4239
R7 470
R8 22
R10 470
R11 22
Q5 2N4239
Q6 SEE TABLE
Q7 SEE TABLE
R12 3K
R13 SEE TABLE
CR4 SEE TABLE
20MIL
CR5 MR822
R17 SEE TABLE
R20 1K
R21 1K
R22 1K, 1%
R18 1K
393
R15 4.7K
R16 4.7K
Q9 2N2222
R19 10K
Q8 2N2222
R23 4.7K
C5 6800 pf
C6 4.7
CR6
R24 62K
R26 1K
R25 1K
R28 1K
R29 2K
R30 2K
R27 10K
Q10 2N2222
R31 4.7K
R32 10K
R33 1K
R34 6.81K
Q11 2N2222
R35 4.7K
R36 4.7K
C8 4.7

DC DC POWER SUPPLY
TYPE 7288

DASH NO.	INPUT VOLT	R1	R2	R3	R5, R13	R17 *	Q2, Q7	Q3, Q6	CR2, CR4	+V
-001E	24V	470 3W	10K 1%	2.1K 1%	68 3W	8.25K 1%	MJ802	MJ802	1N5923B 8.2V	16V
-002E	28V	470 3W	11.3K 1%	2.0K 1%	100 3W	8.25K 1%	MJ802	MJ802	1N5923B 8.2V	18.2V
-003E	48V	3K ½W	8.06K 1%	1.0K 1%	270 3W	8.25K 1%	2N6306	2N6653	1N4740A 10V	25V

*SUGGESTED VALUE ONLY FOR R17. VALUE MAY GET CHANGED DURING TEST FOR A MAXIMUM CURRENT OF 20 AMPS.

T1
SEE TABLE
CR5 1N1200A
CR6 1N1200A
RED
BLUE
BROWN
CR7 1N1200A
CAN GO TO 4843 PIN 15
C3 20,000

OMITTED WHEN NOT REQ'D
J5
7,8,9
4,5,6
K3
CR10 1N2069
TO K1-5

K1
TO K3-8
FROM R2 CENTER TAP
FROM R1 CENTER TAP
J2-7
J2-5

C1 55,000
CR4
CR1
1N3900 (4)
CR3
CR2
+24V
-24V
C2 55,000

A
B
CR1 OMIT
Q1 MJ1000
R2 1.5 2W
R3 1.5 2W
C3 1
R1 2K
R4 510
R5 SEE TABLE
R6 1.8K
R7 SEE TABLE
R8 8.2K
R9 SEE TABLE
R10 5.6K
R11 2.10K
CR2
CR3
C4 100
C1 4700
VC VCC VR NI COMP VCC- 723
J1
+10V (@1.4A)
J2-1, J3-3, A1P1-13
A3(+)
J3-1

DASH	-001	-002
	ADJ	FIXED
R5	OMIT	3.32K
R7	2K	OMIT
R9	OMIT	8.25K

CR4 OMIT
R17 1.5 2W
R12 2.10K
Q2 MJ900
R13 2K
R14 100
R15 510
R18 1.5 2W
Q4 2N4403
R16 8.2K
C2 4700
Q3 2N4403
C5 100
J2
-10V (@ 1.4A)
J2-2, J3-4, A1P1-15
A3(-)
-24V
J3-2
J4

POWER SUPPLY REGULATOR 190-6414-001

J1-1
+8V
J1-4
+24V
J1-2
P2-2
J3-5
+5V (@ 3.5A)
Q1 MJ1000
R7 0.75 2W
R8 0.75 2W
R9 0.75 2W
R6 2K
R10 750
R11 10K
C3 33
C1 1
C2 4700
R1 2K
R2 SEE TABLE
R3 SEE TABLE
R4 5.6K
R5 SEE TABLE
CW

DASH	-001	-002
	ADJ	FIXED
R2	OMIT	2.10K
R3	2K	OMIT
R5	OMIT	4.99K

POWER SUPPLY REGULATOR 190-6810-001

D.C. Power Supply
Schematic and Wiring Diagram

TYPE 3842 INTERFACE CONTROL

CIRCUIT DESCRIPTION

This module contains a set of receivers for the interface control commands:

SYNCHRONOUS FORWARD SFC
SYNCHRONOUS REVERSE SRC
OVERWRITE OVW
REWIND RWC
SELECT SLT
SET WRITE STATUS SWS
OFF LINE OFFC

It also contains drivers that return the recorder status outputs to the interface:

ON LINE ONL
REWINDING RWDG
FILE PROTECT FPT
LOAD POINT LP
WRITE ENABLE WEN
READY RDY
END OF TAPE EOT
TAPE RUNNING TNG

Certain controls and delays are also provided to ensure proper tape motion and transport operation.

TAPE MOTION CONTROLS

The motion control commands from the interface, SFC and SRC, are translated on this card into the internal motion commands of the transport — RUN NORMAL $\overline{\text{RNN}}$, FORWARD $\overline{\text{FWD}}$, and REVERSE $\overline{\text{RVS}}$. These internal motion commands are supplied to the Pushbutton Control module, where they are combined with commands supplied from the transport pushbuttons and internal interlocks to generate the commands that initiate actual tape motion on the Ramp Generator module.

On this module SFC and SRC are supplied to an interlocking network that ensures that the tape comes to a stop before its direction of motion is reversed. The interlocking network includes flip-flop IC1-3, edge circuits IC2-6 and IC2-8, NAND gate IC3-6, and interlocking flip-flop IC3-10. Whenever flip-flop IC1 changes states due to a change in the direction of motion, for example from a reverse command SRC to a forward command SFC, its output generates a pulse through the edge circuits consisting of inverters IC2 and the associated capacitors. The pulse is gated through IC3-6 to the set input of interlocking flip-flop IC3-10. The flip-flop can be set only if TAPE RUNNING $\overline{\text{TNG}}$ is true, indicating that the tape is still moving. In this case $\overline{\text{TNG}}$ low at input pin W is inverted by IC18-12 and supplies a high input to the clear of IC3. The flip-flop can then be set by the pulse on its set input, its 0 output going low. The 0 output of IC3 then inhibits the RUN NORMAL gate IC15 at pin 2, setting RUN NORMAL $\overline{\text{RNN}}$ false. After the tape has ramped down to a stop, TAPE RUNNING $\overline{\text{TNG}}$ goes false, clearing interlocking flip-flop IC3, whose output then enables the RUN NORMAL gate. RUN NORMAL $\overline{\text{RNN}}$ then goes true if the following conditions are satisfied: SELECT SLT1 is true, indicating that the transport is on line and selected by the interface; BUSY $\overline{\text{BSY}}$ is false, indicating the transport is not rewinding or searching for load point; and SRC command is not given at load point. (This would activate NAND gate IC15-8 and would disable the RUN NORMAL gate at IC15-1.) If the above conditions are satisfied, RUN NORMAL $\overline{\text{RNN}}$ goes true at output pin V, and is supplied to the Pushbutton Control module where it initiates tape motion at the normal running speed. The direction of motion is determined by the state of flip-flop IC1. If a forward command SFC has been given, the flip-flop is set and its 1-output enables NAND gate IC14-8, provided that SLT1 is true and $\overline{\text{BSY}}$ is false. This generates FORWARD $\overline{\text{FWD}}$ true at output pin U. If a reverse command SRC has been given, flip-flop IC1 is cleared and enables NAND gate IC14-6, generating REVERSE $\overline{\text{RVS}}$ true, providing SLT1 is true, $\overline{\text{BSY}}$ is false, and LOAD POINT LP is false. No interface reverse command is acknowledged by the transport when the load point is detected.

WRITE SELECT

During a write operation the interface supplies SET WRITE STATUS SWS true at pin K; SWS is inverted by IC9-4 and is supplied to the D input of flip-flop IC7. The flip-flop is toggled provided that the transport is selected and on line, after NOR gate IC1-11 is activated by a synchronous motion command. This would activate NAND gate IC1-8 and trigger one-shot IC4-1, generating a 2 μsec pulse. On the trailing edge of the pulse the $\overline{\text{Q}}$ output of the one-shot toggles IC7-3, the Q output of the flip-flop going high and activating NAND gate IC10-11, generating WRITE SELECT WSEL true at output pin H. During an overwrite operation OVERWRITE OVW true is inverted by IC18-8 and sets the D input of flip-flop IC7-12

high. On the trailing edge of the pulse generated by one-shot IC4-4 the flip-flop is set and enables NAND gate IC8-12. One-shot IC4-4 also direct-sets flip-flop IC11, whose Q output enables the overwrite gate at IC8-9. If write status is true, the gate is enabled at IC8-13 and it is kept activated as long as a synchronous motion command is activating NAND gate IC1-8. IC8-8 then goes low and supplies $\overline{\text{WSEL}}$ for the duration of the motion command only. When a WRITE AMPLIFIER RESET pulse is given at pin P, it toggles flip-flop IC11 to the cleared state and disables the overwrite gate.

REWIND FLIP-FLOP

When a REWIND COMMAND RWC is given by the interface, it sets the rewind flip-flop IC5-3, provided that the transport is selected, on line, and not at load point. The 1-output of the flip-flop then goes high, generating REWINDING RWDG true to the interface, and a rewind command $\overline{\text{RWC1}}$ through an edge circuit consisting of inverter IC6-6, NAND gate IC6-8, and capacitor C5. $\overline{\text{RWC1}}$ is supplied to the Pushbutton Control module. The flip-flop is cleared when the tape returns to and stops at load point, or when BROKEN TAPE BKN is detected.

END OF TAPE

An end of tape indication is set when the EOT marker is encountered in forward direction and remains set until the marker is passed in the reverse direction.

A true EOT signal at pin Z if machine status is $\overline{\text{RWDG}}$ (IC10-5, 8) and $\overline{\text{RVS}}$ (IC14-6) causes IC11 to be preset by IC19-8. An EOT status is then signaled at the interface by IC16-3.

Upon passing the EOT marker in the reverse direction IC13-3 is high and the EOT signal clocks IC11 clear on the trailing edge of the EOT signal dropping the EOT signal at the interface. IC11 is preset to the clear state by BKN signal at pin X.

OUTPUT STATUS

Most status gates on this module are preconditioned by SELECT and ON LINE being true; consequently, the transport returns status indications only when it is selected and on line. The READY status is generated when BUSY $\overline{\text{BSY}}$ supplied from the Pushbutton Control module is false and the transport is not rewinding. The LOAD POINT output is also preconditioned by the rewinding status being false. The only status gate not preconditioned is the rewind via the REWIND pushbutton. If the pushbutton is used to rewind, that status is made available to the interface without being selected and on line.

401-3842-001K

CONTROL TERMINATOR CARD, 3841

CONTROL INTERFACE CONNECTOR J1

OVW	B	T	A	OVW (IC 7-12)
SFC	C	T	5	
SRC	E	T	8	
RWC	H	T	10	
SLT	J		11	
SWS	K	T	12	
OFFC	L	T	13	
ONL	M	P	14	
RWDG	N	P	15	
FPT	P	P	16	
LDP	R	P	17	
WEN	S	P		
RDY	T		19	
EOT	U		20	
TNG	V		21	

WARS1 (FROM WA1-M)

2 BACKWARD STATUS

22 WRITE STATUS

R4 220 · R5 330 · R3 4.7K · R2 4.7K · R1 4.7K · C1 100 · C2 100 · C3 2000 · C4 1000 · C5 2000 · C6 100

ST1 STRAP · ST2 OMIT · ST3 OMIT · ST4 OMIT · ST5 OMIT · ST6 OMIT

CR1 OMIT · CR2 1N270

SEE TABLE · CT1 SEE TABLE

LP (IC18-6) · TNG (PIN W) · LP (PIN Y) · ONL (PIN R) · BSY (PIN N) · OVW (IC 7-8) · TNG (PIN W)

D	+5V			
C	GRD			
W	TNG	(FROM RAMP GENERATOR-Z)		
V	RNN	(TO PUSHBUTTON CONTROL-18)		
U	FWD	(NOT USED)		
T	RVS	(TO PUSHBUTTON CONTROL-16)		
N	BSY	(FROM PUSHBUTTON CONTROL -13)		
S	WRDY	(FROM PUSHBUTTON CONTROL-J)		
F	SLT1	(TO (A10J4-W CONTROL MB; SENSOR AMPL DRIVER-Z)		
K	REWIND LAMP	(FROM PUSHBUTTON CONTROL-L)		
Y	LP	(FROM SENSOR AMP/DRIVER-19)		
L	RWC1	(TO PUSHBUTTON CONTROL- M)		
M	OFFC1	(TO PUSHBUTTON CONTROL-12)		
H	WSEL	(TO PUSHBUTTON CONTROL-7)		
R	ONL	(FROM PUSHBUTTON CONTROL-14)		
X	BKN	(FROM SENSOR AMP/DRIVER-18)		
Z	EOT1	(FROM SENSOR AMP/DRIVER-X)		
J	FPT	(FROM SENSOR AMP/DRIVER-9)		
E	EOT2	(TO PUSHBUTTON CONTROL-22)		

CONTROL TERMINATOR CARD HAS TERMINATORS (T) 220-330 OHM AND PULL-UPS (P) 4.7K AS SHOWN

DASH NO.	CT1	ST5	ST6
001H	NO CUT	OMIT	OMIT
004	SEE SEPARATE SCHEM.		
005	SEE SEPARATE SCHEM.		
006A	CUT	OMIT	ADD

Interface Control, Type 3842, Schematic Diagram

MODEL 9000 SERIES TAPE MOTION CONTROLS

CIRCUIT DESCRIPTION
(TYPE 3843, 3855, 3865 PC BOARDS)

The circuitry used to carry out the motion commands issued by the interface or by the pushbutton panels, both the main control panel and the test panel, is located on Pushbutton Control Type 3843 module. This module generates the motion command lines RUN NORMAL RNN1, RUN FAST RNF1, and REVERSE RVS1, which are supplied to the ramp generator module to initiate actual tape motion.

FRONT PANEL PUSHBUTTON CONTROLS

The LOAD, ON LINE, and REWIND pushbuttons, situated on the main control panel, are connected to respective flip-flops on the Pushbutton Control Card Type 3843. When the LOAD pushbutton is activated, it grounds the input to inverter IC12-1, setting the LOAD flip-flop consisting of NOR gate IC13-6 and inverter IC12-1. Once the LOAD flip-flop is set IC13-6 goes low, is inverted by IC12-4 and removes the direct-clear from the ON LINE flip-flop IC10-3. Thus the ON LINE flip-flop can be set only after the transport has been loaded. When the ON LINE pushbutton is activated the first time, it toggles IC10-1 to the set, or ON LINE, position, the outputs of the flip-flops generating ONL and $\overline{\text{ONL}}$ true. Inverters IC12-8 and IC12-10 are connected as a protective flip-flop on the clock input to IC10-1. Once the ON LINE flip-flop has been set, ONL true is inverted twice by IC9 setting the common of the REWIND pushbutton on the control panel high, disabling that pushbutton. The ON LINE flip-flop can be cleared by pressing the front panel pushbutton a second time, or by an interface OFF LINE COMMAND OFFC1, supplied from the interface control module.

The REWIND pushbutton can be activated only when the transport is off line. When activated the REWIND pushbutton sets the flip-flop consisting of gates IC8-8 and IC8-6, provided that the transport is loaded at the time (LOAD true at IC8-13) and test mode is not selected (IC7-8 high). Consequently the transport cannot be rewound by the pushbutton during test mode, or when on line, or when LOAD is false. When the transport is on line the rewind flip-flop can be alternately set by interface REWIND COMMAND $\overline{\text{RWC1}}$, supplied from the interface control module. The output of the rewind flip-flop, REWINDING $\overline{\text{RWDG1}}$, activates NOR gates IC15-8 and IC14-6, generating RNF1 and RVS1 true to the ramp generator module, initiating a fast reverse motion to load point. When load point is detected the photosensor amp driver module supplies the load point pulse at input pin H of the pushbutton control module, clearing the rewind flip-flop.

An additional flip-flop, IC1-6, is used to locate the tape position. Before the tape is loaded, the flip-flop is cleared by LOAD false at IC10-8. When the transport is loaded the direct-clear is removed and NAND gate IC14-11 is enabled. Since the on tape flip-flop is still cleared, its $\overline{Q}$ output high activates NAND gate IC14-8, generating a RUN NORMAL RNN1 at output pin Y, advancing the tape to load point. When the load point marker is detected, LP true at input pin 21 from the photosensor module is gated through IC16-3 and direct-sets flip-flop IC10-7 to the ON TAPE state, terminating the tape motion. Similarly, when load point is detected during reverse tape motion, the ON TAPE flip-flop is toggled by NAND gate IC16-11 to the clear state, initiating forward tape motion back to load point.

BUSY

This module generates a BUSY output when the tape is not loaded, when it is advancing to load point, or when the transport is off line and not in test mode. In any of these cases NOR gate IC4-8 is activated and supplies $\overline{\text{BSY}}$ true to the interface control module.

WRITE READY

WRITE READY true is generated in two different cases: when the interface supplies WRITE SELECT true and the transport is not in test mode ($\overline{\text{TM}}$ false), or when the transport is in the write test mode and flip-flop IC6-14 is set. In either case NOR gate IC1-8 is activated, enabling NAND gate IC4-5. The gate is activated provided that BUSY $\overline{\text{BSY}}$ is false, FILE PROTECT $\overline{\text{FPT}}$ is false, and the transport is not in reverse motion (RVS1 is false). IC4-3 then goes low, is inverted by IC5-12 and generates WRDY true at output pin J to Write Amplifier Type 3848.

TEST PANEL CONTROL

In order to activate the test panel the transport must be off line, and the test panel STOP pushbutton must be depressed. In that case the TEST MODE pushbutton on the test panel can be activated, setting the flip-flop consisting of inverters IC11-8 and IC11-10, which in turn toggles the test mode flip-flop IC6-6

to the test mode state, generating TM and $\overline{TM}$ true. The test mode flip-flop is direct-cleared when the transport is placed on line, or when the TEST MODE pushbutton is activated a second time. After the test mode flip-flop has been set the other test panel pushbuttons are enabled. The WRITE TEST pushbutton may then be activated, setting the protective flip-flop consisting of inverters IC11-4 and IC11-6, which in turn toggles the write test flip-flop IC6-1 to the write test mode, provided that forward motion is selected. The $\overline{Q}$ output of the write test flip-flop then activates NOR gate IC1-8, in turn activating the write ready gate IC5-3, provided that FILE PROTECT FPT, REVERSE RVS1, and BUSY $\overline{BSY}$ are all false. In that case WRITE READY WRDY true is generated at output pin J to the write amplifier module, where it enables the write data strobe circuitry. During the write test the write amplifiers generate consecutive all-1 characters which may be used to adjust the skew.

Additional test panel pushbuttons are FORWARD RUN, a normal forward run button, FAST FORWARD, a high speed forward button, REVERSE and FAST REVERSE buttons. The reverse motion buttons can be activated only if the on tape flip-flop IC10 is set and the tape is not at load point, activating NAND gate IC3-3, which in turn activates NAND gate IC7-6 (when the test mode flip-flop is set) and setting the common of the reverse buttons low. The forward motion commands are terminated when either the STOP pushbutton is activated, clearing the test mode flip-flop, or end of tape is detected, in which case EOT1 true is inverted by IC17-4, disabling NAND gate IC7-3, and setting the common of both forward motion buttons high. Similarly the reverse motion can be terminated by activating the STOP pushbutton, which terminates all test mode operations, or when load point is detected, in which case LP true is inverted by IC17-3 and disables NAND gates IC3-3 and IC7-6, setting the common of the reverse buttons high. The pushbutton control module also drives the test panel indicators, lighting the data lamp when any data is being processed by the write/read electronics, illuminating the skew indicator when the skew is out of adjustment, illuminating the EOT indicator when the transport is at end of tape, and illuminating the LOAD POINT indicator when the transport is at the beginning of tape.

401-9000-09081

PUSHBUTTON CONTROL CARD TYPE 3843

MAIN CONTROL PANEL 3855

	STD	TMZ	AUTO RESTART
3843	001J	002E	003C
ST1	STRAP	OMIT	STRAP
ST2	OMIT	STRAP	OMIT
C6	OMIT	220	OMIT
ST3	OMIT	OMIT	STRAP
ST4	OMIT	OMIT	STRAP

TEST PANEL 3865

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Tape Motion Controls, Type 3843, 3855, 3865, Schematic Diagram

TYPE 4843 AUTO POWER RESTART PC BOARD
CIRCUIT DESCRIPTION
(OPTIONAL PC BOARD)

Introduction

When incorporated in any of the Kennedy Model 9000, 9100, 9300, 9700, 9800, or 9832 recorders, the type 4843 Pushbutton Control module allows use of several factory optional features. These functions are determined by optional straps and the use of components in the APR field. Not all functions and/or combinations of such are available with every 9000 series recorder. Refer to schematic 401-4843-001 and the dash number of your particular 4843 module for features that have been incorporated and tested at the time your unit was built. Due to the interaction of several of these options the user is advised to consult the factory in writing if he desires to incorporate any additional optional features through field modification. Failure to do so invites the possibility of voiding the warranty of the particular recorder involved.

The major optional features along with suggested usage are outlined below. (Reference is made to schematic 401-4843-001.)

ON TAPE (OT)

Determined by the placement of option strap 1. If this option is specified at the time of factory order, the operator cannot place the tape unit on line until a reel of tape is loaded and positioned at or past the BOT tab.

ONLINE LOCK (ONLL)

Determined by the placement of option strap 2. When specified at the time of factory order, this feature prevents the operator from manually taking the tape unit off line via the front panel switch, unless the tape controller has allowed him to do so. This signal is not normally gated with select and is an input signal line on interface connector J1-A.

FAST (FST)

Determined by diode CR2 and a special control interface module. When specified at the time of factory order, this feature allows interface control of high speed forward and high speed reverse motion of tape. It is used in conjunction with the Synchronous Forward, Synchronous Reverse, and the optional Fast line at the control interface connector of the deck. High speed forward and reverse commands will be accepted when the tape is on line and selected. The high speed reverse command will be implemented at any time when tape is positioned past the BOT tab and the high speed forward command will be carried out only when tape is positioned at or between the BOT and EOT tabs (past EOT, a fast forward command will cause tape to advance at the normal synchronous forward speed). Note: This feature should be used only for purposes of high speed search, as writing cannot be done at high speeds.

AUTO POWER RESTART (APR)

Determined by the configuration of components in the APR field and external assemblies (in some models) driven by this module. When specified at the time of factory order, this option will protect the tape unit against "brownout" and will automatically power up, load, and set the deck on line under certain conditions. With the standard APR option this circuitry continually monitors the line voltage and whether the tape unit is on line or off line. If the external line voltage falls below a minimum value required by the tape deck, this option will force the deck into an off-line state along with issuing a BROKEN TAPE command (i.e., the reel and capstan servos will be disabled and any write current is inhibited). When the input power level returns to an acceptable value, the APR circuitry will do one of two things, depending on whether the deck was on line before the power fell: (1) nothing, if the deck was in an off-line state, or (2) load, advance tape several inches and place the deck on line if it was previously in an on-line state. Additionally, if APR circuitry is used in the Model 9832 buffer, it will issue an INITIALIZE signal (i.e., clear the buffer memory) when power is returned.

OPTIONAL LOAD ON LINE FEATURE

A factory variation (to be specified at time of order) of the standard APR option is the LOAD ON LINE (LOL) feature. If specified, this allows the user, through a control interface signal, to load and place the tape deck on line. The LOL signal is acknowledged only after external power has dropped and returned to an acceptable level and the deck is in an unloaded state. If the LOL feature is used, it is the user's responsibility to provide a TTL logic low-going pulse (minimal pulse duration 500 milliseconds) after power is returned to an acceptable level. The LOL signal is not gated with SELECT and appears as an input signal on interface connector J1A.

SUGGESTED USAGE OF APR FEATURE

The standard APR circuitry is activated only when the deck is placed on line and is deactivated when the deck is placed off line. (In the case of the LOL variation, circuitry is activated only when power has failed and then returned when the deck is in an unloaded state.) Thus, when manually loading a reel of tape on the deck, the APR feature is transparent to the operator and only comes into play when

external power has failed with the tape deck in an on-line state. The tape deck must be mounted in a vertical positon to avoid spilling of tape in the case of power failure. Proper positioning of commands after the APR circuitry has repowered the deck depends on the particular mode of operation and should be determined by the application. If a rewind was in process at the time of power failure, the tape may stop and become repositioned up to 5 feet before load point. For proper operation in this case, tape should be spaced forward 6 feet and then rewound. For any other mode of operation, it is suggested that a REWIND command be issued immediately after an APR power-up. The LOL signal is not gated with SELECT and appears as an input signal on interface connector J1A.

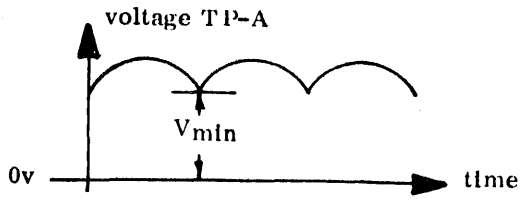
The APR circuitry is designed to operate under conditions of power failure external to the tape deck. Power failure simulations made via the front panel power switch do not come under the above category since this power switch is located between an input power RFI filter and the power transformer.

AUTO POWER RESTART ADJUSTMENT

Normal field adjustment of the Auto Power Restart board is not required unless a new APR board is placed in a machine or an existing board has been refurbished. If this is the case, the following field procedure is recommended:

1. Power up machine and adjust R18 fully CW.

2. Monitor TP-A and TP-B with a scope. TP-B is a logic level and will be high. TP-A is the prereguläted +5 vdc and will appear on the scope as illustrated below:



3. Adjust the input power voltage to the machine so that the value of V_{min} (as shown above) equals the value stated on schematic 401-4843-001 of the APR PC board.

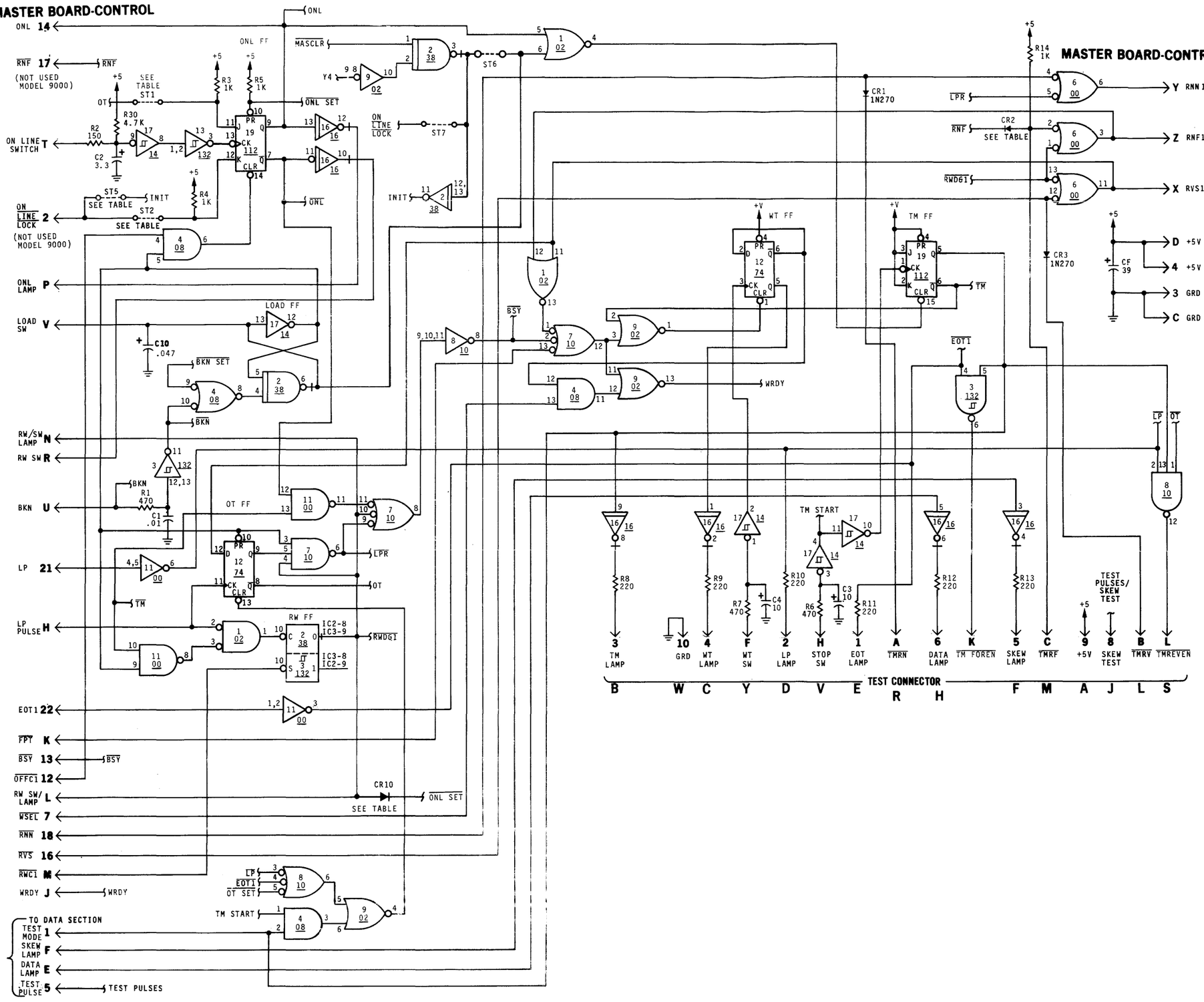
4. Turn R18 CCW until the voltage appearing at TP-B goes low.

APR OPERATION IN MODELS 9100/9300

APR operation in these vacuum column tape transports is identical to the above description with the following exceptions:

a) Manual and power failure initiated load sequences take approximately twice as long due to the increased tape tensioning time required to prevent oversized tape loops from forming in the vacuum columns during a power failure.

b) The manual and APR load sequences are now as follows: Tension Tape; Load Columns, Search forward to load point; if load point is not found after a given time out period, rewind to load point; then place unit online.



APR Pushbutton Control, Type 4843, Schematic Diagram Sheet 1 of 2

STATE	FUNCTION	NEXT (JUMP)	JUMP CONDITION
0	$\overline{\text{BKN SET}}$	1 (0)	$\overline{\text{MAS CLR}}$
1	$\overline{\text{BKN SET}}$	2 (0)	$\overline{\text{MAS CLR}}$
2		3	
3		4	
4		F (7)	$\overline{\text{LOL}}$
5		6	
6		7	
7		8	
8	$\overline{\text{LOSET}}$	9	
9	$\overline{\text{LOSET}}$	A	
A	$\overline{\text{OTSET}}$	B	
B	$\overline{\text{OTSET}}$	C	
C	$\overline{\text{ONLSET}}$	D	
D	$\overline{\text{ONLSET}}$	E	
E	ENABLE	E (0)	$\overline{\text{MAS CLR}}$
F	ENABLE	F (0)	BKN

X TABLE

DASH NO.	-0YZ	-1YZ	-2YZ	-3YZ	-4YZ	-5YZ	-6YZ	-7YZ	-8YZ	-9YZ
SPEED(IPS)	-	10	12.5	15	18.75	25	37.5	45	75+	—
R25	OMIT	180K	150K	100K	82K	68K	47K	39K	2.2M	3.3M

Y TABLE

DASH NO.	-X0Z	-X1Z	-X2Z	-X3Z	-X4Z	-X5Z	-X6Z	-X7Z	-X8Z
FIRST USED ON	9000	9100/9300	9000/9700/9800		9832		9700/9800	9100/9300	9100/9300
FUNCTION	STD	LOL	LOL	AUTO	LOL	AUTO	AUTO RW	AUTO	AUTO/OT
APR CIRCUIT		●	●	●	●	●	●	●	●
ST3, RELAY K1				●		●	●	●	●
ST4			●	●	●	●	●		●
ST5					●	●			
ST6	●		●	●	●	●	●		
ST7		●						●	●
ST8	●		●	●	●	●	●		
ST9		●						●	●
DIODE CR10							1N270		

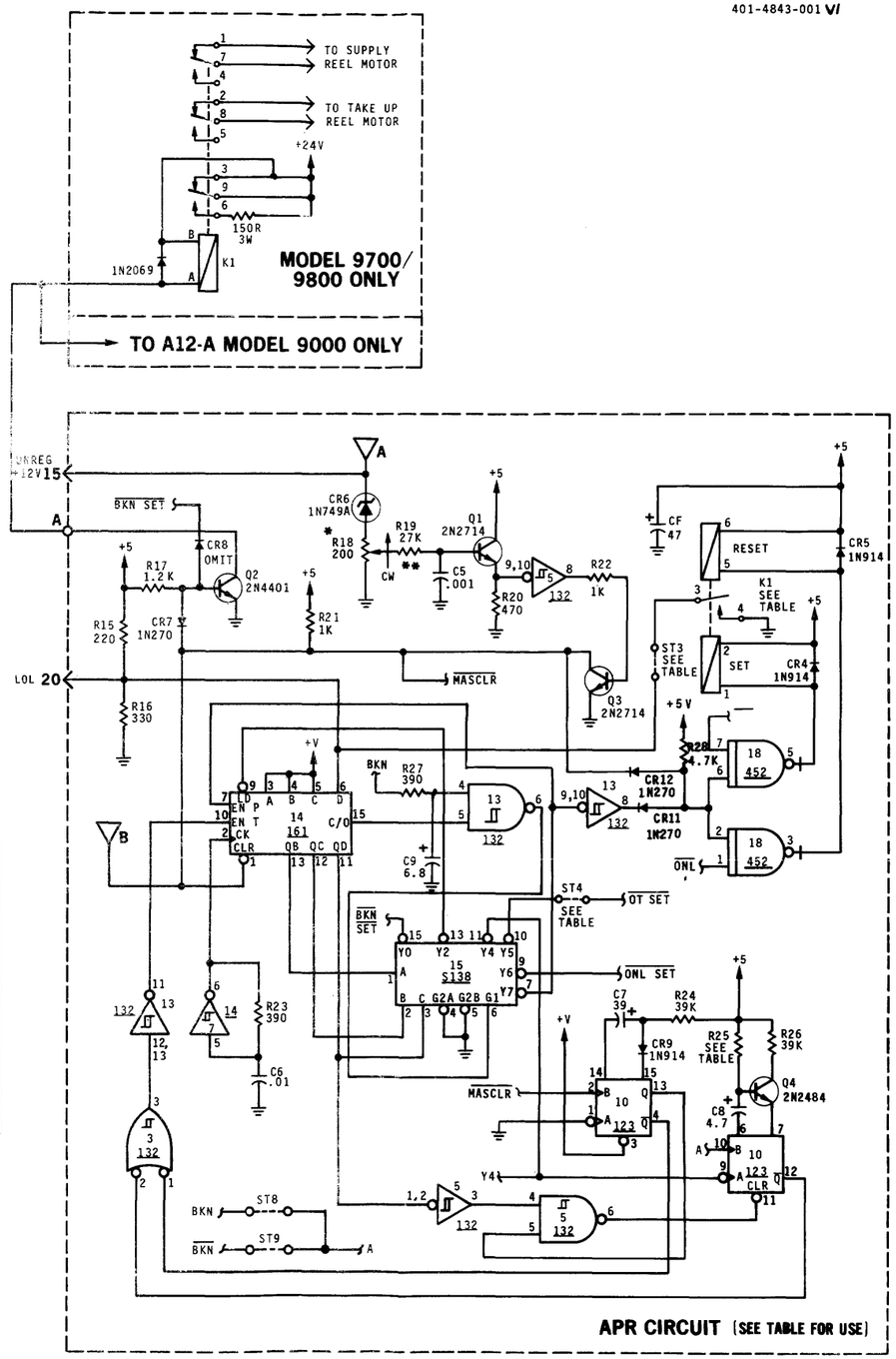
Z TABLE

DASH NO.	-XY1	-XY2	-XY3	-XY4	-XY5	-XY6	-XY7	-XY8
FUNCTION	STD	OT	ONLL	OT/ONLL	FAST	OT/FAST	ONLL/FAST	OT/ONLL/FAST
ST1 (OT)		●		●		●		●
ST2 (ONLL)			●	●			●	●
CR2 (FAST)					1N270	1N270	1N270	1N270

●=USED

*ADJUST R18 SUCH THAT SIGNAL AT TEST POINT B GOES LOW WHEN VOLTAGE FALLS BELOW 6.25 ±.15V MIN AT TEST POINT A (NOTE SCHMITT ACTION OF IC5-3)
**FACTORY SELECT

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.



APR CIRCUIT (SEE TABLE FOR USE)

APR Pushbutton Control, Type 4843, Schematic Diagram Sheet 2 of 2

TYPE 3844 SENSOR AMPLIFIER DRIVER CIRCUIT DESCRIPTION

This module responds to signals from photoresistive cells which sense load point and end of tape reflective strips, and broken tape. In addition, this module contains the file protect circuitry, the write and the erase head drives.

BOT, EOT, AND BKN SENSOR AMPLIFIERS

The load point sensor amplifier and the end of tape sensor amplifier operate interdependently to detect the load point and the end of tape markers. The active components in detecting EOT and load point are two operational amplifiers, IC6 and IC8, and two transistors, Q1 and Q2, in conjunction with associated components. Transistors Q1 and Q2 act as current sources; potentiometer R16 is used to adjust the transistor base currents to equalize the voltage at the inputs of IC8, the load point sensor amplifier, and IC6, the end of tape sensor amplifier. Resistors R18, R19, R20, and R21 are used to bias the amplifiers' inputs when plain tape is in front of the photo-sensors. When either the load point marker or the end of tape marker is detected, the Connector board will generate a high signal at either pin Y or Z of this module. Resistors R17 and R22 serve as feedback loops for noise protection. Thus when load point is detected, the load point sensor output at input pin Y of this module saturates IC8, causing its output to go high, and is inverted twice by IC7 to generate LOAD POINT LDP true at output pin 19 to the Pushbutton Control module. The output of inverter IC7-8 is also supplied to an edge circuit which produces a 1 usec pulse on the trailing edge of LDP. This pulse is output at pin 8 to the Pushbutton Control module. The EOT sensor amplifier operates in the same manner, generating a high output when the EOT marker is detected, and supplying EOT true at output pin X to the Pushbutton Control and Control Interface modules.

When LP and EOT sensors are active at the same time a broken signal is generated at the Connector board. This signal turns on Q3. The collector of the transistor goes to ground, generating broken tape BKN true at output pin 18. When LOAD is high at input pin U the output of IC4-8 is low. This causes the collector of Q3 to be low through diode CR3 and the BKN output will be true at output pin 18. Also when power is initially turned on capacitor C9 will cause the BKN output to be high which presets the LOAD flip-flop on the Interface Control module.

FILE PROTECT CIRCUITS

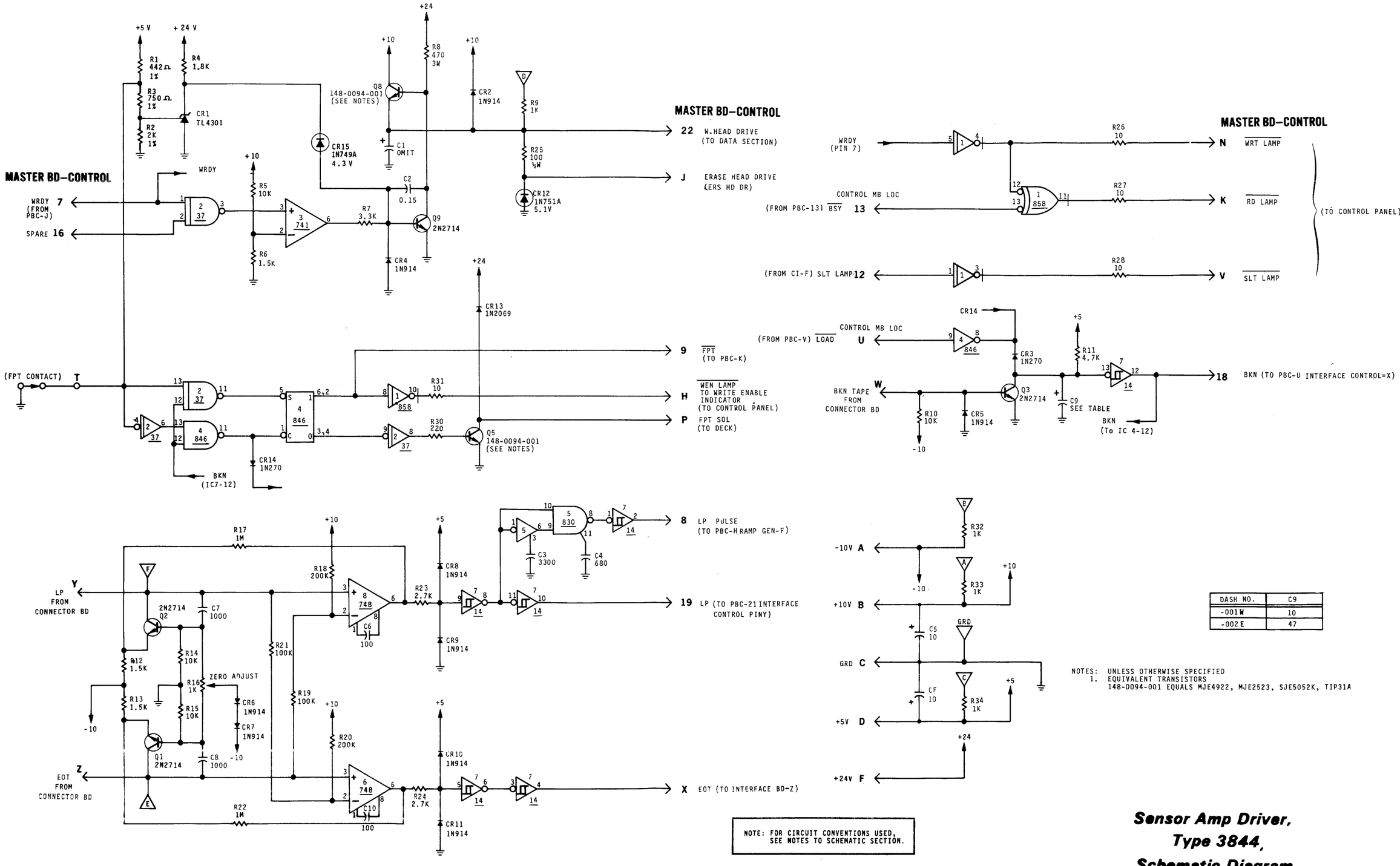
The file protect switch output is supplied to this module at input pin T. When a reel is loaded without a write enable ring, the switch contact remains grounded; the switch input at pin T is inverted by IC2-6 and enables NAND gate IC4-13. The gate is activated when BKN is true before the transport is loaded. Whenever the LOAD pushbutton has not been energized, IC4-8 low grounds the clear input of flip-flop IC4-1 through diode CR14. IC4-2 then issues FILE PROTECT FPT/ true at output pin 9 to the Interface Control card, while the 0 output of IC4 high is inverted by IC2-8 to turn off transistor Q5, disabiling the file protect solenoid output at pin P.

When a reel with a write enable ring is used, the file protect switch is opened, setting input pin T high and enabling NAND gate IC2-13. Again the gate can be activated only when BKN is high, before the transport is loaded. The output of the gate then goes low to set flip-flop IC4-5; the flip-flop can be set only after LOAD/ has gone false. This provision is made to ensure that the write mode can be selected only at the time tape is first loaded. Once flip-flop IC4 is set, its 1 output issues FPT/ false, and after being inverted by IC1-10 lights the WRITE ENABLE LAMP through output pin H. The 0 output of the flip-flop low is inverted by IC2-8 and turns on transistor Q5, activating the file protect solenoid through pin P. The file protect solenoid then draws in the switch pin, and the transport is ready for the write operation.

WRITE, ERASE DRIVES

When the file protect siwtch is grounded, it also turns off transistor Q7, in turn shutting off the current at the base of Q8. This cuts off the write head and erase head drive currents supplied by transistor Q8. In order for the write and erase drives to be turned on, the file protect switch must be opened and WRITE READY must be true at input pin 2. This will activate NAND gate IC2-3, causing op amp IC3 to turn off transistor Q9, in turn enabling transistor Q8 to turn on and supply the write and erase head drives at pins 22 and J.

The zener diode into the base of Q7 detects when power is being dropped. This turns off Q7 early enough in the power down sequence to turn on Q9 and remove the head voltage supplied by Q8. This avoids putting unwanted remnants on tape during a power failure.

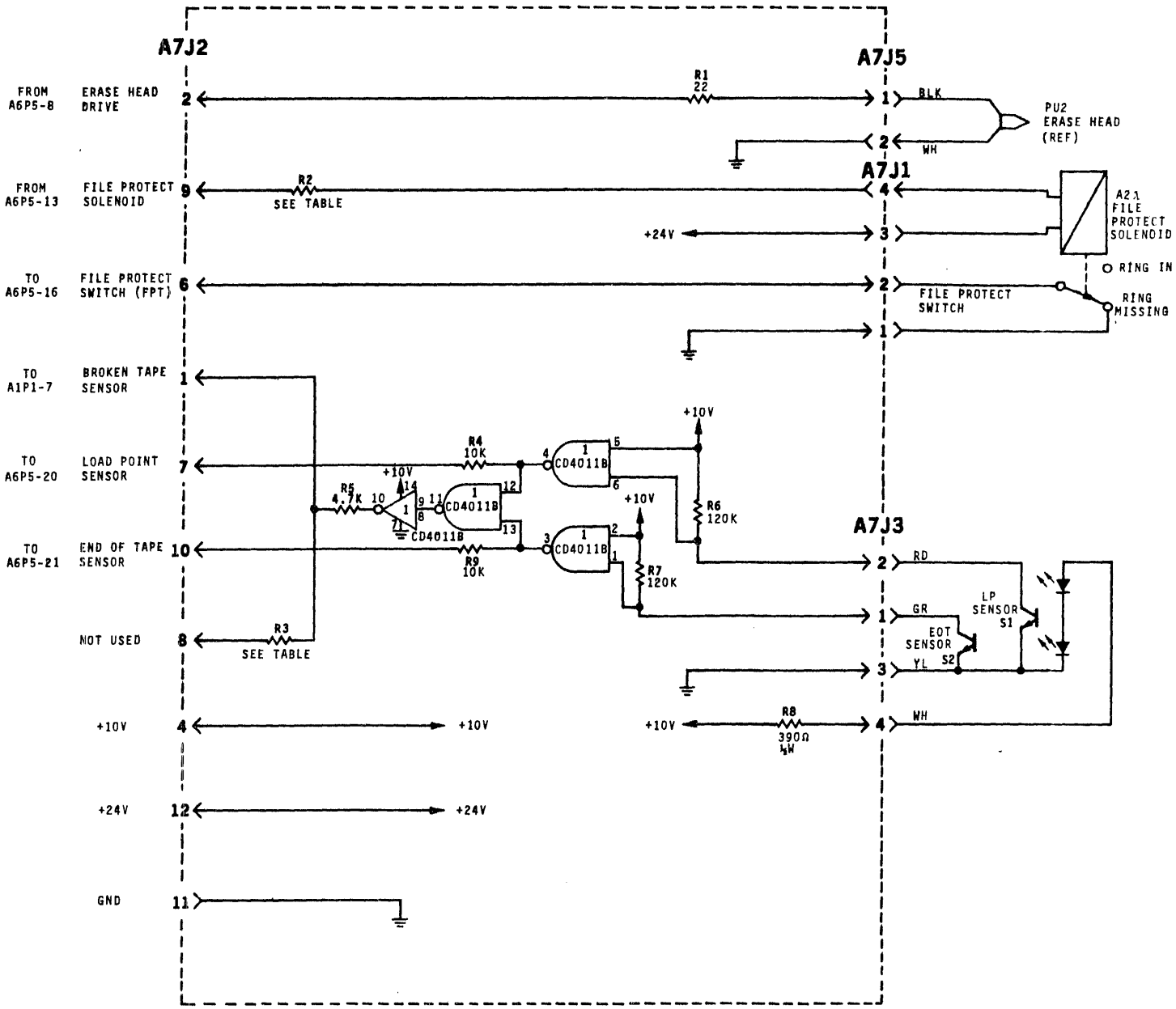


DASH NO.	C9
-001W	10
-002E	47

NOTES: UNLESS OTHERWISE SPECIFIED
1. EQUIVALENT TRANSISTORS
148-0094-001 EQUALS MJE4922, MJE2523, SJE5052K, TIP31A

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Sensor Amp Driver, Type 3844, Schematic Diagram



DASH NO.	R2	R3
001	STRAP	2.2K
002	15,3W	2.2K
003	STRAP	OMIT

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Connector Board Type 5303 Schematic Diagram

CAPSTAN SERVO AMPLIFIER TYPE 3264

CIRCUIT DESCRIPTION

In the capstan servo system, inputs from the ramp generator produce accurately controlled tape speeds through a velocity servo.

The ramp input to the capstan servo amplifier is summed with the tachometer output at the source of Q1. R20 is the tachometer summing resistor while the ramp summing resistor is located on the ramp generator. Error voltage is fed to the + input of operational amplifier IC1. Output from IC1 is applied to driver complementary amplifier Q2, Q3 which in turn drives the output amplifier Q4, Q5, Q6, Q7 to produce a dc voltage across the capstan motor. The motor then runs at a speed that produces a tachometer output equal to the ramp input, causing the tape to be driven at the proper speed.

Amplifier gain is set by R8 and R9 which provide negative feedback from the power stage to IC1.

Q9 is connected as an inverted amplifier controlled by an input from the LOAD switch and its associated flip-flop. This input, if high, causes Q9 to ground the summing function, thereby disabling the capstan drive. SERVO DISABLE high also disables Q1 by isolating its drain from the source.

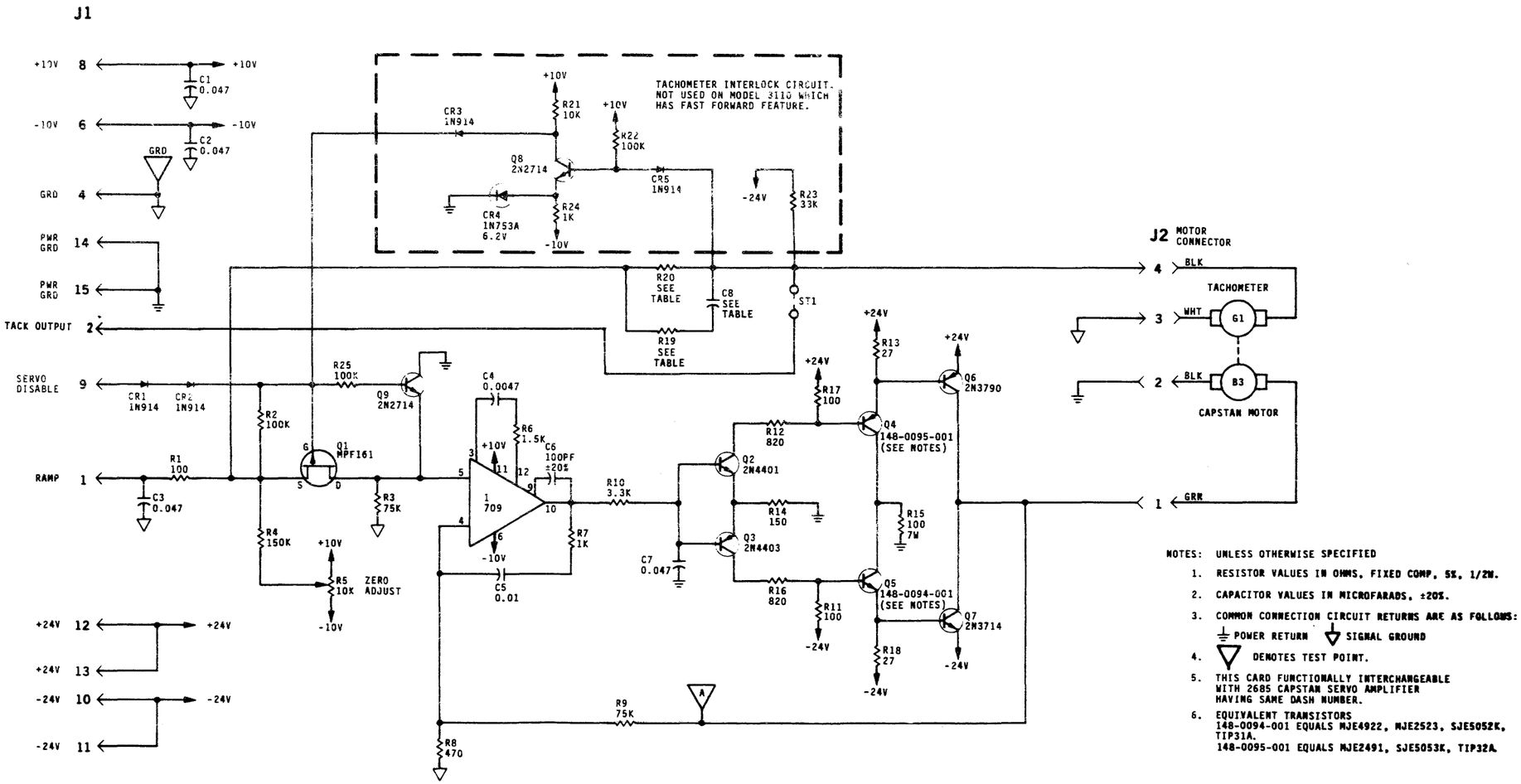
ADJUSTMENT PROCEDURE

An adjustment is provided to set capstan offset at zero. To adjust zero:

a. Connect oscilloscope to observe voltage at the amplifier output. A convenient point is at test point A.

b. With transport ON LINE and loaded but in a stopped condition, adjust R5 so that a straight-line trace is produced. Use 0.5v/cm scale on scope.

c. Observe that capstan does not rotate.



NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES IN OHMS, FIXED COMP, 5%, 1/2W.
2. CAPACITOR VALUES IN MICROFARADS, ±20%.
3. COMMON CONNECTION CIRCUIT RETURNS ARE AS FOLLOWS:
   ⏚ POWER RETURN ▽ SIGNAL GROUND
4. ▽ DENOTES TEST POINT.
5. THIS CARD FUNCTIONALLY INTERCHANGEABLE WITH 2685 CAPSTAN SERVO AMPLIFIER HAVING SAME DASH NUMBER.
6. EQUIVALENT TRANSISTORS
   148-0094-001 EQUALS MJE4922, MJE2523, SJE5052K, TIP31A.
   148-0095-001 EQUALS MJE2491, SJE5053K, TIP32A.

TYPE 3264 DASH NUMBERS

DASH NO.	001	002	003	004	101	201	202	203	204	301
R20	15K 1/8W,1%	15K 1/8W,1%		56.2K 1/8W,1%	6.81K 1/8W,1%	15K 1%	15K 1%		56.2K 1%	6.81K 1%
TACH. INTERLOCK CIRCUIT	OMIT	AS SHOWN		OMIT	OMIT	OMIT	USE		OMIT	OMIT
R19	OMIT	OMIT		OMIT	120K	OMIT	OMIT		OMIT	120K
C8	OMIT	OMIT		OMIT	STRAP	OMIT	OMIT		OMIT	STRAP
ST1	OMIT	OMIT		OMIT	OMIT	USE	USE		USE	USE

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Capstan Servo Amplifier, Type 3264
Schematic Diagram

TYPE 5181 CAPSTAN SERVO AMPLIFIER R

CIRCUIT DESCRIPTION

This module is used in recorders with synchronous running speeds of 25 ips, 37.5 ips or 45 ips. The Capstan Servo Amplifier is a part of a velocity servo system which produces accurately controlled capstan speeds with linear ramp-up and ramps-downs. In addition to driving the capstan motor this module includes circuitry to modify the capstan tachometer output. This MODIFIED TACHOMETER OUTPUT is used in conjunction with the corrective voltage supplied from the buffer arm magnetic position sensors to drive the reel motors.

Capstan Amplifier

The capstan servo amplifier portion of this module amplifies the linear output of the ramp generator module to drive the capstan motor. The output of the ramp generator, supplied at pin 1, is summed with the output of the capstan tachometer, supplied at pin 4, using summing resistors R11, R16 and R17. The summed voltage is supplied to the non-inverting input of operational amplifier IC3. The zero offset of IC3 is adjusted using potentiometer R19 to prevent capstan creep during standstill. FET Q2 disables the capstan amplifier if DISABLE at pin 9 goes true (supplied from the LOAD pushbutton). This occurs when the transport is not loaded or broken tape is detected. When the tape is properly loaded, Q2 will not ground ramp input and the output voltage of IC2 is supplied to IC3. The output of IC3 is supplied to complementary amplifier stages, including transistors Q3, Q4, Q5, Q6, Q7, and Q8. The output of the power stages energize the capstan motor, driving the tape at accurately controlled speeds.

Modified Tachometer Output

The Modified Tachometer Output signal is used in the High Speed Servo Preamplifier Type 4105 to control the reel servo response to capstan motion. In high speed transports the response of the reel servo to capstan motion would not be fast enough if only the outputs of the buffer arm position sensors were used to energize the reel motors. Using the MODIFIED TACHOMETER OUTPUT, the reel servo motors respond directly to capstan motion. It is necessary to modify the tachometer output, however, in order to reduce its effect in high speed rewind. The modification reduces the corrective voltage after the capstan speed has reached approximately 45 inches per second. The TACHOMETER voltage is modified by a pair of operational amplifiers, IC2 and IC1. The TACH signal is supplied to both amplifiers. At speeds of up to 45 ips, the output of IC2 increases linearly and is output at IC1-6 to generate the MODIFIED TACHOMETER OUTPUT. At approximately 45 ips, IC2 is saturated and IC1 then linearly reduces the MODIFIED TACHOMETER OUTPUT as the speed increases, reducing the effect of the capstan on the reel servos.

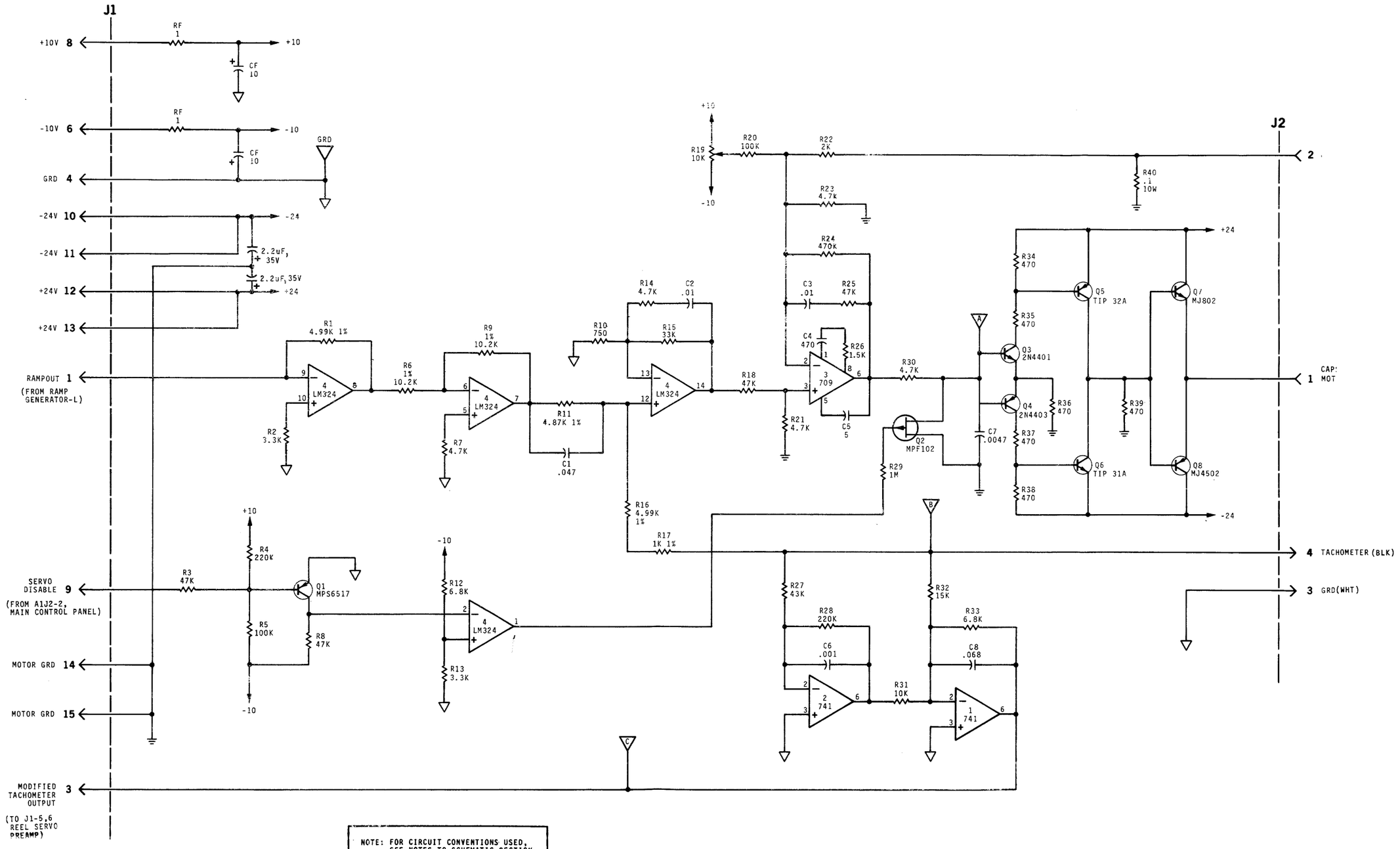
Capstan Servo Amplifier Adjustment

The capstan zero offset is adjusted as follows:

a. Connect an oscilloscope probe to monitor the voltage at test point A, measuring the output of the Capstan Servo Amplifier.

b. With transport ON LINE and loaded but in a stopped condition, adjust potentiometer R19 so that a straight-line trace is produced. Use 0.5 v/cm scale on scope.

c. Make certain the capstan does not rotate.



NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Capstan Servo Amplifier, Type 5181-001 , Schematic Diagram

REEL SERVO SYSTEM (TYPE 2683, 3191, 4210 PC BOARDS)

CIRCUIT DESCRIPTION

(Refer to Schematic 401-4210-001 for Type 4210 Magpot PCB)

Takeup and supply reel servos maintain tape tension at a constant value. Four main components are included: magpot position sensor, preamplifier, power amplifier, and reel motor. The 2683 Servo Preamplifier/3191 Servo Power Amplifier combination is usually employed in tape drives running at or below 25 ips. Two preamplifiers and servo amplifiers are used in the tape drive, one set per reel.

The magpot position sensor measures tape tension by the position of a spring loaded buffer arm. At the approximate center of the arc, sensor output is zero.

As the buffer arm moves off center, a positive or negative voltage is produced which is proportional to the error. The error voltage is fed through a damping network consisting of resistors R1, R2, R3, R5, and capacitors C1, C2, and C3. The voltage is then supplied to a low bias operational amplifier. The output of this amplifier is supplied to a complementary driver stage Q2, Q3.

The circuits described above are part of preamplifier 2683A. The Q2, Q3 outputs are wired to the servo power amplifiers mounted on heatsink assemblies. The power amplifier is a high-power complementary pair Q2, Q4 driven from emitter followers Q1, Q3. Feedback is provided to the differential amplifier by R5, R6, R7, R8 on the preamplifier to set system gain.

The reelmotor is connected to the power amplifier output. Relay contact K1-A shorts the motor armature when power is off. This provides dynamic braking and limits coasting in the event of power failure.

When power is on but the LOAD button has not been pressed, the disable input on pin 4 is +10 volts. The disable input causes Q4, an inverted amplifier, to conduct, grounding out the dc error input at R18. Servo output is now zero and the reel motors are at rest. A path for error rate signals is left open through C2, C3 which applies braking current to the motors when the buffer arms swing out as tape is removed from the machine.

TYPE 4105 SERVO PREAMPLIFIER

CIRCUIT DESCRIPTION

In most applications two of these PC boards are used in transport with synchronous running speeds of 37.5 inches per second; one for each reel motor. Each module amplifies the corrective voltage received from the respective buffer arm position sensor summed with the MODIFIED TACHOMETER OUTPUT voltage received from the High Speed Capstan Servo Amplifier Type 4181. The output of this card is supplied to the High Speed Servo Power Amplifier to energize the respective reel motor.

The corrective voltage from the magnetic buffer arm position sensor (magpot) is input at pin 9 of this module and is supplied to the inverting input of operational amplifier IC1. The MODIFIED TACHOMETER OUTPUT, MTC, is input at either pin 5 or 6, depending upon which reel motor is energized by this card. The MTC voltage provides a direct correlation between the motion of the capstan and the energizing of the reel motors. This is required in higher speed transports to prevent buffer arm bottoming, ensuring carefully controlled ramp-ups and ramp-downs. When capstan motion is first initiated, the MTC voltage is amplified by IC2 and is fed through the AC coupling of R16, C8 to the input of IC1. This provides an initial current surge to the motors even before the corrective voltage from the magpots would have any effect. The effect of this AC coupling is to start reel motor motion almost immediately, preventing lags and arm bottoming. Once motion is initiated the magpot corrective voltage is fed through IC1 and is summed with the amplified MTC voltage through DC coupling including R17, R19. R17 is a potentiometer which controls the effect of the MTC on the reel motion. This potentiometer is adjusted so as to reduce buffer arm travel, maximizing the response of the reel motors to the capstan motion and to the buffer arm position. The adjustment is described below.

The summed MTC and magpot voltages are fed through FET Q3, provided that DISABLE is false, to the inverting input of operational amplifier IC3. Two feedback loops control the amplification of the signal by IC3; one is provided from the output of the complementary stages on this module through diodes CR3 and CR4. The diodes are provided to counter the lag in the power amplifier response. The other feedback loop is supplied from the output of the High Speed Servo Power Amplifier Type 4111 at pin 11 of this module. The output of IC3 is then amplified by complementary stages consisting of transistors Q1 and Q2, whose outputs are supplied to the High Speed Servo Power Amplifier Type 4111, which in turn energizes the respective reel motor.

Whenever DISABLE goes true, indicating that the tape is not loaded or that broken tape has been detected, DISABLE high at input pin 4 of this module disables FETs Q3, Q4 to inhibit the operation of this module. This prevents reel motion when the tape is broken or not loaded.

Buffer Arm Adjustment

Potentiometer R17 is adjusted on this card to minimize buffer arm travel, preventing arm bottoming and overshooting. The adjustment procedure is as follows:

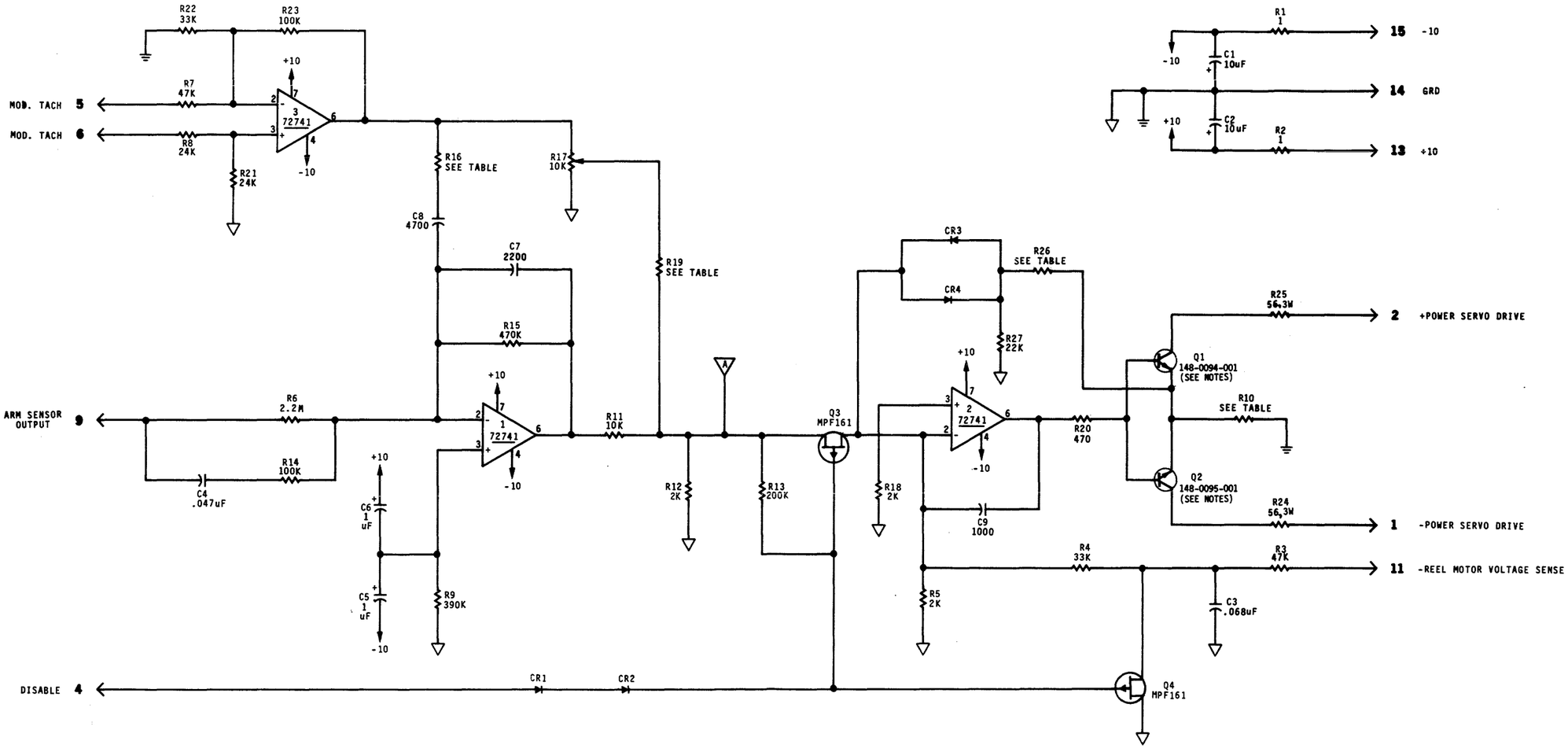
a. Load a full reel of tape on the supply reel.

b. With the transport off line, press the test panel TEST MODE pushbutton.

c. Press the FORWARD RUN and REVERSE RUN pushbuttons alternately, initiating synchronous forward and reverse tape motion.

d. Adjust potentiometer R17 on the supply Servo Preamplifier Type 4105 until the travel of the Supply buffer arm is at a minimum during the ramp-ups and ramp-downs.

e. Repeat the above steps for the takeup servo preamplifier.



NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

DASH NO.	-001E	-002C
R10	100,3W	56,3W
R16	1.0M	OMIT
R19	47K	OMIT
R26	36K	43K

NOTES: UNLESS OTHERWISE SPECIFIED
1. 148-0094-001 EQUALS MJE4922, MJE2523, SJE5052K, TIP31A.
148-0095-001 EQUALS MJE2491, SJE5053K, TIP32A.

Servo Preamplifier, Type 4105-001D, Schematic Diagram

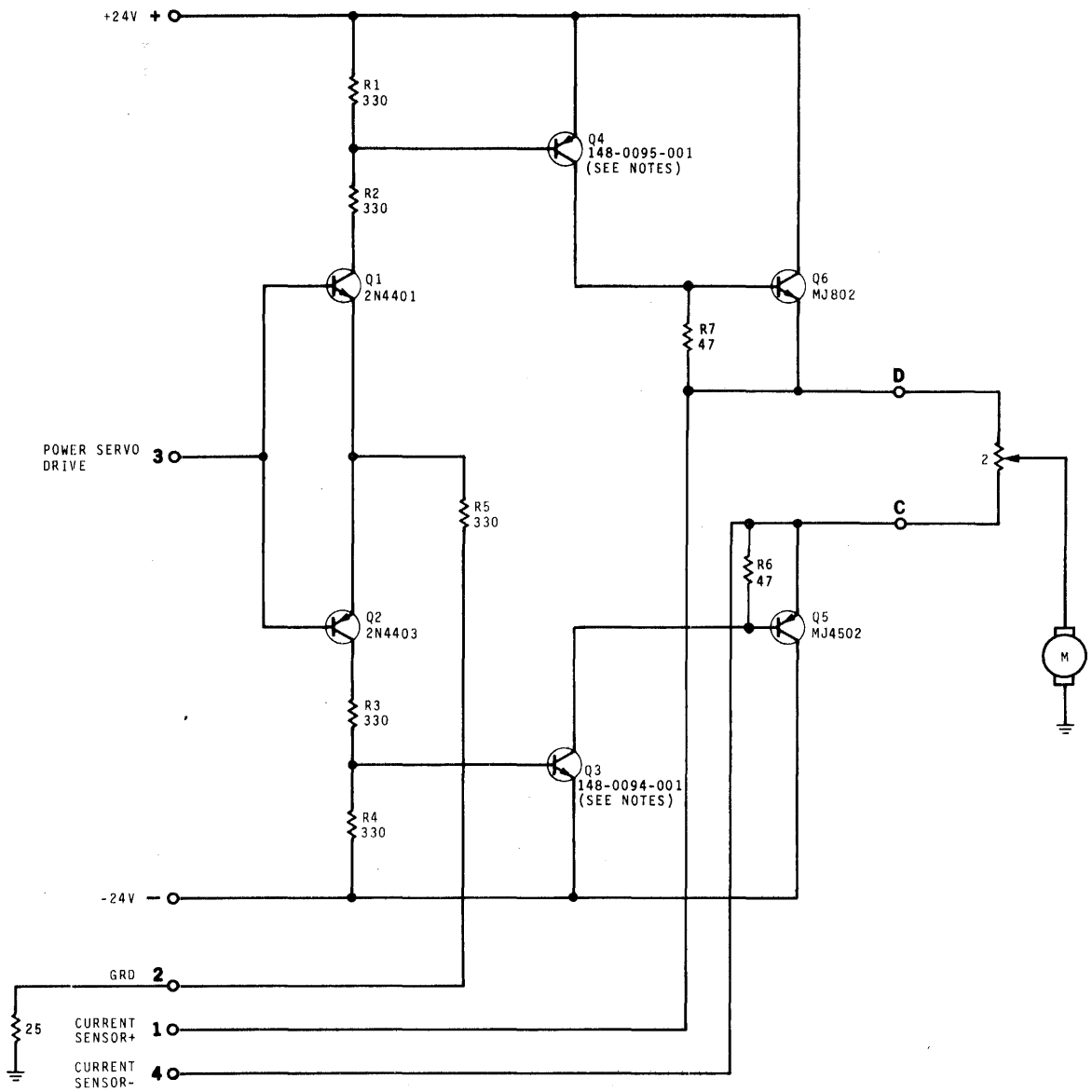
TYPE 4911 SERVO POWER AMPLIFIER

CIRCUIT DESCRIPTION

In normal applications, two of these modules are used in transports having synchronous running speeds of 45 ips; one module for each reel motor. This module amplifies the signal received from the High Speed Servo Preamplifier Type 4905, and supplies the power output of the respective reel motor.

The signal from the Servo Preamplifier, input at pin 3, is supplied to the base of drivers Q1 and Q2 which in turn activate power transistors Q6 and Q5 to drive the reel motors.

The output of the power stages is fed back through pins 1 and 4 (Current Sensor + and -) on this board to the High Speed Servo Preamplifier Type 4905 where it is used to control the amplification characteristics of the preamplifier.



NOTES: UNLESS OTHERWISE SPECIFIED
1. EQUIVALENT TRANSISTORS
148-0094-001 EQUALS MJE4922, MJE2523, SJE5052K, TIP31A.
148-0095-001 EQUALS MJE2491, SJE5053K, TIP32A.

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

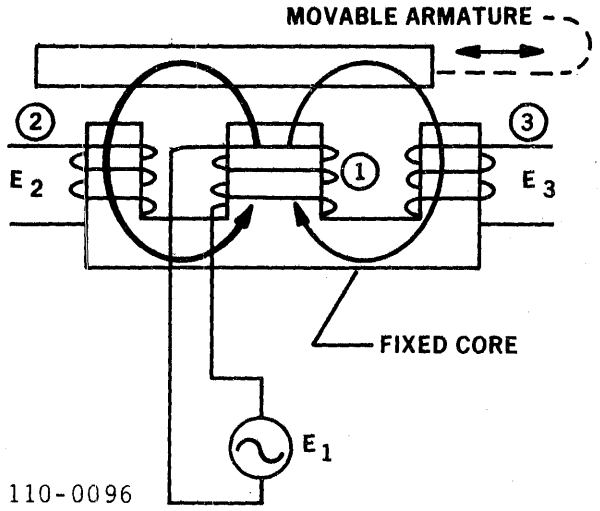
Model 9000, Servo Power Amplifier
Type 4911-001A
Schematic Diagram

TYPE 4210 MAGPOT TENSION ARM POSITION SENSOR

CIRCUIT DESCRIPTION

In the reel servo system it is necessary to produce an analog signal representing tension arm position. The signal must be zero at the nominal resting position of the tension arms and should linearly represent angular deviations from the center of arm travel by positive and negative voltages. A common method utilizes lamps, photocells, and a shutter to produce the required voltage. This method suffers from the mortality of lamps and the relatively slow response of photocells.

The magpot operates as a differential transformer, an example of which is shown below.



Magnetic flux produced by current in winding (1) will produce voltages E_2 and E_3 in the other windings. If the armature is symmetrically located with respect to (2) and (3), flux in the two windings will be equal, and since they have the same number of turns, $E_2 = E_3$. If the armature is displaced as shown, $E_2 > E_3$ since the flux coupling E_3 has been reduced. Displacement in the opposite direction produces $E_3 > E_2$. Displacement from center then is represented by $E_0 = E_2 - E_3$. In the configuration shown this relation is linear only for very small displacements because area relations are not linear.

The magpot is an adaptation of the above scheme in that there are three windings on a magnetic core. The core in this case is a ferrite pot core while the armature is half a pot core. The windings (2) and (3) are around legs of the pot core while (1) is around the center portion common to the two legs. Winding (1) is energized by a high frequency oscillator (approximately 200 kHz). The magpot is in balance and $E_2 = E_3$ when the armature couples equally to the two legs. As the armature is rotated the area available for magnetic flux increases linearly for one leg and decreases linearly for the other leg. Thus the difference in induced voltages is a linear representation of angular movement.

The 200 kHz oscillator is a Hartley circuit comprising Q1, C1, C2, R1, R2. It produces a 40 volt ptp sine wave across the primary winding.

The two secondary windings are connected in series and their voltages are rectified by CR1, CR2. The two rectified voltages are subtracted and referenced to ground. Thus the input to IC1 operational amplifier is a dc voltage equal to $E_2 - E_3$. This voltage is null when $E_2 = E_3$ and is positive or negative depending upon which is larger. Secondary voltages induced are at all times large enough to overcome the diode drops in CR1, CR2.

DC output of the rectifier circuit is amplified by IC1 and fed from the output to the appropriate reel servo amplifier.

Voltage output for a given angular deflection depends upon coupling between the fixed core and armature at that setting. The gain relations are such that a spacing of 0.030 inch between core and armature results in ±5v output for full arm travel. Spacing is established by two 0.015 inch thick plastic spacer washers on the shaft.

Adjustment Procedure

If adjustment should be required:

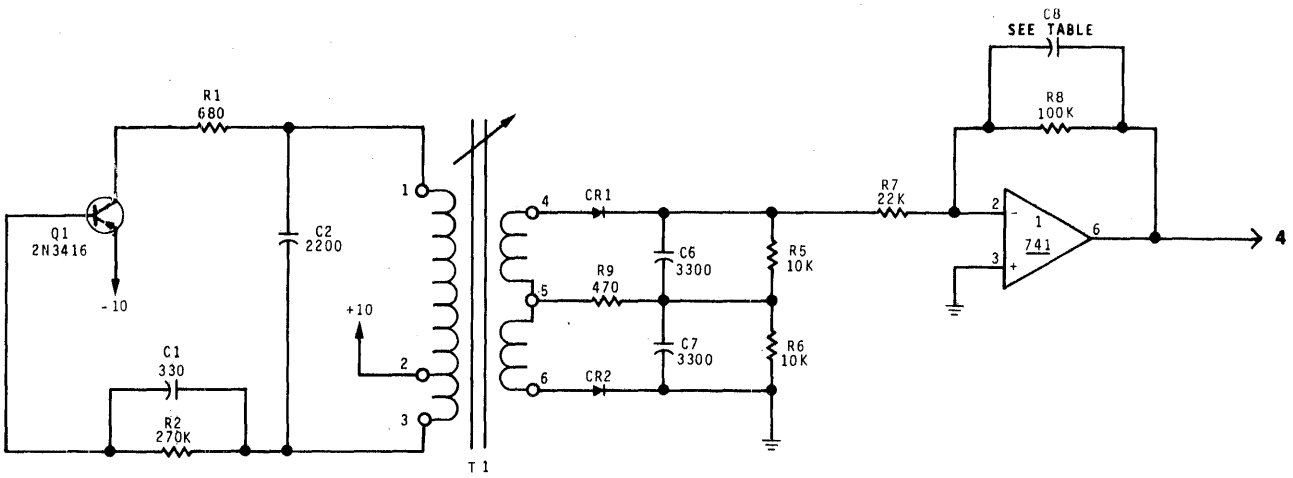
1. Remove tape from machine.
2. Place a short length of tape in front of broken tape sensor.
3. Turn power on, press LOAD. Reels will rotate.
4. Hold tension arm in approximate center of arc. Reel rotation should stop.
5. If reel continues to rotate loosen setscrew holding the armature to the tension arm shaft.

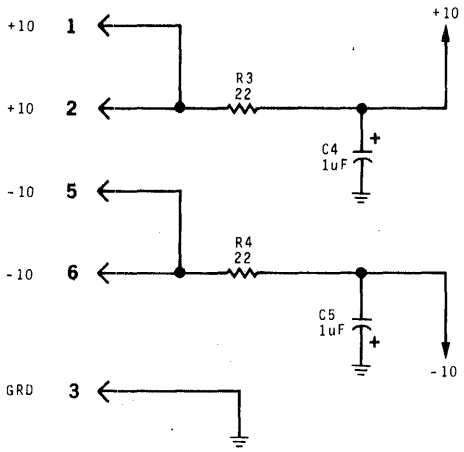
6. Rotate armature until reel hub motion ceases. Press firmly against the fixed core to maintain core to armature spacing.

7. Tighten setscrew.

8. Move arm to limits of travel and observe directions of reel hub rotation. There are two null positions 180^{o} apart. The sense of the output is reversed for one null causing hub rotation to be wrong. If this null has been chosen, loosen setscrew, rotate armature 180^{o}, and repeat.

9. Check output at pin 4 using a voltmeter. Total output swing should be between 10 and 12 volts (±5v nominal).





UNLESS OTHERWISE SPECIFIED:
- RESISTOR VALUES ARE IN OHMS ±5%
- CAPACITOR VALUES ARE IN PICOFARADS ±5%
- NPN TRANSISTORS ARE 2N2714
- PNP TRANSISTORS ARE MPS6517
- DIODES ARE 1N914
- IC ARE TTL, 7400 SERIES
-- NUMBER IN LOGIC SYMBOL IS REFERENCE DESIGNATOR, UNDERLINED NUMBER IS IC TYPE. (IF 7400 SERIES, 74 IS OMITTED)
-- IC PIN 7 IS CONNECTED TO GROUND
-- IC PIN 14 IS CONNECTED TO +5V
-- UNUSED INPUTS OF IC MAY BE TIED TOGETHER OR TO +5V THROUGH RESISTOR (+V)
- (*) DENOTES FACTORY SELECTED VALUE. TYPICAL VALUE IS SHOWN
- FILTER CAPACITORS ARE NOT SHOWN BUT ARE IDENTIFIED BY CF ON PC BOARD

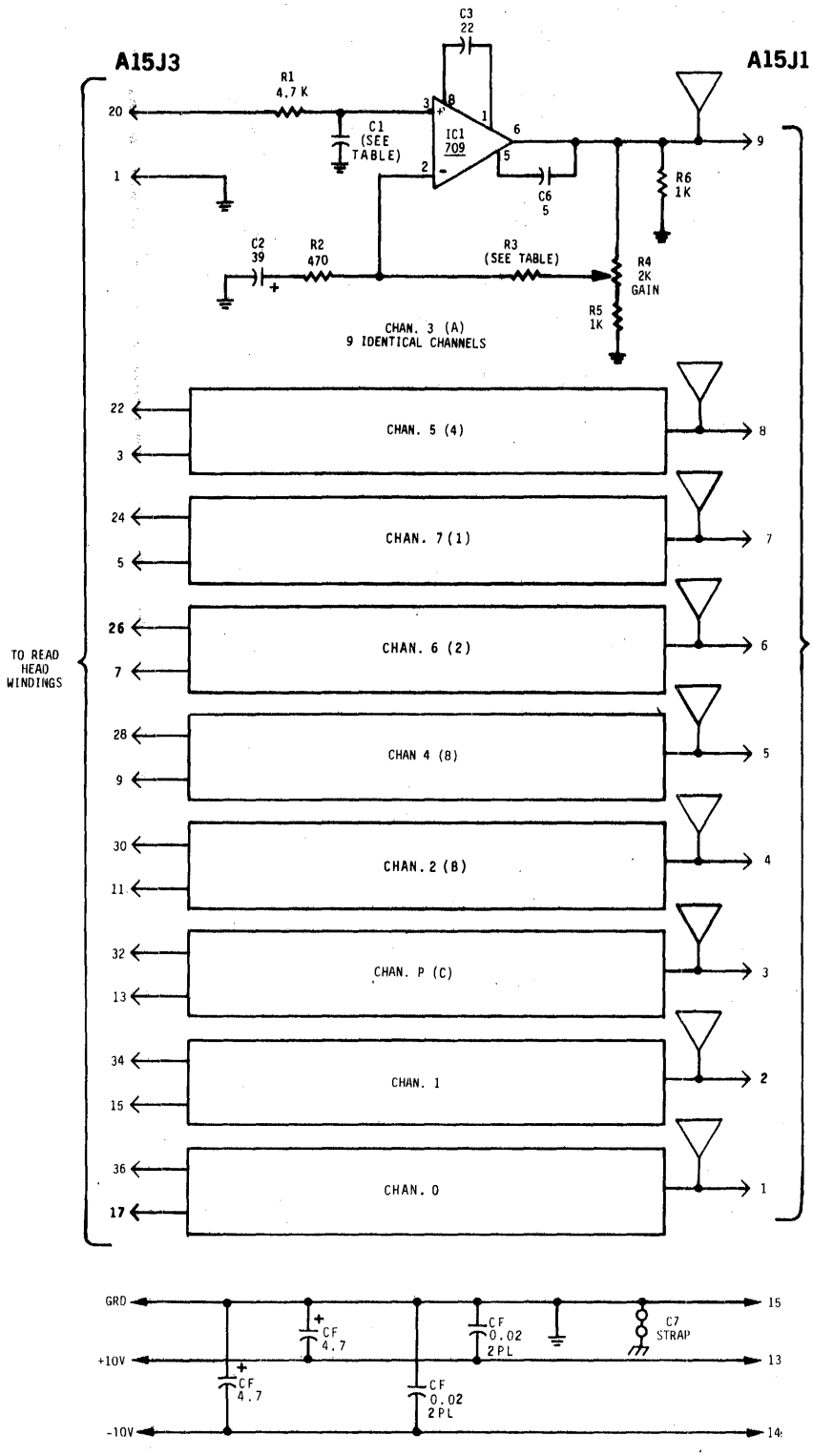
DASH NO.	MODELS	C8
-001C	ALL OTHERS	.033uF
-002A	9800/9801	.01uF

Magpot,
Type 4210
Schematic Diagram

TYPE 3935 READ PREAMPLIFIER

CIRCUIT DESCRIPTION

This module contains nine identical high gain amplifier stages which amplify the input signal from the read head and supply it to the read amplifier cards. Each amplifier stage consists of an operational amplifier with a negative feedback loop. The gain of the amplifier can be adjusted using the potentiometer in the loop, and should be approximately 9 volts peak to peak single density and 8 volts peak to peak dual density. Each gain has a tolerance of +/-0.5v.



NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES IN OHMS, FIXED COMP 5%, ¼W
2. CAPACITOR VALUES IN MICROFARADS
3. ▽ DENOTES TEST POINT
4. UNUSED IC INPUTS MAY BE TIED TOGETHER OR TO +5V
5. DASH 103 SAME AS 003 EXCEPT OMIT IC1 (709) @ CHAN 0 & 1

DASH NUMBER		-005M	-004M	-001M	-002M	-003M	-006M
SPEED	9 TRACK (IPS)	10-15	15-20	20-30	30-40	40-60	
	7 TRACK (IPS)		10-15	15-20	20-30	30-40	40-60
R3 (OHMS)		300K	220K	150K	110K	82K	75K
C1 (PF)		1000	680	470	330	270	180

Read Preamplifier, Type 3935
Schematic Diagram

TYPE 3845 DELAY TIMING MODULE

CIRCUIT DESCRIPTION

This module contains the crystal oscillator and dividing network which produce the synchronous clocks used by the read and write electronics. In addition, this module includes the read data strobe generation network, a read skew delay counter, the gap detect network, and the SELECT 2 circuitry. These functions are discussed in detail below.

CRYSTAL CONTROLLED OSCILLATOR AND DIVIDING NETWORK

The oscillator consists of crystal Y1 used in a feedback loop between two inverter sections of IC5. The oscillator output is supplied to a dividing network which provides the synchronous clocks used in the transport. The dividing network includes divide by 2 and 8 counter IC2, flip-flops IC1, and divide by 16 counter IC4. The clocks generated by the network are a function of tape speed and a series of switches is provided to divide the master oscillator frequency according to the tape speed of the particular transport. The switch positions for the different tape speeds are tabulated on the schematic diagram. The clocks output by the network are f_1, a square wave at 32 times the character frequency, and f_r, a square wave at the character frequency.

SKEW CHECK COUNTER AND READ DATA STROBE GENERATION

The wire-OR'd peak pulses supplied from the read amplifier stages are input at pin R of this module, and after being inverted by IC14 are supplied to NAND gate IC14-10. At this time the Q output of flip-flop IC15-3 is high, enabling IC14-9, and the peak pulses are gated through IC14-8 to the direct-clear input of flip-flop IC15-13. During each data character the pulse of the leading channel direct-clears flip-flop IC15-13, setting the $\overline{Q}$ output high to enable the skew counter, divide-by-16 IC16. The counter is clocked by f_1 at 32 times the data frequency. During a test mode, TEST MODE true at input pin H (from the pushbutton control module) direct-sets the skew counter to the count of 11. The counter then counts from 11 to 16, at which point its Q_d output toggles flip-flop IC15-12, locking itself. The skew tolerance is restricted to the period of the count; any peak coming in after the skew counter has set flip-flop IC15 would cause a skew indication, as explained below. Once IC15 flip-flop has been toggled to the set state, its $\overline{Q}$ output goes low and toggles flip-flop IC12-12. The $\overline{Q}$ output of IC12-2 goes low, is inverted by IC10-12 and supplies DATA TRANSFER true to the read amplifier module, shifting the data to the output buffer on those modules. The next f_1 pulse after DATA TRANSFER toggles the second IC12 flip-flop to the set state; the $\overline{Q}$ output of IC12-6 goes low, is inverted twice by two IC10 inverters and is output as the READ DATA STROBE RDS at output pin A to the interface. IC12-6 low also direct-clears the first IC12 flip-flop; consequently the next f_1 pulse also toggles the second IC12 flip-flop to the cleared state and terminates the data strobe. Should the skew tolerance be exceeded and a pulse arrive after flip-flop IC15 has been set, the lagging pulse will direct-clear IC15-13 again and enable NAND gate IC13-12. The gate is activated when IC12-5 goes high and fires the skew one-shot IC11-4, illuminating the skew lamp on the test panel. During a normal write mode the skew tolerance is increased, as WRITE READY true and TEST MODE false activate NAND gate IC14-6 and direct-set the skew counter to the count of four. This increases the skew tolerance from the five counts used during the test mode to 12 counts. During the read only mode both WRDY and TEST MODE are false, and the skew tolerance count is increased to 16, or half a character space.

GAP DETECT COUNTER

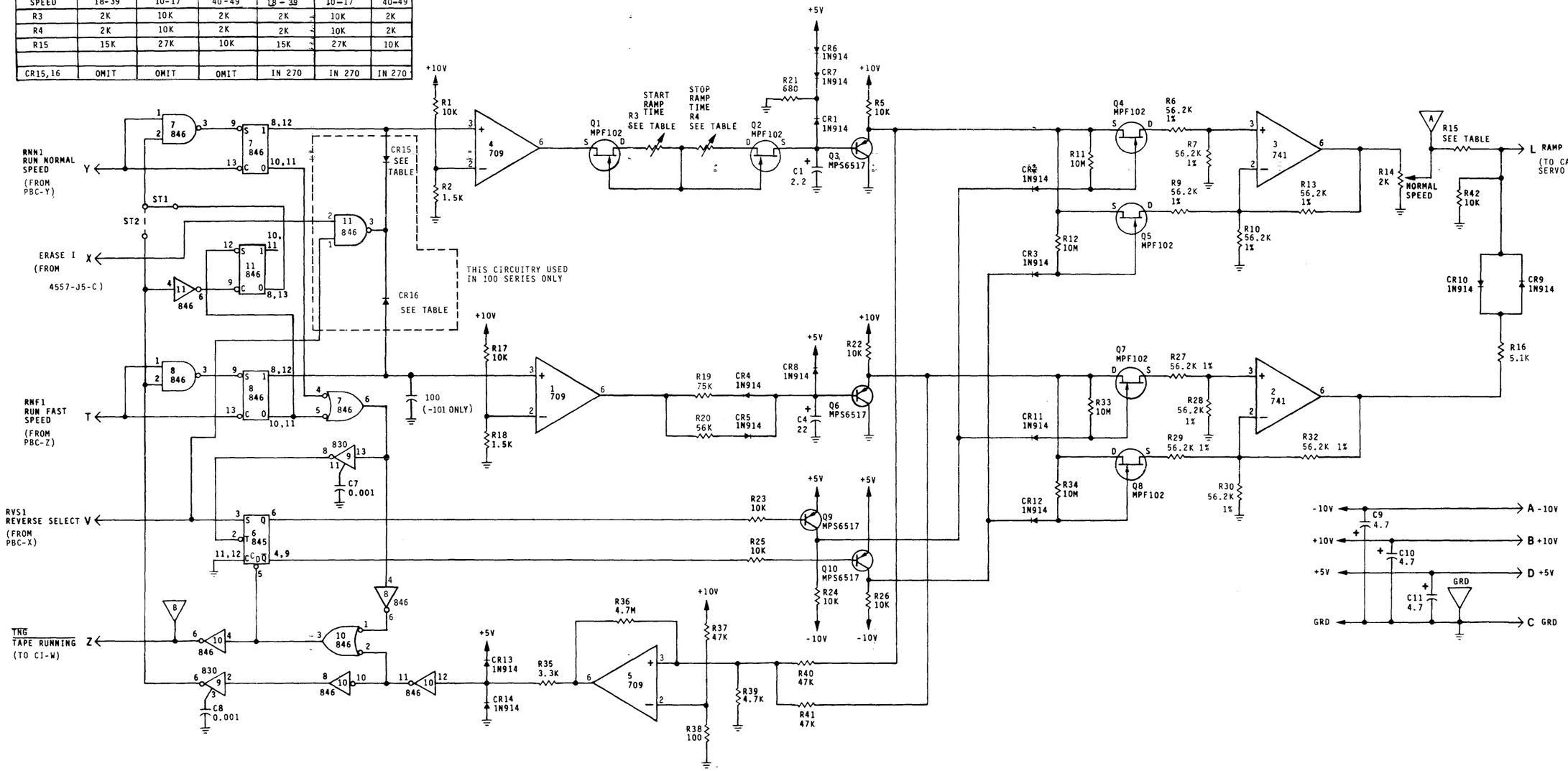
The gap detect counter consists of two divide-by-16 counters in tandem: IC6 and IC7. It is clocked by f_1 at 32 times the data frequency. After each data pulse flip-flop IC15-13 is direct-cleared, its $\overline{Q}$ output goes high and resets the gap counter. After the skew delay IC15 is set again and the gap counter is enabled. Following the last data character of a record, the gap counter is not reset immediately but keeps counting. When it reaches the count of 32, one character time after the last data character of the block, the Q_b output of IC7 activates NAND gate IC9-13. IC9-11 goes low and direct-clears flip-flop IC8-13. The Q output of the flip-flop in turn direct-sets the gap detect flip-flop IC15-10, generating GAP DETECT true at output pin H to the interface, provided that the transport is selected and on line (SLT1 true). The Q output of IC8-3 low also activates NOR gate IC9-1, keeping the counter enabled and counting while the check characters are being read; otherwise the LRC and CRC characters will have reset the gap counter, signifying end of gap. When the gap counter reaches

the count of 256 it toggles flip-flop IC8-9, enabling NAND gate IC9-10. Thirty-two counts later, equivalent to the tenth character space of the interrecord gap, IC9-8 goes low and toggles flip-flop IC8-12 to the set state. The Q output of the flip-flop goes high and activates NAND gate IC9-4, so that the gap counter will clear when the next data character is detected (IC15-2 high).

SELECT 2 GENERATION

SELECT 2 is used to enable the output data gates on the read amplifier modules. SLT2 is generated by combining BUSY $\overline{BSY}$ false, LOAD POINT LP false, SELECT 1 SLT1 true, and RUN NORMAL $\overline{RNN}$ true. Once $\overline{RNN}$ goes true, initiating synchronous tape motion, a delay count consisting of divide-by-16 counters IC18 and IC19 is enabled. The counters are advanced by data frequency clock f_r. On the count of 128 the Q_d output of IC19 goes high and activates NAND gate IC20 if all the requirements mentioned above are met. IC20-8 goes low, is inverted by IC20-6, and generates SLT2 true at output pin L to the read amplifiers. The purpose of the SLT2 delay is to disable the output data gates during the tape ramp-up. When IC19-11 goes high IC17-8 goes low preventing further clocks to the counter. The counter is reset to the count of zero when RUN NORMAL $\overline{RNN}$ goes high.

DASH NO.	001E	002E	010F	101B	102A	110A
SPEED	18-39	10-17	40-49	18-39	10-17	40-49
R3	2K	10K	2K	2K	10K	2K
R4	2K	10K	2K	2K	10K	2K
R15	15K	27K	10K	15K	27K	10K
CR15,16	OMIT	OMIT	OMIT	IN 270	IN 270	IN 270



*Ramp Generator, Type **3645***
Schematic Diagram

TYPE 4118 DELAY TIMING MODULE

CIRCUIT DESCRIPTION

(Refer to 7 Track Read Control Logic Schematic 401-9000-005)

This module contains the crystal oscillator and dividing network which produce the synchronous clocks used by the read and write electronics. In addition, this module includes the read data strobe generation network, a read skew check counter, the gap detect network, and the SELECT 2 circuitry. These functions are discussed in detail below.

CRYSTAL CONTROLLED OSCILLATOR AND DIVIDING NETWORK

The oscillator consists of crystal Y1 used in a feedback loop between two inverter sections of IC11. The oscillator output is supplied to a dividing network which provides the synchronous clocks used in the transport. The dividing network includes divide by 2 and 8 counter IC3, and divide by 16 counter IC12. The clocks generated by the network are a function of tape speed and a series of switches is provided to divide the master oscillator frequency according to the tape speed of the particular transport. The switch positions for the different tape speeds are tabulated on the schematic diagram. The clocks output by the network are f_1, a square wave at 32 times the character frequency, and f_r, a square wave at the character frequency.

SKEW CHECK COUNTER AND READ DATA STROBE GENERATION

The wire-OR'd peak pulses supplied from the read amplifier stages are input at pin R of this module. After being inverted by IC15 they are supplied to IC15-10. At this time the Q output of flip-flop IC16-3 is high, enabling IC15-9, and the peak pulses are gated through IC15-8 to the direct-clear input of flip-flop IC16-13. During each data character the pulse of the leading channel direct-clears flip-flop IC16-13, setting the $\overline{Q}$ output high to enable the skew counter, divide-by-16 IC17. The counter is clocked by f_1 at 32 times the data frequency. During a test mode, TEST MODE true at input pin H (from the pushbutton control module) direct-sets skew counter IC17 to the count of 11. The counter then counts from 11 to 16, at which point its Q_d output toggles flip-flop IC16-12, locking itself. The skew tolerance is restricted to the period of the count; any peak coming in after the skew counter has set flip-flop IC16 would cause a skew indication, as explained below. Once the IC16 flip-flop has been toggled to the set state, its $\overline{Q}$ output goes low and toggles flip-flop IC14-12. The Q output at IC14-2 goes low, is inverted by IC12-12 and supplies DATA TRANSFER true to the read amplifier module, shifting the data to the output buffer on those modules. The next f_1 pulse after DATA TRANSFER toggles the second IC14 flip-flop to the set state; the $\overline{Q}$ output of IC14-6 goes low, is inverted twice by two IC12 inverters and is output as the READ DATA STROBE RDS at output pin A to the interface. IC14-6 low also direct-clears the first IC14 flip-flop; consequently the next f_1 pulse also toggles the second IC14 flip-flop to the cleared state and terminates the data strobe. Should the skew tolerance be exceeded and a pulse arrive after flip-flop IC16 has been set, the lagging pulse will direct-clear IC16-13 again. The gate is activated when IC14-5 goes high and fires the skew one-shot IC11-4, illuminating the skew lamp on the test panel. During a normal write mode the skew tolerance is increased, as WRITE READY true and TEST MODE false activate NAND gate IC15-6 and direct-set the skew counter to the count of four. This increases the skew tolerance from the five counts used during the test mode to 12 counts. During the read only mode both WRDY and TEST MODE are false, and the skew tolerance count is increased to 16, or half a character space.

GAP DETECT COUNTER

The gap detect counter consists of two divide-by-16 counters in tandem: IC8 and IC9. It is clocked by f_1 at 32 times the data frequency. After each data pulse flip-flop IC16-13 is direct-cleared, its $\overline{Q}$ output goes high and resets the gap counter. The skew delay IC16 is reset and the gap counter is enabled. Following the last data character of a record, the gap counter is not reset immediately but keeps counting. When it reaches the count of 32, one character time after the last data character of the block, the Q_b output of IC9 activates NAND gate IC11-13. IC11-11 goes low and direct-clears flip-flop IC10-13. The Q output of the flip-flop in turn direct-clears the gap detect flip-flop IC16-10, generating GAP DETECT true at output pin H to the interface, provided that the transport is selected and on line (SLT1 true). The Q output of IC10-3 low also activates NOR gate IC18-10, keeping the counter enabled and counting while the check characters are being read. Otherwise the LRC and CRC characters will have reset the gap counter, signifying end of gap. When the gap counter reaches

the count of 256 it toggles flip-flop IC10-9, enabling NAND gate IC11-3. Sixty-four counts later, equivalent to the tenth character space of the interrecord gap, IC10-8 is activated and toggles flip-flop IC12-12 to the set state. The Q output of the flip-flop goes high and activates NAND gate IC18-4, clearing the gap counter, and keeping it cleared until the first character of the next block is read.

SELECT 2 GENERATION

SLT2 Delay disables the output data gates during tape ramp-up. SELECT 2 is used to enable the output data gates on the read amplifier modules. SLT2 is generated by combining BUSY $\overline{\text{BSY}}$ false, LOAD POINT LP false, SELECT 1 SLT1 true, and RUN NORMAL $\overline{\text{RNN}}$ true. Once $\overline{\text{RNN}}$ goes true, initiating synchronous tape motion, a delay counter consisting of divide-by-16 counter IC20 and IC21 is enabled. The counter is advanced by data frequency clock f_r. On the count of 128 the Q_d output of IC21 goes high and activates NAND gate IC22 if all the requirements mentioned above are met. IC22-8 goes low, is inverted by IC12-6, and generates SLT2 true at output pin L to the read amplifiers. The purpose of the SLT2 delay is to disable the output data gates during the tape ramp-up.

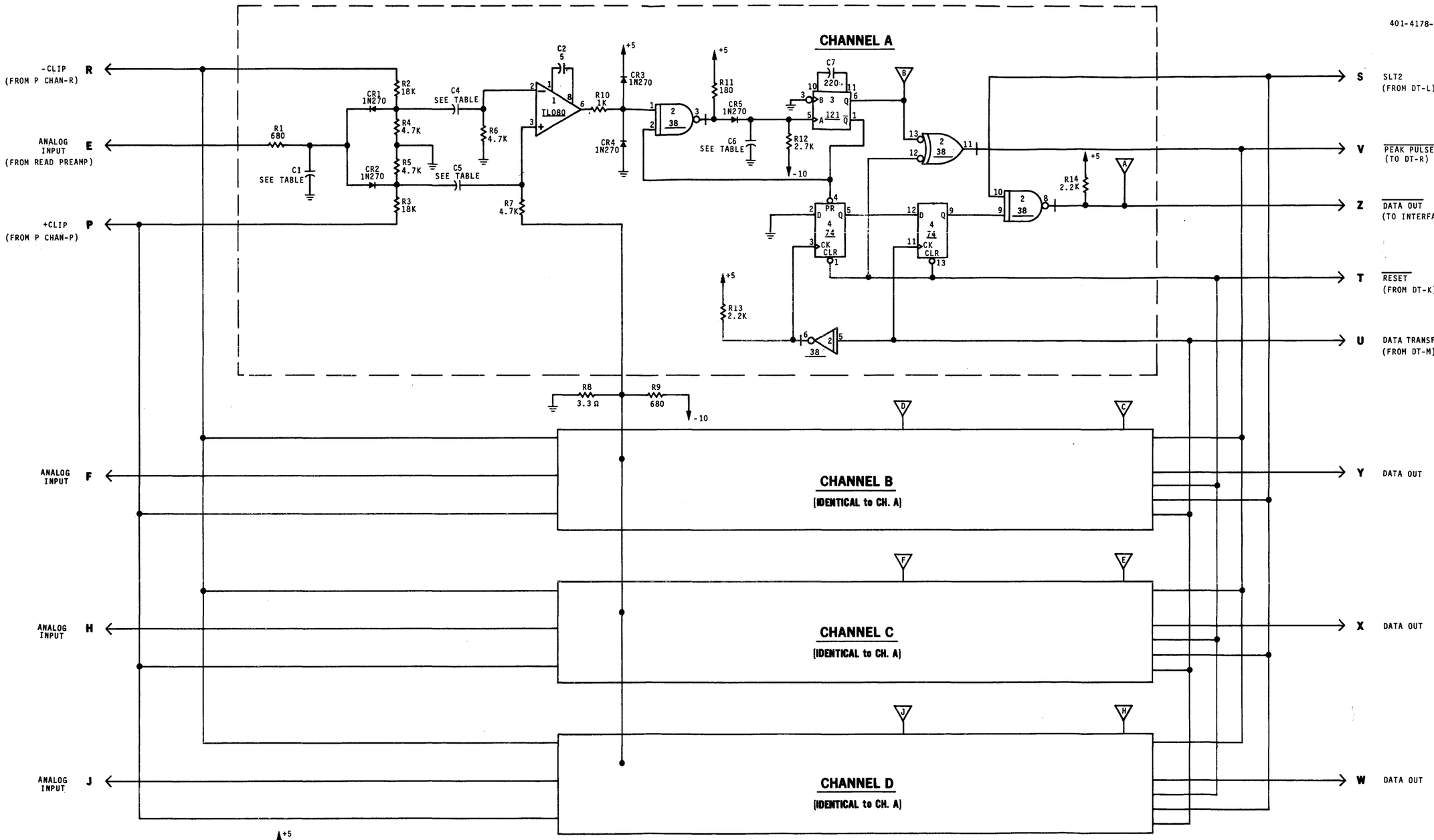
TYPE 4178 QUAD READ AMPLIFIER
CIRCUIT DESCRIPTION

Quad Read Amplifier Type 4178 accepts amplified head signals from the head preamplifier module and supplies decoded and deskewed data outputs to the interface. Each module contains four amplifier stages, and each recorder contains two of these modules. The channel P amplifier stage is located on Read Amplifier/Clipping Control module. The operation of the channel A amplifier stage is explained in the following paragraphs. The other amplifier stages operate identically.

The amplified analog signal is supplied from the read preamplifier at input pin E. The signal is filtered through R1, C1; the negative half waves are routed through diode CR1 while the positive half waves are routed through CR2. CR1 and CR2 are back biased respectively by the negative and positive clipping levels, supplied from the Read Amplifier/Clipping Control Module, to eliminate spurious baseline pulses. The negative half waves are then differentiated by C4 and R6 and are input at the inverting input of operational amplifier IC1. At the leading edge of the negative analog half wave the differentiated output of C4 and R6 swings negative, crossing zero at the peak of the analog signal and then going positive until the trailing edge of the analog signal. Normally the op amp output is low, since the noninverting input of IC1 is negatively biased through R7 and R9. When the leading edge of the differentiated signal exceeds the input threshold, the output of the amplifier swings positive. The amplifier output returns to 0v at the zero crossover of the differentiated signal, corresponding to the peak of the input analog signal. A similar transition occurs for the positive half wave, since it is input at the noninverting input of the amplifier. Consequently the amplifier output goes high and returns low for each 1 character, with the negative-going transition occurring at the analog peak. The output of the amplifier is limited by diodes CR3 and CR4 and is inverted by NAND gate IC2-3. IC2-3 output is supplied to a filtering network consisting of C6, R11, R12, and CR5, whose output is in turn supplied to the Schmitt trigger input of one-shot IC3. The output of IC2-3 is normally high, and the voltage at the input of IC3-5 is at 3.3v. When the output of IC1 swings positive, IC2-3 goes low and capacitor C6 discharges through R12 with a slow time constant, approximately 5 μsec at 25 ips. The voltage is clamped at 0v by diode CR5. When the output of IC1 goes low again at the peak of the analog input, IC2-3 goes high and C6 charges with a much faster time constant, approximately 300 nsec. When C6 charges up to 1.8v, one-shot IC3 triggers, generating a 300 nsec pulse. The $\overline{Q}$ output of the one-shot is connected back to IC2-2, disabling the gate and preventing the one-shot from being retriggered by spurious pulses on the input.

The positive pulse generated by the Q output of IC3 is inverted by IC2-11 and is output as $\overline{\text{PULSE OUT}}$ at pin V. The pulses of all the amplifier stages are wire-OR'd and supplied to the Delay Timing module where they are used for read deskewing and read data strobe generation. The $\overline{Q}$ output of one-shot IC3 direct-sets flip-flop IC4-4, the data storage register. The Q output of IC4-5 sets the D input of the output register IC4-12 high. A skew delay time is provided for all channels to be read after the leading data pulse is detected. DATA TRANSFER (supplied from the Delay Timing module) toggles the output register flip-flops of all channels simultaneously after the allowed skew delay time, outputing the deskewed, decoded data to NAND gate IC2-9 and, on its trailing edge, clears the first stage of IC4. The gate is enabled by SELECT 2 true, supplied from the Delay Timing module at input pin S. IC2-8 supplies the output data at pin Z to the interface. The length of the skew delay time is varied depending on the operation being performed. This is described in the Delay Timing module circuit description.

401-4178-001F



DASH NO.	-004	-005C	-001B	-002B	-003B
FIRST USED	9000	9000	9000	9000	9000
SPEED IPS	10-14.99	15-19.99	20-29.99	30-39.99	40-49.99
C1	3900	3000	2200	1500	1000
C4,C5	1000	680	470	330	270
C6	.022	.015	.01	6800	4700

Quad Read Amp, Type 4178, Schematic Diagram

TYPE 4179 READ AMPLIFIER CLIPPING CONTROL

CIRCUIT DESCRIPTION

This module contains the P channel read amplifier stages and the read amplifier clipping level control. The operation of the P channel amplifier is explained in the circuit description of the Quad Read Amplifier module, and the read amplifier clipping level control is explained below.

The read amplifier clipping control provides four clipping levels to the read amplifier: normal, low, high, and very high. When an error is detected during a read operation the transport may be commanded by the tape control unit to backspace over the erroneous block to reread it. The clipping level is kept at a normal level during the first reread. If a second reread is commanded, the clipping level is switched from normal to a lower clipping level, to compensate for a possible partial dropout. If a third reread is initiated, the clipping level is switched to a higher than normal level to eliminate possible baseline noise spikes. During a read after write operation the normal and high clipping levels are combined to supply a still higher clipping level which is not used during a read operation. The switching of the clipping levels is explained in detail below.

The initial state of the circuitry will be both IC10 flip-flops set and both IC11 flip-flops clear. This is established by BUSY $\overline{\text{BSY}}$ at pin Y true when tape is initially loaded or rewound. Since the first command from load point is always a run forward command, RUN NORMAL $\overline{\text{RNN}}$ at pin H true and REVERSE SELECT $\overline{\text{RVSI}}$ at pin W false cause IC8-8 to be low clearing IC9 flip-flop. The IC10 flip-flops remain in the set state when clocked by IC9-3 high. The circuitry remains in the states just described until a reverse command is given to the tape unit. When $\overline{\text{RNN}}$ and $\overline{\text{RVSI}}$ are true IC8-6 goes low direct-clearing the IC10 flip-flops which causes IC10-8 to go high removing the direct-clear from the IC11 counter flip-flops. Also IC8-6 low sets IC9 flip-flop which makes IC9-6 low; IC11-12 toggles causing IC11-3 to go high putting the counter in the "01" state. The clipping level does not change because the IC12, IC13 gating described in the next paragraph establishes the same clipping level. The circuitry will now remain in this state until a forward command is given. The next forward command causes IC8-8 to go low clearing IC9 flip-flop and toggling IC10-5 high. At this point two things could happen: The tape unit will be commanded to go forward to continue reading the next data block, or to backspace if the interface decides to reread the data block. If the tape unit is commanded to go forward to continue reading, then IC8-8 low makes IC9-3 high causing IC10-8 to go low which direct-clears the IC11 counter to its initial state. If instead the tape unit is commanded to go in reverse IC11-12 goes low toggling the IC11 counter to its next state. This establishes the next clipping level in the sequence. The IC10 flip-flops are cleared as described above. The IC11 counter will continue to toggle every time the tape unit is commanded to backspace after being commanded to go forward once. Two forward commands in succession will reset the IC11 counter by setting IC10-8 low, and reading continues at the normal clipping level.

The clipping levels established by the IC11 counter through IC12 and IC13 are as follows: (a) 00 and 01 cause IC13-6 and IC13-11 to be low and IC13-3 to be high establishing the normal read clipping level; (b) 10 causes IC13-6 and IC13-3 to be low and IC13-11 to be high establishing the low clipping level; (c) 11 causes IC13-3 and IC13-11 to be low and IC13-6 to be high establishing the high read clipping level.

During a read after write operation WRITE READY at input pin J is inverted by IC7-12 and disables the automatic clipping level control by direct-setting IC10 flip-flops, keeping the IC11 counter direct-cleared. At the same time WRDY true activates NOR gate IC13-4, enabling the higher clipping level, while the Q output of IC11-5 low enables the normal clipping level. Thus the normal and high clipping levels are combined to generate a still higher clipping level used during read after write only.

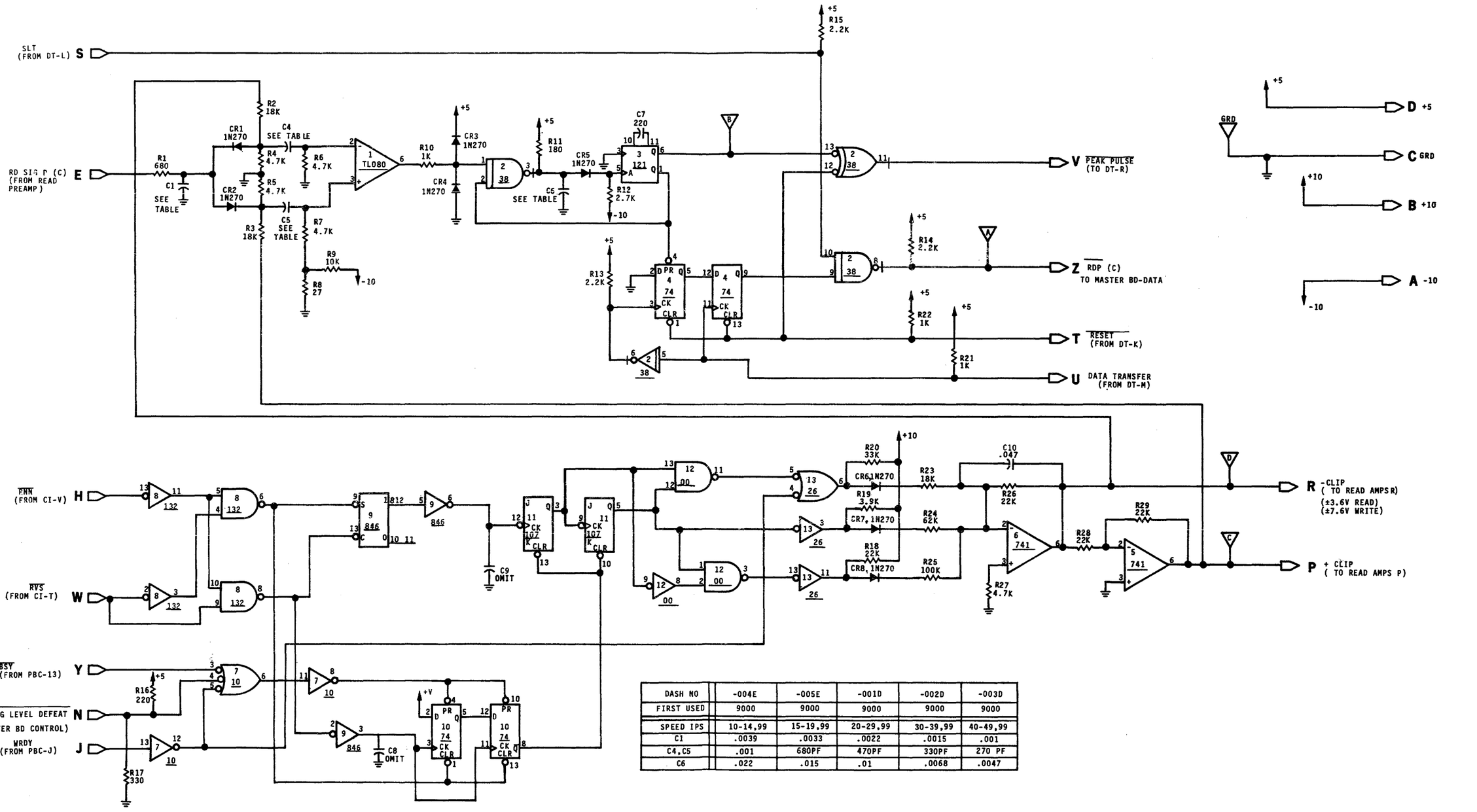
The automatic clipping level control is also disabled when the interface supplies AUTO DISABLE true at input pin N, or when BUSY $\overline{\text{BSY}}$ is true at input pin Y of the module. In either case NOR gate IC7-6 is high, and direct-sets the IC10 flip-flops which in turn keep the reread counter IC11 cleared.

Operational amplifier IC6 is connected with negative feedback through R26, establishing its gain at a value determined by the ratio of the input resistance to +10v switched by IC13 to the value of R26 (22K).

Capacitor C10 acts as an integrator slowing the response of IC6 to a change in input, which avoids coupling enough signal through C4 and C5 into IC1 to cause a spurious output. IC5 is connected as an

inverter outputing an equal but opposite polarity voltage to that voltage at IC6-10. The negative clipping level voltage (TPD) and positive clipping level voltage (TPC) are then applied to each read amplifier through a resistor dividing network to backbias diodes CR1 and CR2. This establishes the amplitude of analog input from the read preamplifier required for IC1 to switch and thus detect data.

401-4179-001H1



DASH NO	-004E	-005E	-001D	-002D	-003D
FIRST USED	9000	9000	9000	9000	9000
SPEED IPS	10-14,99	15-19,99	20-29,99	30-39,99	40-49,99
C1	.0039	.0033	.0022	.0015	.001
C4,C5	.001	680PF	470PF	330PF	270 PF
C6	.022	.015	.01	.0068	.0047

Read Amp Clipping Level Control
Type 4179
Schematic Diagram

TYPE 3848; 3849 WRITE AMPLIFIERS

CIRCUIT DESCRIPTION

These PC boards generate the internal write data strobe and contain the write amplifier stages for data channels P through 7 as explained below.

WRITE DATA STROBE GENERATION

The Write Data Strobe WDS is input from the interface at pin N and is supplied to an edge circuit consisting of inverters IC5 and IC6, capacitor C8, and NAND gate IC6-8. If Write Ready WRDY and Select SLT1 are true at input pins 12 and 13 of IC6, the gate transmits a short pulse on the leading edge of each input WDS. The pulse is gated through NOR gate IC5-6 and triggers one-shot IC1-1 on its trailing edge. The Q output of the one-shot supplies a positive 0.5 μsec pulse which is gated through NAND gate IC7-3, provided that the transport is not in a test mode. The pulse then enables the write NAND gates IC11 and IC15, gating the input write data to the write amplifier stages. It is also supplied as WDS1 to Type 3849 Write Amplifier module. When IC1-13 generates the write strobe, its $\overline{Q}$ output triggers the second IC1 one-shot, which in turn inhibits IC6 for a 3.5 μsec duration, inhibiting any pulses during that time.

If the transport is in test mode, TM true at pin K enables NAND gates IC5-2 and IC7-10, 12 while disabling NAND gate IC7-2. If Write Ready WRDY is true, crystal controlled data frequency f_r, supplied from the Delay Timing module, is gated through NAND gate IC5-12 and NOR gate IC5-6 to generate the test mode strobes. These are gated through the two IC7 NAND gates and direct-clear the write amplifier flip-flops on this module and on the other Write Amplifier module, writing the all-1 characters of the test mode.

WRITE AMPLIFIER STAGES

The data inputs are supplied from the data terminator card at pins R, S, T, and U, are inverted and then strobed through NAND gates IC11 and IC15 by the write data strobe WDS1, generated at test point B. The write channels are then supplied to the amplifier stages, each consisting of a divide-by-16 counter, a pair of flip-flops, and a pair of drivers. The amplifier stages are digitally deskewable, where the delay of channels 0 through 7 is adjusted to coincide with that of the reference channel, channel P, when read back.

The delay of channel P is permanently set to the count of eight, equivalent to a quarter character delay, by counter IC8. Whenever the input data is 1, the WDS pulse is gated through IC11-8 and direct-clears flip-flop IC9-13. The $\overline{Q}$ output of the flip-flop goes high, removing the direct-clear from the IC8 counter. The counter is then clocked by f_1 at 32 times the data frequency until the count of eight, at which point the Q_d output of the counter goes low and toggles IC9 flip-flop to the set state. The $\overline{Q}$ output of IC9 then goes low, locking the counter and toggling the output flip-flop IC9-9. During the next 1 character the same process is repeated with the output flip-flop IC9-9 toggling to the opposite state. When a 0 is input, the input NAND gate IC11-8 does not transmit the write data strobe, and consequently the write amplifier flip-flops are not toggled. The outputs of flip-flop IC9-5, 6 are then supplied to a pair of drivers IC10 which energize the write head, reversing the flux for each 1 while remaining unchanged for each 0, as required for NRZ1.

The operation of the amplifier stages of the eight other channels is identical to that of channel P, except that their delay is digitally adjustable. Four switches are connected to the parallel inputs of the skew delay counters of the eight channels, as shown for data channel 0. The skew of each channel can be measured and adjusted during the write test mode, which writes all 1's characters, by observing the analog outputs at the Type 3631 Read Preamplifier module.

Trigger channel 1 of a dual trace oscilloscope on the P channel so that one peak is easily observed. With channel 2 of the oscilloscope, observe the preamplifier channel that is to be checked or adjusted. Set the switches on the write amplifier channel so that the peaks of the two observed channels coincide. A small amount of jitter will be seen on the channel being adjusted due to tape recorder dynamics. Repeat the observations for all eight channels leaving the P channel as the reference.

Opening the switches reduces the count while closing them increases it. Thus when the switches are all opened the counter is direct-set to 16, gating the data character to the output without any delay. When the switches are all closed the skew counter is set at 0 and the character will be delayed 16 counts, or a quarter of a character time behind channel P.

WARS

The Write Amplifier Reset pulse $\overline{\text{WARS}}$ is input at pin P from the data terminator card, and is gated through NAND gate IC2-3, provided that Select 1 is true, to set flip-flop IC2-12. The 1 output of the flip-flop goes high, removing the direct-clear from shift register IC3. The register is then clocked by f_1 at 32 times the data frequency. On the seventh pulse, the Q_g output of the register goes high and is inverted by IC4-8 to issue $\overline{\text{WARSI}}$, resetting the write amplifier flip-flops on this module. $\overline{\text{WARSI}}$ is also output at pin H to Type 3849 Write Amplifier where it resets the flip-flops of the other amplifier stages. On the eighth pulse to the register the Q_h output goes high and is inverted by IC4-11, clearing flip-flop IC2 and locking itself until the next $\overline{\text{WARS}}$ is issued by the interface.

WRITE AMPS CARD

MASTER BD–DATA

401-3848-001K

DATA TERMINATOR CARD

MASTER BOARD DATA

WDS N

SLT 1 W

WRDY R

fR Y

TEST MODE H

A11 J1 DMB WARS P

f1

WARS 1

MASTER BD–DATA

WDP R

WD0 S

WD1 T

WD2 U

DATA TERMINATOR CARD HAS TERMINATORS (T) 220-330 OHM

+5V D

GRD C

C3 SEE TABLE

C4 SEE TABLE

CR3 1N914

CR4 1N270

CR1,1N270

CR2,1N270

CR4 SEE TABLE

DESKEW SWITCH

CHANNEL P

CHANNEL O

CHANNEL 1
IDENTICAL to CH. 0

CHANNEL 2
IDENTICAL to CH. 0

WRITE HEAD DRIVE (PIN 22, 3844)

A11J2

HEAD CONNECTOR P2

E WDS 1

2 TS

H WARS 2

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

TABLE

DASH NO.	C3	C4	CR4(CH2)
-001H	OMIT	OMIT	1N270
-002D	220PF	OMIT	1N270
-003B	OMIT	0.01	1N270
-004C	OMIT	OMIT	OMIT

Write Amps, Type 3848, Schematic Diagram

401-3849-001C

WRITE AMPS CARD

DATA TERMINATOR CARD

A11J1

CHANNEL 3

DESKEW SWITCH

CHANNEL 4
(IDENTICAL to CH. 3)

CHANNEL 5
(IDENTICAL to CH. 3)

CHANNEL 6
(IDENTICAL to CH. 3)

CHANNEL 7
(IDENTICAL to CH. 3)

WDS 1

DATA 3 V

f1

WARS 1

DATA 4 W

DATA 5 X

DATA 6 Y

DATA 7 Z

CR1 1N270

R1 10K

R2 10K

R3 10K

R4 10K

R5 220 ½W

R6 220 ½W

75451

846

177/197

107

WRITE HEAD DRIVE (PIN 22, 3844)

A11J2

HEAD CONNECTOR P2

DATA TERMINATOR CARD HAS TERMINATORS (T) 220-330 OHM

+5V

GRD

Write Amps, Type 3849-001C, Schematic Diagram

SECTION VII
GENERAL INFORMATION AND APPENDIX

DIGITAL RECORDING ON MAGNETIC TAPE USING NRZ1 CONVENTIONS AND FORMAT

1.1 INTRODUCTION

There are many recording techniques that may be employed to record digital information onto magnetic tape. Some of these are: non-return-to-zero (NRZ), return-to-zero, phase-encoded, Manchester coding, and NRZ1. Of these methods the NRZ1, non-return-to-zero change at logic 1, has been most widely accepted for recording parallel data onto multitrack recorders. This method has been used by IBM and other computer manufacturers for many years, and packing densities, formats, and mechanical dimensions have been fairly well standardized by usage throughout the industry.

1.1.1 IBM COMPATIBLE

The term IBM compatible, or more specifically IBM compatible 2400 series, is found frequently in specifications of tape units manufactured by companies other than IBM. This means that a tape written on a machine that is IBM compatible can be successfully entered into an IBM computer utilizing the IBM 2400 series of magnetic tape units. The converse, of course, is also true. Tapes written on an IBM 2400 can be read on IBM compatible tape units equipped with the read function.

This common denominator between systems is important, for often it is the only common point between computer systems and data acquisition systems. The parameters that ensure this compatibility relate to track width, number of tracks, position of the tracks on the width of the tape, form of check characters, spacing of check characters from data, length of interblock gaps, length of file gaps, and the character used to identify a file gap, as well as the mechanical dimensions of reels and hubs. This note describes these factors for the IBM compatible NRZ1 method of recording.

1.1.2 ADVANTAGES OF NRZ1 RECORDING METHOD

In the NRZ1 method of recording, current is flowing in one direction in the magnetic head at all times it is writing. This factor makes it possible to record over old data, erasing the old data as the recording is taking place. Head current also flows in a uniform direction during the interrecord gap. This is useful when it is necessary to rewrite a record or skip a bad area of tape found on re-read and allows the head current to be turned on again in a known direction without causing unwanted spikes.

Another advantage of the NRZ1 system is that the electronics for writing and reading are simpler than those required for other recording techniques, such as phase encoding.

A disadvantage of the NRZ1 system is that it is not self-clocking and is useful only where multiple track recording is employed. A further restriction is that in order to derive a clock from the multiple tracks, at least one of the tracks must have a one in it for each byte or character recorded. This last factor is ensured when a parity check is employed and the parity is odd. If even parity is used, then of course the all-zero character must be declared invalid and not used during the block.

1.2 WRITING NRZ1 TAPES

To record digital data on magnetic tape, it is necessary to magnetize the tape discretely to indicate binary ones and zeros. In the NRZ1 method, current is flowing in the head at all times the magnetic tape unit is in the write mode. As long as the head current does not change, the data will be written such that it will be interpreted as zeros. When a transition occurs between saturation magnetism (plus and minus) on the tape, this will be interpreted as a one. Figure 1-1 shows typical waveforms for data recorded on tape in the pattern 011010. The data is entered together with write clocks as shown, with a write clock for each bit recorded. With tape in continuous motion, a flux pattern corresponding to the tape magnetization will appear on the tape as shown.

NRZ1 recording is implemented by driving current through the head winding in a direction determined by a flip-flop that toggles for each one, gated in by coincidence between data and a write clock.

1.3 READING NRZ1 RECORDINGS

To recover the data written in NRZ1 format, the tape is moved at a constant velocity past the gap in the head. Refer to Figure 1-2. If the same pattern shown above is present on the tape, the head voltage

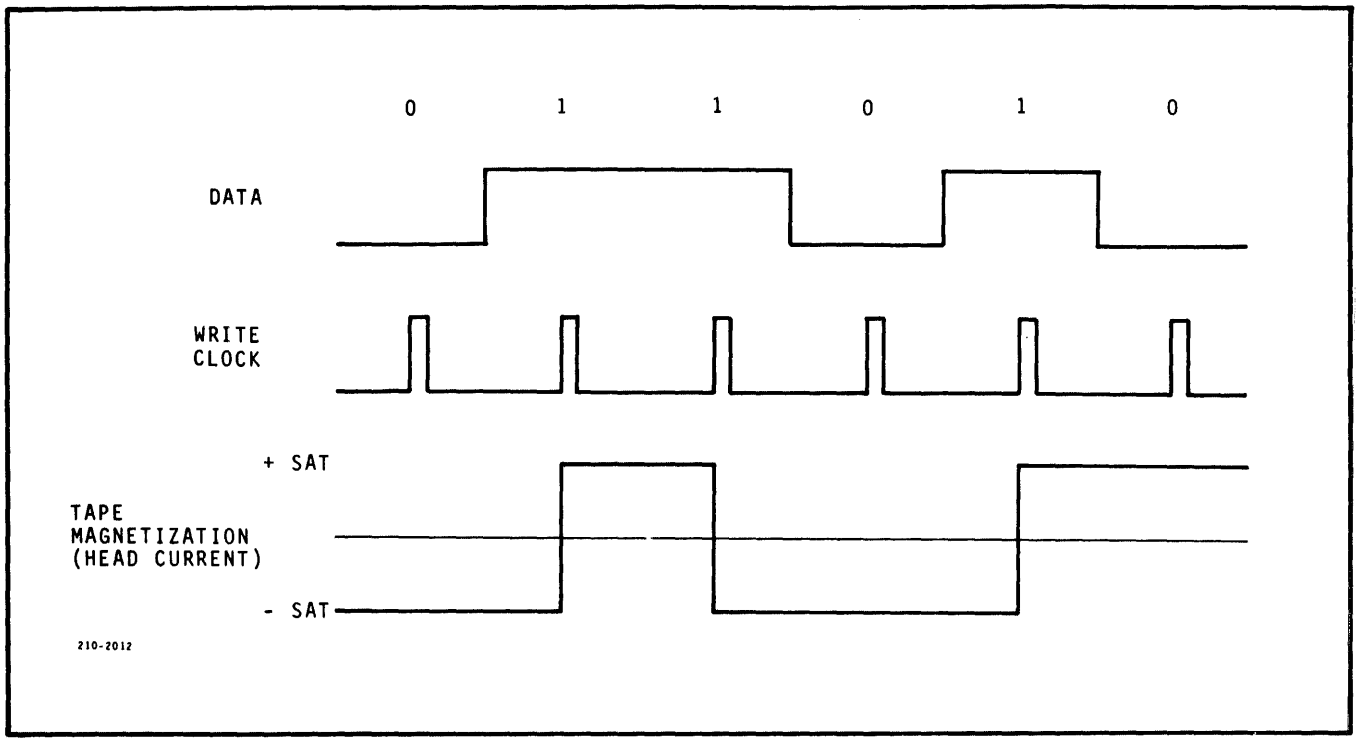


Figure 1-1 NRZ1 Waveforms - Writing

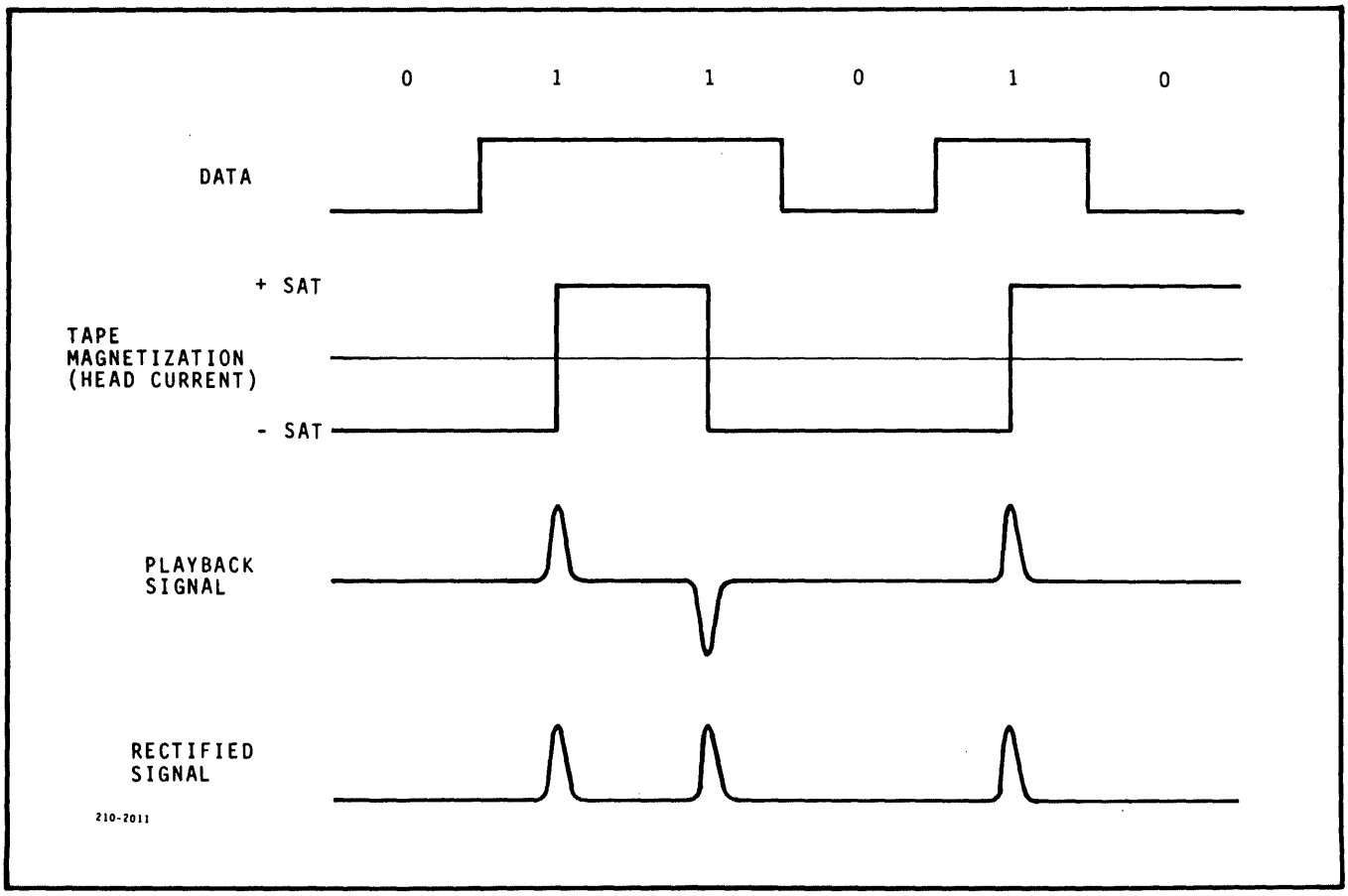


Figure 1-2. NRZ1 Waveforms - Reading

will look like the playback signal since the voltage induced in the head is the differential of the flux pattern on the tape. The characteristic half sine wave results from the fact that the gap on the head has a finite width.

The pattern shown is typical of what would be seen with 200 bits per inch (bpi) recording. As the recording density increases, the mechanical dimensions of the head remain the same, resulting in the same waveform but with the individual waves crowded close together. This ultimately presents a limit beyond which this type of recording is useful with state-of-the-art tapes and magnetic heads. Recording of 800 bpi seems to be a practical limit and is the maximum density utilized in present-day systems.

The playback signal is then rectified and, as can be seen from the figures, a pulse is present for every one recorded and the base line remains stationary for all zeros recorded. Note, however, that it is not practical to derive an accurate clock from the signal on the basis of a single-track recording. However, since this is a multiple track system and employs a parity generator, a data bit will be found on one of the multiple tracks for each character written, assuming that an all-zeros character is not employed in conjunction with even parity.

Considering the above factors, a typical read amplifier consists of an analog amplifier, a rectifier, a peak detector, suitable logic to create a clock, and an output buffer stage to enable interfacing to the customer's unit.

1.3.1 SKEW AND GAP SCATTER

Another major factor that limits the design of an NRZ1 multiple track system is that heads are not perfect because of gap scatter and head mounting to decks is not perfect causing skew. Both these factors have the same effect in that the signals from all the tracks do not occur perfectly in unison. The problem is minimal if the same head and deck are used for reading and writing a given tape, but since interchangeability of tapes between machines is mandatory provisions must be made to cancel out these effects. The allowable tolerances in head manufacture have practical limits and are typically in the ±50 microinch region for high quality heads. Fixed heads without adjustment are practical with 200 bpi and 556 bpi recording, but 800 bpi recording requires adjustments.

All Kennedy recorders are equipped with the necessary deskewing adjustment to enable operation and assure compatibility with other magnetic tape units. These adjustments take the following form.

1.3.1.1 Read Head Alignment

The read head is adjusted so that its gaps are perpendicular to the direction of tape motion using an IBM skewmaster tape. A mechanical adjustment is provided consisting of a spring loaded mounting plate working against a fine pitch adjusting screw. (On incremental and some low density machines this adjustment is either not required or is made by shimming tape guides.)

1.3.1.2 Read Electronic Deskew Register

All Kennedy read amplifiers are provided with a deskewing register. This register allows a total skew of 50 percent for all reasons including write head gap scatter, dynamic read skew, read head misalignment, and speed variation in writing or reading.

1.3.1.3 Write Electronic Deskewing (continuous tape units only)

The mechanical relationship between the read gap and the write gap is fixed in any given read after write head. Since the read head is adjusted perpendicular to tape motion (paragraph 1.3.1.1), the write time for each channel may be delayed selectively so that a character is written on the tape perpendicular to tape motion. In Kennedy continuous tape units a fixed delay is inserted for one channel and individual delays are provided for the remaining channels. This arrangement allows each channel to be adjusted in exact relationship to the fixed channel and allows adjustment for skew and gap scatter as well.

1.4 TAPE FORMATS

There are other factors that affect compatibility in addition to density and recording method:

a. Tape markers
b. Gaps
c. Check characters
d. Codes

1.4.1 TAPE MARKERS

When recording on magnetic tape, care must be taken to avoid physical handling and damage to the recorded surface. A portion of tape — at least 10 feet — at each end is reserved for threading and loading and is not used for storing data. To define the recorded area, pressure sensitive reflective markers are applied to the nonoxide side of the tape as shown in Figure 1-3.

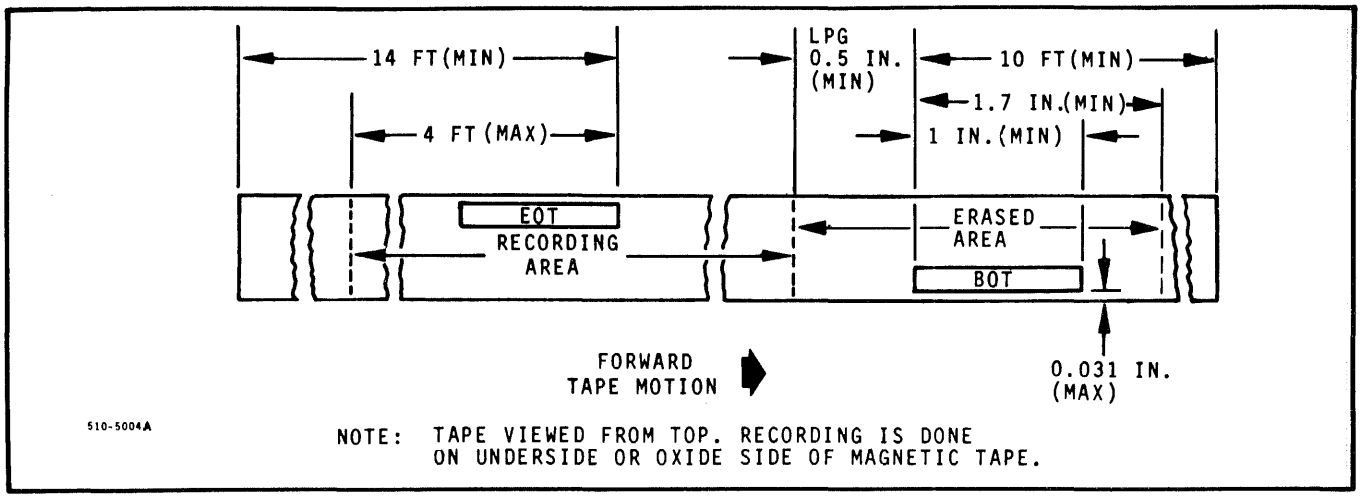


Figure 1-3. Tape Markers

These markers are sensed optically and define the recorded area in a standardized manner.

The BOT marker signal is used internally to define the load point or starting of recording. The EOT marker signal is not used internally but is available to the interface as an end of tape warning signal and should be used by the unit interfaced to the magnetic units to terminate recording within the next 4 feet of tape.

1.4.2 GAPS

Tape reading can only take place reliably when tape is moving at a known speed across the head. To allow tape to start and stop while the computer manipulates data, a section of tape with no data is provided between records or blocks of data and at the beginning and end of tape. This section is recorded with the head current turned on in the direction defined as erased and results in a constant flux in a predetermined direction which is independent of tape speed or motion. The direction of current in the heads defining the erased condition is also controlled to be uniform in all recorders. On readback this flux is constant as the tape accelerates and decelerates. Since a change in flux is required for the read head to sense data, no signal occurs and orderly starts and stops may be made.

Mechanical limitations preclude instantaneous starts and stops, and a distance of tape must be reserved, conditioned by the requirements of the "worst case" machines, to use the standards. While high speed units (IBM 2400 series) set the length of the gaps, Kennedy recorders utilize the full gap length to advantage by providing controlled acceleration and deceleration, resulting in minimum stresses to the tape.

1.4.2.1 Beginning of Tape Gap

An erased section of tape is required surrounding the BOT marker. This serves as a defined area within which data recording or reading can start. To comply with IBM specifications this section extends a minimum of 1.7 inches ahead of the trailing edge of the BOT marker and extends a minimum of 0.5 inch past the trailing edge of the BOT marker. In nearly all systems (including IBM) this erased section totals about 3.5 inches (Figure 1-3).

1.4.2.2 Interrecord Gaps

Interrecord gaps are areas, without data, placed between data blocks or records as shown in Figure 1-4. The length of the gap is 0.75 inch minimum for seven-track systems and 0.60 inch minimum for nine-track

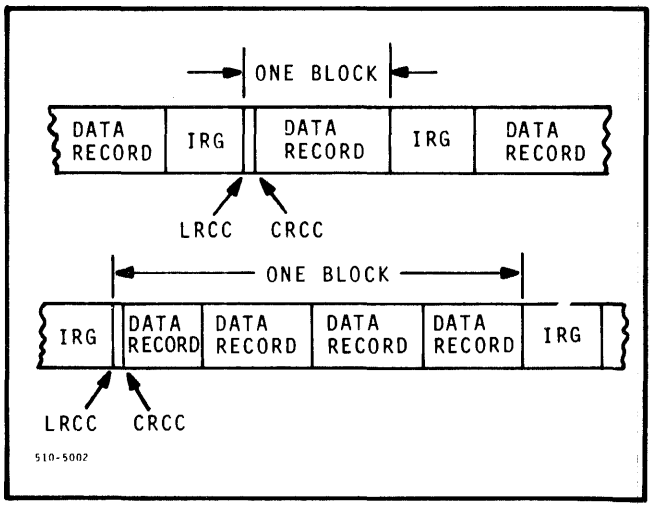


Figure 1-4. Interrecord Gaps

systems. The maximum length is not critical. The USA Standard Institute specifies the maximum length at 25 feet.

If records are short it can be seen that a large portion of the tape is used for interrecord gaps. In many cases computers are programmed to handle records in batches as shown in Figure 1-4. In this case the IRG and check characters are inserted on a block basis.

Figure 1-5 shows the format of the file mark for seven- and nine-track tapes. The distinguishing feature of the block is the fact that it is a single specific character record with a check character. The erased gap itself is nearly always used but IBM standards state that it is optional.

1.4.3 CHECK CHARACTERS

The NRZ1 format provides for both vertical and horizontal parity checks. In the nine-track system an additional check called the cyclic redundancy check character is used. Refer to Figures 1-6 and 1-7 for the location of the check characters.

The check characters define to a very high level of confidence that a block that is read is accurate.

1.4.3.1 Vertical Parity

Seven-track and nine-track systems use six and eight tracks respectively for recording data. The remaining track is redundant and carries the parity information. When the data is written on tape, a parity generator senses the input data and determines if the number of bits in the byte is odd or even. It outputs a "1" or a "0" to the redundant track to make the count odd if odd parity is selected, or even if even parity is selected.

On readback a similar circuit can be used to count the number of bits in each byte and determine if the count is odd or even. Depending on which is defined as correct, it signals the error line if the count is wrong. Thus each byte is checked. However, if an even number of bits is dropped the test will not result in an error signal, so an additional check called longitudinal parity is employed.

Odd or even parity may be selected on seven-track recorders. Nine-track recorders are always odd parity.

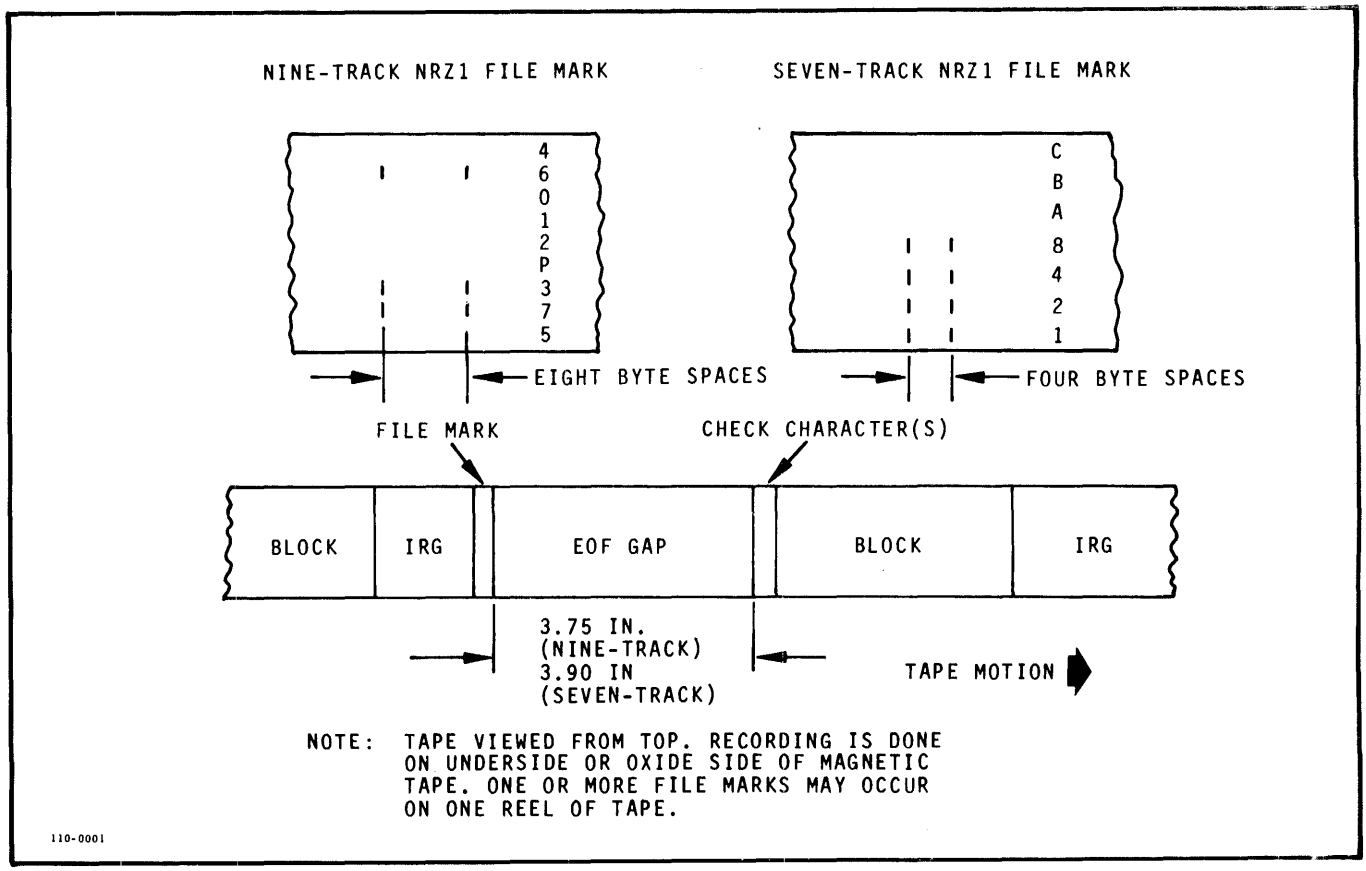
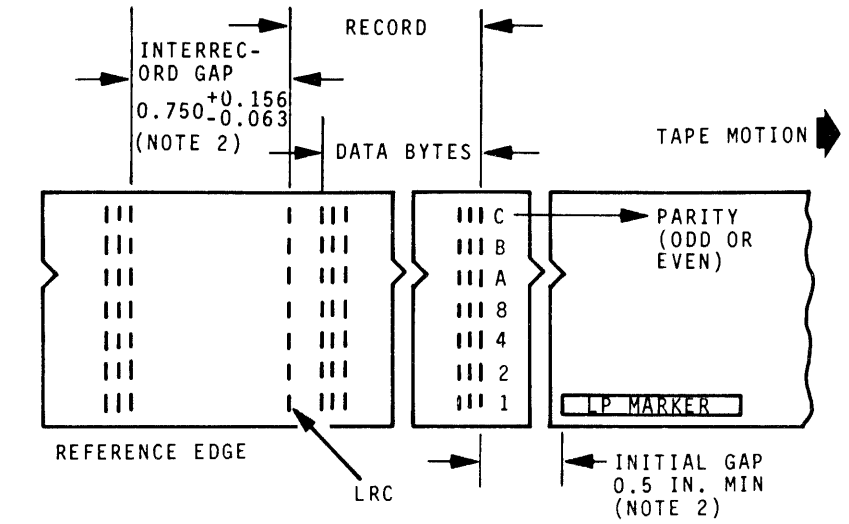


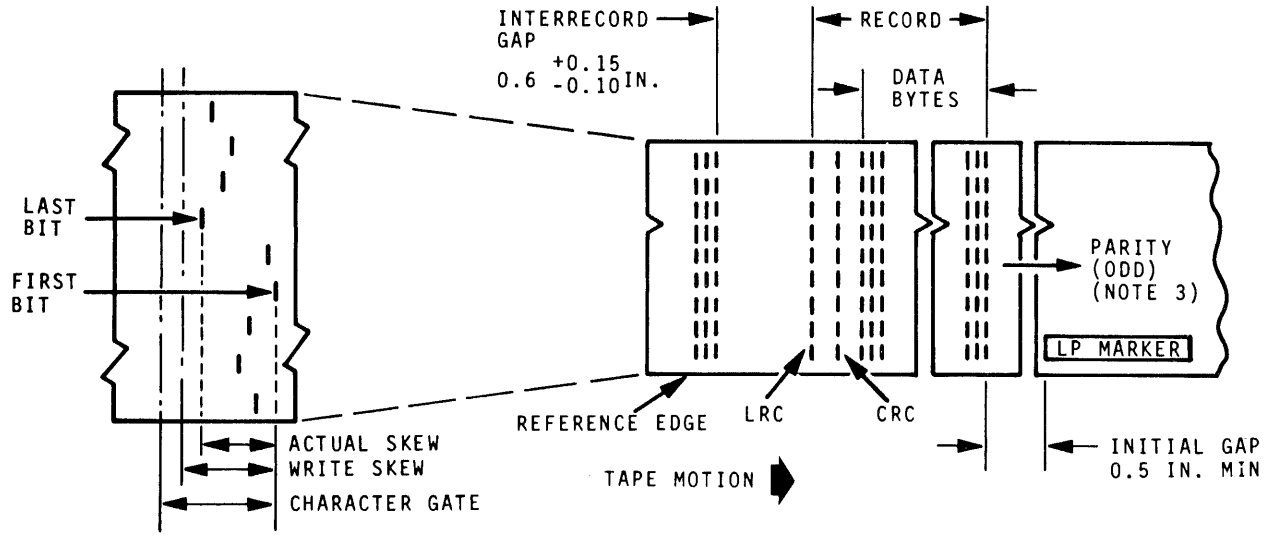
Figure 1-5. NRZ1 File Marks



NOTES:
1. TAPE IS SHOWN WITH OXIDE SIDE DOWN. NRZ1 RECORDING. BIT PRODUCED BY REVERSAL OF FLUX POLARITY.
2. TAPE TO BE FULLY SATURATED IN THE ERASED DIRECTION IN THE INITIAL GAP AND THE INTERRECORD GAP. ERASURE SUCH THAT A NORTH SEEKING END OF COMPASS WILL POINT TO START OF TAPE.
3. LRC (LONGITUDINAL REDUNDANCY CHECK CHARACTER) ODD OR EVEN-SPACED FOUR BITS FROM DATA CHARACTER.
4. PARITY BIT (A VERTICAL PARITY BIT IS WRITTEN FOR EACH BYTE).

110-0017

Figure 1-6. Data Format - Seven Track



NOTE:
1. CRC (CYCLIC REDUNDANCY CHECK CHARACTER). PARITY OF CRC CHARACTER IS DETERMINED BY THE NUMBER OF DATA CHARACTERS IN RECORD. ODD NUMBER OF DATA CHARACTERS-EVEN CRC CHARACTER, ETC. CRC USED ONLY IN IBM SYSTEM SYSTEM/360 800BPI. CRC CHARACTER SPACED FOUR BITS FROM DATA CHARACTERS.
2. LRC (LONGITUDINAL REDUNDANCY CHARACTER) ALWAYS ODD PARITY. SPACED FOUR BITS FROM CRC.
3. PARITY BIT (A VERTICAL PARITY BIT IS WRITTEN FOR EACH CHARACTER CONTAINING AN EVEN NUMBER OF BITS).

110-0018

Figure 1-7. Data Format - Nine Track

1.4.3.2 Longitudinal Parity

A longitudinal redundancy check character is written at the end of each block. It is separated from the end of each block as shown in Figure 1-8. This character is made up on a per-track basis. The number of 1's recorded in a given track of a block is counted and a "1" is written in the track as the LRCC if the count was odd, and, therefore, the number of 1's recorded in each track becomes even for any given block. On readback this is checked and an error is detected if the count is odd in any track. The possibility of not detecting an erroneous block still exists if an even number of bits in a given track of a block is dropped. However, when this test is combined with the vertical parity test the probability of not detecting an error is reduced.

1.4.3.3 Cyclic Redundancy Check Character (CRCC)

In the nine-track system another check character must be written. This character is derived with relatively complex logic, the result of which, in combination with the LRCC and vertical parity information, enables a computer to determine in which track a dropout occurred. If the dropout occurred in only one track in the given block, the computer can then nullify that track and generate the information in that track from the data in the remaining tracks, which includes the parity track.

This check character follows the last data byte by four cell positions, as shown in Figure 1-8.

1.4.3.4 Codes

The recorder will accept and read back any code set applied (six-bit for seven-track, eight-bit for nine-track). The only restriction is that the 000000 character in a seven-track system using even parity must not be used. This is a blank position or missing character, and most IBM systems will register an error condition if it is found in a block.

Two code sets are shown in Figure 1-9. These are the graphic symbols portion of the codes used by IBM for nine-track and seven-track systems. They are shown for reference only. Systems may use different code structures when they are programmed for them.

In the seven-track system the 000000 character may be converted to the 001010 character by use of the "BCD 0 to 10" option which is available for most Kennedy recorders. This senses the 000000 character on the data lines in conjunction with a write clock and converts it internally to record the IBM character for the number 0 (001010).

1.4.4 SUMMARY OF FORMAT

A summary of the above factors is shown in Figure 1-6 for seven-track data format and Figure 1-7 for nine-track data format Record blocks and tape markers are shown in Figure 1-10.

1.4.5 REFERENCES

Additional information may be found in the following publications:

a. IBM 2400-Series Magnetic Tape Units Original Equipment Manufacturers' Information, IBM Form 226862-4

b. USA Standard Recorded Magnetic Tape for Information Interchange (800 cpi, NRZ1), United States of America Standards Institute, 10 East 40th Street, New York 10016

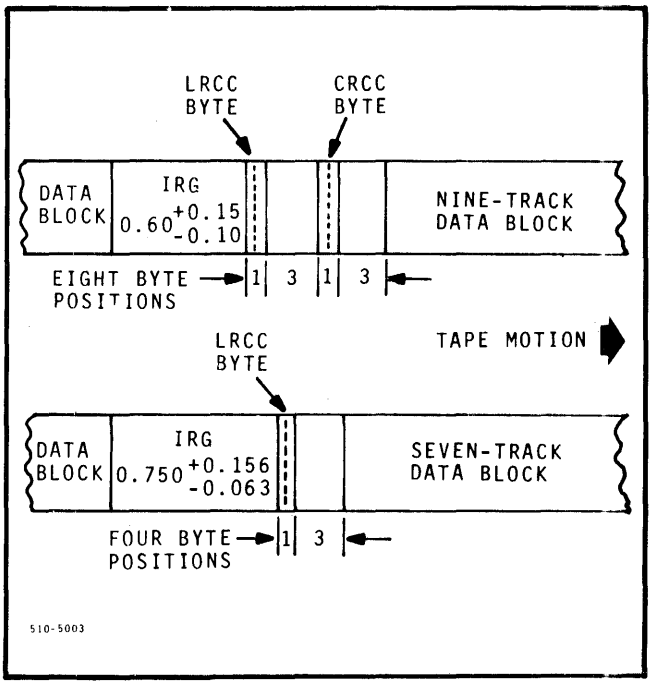
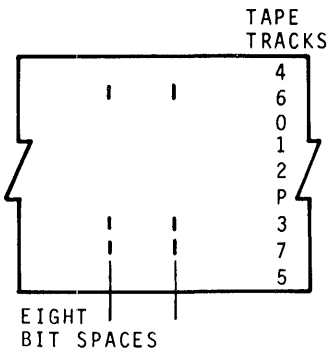


Figure 1-8. Check Characters

COLLATING SEQUENCE	GRAPHICS		EXTENDED BINARY CODED DECIMAL INTERCHANGE CODE (EBCDIC)								BINARY CODED DECIMAL INTERCHANGE CODE (BCD)					
	8 Bit	BCD	0	1	2	3	4	5	6	7	B	A	8	4	2	1
00	blank	blank	0	1	0	0	0	0	0	0	0	0	0	0	0	0
01	.	.	0	1	0	0	1	0	1	1	1	1	1	0	1	1
02	←	¤)	0	1	0	0	1	1	0	0	1	1	1	1	0	0
03	(	[	0	1	0	0	1	1	0	1	1	1	1	1	0	1
04	+	<	0	1	0	0	1	1	1	0	1	1	1	1	1	0
05	GM	GM	0	1	0	0	1	1	1	1	1	1	1	1	1	1
06	&	& +	0	1	0	1	0	0	0	0	1	1	0	0	0	0
07	$	$	0	1	0	1	1	0	1	1	1	0	1	0	1	1
08	*	*	0	1	0	1	1	1	0	0	1	0	1	1	0	0
09	)	]	0	1	0	1	1	1	0	1	1	0	1	1	0	1
10	;	;	0	1	0	1	1	1	1	0	1	0	1	1	1	0
11	MC	MC	0	1	0	1	1	1	1	1	1	0	1	1	1	1
12	-	-	0	1	1	0	0	0	0	0	1	0	0	0	0	0
13	/	/	0	1	1	0	0	0	0	1	0	1	0	0	0	1
14	,	,	0	1	1	0	1	0	1	1	0	1	1	0	1	1
15	%	%(	0	1	1	0	1	1	0	0	0	1	1	1	0	0
16	WS	WS	0	1	1	0	1	1	0	1	0	1	1	1	0	1
17	↑	\	0	1	1	0	1	1	1	0	0	1	1	1	1	0
18	SM	SM	0	1	1	0	1	1	1	1	0	1	1	1	1	1
19	ъ	ъ	0	1	1	1	1	0	1	0	0	1	0	0	0	0
20	#	#=	0	1	1	1	1	0	1	1	0	0	1	0	1	1
21	@	@'	0	1	1	1	1	1	0	0	0	0	1	1	0	0
22	∇	:	0	1	1	1	1	1	0	1	0	0	1	1	0	1
23	=	>	0	1	1	1	1	1	1	0	0	0	1	1	1	0
24	TM	TM	0	1	1	1	1	1	1	1	0	0	1	1	1	1
25	ŏ	ŏ	1	1	0	0	0	0	0	0	1	1	1	0	1	0
26	A	A	1	1	0	0	0	0	0	1	1	1	0	0	0	1
27	B	B	1	1	0	0	0	0	1	0	1	1	0	0	1	0
28	C	C	1	1	0	0	0	0	1	1	1	1	0	0	1	1
29	D	D	1	1	0	0	0	1	0	0	1	1	0	1	0	0
30	E	E	1	1	0	0	0	1	0	1	1	1	0	1	0	1
31	F	F	1	1	0	0	0	1	1	0	1	1	0	1	1	0
32	G	G	1	1	0	0	0	1	1	1	1	1	0	1	1	1
33	H	H	1	1	0	0	1	0	0	0	1	1	1	0	0	0
34	I	I	1	1	0	0	1	0	0	1	1	1	1	0	0	1
35	ŏ	ŏ	1	1	0	1	0	0	0	0	1	0	1	0	1	0
36	J	J	1	1	0	1	0	0	0	1	1	0	0	0	0	1
37	K	K	1	1	0	1	0	0	1	0	1	0	0	0	1	0
38	L	L	1	1	0	1	0	0	1	1	1	0	0	0	1	1
39	M	M	1	1	0	1	0	1	0	0	1	0	0	1	0	0
40	N	N	1	1	0	1	0	1	0	1	1	0	0	1	0	1
41	O	O	1	1	0	1	0	1	1	0	1	0	0	1	1	0
42	P	P	1	1	0	1	0	1	1	1	1	0	0	1	1	1
43	Q	Q	1	1	0	1	1	0	0	0	1	0	1	0	0	0
44	R	R	1	1	0	1	1	0	0	1	1	0	1	0	0	1
45	RM	RM	1	1	1	0	0	0	0	0	0	1	1	0	1	0
46	S	S	1	1	1	0	0	0	1	0	0	1	0	0	1	0
47	T	T	1	1	1	0	0	0	1	1	0	1	0	0	1	1
48	U	U	1	1	1	0	0	1	0	0	0	1	0	1	0	0
49	V	V	1	1	1	0	0	1	0	1	0	1	0	1	0	1
50	W	W	1	1	1	0	0	1	1	0	0	1	0	1	1	0
51	X	X	1	1	1	0	0	1	1	1	0	1	0	1	1	1
52	Y	Y	1	1	1	0	1	0	0	0	0	1	1	0	0	0
53	Z	Z	1	1	1	0	1	0	0	1	0	1	1	0	0	1
54	0	0	1	1	1	1	0	0	0	0	0	0	1	0	1	0
55	1	1	1	1	1	1	0	0	0	1	0	0	0	0	0	1
56	2	2	1	1	1	1	0	0	1	0	0	0	0	0	1	0
57	3	3	1	1	1	1	0	0	1	1	0	0	0	0	1	1
58	4	4	1	1	1	1	0	1	0	0	0	0	0	1	0	0
59	5	5	1	1	1	1	0	1	0	1	0	0	0	1	0	1
60	6	6	1	1	1	1	0	1	1	0	0	0	0	1	1	0
61	7	7	1	1	1	1	0	1	1	1	0	0	0	1	1	1
62	8	8	1	1	1	1	1	0	0	0	0	0	1	0	0	0
63	9	9	1	1	1	1	1	0	0	1	0	0	1	0	0	1

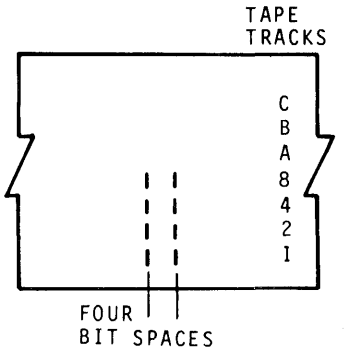
Figure 1-9. Typical IBM Codes

NINE-TRACK NRZ1 TAPE MARK



A NINE-TRACK NRZ1 TAPE MARK IS A SPECIAL CONTROL BLOCK THAT CONSISTS OF A CHARACTER WITH 1-BITS IN DATA TRACKS 3, 6, AND 7, AND AN IDENTICAL LRC CHARACTER EIGHT BIT SPACES FROM IT. NO CRC CHARACTER IS WRITTEN. ALTHOUGH THE TAPE MARK IS PRECEDED BY APPROXIMATELY 3.75 INCHES OF ERASED TAPE, THIS GAP IS NOT A REQUIREMENT.

SEVEN-TRACK NRZ1 TAPE MARK



A SEVEN-TRACK NRZ1 TAPE MARK IS A SPECIAL CONTROL BLOCK THAT CONSISTS OF A CHARACTER WITH 1-BITS IN A DATA TRACKS 8, 4, 2, AND 1, AND AN IDENTICAL LRC CHARACTER FOUR BIT SPACES FROM IT. ALTHOUGH THE TAPE MARK IS PRECEDED BY APPROXIMATELY 3.90 INCHES OF ERASED TAPE, THIS GAP IS NOT A REQUIREMENT.

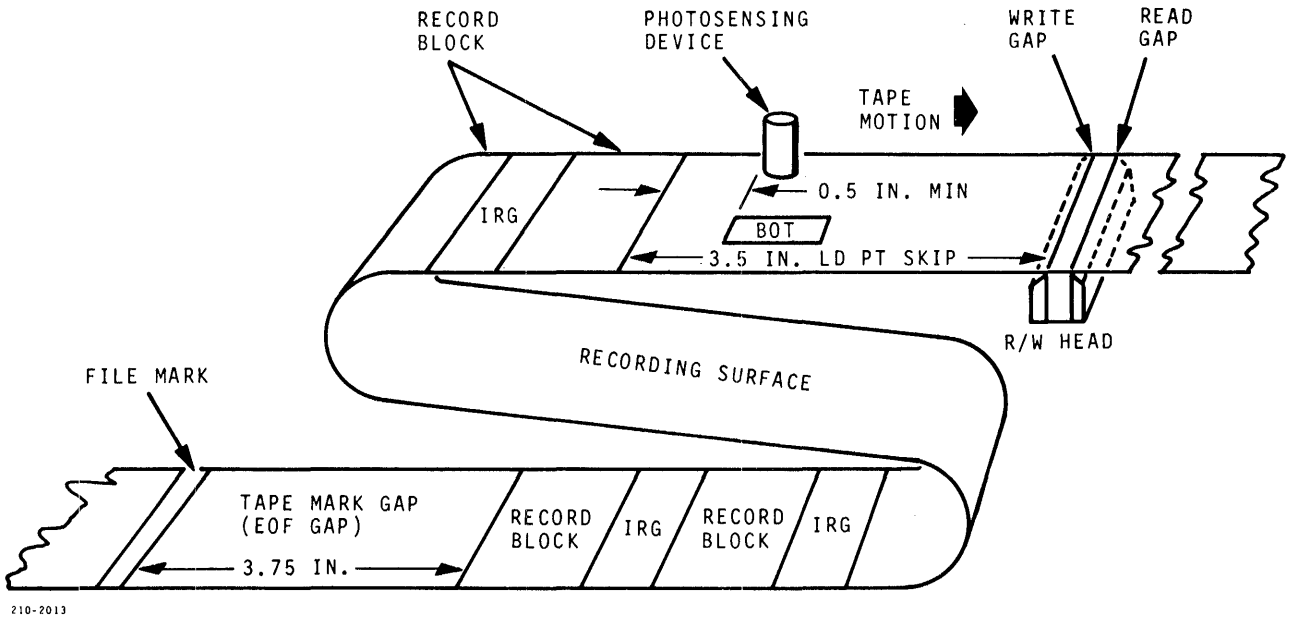


Figure 1-10. Record Blocks and Tape Marks

PHASE ENCODED RECORDING

Introduction

For many years, NRZ1 recording has been used in most computer tape systems. Density has increased from 200 cpi to 556 cpi and 800 cpi in the quest to increase data storage capability of tape and to achieve higher data rates.

With higher densities mechanical tolerances become more and more critical, however, and 800 cpi is probably the practical limit for NRZ1 recording. If higher densities were to be achieved, a new recording method was required.

Phase encoding was chosen. Its advantages were well known from use of similar systems on drums and specialized tape drives. In computer use, tape density of 1600 cpi was selected, and a tape format was established first by IBM and later adopted by ANSI as a proposed American national standard.

Figure 1 shows graphically the effect of density on tape storage capacity as a function of block length.

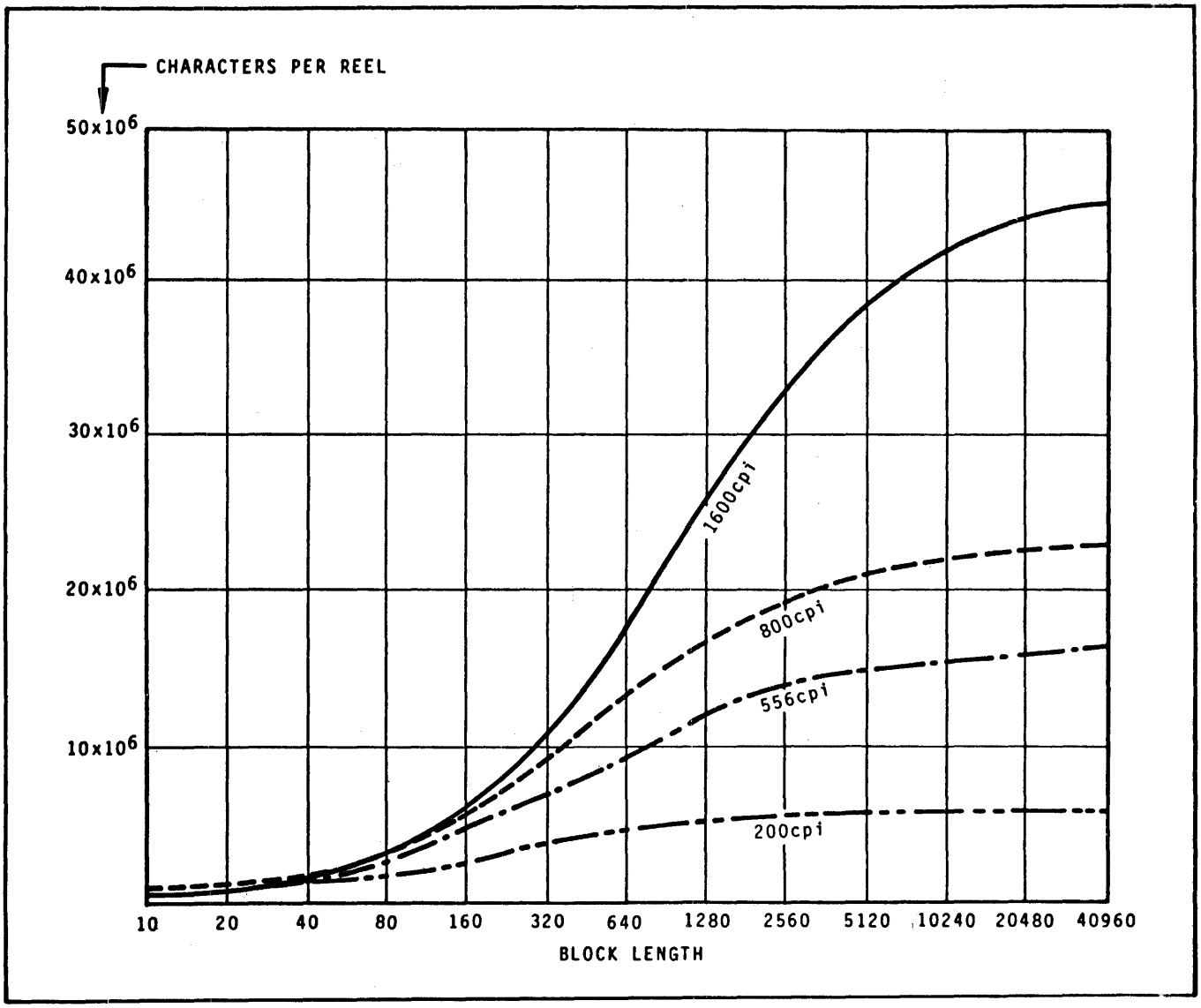


Figure 1. Comparison of Packing Density, Phase Encoded and NRZ1 Formats

Phase Encoded Recording

Each of the nine tracks on a PE tape is recorded in such a manner as to allow recovery of a track clock plus the data. This removes the requirement for close skew alignment as in NRZ1 recording, since clocked data can be assembled in a register to remove the effects of skew.

Saturation recording is used. Tape is dc erased with a polarity such that the rim end of the tape becomes a north seeking pole. A one bit is defined as a flux reversal to the reference polarity. A zero bit is defined as a flux reversal toward the opposite polarity. A "phase flux reversal" is written at the nominal midpoint between successive ones or successive zeros to establish proper polarity.

Figure 2 shows the resulting pattern of reversals on tape. It will be seen that the recording results in two bit densities being recorded, 1600 flux reversals per inch (frpi) and 3200 frpi. Phase shift of these two frequency components is of the utmost importance for decoding after playback.

Figure 3 is a logic diagram of a write amplifier that generates the required waveforms.

Tape Format

For IBM compatibility, tapes must be written in the proper format. This includes conventions on gap-lengths and special marks on tape. These have been chosen to ensure compatibility with nine-track 800 cpi NRZ1 on the same transport but with different electronics.

PE Format Requirement

a. Identification burst. A burst of recording in track 4 (P channel) only starting a minimum of 1.7 inches before the load point marker and extending past load point, but ending at least 0.5 inch before the first data block. Used to identify PE tapes.

b. Initial gap. A gap of at least 3 inches between the load point marker and the beginning of the first data block.

c. Preamble. A burst of 40 zero characters in each track followed by a character containing ones in each track.

d. Data. Nine tracks, channel assignments same as 800 cpi.

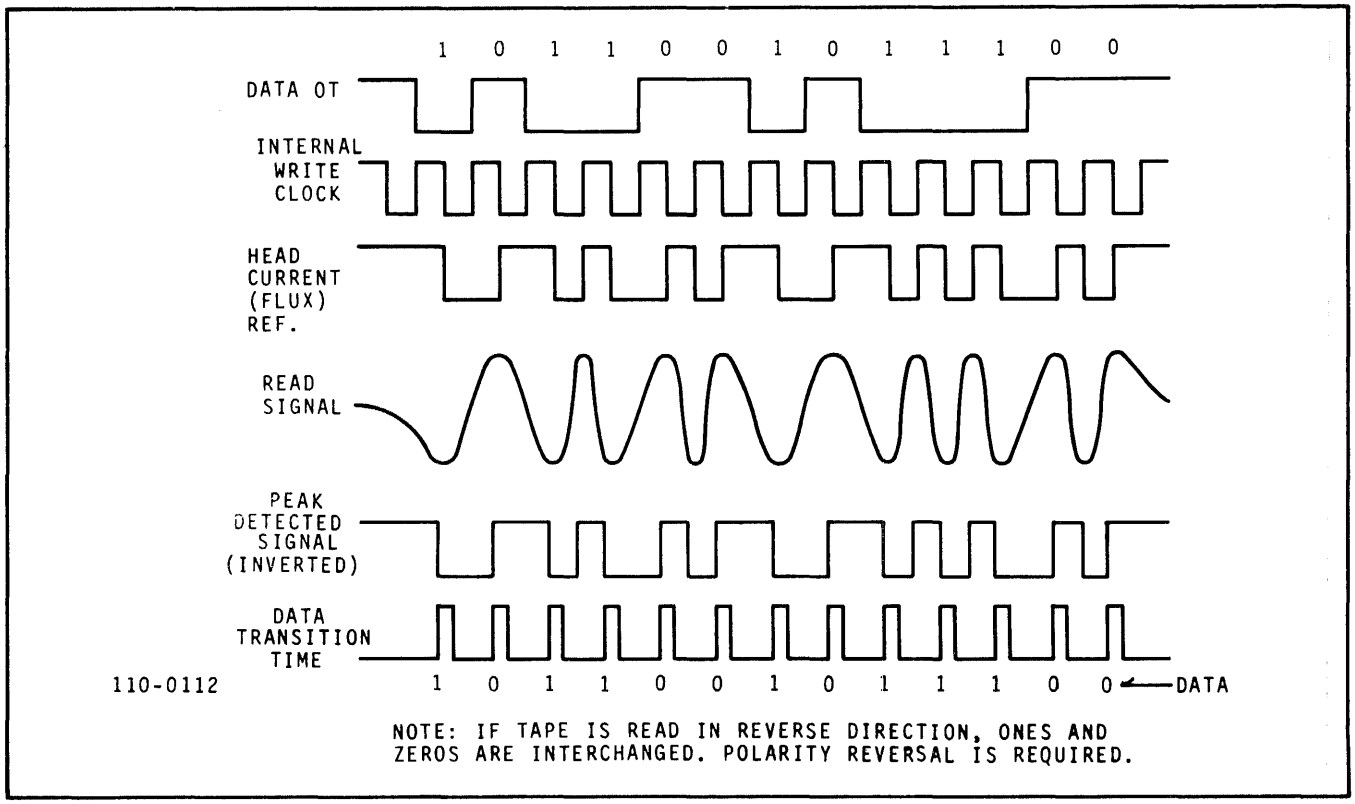


Figure 2. Phase Encoded Waveforms

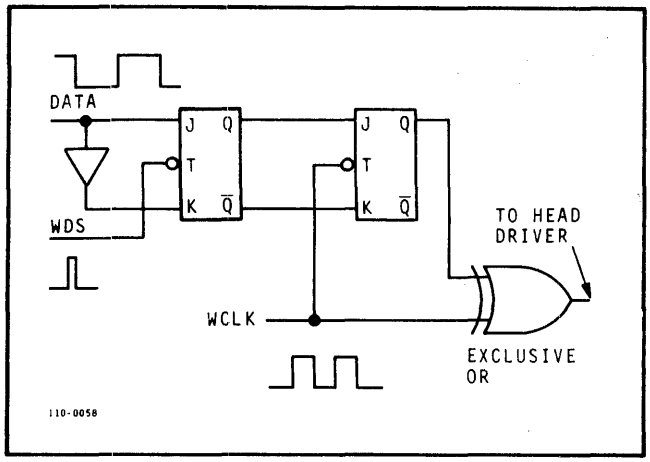


Figure 3. Write Amplifier Logic

e. Postamble. An all ones character followed by 40 all zero characters.

f. Interrecord gap. A gap 0.6 inch long nominal (0.5 inch minimum, 25 feet maximum) erased in the reference direction.

g. Tape marks. Tape marks are special control blocks used to identify portions of the tape. As opposed to NRZ1 format which has only one tape mark, there are eight possible marks in PE format. Tape mark blocks may be from 64 to 256 characters in length and are recorded in the format shown in Table 1.

Reflective Strips

Load point and end-of-tape reflective strips are attached to the tape in the same positions and with the same meaning as in NRZ1 recording.

Check Characters

All PE tapes are written with odd vertical parity. There are no LRC or CRC characters in the PE system. They are not needed since the location of the track in error can be easily detected through the coding system.

Reading Phase Encoded Tapes

Reading methods for PE tapes differ, naturally, from NRZ1 methods. Following is a general discussion of means employed to extract recorded information. More specific circuit descriptions will be found in instruction manuals for Kennedy Company PE units.

Amplified head signal waveforms are shown in Figure 4 for a typical data block. Preamble and postamble are easily identified at the beginning and end of the block. Purpose of the preamble is to allow synchronization with the signal by a phase-locked oscillator before data begins. It is written at 3200 frpi (all zeros).

Because of tape and head response limitations, the high frequency components are of lower amplitude than the low frequency components.

Differentiation of the amplified signal is performed in read electronics. Signal is then crossover detected, and digitized. A new signal envelope detector is used to detect "dropouts" in order to precisely determine defective parts of tape. Up to three characters may be lost at the beginning of the block and some noise can be seen at the end of the block (after the last zero) for up to two characters time.

Two conditions should be met before signals are recognized as valid data: (a) Signals must be present in all tracks; (b) a number of zeros (approximately 25) must be followed by an all ones character preamble detected).

Once detected, the preamble combination of all ones must be treated as a valid character. All zeros is not a valid character unless the single track dropout line is active.

One phase-locked oscillator and associated electronics is recommended for better tolerance to tape deck

TRACK	CHANNEL	1	2	3	4	5	6	7*	8
1	5	X	-	X	-	X	-	X	-
2	7	X	X	X	X	X	X	X	X
3	3	-	-	-	-	-	-	-	-
4	P	-	X	X	-	-	X	X	-
5	2	X	X	X	X	X	X	X	X
6	1	-	-	-	-	-	-	-	-
7	0	-	-	-	X	X	X	X	-
8	6	X	X	X	X	X	X	X	X
9	4	-	-	-	-	-	-	-	-

\- dc erased

x recorded at 3200 frpi

* most frequently used combination

110-0113

Table 1. Tape Mark Combinations

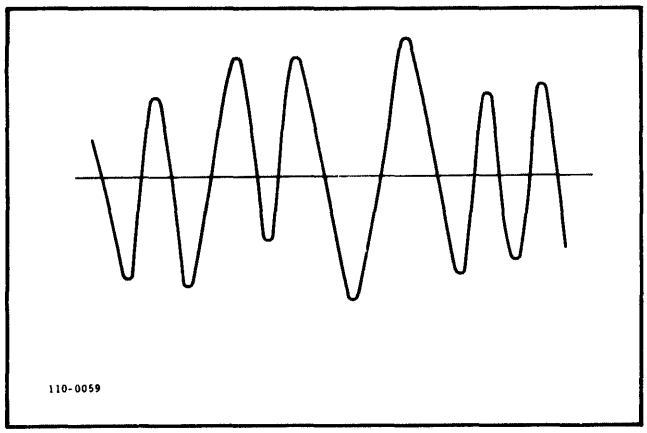


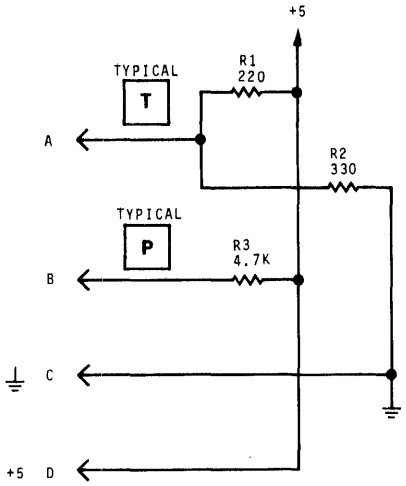
Figure 4. Read Signal

speed variation and write data timing. Two detectors, a one detector and a zero detector, are used to develop data. If, in the required time, neither detector has an output, a single track dropout is signaled and data correction ensues.

Each read channel has three output lines: one, zero, clock. These three lines are fed to a four-stage shift register controlled by an up-down counter. Upon entering the shift register, the 1 or 0 bit is shifted to the right to occupy the last open shift register cell. As data characters are read out, the shift register contents are shifted to the right. This allows up to four characters of skew. An error is posted if the skew register overflows.

Since single track dropouts are detected on a per bit basis and since the track in error is known, the character in the SR output stage can be corrected. This is done by reconstructing the missing bit by placing the remaining bits in a parity generator and adjusting the missing bit so that odd parity is achieved. If more than one track drops out, a multiple track error condition is flagged. In this case correction is not possible.

It can be seen from the preceding discussion that some complexity is required in the PE read electronics. If possible, it is desirable to share read electronics among several tape units as in Kennedy System 9000. If a customer wishes to build his own PE electronics, licenses are available to use Kennedy Company designs, thereby saving a considerable amount of engineering time.



E ← T

F ← T

J ← T

L ← T

M ← OMIT

N ← T

P ← T

R ← P

S ← P

T ← P

U ← P

V ← P

W ← P

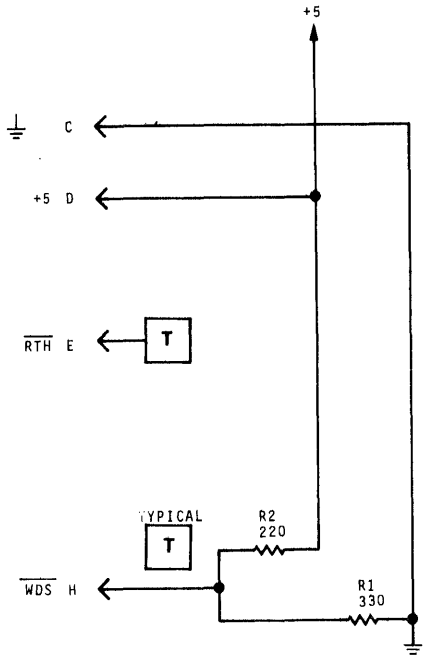
X ← P

Y ← P

Z ← P

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Control Terminator, Type 3841-001C, Schematic Diagram



W DATA 1 P ← T

W DATA 2 R ← T

W DATA 7 V ← T

W DATA 6 W ← T

W DATA 5 X ← T

W DATA 4 Y ← T

W DATA 3 Z ← T

W DATA P M ← T

W DATA 0 N ← T

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Data Terminator, Type 3860-001B, Schematic Diagram

DUAL DENSITY 800/1600 CPI

ELECTRONICS SUPPLEMENT

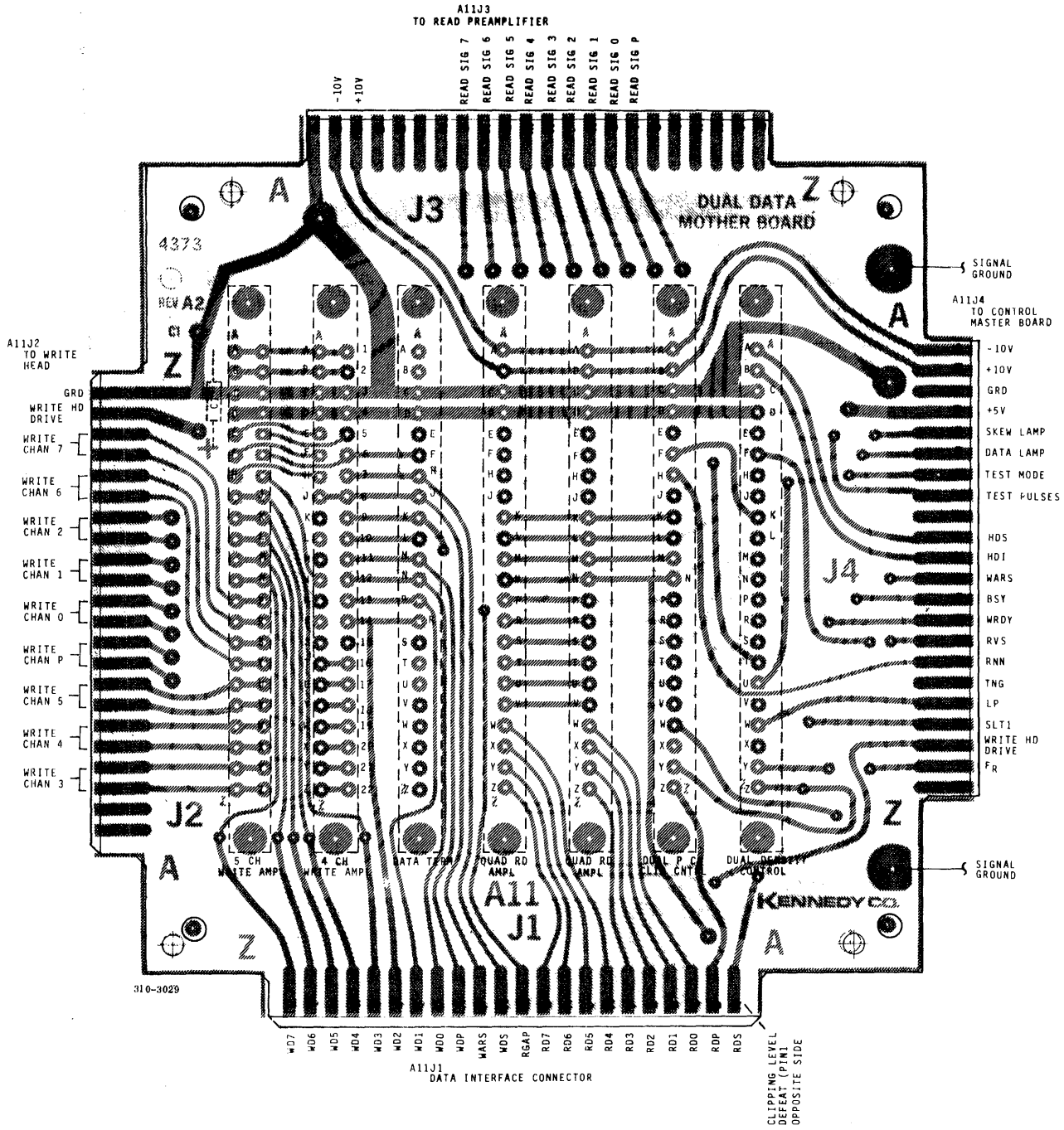
MODELS 9000/9700/9800

Your model includes dual density data electronics for processing nine-track 800 cpi NRZI and 1600 cpi phase encoded data. The new data electronics include the following modules:

Location	Type	Function
1	4365	Dual Density Control
2	6367	Dual P Channel/Clipping
3	6385	Quad Read Amplifier
4	6385	Quad Read Amplifier
5	3860	Data Terminator
6	4366	Four-Channel Write Amplifier
7	4368	Five-Channel Write Amplifier

These modules replace the following NRZI modules:

Location	Type	Function
1	3845	Timing Delay
2	4179	Read Amplifier/Clipping
3	4178	Quad Read Amplifier
4	4178	Quad Read Amplifier
5	3860	Data Terminator (no change)
6	3848	Four-Channel Head Driver
7	3849	Five-Channel Head Driver



Type 4373 Dual Density Data Master Board

TYPE 4365 DUAL DENSITY CONTROL

CIRCUIT DESCRIPTION

This module performs the following control functions:

a. Generates the read clock, supplies the READ REGISTER RESET signal to the NRZ1 data registers, and detects excessive skew

b. Detects the interrecord gap

c. Provides the interlocks required for the density selection

d. Supplies the reference frequencies for the write test

These operations are described below.

READ CLOCK, REGISTER RESET, AND SKEW DETECT NETWORK

The read clock and its related functions are performed as a function of a crystal generated master clock. The clock is produced by a master oscillator consisting of crystal Y1, transistors Q1 and Q2, and capacitor C4, connected in a feedback loop. The output clock of the oscillator is a square wave with a frequency equivalent to 64 times the 800 cpi data rate. (The master frequency is divided by two in transports with running speeds slower than 25 ips, by connecting flip-flop IC16 in the network.) The master clock is supplied to a skew counter consisting of two divide-by-16 counters, IC14 and IC17, in tandem. The counter is preset to one of three counts, depending on the mode of operation, and then counts up to its maximum count. During a read mode the skew count is 29, or approximately 45 percent of the character time. During a read-after-write mode the skew count is reduced to 21 (by WRITE READY activating NAND gate IC5-6), or approximately 33 percent of the character, and during the read test mode the count is reduced to 8, or approximately 13 percent of the character space. The skew gate is shortened during the read test mode to enable accurate alignment of the read head with respect to the tape path using an 800 cpi skewmaster tape.

When the leading channel detects data it supplies $\overline{\text{DATA IN REGISTER}}$ true at input pin H, setting the D input of flip-flop IC16 high. The succeeding master clock pulse clocks IC16 to the set state, the Q output going high to enable the skew counter to count. When the counter reaches its maximum count, the CARRY output of IC14 goes high and sets the D input of the first IC9 flip-flop high. The next master clock pulse clocks the flip-flop to the set state, and its Q output goes high to generate the read clock pulse through NAND gate IC5-3 (since the $\overline{Q}$ output of the third IC9 flip-flop is still high). The duration of the read clock is equivalent to two master clock intervals; the third master clock toggles IC9-15 to the set state, its $\overline{Q}$ output going low to terminate the output READ CLOCK pulse. The fourth clock pulse following the completion of the skew count toggles IC9-7 to the set state, its Q output going high to supply a RESET READ REGISTER RESETR pulse. RESETR clears the NRZ1 data register portions of the read amplifier stages, setting the $\overline{\text{DATA IN REGISTER}}$ signals of all nine read amplifier stages false. RESETR is also generated when signal C goes low. This occurs when any one of the following conditions is true: the transport is deselected (SLT1 going false), BUSY goes true, LOAD POINT goes true, or HIGH DENSITY is selected. Any of these conditions would clear the NRZ1 read registers.

The fourth clock pulse following the skew count completion also sets the input of D type flip-flop IC11 high. On the fifth pulse that flip-flop is toggled to the set state, its $\overline{Q}$ output going low to enable one-shot IC12 at pin 9. If one of the channels detects an additional character at this time its $\overline{\text{DATA IN REG}}$ goes true again, is inverted by IC1-6 and triggers the skew one-shot IC12 at pin 10. The $\overline{Q}$ output of the one-shot supplies a pulse through inverter IC2-6 that is used to illuminate the test panel skew indicator.

GAP DETECTION NETWORK

A 12-character delay is provided between the last character of the block and the GAP DETECT indication. The gap detection is performed by a network including flip-flop IC11, divide-by-16 counter IC13, and NAND gate IC7-3. During the data block $\overline{\text{DATA IN REGISTER}}$ (a wire-OR'd signal supplied from the nine read amplifier stages) remains true; it is inverted twice by IC1-6, IC7-6 and keeps counter IC13 cleared until the end of the data block. Following the last character in the block $\overline{\text{DATA IN REG}}$ goes high and the direct-clear is removed from IC13. At this time the $\overline{Q}$ output of flip-flop IC11 is high, the flip-flop having been clocked to the clear state when $\overline{\text{DATA IN REG}}$ first went true at the beginning of the block. Counter IC13 is then clocked by Ct, an 800

cpi data rate clock supplied from the clock dividing network including IC15 and IC18. Twelve clock counts into the gap IC13 activates NAND gate IC7-3; the output of the gate goes low and direct-sets flip-flop IC11, the $\overline{Q}$ output of IC11 going low to lock the counter while the Q output goes high and supplies $\overline{\text{GAP DETECT}}$ true at output pin K. $\overline{\text{GAP DETECT}}$ remains true until either the beginning of the next block or until the transport is deselected (SEL A going false).

DENSITY SELECT CIRCUITS

The NRZ1 800 cpi mode is selected either when the transport is selected and on line (SLT1 true, activating OR gate IC19-3) or when the transport is in the test mode (TM true at input pin U), provided that LOAD POINT is false and that HIGH DENSITY SELECTED is also false. If these conditions are satisfied then NAND gate IC3-8 is activated, supplying NRZ1 true at output pin M to enable the NRZ1 portions of the data electronics.

The high density is selected whenever the interface supplies HIGH DENSITY SELECT HDS true at input pin A of this card, the transport is selected and on line (SLT1 true), and not in the test mode (TM false). When these conditions are satisfied NAND gate IC6-3 is activated, supplying HIGH DENSITY true HDENS at pin Y and $\overline{\text{HDI}}$ true at pin B. If in addition to the above conditions the $\overline{\text{BUSY}}$ and the LOAD POINT status lines are both false, AND gate IC19-8 is activated, supplying PHASE ENCODED $\overline{\text{PE}}$ true at output pin J to enable the phase encoded portions of the data electronics.

WRITE TEST FREQUENCIES

The reference frequencies $\overline{\text{TMX1}}$ and $\overline{\text{TMX2}}$ are 800 cpi data rate square waves, 180 degrees out of phase, used to alternately set and reset the write amplifier flip-flops to generate the NRZ1 write test mode all-1 pattern.

These frequencies are generated by the divider network including IC15 and IC18 counters, which divides the master oscillator frequency into the data rate clock Ct. Ct is then gated through two IC5 NAND gates, with the Qc output of IC15 used to invert the phase of one frequency with respect to the other. The two test frequencies are then gated through the IC4 NAND gates when the write test mode is selected, indicated by both TM and WRITE READY being true. The two frequencies are then output at pins F and E as TMX1 and TMX2 and are supplied to the write amplifier cards.

TYPE 6367 DUAL P CHANNEL /CLIPPING PC BOARD

CIRCUIT DESCRIPTION

This module contains the read amplifier stage for channel P as well as the automatic clipping level switching control. The operation of the read amplifier stage is identical to that of the read amplifier stages located on the 6385 Dual Density Quad Read Amplifier, and as described in the circuit description of that card. The generation of the clipping levels and their switching control is explained below.

The purpose of the clipping levels is to eliminate spurious baseline noise pulses, requiring the analog signal supplied from the read preamplifier to exceed a certain amplitude before it is detected by the read amplifier stages. Different clipping levels are used during different modes of operation. The lowest clipping threshold occurs during read only NRZI mode. This level is increased during read after write operations. During the gap the clipping levels are raised even higher to reduce the probability of detecting random noise. When an error is detected in a read only mode and the transport is commanded to backspace over the erroneous block and reread it, the clipping levels are switched automatically to maximize the recoverability of marginally recorded data. First the clipping levels are lowered to recover possible partial dropouts, and if the error is still detected the clipping levels are raised to eliminate possible high baseline noise spikes.

The main component used in producing the clipping level voltages is operational amplifier IC17. The output of IC17 is used as the negative clipping level, and is supplied to the P channel read amplifier stage on this card and to the read amplifier stages of the other channels through output pin R. Operational amplifier IC18 inverts the output of IC13, supplying the positive clipping level.

During the NRZI mode FET Q2 is turned off by Phase Encoded (PE) false. As a result, resistors R14 and R15 are included in the negative feedback loop of operational amplifier IC17. The +10v routed through resistor R11 provides the minimum input voltage to IC17, producing an output clipping level of approximately 0.4 volt. Other voltages are added to the input of IC17 through R16, R17, or R18, increasing the clipping level's amplitude as required by the particular mode of operation. Thus, during a read only operation, the voltage through R17 is combined with R11's voltage.

During a read after write mode, WRDY true at input pin J direct-sets flip-flop IC16-4. The Q output of IC12 then goes high to add the voltage through R18 to that used during the read mode. This increases the read-after-write clipping level.

During the NRZI gap, GAP DET true at input pin F supplied from the Dual Density Control module is inverted by IC4-6 to activate NAND gate IC9-8, which adds the voltage through R16 to that used during the read only mode.

During a phase encoded operation, PE/ true (supplied at pin L from the Dual Density Control module) turns FET Q1 on, in effect bypassing R17 in the feedback loop of operational amplifier IC17. This reduces the output levels during PE.

The automatic clipping level switching is provided by the network including flip-flops IC7, IC16, exclusive - OR gate IC12 and associated circuitry. The circuit is used as a direction reversal indicator, the Q output of IC7-5 going high whenever the direction of motion is switched from reverse to forward or forward to reverse. Whenever two RUN NORMAL (RNN/) commands are given in the same direction, the Q output of IC7-5 goes low. The two J-K flip-flops of IC16 are connected as a divide-by-three counter, to count the number of direction reversals. If an error is detected during the read mode and the transport backspaces over the erroneous block, the Q output of IC7-5 goes high, setting the J-K input of IC16-11 high. During the second reread of the block, IC16-9 is toggled to the set state by a pulse formed on the leading edge of the RUN NORMAL (RNN/) command. The Q output of IC16-9 high is inverted at IC13-4, grounding resistor R17. This reduces the clipping levels during the second reread of the block. If an error is still detected, counter IC16 moves to the count of 2, with the Q output of the second IC16 flip-flop going high and that of the first going low. As a result, the voltages through R17 and R18 are added to the clipping levels, to increase the clipping threshold. During the next reread the voltage through R17 would be removed, further reducing the clipping level. The cycle would be repeated on the subsequent reread attempt.

The automatic switching is disabled if the transport interface supplies CLIPPING LEVEL DEFEAT (RTH/) true at input pin N, provided that the transport is selected. This would activate NAND gate IC1-12, to clear the IC7 flip-flops and direct set IC16-4. BUSY (BSY/) true or WRITE READY (WRDY) true would have the same effect.

TYPE 6385 QUAD READ AMPLIFIER

CIRCUIT DESCRIPTION

This module contains four identical read amplifiers which detect, filter and digitize both 800 cpi NRZI and 1600 cpi PE read data. Two of the boards are employed in dual density transports to process the eight read data channels. The read amplifier for channel P is located on the Dual Density P Channel Clipping PC board. The operation of read amplifier channel A is explained below; the other read amplifiers operate identically.

NRZI Operation

Analog read data from the read preamplifier is input at pin E as SIG. Part of the signal is differentiated by resistor R2 and capacitor C1, then applied to the NRZI peak detectors IC10-9 and IC10-5. Part of the SIG input remains undifferentiated and is applied to the positive and negative clipper comparators at IC5-9 and IC5-5. Note that the output of all these comparators will be positive, since negative signal excursions are inverted at the comparator inputs.

The peak of the differentiated signal waveform exhibits a 90 degree phase advance with respect to the peak of the undifferentiated signal waveform at the clipper comparator outputs. This phase difference defines the length of the negative-going clock pulse applied to the NRZI read register, J-K flip-flop IC6.

During positive signal excursions, IC10-7 and IC10-12 go high, causing IC15-8 to go low. To eliminate spurious noise pulses, capacitor C6 delays the read signal. When the differentiated signal at IC10-9 passes the 0v reference point, IC15-8 goes high to eliminate spurious noise pulses. Capacitor C6 delays the signal slightly. Since this delay is a function of tape speed, the value of C6 varies accordingly. (See table on schematic.)

The low output pulse from inverter IC19-2 clocks NRZI Read Register IC6. The Q output at IC6-3 goes high, enabling NAND gate IC1 at pin 4. (NRZI signal at IC1-5 input remains true as long as the transport is selected, the tape is past load point and BUSY is false.) The low true digitized NRZI read data is output to the interface from pin Z.

When the NRZI read register is set, its Q/ output goes low, causing a low true DATA IN REGISTER/ pulse to be output to the Dual Density Control board. After an appropriate interval, a Reset Read Register (RESETR/) pulse will be clear the NRZI Read Register, making DATA IN REG/ false until the next NRZI read data bit is applied to the Read Register's clock input.

RESETR also pulses true to clear the NRZI Read Register when: LOAD POINT goes true, BUSY goes true, high density recording (PE mode) is selected, or the tape transport is deselected.

Incidentally, positive or negative NRZI excursions must exceed their respective clipping thresholds at IC10-10 and IC10-4. The purpose of the clipping levels is to eliminate spurious baseline noise pulses, requiring the analog signal supplied from the read preamplifier to exceed a certain amplitude before it is detected by the read amplifier stages. Different clipping levels are used during different modes of operation. The clipping level during a read only NRZI mode is 20 percent of the maximum peak-to-peak signal. During a read-after-write operation the clipping levels are raised to 33 percent of the maximum signal. During the interrecord gap the clipping levels are raised 7 percent higher than their values during the data block to reduce the probability of detecting random noise. When an error is detected in a read only mode and the transport is commanded to backspace over the erroneous block and reread it, the clipping levels are switched automatically to maximize the recoverability of marginally recorded data. First, the clipping levels are lowered to recover possible partial dropouts, and if the error is still detected the clipping levels are raised to eliminate possible high baseline noise spikes.

PE Operation

When High Density Status (HDS) true is output from the controller, PE true is generated on the Dual Density Control board and input on the Quad Read Amplifier at pin L. NRZI signal goes false, disabling the Q output of NRZI read register IC6 at NAND gate IC1-5.

To conform to the PE format, only positive PE read data excursions will be peak and threshold detected during a PE read forward operation. To accomplish this, AND gates IC15-9 is disabled by low signal from NOR gate IC21-1 to disable negative signal processing. Simultaneously, IC15-2 is enabled to pass any positive-going PE read data. During a read reverse PE operation, PE RVS goes true, enabling the negative transition processing gates and disabling the positive ones.

Note that the PE signal path to the DATA output now passes through NAND gate IC1-3. This gate is enabled at pin 1 because inverter IC19-2 goes high during each PE read data transition.

DUAL DENSITY WRITE SECTION

CIRCUIT DESCRIPTION

This is a composite schematic of the Type 4366A Four Channel Write Amplifier and the Type 4368A Five Channel Write Amplifier. Write channels P, 0, 1, and 2 are processed by the Type 4366A Write Amplifier, while write channels 3-7 are processed by the Type 4368A Write Amplifier.

WRITE AMPLIFIER OPERATION

Each write amplifier stage consists of two OR gates, an input buffer flip-flop, a delay counter, and a pair of drivers. The operation of the write channel P amplifier stage is explained; the other stages operate similarly.

Write data channel P signal from the transport interface is inverted and supplied to the J input of input buffer flip-flop IC8, as well as one input of OR gate IC7. Write data is processed differently, depending on whether the tape transport is operating in the PE mode or the NRZ1 mode.

In the NRZ1 mode, NRZ1 high from the Dual Density Control module is inverted and supplied to one input of OR gate IC7. During NRZ1 high, this gate will pass the NRZ1 data without inverting it. Each time the input NRZ1 data goes low, both the J and K inputs of the input buffer flip-flop are set high. The WRITE DATA STROBE (WDS) from the interface now toggles the input buffer flip-flop to the opposite state. Thus for each 1 input, a polarity transition is recorded on tape. When the input data is high, containing a logic 0, the J and K inputs of the buffer flip-flop are set low. Thus the flip-flop does not change states when clocked by the WRITE DATA STROBE.

In the PE mode, NRZ1 false is inverted, causing OR gate IC7 to become an inverter. Now the input buffer flip-flop stores the input logic states whenever clocked by the phase encoded 3200 fci WRITE DATA STROBE. In the PE mode the data lines are already encoded in the formatter.

The input buffer flip-flop will store the data until the delay counter of the respective stage reaches its maximum count. The delay counter of each stage digitally deskews the write data, using channel P as a fixed reference. Although the delay counter of channel P is permanently preset to the count of 8, the counters of write data channels 0-7 can be preset to any count, using switches to either ground or open their parallel inputs. These delay counters are clocked by a reference frequency (Cx) at approximately 80 times the 800 cpi data rate, 40 times the 1600 cpi data rate, or 20 times the fci rate. Generated by an oscillator circuit, this clock advances each delay counter from the preset count until it reaches the maximum count of 16. At this point the Q_d output of the delay counter will clock the respective output register flip-flop. This transfers data from the input buffer to the output of the amplifier stage, where a pair of drivers energizes the respective head winding.

Write data deskewing is performed by manually adjusting the switches of one channel at a time until the output of that channel, as displayed on an oscilloscope connected to the Read Preamplifier module, coincides with channel P. The write deskewing compensates for the physical displacement of the channels with respect to each other on the write head. The write deskewing procedure does not correct for the misalignment of the head with respect to the tape path. The delay counter switches are preset in the factory and normally their positions should not be changed unless the write head has to be replaced. In that case the new factory supplied head is provided with a tag showing the new delay counter switch positions, as required to compensate for the new head's characteristics. Should readjustment become necessary, follow the write deskewing procedure outlined in the maintenance section of this manual.

WRITE TEST MODE

When the transport is in the write test mode, input frequencies TMX1 and TMX2 from the Dual Density Control module alternately set and reset the input data buffer flip-flops of each write amplifier stage, generating the required NRZ1 all-1 test pattern on the tape. TMX2 true pulse also fires one-shot IC5. This disables WRITE AMPLIFIER RESET (WARS) from the interface, permitting the tape to be written on during the test mode without disconnecting the Model 9100 from the interface.

TYPE 4368A AMPLIFIER OPERATION

The operation of these write amplifiers is identical to that of the Type 4366A Four Channel Write Amplifier module described above.

Warranty

The Company warrants its devices against faulty workmanship or the use of defective materials (except in those cases where the materials are supplied by OEM) for a period of one year from the date of shipment to OEM, with the exception of ¼" cartridge products which are warranted for a period of ninety (90) days.

The liability of the Company under this warranty is limited to replacing, repairing, or issuing credit (at the Company's discretion) for any devices which are returned by OEM during such period provided that (a) the Company is promptly notified in writing upon discovery of such defects by OEM; (b) the defective unit is returned to the Company, transportation charges prepaid by OEM; and (c) the Company's examination of such unit shall disclose to its satisfaction that such defects have not been caused by misuse, neglect, improper installation, repair alteration or accident.

Kennedy Company is continually striving to provide improved performance, value and reliability in its products and reserves the right to make these changes without being obligated to retrofit delivered equipment.

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