Signature II

Kurz·Kasch, Inc.

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CONTENTS

I. — SPECIFICATIONS
SIGNATURE II

Data Probe

Indicators:	3 LEDS "0", "1", "P"
Duty Cycle:	DC to 100 MHZ
Pulse Stretch:	50 Ms
Threshold:	Single or Dual Selectable
Input Z:	"0">22k "1">83k
Tip Protection	150V, DC

Control Probe

Inputs:	Clock — White Start — Blue Stop — Yellow V. REF — Orange Ground — Black
Input Z:	>2 MEG For clock, start, stop
Input Protection:	150V, DC
Input FREQ:	>50 MHZ each channel
Logic Levels:	TTL — Automatic MOS — V. REF Adjusts
Pulse Edge:	Switch Selectable All Channels

Data Processor

Clock:	Up to 15 MHZ
Data:	Up to clock speed
Set-up Time:	15NS (data required to be valid at least 15NS before selected clock edge)
Hold Time:	0 NS
Accuracy:	100% probability on validating a data system $1.00 - \frac{\text{BIT ERRORS}}{\text{Bits Stream Length}} =$ probability of detecting a faulty data stream
Min Gate:	1 clock cycle
Min time between Last Stop & Next Start:	1 clock cycle

Power

120V 50/60 HZ @ 11.5VA
220V 50/60 HZ @ 9.5VA

Weight

Net: 5 lbs.

Dimensions

Case Closed: 5.5" H x 9.0" W x 9.0" D (max)

Environmental:

Temperature:	0 to 55 degrees C
Relative Humidity:	95% @ 40 degrees C
Case:	Drip proof

II. — SIGNATURE II
UNDERSTANDING ITS OPERATION

ROMs, RAMs, CPU's, data buses, all have one thing in common — they are difficult for the average technician to troubleshoot. Kurz-Kasch, Electronic Division, developed the Signature II system to solve this problem.

Understanding how it works is essential before using the Signature II system. (Figure 1 shows the system and its controls).

Main Logic Unit

The main logic unit contains the power supplies; on-off switch, 5V power LED, hexidecimal readouts, gate LED, error LED, self test button, glitch switch, and hold switch (model A only). (Figure 2 shows the circuits contained in the main unit).

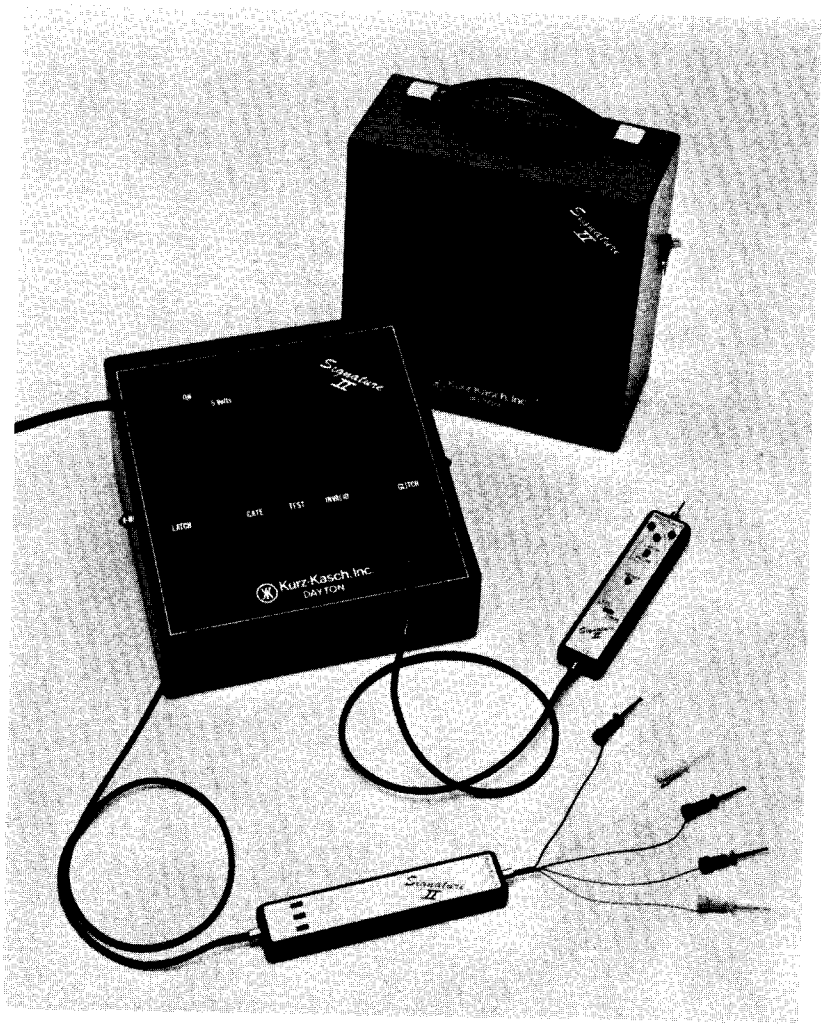


Figure 1

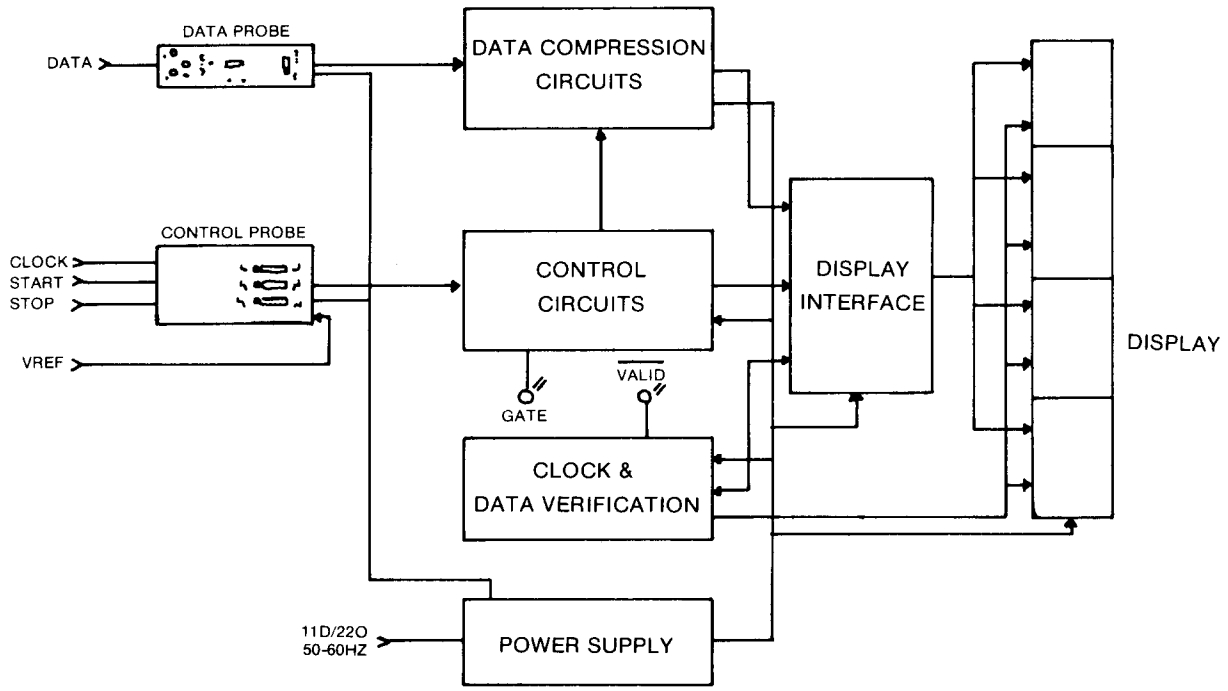
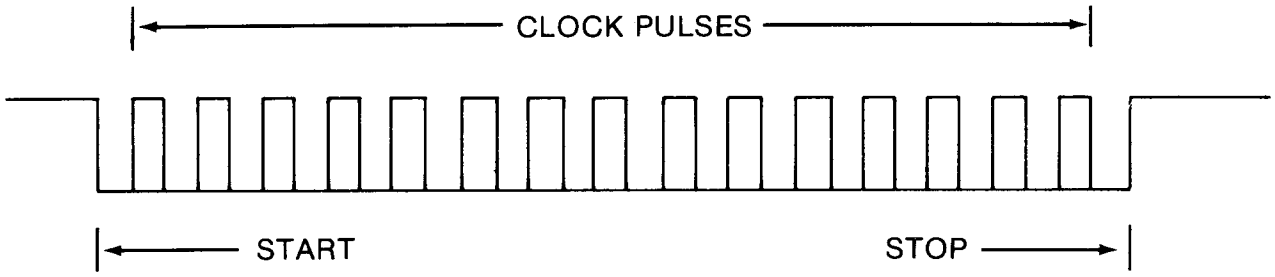


Figure 2



Here's how it works:

The control probe is connected to the start/stop and clock sources on the board to be tested. The start/stop pulse creates a window which enables internal circuits to accept clock pulses. These clock pulses allow acceptance of data bits (from the data probe) by the data compression circuits.

In the above sketch the start/stop control allows 15 clock pulses to be accepted. (In reality the system can operate with from 1 to in excess of 1 megabits of clock).

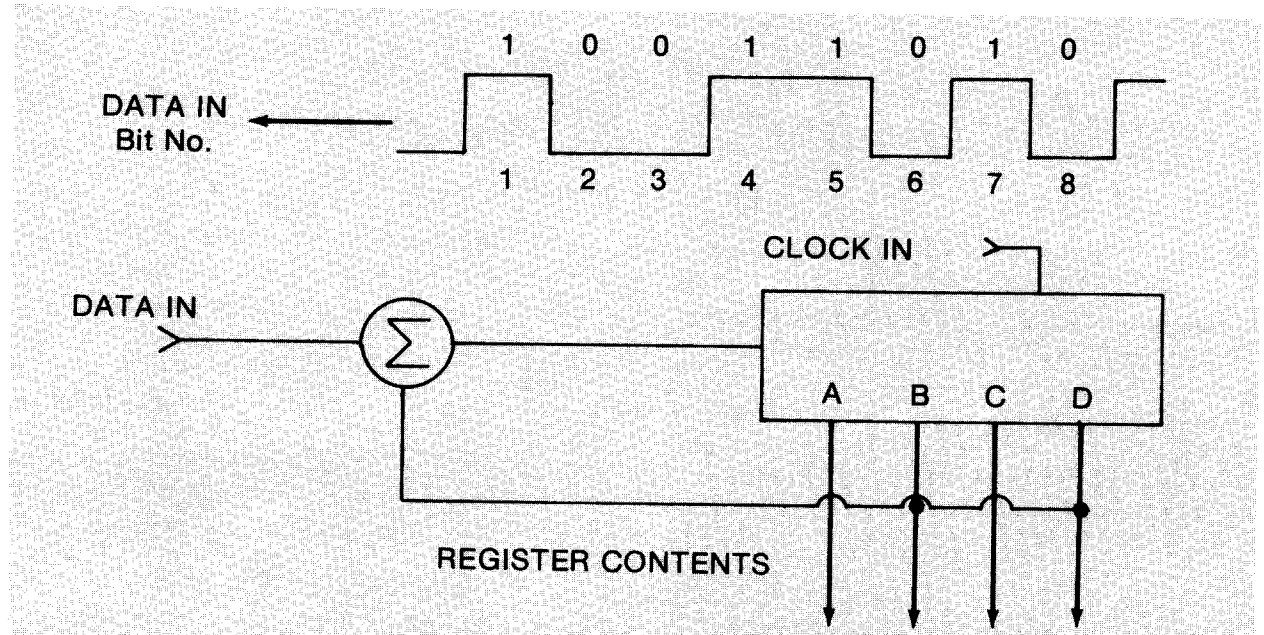
These 15 clock pulses allow 15 data bits to be clocked into the compression circuits. The compression circuits only accept data between the start/stop pulses. This being the case it can be said that 1 data bit or as many as a megabit can be clocked in. These are compressed to 16 bits. These 16 bits are further compressed to 4 bits. The bits are used to address a decoder ROM. The ROM Data output is further decoded to give 4 four bit hexidecimal words. The 4 words have **NO SIGNIFICANCE AS TO THE DATA WORDS CLOCKED IN.** In other words, no displayed word is the computer word or word the Signature II system saw.

To simplify the explanation, lets look at a 4 bit compression circuit. We will clock in 8 data bits and see what is left in the register to display. (Figure 3).

As you can see, after we clocked in 8 bits, two words 1001 (9) & 1010 (A), there remained 4 bits 0011 the word 3.

The only difference between the above example and the Signature II is the quantity of bits of both clock and data that are processed.

The modified hexidecimal words used by the Signature II are:
0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, C, F, H, P, & U.



DATA	CLOCK PULSE #	A	B	C	D
—	0	0	0	0	0
1	1	1	0	0	0
0	2	0	1	0	0
0	3	0	0	1	0
1	4	1	0	0	1
1	5	0	1	0	0
0	6	0	0	1	0
1	7	1	0	0	1
0	8	1	1	0	0

Figure 3

There are a couple of other circuits which are interesting. One is the Gate. The Gate circuit LED indicates that clock and start/stop pulses ARE VALID.

The second circuit is the DATA INVALID. This is a bit more complicated, but easily understood. It works this way — When the stop pulse is received by the compression circuits all activity within these circuits cease. The compressed data stream, now 4 bits in length are stored in a RAM and at the same time they are decoded and displayed. When a new start pulse is received, the data stream is again compressed until another stop pulse is received. At this time the same (or new words) are displayed and moved to storage. The first words and the last words are taken from storage and compared. If they are in any way different, the INVALID LED will flash. Remember that 1 data bit error will cause the 4 displayed words to be entirely different. When the glitch switch is activated a single or multiple bit error will cause the INVALID LED to remain on.

Control Probe

The control probe consists of 3 level detectors automatically toggling either TTL or MOS levels set by the "V REF" E-Z Hook or the internal 5V TTL levels.

Each of the 3 channels will accept pulses as fast as 20 NS.

Leading edge or trailing edge pulse selection located on the control probe, can be made by moving the appropriate selector switch for either start, stop or clock.

The "V REF" input is used to automatically set the reference level for C-MOS. If your C-MOS circuits are operating from a VDD of say 10 Volts, then the Control probe reference levels are set to 10 volts internally. With "V REF" not connected, the system is automatically set for 5 Volt, TTL or compatible C-MOS.

Data Probe

The data probe, which is a part of Signature II, is a 10 NS logic probe. This is a dual threshold probe — has memory (latch) and independent LEDS for "0", "1", & "P". All three LEDS work full time and display hi's, lows, & pulses from DC to 100 MHZ. This is truly a 10 NS probe and can be used independently if the control probe ground is connected to logic ground.

The reset button on the probe is to reset the registers, latches and displays in the main logic unit to all Zero's.

Duty cycle is displayed by the LEDS from DC to 100 MHZ. Duty cycle is the relative intensity of the "0" & "1" LEDS. Equal intensity is a 50% duty cycle. A "0" or "1" LED will begin to glow at a 20:1 duty cycle. You can see 10 NS pulses spaced 200 NS apart. At a 20:1 duty cycle one LED will be full brilliance and the other one will just begin to glow.

Self Test

To self test the Signature II, connect clock, start, stop and ground to the proper places on the logic board to be tested per software. **NOTE:** "Gate" LED must be on.

Touch data probe tip to ground — Signature II should read **0000**. Touch data probe tip to VCC. Signature II should read the VCC notation on software of board to be tested. While touching VCC push "TEST BUTTON" and readout should be **UUUU**.

During all tests the INVALID LED should only flash on touch, unless the Signature is unstable or remain on if glitch switch is on.

If Signature II passes all the above tests you can be sure the system is working.

Some Signature Indications & What They Can Mean:

A 0000 Signature at a logic node means a short to ground or a stuck at "0" device.

A VCC Signature at a logic node means a short to VCC or a stuck at "1" device.

Two address or data buses with the same but incorrect Signature indicates these two lines are shorted together.

Unstable Signatures where they should be stable, could be improper start, stop, clock or ground connections. "Dirty" power supplies or ground loops can cause instability.

Whenever wrong Signatures or unstable ones are observed, recheck the 3 switches on the pod. They should be in the position indicated by the software.

Remember Murphy's Law — "The least suspected error is probably the fault".

With the threshold switch in "Dual" mode absence of a pulse light on the probe indicates a faulty or tri-state mode if the Signature is other than 0000 or VCC.

III. — MAINTENANCE

Signature II is a very high performance piece of equipment. For this reason the original configuration, both electrical and mechanical, must be preserved.

Should a failure occur it would be best to return the Signature II to the factory. If this is not practical, parts replacement in the field can be made. There are a few components which affect the operation and these must be replaced with factory produced or selected ones. These critical components are listed below.

Under no circumstance should the cables be either shortened or lengthened. All other parts are standard and should be available from your normal supplier.

SYMBOL	DESCRIPTION	KK PART NO.
U-1	IC	0500016
U-4	IC	0500023
U-10, 19	IC	0500017
U-12	IC	0500018
U-14	IC	0500019
U-17	IC	0500020
None	Cable (POD)	0860014
	Cable (PROBE)	0860014
None	FET (3 Req.)	0480025
T1	Transformer	0570010
None	Operating Instructions	1670038

IV. — ASYNCHRONOUS COUNTERS

Any system which can be made repetitive is a candidate for Signature II.

Bit errors, glitches, or other digital ills can be isolated with Signature II in a minimum of time using technicians without extensive training. Usually, an hour or less to familiarize oneself with this new system is all that is required. The technician or engineer can isolate the failure mode without the use of schematics, flow charts, or look-up tables.

The only requirement for use of Signature II is that the data be repetitive. A system designed with Signature II in mind is obviously more flexible but almost all existing systems are adaptable.

An asynchronous counter or system is one in which the logic circuits changes states at arbitrary instants of time determined by the propagation delays through the system components.

The main thrust of this paper addresses itself to the many systems already in existence and crying for solutions to laboratory and field problems.

If one can understand the methods of causing repetitive bit streams in existing equipment then new designs will come easily.

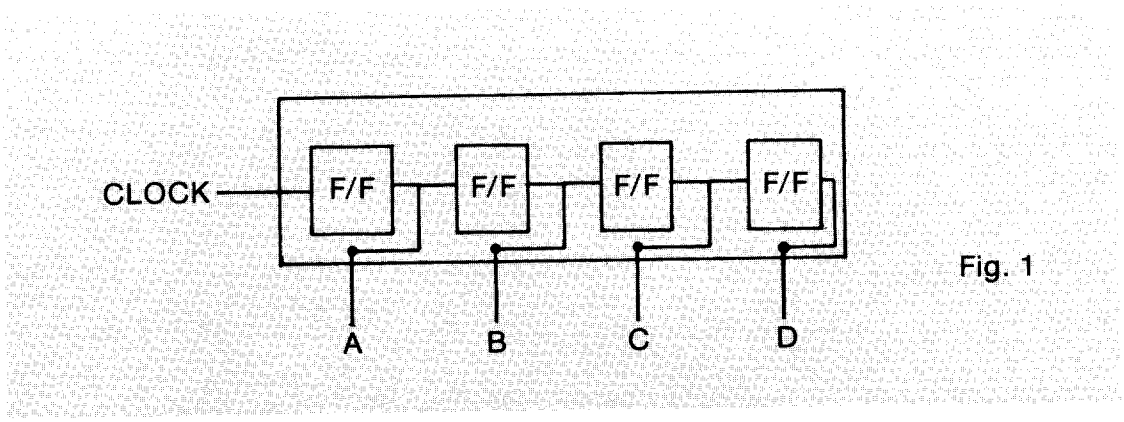


Fig. 1

An asynchronous type counter is one shown in Figure 1. These are typically the 7490, 7492, 7493 types wherein the first flip-flop is clocked which in turn clocks flip-flop #2, which clocks #3, etc. A typical 7493 which is clocking can have a "D" (most significant bit) output delayed greater than the width of the clock pulse. For this reason, asynchronous counter chains should be checked not over two counters at a time.

How do we check them? A simple rule applied here and in all future Signature II set-ups apply.

1. Signature II clock-to-counter clock input.
2. Start/Stop to **most significant bit** of counter **that is used.**

We emphasize "most significant that is used" because an unused output may be noisy or not terminated (no pull-up). Eratic or unstable signatures can result.

To obtain signatures or to test an asynchronous counter, Figure 2 shows the connections and signatures to be expected.

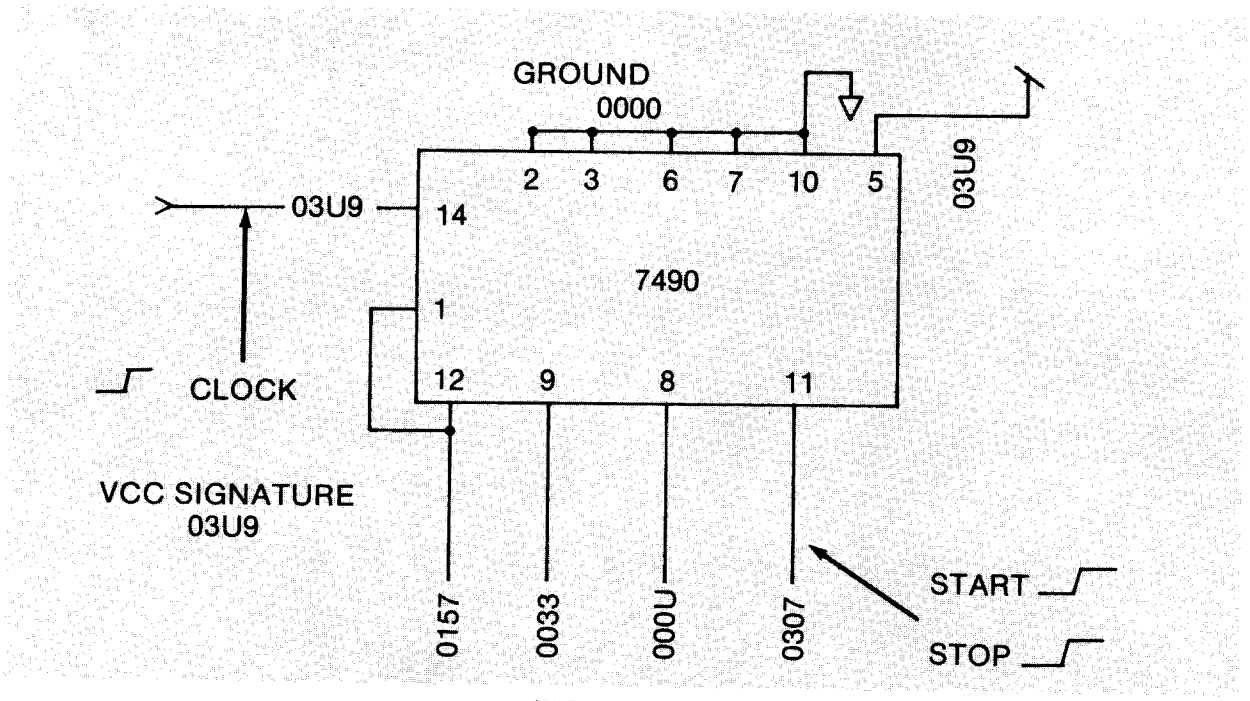


FIGURE 2

As shown in Figure 2, the Signature II clock is connected to the counter clock input, start and stop to the most significant bit of the counter, pin 11, "D" output.

When obtaining signatures to be later used, the first signature to be taken after the Signature II connections are determined is VCC. Touch the data probe tip to VCC. Recording this signature along with the connection information will insure later connections are correct.

SUMMARY

To obtain signatures from asynchronous counter systems follow these rules:

1. Clock input of Signature II connected to clock input of counter under test.
2. Start and stop of Signature II to most significant bit that is terminated. Do not have clock & start/stop separated by more than 2 IC's.
3. Ground of Signature II at point as close to clock input as is practical.
4. Select and record pulse edge used for clock, start, and stop.
5. Record VCC signature.
6. Record signatures at counter or any point in system fed by this counter.

V. — SYNCHRONOUS COUNTERS

A synchronous counter or system is one in which the logic circuits changes state only at certain instances determined by a common clock.

Figure 3 is a typical synchronous counter. A 74161 or 9316 is an example of this type of counter.

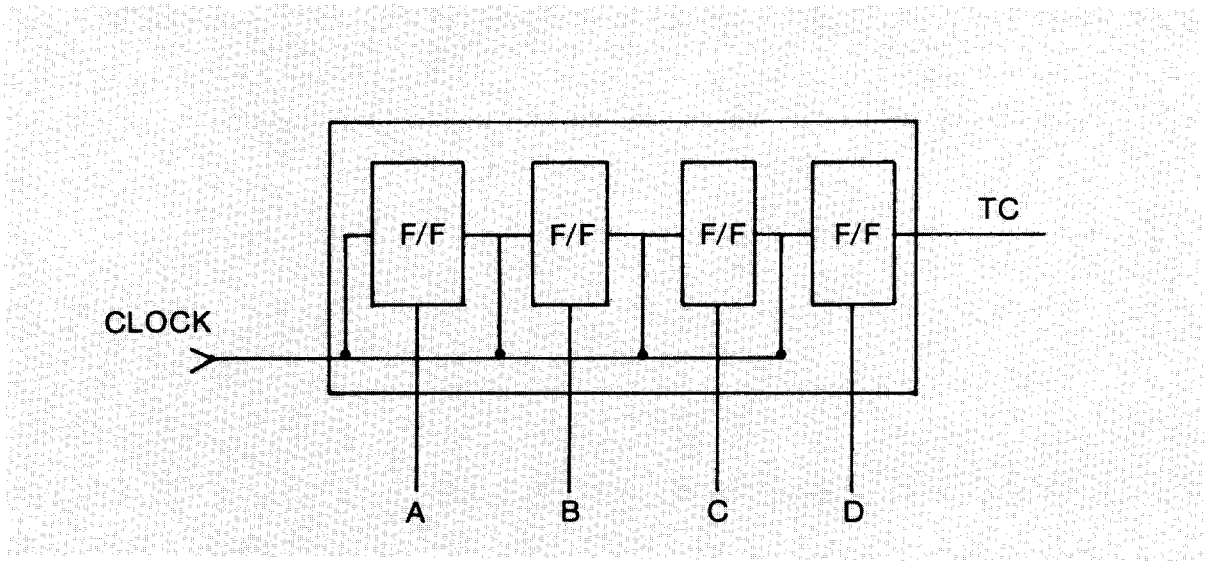


FIGURE 3

The significant difference between an asynchronous and a synchronous counter is the clocking. In Figure 1, in an asynchronous counter, the clock is applied to the first flip-flop which in turn clocks #2, etc. Figure 3 shows the clock being applied simultaneously to each of the flip-flops (synchronous).

Signature II connections to this type of counter or counter chain is no different than with an asynchronous counter. Clock goes to Signature II clock input and the most significant bit — That Is Used — is the start/stop input to Signature II. The connections and signatures to be expected for a single 9316 are shown in Figure 4.

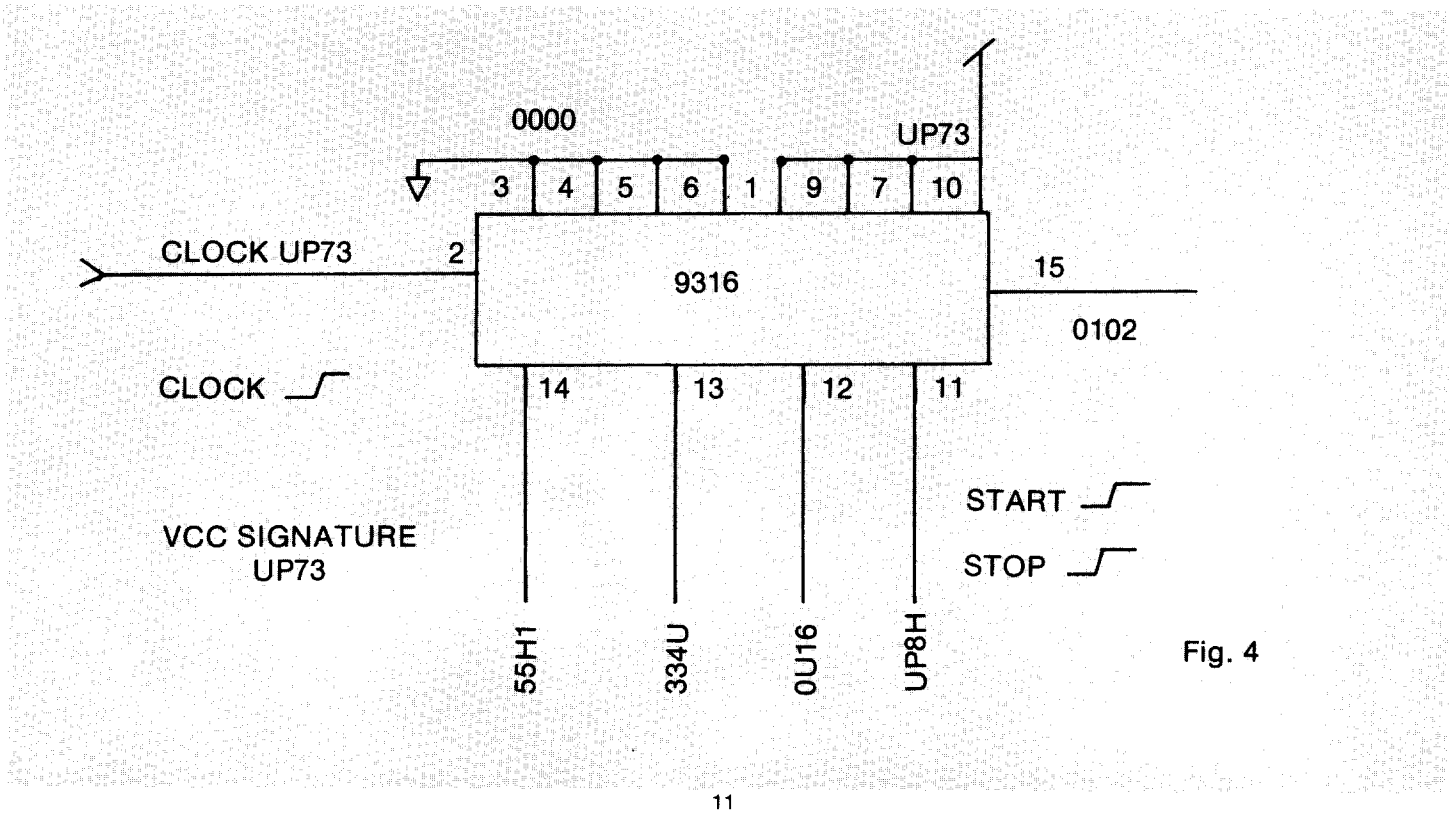


Fig. 4

Again as with the asynchronous counter and with any initial signature recording, the first signature to be taken and recorded is VCC. This assures that the counter is operating and that the start, stop, and clock inputs to the Signature II are properly connected.

As you will have noticed nothing has been said about clock frequency. As long as the clock is a relatively clean square wave the Signature II is independent of clock frequency within the clock specifications. The limiting factor generally will be the logic speed.

Before we leave the counters let us look at a counter chain consisting of 3 each 9316's. The schematic in Figure 5 is the one used in the final test for Signature II. The clock is 15 MHZ.

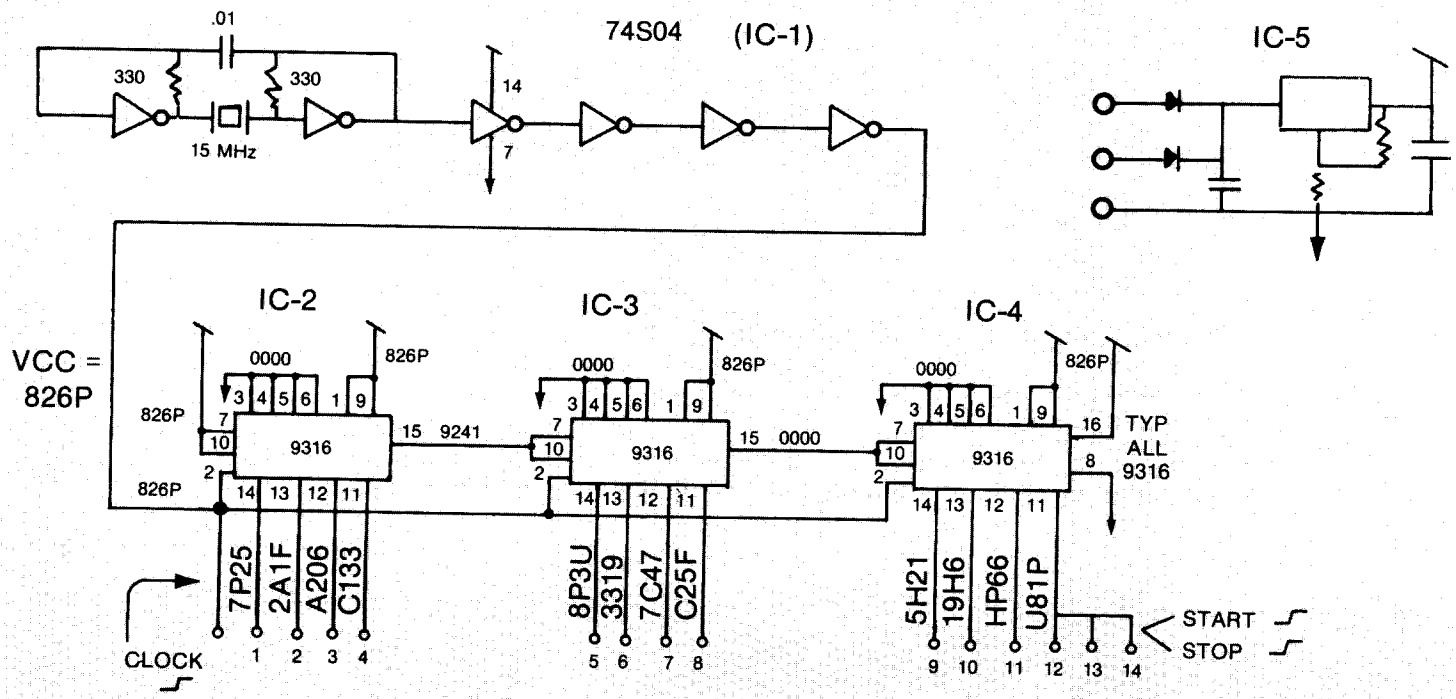


FIGURE 5

Clock is the 15 MHZ square wave from the 74S04 connected to all pin 2's of the 9316's. Start/stop is connected to pin 11 of IC-4. This is the most significant bit of the counter chain.

VI. — VCC SIGNATURES FOR COUNTER CHAIN

There is another technique, other than shown in sections I and II, to check a counter chain. Figure 6 shows how this is done and the signatures to be expected.

Clock input to the Signature II is the same — first counter or system clock. The data probe tip is connected to VCC and the start/stop inputs are connected together using a probe shown in Figure 7. The new probe tip (Figure 7) then is touched to the counter outputs (pins 14, 13, 12, 11, & 15). The VCC Signatures will be as shown in Figure 6.

This system is very useful if a counter output is stuck high, low, or to another line on the logic board.

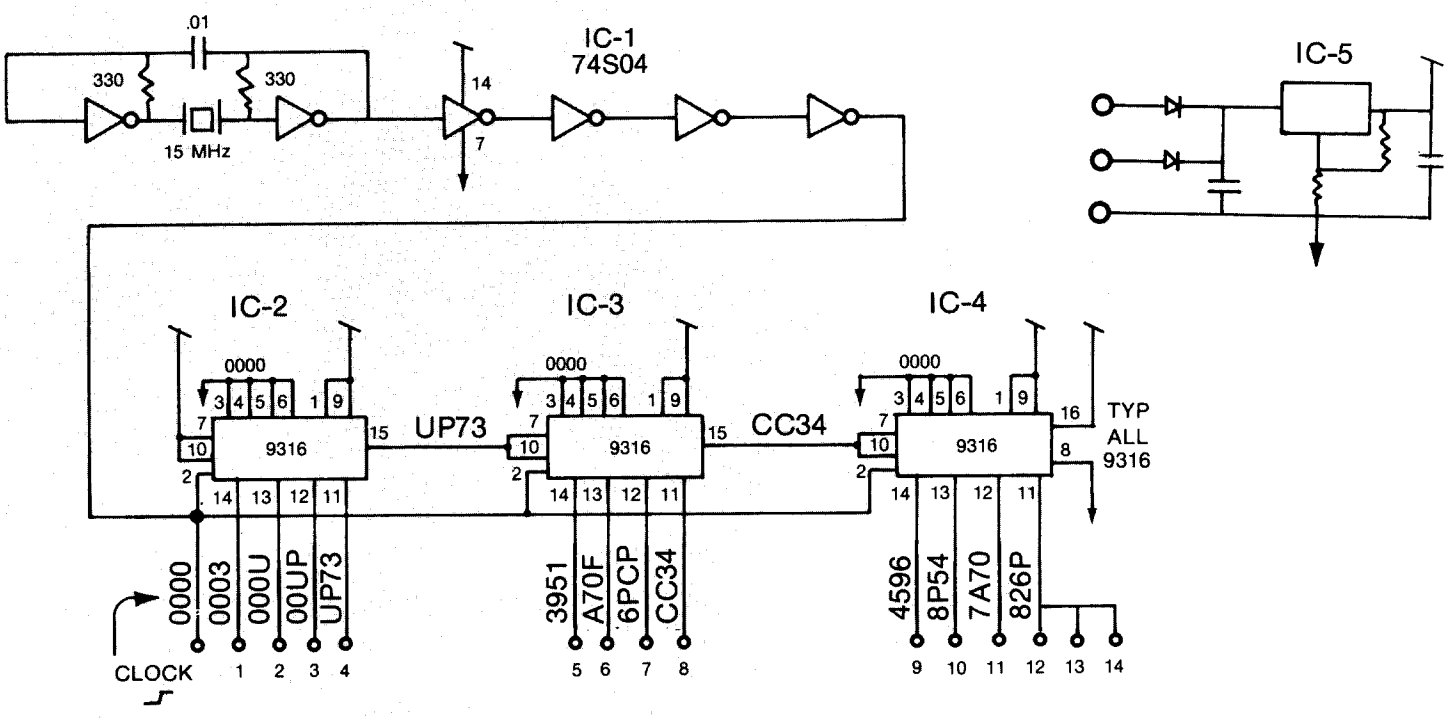


FIGURE 6

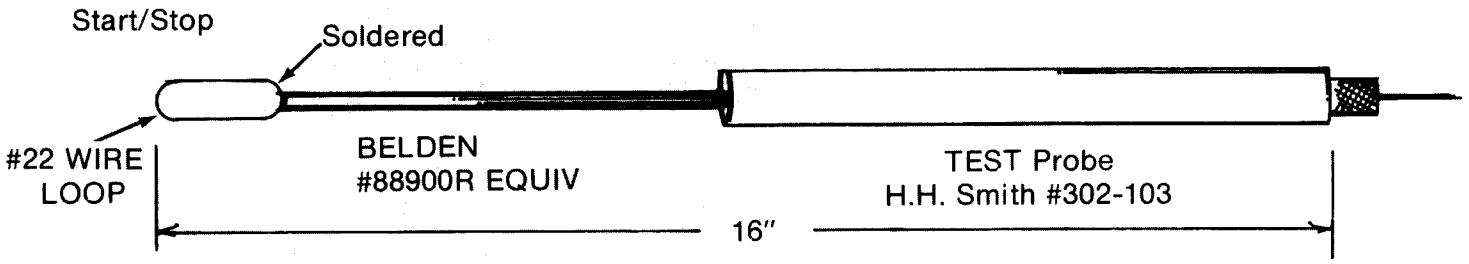


FIGURE 7

VII. — PROCESSORS (CPU)

If a CPU has an instruction forced into its data bus called a "NOP" (No operation) the CPU will become a 16 bit synchronous counter. The 16 counter outputs are the address lines A_0 thru A_{15}.

The instruction sets for the various CPU's will give the machine language for the NOP. Here are the ones for the most popular CPU's:

CPU	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
6502	0	1	0	1	0	1	1	1
6800	1	0	0	0	0	0	0	0
Z-80	0	0	0	0	0	0	0	0
8080	0	0	0	0	0	0	0	0

This NOP instruction causes the program counter (PC) to be advanced (incremented) 1 count each instruction fetch.

If a processor system were designed for Signature II the system would look something like Figure 8.

In computer terminology the largest numbered bus lines are the most significant ie: D^7 is the most significant of D^0 to D_7, A_{15} is the most significant of the address lines A_0 to A_{15}.

As in Figure 8 we can cause a processor to "free-run" or to act as a 16 bit counter by use of an 8 pole double throw switch. The same results could be obtained by installing an IC socket in the data bus. A header could be inserted with either a wired feed through or a wired NOP instruction.

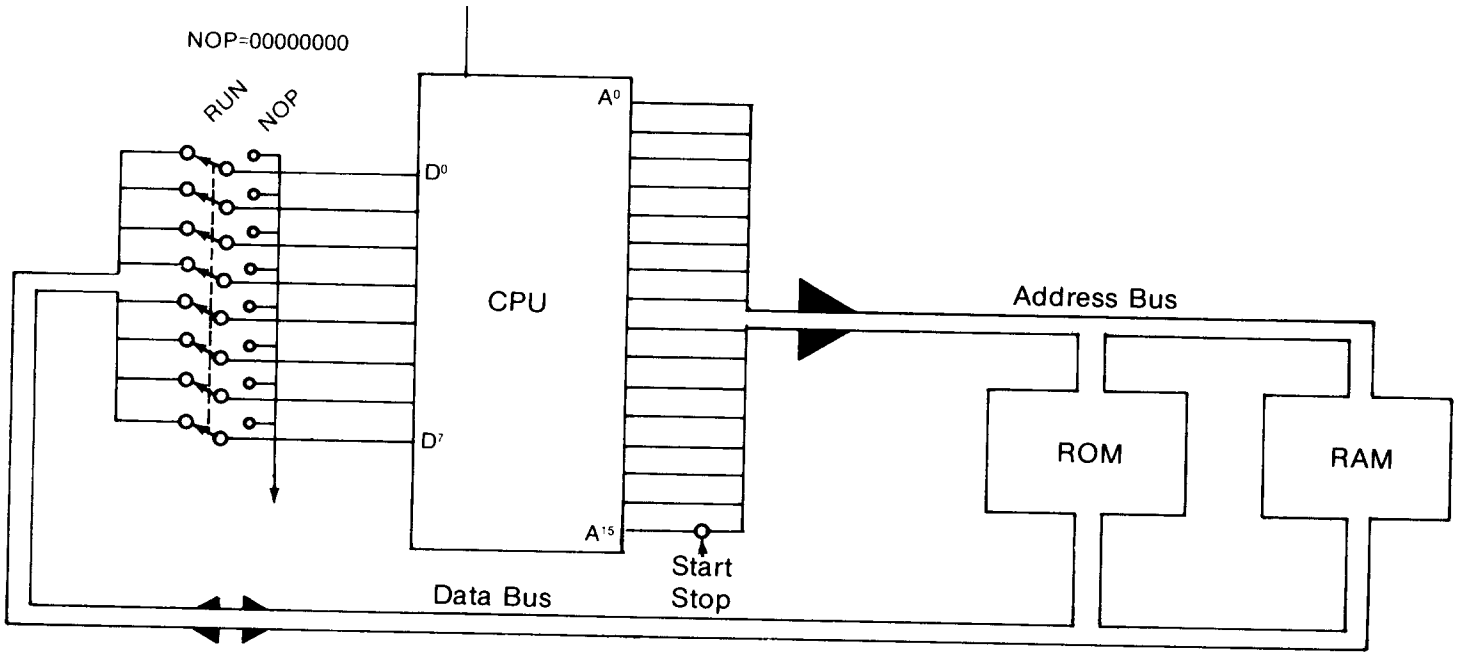


FIGURE 8

Unfortunately all bus oriented systems are not designed for Signature II systems. Let this not deter you. There are several ways to accomplish the task.

1. Data bus with bus drivers hardwired. (Figure 9)
2. NOP test fixture. (see Figure 10)

Where tri-state bus drivers are used the data bus can be opened by forcing the enable input to the proper logic level.

For example a 74LS245 pin 19 is the "ENABLE G". This means that pin 19 must be low for the drivers to operate. If pin 19 is taken high then the data bus is effectively "cut loose" from the CPU.

A word of warning — NO LOGIC GATE OUTPUT CAN BE TIED HIGH. The enable comes from some gate output. Since this input cannot be tied high check the source of this logic level. The chances are good that there is an invertor feeding this enable line. If it is, then the invertor (or NAND/or NOR) input can be pulled low making the "ENABLE G" go high.

Once the buffer or bus driver has been forced to the isolation mode then a test clip such as the Kurz Kasch TC-590-89 or one of the AP Product "TC" series is placed on the bus driver or drivers and the CPU side of the bus can be hard-wired for the proper NOP instruction.

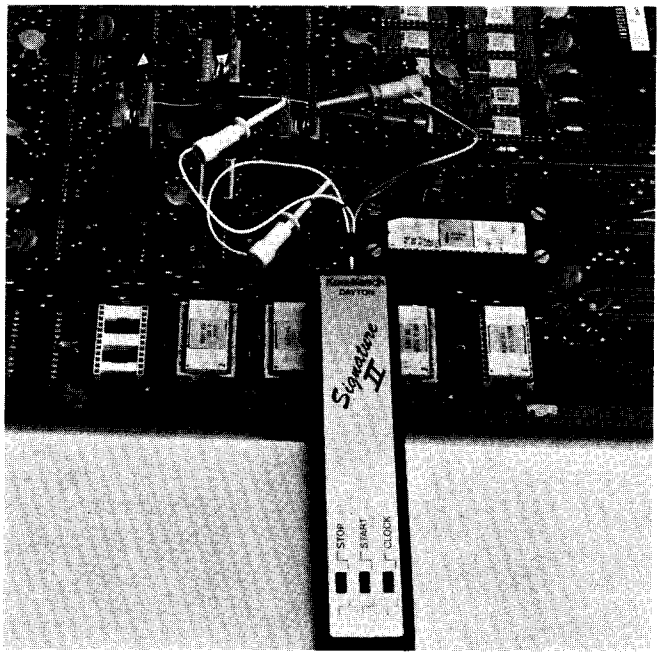


FIGURE 9

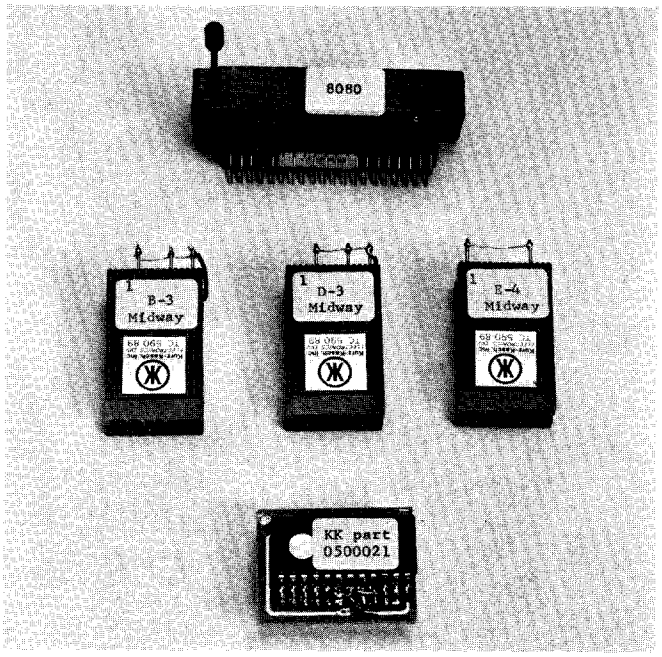


FIGURE 10

Some of the common bus drivers (buffers) and their control inputs with the levels to cause isolation are:

IC	PIN	LEVEL
8T09	2, 4, 9, & 12	1
8T26	15	0
8T28	1 & 15	0
74LS245	19	1
8216	15	1

To hardwire the test clips for an 8216 pins 3, 6, 10, & 13 are connected together then connected to pin 8 (ground). This would give the NOP code for an 8080. (Of course two 8216's are used to obtain 8 drivers, necessitating two test clips be hardwired).

A WORD OF WARNING

NEVER POWER UP A LOGIC BOARD WITH HARDWIRED TEST CLIPS ON THE DRIVERS WITHOUT THE DRIVERS FORCED TO THE ISOLATION STATE.

The second way to isolate the CPU data bus from the outside world is for a NOP test fixture be made. Figures 11 & 12 show how this can be done.

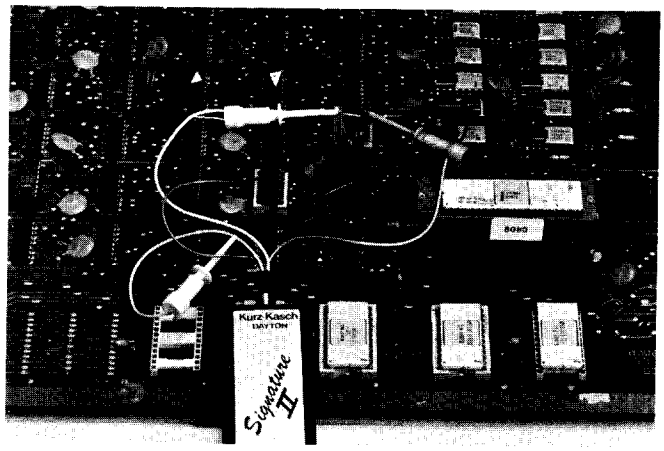


FIGURE 11

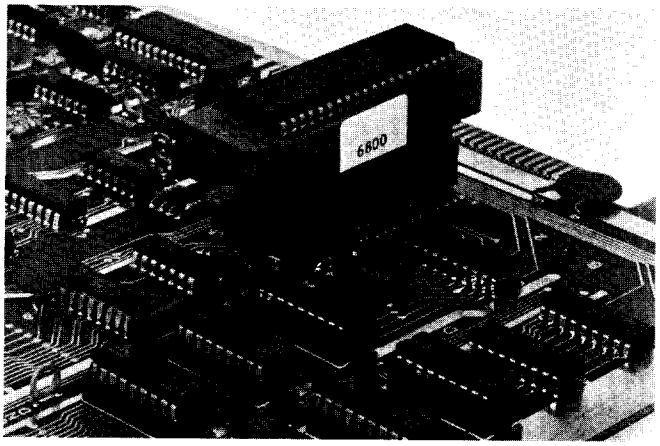


FIGURE 12

CLOCK FOR CPU

We now know how to cause the CPU to become a counter and know to connect start/stop to the highest order address line. (Most significant bit of the CPU counter A-15). Be sure to use the highest order address line that is used.

The clock to be used for the clock input to the Signature II is a bit more difficult to select. With the NOP fixture, clock is designated in Fig. 14 for the four CPU's most commonly used.

The 8080 uses a 2 phase clock neither phase alone is suitable for the system clock. From the timing diagrams for the 8080 we find the address bus and the data bus are both stable when ϕ (phase 1) and sync (pin 19 of the CPU) are both high. If we AND both ϕ & sync we will have what we need. Some processor systems perform this AND function as the **system time base.** If it is not already done for you, an AND gate can be added to a NOP test fixture or a 74LS08 could be piggy-backed on an IC that has either ϕ or sync as an input or output.

The 6800 CPU, pin 37, ϕ 2 is stable for the Signature II clock if the trailing edge of the clock is used.

For Z 80 use pin 21, RD, leading edge for clock and start/stop trailing edge for addresses.

The 6502 clock ϕ 2 is used as clock input to Signature II.

For other microprocessors consult the CPU timing diagrams or contact Kurz-Kasch.

Since the NOP (PC+1) repetitively runs through all possible addresses a signature from each address line can be obtained. These addresses will follow paths throughout the system. In other words A12 signature at the processor can be traced with the data probe from the processor to its termination, including all branches. ROMS, RAMS, MUX, IO'S, etc. can be tested both inputs and outputs as long as they are addressed by the CPU.

A known good board or system must be probed and VCC signature along with signatures at chosen points be recorded. All future checks on like boards or systems must produce the same signatures. A different signature is indicative of a failure node. Figure 13 shows signatures for the four most common CPU's.

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SIGNATURE II MANUAL

CPU NOP FIXTURE CONNECTIONS

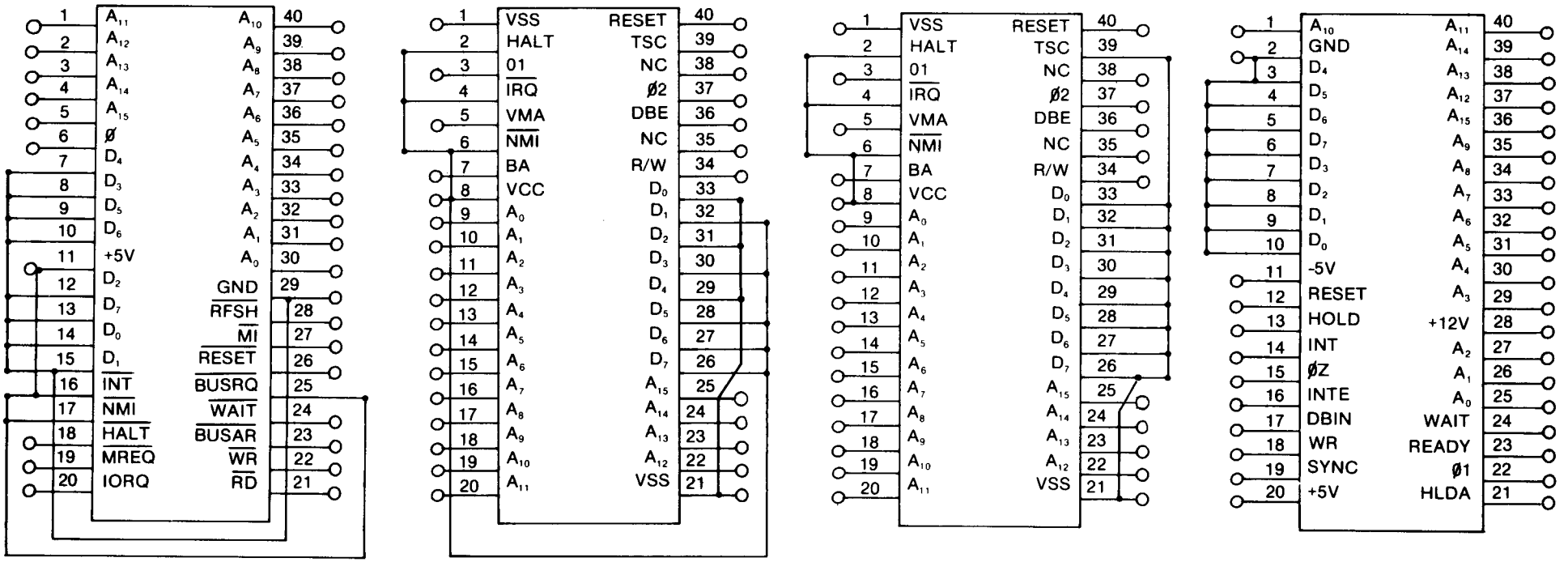

FIGURE 13

O- THESE PINS CONNECT DIRECT FROM LOGIC BOARD CPU SOCKET TO FIXTURE SOCKET PINS WITHOUT O- ARE INTERCONNECTED AS SHOWN. THESE PINS ARE NOT CONNECTED TO LOGIC BOARD CPU SOCKET.

Kurz·Kasch, Inc.
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June 1, 1979

Dear Signature II Owner:

The Signature II Data probe has a "dual threshold pulse circuit*," incorporated. This feature is exclusive to the Kurz-Kasch, Inc., logic probe and the Signature II Data Probe. It will give you another dimension in trouble-shooting. It functions differently than our previous probes and everyone elses, too. It is included at no additional cost because we are constantly striving to make our product more useful to you.

You will notice a switch at the rear of the label. This switch in the "single" position allows your probe to operate as a "single threshold" probe (just like the old ones). When the switch is in the "dual" position, your probe becomes a "dual-threshold" probe.

To explain the operation of this feature consider Figure 1, and how all previous logic probes operated.

All probes prior to this unit will illuminate the pulse indicator when either threshold (0.8V or 2.4V) is crossed.

FIG. 1

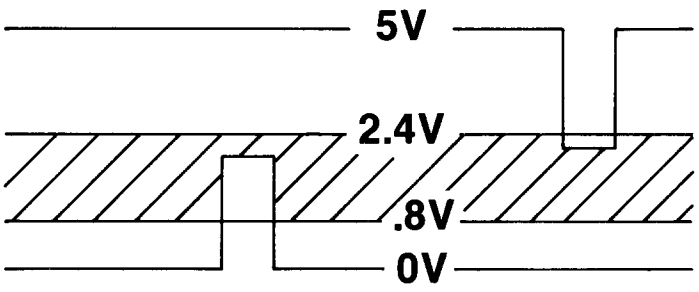
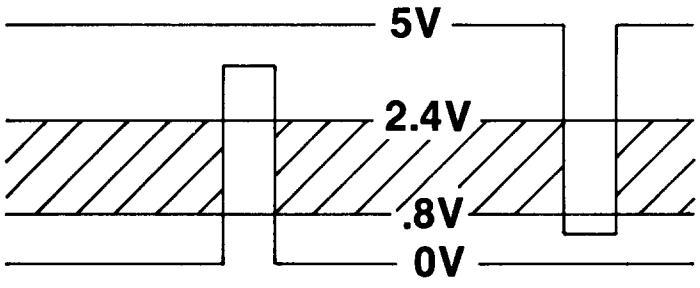


FIG.2



Now refer to Figure 2, to see how the new probes operate.

You must cross both thresholds (0.8V and 2.4V) to cause the pulse indicator to light. The obvious benefit to you, the pulse must be of a VALID logic level in order for the pulse lamp to illuminate. No longer can glitches or small pulses or noise cause the pulse indicator to light. Only VALID pulses will properly operate your probe and cause the pulse indicator to light.

The Dual Threshold Mode has another benefit, and that is the transition across both thresholds must be accomplished within 35 NS. A rise or fall time out of spec will be indicated by a lack of pulse light in the D.T. Mode. When you have a "0" and "1" indication and no pulse indicating then you know the transition time is greater than 35 NS. Since Cmos is generally much slower than this it should be tested in the "single" mode.

*Pat. No. 4110687

NOP FIXTURE SIGNATURES
FOR PROCESSORS

PROCESSOR	Z-80		8080		6502		6800
CLOCK	PIN 21		PIN 17		PIN 37		PIN 37
START/STOP	5		36		25		25
GROUND	29		2		21		21
A0	30	UUUU	25		9	UUUU	9
A1	31	5555	26		10	FFFF	10
A2	32	CCCC	27		11	8484	11
A3	33	7F7F	29		12	P763	12
A4	34	5H21	30		13	1U5P	13
A5	35	0AFA	31		14	0356	14
A6	36	UPFH	32		15	U759	15
A7	37	52F8	33		16	6F9A	16
A8	38	HC89	34		17	7791	17
A9	39	2H70	35		18	6321	18
A10	40	HPP0	1		19	37C5	19
A11	1	1293	40		20	6U28	20
A12	2	HAP7	37		22	4FCA	22
A13	3	3C96	38		23	4868	23
A14	4	3827	39		24	9UP1	24
A15	5	755P	36		25	0002	25
VCC		0001				0003	

FIGURE 14

VIII. — ROM TESTS

Once the processor is in the NOP condition the address bus starts with all address lines at "0" at reset. The 16 addresses count binarily to all "1's". Any ROM on the address bus will have all its addresses exercised repetitively. ROM data will be output in a serial stream on each of the ROM data lines. A signature will be obtained for each data line and will be repeatable. Any deviation from the signature obtained from a good ROM indicates a defective device.

Chip enables, in multiple ROM banks are extremely useful in isolating which device is outputting bad data.

The system stable clock is used for Signature II clock. Start/Stop comes from the chip enable pin of the particular ROM you wish to check.

If the particular chip enable ($\overline{CE}$) is an active low then that ROM will only output data during the time this input is low. If you visualize the $\overline{CE}$ waveform it becomes clear that the Signature II should begin to take data on the falling edge of this line and cease to accept data on the rising edge. Conversely, if the CE is an active high then select the rising edge for start and trailing edge for stop.

ROM signatures should be taken collectively (clock-system time base, start & stop on most significant address line used). Any one ROM which is defective will cause the collective signatures to be wrong. Should this occur then individual ROM signatures, using CE as start/stop, previously recorded from a good system will pinpoint which device is defective.

IX. — RAM TESTS

These are the most difficult devices to test in any system. Software must be developed which will write into the RAM a pattern of "0" & "1" 's and read out this pattern as a signature. A ROM with a RAM exercise pattern on the address and instruction bus must be developed.

There are several RAM cell test patterns, the best being an individual preference. Kurz-Kasch will assist you in developing a RAM test if you should desire.

The start/stop and clock inputs to the Signature II are generally the same ones used for the ROM test. KK PROM part #0500021 is used with Z80 & 8080 Systems.

X. — DATA PRESENTATION

Tabulation, schematic notation, or flow charts all have a place in the presentation of Signature II signatures.

The next few pages give an example of each of these methods. It would be expected that the number of signatures taken, as well as, the method of presentation would become a procedure which fits more adequately your own method of servicing. However you do it, remember the Signature II system is probably the most accurate test system you have or will ever use.

NO. _____
TO TEST _____
MANUFACTURER _____
_____

CLOCK F3-8 ⌐¬
START F3-6 ⌐¬
STOP F3-6 ⌐¬
GROUND F3-7
VCC 1180

HARDWIRED CLIPS ON B3, D3 & E4
ALL SWITCHES ON POD FORWARD

*Chip Enable H-1 U4CH
G-1 6947
F-1 4F68
E-1 16C8

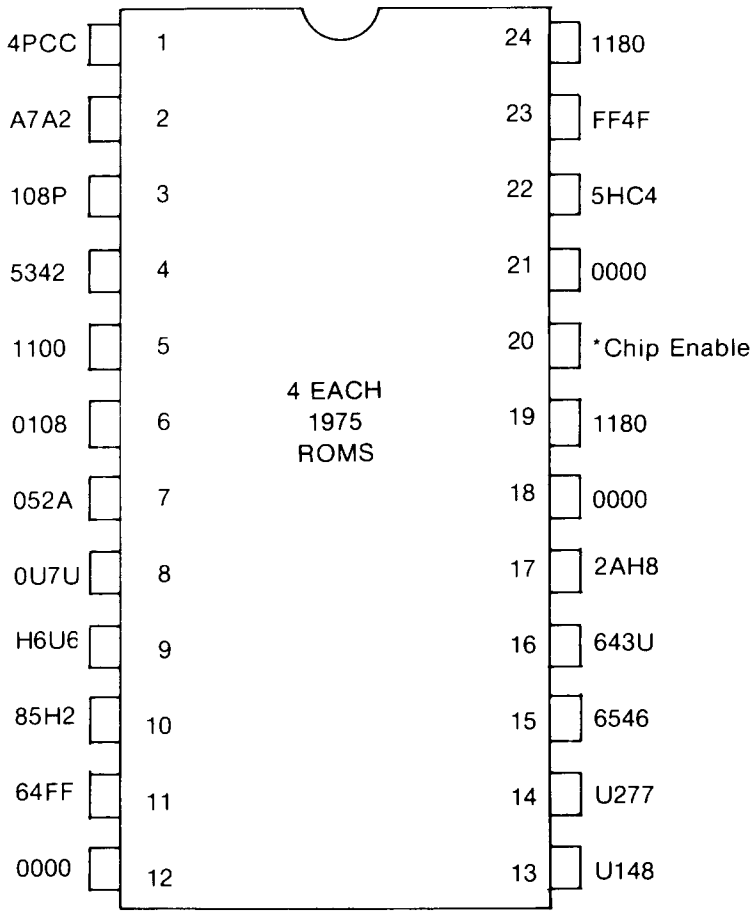
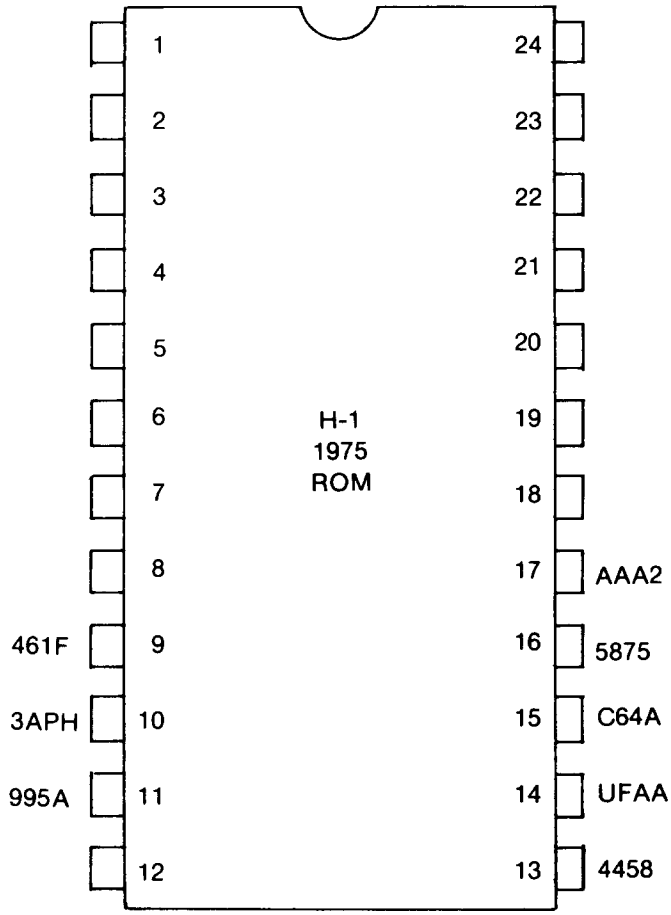


FIGURE 1

COLLECTIVE ROM TEST



INDIVIDUAL
ROM
TEST

NO. _____
TO TEST _____
MANUFACTURER _____
_____

CLOCK F3-8 ⌐¬
START E2-2 ⌐¬
STOP E2-2 ⌐¬
GROUND F3-7
VCC 8P54

HARDWIRED CLIPS ON B3, D3 & E4
POD SWITCHES: CLOCK FORWARD
: START REAR
: STOP FORWARD

FIGURE 2

I. SYNC CHAIN

Clock	E7-2	(white pod wire)
Start	E7-11	(yellow pod wire)
Stop	E7-11	(blue pod wire)
Ground	E7-8	(black pod wire)
VREF	not used	(orange pod wire)
VCC	8UA3	

COMP SYNC A6-8 C8PP

(if comp sync signature is correct proceed to processor tests)

D5

Clock	D5-2	(white)
Start	D5-11	(yellow)
Stop	D5-11	(blue)
Ground	D5-8	(black)
VREF	not used	(orange)
VCC	UP73	

Pin	Signature
11	UP8H
12	OU16
13	334U
14	55H1
15	0102

E5

Clock	E5-2	(white)
Start	E5-11	(yellow)
Stop	E5-11	(blue)
Ground	E5-8	(black)
VREF	not used	(orange)
VCC	IH44	

Pin	Signature
2	1H44
3	0000
4	0000
5	FH8U
6	FH8U
9	6F19
10	68PU
11	73UA
12	7286
13	5979
14	H85A
15	715H

E6

(This chip may be unstable)

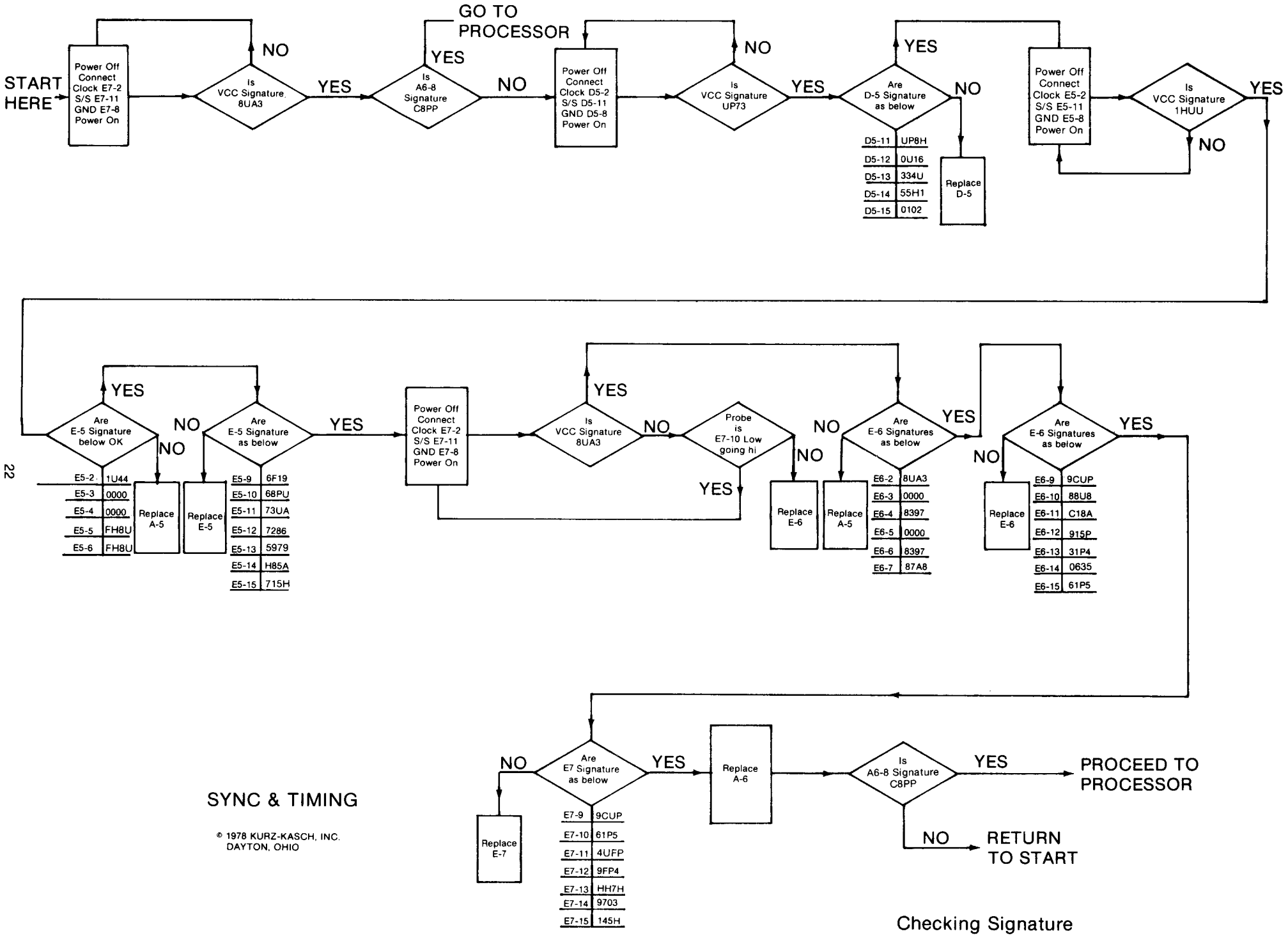
Clock	E7-2	(white)
Start	E7-11	(yellow)
Stop	E7-11	(blue)
Ground	E7-8	(black)
VREF	not used	(orange)
VCC	8UA3	

Pin	Signature
2	8UA3
3	0000
4	8397
5	0000
6	8397
7	87A8
9	9CUP
10	88U8
11	C18A
12	915P
13	31P4
14	0635
15	61P5

E7

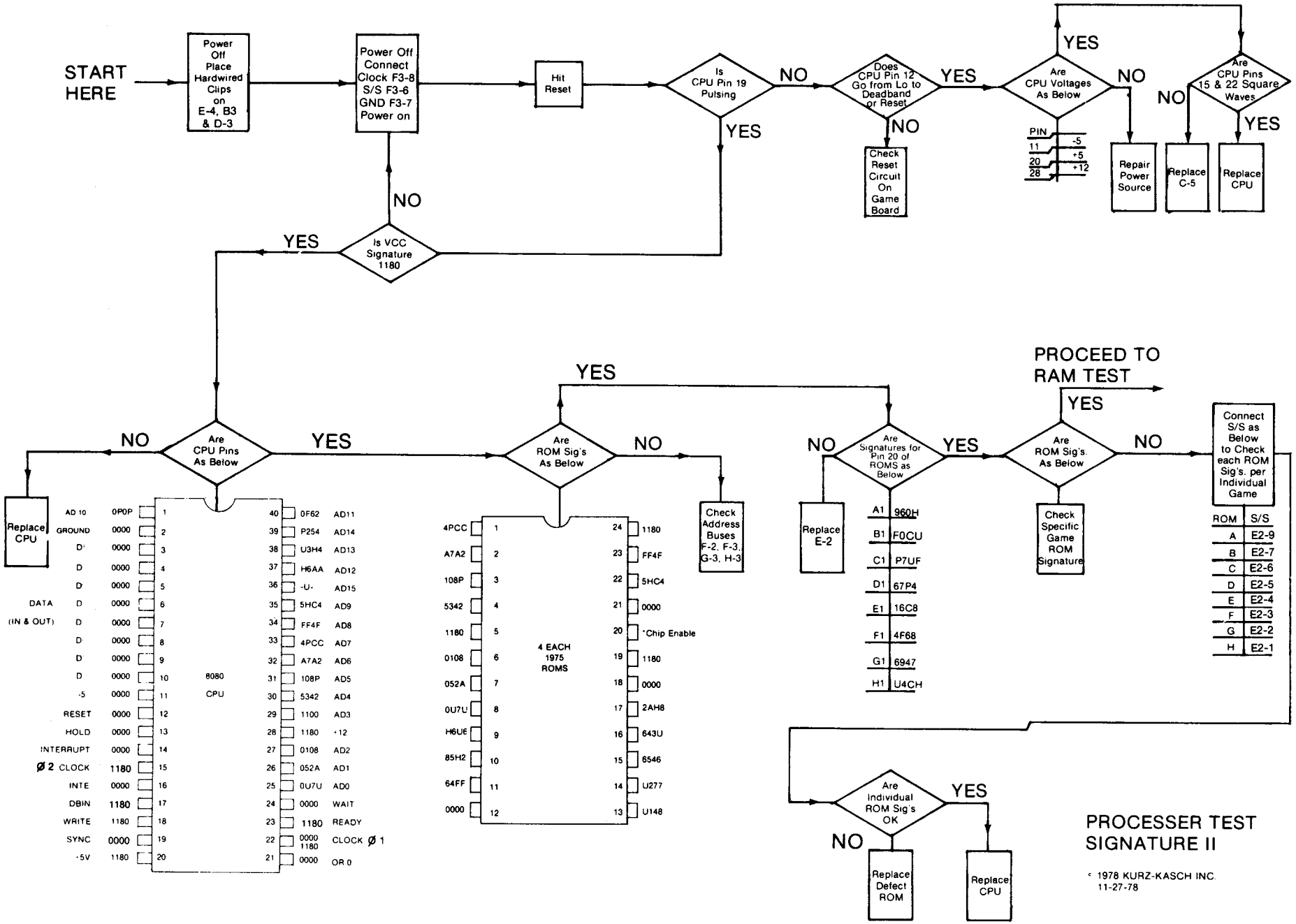
Clock	E7-2	(white)
Start	E7-11	(yellow)
Stop	E7-11	(blue)
Ground	E7-8	(black)
VREF	not used	(orange)
VCC	8UA3	

Pin	Signature
2	8UA3
3	8397
4	OF34
5	8397
6	8397
7	87A8
9	9CUP
10	61P5
11	4UFP
12	9FP4
13	HH7H
14	9703
15	145H



Checking Signature

SYNC & TIMING



Checking Signature

II. **PROCESSOR**

A. Be sure power is not on.

B. Place TC-590-89 test clip E-4 on IC E-4 observing pin 1. (if placed wrong, damage to IC B-3 & D-3 will result.)

C. Place program wired TC-590-89 test clip B-3 & D-3 on IC's B-3 & D-3 observing pin 1. (if placed wrong damage to other IC's can result.)

D. Connect Signature II per instruction on page 8.

E. Turn on power, activate "Reset" and probe CPU pin 19 for pulse activity. If not pulsing check voltages and clock on CPU.

F. Compare CPU Signatures shown on page 8, if OK proceed to "G". (Gunfight only)

G. Compare ROM Signatures per page 9. If Signatures are wrong, proceed to "H". (These Signatures are for Gunfight only.)

H. To obtain individuals ROM Signatures, connect Signature II as follows: (Leave TC-590-89's in place)

Clock	F3-8	VCC
Start	E2-*	P254
Stop	E2-*	
Ground	F3-7	
VREF	Not used	

I. Individual ROM Signatures should be obtained from a known good board. Only pins 9, 10, 11, 13, 14, 15, 16 & 17 need be probed and recorded as these are the only different Signatures necessary.

J. This completes the ROM tests. Proceed to RAM test; Proceed to RAM test; paragraph K.

*E2-1	ROM H-1
E2-2	ROM G-1
E2-3	ROM F-1
E2-4	ROM E-1
E2-5	ROM D-1
E2-6	ROM C-1
E2-7	ROM B-1
E2-9	ROM A-1

K. Ram Test Connect Signature II as follows:

KK ROM #0500021 in H-1 socket

Clock	F3-8
Start	F3-6
Stop	F3-6
Ground	F3-7
VREF	not used
VCC	003U

Hit Reset — Do Not Reset Again Unless You Lose Gate

L. Probe pin 7 of each RAM. Signatures must be alternating 0000 then 003U.

M. If any Signature is unstable, ground pin 17 of RAM being probed. If Signature becomes stable then this RAM is bad. If Signature is still unstable it is the RAM in "G" or "H" not being tested.

Should Signature be unstable with 17 grounded and ungrounded then both RAMS (G & H) are bad.

NOTE: During all processor tests pin 19 of 8080 CPU must be active.

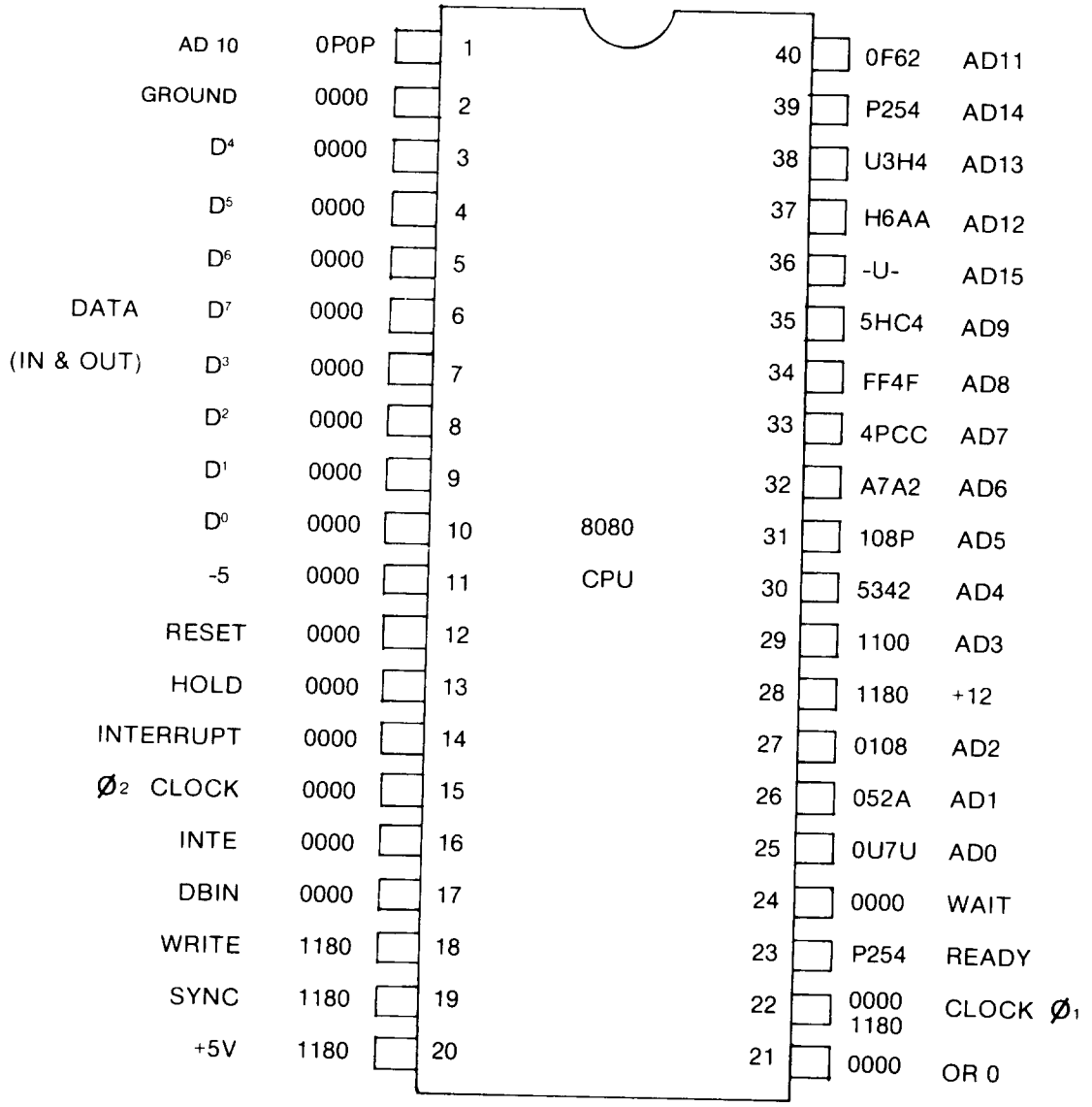
CLOCK F-3-8
START/STOP F-3-6

VCC 1180
GND 0000

GND F3-7

Used wired clips on B-3, D-3 & E-4.

*Note



*Note: If power is not off when clips are installed, damage to B-3 & D-3 will occur.

KURZ - KASCH

SIGNATURE ANALYSIS FOR MICROPROCESSORS

I

SIGNATURE ANALYSIS

A means of isolating digital logic faults at the components level. Although considered most useful in servicing micro-processor based products, the technique is applicable to all digital systems. Basically, the technique involves the tracing of signals and the conversion of lengthy bit streams into four-digit hexidecimal "signatures". Using logic diagrams and schematics specially annotated with correct signatures at each node and guided by troubleshooting trees, the technician traces back until he finds a point in the circuit which has a correct input signature and incorrect output signature.

NODE

A point of convergence on a diagram, chart or graph. Nodes can be used to designate a state, event, time convergence, or a coincidence of paths or flows.

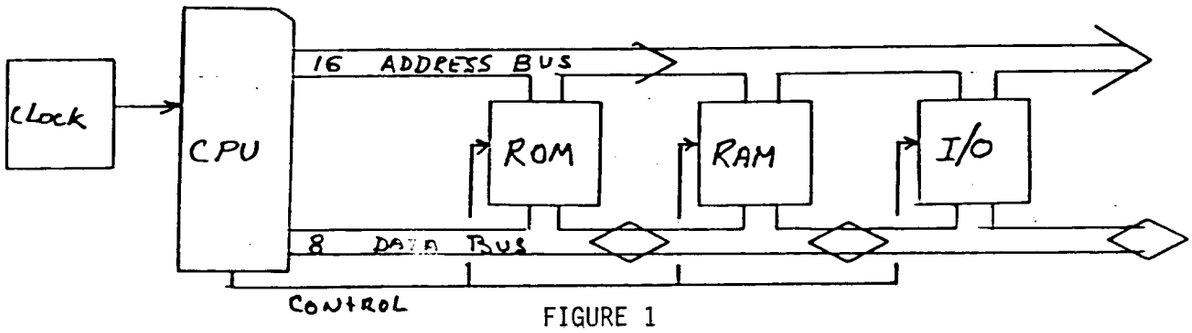


FIGURE 1

Here is a block diagram of a common bus oriented processor. The clock is the heart of the system and is the timing for the entire processor.

A CPU accepts timing information from the clock, generates addressing information, controls functions of various devices in the system, accepts information from memory and/or I. O. devices. This information or data tells the CPU what to do, it does what it is instructed and generates a response to the instructions.

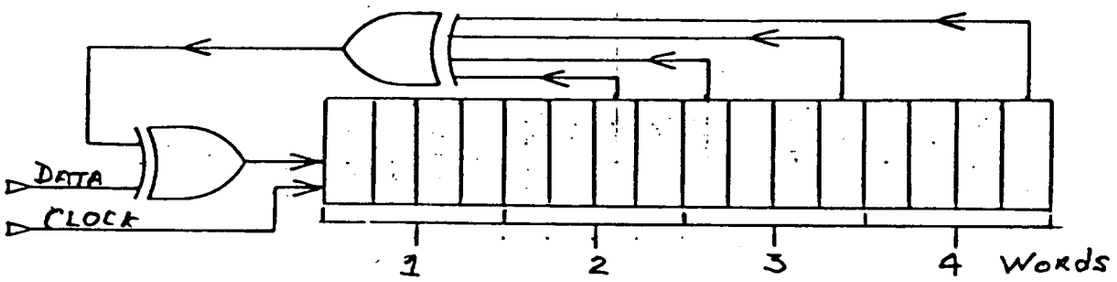
ROM is the permanent memory wherein resides the basic instructions for the CPU. Without ROM the CPU can do nothing. (ROM here is defined as CPU instructions).

RAM is the temporary storage mediam where information is temporarily stored until acted upon by the processor and moved to its final destination. RAMS also hold partially processed data.

I. O. (input-output) devices are the interfaces between the computor system and the outside world.

Throughout the entire processor system, past each node, there are streams of data. These data streams have two forms or characteristics which make them unique-quantity of "0's" & "1's" and the placement in time of them. Polarity of the pulse is important but its placement in time is equally important. The most practical and most accurate method of determining if the time and polarity criteria is met is with Signature Analysis.

Signature Analysis is a technique based on data compression to provide a unique fingerprint of each interconnection or test node in the unit under test (UUT). The Signature II provides the technician with a test probe that can be used to enter data to be recorded and read out for the test node.



Signature Analyzers convert serial bit streams into a 4 hexdigit "Signature "

FIGURE 2

Since a unique signature is generated for each data stream a prime requirement is that the data stream passing a node be indentical (unless faulty) for the same node on each identical board. The second requirement is that this data stream repeat itself. This repetition is assured by having a start and stop pulse which is time and polarity related to the data stream.

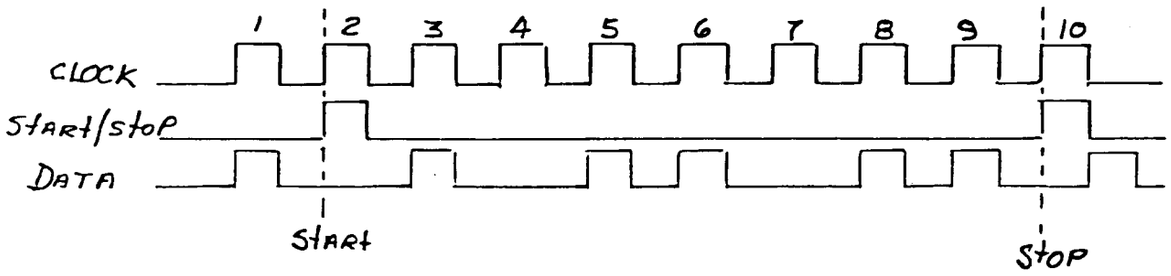


FIGURE 3

If we start the Signature Analyzer by placing "Start" on the rising edge (⎍) of the first pulse on line 2 above and the "Stop" on the rising edge (⎍) of the 2nd pulse labeled "Stop" we will allow clock pulses 2 thru 9 to enter the system. There is one data bit entered into the compression circuit for each clock pulse.

In figure 3, the data stream entered would be: 01011011

This stream would be entered each time the window is generated.

To demonstrate how a single bit difference between two data streams affect the "Signature" consider these two streams: 11111111100000111111 = D953

11111111100000011111 = 99F6

Either a bit difference or displacement by time (clock pulses) gives a totally different signature - not one digit or segment difference.

Certain portions of a processor system not designed for Signature Analysis can cause some problems but by and large following a few simple rules will overcome these problems.

Let us take a processor system from the beginning and follow through to develop signatures.

II

ALL VOLTAGES

For any electronic system to operate properly the required voltages must be present and within tolerances.

Tolerances for voltage regulators commonly used are usually ±5%. This will allow a 5 volt regulator to be between 4.75 and 5.25 volts. A 12 volt regulator can vary between 11.4 and 12.6 volts.

A regulated voltage less than the allowed minimum could be caused by:

A. Bad diodes
B. Bad filter
C. Overloaded regulator
D. Bad regulator

in that order.

Of course a power supply not plugged in, turned on, or one with blown fuses does not have voltages within tolerance. Usually the voltage is extremely low--say 0 volts. Don't laugh, it has happened to you--or will some day.

SOME COMMON FAULT SIGNATURES & HOW TO DEAL WITH THEM

Figure 1

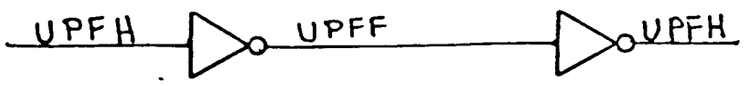


Figure 1 shows a normal inverter chain with signatures you might expect.

Figure 2

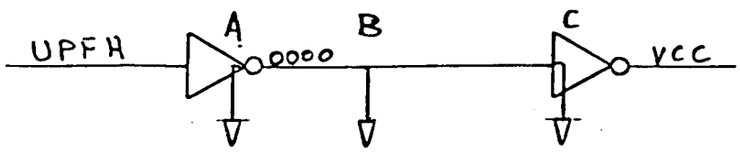


Figure 2 we see a proper signature on the first inverter's input and a "stuck at 0" at the output. As shown at points A, B & C we can have 3 failure modes. Point A is a failed output on the inverter, Point B would be a physical short to ground and C, a failed inverter input.

To determine which failure mode we have:

1--Connect Signature II Pod ground-board ground.
2--Connect HL-480 power leads to board (+5 & Ground)
3--Put Signature II Probe to inverter output.
4--Place HL-480 tip to inverter output.
5--Activate pulser, either 1 shot or 5 HZ mode.
6--If the Signature II Probe pulse light pulses the fault is at point A or C. To isolate the fault further, lift or clip the pin at the output of the inverter and if the output gives the proper signature, UPFF, then the input of the second inverter is bad. If you still have 0000 then the first inverter is bad.
7--If in 6 above the pulse light does not pulse then you have a physical short.

Figure 3

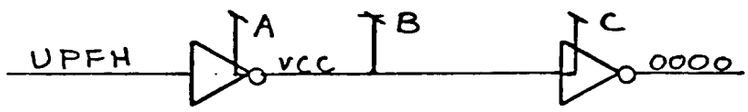


Figure 3 shows a gate or line with a failure mode "stuck at 1". This is fault isolated the same for a "stuck at 0".

Figure 4

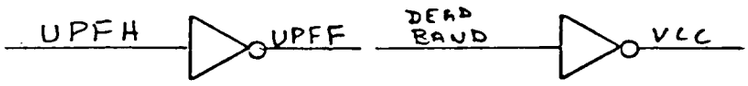


Figure 4 shows the signatures (or probes) indications for a broken trace.

Figure 5

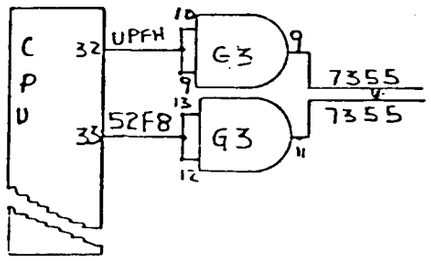


Figure 5 shows address lines from a CPU to buffers (G3) to the address bus. Proper signatures at the CPU and input of buffers but incorrect at buffer output is a fault mode. Where you find 2 or more incorrect but some signatures this indicated two bus lines shorted togeter.

Figure 6

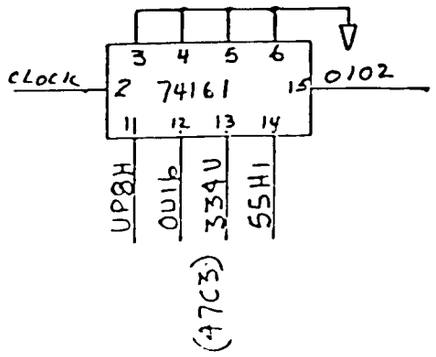
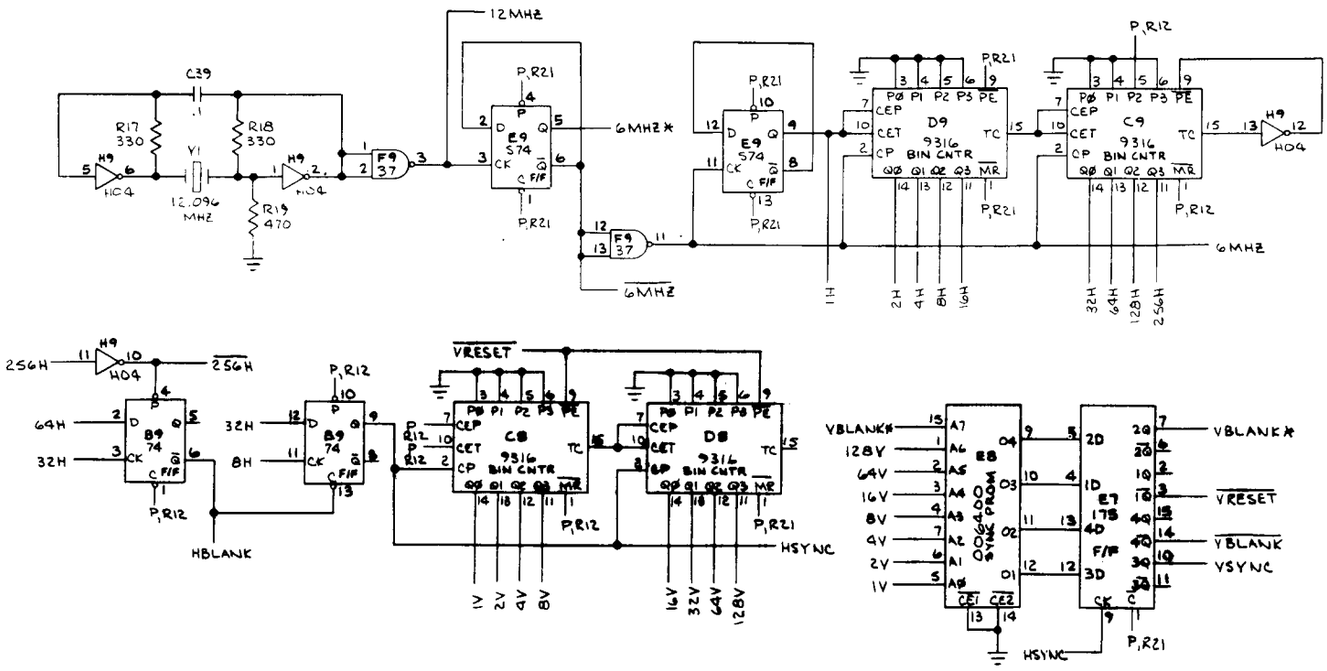


Figure 6 shows a counter which has an incorrect signature (47C3) on pin 13 but correct signature on the ohter pins. To determine if the IC is bad, lift or clip pin 13 and take the signature from the pin. If it is correct you will find another signature on the trace showing a short trace. Incorrect signatures on the lifted or slipped pin indicates a bad IC.

In any test we must check to be sure the device has proper voltages. For the CPU we must also be certain we have clock both $\emptyset_1$ & $\emptyset_2$, if required. A properly designed NOP will eliminate the possibility of an interrupt causing a CPU lockup.

IV

CLOCK & SYNC CIRCUITS



In the above circuit we notice a 12 MHZ clock which is divided by 2 by E9. This 6 MHZ square wave is used to clock the horizontal divider chain (E9, D9, C9, and B9). Derived from this chain is H blank (B9-6) and H SYNC (B9-9).

H SYNC is used to clock the vertical SYNC Divider Chain (C8, D9, E8, and E7). V Blank, V Reset, V Blank, and V SYNC are outputs of E7.

These SYNC circuits are a "piece of cake" to obtain signatures from and to test using SA. Here's all you have to do;

HORIZONTAL SYNC

A. Use D9-2 as CLOCK
   Use 9-11 as START/STOP

Read and record signatures on D9 pins 7, 14, 13, 12, 11 and 15. If these signatures are correct, proceed.

B. Use C9-2 as CLOCK
   Use C9-11 as START/STOP

Read and record signatures on C9 pins 10, 9, 14, 13, 12, 11 and 15, and E7-9.

C. After the signatures are obtained on all above pins in steps A & B leave SA connected as in step B and read and record signatures from B9, 2, 3, 4, 5 & 6. Pin 6 gives you H blank.

Now read and record signatures from B9-8, 9, 11, 12 and 13. Pin 9 gives you H SYNC.

If H SYNC is OK, you can proceed to:

VERTICAL SYNC

A. CLOCK C8-2
   START/STOP C8-11

Read and record signatures on C8 pins 14, 13, 12, 11, 15 and 9. If these signatures are OK, proceed.

B. CLOCK D8-2
   START/STOP D8-11

Read and record signatures on D8-9, 10, 14, 13, 12, 11, 15
E8-pins 1, 2, 3, 4, 5, 6, 7, 9, 10, 11, 12 & 15
E7-pins 2*, 3, 4, 5, 6*, 7, 10, 11*, 12, 13, 14 & 15

You have fully documented this SYNC Chain.

The sequence of the SYNC circuit is CLOCK-H SYNC-V SYNC, all in series. Bad clock can kill everything, H SYNC can kill V SYNC. So start at the beginning.

A quick check can be made by connecting the Signature II to:

C9-2 CLOCK
C9-11 START/STOP

Read signature at B9-9, if correct you have horizontal SYNC.

Connect Signature II

D8-2 CLOCK
D8-11 START/STOP

Read signature at E7-10, if correct you have V SYNC.

*NOTE: On pins so marked an unstable or no signature may be noticed....

V
MICROPORCESSOR RESET

One of the basic system control functions is the system RESET signal. Whether this signal is generated automatically by external power-on circuitry or manually from a push-button switch, the system components must obey a fixed set of rules to assure proper system operation.

In 6500, 6800 series microprocessor systems the RESET pin must be held low during power-on until the supply voltages and clocks have stabilized. Usually the RESET pin is held low for a minimum of 8 clock pulses. The 8080, Z80, etc., series is just the opposite. RESET is normally low and is taken high for a minimum of 3 clock pulses.

Checking of the reset circuit is best done with the Signature II probe. (Be sure the pod black wire is connected to PC board ground.)

On microprocessors which have watchdog or automatic data resets a continuing pulsing of the reset is an indication of a memory problem. This problem can be located by Signature II using instructions in sections 6-8 of this paper.

The reset circuits are rather simple so we need not spend too much time on them.

VI
CPU AND ADDRESS BUS

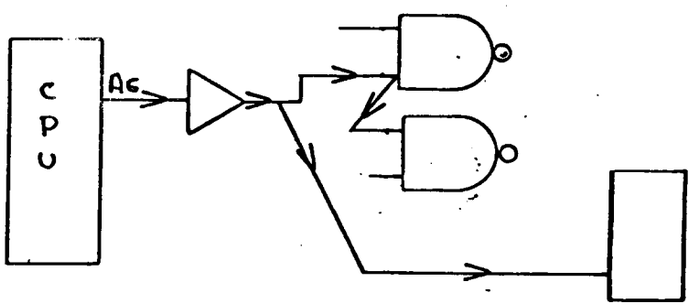
To test a CPU we must give it an instruction which it can execute in a repetitive fashion and generate signatures which are stable and the same for all like CPU's (8080's, Z-80's, 6502's, etc.). This instruction is "NOP". In order that we can be assured the CPU will only see this instruction we must break the data bus and "hardwire" the NOP into the CPU. This is done by a Kurz-Kasch NOP fixture.

This NOP fixture does a few other things such as disable the interrupts so the processor will run even if board faults would tend to "lock up" the processor.

The NOP instruction causes the CPU to become a 65K counter with its 16 address lines being the outputs. If the address outputs are counted through from all "0's" to all "1's", then the address bus has been exercised for all possible combinations and it does this repeatedly. Each of the address lines $A_{\emptyset}$ - A_{15} have a unique signature unless there is a fault with the processor or a trace or a device connected to that address line.

To obtain the signature for the address lines we use the system clock and as in all counters (remember the CPU is now a counter) the start and stop go to the most significant bit. Since we wish to input the maximum number of clock pulses we start and stop on the A-15 leading edge.
Page 11 gives the address bus signatures.

Once we have determined we have a operational CPU with proper signatures on each address pin, each address line can be traced to its termination. The figure below shows the logical test progression for the address bus. Checking inputs of the bus drivers and then the outputs assure you that the address bus is clear. If it isn't, use the fault isolation instructions give you in Section III.



All devices are now being properly addressed so we are ready to begin to measure their response.

NOP FIXTURE SIGNATURES - FOR PROCESSORS

PROCESSOR	Z-80	*6502-A	8080	6502		6800
CLOCK	PIN 21	Pin 37	PIN 17	PIN 37		PIN 37
START/STOP	5	25	36	25		25
GROUND	29	21	2	21		21
A0	30	UUUU	25	9	UUUU	9
A1	31	5555	26	10	FFFF	10
A2	32	CCCC	27	11	8484	11
A3	33	7F7F	29	12	P763	12
A4	34	5H21	30	13	1U5P	13
A5	35	OAFA	31	14	0356	14
A6	36	UPFH	32	15	U759	15
A7	37	52F8	33	16	6F9A	16
A8	38	HC89	34	17	7791	17
A9	39	2H70	35	18	6321	18
A10	40	HPPO	1	19	37C5	19
A11	1	1293	40	20	6U28	20
A12	2	HAP7	37	22	4FCA	22
A13	3	3C96	38	23	4868	23
A14	4	3827	39	24	9UP1	24
A15	5	755P	36	25	0002	25
VCC		0001			0003	

*Atari games will use a KK 6502-A NOP. The signatures will be the same as for an 8080.

Signature II connections to 6502 does not change.

THIS IS CORRECTED COPY
FOR PAGE 17 OF
SIGNATURE II MANUAL

CPU NOP FIXTURE CONNECTIONS

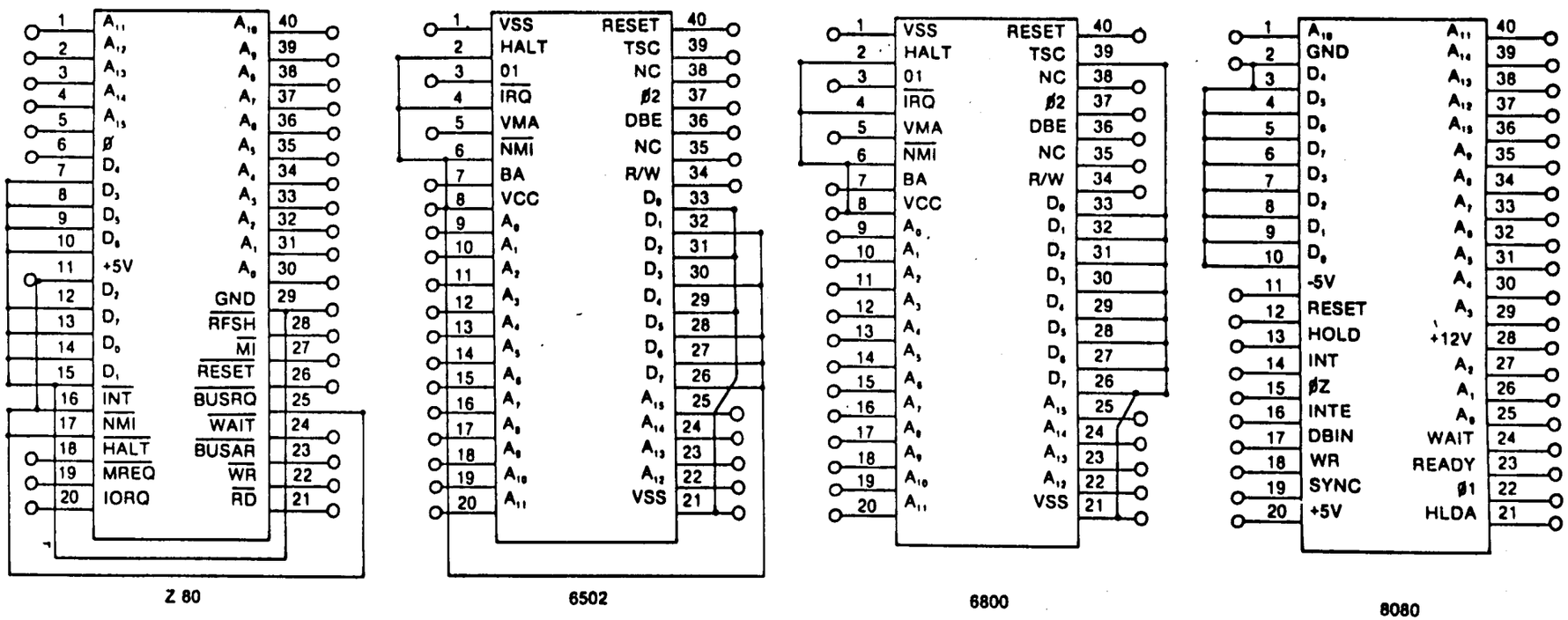


FIGURE
4

O- THESE PINS CONNECT DIRECT FROM LOGIC BOARD CPU SOCKET TO FIXTURE SOCKET PINS WITHOUT O- ARE INTERCONNECTED AS SHOWN. THESE PINS ARE NOT CONNECTED TO LOGIC BOARD CPU SOCKET.

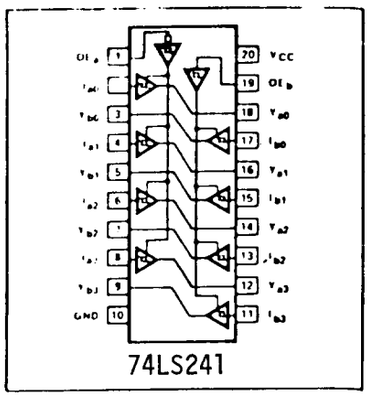
VII

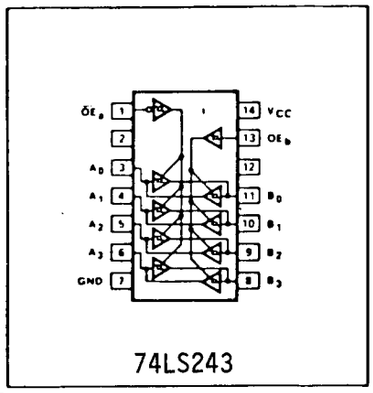
BUS DRIVERS

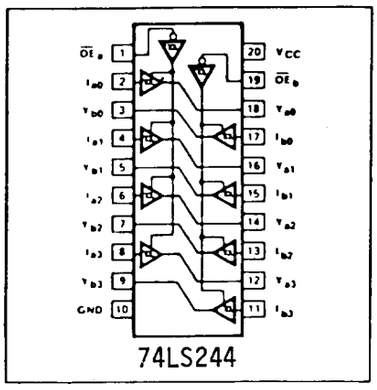
Bus drivers are devices which isolate sections of the various buses. The drivers are directional and have the capability of being removed electrically from the bus by proper logic levels on the OE (output enable) inputs.

When testing a computor board with signature analysis often the drivers are disabled. In order to take signatues on the inputs and outputs they often must be force enabled.

The 74LS241 may be forced by applying a low on Pin 1 and a high on Pin 19. Pin 19 cannot be pulled high. This must be done by a previous inverting gate whose input can be taken low or by clipping Pin 19. Pin 1 can just be pulled low.


74LS241


74LS243


74LS244

A 74LS243 is a bi-directional driver. If pin 1 and 13 are low, data will flow from A to B. A high on pins 1 and 13 will cause data to flow from B to A. Under no circumstances take 1 low and 13 high at the same time or pull either pin high. (see 74LS241 above)

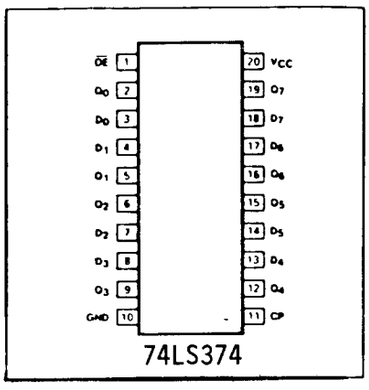
The 74LS244 operates much like the LS241 except the levels on pins 1 and 19 must be low to enable the devices.

On non-inverting devices like the ones above, signatures on input and output will be the same when enabled. Inverting drivers will have different input-out signatures.

A latch such as the 74LS374 must have two conditions satisfied to pass data.

1. pin 1 $\overline{OE}$ must be low.
2. pin 11 must clock high.

Pin 1 can be taken low and held while a pulser (KK/HL-480) is touched to pin 11 and "one shot" pulsed. This will transfer whatever data on D to Q.


74LS374

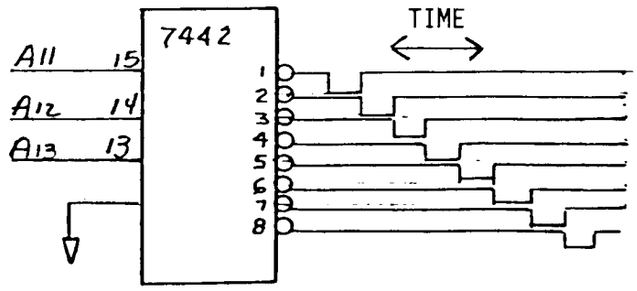
VIII

ROMs, RAMs, DECODERs

The ROM is the permanent memory which causes the processor system to begin and continue to perform in a predetermined manner. Bad ROMs can and will cause the system to do crazy things. Fortunately ROMs are very easily tested by Signature Analysis. The easiest way is whth a Kurz-Kasch ROM Test I or ROM TEST II, but equally as accurate is with the Signature II.

For the ROM Test we still use the system clock for the Signature II, but for start/stop we must select a point which will allow us to look at an individual device.

This point is the ROM enable (decoder). The figure below shows the address decoder and what its outputs look like.



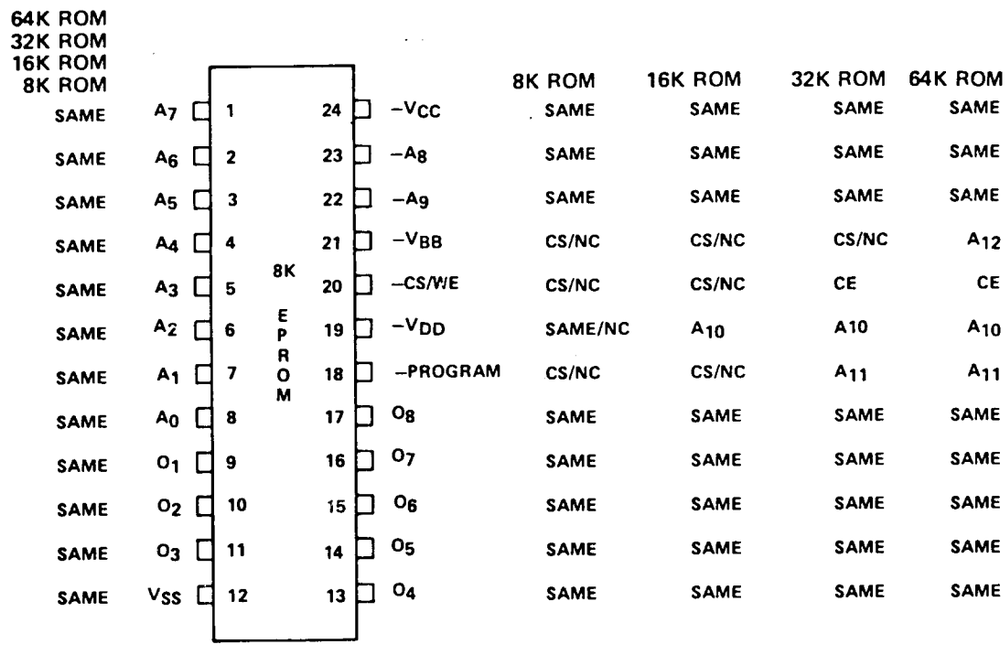
The decoder is addressed by A11, 12, & 13. Three address lines when decoded will cause 8 outputs to sequence.

A13	A12	A11	7442
0	0	0	Pin 1 goes low
0	0	1	Pin 2 goes low
0	1	0	Pin 3 goes low
0	1	1	Pin 4 goes low
1	0	0	Pin 5 goes low
1	0	1	Pin 6 goes low
1	1	0	Pin 7 goes low
1	1	1	Pin 8 goes low

With the Signature II connected in the address signature mode (start ⎍, stop ⎍ to A15) you will get the signatures for the 7442 outputs. These signatures will assure you that the ROMs will be properly enabled.

If we look at a ROM we can see what needs to transpire in order to get it to output the data it holds.

EPROM AND ROM PIN CONNECTION COMPATIBILITY
Figure 6



Virtually all pin connections are same for an 8K EPROM through a 64K ROM. Significant difference occurs on the EPROM V_{BB}, V_{DD}, and program pins. These pins in ROM are either CS/$\overline{CS}$ functions or address inputs with some manufacturers allowing no-connect options. With N/C option, EPROM can be directly replaced by ROM with no circuit change, except when using 16K or larger.

We see that this ERPOM (2716) is to be addressed by AØ - A10, that it needs ground & +5V for its operation. We also note there are two pins, 18 & 20, $\overline{CE}_1$ and $\overline{CE}_2$ which may be used as enables. If we tie pin 20 low we have a single enable, pin 18 ($\overline{CE}$). The bar over the CE indicates that this pin must go low to enable the EPROM.

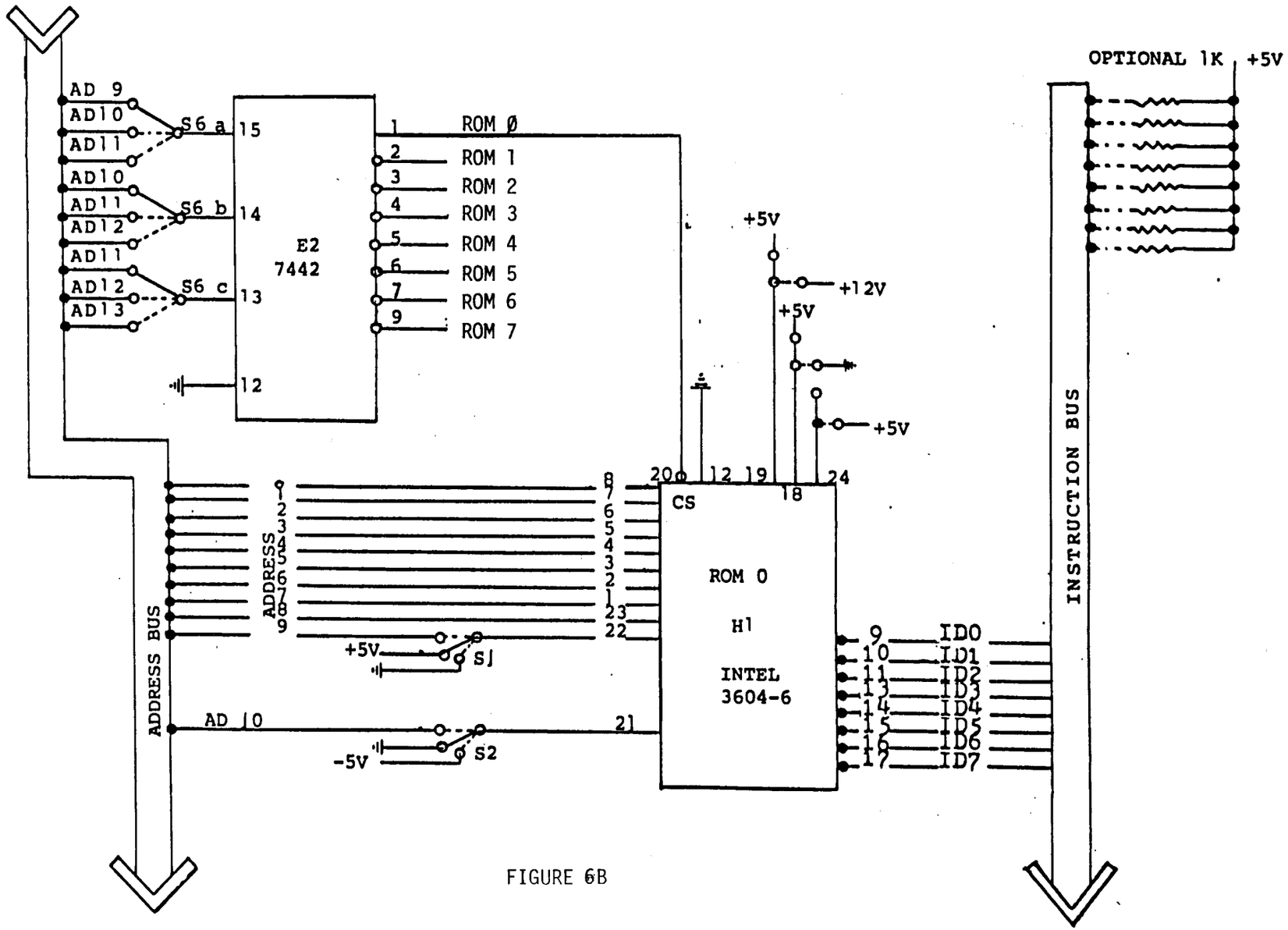
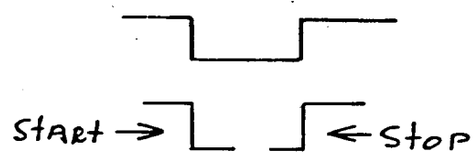

AD 9
AD10
AD11
S6 a
AD10
AD11
AD12
S6 b
AD11
AD12
AD13
S6 c
15
14
13
12
E2
7442
1
2
3
4
5
6
7
9
ROM Ø
ROM 1
ROM 2
ROM 3
ROM 4
ROM 5
ROM 6
ROM 7
OPTIONAL 1K
+5V
+5V
+12V
+5V
+5V
20
12
19
24
18
CS
ROM 0
H1
INTEL
3604-6
ADDRESS BUS
ADDRESS
1
2
3
4
5
6
7
8
9
8
7
6
5
4
3
2
1
23
22
+5V
S1
AD 10
21
-5V
S2
9
10
11
13
14
15
16
17
ID0
ID1
ID2
ID3
ID4
ID5
ID6
ID7
INSTRUCTION BUS

FIGURE 6B

Going back to page 14 we see that the 7442 outputs go low in sequence starting with the address lines all at "0". First pin 1 goes low. If we tied pin 18 of the EPROM to pin 1 of the decoder, for a period of time the 2716 would be low thereby enabled and would output data. The data outputted will be dependant upon the addresses applied, in practice the EPROM would be totally addressed and therefore all data contained therin would appear at the data outputs ($D_{\emptyset}$ - D_7). Further there will be an address change and a resulting data change with each clock pulse.

Since we wish to have the Signature II only look at the data bus (EPROM output) during the time the EPROM is enabled we set the start-stop switches in a manner to portray the enable pulse.



The Signature II will give a signature for each of the 8 data output data streams which would occur between the start and stop times.

Should there be more than 1 ROM or other memory device necessary to perform the computor's mission one would only need to connect the other ROM (s) to the 7442 enables in the order you would want them to operate. (see page 16)

To read signatures for the additional ROM (s) one would only need to connect the Signature II to the enable pin (18) of the device you wish to check.

If when checking a multi ROM bank the signatures will not stabilize, remove all ROMs except the one you are checking, or connect a 4.7 K pull-up to data probe tip.

Here again faults such as outlined in the common fault section will be effective for isolating a problem.

Les us stop at this point and reflect where we are:

1. CPU is running
2. Address bus including drivers (buffers) is clear and healthy.
3. ROMs are being addressed and enabled properly.
4. ROMs are outputting proper data and the data bus is clear.

We move on to the next major item in the computor:

RAM

The RAMs are the most difficult components to test in a processor. It is necessary to be able to write into them a known program which can be repeated. This must be done with software.

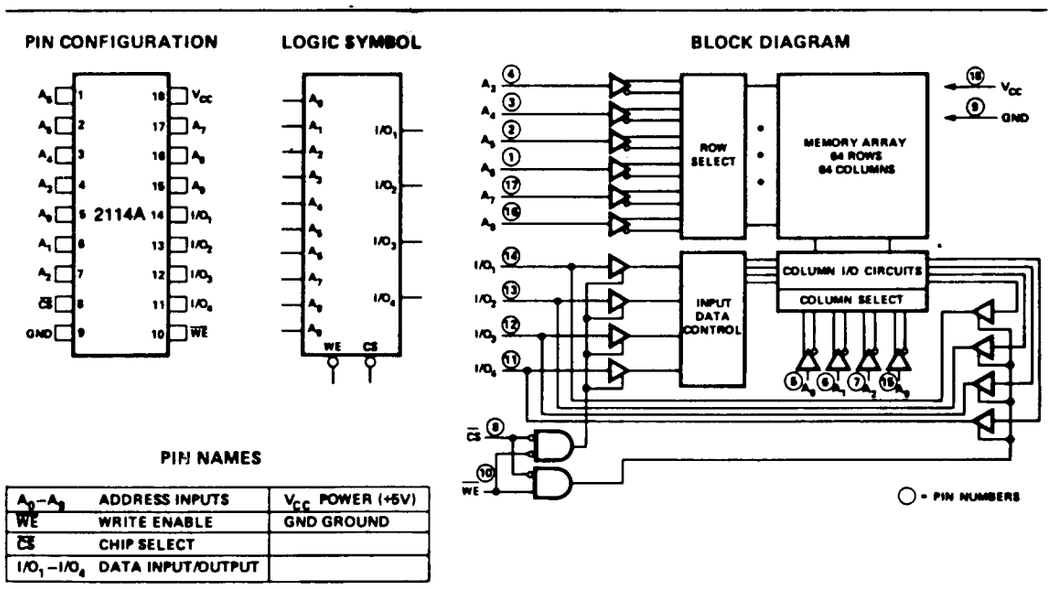
If the board you are testing has RAM-TEST program in its memory or can be loaded in via a PIA then the processor system at this point can execute the program and dynamically test the RAMs. This is a good deal, but, if you don't have a built-in RAM test they can still be tested.

A simple program which will write a "0" and a "1" into alternate cells in the RAMs then compliment this pattern ("1" where there was a "0", and a "0" where there was a "1"). This forms a checkerboard pattern.

Kurz-Kasch has programs for several of the processors and will assist in programs for specific applications.

Assume we have software (a ROM) with a RAM TEST pattern in it, the Signature II can tell you which one of a multi-ram bank is defective.

Refer back to pages 14 & 16, and we see a decoder, RAMs are enabled in the same manner as ROMs with one exception---a read-write enable. Look at the figure below, which is a pinout of a 2114 RAM.



Pins 1-7 and 15-17 are the address lines which define the cells into which data is to be written or read. Pin 8 is the chip enable just like the ROM. When this pin goes low the RAM is enabled but---it can't input data until pin 10 (write) goes low. This pin is controlled by the CPU which commands that it write onto or read from the data bus. Remember a command must be always viewed from the CPU. The command is what it is doing---not other devices.

If the Signature II start and stop are connected to the CE (just as in the case of ROM) and set the switches to read signatures where CE is low you will get signatures for the data being written into the RAM. By using the write line as start---stop we can read signatures for the contents of the RAM.

IX
MULTIPLEXERS

A multiplexer is a device which has two (2) or more inputs and selects one input at a time to be outputted.

For a practical application the Midway 8080 motherboard uses four 9322 muxes. Pin 1, when low allows the data on input 1 to appear at the output. When pin 1 is high data on input 2 appears at the output.

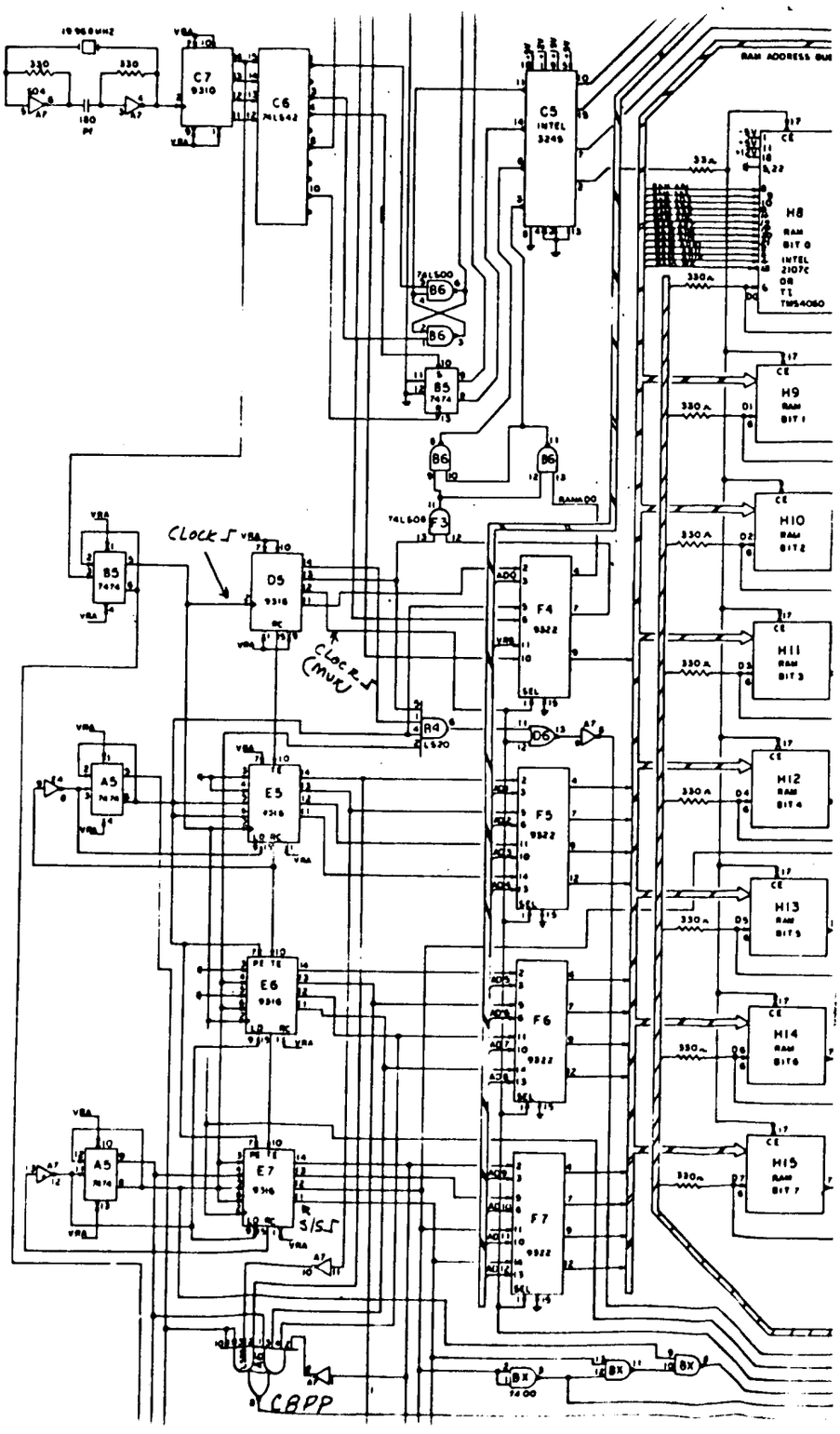
The schematic on page 22 shows one of the two inputs orginate at the CPU and the other from the counter chain. In other words data from two systems can appear at the mux output. This normally would cause the signatures to be unstable. The Signature II clock when in the rising ⎍⎾ mode allows us to look at input 1 through the mux and gives a stable signature.

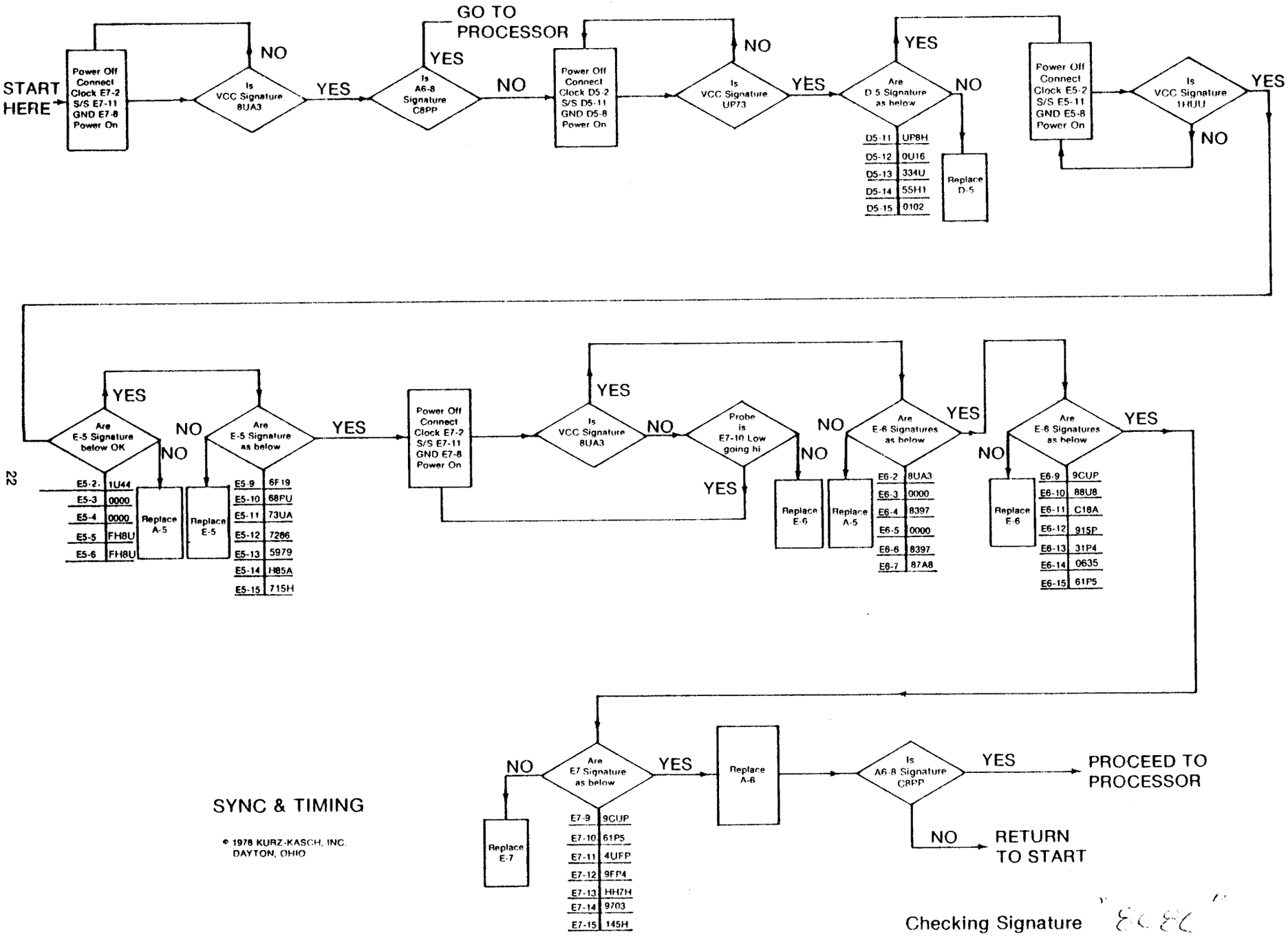
To test the multiplexes with the Signature II connect as follows and read the signatures:

8080 MIDWAY RAM ADDRESS MULTIPLEXERS

CLOCK D5 - 12⎍⎾
START/STOP E7 - 11⎍⎾
VCC H6HU

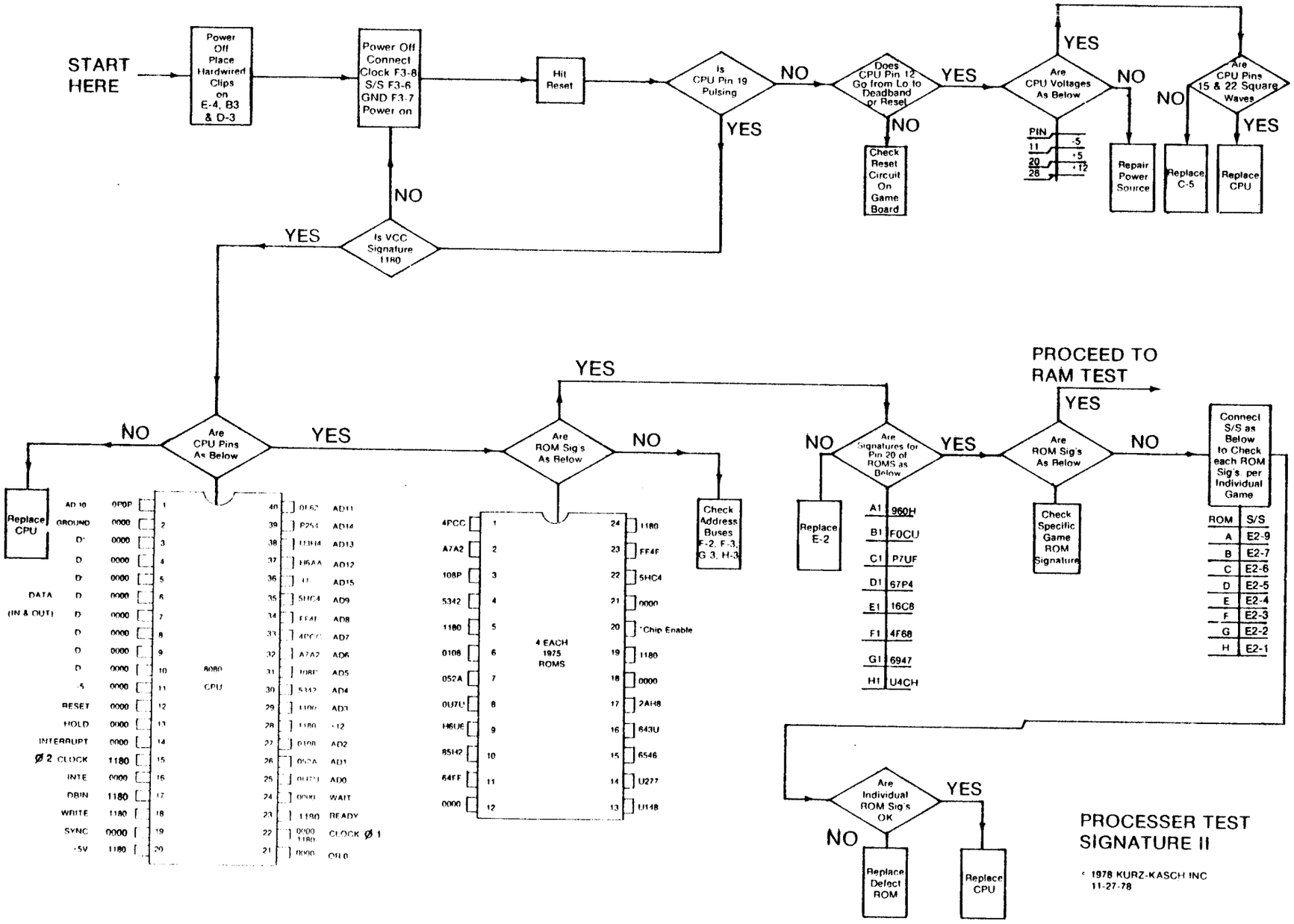
PIN	F4	F5	F6	F7
2	4HC5	3C6F	43CF	6172
5	CCC6	U249	7U95	599P
11	H6HU	8F33	C674	067U
14	Dead Band	6481	3669	07HA
4	4HC5	3C6F	43CF	6172
7	CCC6	U249	7U95	599P
9	H6HU	8F33	C674	067U
12	H6HU	6481	3669	07HA


19.968 MHZ
C7
9310
C6
C5
INTEL
3245
RAM ADDRESS BUS
H8
H9
H10
H11
H12
H13
H14
H15
B5
B6
B4
D5
9318
F4
F5
F6
F7
9322
E5
E6
E7
A5
D6
F3
74LS08
74LS00
Clock
Clock
(MUX)
S/S
CBPP
RAM D0



SYNC & TIMING

Checking Signature 8C8C



Checking Signature 8C8C

Trouble Shooting Microprocessors With "Free Run" Fixtures

By Mark Stirling — Coastal Games Ltd.
Richmond, B.C.

This is the first of a series of articles intended to help games service people detect and cure microprocessor system faults quickly and easily. This will be accomplished with the aid of some inexpensive and easily constructed tools.

When a microprocessor system fails to the point where the self-test will not run, troubleshooting the fault can quickly become extremely difficult. This is due to a simple characteristic common to all microprocessor sytems. That is; the data bus forms part of a complex feedback loop and any error in the loop compounds itself causing all components in the loop to act erractically,whether they are good or not. Signature analysis has been put forth as a sophisticated technique to aid in trouble shooting but even this, requires a predictable core of the system to function in order to be of any use. Free-run fixtures will give you a predictable pattern from the microprocessor allowing orderly troubleshooting.

What exactly does this free run fixture do? A free run fixture forces the processor to cycle continuously through all its addresses. This in turn means that all chip selects are activated with a stable regular signal that you can now use your oscillosope to check. In this manner for instance address decoding can be located. Shorted or open address lines can also be easily detected Address buffers can be checked because we have a predictable signal passing through. The nature of the signal is similar to the output of a 16 stage counter. Address line A0will cycle fastest with Address line A1 at half the speed of A0and so on to address line A15. This regular pattern also will generate a stable data stream for those of you with access to signature analysis.

How does the fixture work? The free run fixture works by isolating the data bus, thereby opening the feedback loop and forcing a hard wired no operation instruction on the data bus at the processor. No matter what address is output by the processor the instruction seen is the same. This forces the program counter to step in a regular fashion through the complete memory space of the system.

Fig 1 shows how a typical free run test fixture is constructed. Figs 2, 3, 4, 5 show the actual connection for 6800, Z80, 6502 and 8080A processors; these being the most common processors at the moment.

To design your own fixture for another processor, all that is required is to wire the no operation (NOP) instruction to the processor and ensure that interrupt and halt and BUS request lines cannot be activated.

Next month I will explain a simple address mapper which can help detect some types of intermittent faults.

Feel free to drop me a line. Your comment will be appreciated along with any questions. I cannot promise to answer each letter individually but will answer those of merit in upcoming articles.

Coastal Games Ltd.,
#105 — 3860 Jacombs Road,
Richmond, B.C.
V6V 1Y6
(604) 270-9346

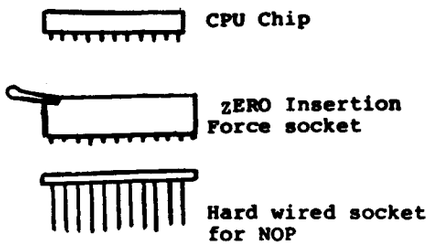


FIG. 1 "FREE RUN" FIXTURE PLUGS INTO GAME CPO SOCKET.

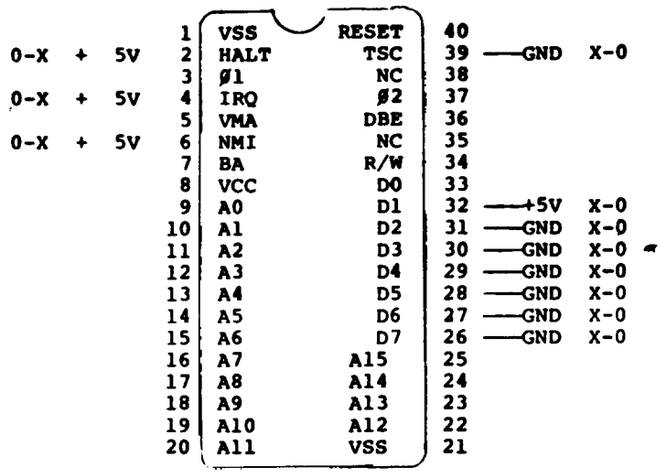


FIG. 2 6800

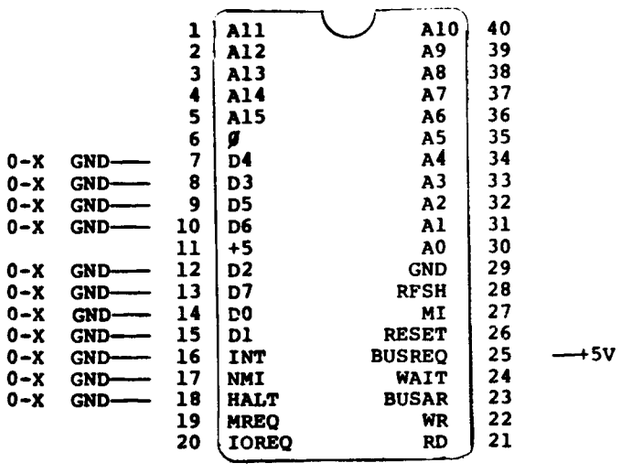


FIG. 3 Z80

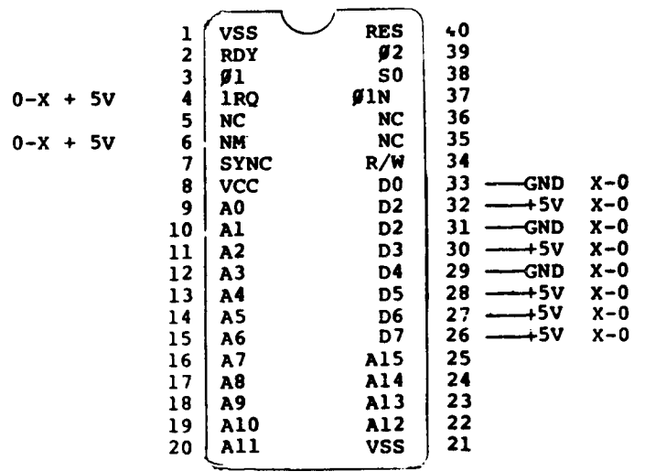


FIG. 4 6502

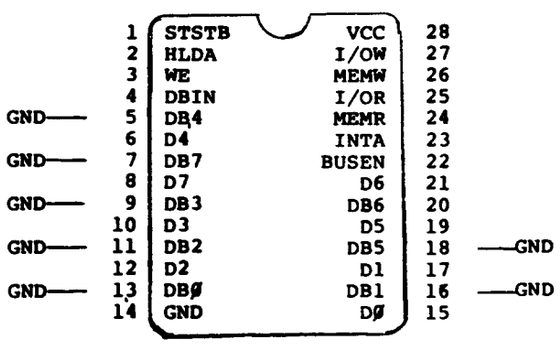


FIG. 5 8228/38 SYSTEM CONTROLLER FOR 8080A

NOTE: Due to the fact that its status signals are multiplexed with data merely cutting the data lines would completely stop its operation. The data lines must therefore be broken "outside" the system controller chip or chips that demultiplex the status and data lines.