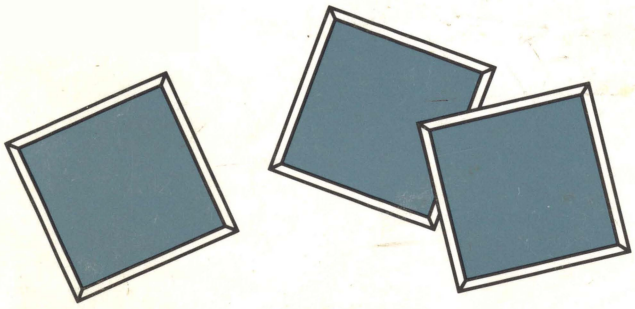
MVME224A-1/-2/-3/-4 (4Mb/8Mb/16Mb/32Mb) Series of DRAM Memory Modules User's Manual



MOTOROLA

MVME224A-1 (4Mb), MVME224A-2 (8Mb),

MVME224A-3 (16Mb), AND MVME224A-4 (32Mb)

SERIES OF DRAM MEMORY MODULES

USER'S MANUAL

(MVME224A/D1)

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PREFACE

This manual provides general information, hardware preparation, installation instructions, functional description, and support information for the MVME224A-1/-2/-3/-4 series of DRAM memory modules.

This manual is intended for anyone who wants to design OEM systems, supply additional capability to an existing compatible system or in a lab environment for experimental purposes.

A basic knowledge of computers and digital logic is assumed.

To use this manual, you should be faimilar with the publications listed in the *Related Documentation* paragraph in Chapter 1 of this manual.

WARNING

THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND IF NOT INSTALLED AND USED IN ACCORDANCE WITH THE INSTRUCTIONS MANUAL, MAY CAUSE INTERFERENCE TO RADIO COMMUNICATIONS. IT HAS BEEN TESTED AND FOUND TO COMPLY WITH THE LIMITS FOR A CLASS A COMPUTING DEVICE PURSUANT TO SUBPART J OF PART 15 OF FCC RULES, WHICH ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINST SUCH INTERFERENCE WHEN OPERATED IN A COMMERCIAL INVIRONMENT. OPERATION OF THIS EQUIPMENT IN A RESIDENTIAL AREA IS LIKELY TO CAUSE INTERFERENCE IN WHICH CASE THE USER, AT HIS OWN EXPENSE, WILL BE REQUIRED TO TAKE WHATEVER MEASURES NECESSARY TO CORRECT THE INTERRFERENCE.

First Edition

SAFETY SUMMARY
SAFETY DEPENDS ON YOU

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola Inc. assumes no liability for the customer's failure to comply with these requirements. The safety precautions listed below represent warnings of certain dangers of which we are aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

GROUND THE INSTRUMENT.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter, with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified maintenance personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY EQUIPMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact Motorola Field Service Division for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

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CHAPTER 1 - GENERAL INFORMATION

1.1 INTRODUCTION

This user's manual provides general information, preparation and installation instructions, functional description, and support information for the MVME224A-1 (4Mb), MVME224A-2 (8Mb), MVME224A-3 (16Mb), and the MVME224A-4 (32Mb) DRAM memory modules with VME/VSB interface. These modules are referred to as the MVME224A throughout the remainder of this manual.

1.2 FEATURES

The features of the MVME224A include:

- Memory Capacity - 4Mb or 8Mb using 1-megabit DRAMs in ZIP packages (MVME224A-1 and MVME224A-2 versions).
- Memory Capacity - 16Mb or 32Mb using 4-megabit DRAMs in ZIP packages (MVME224A-3 and MVME224A-4 versions).
- Dual ported VMEbus interface with 16-/24-/32-bit address selection and 16-/32-bit data.
- Multiplexed VSBbus interface with 32-bit address/data.
- Longword (32-bit), Word (16-bit), and byte (8-bit) data transfers.
- Memory base address switch-selectable on any 1Mb boundary throughout the VMEbus and VSBbus address space.
- Error Protection -- Parity is provided on a byte basis.
- Command and Status Register -- Control over parity and error status reporting.
- Fast Read -- Selectable to start reads on PAS* on VSBbus for fast access or DS* to allow a cache detection.
- Fast Write -- Both VMEbus and VSBbus provide early DTACK on a write access.
- Two board interleave.
- Block transfer on VSBbus.

1.3 SPECIFICATIONS

General specifications for the MVME224A are provided in Table 1-1.

TABLE 1-1. MVME224A SPECIFICATIONS

Characteristic	Specification
Storage capacity:	
MVME224A-1	4 Megabytes
MVME224A-2	8 Megabytes
MVME224A-3	16 Megabytes
MVME224A-4	32 Megabytes
Data transfer size	8-, 16-, and 32-bit
Error detection	Odd byte parity
Data Input/Output	16-/32-bit VMEbus, 32-bit VSBbus
Input address	16-/24-/32-bit VMEbus, 32-bit VSBbus
Power requirements:	
MVME224A-1	+4.75 to 5.25 Vdc at 5.Ø A maximum (3.9A typical)
MVME224A-2	+4.75 to 5.25 Vdc at 5.Ø A maximum (3.9A typical)
MVME224A-3	+4.75 to 5.25 Vdc at 5.Ø A maximum (3.9A typical)
MVME224A-4	+4.75 to 5.25 Vdc at 5.9 A maximum (4.5A typical)
Relative humidity	5% to 95% (non-condensing)
Temperature:	
Operating	Ø degree to 5Ø degrees C inlet air temperature with forced air cooling.
Storage	-4Ø degrees to 85 degrees C
Physical size (PCB):	
Height x width	6.3Ø inches (16.ØØ cm) x 9.19 inches (23.34 cm)
Thickness	Ø.Ø62 inch (Ø.157 cm)
Part projections:	
Component side	Ø.5Ø inch (1.27 cm) maximum
Solder side	Ø.Ø67 inch (Ø.17 cm) maximum

1.4 GENERAL DESCRIPTION

The MVME224A module is a high performance dynamic memory module, dual ported to both the VMEbus and VSBbus. Both modules can be mapped to start on any 1Mb boundary and extend by the module (board) size. The MVME224A uses an advanced arbitration method which buries the arbitration time for the next cycle in the current cycle, thus increasing throughput.

1.5 REFERENCE DOCUMENTATION

The following publications may provide additional helpful information. If not shipped with this product, they may be purchased from Motorola's Literature Distribution Center, 616 West 24th Street, Tempe, Arizona 85282; telephone (6Ø2) 994-6561.

DOCUMENT TITLE	MOTOROLA PUBLICATION NUMBER
VME Subsystem Bus (VSBbus) Specification (Rev A.1)	MVMESB

An additional publication that may provide helpful information is listed below.

ANSI/IEEE Std 1Ø14-1987 IEEE Standard for a Versatile Backplane Bus: VMEbus	Institute of Electrical and Electronics Engineers, Inc. 345 East 47th Street New York, New York 1ØØ17

1.6 MANUAL TERMINOLOGY

Throughout this manual, a convention has been maintained whereby data and address parameters are preceded by a character which specifies the numeric format as follows:

$	dollar	specifies a hexadecimal number
%	percent	specifies a binary number
&	ampersand	specifies a decimal number

Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on high to low transition.

In this manual, assertion and negation are used to specify forcing a signal to a particular state. In particular, assertion and assert refer to a signal that is active or true; negation and negate indicate a signal that is inactive or false. These terms are used independently of the voltage level (high or low) that they represent.

CHAPTER 2 - HARDWARE PREPARATION AND INSTALLATION

2.1 INTRODUCTION

This chapter provides the unpacking, hardware preparation, and installation instructions for the MVME224A memory modules. It also describes the start-up procedures.

2.2 UNPACKING INSTRUCTIONS

NOTE

If shipping carton is damaged upon receipt, request that the carrier's agent be present during unpacking/inspection of equipment.

Carefully unpack the equipment from the shipping carton. Refer to the packing list and verify that all items are present. Save the shipping carton and packing materials for storing or reshipping of the equipment.

CAUTION

AVOID TOUCHING AREAS OF INTEGRATED CIRCUITS; STATIC DISCHARGE CAN DAMAGE THESE CIRCUITS.

Inspect for any shipping damage. If no damage exists, then the module can be prepared for operation according to the following sections of this chapter.

2.3 HARDWARE PREPARATION

This section describes the hardware preparation of the MVME224A memory module prior to installation. Observance of this description will ensure the user that all components are properly configured for operation.

Jumper blocks are used to select the various functions and options of the MVME224A memory module. Before the MVME224A is installed, the user should verify the jumper block configurations and alter the jumpers, as required, for the user's particular system operation.

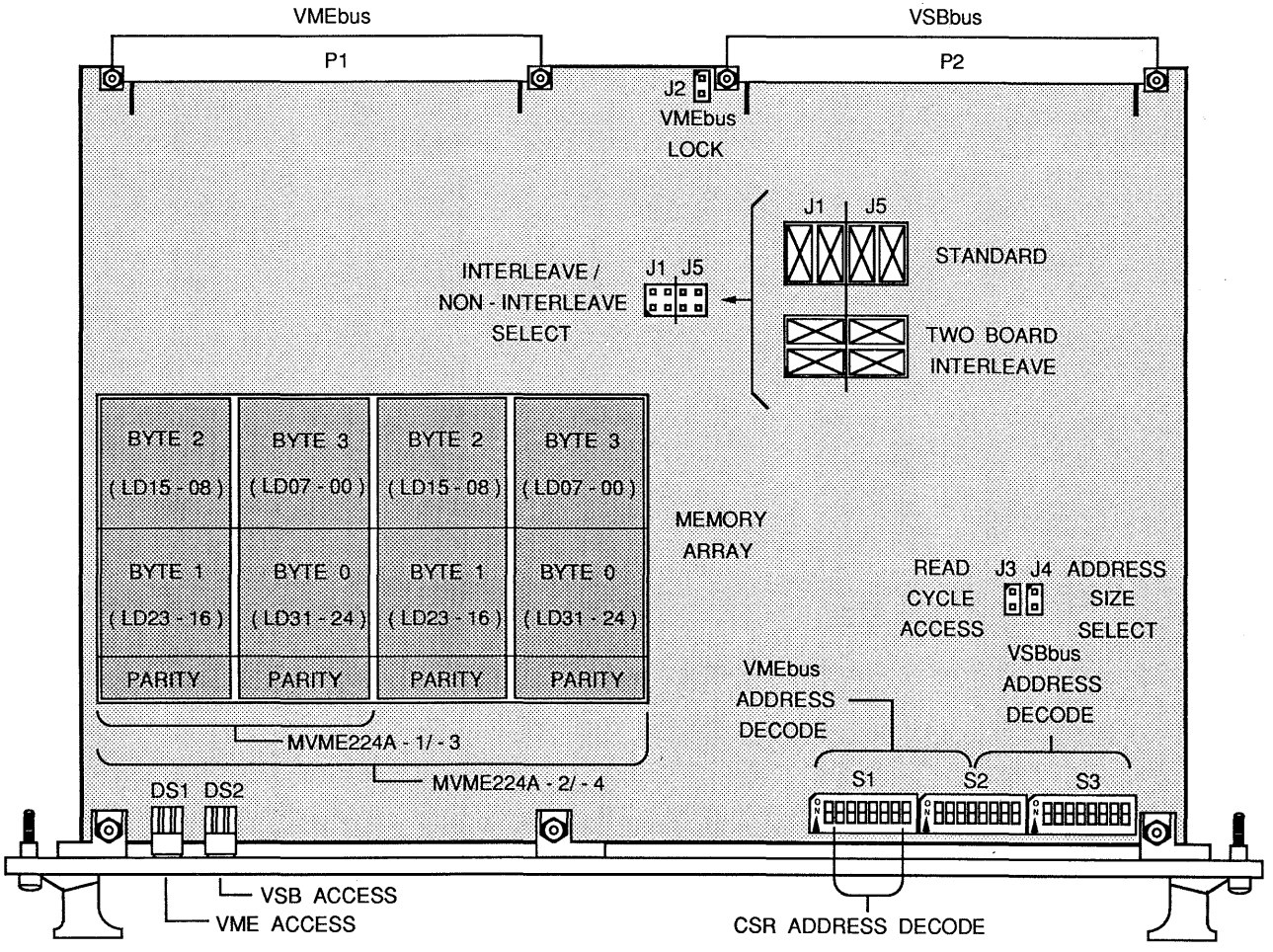


FIGURE 2-1. JUMPER, CONNECTOR, AND SWITCH LOCATION DIAGRAM

The MVME224A has been factory tested and is shipped with factory-installed jumper configurations that are illustrated in Figure 2-1. The MVME224A is operational with these factory-installed jumpers. Table 2-1 lists the jumper blocks by designation, function, and factory configuration. A more detailed description of these jumper blocks is provided in the following sections.

Also, three DIP-type switches (S1, S2, and S3) are located on the MVME224A. For detailed information regarding the use of these three switches, refer to the section "VME/VSB Address Decode Switches".

2.3.1 Jumper Block Settings

The following table lists and describes the MVME224A jumper blocks.

TABLE 2-1. MVME224A FACTORY JUMPER PLACEMENTS

Jumper	Function	Factory Configuration
J1	Interleave/Non-Interleave Select (VME)	J1(1-2)(3-4)
J2	VMEbus Lock	No Jumper(s) Installed.
J3	Read Cycle Access	No Jumper(s) Installed.
J4	Address Size Select	No Jumper(s) Installed.
J5	Interleave/Non-Interleave Select (VSB)	J5(1-2)(3-4)

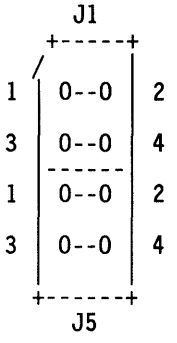
2.3.2 Interleave/Non-Interleave Select (J1,J5)

Jumper blocks J1 and J5 determine whether the MVME224A module is operating independently, or in the two-board interleave mode. With jumper caps installed across J1 pins (1-2), (3-4) and J5 pins (1-2), (3-4), the MVME224A is configured in the **non-interleave mode**. The MVME224A's addressing is independent of any other boards in the system, and there are no restrictions on its mapping.

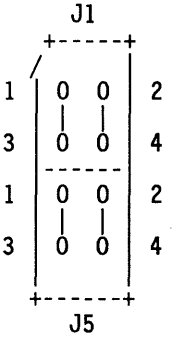
With jumper caps installed across J1 pins (1-3), (2-4), and J5 pins (1-3), (2-4), the MVME224A is configured in the **interleave mode**. The MVME224A can, in some high performance systems, enhance performance. The MVME224A must be installed in pairs and there are addressing restrictions (refer to the section, "Address Select - Interleave Mode" for more details). Block transfer on the VSBbus is not available in the interleave mode.

In all cases, VME and VSB must be set the same, i.e., both must be set to non-interleave, or, both must be set to interleave.

Jumper Block J1 and J5
Interleave/Non-Interleave Select
No Interleave Selected
(Factory Setting)



Jumper Block J1 and J5
Interleave/Non-Interleave Select
Interleave Selected



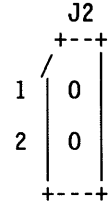
2.3.3 VMEbus Lock (J2)

In systems that support the VMELOCK signal option (such as the MVME13Ø, MVME131, MVME135, or MVME141), installing a jumper pin across jumper J2 pins 1-2 will allow control of locking the VMEbus.

Normally, the VSBbus is locked out until Address Strobe (AS*) on the VMEbus returns to high, as there is no way to detect a read-modify-write cycle.

If this jumper is installed, only those cycles that drive VMELOCK* low are locked and the MVME224A is allowed to start a VSBbus cycle earlier. If the VME cycles they follow are not locked, it will not have to wait for the VMEbus AS* signal to return high. The VMELOCK signal is driven by the bus master on the reserved bus pin P2-B3.

Jumper Block J2
VMEbus Lock
No Jumper Installed
(Factory Setting)



2.3.4 Read Cycle Access (J3)

Jumper block J3 serves two functions. First, it determines whether a read cycle will start from PAS* or DS* on the VSBbus. In some systems doing caching, the master will drive addresses and PAS* during the time it is decoding a potential local cache hit. If a cache hit is found, it simply removes the strobes without driving DS* or completing the cycle.

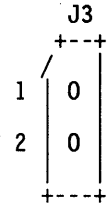
Installing a jumper pin across jumper J3 pins 1-2, starts read cycles on DS* to avoid starting false cycles. Systems not employing these address-only cache cycles should start reads on PAS* (i.e., with the jumper not installed).

Secondly, jumper block J3 also determines whether the WAIT* signal will be driven. In a system with one or more slaves who decode and drive ASACKØ* or ASACK1* in less than 5Ø nanoseconds, jumper J3 should be installed. Installing jumper J3 causes the MVME224A to drive the WAIT* signal and forces the master to hold addresses stable until decoding is done by the MVME224A. This slows system performance slightly, so it should be avoided unless necessary.

In a system where all slaves are MVME224As, or no slaves are capable of decoding addresses and driving ASACKØ* or ASACK1* in less than 5Ø nanoseconds from PAS*, do not install jumper J3.

2

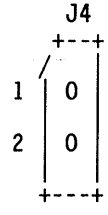
Jumper Block J3
Read Cycle Access
No Jumper Installed
(Factory Setting)



2.3.5 Address Size Select (J4)

Jumper block J4 determines the address size selection. With no jumper pin installed, 24- or 32-bit addressing is allowed. With a jumper pin installed across jumper J2 pins 1-2, 24-bit address modifiers will not be decoded and the module will not respond to 24-bit addresses.

Jumper Block J4
Address Size Select
No Jumper Installed
(Factory Setting)



Installed
A32 only

2.3.6 VME/VSB Address Decode Switches

DIP switches S1, S2, and S3 are used in selecting the starting address for the VMEbus and the VSBbus mapping. Addressing is independently selectable on 1Mb boundaries.

The VME portion of the switches is also used in selecting the starting address for the CSR mapping. The CSR is mapped dependent on the mapping of the addressing to the RAMs on the VMEbus. The following figures illustrate how the switch positions can be set for any required address.

Examples: VMEbus Address Mapping (S1-1 to S1-8 and S2-1 to S2-4) on 1Mb boundaries.

CSR Mapping - Base address is BEØ1, increasing 4 bytes for each 2Mb increase of RAM base address.

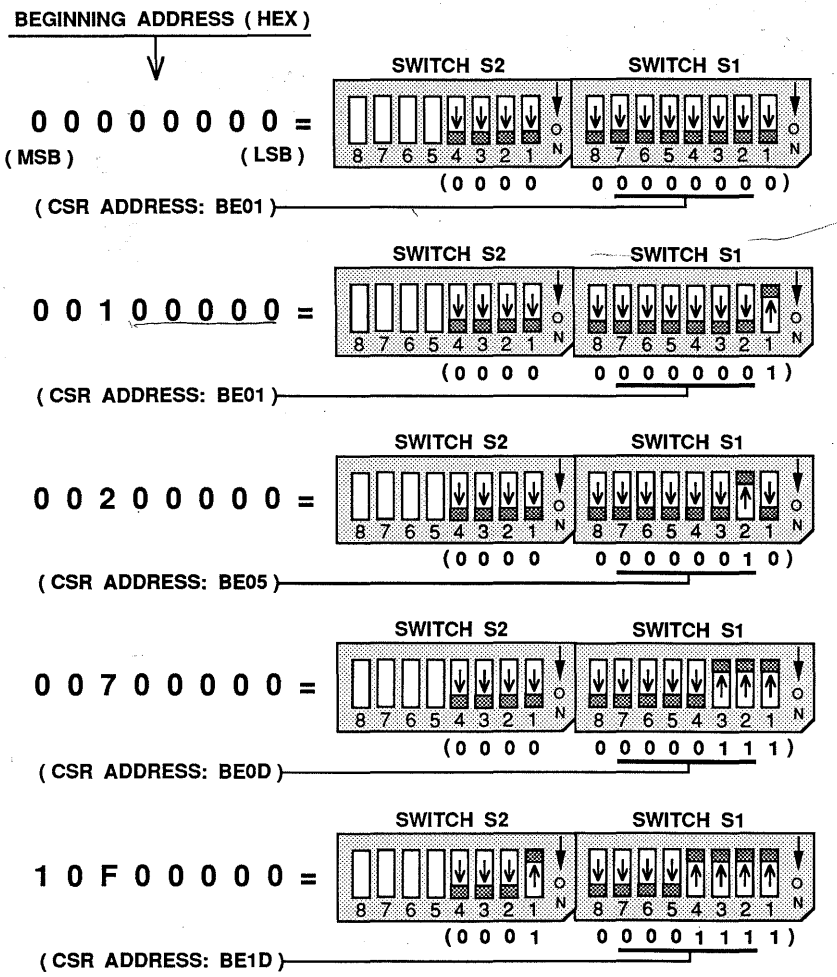


FIGURE 2-2. VMEbus ADDRESS MAPPING SWITCH EXAMPLES

Examples: VSBbus Address Mapping (S2-5 to S2-8 and S3-1 to S3-8) on 1Mb boundaries.

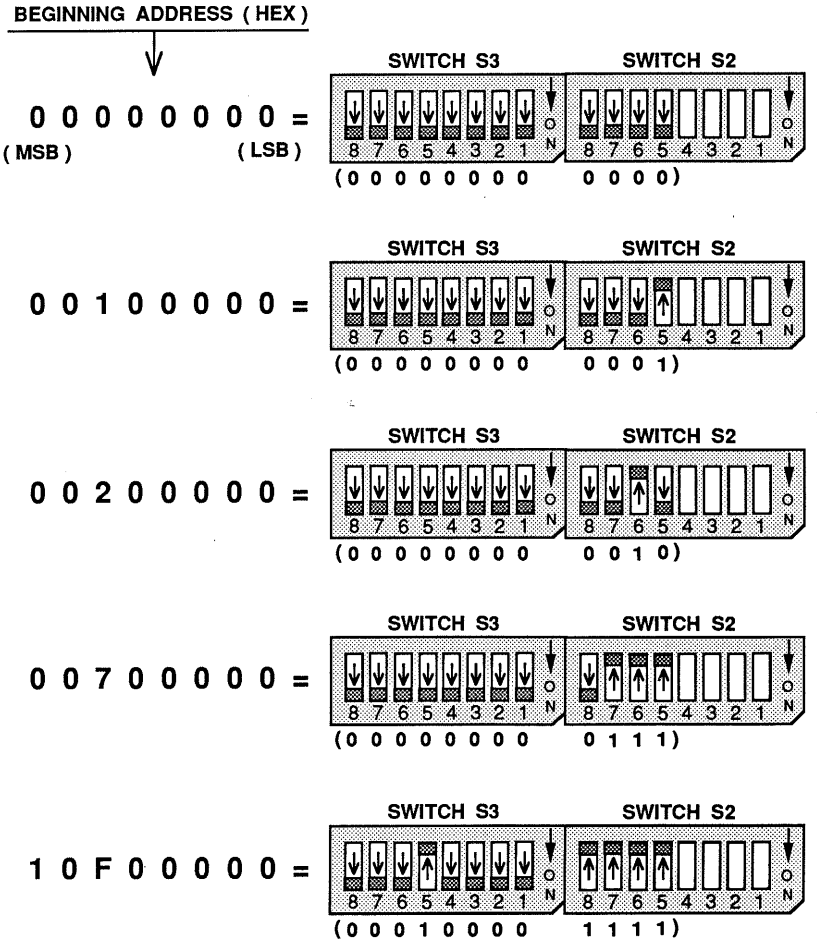


FIGURE 2-3. VSBbus ADDRESS MAPPING SWITCH EXAMPLES

TABLE 2-2. VME/VSB ADDRESS MAPPING

VME				VME								VME OR VSB BEGINNING ADDRESS (HEX)	VME CSR ADDRESS SHORT I/O (1 BYTE)
S2-4	S2-3	S2-2	S2-1	S1-8	S1-7	S1-6	S1-5	S1-4	S1-3	S1-2	S1-1		
A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20		
0	0	0	0	0	0	0	0	0	0	0	0	00000000	BE01
0	0	0	0	0	0	0	0	0	0	0	1	00100000	BE01
0	0	0	0	0	0	0	0	0	0	1	0	00200000	BE05
0	0	0	0	0	0	0	0	0	0	1	1	00300000	BE05
0	0	0	0	0	0	0	0	0	1	0	0	00400000	BE09
0	0	0	0	0	0	0	0	0	1	0	1	00500000	BE09
0	0	0	0	0	0	0	0	0	1	1	0	00600000	BE0D
0	0	0	0	0	0	0	0	0	1	1	1	00700000	BE0D
0	0	0	0	0	0	0	0	1	0	0	0	00800000	BE11
0	0	0	0	0	0	0	1	0	0	0	0	01000000	BE21
0	0	0	0	0	0	1	0	0	0	0	0	02000000	BE41
0	0	0	0	0	1	0	0	0	0	0	0	04000000	BE81
0	0	0	0	1	0	0	0	0	0	0	0	08000000	BE01
0	0	0	1	0	0	0	0	0	0	0	0	10000000	BE01
0	0	1	0	0	0	0	0	0	0	0	0	20000000	BE01
0	1	0	0	0	0	0	0	0	0	0	0	40000000	BE01
1	0	0	0	0	0	0	0	0	0	0	0	80000000	BE01

AD31	AD30	AD29	AD28	AD27	AD26	AD25	AD24	AD23	AD22	AD21	AD20	VME OR VSB BEGINNING ADDRESS (HEX)	VME CSR ADDRESS SHORT I/O (1 BYTE)
S3-8	S3-7	S3-6	S3-5	S3-4	S3-3	S3-2	S3-1	S2-8	S2-7	S2-6	S2-5		
VSB								VSB					

2.4 INSTALLATION INSTRUCTIONS

After the MVME224A has been properly configured for operation, it is ready for installation in a VMEmodule chassis.

1. Ensure that power is turned **OFF** to the chassis and that the board ejector handles are in their non-eject positions.

> **CAUTION**
>
> INSERTING OR REMOVING THE BOARD WHILE POWER IS APPLIED CAN DAMAGE THE BOARD CIRCUITRY. AVOID TOUCHING AREAS OF INTEGRATED CIRCUITS; STATIC DISCHARGE CAN DAMAGE THESE CIRCUITS.

2. The Bus Grant and IACK backplane jumpers may either be installed or removed in the card slot in which the MVME224A is installed. The MVME224A does not use these signals.

3. Slide the board into the board slides of the selected slot until the P1/P2 connectors align and seat into their backplane sockets. Press firmly on the top and bottom sections of the front panel until the connectors seat fully into their backplane sockets. Avoid pressing against the board ejector handles as they may slide into their board eject positions. When installing, check the position of the two captive screws at the top and bottom ends of the front panel. They may jam against the chassis frame and prevent the board from seating fully.

4. Once installed, screw in the two captive screws to secure the board in place. Avoid over-tightening the screws as they may strip out the screw sockets. The screws also serve to electrically connect the front panel to the frame of the chassis by pressing the conductive top and bottom sections of the front panel against the conductive frame of the chassis. This integrates the front panel into the EMI (Electromagnetic Interference) shield of the chassis. This also reduces the susceptibility of the board to static discharge that can result from touching the front panel. These EMI protections rely on the use of a chassis that is properly designed to control the susceptibility and emission of EMI.

5. Connect the power cable to the AC power source and turn the unit **ON**.

CHAPTER 3 - FUNCTIONAL DESCRIPTION

3.1 INTRODUCTION

This chapter provides an overall block diagram view of the MVME224A memory module. The discussion includes sections with detailed descriptions of the 4/8Mb - 1 MEG x 1 DRAM array (MVME224A-1/-2), the 16/32Mb - 4 MEG x 1 DRAM array (MVME224A-3/-4), the DRAM timing and control circuitry with dual port and refresh arbitration, the VMEbus interface and address decode, the VSBbus interface and address decode, parity generation and checking, and the Control/Status Register. For the purpose of the following description, the MVME224A is regarded as consisting of functional blocks as illustrated in Figure 3-1. For further details, refer to the schematic diagram in Chapter 4 and to the ANSI/IEEE Std 1014-1987, IEEE Standard for a Versatile Backplane Bus: VMEbus.

3.2 DRAM ARRAY

The MVME224A-1 (4Mb version) provides a DRAM array of 36 1-megabit DRAMs in zip packages. The MVME224A-2 (8Mb version) provides a DRAM array of 72 1-megabit DRAMs in zip packages. The MVME224A-3 (16Mb version) provides a DRAM array of 36 4-megabit DRAMs in zip packages. The MVME224A-4 (32Mb version) provides a DRAM array of 72 4-megabit DRAMs in zip packages. The DRAM array is arranged in 4 bytes with 1 parity bit per byte on the 4Mb and 16Mb versions, or 8 bytes with 1 parity bit per byte on the 8Mb and 32Mb versions. CAS before RAS refresh is utilized, using the address counter internal to the DRAMs, therefore, no refresh addresses must be supplied.

3.3 DRAM TIMING, CONTROL, AND ARBITRATION

DRAM timing, arbitration of the internal bus between VMEbus and VSBbus, and refresh arbitration are all accomplished from two timing chains. The TØ* timing handles arbitration while the RASTØ* timing handles RAM signals. One of the potential users of the arbitration scheme (VMEbus, VSBbus, and refresh) will have control at any time. When a request for a cycle is generated from either of the address decode circuits or the refresh circuit, the TØ* timing chain is started. This timing chain will cause arbitration to take place. If the user that generated the request is the same as the one which has the internal control, then the RASTØ* timing is also started. This will cause a memory cycle, or CSR cycle to take place. The third possibility is that a cycle can be started on the TØ* timing chain by a user not having control causing an arbitration cycle to start. If within 5Ø nanoseconds, a cycle is decoded on the circuit which does have control, the RASTØ* timing chain will start causing what started as an arbitration only cycle to become also a valid memory cycle.

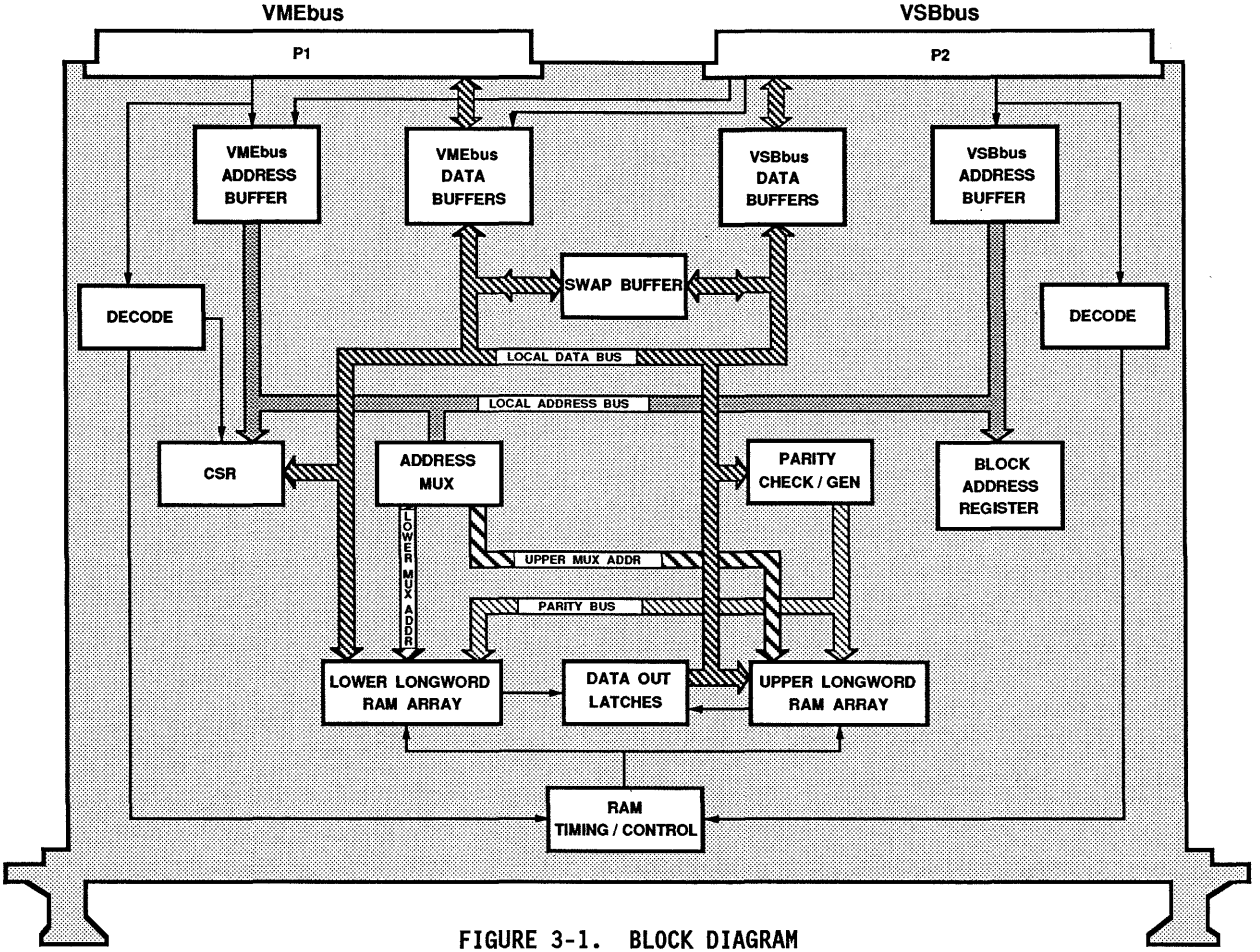


FIGURE 3-1. BLOCK DIAGRAM

In each case, an arbitration is done midways in the cycle to determine who will have control for the next cycle. In the case of a refresh cycle, it is always arbitrated back to either VME or VSB. It will go to VSB if a VSB cycle is pending, to VME if a VME cycle is pending with no VSB pending, or, if neither has a cycle pending, back to the one that preceded it. The result of this arbitration method is greater performance and, under heavy loading of both busses, performance actually increases over light loading of both busses.

The read cycle timing diagram is illustrated in Figure 3-2. The write cycle timing diagram is illustrated in Figure 3-3.

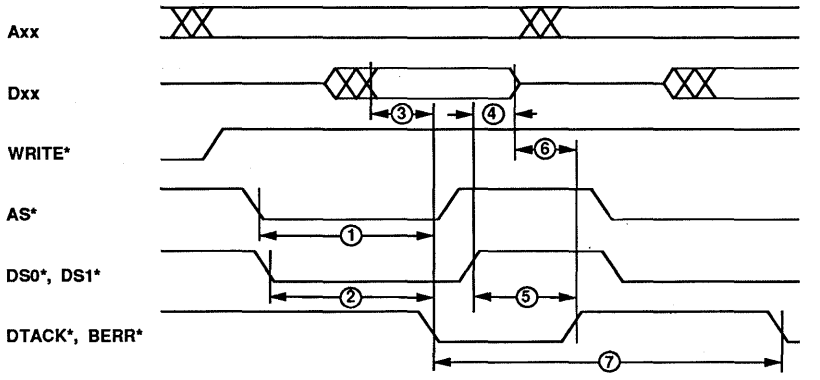


FIGURE 3-2. VME READ CYCLE TIMING

No.	Parameter	Min	Typ	Max	Unit	Notes
1	AS* low to DTACK*/BERR* low	165	17Ø	485	nsec	1,3
2	DSØ*/DS1* low to DTACK*/BERR* low	165	17Ø	485	nsec	3
3	Data valid to DTACK* low	Ø	--	3Ø	nsec	--
4	DSØ*/DS1* high to data invalid	1Ø	--	4Ø	nsec	--
5	DSØ*/DS1* high to DTACK*/BERR* high	15	2Ø	3Ø	nsec	--
6	Data high imp. to DTACK*/BERR* high	Ø	--	35	nsec	--
7	DTACK* low to DTACK* low	195	2ØØ	565	nsec	2,3

Notes:
1) Provided that the VMEbus master drives AS* and DSØ*/DS1* low at the same time.
2) Provided that the VMEbus master drives DSØ*/DS1* low less than 4Ø nsec after receiving DTACK* low.
3) The maximum time can result if a refresh cycle has just started when the board is selected, and a VSB cycle comes before the refresh cycle is finished.

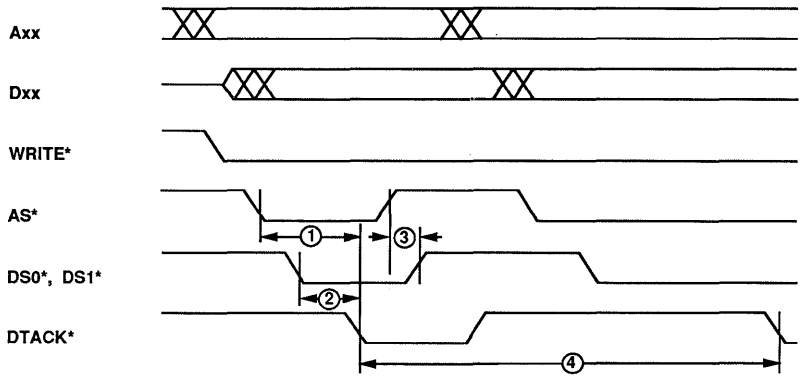


FIGURE 3-3. VME WRITE CYCLE TIMING

No.	Parameter	Min	Typ	Max	Unit	Notes
1	AS* low to DTACK* low	55	65	355	nsec	1,3
2	DSØ*/DS1* low to DTACK* low	55	65	355	nsec	3
3	DSØ*/DS1* high to data high	15	2Ø	3Ø	nsec	--
4	DTACK* low to DTACK* low	19Ø	2ØØ	435	nsec	2,3

Notes:
1) Provided that the VMEbus master drives AS* and DSØ*/DS1* low at the same time.
2) Provided that the VMEbus master drives DSØ*/DS1* low less than 4Ø nsec after receiving DTACK* low.
3) The maximum time can result if a refresh cycle has just started when the board is selected, and a VSB cycle comes before the refresh cycle is finished.

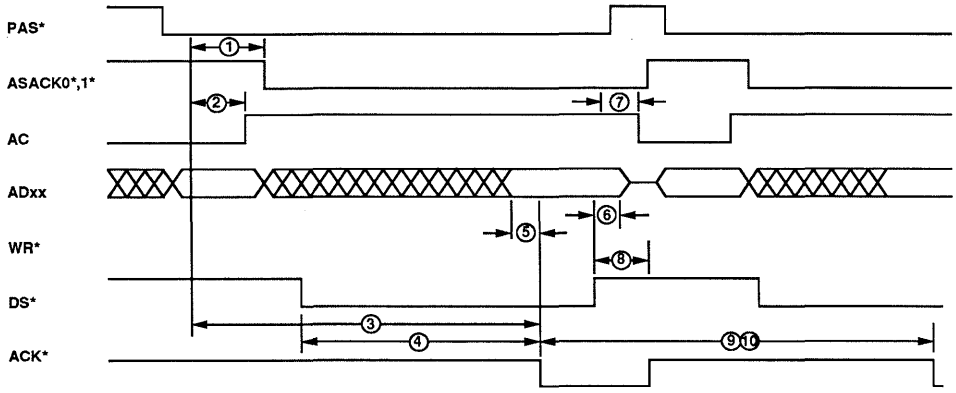


FIGURE 3-4. VSB READ CYCLE TIMING

No.	Parameter	Min	Typ	Max	Unit	Notes
1	PAS* low to ASACKØ*/ASACK1* low	5Ø	55	6Ø	nsec	--
2	PAS* low to AC high	65	75	85	nsec	--
3	PAS* low to ACK* low	165	175	47Ø	nsec	1,2
4	DS* low to ACK* low	165	175	47Ø	nsec	2,3
5	Data valid on bus to ACK* low	1Ø	15	--	nsec	--
6	PAS* high to data three-state on bus	1Ø	15	2Ø	nsec	--
7	PAS* high to AC low	1Ø	15	2Ø	nsec	--
8	PAS* high to ASACKØ*/ASACK1* high	15	2Ø	25	nsec	--
9	ACK* low to ACK* low	--	23Ø	47Ø	nsec	2,4,5
1Ø	ACK* low to ACK* low	--	3Ø5-	57Ø	nsec	2,4,6

Notes:
1) With the cache mode jumper J3 not installed, read cycles begin on PAS*. ACK will be stated time or 2Ø nsec after DS* low if PAS* low to DS* low exceeds 17Ø nsec.
2) The maximum time can result if a refresh has just started when the board is selected.
3) With the cache mode jumper J3 installed, read cycles begin on DS*. Time stated in item 4 above applies.
4) Cycle time is dependent on handshakes and speed of master changing from address to data phases. These figures represent DS* low, 75 nsec after PAS* goes low, with ACK* low to DS* high = 1Ø nsec, DS* high to ACK* high = 15 nsec, and ACK* high to PAS* low = 3Ø nsec.
5) These figures are in non-cache mode, with jumper J3 not installed.
6) These figures are in cache mode, with jumper J3 installed.

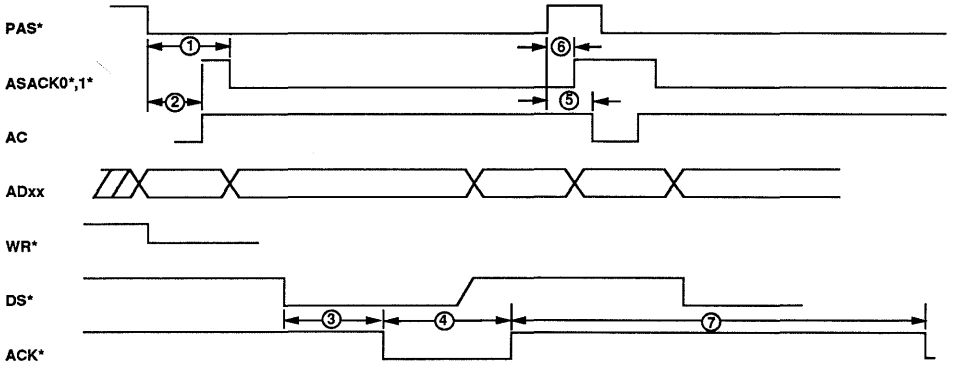


FIGURE 3-5. VSB WRITE CYCLE TIMING

No.	Parameter	Min	Typ	Max	Unit	Notes
1	PAS* low to ASACKØ*/ASACK1* low	5Ø	55	6Ø	nsec	--
2	PAS* low to AC high	65	75	85	nsec	--
3	DS* low to ACK* low	55	65	385	nsec	1
4	DS* high to ACK* high	1Ø	2Ø	3Ø	nsec	--
5	PAS* high to AC low	1Ø	15	2Ø	nsec	--
6	PAS* high to ASACKØ*/ASACK1* high	15	2Ø	25	nsec	--
7	ACK* low to ACK* low	--	2ØØ	48Ø	nsec	1,2

Notes:
1) The maximum time can result if a refresh has just started when the board is selected.
2) Cycle time is dependent on handshakes and speed of master changing from address to data phases. These figures represent DS* low, 75 nsec after PAS* goes low, with ACK* low to DS* high = 1Ø nsec, DS* high to ACK* high = 15 nsec, and ACK* high to PAS* low = 3Ø nsec.

3.4 VMEbus INTERFACE

The VMEbus interface is one of two ports to the MVME224A's DRAM array. The VMEbus interface receives address, data, and control from the VMEbus and provides access to the DRAM array and the Control and Status Register (CSR). It supports byte, word, and longword transfer and unaligned transfers. It responds to 24- or 32-bit addresses with the proper address modifier codes supplied. When responding to 24-bit address codes, the upper eight address lines are not considered. However, the upper eight address mapping

switches must be mapped to Ø (closed). Therefore, with 24-bit addressing, the module cannot be decoded higher than ØØFFFFFF. It supports 16- or 32-bit data transfers. The address modifier codes are decoded in PAL U99, which can be changed to support unique user requirements. It may be mapped to be decoded on any 1-megabyte boundary in the addressing range. It does not support block transfer on the VMEbus.

3.5 VSBbus INTERFACE

The VSBbus interface is one of two ports to the MVME224A's DRAM array. The VSBbus interface receives address, data and control information from the VSBbus and provides access to the DRAM array. It is a 32-bit address bus and supports byte, word, and longword transfers including unaligned transfers. It does support block transfers up to one megabyte.

3.6 CONTROL/STATUS REGISTER

The Control/Status Register provides a VMEbus accessible register for MVME224A status and control. This register is writable and readable from the VMEbus. The Control/Status Register bits are defined in the following text.

LDØ7	LDØ6	LDØ5	LDØ4	LDØ3	LDØ2	LDØ1	LDØØ
PES	N/U	N/U	N/U	N/U	N/U	WWP	EPD

EPD **< Enable Parity Detection>**

This bit, when set to a "1", allows parity error detection. It is used to enable or disable parity error detection. It is cleared (parity error detection disabled) on power up or reset. It is changed to a "1" when a "1" is written to this bit and cleared to a "Ø" when a "Ø" is written to this bit. When this bit is a "Ø", parity is still written according to the status of the Write Wrong Parity bit.

WWP **< Write Wrong Parity>**

This bit, when a "Ø", causes odd parity (normal) to be written to the RAMs. When set to a "1", it causes even parity (error condition) to be written to the RAMs. It is used for diagnostic purposes. It is set to a "Ø" on power up or reset, or when a "Ø" is written to this bit in the CSR. It is set to a "1" when a "1" is written to this bit in the CSR.

N/U **< Not Used Bits LDØ2-LDØ6>**

These bits are always driven to a "1". They are never cleared and are not used.

PES **< Parity Error Status>**

This bit, when set to a "1", indicates that a parity error has occurred on this module on either the VMEbus or the VSBbus. It does not indicate that the last read was a parity error, but that a parity error has occurred since it was last cleared. It is cleared to a "Ø" on power up or reset or when any write occurs to the CSR and changed to a "1" when a parity error is detected, whether parity is enabled or not.

3.7 PARITY

Parity is generated and checked on a byte wide basis. Parity is odd and is checked on each read and reported according to the state of the CSR Parity Enabled bit (bit Ø) in the form of BERR* (VMEbus) or ERR* (VSBbus).

3.8 ADDRESS SELECT - NON-INTERLEAVE MODE

Addressing is independently selectable on the VMEbus and VSBbus on 1Mb boundaries. The CSR is mapped dependent on the addressing of the RAM to the VMEbus.

When mapping to different addresses on the VMEbus and VSBbus, it must be observed that the RAM on both busses at the same address is the same RAM location, even if they have different starting addresses.

For example, if the VMEbus is mapped at ØØØØØØØØ and the VSBbus is mapped at ØØ2ØØØØØ, the RAM at ØØ2ØØØØØ will be the same RAM location on both busses. The RAM location on VME at ØØØØØØØØ is not the same as the RAM location at ØØ2ØØØØØ on the VSBbus.

Table 3-1 provides the VME/VSB mapping.

it seems MVME224 works differently than MVME204F2. the [illegible]

3

TABLE 3-1. VME/VSB ADDRESS MAPPING - NON-INTERLEAVE

VME ADDRESS MAPPING SWITCHES												VME OR VSB RAM ADDRESS (HEX)
S2-4	S2-3	S2-2	S2-1	S1-8	S1-7	S1-6	S1-5	S1-4	S1-3	S1-2	S1-1	
VSB ADDRESS MAPPING SWITCHES												
S3-8	S3-7	S3-6	S3-5	S3-4	S3-3	S3-2	S3-1	S2-8	S2-7	S2-6	S2-5	
0	0	0	0	0	0	0	0	0	0	0	0	00000000
0	0	0	0	0	0	0	0	0	0	0	1	00100000
0	0	0	0	0	0	0	0	0	0	1	0	00200000
0	0	0	0	0	0	0	0	0	0	1	1	00300000
0	0	0	0	0	0	0	0	0	1	0	0	00400000
0	0	0	0	0	0	0	0	0	1	0	1	00500000
0	0	0	0	0	0	0	0	0	1	1	0	00600000
0	0	0	0	0	0	0	0	0	1	1	1	00700000
0	0	0	0	0	0	0	0	1	0	0	0	00800000
0	0	0	0	0	0	0	0	1	0	0	1	00900000
0	0	0	0	0	0	0	0	1	0	1	0	00A00000
0	0	0	0	0	0	0	0	1	0	1	1	00B00000
0	0	0	0	0	0	0	0	1	1	0	0	00C00000
0	0	0	0	0	0	0	0	1	1	0	1	00D00000
0	0	0	0	0	0	0	0	1	1	1	0	00E00000
0	0	0	0	0	0	0	0	1	1	1	1	00F00000
0	0	0	0	0	0	0	1	0	0	0	0	01000000
0	0	0	0	0	0	0	1	0	0	0	1	01100000
0	0	0	0	0	0	0	1	0	0	1	0	01200000
0	0	0	0	0	0	0	1	0	0	1	1	01300000
0	0	0	0	0	0	0	1	0	1	0	0	01400000
0	0	0	0	0	0	0	1	0	1	0	1	01500000
0	0	0	0	0	0	0	1	0	1	1	0	01600000
0	0	0	0	0	0	0	1	0	1	1	1	01700000
0	0	0	0	0	0	0	1	1	0	0	0	01800000
0	0	0	0	0	0	0	1	1	0	0	1	01900000
0	0	0	0	0	0	0	1	1	0	1	0	01A00000
0	0	0	0	0	0	0	1	1	0	1	1	01B00000
0	0	0	0	0	0	0	1	1	1	0	0	01C00000
0	0	0	0	0	0	0	1	1	1	0	1	01D00000
0	0	0	0	0	0	0	1	1	1	1	0	01E00000
0	0	0	0	0	0	0	1	1	1	1	1	01F00000
0	0	0	0	0	0	1	0	0	0	0	0	02000000
0	0	0	0	0	1	0	0	0	0	0	0	04000000
0	0	0	0	1	0	0	0	0	0	0	0	08000000
0	0	0	1	0	0	0	0	0	0	0	0	10000000
0	0	1	0	0	0	0	0	0	0	0	0	20000000
0	1	0	0	0	0	0	0	0	0	0	0	40000000
1	0	0	0	0	0	0	0	0	0	0	0	80000000

3.9 CSR MAPPING - NON-INTERLEAVE MODE

Table 3-2 provides the switch settings for the CSR address mapping.

TABLE 3-2. CSR ADDRESS MAPPING - NON-INTERLEAVE

CSR SWITCH SETTINGS						CSR ADDRESS	RAM ADDRESSES
S1-7	S1-6	S1-5	S1-4	S1-3	S1-2		
0	0	0	0	0	0	BE01	x00xxxxx, x01xxxxx, x80xxxxx, x81xxxxx
0	0	0	0	0	1	BE05	x02xxxxx, x03xxxxx, x82xxxxx, x83xxxxx
0	0	0	0	1	0	BE09	x04xxxxx, x05xxxxx, x84xxxxx, x85xxxxx
0	0	0	0	1	1	BE0D	x06xxxxx, x07xxxxx, x86xxxxx, x87xxxxx
0	0	0	1	0	0	BE11	x08xxxxx, x09xxxxx, x88xxxxx, x89xxxxx
0	0	0	1	0	1	BE15	x0Axxxxx, x0Bxxxxx, x8Axxxxx, x8Bxxxxx
0	0	0	1	1	0	BE19	x0Cxxxxx, x0Dxxxxx, x8Cxxxxx, x8Dxxxxx
0	0	0	1	1	1	BE1D	x0Exxxxx, x0Fxxxxx, x8Exxxxx, x8Fxxxxx
0	0	1	0	0	0	BE21	x10xxxxx, x11xxxxx, x90xxxxx, x91xxxxx
0	0	1	0	0	1	BE25	x12xxxxx, x13xxxxx, x92xxxxx, x93xxxxx
0	0	1	0	1	0	BE29	x14xxxxx, x15xxxxx, x94xxxxx, x95xxxxx
0	0	1	0	1	1	BE2D	x16xxxxx, x17xxxxx, x96xxxxx, x97xxxxx
0	0	1	1	0	0	BE31	x18xxxxx, x19xxxxx, x98xxxxx, x99xxxxx
0	0	1	1	0	1	BE35	x1Axxxxx, x1Bxxxxx, x9Axxxxx, x9Bxxxxx
0	0	1	1	1	0	BE39	x1Cxxxxx, x1Dxxxxx, x9Cxxxxx, x9Dxxxxx
0	0	1	1	1	1	BE3D	x1Exxxxx, x1Fxxxxx, x9Exxxxx, x9Fxxxxx
0	1	0	0	0	0	BE41	x20xxxxx, x21xxxxx, xA0xxxxx, xA1xxxxx
0	1	0	0	0	1	BE45	x22xxxxx, x23xxxxx, xA2xxxxx, xA3xxxxx
0	1	0	0	1	0	BE49	x24xxxxx, x25xxxxx, xA4xxxxx, xA5xxxxx
0	1	0	0	1	1	BE4D	x26xxxxx, x27xxxxx, xA6xxxxx, xA7xxxxx
0	1	0	1	0	0	BE51	x28xxxxx, x29xxxxx, xA8xxxxx, xA9xxxxx
0	1	0	1	0	1	BE55	x2Axxxxx, x2Bxxxxx, xAAxxxxx, xABxxxxx
0	1	0	1	1	0	BE59	x2Cxxxxx, x2Dxxxxx, xACxxxxx, xADxxxxx
0	1	0	1	1	1	BE5D	x2Exxxxx, x2Fxxxxx, xAExxxxx, xAFxxxxx
0	1	1	0	0	0	BE61	x30xxxxx, x31xxxxx, xB0xxxxx, xB1xxxxx
0	1	1	0	0	1	BE65	x32xxxxx, x33xxxxx, xB2xxxxx, xB3xxxxx
0	1	1	0	1	0	BE69	x34xxxxx, x35xxxxx, xB4xxxxx, xB5xxxxx
0	1	1	0	1	1	BE6D	x36xxxxx, x37xxxxx, xB6xxxxx, xB7xxxxx
0	1	1	1	0	0	BE71	x38xxxxx, x39xxxxx, xB8xxxxx, xB9xxxxx
0	1	1	1	0	1	BE75	x3Axxxxx, x3Bxxxxx, xBAxxxxx, xBBxxxxx
0	1	1	1	1	0	BE79	x3Cxxxxx, x3Dxxxxx, xBCxxxxx, xBDxxxxx
0	1	1	1	1	1	BE7D	x3Exxxxx, x3Fxxxxx, xBExxxxx, xBFxxxxx
1	0	0	0	0	0	BE81	x40xxxxx, x41xxxxx, xC0xxxxx, xC1xxxxx
1	0	0	0	0	1	BE85	x42xxxxx, x43xxxxx, xC2xxxxx, xC3xxxxx
1	0	0	0	1	0	BE89	x44xxxxx, x45xxxxx, xC4xxxxx, xC5xxxxx
1	0	0	0	1	1	BE8D	x46xxxxx, x47xxxxx, xC6xxxxx, xC7xxxxx
1	0	0	1	0	0	BE91	x48xxxxx, x49xxxxx, xC8xxxxx, xC9xxxxx
1	0	0	1	0	1	BE95	x4Axxxxx, x4Bxxxxx, xCAxxxxx, xCBxxxxx
1	0	0	1	1	0	BE99	x4Cxxxxx, x4Dxxxxx, xCCxxxxx, xCDxxxxx
1	0	0	1	1	1	BE9D	x4Exxxxx, x4Fxxxxx, xCExxxxx, xCFxxxxx
1	0	1	0	0	0	BEA1	x50xxxxx, x51xxxxx, xD0xxxxx, xD1xxxxx
1	0	1	0	0	1	BEA5	x52xxxxx, x53xxxxx, xD2xxxxx, xD3xxxxx
1	0	1	0	1	0	BEA9	x54xxxxx, x55xxxxx, xD4xxxxx, xD5xxxxx
1	0	1	0	1	1	BEAD	x56xxxxx, x57xxxxx, xD6xxxxx, xD7xxxxx

TABLE 3-2. CSR ADDRESS MAPPING - NON-INTERLEAVE (cont.)

CSR SWITCH SETTINGS						CSR	RAM ADDRESSES
S1-7	S1-6	S1-5	S1-4	S1-3	S1-2	ADDRESS	
1	0	1	1	0	0	BEB1	x58xxxxx, x59xxxxx, xD8xxxxx, xD9xxxxx
1	0	1	1	0	1	BEB5	x5Axxxxx, x5Bxxxxx, xDAxxxxx, xDBxxxxx
1	0	1	1	1	0	BEB9	x5Cxxxxx, x5Dxxxxx, xDCxxxxx, xDDxxxxx
1	0	1	1	1	1	BEBD	x5Exxxxx, x5Fxxxxx, xDExxxxx, xDFxxxxx
1	1	0	0	0	0	BEC1	x60xxxxx, x61xxxxx, xE0xxxxx, xE1xxxxx
1	1	0	0	0	1	BEC5	x62xxxxx, x63xxxxx, xE2xxxxx, xE3xxxxx
1	1	0	0	1	0	BEC9	x64xxxxx, x65xxxxx, xE4xxxxx, xE5xxxxx
1	1	0	0	1	1	BECD	x66xxxxx, x67xxxxx, xE6xxxxx, xE7xxxxx
1	1	0	1	0	0	BED1	x68xxxxx, x69xxxxx, xE8xxxxx, xE9xxxxx
1	1	0	1	0	1	BED5	x6Axxxxx, x6Bxxxxx, xEAxxxxx, xEBxxxxx
1	1	0	1	1	0	BED9	x6Cxxxxx, x6Dxxxxx, xECxxxxx, xEDxxxxx
1	1	0	1	1	1	BEDD	x6Exxxxx, x6Fxxxxx, xEExxxxx, xEFxxxxx
1	1	1	0	0	0	BEE1	x70xxxxx, x71xxxxx, xF0xxxxx, xF1xxxxx
1	1	1	0	0	1	BEE5	x72xxxxx, x73xxxxx, xF2xxxxx, xF3xxxxx
1	1	1	0	1	0	BEE9	x74xxxxx, x75xxxxx, xF4xxxxx, xF5xxxxx
1	1	1	0	1	1	BEED	x76xxxxx, x77xxxxx, xF6xxxxx, xF7xxxxx
1	1	1	1	0	0	BEF1	x78xxxxx, x79xxxxx, xF8xxxxx, xF9xxxxx
1	1	1	1	0	1	BEF5	x7Axxxxx, x7Bxxxxx, xFAxxxxx, xFBxxxxx
1	1	1	1	1	0	BEF9	x7Cxxxxx, x7Dxxxxx, xFCxxxxx, xFDxxxxx
1	1	1	1	1	1	BEFD	x7Exxxxx, x7Fxxxxx, xFExxxxx, xFFxxxxx

SWITCH SETTINGS: 0 = CLOSED (ON), 1 = OPEN (OFF).
CSR ADDRESSES ARE IN SHORT I/O ADDRESS SPACE.
RAM ADDRESS: x = DON'T CARE.

3.10 ADDRESS SELECT - INTERLEAVE MODE

When operating in the interleave mode there are three restrictions.

1. Block transfer on the VSBbus is not allowed.
2. Boards must be installed in pairs.
3. Mapping is not allowed on 1Mb increments, but on blocks of double the board size.

MVME224A-1 modules configured for interleave mode must be mapped on 8Mb boundries for the pair, MVME224A-2 modules configured for interleave mode must be mapped on 16Mb boundries for the pair, MVME224A-3 modules configured for interleave mode must be mapped on 32Mb boundries for the pair, and MVME224A-4 modules configured for interleave mode must be mapped on 64Mb boundries for the pair.

3.11 CSR MAPPING - INTERLEAVE MODE

The CSR will be mapped the same as in non-interleave mode. It is still keyed to the RAM address through switch S1, positions 2 through 7. Tables 3-3 through 3-6 provide the CSR address that goes with sample RAM addresses.

The lower of the addresses goes with the module having switch S1-3 closed on the MVME224A-1, switch S1-4 closed on the MVME224A-2, switch S1-5 closed on the MVME224A-3, or switch S1-6 closed on the MVME224A-4.

The higher of the addresses goes with the module having switch S1-3 open on the MVME224A-1, switch S1-4 open on the MVME224A-2, switch S1-5 open on the MVME224A-3, or switch S1-6 open on the MVME224A-4.

Note that a closed switch denotes an ON condition, while an open switch denotes an OFF condition.

3.11.1 MVME224A-1 Mapping - Interleave

To map for interleaving on the MVME224A-1, switches S1-1, S1-2, S2-5, and S2-6 must be a "Ø" (closed) on both modules. Switches S1-3 and S2-7 must be a "Ø" (closed) on one module and a "1" (open) on the other. Switches S1-4 through S1-8 and S2-1 through S2-4 will set the beginning of the 8Mb block the pair of modules will occupy on the VMEbus. Switches S2-8 and S3-1 through S3-8 will set the beginning of the 8Mb block the pair of modules will occupy on the VSBbus. They can have the same beginning address but are not required to. Table 3-3 provides the MVME224A-1 mapping.

TABLE 3-3. MVME224A-1 ADDRESS MAPPING - INTERLEAVE

VME ADDRESS MAPPING SWITCHES									RAM BLOCK IN MEMORY MAP	CSR ADDRESS SHORT VME I/O
S2-4	S2-3	S2-2	S2-1	S1-8	S1-7	S1-6	S1-5	S1-4		
VSB ADDRESS MAPPING SWITCHES										
S3-8	S3-7	S3-6	S3-5	S3-4	S3-3	S3-2	S3-1	S2-8		
0	0	0	0	0	0	0	0	0	$00000000 - $007FFFFF	$BE01 & $BE09
0	0	0	0	0	0	0	0	1	$00800000 - $00FFFFFF	$BE11 & $BE19
0	0	0	0	0	0	0	1	0	$01000000 - $017FFFFF	$BE21 & $BE29
0	0	0	0	0	0	0	1	1	$01800000 - $01FFFFFF	$BE31 & $BE39
0	0	0	0	0	0	1	0	0	$02000000 - $027FFFFF	$BE41 & $BE49
0	0	0	0	0	0	1	0	1	$02800000 - $02FFFFFF	$BE51 & $BE59
0	0	0	0	0	0	1	1	0	$03000000 - $037FFFFF	$BE61 & $BE69
0	0	0	0	0	0	1	1	1	$03800000 - $03FFFFFF	$BE71 & $BE79
0	0	0	0	0	1	0	0	0	$04000000 - $047FFFFF	$BE81 & $BE89
0	0	0	0	0	1	0	0	1	$04800000 - $04FFFFFF	$BE91 & $BE99
0	0	0	0	0	1	0	1	0	$05000000 - $057FFFFF	$BEA1 & $BEA9
0	0	0	0	0	1	0	1	1	$05800000 - $05FFFFFF	$BEB1 & $BEB9
0	0	0	0	0	1	1	0	0	$06000000 - $067FFFFF	$BEC1 & $BEC9
0	0	0	0	0	1	1	0	1	$06800000 - $06FFFFFF	$BED1 & $BED9
0	0	0	0	0	1	1	1	0	$07000000 - $077FFFFF	$BEE1 & $BEE9
0	0	0	0	0	1	1	1	1	$07800000 - $07FFFFFF	$BEF1 & $BEF9
0	0	0	0	1	0	0	0	0	$08000000 - $087FFFFF	$BE01 & $BE09
0	0	0	0	1	0	0	0	1	$08800000 - $08FFFFFF	$BE11 & $BE19
0	0	0	0	1	0	0	1	0	$09000000 - $097FFFFF	$BE21 & $BE29
0	0	0	0	1	0	0	1	1	$09800000 - $09FFFFFF	$BE31 & $BE39

TABLE 3-3. MVME224A-1 ADDRESS MAPPING - INTERLEAVE (cont.)

VME ADDRESS MAPPING SWITCHES									RAM BLOCK IN MEMORY MAP	CSR ADDRESS SHORT VME I/O
S2-4	S2-3	S2-2	S2-1	S1-8	S1-7	S1-6	S1-5	S1-4		
VSB ADDRESS MAPPING SWITCHES										
S3-8	S3-7	S3-6	S3-5	S3-4	S3-3	S3-2	S3-1	S2-8		
0	0	0	0	1	0	1	0	0	$0A000000 - $0A7FFFFF	$BE41 & $BE49
0	0	0	0	1	0	1	0	1	$0A800000 - $0AFFFFFF	$BE51 & $BE59
0	0	0	0	1	0	1	1	0	$0B000000 - $0B7FFFFF	$BE61 & $BE69
0	0	0	0	1	0	1	1	1	$0B800000 - $0BFFFFFF	$BE71 & $BE79
0	0	0	0	1	1	0	0	0	$0C000000 - $0C7FFFFF	$BE81 & $BE89
0	0	0	0	1	1	0	0	1	$0C800000 - $0CFFFFFF	$BE91 & $BE99
0	0	0	0	1	1	0	1	0	$0D000000 - $0D7FFFFF	$BEA1 & $BEA9
0	0	0	0	1	1	0	1	1	$0D800000 - $0DFFFFFF	$BEB1 & $BEB9
0	0	0	0	1	1	1	0	0	$0E000000 - $0E7FFFFF	$BEC1 & $BEC9
0	0	0	0	1	1	1	0	1	$0E800000 - $0EFFFFFF	$BED1 & $BED9
0	0	0	0	1	1	1	1	0	$0F000000 - $0F7FFFFF	$BEE1 & $BEE9
0	0	0	0	1	1	1	1	1	$0F800000 - $0FFFFFFF	$BEF1 & $BEF9
0	0	0	1	0	0	0	0	0	$10000000 - $107FFFFF	$BE01 & $BE09
0	0	1	0	0	0	0	0	0	$20000000 - $207FFFFF	$BE01 & $BE09
0	1	0	0	0	0	0	0	0	$40000000 - $407FFFFF	$BE01 & $BE09
1	0	0	0	0	0	0	0	0	$80000000 - $807FFFFF	$BE01 & $BE09
SWITCH SETTINGS: 0 = CLOSED (ON), 1 = OPEN (OFF).										

3.11.2 MVME224A-2 Mapping - Interleave

On the MVME224A-2, switches S1-1, S1-2, S1-3, S2-5, S2-6, and S2-7 must be a "Ø" (closed) on both modules. Switches S1-4 and S2-8 must be a "1" (open) on one module and a "Ø" (closed) on the other. Switches S1-5 through S1-8 and S2-1 through S2-4 set the beginning of the 16Mb block the pair of modules will occupy on the VMEbus and must be the same on both modules. Switches S3-1 through S3-8 set the beginning of the 16Mb block the pair of modules will occupy on the VSBbus and must be the same on both modules. VMEbus and VSBbus may, but do not have to be mapped the same. Table 3-4 provides the MVME224A-2 mapping.

TABLE 3-4. MVME224A-2 ADDRESS MAPPING - INTERLEAVE

VME ADDRESS MAPPING SWITCHES								RAM BLOCK IN MEMORY MAP	CSR ADDRESS SHORT VME I/O
S2-4	S2-3	S2-2	S2-1	S1-8	S1-7	S1-6	S1-5		
VSB ADDRESS MAPPING SWITCHES									
S3-8	S3-7	S3-6	S3-5	S3-4	S3-3	S3-2	S3-1		
0	0	0	0	0	0	0	0	$00000000 - $00FFFFFF	$BE01 & $BE11
0	0	0	0	0	0	0	1	$01000000 - $01FFFFFF	$BE21 & $BE31
0	0	0	0	0	0	1	0	$02000000 - $02FFFFFF	$BE41 & $BE51
0	0	0	0	0	0	1	1	$03000000 - $03FFFFFF	$BE61 & $BE71
0	0	0	0	0	1	0	0	$04000000 - $04FFFFFF	$BE81 & $BE91
0	0	0	0	0	1	0	1	$05000000 - $05FFFFFF	$BEA1 & $BEB1
0	0	0	0	0	1	1	0	$06000000 - $06FFFFFF	$BEC1 & $BED1
0	0	0	0	0	1	1	1	$07000000 - $07FFFFFF	$BEE1 & $BEF1

TABLE 3-4. MVME224A-2 ADDRESS MAPPING - INTERLEAVE (cont.)

VME ADDRESS MAPPING SWITCHES								RAM BLOCK IN MEMORY MAP	CSR ADDRESS SHORT VME I/O
S2-4	S2-3	S2-2	S2-1	S1-8	S1-7	S1-6	S1-5		
VSB ADDRESS MAPPING SWITCHES									
S3-8	S3-7	S3-6	S3-5	S3-4	S3-3	S3-2	S3-1		
0	0	0	0	1	0	0	0	$08000000 - $08FFFFFF	$BE01 & $BE11
0	0	0	0	1	0	0	1	$09000000 - $09FFFFFF	$BE21 & $BE31
0	0	0	0	1	0	1	0	$0A000000 - $0AFFFFFF	$BE41 & $BE51
0	0	0	0	1	0	1	1	$0B000000 - $0BFFFFFF	$BE61 & $BE71
0	0	0	0	1	1	0	0	$0C000000 - $0CFFFFFF	$BE81 & $BE91
0	0	0	0	1	1	0	1	$0D000000 - $0DFFFFFF	$BEA1 & $BEB1
0	0	0	0	1	1	1	0	$0E000000 - $0EFFFFFF	$BEC1 & $BED1
0	0	0	0	1	1	1	1	$0F000000 - $0FFFFFFF	$BEE1 & $BEF1
0	0	0	1	0	0	0	0	$10000000 - $10FFFFFF	$BE01 & $BE11
0	0	1	0	0	0	0	0	$20000000 - $20FFFFFF	$BE01 & $BE11
0	1	0	0	0	0	0	0	$40000000 - $40FFFFFF	$BE01 & $BE11
1	0	0	0	0	0	0	0	$80000000 - $80FFFFFF	$BE01 & $BE11

SWITCH SETTINGS: 0 = CLOSED (ON), 1 = OPEN (OFF).

3.11.3 MVME224A-3 Mapping - Interleave

On the MVME224A-3, switches S1-1 through S1-4, and S2-5 through S2-8 must be a "Ø" (closed) on both modules. Switches S1-5 and S3-1 must be a "1" (open) on one module and a "Ø" (closed) on the other. Switches S1-6 through S1-8 and S2-1 through S2-4 set the beginning of the 32Mb block the pair of modules will occupy on the VMEbus and must be the same on both modules. Switches S3-2 through S3-8 set the beginning of the 32Mb block the pair of modules will occupy on the VSBbus and must be the same for both modules. VMEbus and VSBbus may, but do not have to be mapped the same. Table 3-5 provides the MVME224A-3 mapping.

TABLE 3-5. MVME224A-3 ADDRESS MAPPING - INTERLEAVE

VME ADDRESS MAPPING SWITCHES							RAM BLOCK IN MEMORY MAP	CSR ADDRESS SHORT VME I/O
S2-4	S2-3	S2-2	S2-1	S1-8	S1-7	S1-6		
VSB ADDRESS MAPPING SWITCHES								
S3-8	S3-7	S3-6	S3-5	S3-4	S3-3	S3-2		
0	0	0	0	0	0	0	$00000000 - $01FFFFFF	$BE01 & $BE21
0	0	0	0	0	0	1	$02000000 - $03FFFFFF	$BE41 & $BE61
0	0	0	0	0	1	0	$04000000 - $05FFFFFF	$BE81 & $BEA1
0	0	0	0	0	1	1	$06000000 - $07FFFFFF	$BEC1 & $BEE1
0	0	0	0	1	0	0	$08000000 - $09FFFFFF	$BE01 & $BE21
0	0	0	0	1	0	1	$0A000000 - $0BFFFFFF	$BE41 & $BE61
0	0	0	0	1	1	0	$0C000000 - $0DFFFFFF	$BE81 & $BEA1
0	0	0	0	1	1	1	$0E000000 - $0FFFFFFF	$BEC1 & $BEE1
0	0	0	1	0	0	0	$10000000 - $11FFFFFF	$BE01 & $BE21
0	0	1	0	0	0	0	$20000000 - $21FFFFFF	$BE01 & $BE21
0	1	0	0	0	0	0	$40000000 - $41FFFFFF	$BE01 & $BE21
1	0	0	0	0	0	0	$80000000 - $81FFFFFF	$BE01 & $BE21

SWITCH SETTINGS: 0 = CLOSED (ON), 1 = OPEN (OFF).

3.11.4 MVME224A-4 Mapping - Interleave

On the MVME224A-4, switches S1-1 through S1-5, S2-1, S2-5 through S2-8, and S3-1 must be a "Ø" (closed) on both modules. Switches S1-6 and S3-2 must be a "1" (open) on one module and a "Ø" (closed) on the other. Switches S1-7, S1-8 and S2-1 through S2-4 set the beginning of the 64Mb block the pair of modules will occupy on the VMEbus and must be mapped the same on both modules. Switches S3-3 through S3-8 set the beginning of the 64Mb block the pair of modules will occupy on the VSBbus and must be mapped the same on both modules. VMEbus and VSBbus may, but do not have to be mapped the same. Table 3-6 provides the MVME224A-4 mapping.

TABLE 3-6. MVME224A-4 ADDRESS MAPPING - INTERLEAVE

VME ADDRESS MAPPING SWITCHES						RAM BLOCK IN MEMORY MAP	CSR ADDRESS SHORT VME I/O
S2-4	S2-3	S2-2	S2-1	S1-8	S1-7		
VSB ADDRESS MAPPING SWITCHES							
S3-8	S3-7	S3-6	S3-5	S3-4	S3-3		
0	0	0	0	0	0	$00000000 - $03FFFFFF	$BE01 & $BE41
0	0	0	0	0	1	$04000000 - $07FFFFFF	$BE81 & $BEC1
0	0	0	0	1	0	$08000000 - $0BFFFFFF	$BE01 & $BE41
0	0	0	0	1	1	$0C000000 - $0FFFFFFF	$BE81 & $BEC1
0	0	0	1	0	0	$10000000 - $13DFFFFF	$BE01 & $BE41
0	0	1	0	0	0	$20000000 - $23FFFFFF	$BE01 & $BE41
0	1	0	0	0	0	$40000000 - $43FFFFFF	$BE01 & $BE41
1	0	0	0	0	0	$80000000 - $83FFFFFF	$BE01 & $BE41
SWITCH SETTINGS: 0 = CLOSED (ON), 1 = OPEN (OFF).							

CHAPTER 4 - SUPPORT INFORMATION

4.1 INTRODUCTION

This chapter provides the connector pin signal descriptions, parts list, parts location diagram, and the schematic diagram for the MVME224A-1/-2/-3/-4 memory modules.

4.2 INTERCONNECT SIGNALS

The MVME224A-1/-2/-3/-4 memory modules use the P1 and P2 backplane connectors to interconnect with VMEbus and to power the board. The P1 and P2 connectors are described in the following sections.

4.2.1 Connector P1

The P1 connector is used to interconnect with the main body of VMEbus signals. It is a standard DIN, triple row, 96-pin male connector. The pin connections, VMEbus signal mnemonics, and signal descriptions for the P1 connector are provided in Table 4-1. Refer to the ANSI/IEEE Std 1014-1987, IEEE Standard for a Versatile Backplane Bus: VMEbus for a complete description of the VMEbus signals.

TABLE 4-1. CONNECTOR P1 INTERCONNECT SIGNALS

Pin Number	Signal Mnemonic	Signal Name and Description
A1-A8	D00-D07	DATA BUS (bits 0-7) - Eight of 16 three-state bidirectional data bus signals on P1.
A9	GND	GROUND
A10	NC	NOT CONNECTED
A11	GND	GROUND
A12	DS1*	DATA STROBE 1 - A three-state driven signal that enables a data transfer with the slave. It indicates for byte/word transfers that the data transfer will occur on data bus signals D08 through D15.
A13	DS0*	DATA STROBE 0 - A three-state driven signal that enables a data transfer with the slave. It indicates for byte/word transfers that the data transfer will occur on data bus signals D00 through D07.

TABLE 4-1. CONNECTOR P1 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
A14	WRITE*	WRITE ENABLE - A three state driven signal that indicates the data transfer is a write cycle to the slave when asserted, or a read cycle from the slave when not asserted.
A15	GND	GROUND
A16	DTACK*	DATA TRANSFER ACKNOWLEDGE - An open-collector signal driven by the slave. A falling edge indicates that the slave has driven valid data on the data bus during a read cycle, or that the slave has received valid data from the data bus during a write cycle. A low level also indicates the slave may be active on the data bus.
A17	GND	GROUND
A18	AS*	ADDRESS STROBE - A three-state driven signal whose falling edge indicates a valid address is on the address bus. A low level also indicates ownership of VMEbus and the slave resource.
A19	GND	GROUND
A2Ø	IACK*	INTERRUPT ACKNOWLEDGE - A three-state driven signal that indicates an interrupt acknowledge cycle.
A21	IACKIN*	(INTERRUPT) ACKNOWLEDGE INPUT - The IACKIN* and IACKOUT* signals form an interrupt acknowledge daisy-chain to select the interrupting device to supply an interrupt vector. IACKIN* is connected to IACKOUT*.
A22	IACKOUT*	(INTERRUPT) ACKNOWLEDGE OUTPUT - The IACKIN* and IACKOUT* signals form an interrupt acknowledge daisy-chain to select the interrupting device to supply an interrupt vector. IACKOUT* is connected to IACKIN*.
A23	AM4	ADDRESS MODIFIER (bit 4) - One of six three-state driven signals that specify information about the bus cycle including address size and cycle type.

TABLE 4-1. CONNECTOR P1 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
A24-AØ	AØ7-AØ1	ADDRESS BUS (bits 7-1, reverse ordered) - Seven of 23 three-state driven address bus signals on P1. The extended 8 signals of the address bus are on connector P2.
A31	-12V	-12 Vdc POWER
A32	+5V	+5 Vdc POWER
B1-BØ3	NC	NOT CONNECTED
B4	BGØIN*	BUS GRANT Ø IN - Bus-grant-in and bus-grant-out form a daisy-chained bus grant. The remaining three bus-grant-in lines are connected directly to their respective bus-grant-out lines.
B5	BGØOUT*	BUS GRANT Ø OUT - Bus-grant-in and bus-grant-out form a daisy-chained bus grant. The remaining three bus-grant-out lines are connected directly to their respective bus-grant-in lines.
B6	BG1IN*	BUS GRANT 1 IN - Same as BGØIN on pin B4.
B7	BG1OUT*	BUS GRANT 1 OUT - Same as BGØOUT on pin B5.
B8	BG2IN*	BUS GRANT 2 IN - Same as BGØIN on pin B4.
B9	BG2OUT*	BUS GRANT 2 OUT - Same as BGØOUT on pin B5.
BIØ	BG3IN*	BUS GRANT 3 IN - Same as BGØIN on pin B4.
B11	BG3OUT*	BUS GRANT 3 OUT - Same as BGØOUT on pin B5.
B12-B15	BRØ*-BR3*	BUS REQUEST (bits Ø-3) - The bus request lines are open-collector signals generated by requesters. A low level on one of these lines indicates that some master needs to use the DTB.
B16-B19	AMØ-AM3	ADDRESS MODIFIER (bits Ø-3) - Same as pin A23.
B2Ø	GND	GROUND
B21,B22	(reserved)	NOT CONNECTED
B23	GND	GROUND

TABLE 4-1. CONNECTOR P1 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
B24-B3Ø	IRQ7*-IRQ1*	INTERRUPT REQUEST (bits 7-1, reverse ordered) - Seven open-collector signals used to request interrupt servicing.
B31	NC	NOT CONNECTED
B32	+5V	+5 Vdc POWER
C1-C8	DØ8-D15	DATA BUS (bits 8-15) - Same as pins AØ through A8.
C9	GND	GROUND
C1Ø	NC	NOT CONNECTED
C11	BERR*	BUS ERROR - An active low output signal that indicates an error has occurred during a data transfer cycle.
C12	SYSRESET*	SYSTEM RESET - An open-collector signal which, when low, causes the system to be reset.
C13	LWORD*	LONGWORD - A three-state driven signal that indicates the data transfer is a longword (32-bit transfer) aligned operation. When not asserted, it indicates a byte or word operation.
C14	AM5	ADDRESS MODIFIER 5 - Same as AM4 on pin A23.
C15-C3Ø	A23-AØ8	ADDRESS BUS (bits 23-Ø8, reverse ordered) - Sixteen of 23 three-state driven address bus signals on P1. The extended 8 signals of the address bus are on connector P2.
C31	NC	NOT CONNECTED
C32	+5V	+5 Vdc POWER

4.2.2 Connector P2

The P2 connector is used to interconnect with the extended sections of the address and data busses on the VMEbus, the VSBbus, and to additional power and ground pins. Connector P2 is a standard DIN, triple row, 96-pin male connector. Table 4-2 provides the pin connections, signal mnemonics, and signal descriptions. Refer to the ANSI/IEEE Std 1014-1987, IEEE Standard for a Versatile Backplane Bus: VMEbus for a complete description of VMEbus signals.

TABLE 4-2. CONNECTOR P2 INTERCONNECT SIGNALS

Pin Number	Signal Mnemonic	Signal Name and Description
A1	AD00	(VSBbus) ADDRESS/DATA BUS (bit 00) - One of 32 multiplexed address/data lines that are controlled by the three-state drivers on the master and slave devices. These lines are all active high, TTL three-state signals.
A2	AD02	(VSBbus) ADDRESS/DATA BUS (bit 02) - Same as AD00 on pin A1.
A3	AD04	(VSBbus) ADDRESS/DATA BUS (bit 04) - Same as AD00 on pin A1.
A4	AD06	(VSBbus) ADDRESS/DATA BUS (bit 06) - Same as AD00 on pin A1.
A5	AD08	(VSBbus) ADDRESS/DATA BUS (bit 08) - Same as AD00 on pin A1.
A6	AD10	(VSBbus) ADDRESS/DATA BUS (bit 10) - Same as AD00 on pin A1.
A7	AD12	(VSBbus) ADDRESS/DATA BUS (bit 12) - Same as AD00 on pin A1.
A8	AD14	(VSBbus) ADDRESS/DATA BUS (bit 14) - Same as AD00 on pin A1.
A9	AD16	(VSBbus) ADDRESS/DATA BUS (bit 16) - Same as AD00 on pin A1.
A10	AD18	(VSBbus) ADDRESS/DATA BUS (bit 18) - Same as AD00 on pin A1.

TABLE 4-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
A11	AD2Ø	(VSBbus) ADDRESS/DATA BUS (bit 2Ø) - Same as ADØØ on pin A1.
A12	AD22	(VSBbus) ADDRESS/DATA BUS (bit 22) - Same as ADØØ on pin A1.
A13	AD24	(VSBbus) ADDRESS/DATA BUS (bit 24) - Same as ADØØ on pin A1.
A14	AD26	(VSBbus) ADDRESS/DATA BUS (bit 26) - Same as ADØØ on pin A1.
A15	AD28	(VSBbus) ADDRESS/DATA BUS (bit 28) - Same as ADØØ on pin A1.
A16	AD3Ø	(VSBbus) ADDRESS/DATA BUS (bit 3Ø) - Same as ADØØ on pin A1.
A17	GND	GROUND
A18	NC	NOT CONNECTED
A19	DS*	(VSBbus) DATA STROBE - The falling edge of DS* indicates that a valid data transfer will occur over ADØØ through AD31. During write cycles, write data is valid at the falling edge of DS*. This line is an active low, TTL three-state signal.
A2Ø	WR*	(VSBbus) WRITE - This signal, when low, indicates that a write operation is to be performed and when high, indicates that a read operation will occur. WR* is valid when AS* is asserted on the bus. Line WR* is a TTL, three-state signal.
A21	SPACEØ	SPACE SELECT (bit Ø) - One of two lines that are driven by the active master with a space code. They are used to select one of three address spaces, or to initiate an (interrupt) ACK* or an arbitration cycle.
A22	SPACE1	SPACE SELECT (bit 1) - Same as SPACEØ on pin A21.

TABLE 4-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
A23	LOCK	(VSBbus) BUS LOCK - This signal, when low, indicates the bus is locked and that no other master can obtain possession of the bus. LOCK* is also used in certain modes to indicate that a block transfer cycle is in progress. LOCK* is an active low, TTL three-state signal.
A24	ERR*	(VSBbus) BUS ERROR - This signal, when low, is issued by the selected slave module to indicate a fault condition while attempting a data transfer operation. This would typically be the result of a parity error detected on a slave device. Line ERR* is an active low, TTL open-collector signal.
A25-A27	GND	GROUND
A28-A3Ø	NC	NOT CONNECTED
A31	BGIN*	(VSBbus) BUS GRANT IN - Bus-grant-in and bus-grant-out form a daisy-chained bus grant. Connected directly to BGOUT*.
A32	NC	NOT CONNECTED
B1	+5V	+5 Vdc POWER
B2	GND	GROUND
B3	VMELOCK*	VMEbus LOCK - This signal, when low, indicates that the bus is in the middle of a multiple-cycle access and that any other bus should be excluded from shared memory.
B4-B11	A24-A31	ADDRESS BUS (bits 24-31) - Eight three-state driven address bus signals that form the extended section of the address bus. The standard 23 signals of the address bus are on connector P1.
B12	GND	GROUND
B13	+5V	+5 Vdc POWER

TABLE 4-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
B14-B21	D16-D23	DATA BUS (bits 17-23) - Eight of 16 bidirectional three-state driven data lines which provide the expanded data path between the data transfer bus master and slave.
B22	GND	GROUND
B23-B3Ø	D24-D31	DATA BUS (bits 24-31) - Same as D16 through D23 on pins B14 through B21.
B31	GND	GROUND
B32	+5V	+5 Vdc POWER
C1	ADØ1	(VSBbus) ADDRESS/DATA BUS (bit Ø1) - Same as ADØØ on pin A1.
C2	ADØ3	(VSBbus) ADDRESS/DATA BUS (bit Ø3) - Same as ADØØ on pin A1.
C3	ADØ5	(VSBbus) ADDRESS/DATA BUS (bit Ø5) - Same as ADØØ on pin A1.
C4	ADØ7	(VSBbus) ADDRESS/DATA BUS (bit Ø7) - Same as ADØØ on pin A1.
C5	ADØ9	(VSBbus) ADDRESS/DATA BUS (bit Ø9) - Same as ADØØ on pin A1.
C6	AD11	(VSBbus) ADDRESS/DATA BUS (bit 11) - Same as ADØØ on pin A1.
C7	AD13	(VSBbus) ADDRESS/DATA BUS (bit 13) - Same as ADØØ on pin A1.
C8	AD15	(VSBbus) ADDRESS/DATA BUS (bit 15) - Same as ADØØ on pin A1.
C9	AD17	(VSBbus) ADDRESS/DATA BUS (bit 17) - Same as ADØØ on pin A1.
C1Ø	AD19	(VSBbus) ADDRESS/DATA BUS (bit 19) - Same as ADØØ on pin A1.

TABLE 4-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
C11	AD21	(VSBbus) ADDRESS/DATA BUS (bit 21) - Same as ADØØ on pin A1.
C12	AD23	(VSBbus) ADDRESS/DATA BUS (bit 23) - Same as ADØØ on pin A1.
C13	AD25	(VSBbus) ADDRESS/DATA BUS (bit 25) - Same as ADØØ on pin A1.
C14	AD27	(VSBbus) ADDRESS/DATA BUS (bit 27) - Same as ADØØ on pin A1.
C15	AD29	(VSBbus) ADDRESS/DATA BUS (bit 29) - Same as ADØØ on pin A1.
C16	AD31	(VSBbus) ADDRESS/DATA BUS (bit 31) - Same as ADØØ on pin A1.
C17-C2Ø	GND	GROUND
C21	SIZEØ*	(VSBbus) BUS SIZE (bit Ø) - One of two lines that in conjunction with address AØØ, determines the active portion of the data bus. This line is an active low, TTL three-state signal.
C22	PAS*	(VSBbus) ADDRESS STROBE - The falling edge of PAS* indicates that a valid address is present on the ADØØ through AD31 bus. This line is an active low, TTL three-state signal.
C23	SIZE1*	(VSBbus) BUS SIZE (bit 1) - Same as SIZEØ on pin C21.
C24	GND	GROUND
C25	ACK*	(VSBbus) DATA TRANSFER ACKNOWLEDGE - This signal is issued by a slave device to complete the handshake for a data transfer operation. This line is an active low, TTL open-collector signal.
C26	AC	(VSBbus) ADDRESS DECODE COMPLETE - This signal is issued by a slave device to indicate that address decoding has been completed. All slave devices

TABLE 4-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
		must allow AC (Address Decode Complete) to go high after the decode interval has elapsed regardless whether the device is selected by the current address on the bus. This line is an active high, TTL open-collector signal.
C27	ASACK1*	(VSBbus) ADDRESS/SIZE ACKNOWLEDGE (bit 1) - One of two lines that are driven by the VSBbus slave devices and are used to perform several functions. The slave device that is selected by the address decoding must drive at least one ASACK* signal to control switching the multiplexed address/data bus from address to data. Secondly, both are encoded to indicate to the master the size of the data bus for the slave module. Finally, ASACK* can be gated with the signal AC (Address Decode Complete) on the master device. The condition of AC active and ASACK* inactive, while AS* is asserted, is defined to indicate that no VSBbus slave module has decoded the address being driven at that time, or that there are no VSBbus slave modules installed. This provides the VSBbus master the opportunity to switch to the VMEbus when VSBbus slaves are not responding. ASACKØ* and ASACK1* are active low, TTL open-collector signals.
C28	ASACKØ*	(VSBbus) ADDRESS/SIZE ACKNOWLEDGE (bit Ø) - Same as ASACK1* on pin C27.
C29	CACHE*	(VSBbus) CACHEABLE - CACHE* is issued by a slave device at the same time that ASACKØ* and ASACK1* are issued to indicate that the current transfer is cacheable. CACHE* remains inactive to indicate that the transfer is non-cacheable. This line is an active low, TTL open-collector signal.
C3Ø	WAIT*	(VSBbus) HOLD THIS CYCLE - This signal is an output line used in conjunction with the signals AC. If this line is driven low at the beginning of a cycle, addresses must remain stable and DS* remain stable and DS* cannot be driven until AC

TABLE 4-2. CONNECTOR P2 INTERCONNECT SIGNALS (cont.)

Pin Number	Signal Mnemonic	Signal Name and Description
		goes high. Also, data must remain valid along with DS* during the data transfer portion of the cycle until WAIT* is negated. This signal is an active low TTL open-collector signal.
C31	NC	NOT CONNECTED (on MVME224A).
C32	BGOUT*	(VSBbus) BUS GRANT OUT - Bus-grant-in and bus-grant-out form a daisy-chained bus grant. Connected directly to BGIN*.

4.3 PARTS LIST

The parts location diagram for the MVME224A is provided in Figure 4-1. The reference designation, part number, and description for each component are listed in Table 4-3. This parts list reflects the latest issue of the MVME224A hardware at the time of the release of this user's manual.

TABLE 4-3. MVME224A PARTS LIST

Reference Designation	Motorola Part Number	Description
--	84-W8588BØ1A	Printed wiring board assembly, MVME224A
C1-7, C1Ø-16	21NW9632AØ3	Capacitor, ceramic, axial, .1MF, 5Ø Vdc
C8	21NW96Ø4A58	Capacitor, ceramic, radial, 33ØpF, 5Ø Vdc
C9	21SW992CØ14	Capacitor, ceramic, .Ø1ØMF, 5Ø Vdc
C17-2Ø	23NW9618A82	Capacitor, electrolytic, radial, 22MF, 25 Vdc
C21-97	21NW9711AØ2	Capacitor, ceramic, SMD, .1MF, 5Ø Vdc
DL1,DL3	51NW9615Y91	IC, DS1Ø1Ø-1ØØ
DL2	51NW9615Z43	IC, DS1Ø13-4Ø
DL4	51NW9615W46	IC, DS1ØØØM-5Ø
DL5	51NW9615Y51	IC, DS1Ø13M-3Ø
DS1,DS2	48NW9612A59	LED, green
P1,P2	28NW98Ø2E51	Connector, 96-pin, plug, PWB
--	Ø5NW9ØØ7A26	Eyelet, Ø.Ø89-inch OD x Ø.344-inch long (4 req'd)(used with P1 and P2)
R1,R2	Ø6SW-962A29	Resistor, film, 1/8W, 5%, 15Ø ohms
R3,R4,R7, R8,R11	51NW9626B94	Resistor network, SIP, four 33 ohms **(for MVME224A-1/-3 versions only)**
R3,R4, R7-R11, R13-15	51NW9626B94	Resistor network, SIP, four 33 ohms **(for MVME224A-2/-4 versions only)**

TABLE 4-3. MVME224A PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
R5	51NW9626B75	Resistor network, SIP, seven 1ØK ohms
R6,R16-22	51NW9626B56	Resistor network, SIP, nine 1ØK ohms
R12	Ø6SW-124A81	Resistor, film, 1/8W, 5%, 22K ohms
R23	51NW9626CØ5	Resistor network, SIP, nine 22K ohms
S1-3	4ØNW98Ø1A34	Switch, DIP, SPST, 8-position
U1	51NW9615K47	IC, 74F244PC **(for MVME224A-1/-3 versions only)**
U1,U51	51NW9615K47	IC, 74F244PC **(for MVME224A-2/-4 versions only)**
U2-19, U27-44	51NW9615U44	IC, TC511ØØØAZ-1Ø **(for MVME224A-1/-3 versions only)**
U2-19, U27-44, U52-69, U76-93	51NW9615U44	IC, TC511ØØØAZ-1Ø **(for MVME224A-2/-4 versions only)**
U2Ø,U45, U7Ø	51NW9615K6Ø	IC, 74F158APC **(for MVME224A-1/-3 versions only)**
U2Ø,U21, U45,U7Ø, U71,U94	51NW9615K6Ø	IC, 74F158APC **(for MVME224A-2/-4 versions only)**
--	Ø9-W58Ø6BØ2	Socket, IC, DIL, 16-pin (1 req'd)(used at U21) **(for MVME224A-2/-4 versions only)**
U22	51NW9615K72	IC, 74FØ2PC
U23,U24, U122,U123, U134,U135, U148,U149	51NW9615R36	IC, 74F543SPC
U25	51-W5889BØ4	IC, programmed

TABLE 4-3. MVME224A PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
U26	51-W5889BØ5	IC, programmed (for MVME224A-1/-3 versions only)
U26	51-W5889BØ6	IC, programmed (for MVME224A-2/-4 versions only)
U46	51-W5855B13	IC, programmed
--	Ø9-W58Ø6BØ2	Socket, IC, DIL, 24-pin (1 req'd)(used at U46) (for MVME224A-2/-4 versions only)
U47	51-W5388B39	IC, programmed
U48	51-W5856B11	IC, programmed
U49,U74, U75,U121, U132,U133	51NW9615K99	IC, 74F374PC
U5Ø	51NW9615B65	IC, MC1455P1
U72	51AW4591D24	IC, programmed
U73	51-W5855B12	IC, programmed
U95,U145, U146	51NW9615F85	IC, SN74S38N
U96	51-W5388B67	IC, programmed (for MVME224A-1/-2 versions only)
U96	51-W5388B68	IC, programmed (for MVME224A-3 version only)
U96	51-W5388B69	IC, programmed (for MVME224A-4 version only)
U97	51-W5388B31	IC, programmed (for MVME224A-1 version only)
U97	51-W5388B34	IC, programmed (for MVME224A-2/-3/-4 versions only)

TABLE 4-3. MVME224A PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
U98	51-W5855B1Ø	IC, programmed **(for MVME224A-1 version only)**
U98	51-W5855B11	IC, programmed **(for MVME224A-2 version only)**
U98	51-W5855B41	IC, programmed **(for MVME224A-3 version only)**
U98	51-W5855B43	IC, programmed **(for MVME224A-4 version only)**
U99	51-W5388B37	IC, programmed
--	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U99)
U1ØØ	51NW9615R16	IC, SN74ALSØ4AN
U1Ø1	51-W48Ø4D1Ø	IC, programmed **(for MVME224A-1/-3 versions only)**
U1Ø1	51-W48Ø4D36	IC, programmed **(for MVME224A-2/-4 versions only)**
U1Ø2,U1Ø4	51NW9615K18	IC, 74F373PC
U1Ø3,U1Ø5	51NW9615W31	IC, SN74AS841NT
U1Ø6,U1Ø7	51NW9615M9Ø	IC, 74F245PC
U1Ø8,U1Ø9, U119,U12Ø	51NW9615V91	IC, SN74AS28ØN
U11Ø	51NW9615K65	IC, 74F64PC
U111	51NW9615C24	IC, SN74LS32N
U112	51-W5388B62	IC, programmed
U113	51AW5889BØ7	IC, programmed
U114	51-W5856B18	IC, programmed

TABLE 4-3. MVME224A PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
U115	51AW512ØB75	IC, programmed
U116	51-W48Ø4C91	IC, programmed
U117	51-W5552B17	IC, programmed
U118	51-W5473BØ8	IC, programmed
U124	51NW9615K71	IC, 74FØ4PC
U125,U137	51NW9615K73	IC, 74FØØPC
U126-13Ø, U138	51NW9615J39	IC, 74F74PC
U131	51-W5855B14	IC, programmed (for MVME224A-1 version only)
U131	51-W5855B15	IC, programmed (for MVME224A-2 version only)
U131	51-W5855B47	IC, programmed (for MVME224A-3/-4 versions only)
U136	51NW9615K7Ø	IC, 74FØ8PC
U139	51AW51ØØB21	IC, programmed
--	Ø9-W58Ø6BØ6	Socket, IC, DIL, 24-pin (1 req'd)(used at U139)
U14Ø	51-W5889BØ1	IC, programmed
U141	51-W5889BØ2	IC, programmed
U142	51-W5855B18	IC, programmed (for MVME224A-1 version only)
U142	51-W5855B19	IC, programmed (for MVME224A-2 version only)
U142	51-W5855B42	IC, programmed (for MVME224A-3 version only)

TABLE 4-3. MVME224A PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
U142	51-W5855B44	IC, programmed **(for MVME224A-4 version only)**
--	Ø9NW9811BØ1	Socket, IC, DIL, 24-pin (1 req'd)(used at U142)
U143	51-W5855B16	IC, programmed
U144	51-W5855B17	IC, programmed
U147	51-W5889BØ3	IC, programmed
--	Ø9-W58Ø6BØ6	Socket, IC, DIL, 24-pin (1 req'd)(used at U147)
--	67NW9415A17	Kit, ejector handle, 6U component
--	29NW98Ø5B17	Jumper, insulated, shorting (4 req'd)[used at J1(1-2,3-4,5-6,7-8)]
--	29NW9814AØ1	Jumper, SMD, autoinsert, insulated (11 req'd)[used at R33,R39,R45,R51]
--	29NW9814AØ1	Jumper, SMD, autoinsert, insulated (11 req'd)[used at R24,R3Ø,R33,R34,R38, R39,R42,R45,R46,R5Ø,R51] **(for MVME224A-1 version only)**
--	29NW9814AØ1	Jumper, SMD, autoinsert, insulated (11 req'd)[used at R26,R28,R32,R33,R36, R39,R4Ø,R44,R45,R48,R51] **(for MVME224A-2 version only)**
--	29NW9814AØ1	Jumper, SMD, autoinsert, insulated (12 req'd)[used at R26,R27,R31,R32,R35, R38,R39,R43,R44,R47,R5Ø,R51] **(for MVME224A-3 version only)**
--	29NW9814AØ1	Jumper, SMD, autoinsert, insulated (11 req'd)[used at R25,R26,R29,R32,R33, R37,R38,R41,R44,R45,R49,R5Ø] **(for MVME224A-4 version only)**
--	64-W55Ø1BØ1A	Panel, front, MVME224A

TABLE 4-3. MVME224A PARTS LIST (cont.)

Reference Designation	Motorola Part Number	Description
--	29NW98Ø5CØ7	Pin, Ø.Ø25-inch square, gold, autoinsert (14 req'd)[used at J1(1-8),J2(1-2),J3(1-2), J4(1-2)]
--	33-W5Ø89BØ1	Nameplate, Scanbe, logo
--	33-W6Ø73BØ1A	Nameplate, MVME224A-1 **(for MVME224A-1 version only)**
--	33-W6Ø73BØ2A	Nameplate, MVME224A-2 **(for MVME224A-2 version only)**
--	33-W6Ø73BØ3A	Nameplate, MVME224A-3 **(for MVME224A-3 version only)**
--	33-W6Ø73BØ4A	Nameplate, MVME224A-4 **(for MVME224A-4 version only)**
--	Ø3NW9ØØ4B48	Screw, captive, M2.5 (2 req'd)

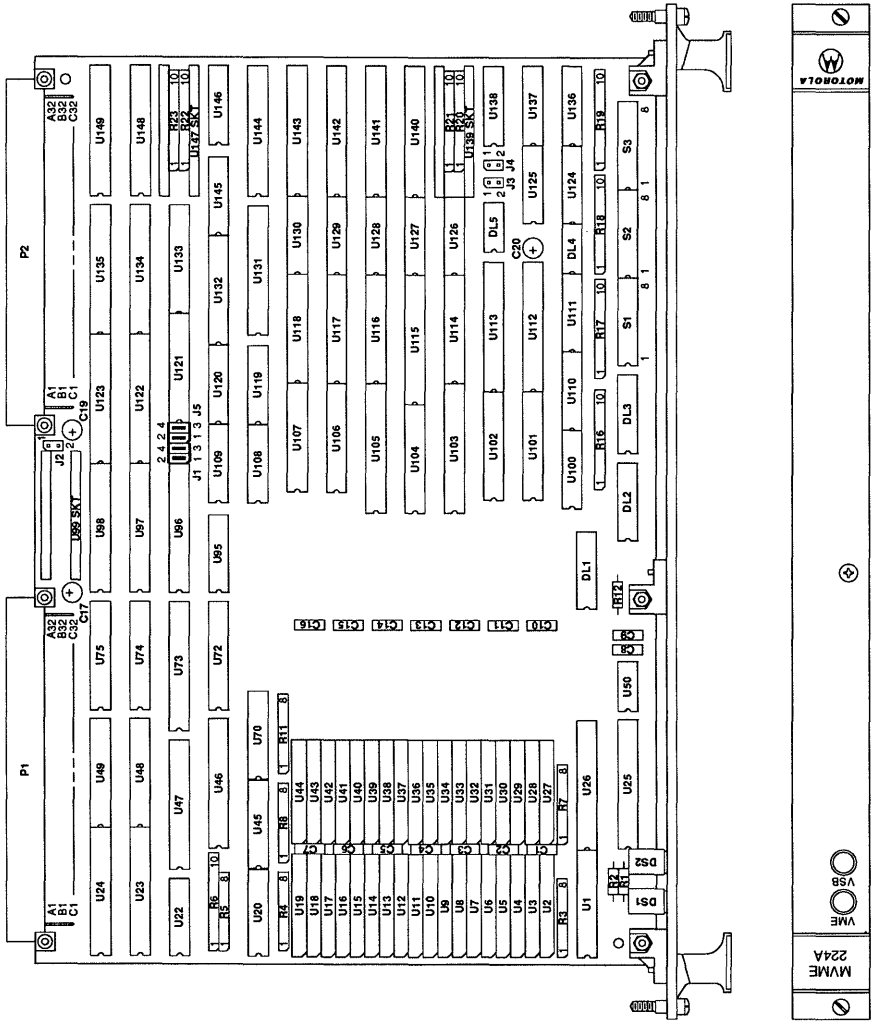


FIGURE 4-1. MVME224A PARTS LOCATION DIAGRAM

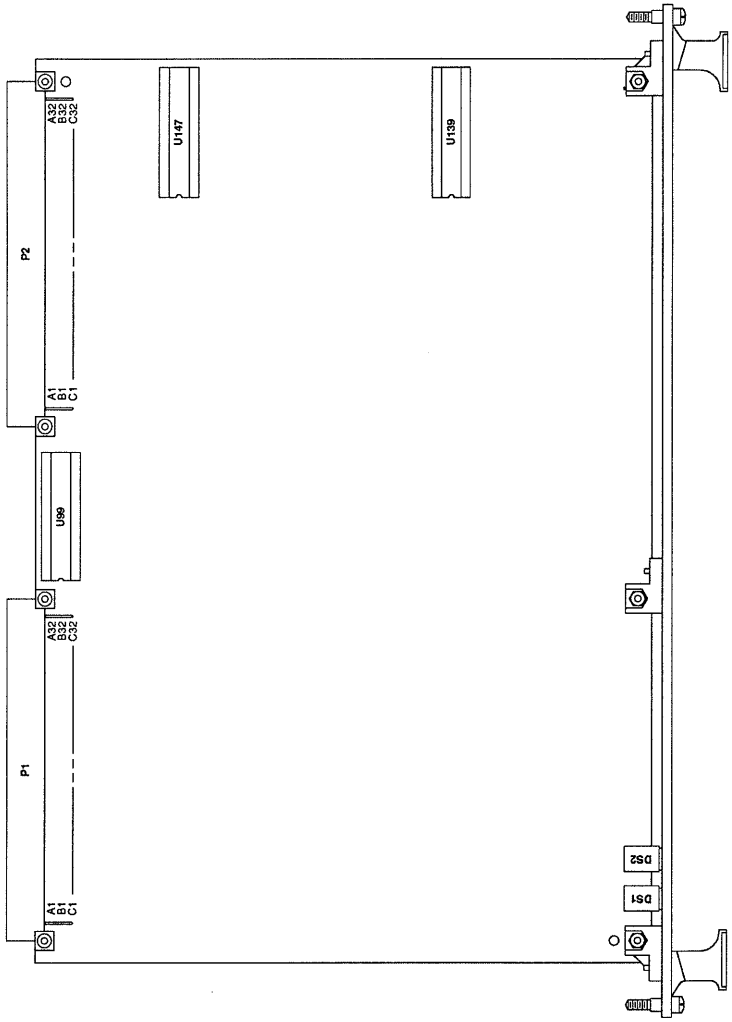


FIGURE 4-1. MVME224A PARTS LOCATION DIAGRAM (cont.)

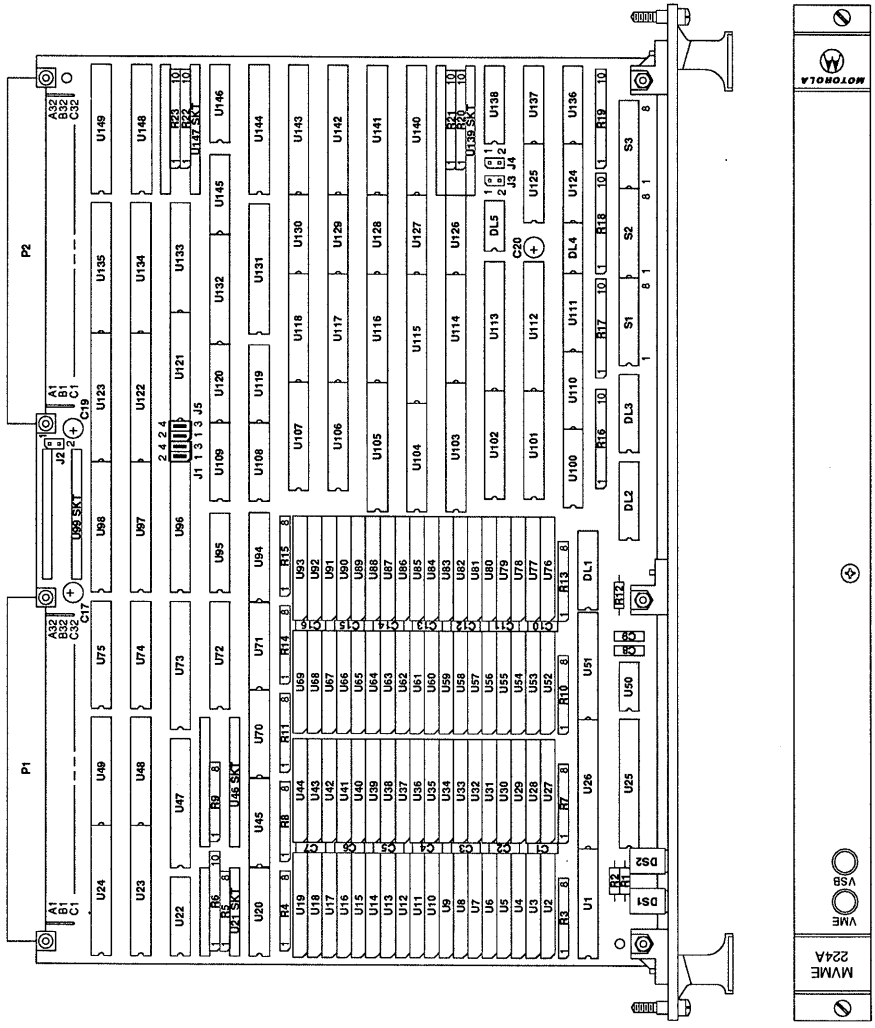


FIGURE 4-1. MVME224A PARTS LOCATION DIAGRAM (cont.)

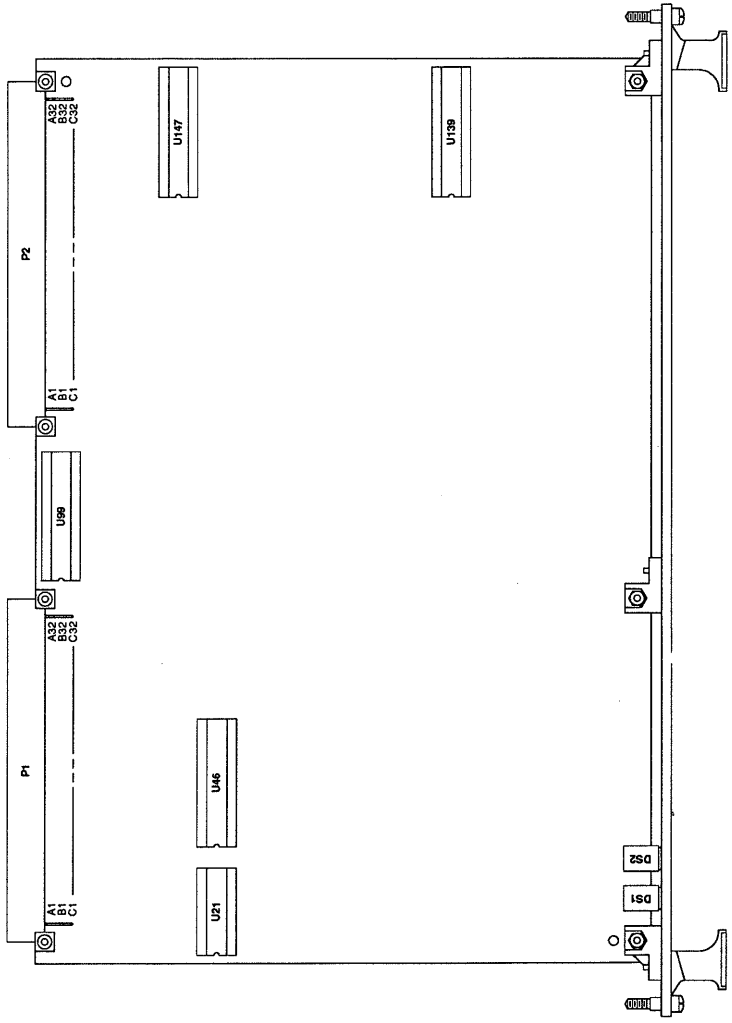


FIGURE 4-1. MVME224A PARTS LOCATION DIAGRAM (cont.)

4.4 SCHEMATIC DIAGRAMS

Figure 4-2 (25 sheets) contains detailed schematic diagrams of the internal circuitry comprising the MVME224A. These schematic diagrams represent the lastest design. Occasionally, minor component changes are made at the factory. Therefore, when replacing a component, always use the same value as the defective component even though the schematic diagram may indicate a different value or type.

NOTES:

1. FOR REFERENCE DRAWINGS REFER TO

   CURRENT REVISION/CONFIGURATION APPLIES.
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, +/- 5PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UF.
   ALL VOLTAGES ARE DC.
   ALL DELAYS ARE IN NS.
3. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
4. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
5. SPECIAL SYMBOL USAGE:
   * DENOTES - ACTIVE LOW SIGNAL.
   <> DENOTES - VECTORED SIGNALS.
6. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION, WITH THE EXCEPTION OF LOGIC BLOCK SYMBOLOGY.
7. CODE FOR SHEET TO SHEET REFERENCES IS AS FOLLOWS:

   <SHEET> S C7 <ZONE>

REF DES	TYPE (4)	GND	VCC
DL1	DELAY10	7	14
DL2	DLY3	7	14
DL3	DELAY10	7	14
DL4	DELAY5M	4	8
DL5	DLY2PD	4	8
U1	F244	10	20
U2	M5M4C2000L	4	15
THRU	M5M4C2000L	4	15
U19	M5M4C2000L	4	15
U20	F258	8	16
U21	F258	8	16
U22	F02	7	14
U23	F543	12	24
U24	F543	12	24
U25	RASPAL	12	24
U26	T0PAL	12	24
U27	M5M4C2000L	4	15
THRU	M5M4C2000L	4	15
U44	M5M4C2000L	4	15
U45	F258	8	16
U46	CTR2	12	24
U47	CTR3	12	24
U48	VMEADD	10	20
U49	F374	10	20
U50	MC1455	1	8
U51	F244	10	20
U52	M5M4C2000L	4	15
THRU	M5M4C2000L	4	15
U69	M5M4C2000L	4	15
U70	F258	8	16
U71	F258	8	16
U72	BLOCKDETECT	10	20
U73	CTR1	12	24
U74	F374	10	20
U75	F374	10	20
U76	M5M4C2000L	4	15
THRU	M5M4C2000L	4	15
U93	M5M4C2000L	4	15
U94	F258	8	16
U95	S38	7	14
U96	VMEDECODE2	12	24
U97	VMEDECODE1	12	24
U98	VMEDECODE4	12	24
U99	VMEDECODE3	12	24
U100	AL504	7	14
U101	WRITEPAL	10	20
U102	F373	10	20
U103	A5841	12	24
U104	F373	10	20
U105	A5841	12	24
U106	F245	10	20
U107	F245	10	20
U108	A5280	7	14
U109	A5280	7	14
U110	F54	7	14
U111	F32	7	14
U112	BYTEPAL	12	24
U113	ADDRESSPAL	12	24
U114	LOGICPAL	10	20
U115	20L8	12	24

REF DES	TYPE (4)	GND	VCC
U116	REQPAL	10	20
U117	ARBPAL	10	20
U118	PARITY	10	20
U119	AS280	7	14
U120	AS280	7	14
U121	F374	10	20
U122	F543	12	24
U123	F543	12	24
U124	F04	7	14
U125	F00	7	14
U126	F74	7	14
THRU	F74	7	14
U130	F74	7	14
U131	VSBDECODE1	12	24
U132	F374	10	20
U133	F374	10	20
U134	F543	12	24
U135	F543	12	24
U136	F08	7	14
U137	F00	7	14
U138	F74	7	14
U140	VME_BUS	12	24
U141	VSB_BUS	12	24
U142	VSBDECODE4	12	24
U143	VSBDECODE2	12	24
U144	VSBDECODE3	12	24
U145	S38	7	14
U146	S38	7	14
U147	VSBADD	12	24
U148	F543	12	24
U149	F543	12	24

REF DES	SH
?0	2
C1	2
THRU	2
C7	2
C8	13
C9	13
C10	2
THRU	2
C97	2
DL1	14
DL2	14
DL3	14
DL4	10
DL5	7
DL5	9
DL5	10
DS1	15
DS2	15
J1	8
J2	13
J3	10
J4	8
J5	11
P1	3
P2	4
R1	15
R2	15
R3	14
R4	18
R5	8
R5	11
R5	15
P5	16
R6	2
R6	7
R6	8
P6	17
R7	14
R8	18
R9	2
R9	18
R10	14
R11	2
P11	18
R12	13
R13	14
R14	18
R15	18
R16	6
R16	11
R16	12
R16	13
R16	14
R16	15
R17	2
R17	8
R18	8
R18	11
R19	11
R20	13

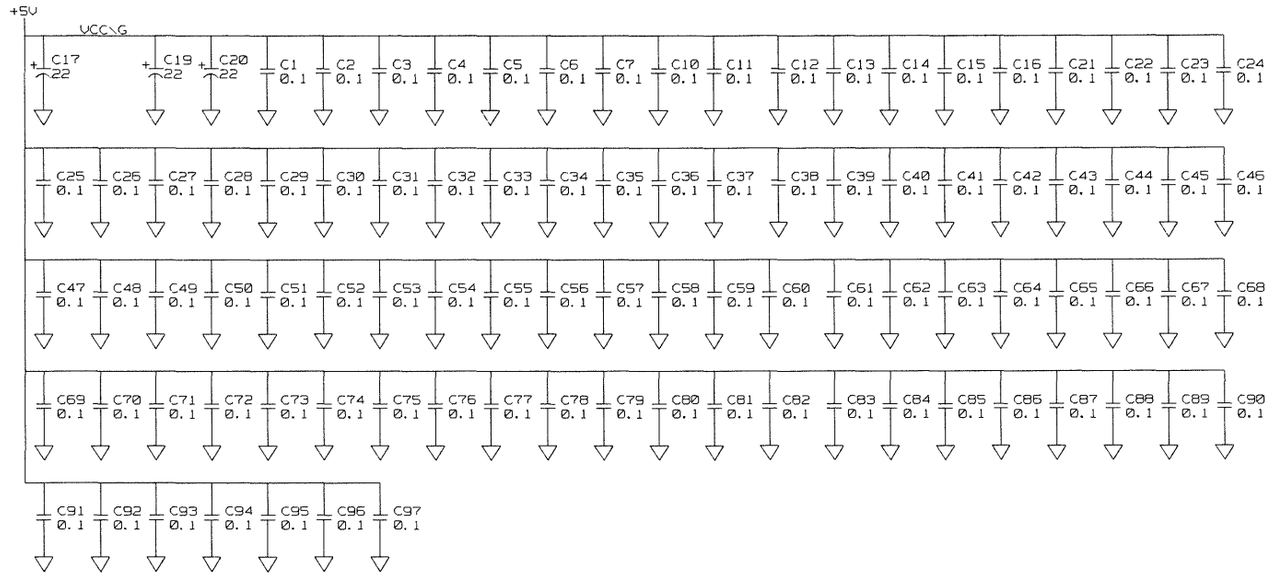
REF DES	SH
R20	14
R20	15
R20	16
R20	17
R21	6
R21	15
R22	8
R22	9
R22	10
R22	19
R23	2
R23	6
R23	10
R23	11
R23	13
R24	18
THRU	18
R27	18
R28	8
THRU	8
R39	8
R40	11
THRU	11
P51	11
S1	8
S2	8
S3	11
U1	14
U2	25
U3	25
U4	22
THRU	22
U11	22
U12	21
THRU	21
U19	21
U20	18
U21	18
U22	2
U22	9
U23	6
U24	6
U25	14
U26	14
U27	25
U28	25
U29	22
THRU	22
U36	22
U37	21
THRU	21
U44	21
U45	18
U46	17
U47	17
U48	7
U49	7
U50	13
U51	14
U52	25

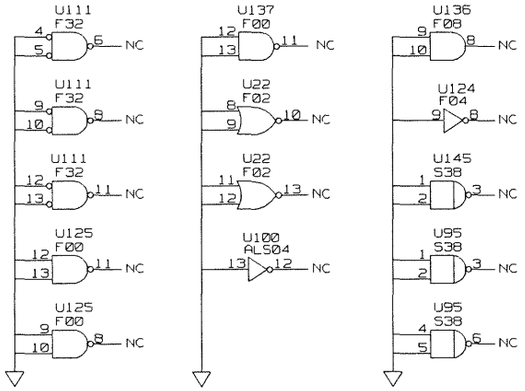
REF DES	SH
U53	25
U54	24
THRU	24
U61	24
U62	23
THRU	23
U69	23
U70	18
U71	18
U72	17
U73	17
U74	7
U75	7
U76	25
U77	25
U78	24
THRU	24
U85	24
U86	23
THRU	23
U93	23
U94	18
U95	2
U95	6
U96	8
THRU	8
U99	8
U100	2
U100	7
U100	12
U100	13
U101	16
U102	20
THRU	20
U105	20
U106	12
U107	12
U108	19
U109	19
U110	19
U111	14
U112	16
U113	16
U114	16
U115	17
U116	15
U117	15
U118	19
U119	19
U120	19
U121	10
U122	9
U123	9
U124	2
U124	10
U124	14
U125	2
U125	7
U125	10
U126	13

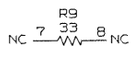
REF DES	SH
U126	17
U127	15
U128	15
U129	15
U130	9
U131	11
U132	10
U133	10
U134	9
U135	9
U136	2
U136	9
U136	10
U136	17
U137	9
U137	14
U138	6
U139	13
U140	6
U141	9
U142	11
U143	11
U144	11
U145	2
U145	9
U146	9
U146	10
U147	10
U148	6
U149	6

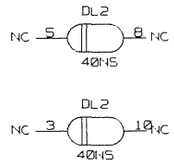
63DW3588B0C REV A SH 1 OF 25

FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 1 OF 25)



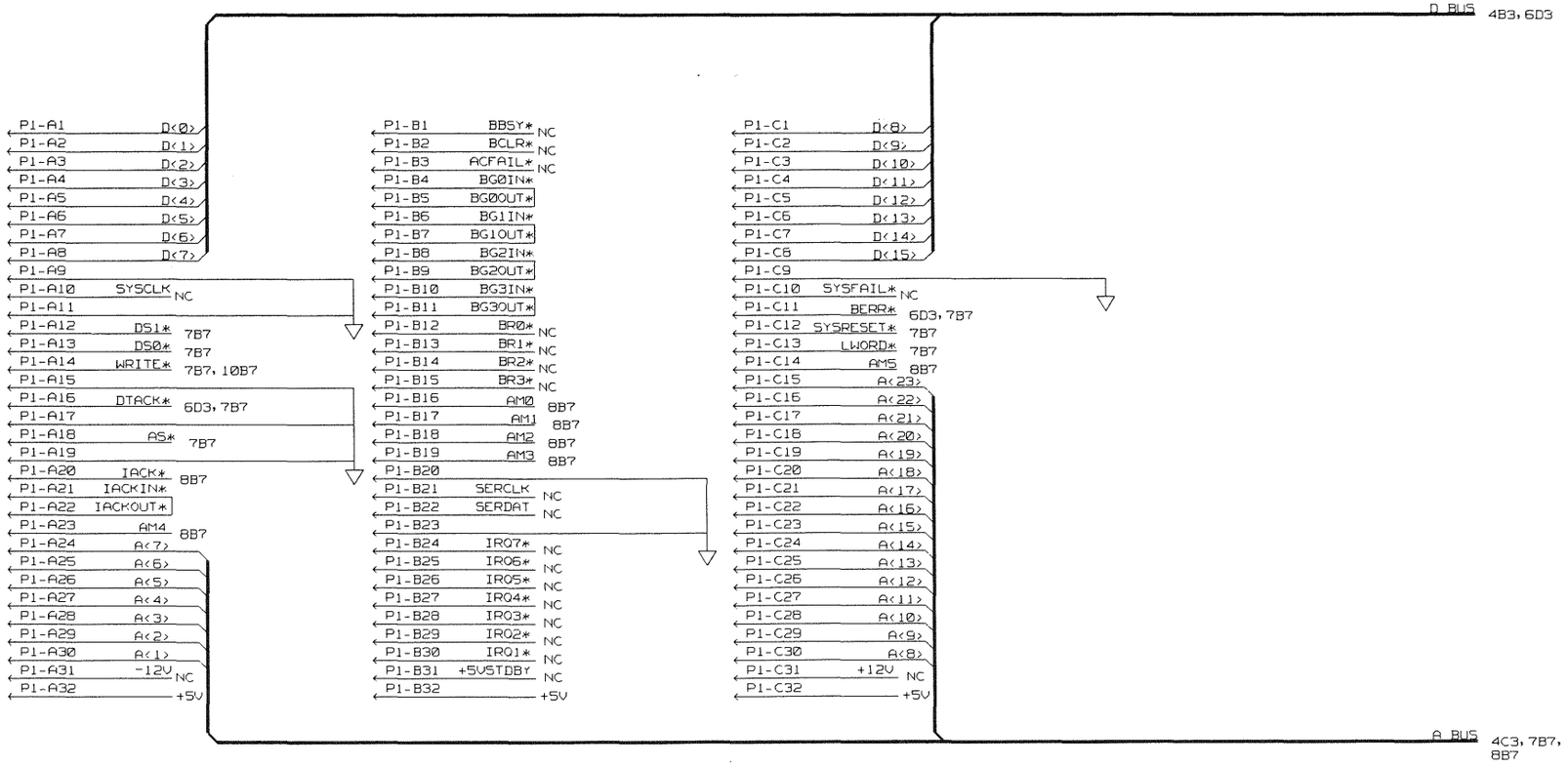






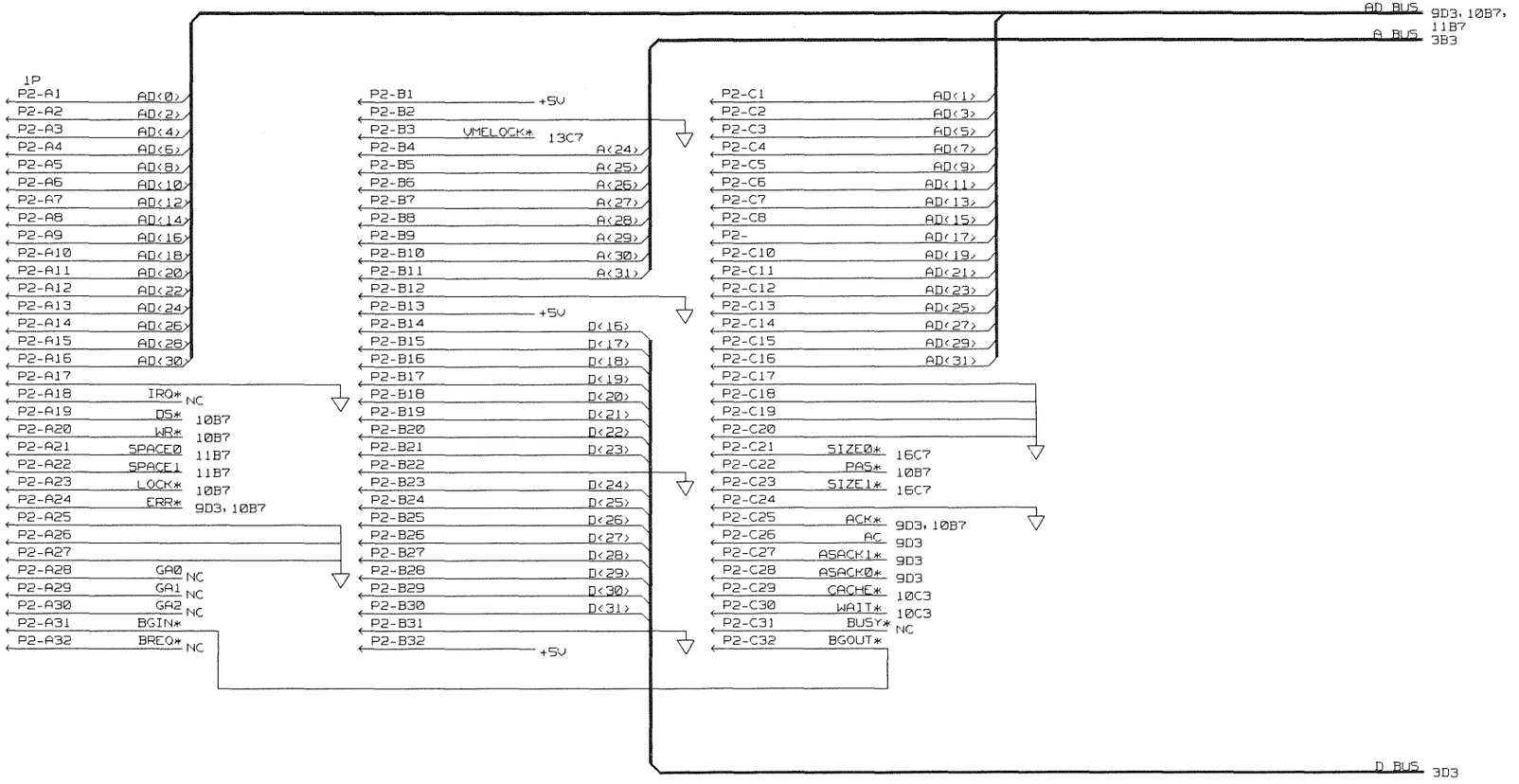
SPARES AND BYPASS CAPS
63DW3588B0C REV A SH 2 OF 25

FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 2 OF 25)



P1 CONNECTOR
63DW3588B0C REV A SH 3 OF 25

FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 3 OF 25)



P2 CONNECTOR
63DW3588B0C REV A SH 4 OF 25

FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 4 OF 25)

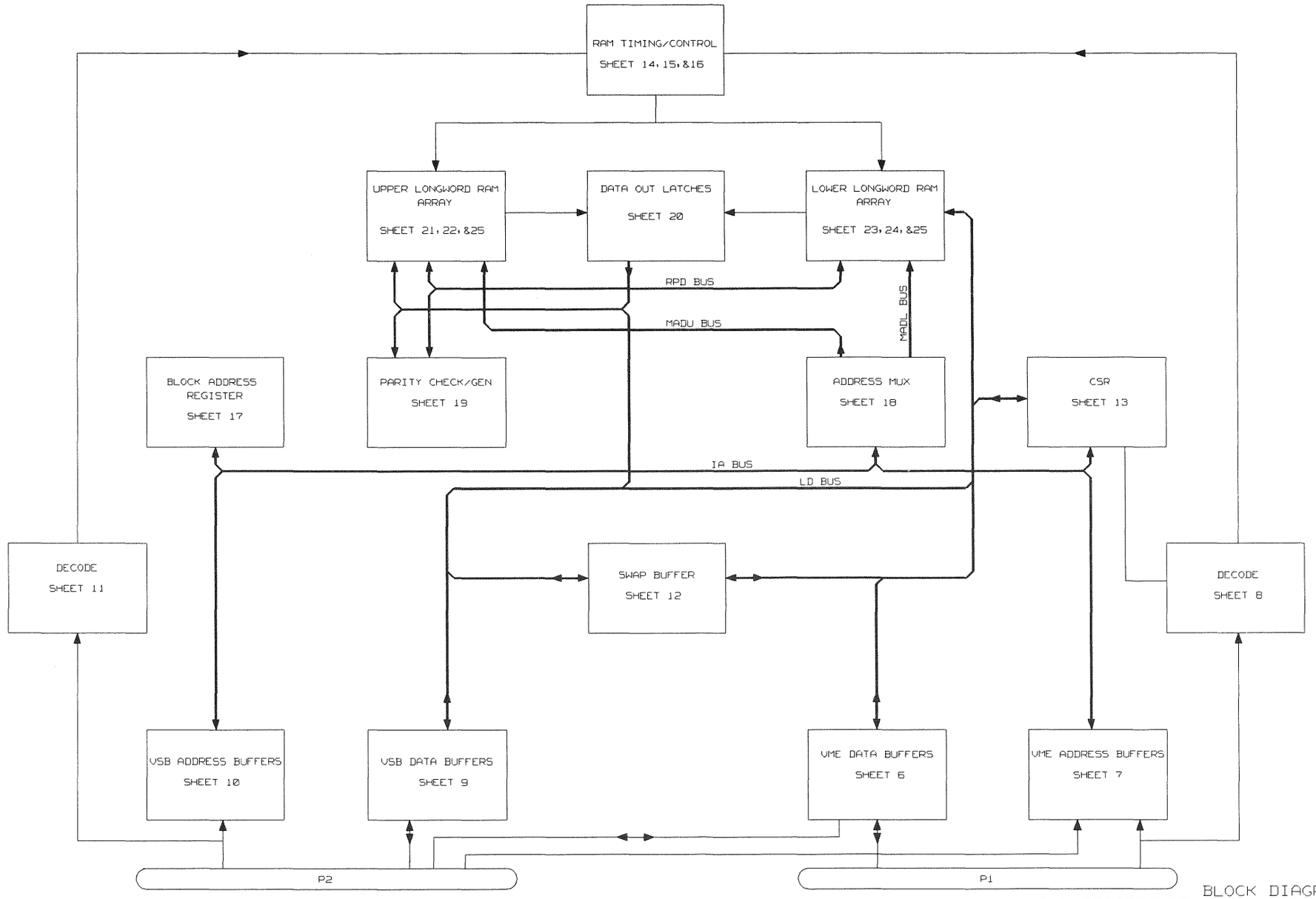


FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 5 OF 25)

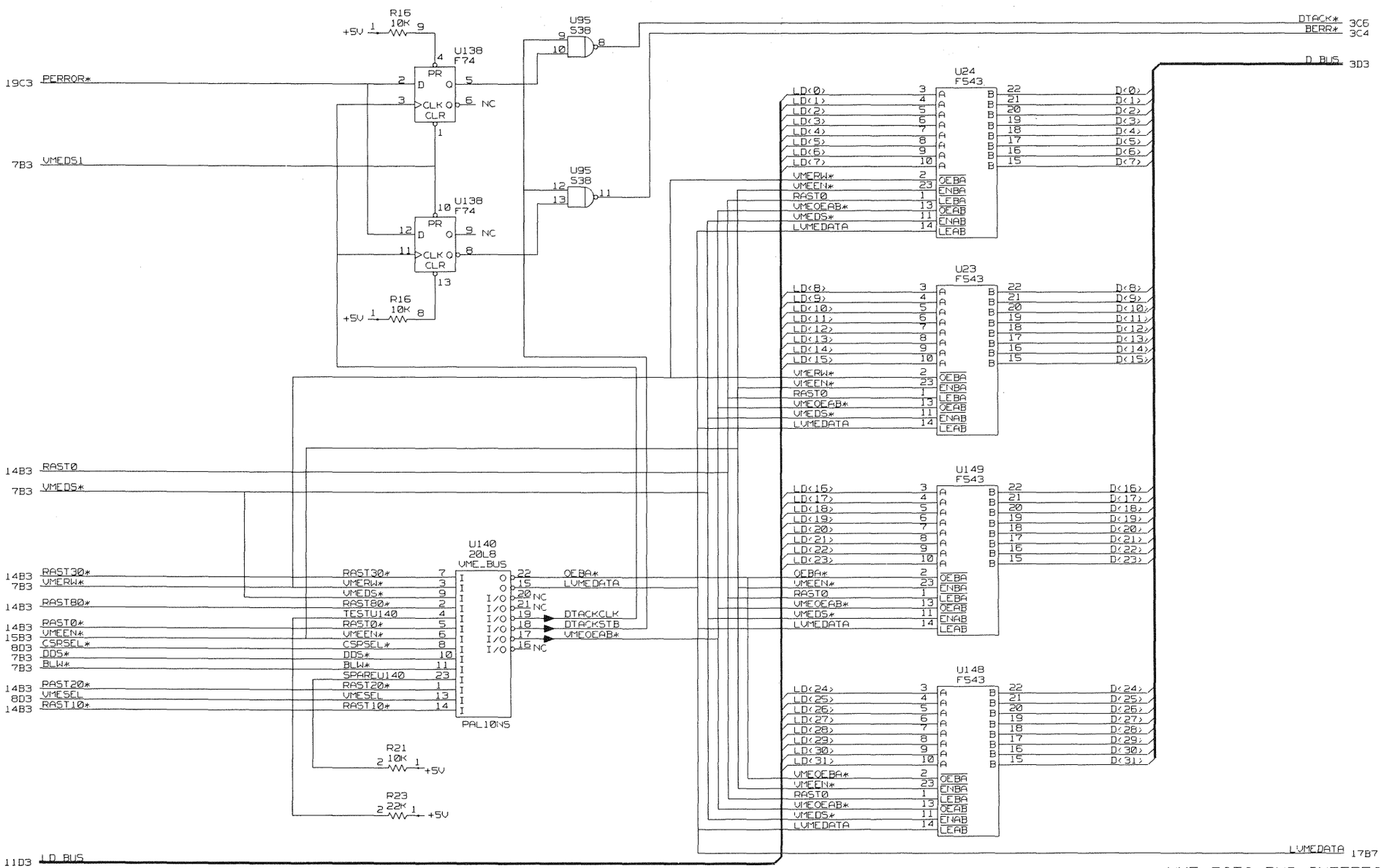
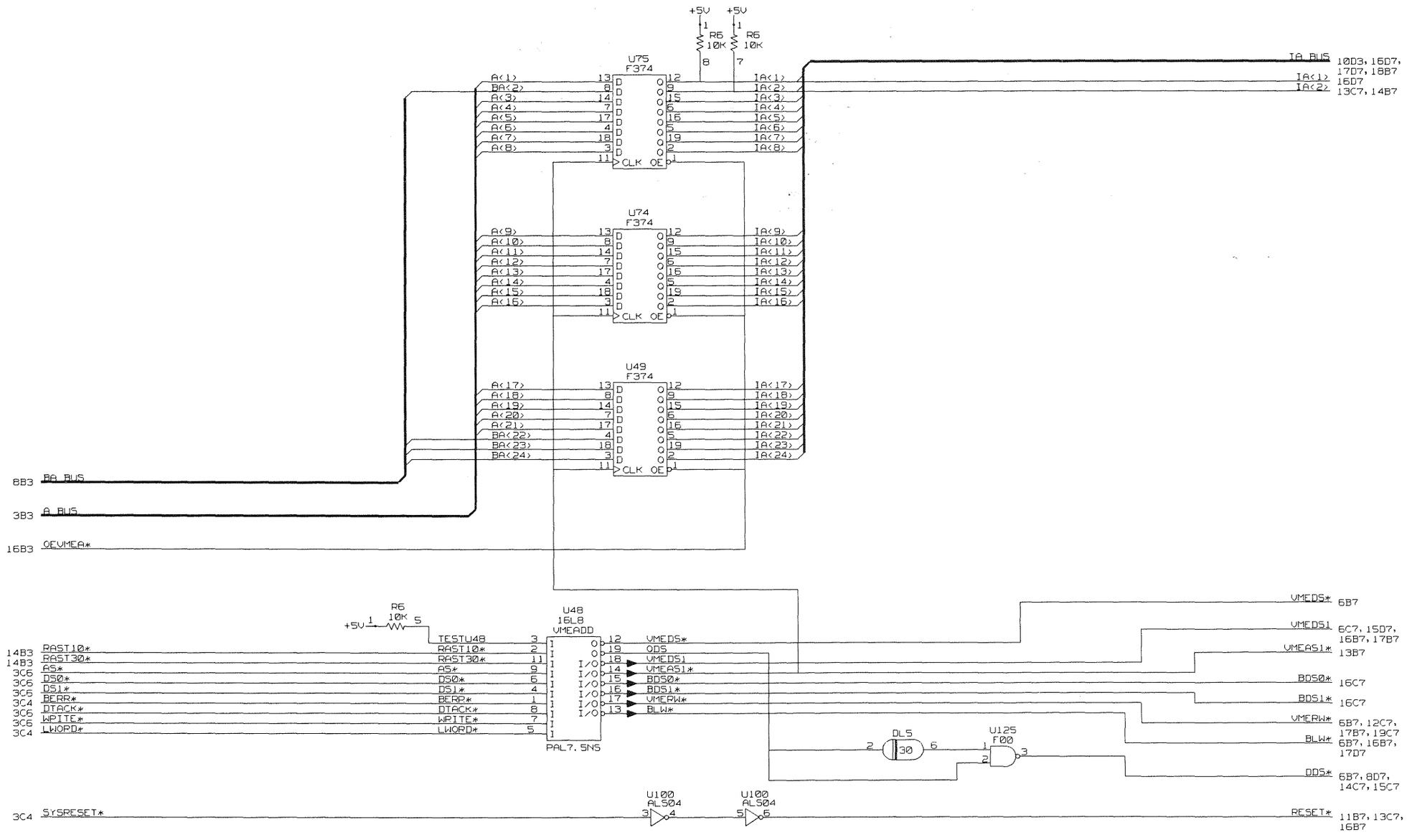
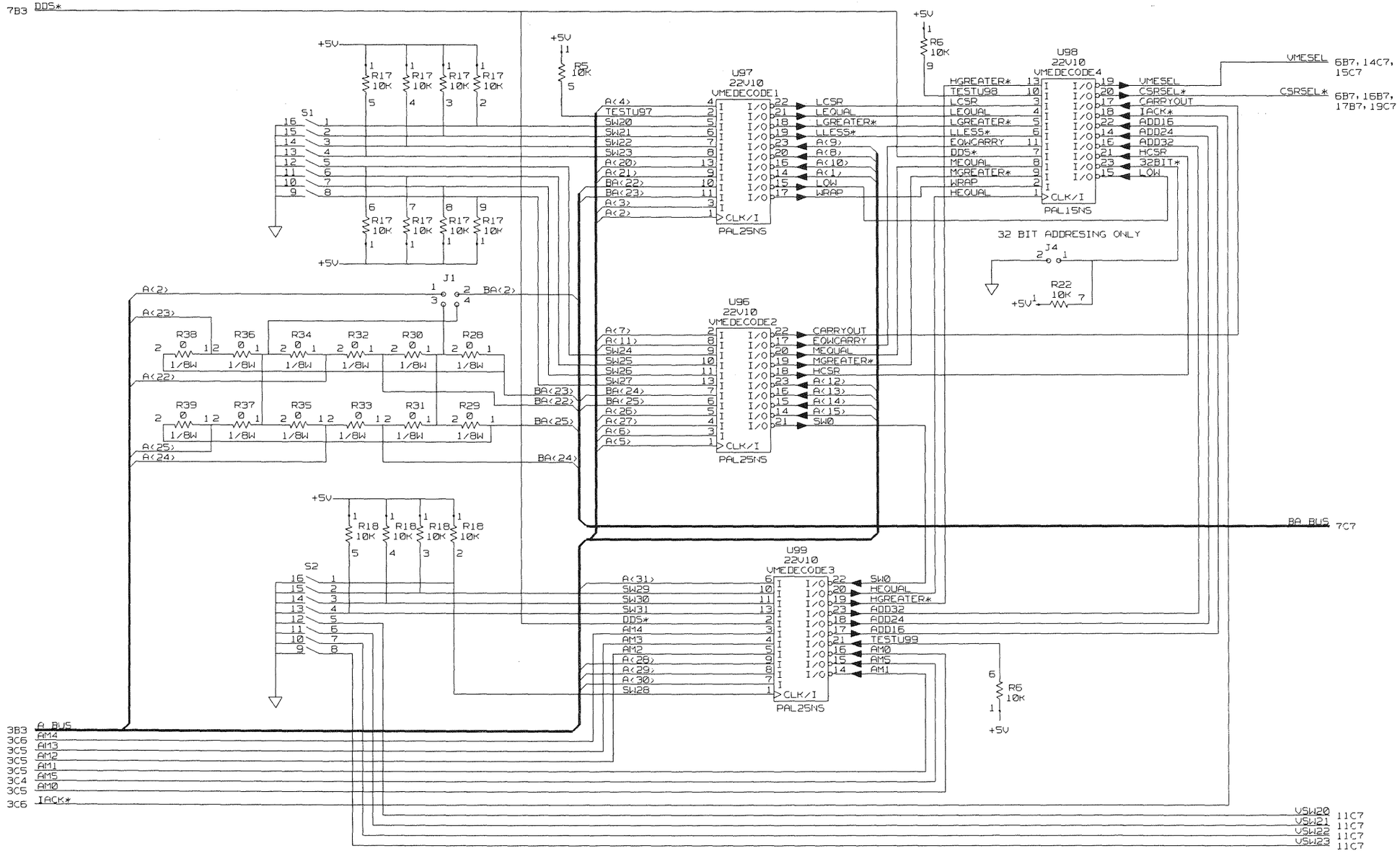


FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 6 OF 25)



VME ADDRESS INTERFACE
63DW3588B0C REV A SH 7 OF 25

FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 7 OF 25)



VME ADDRESS DECODE
63DW3588B0C REV A SH 8 OF 25

FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 8 OF 25)

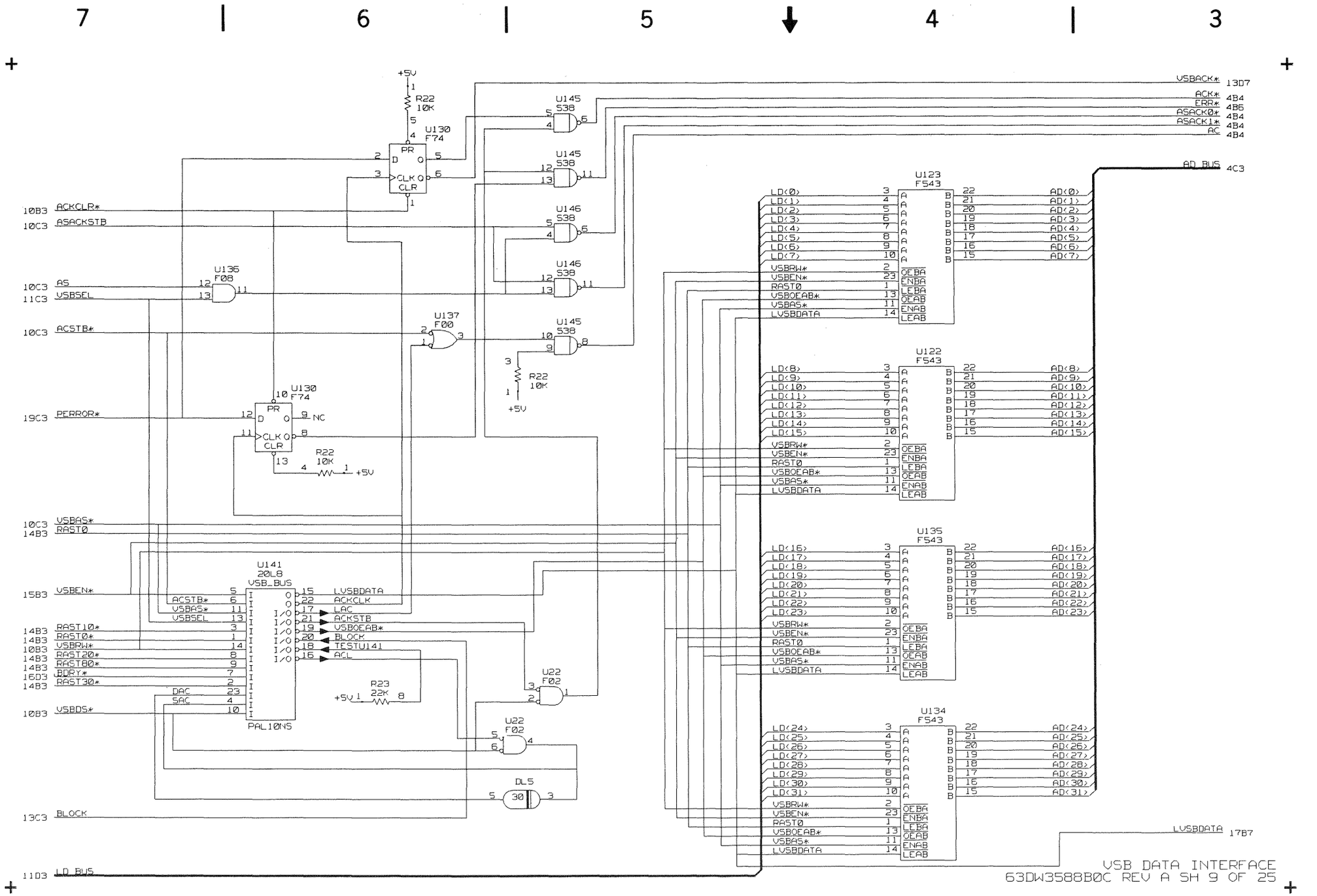
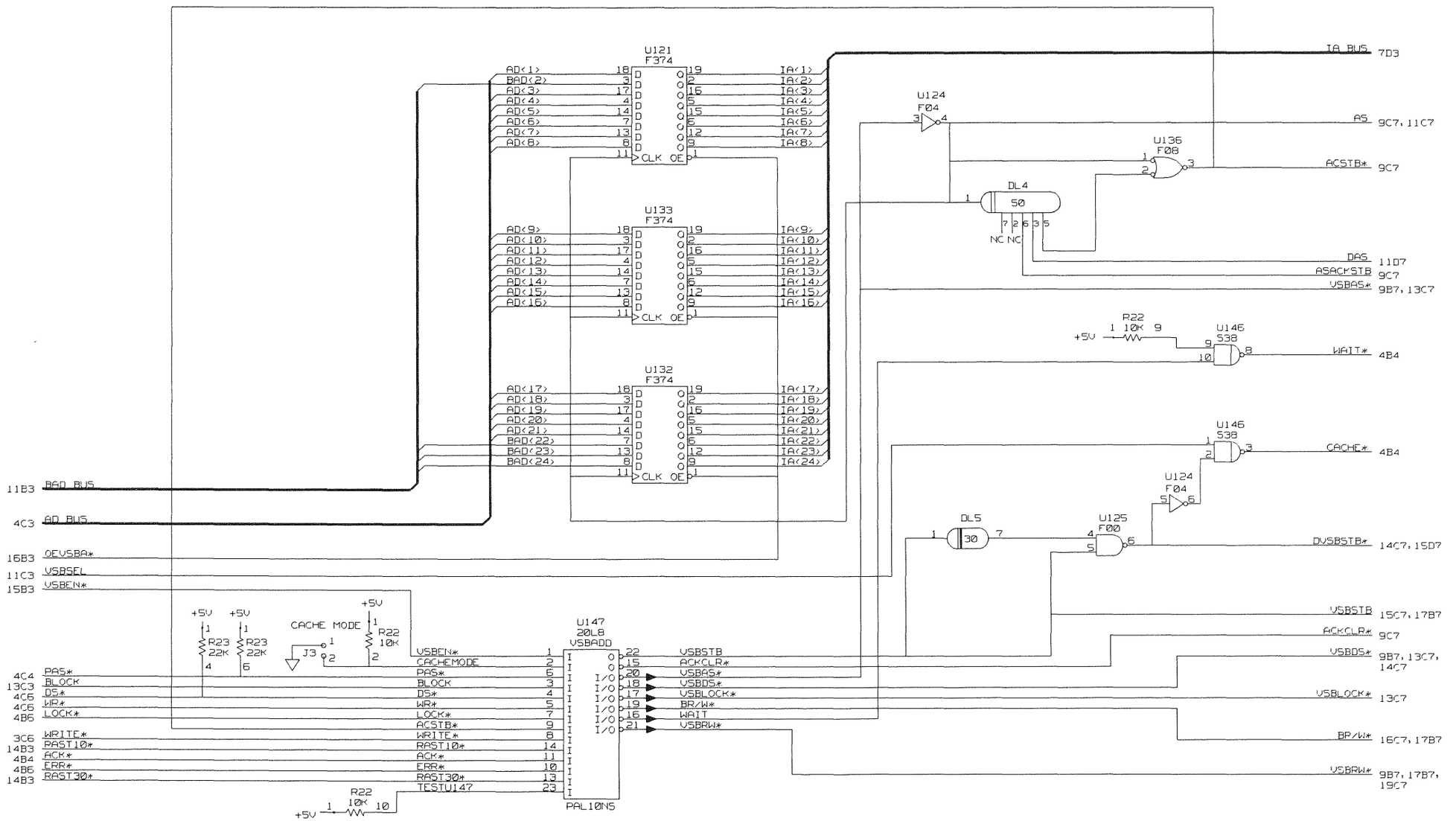
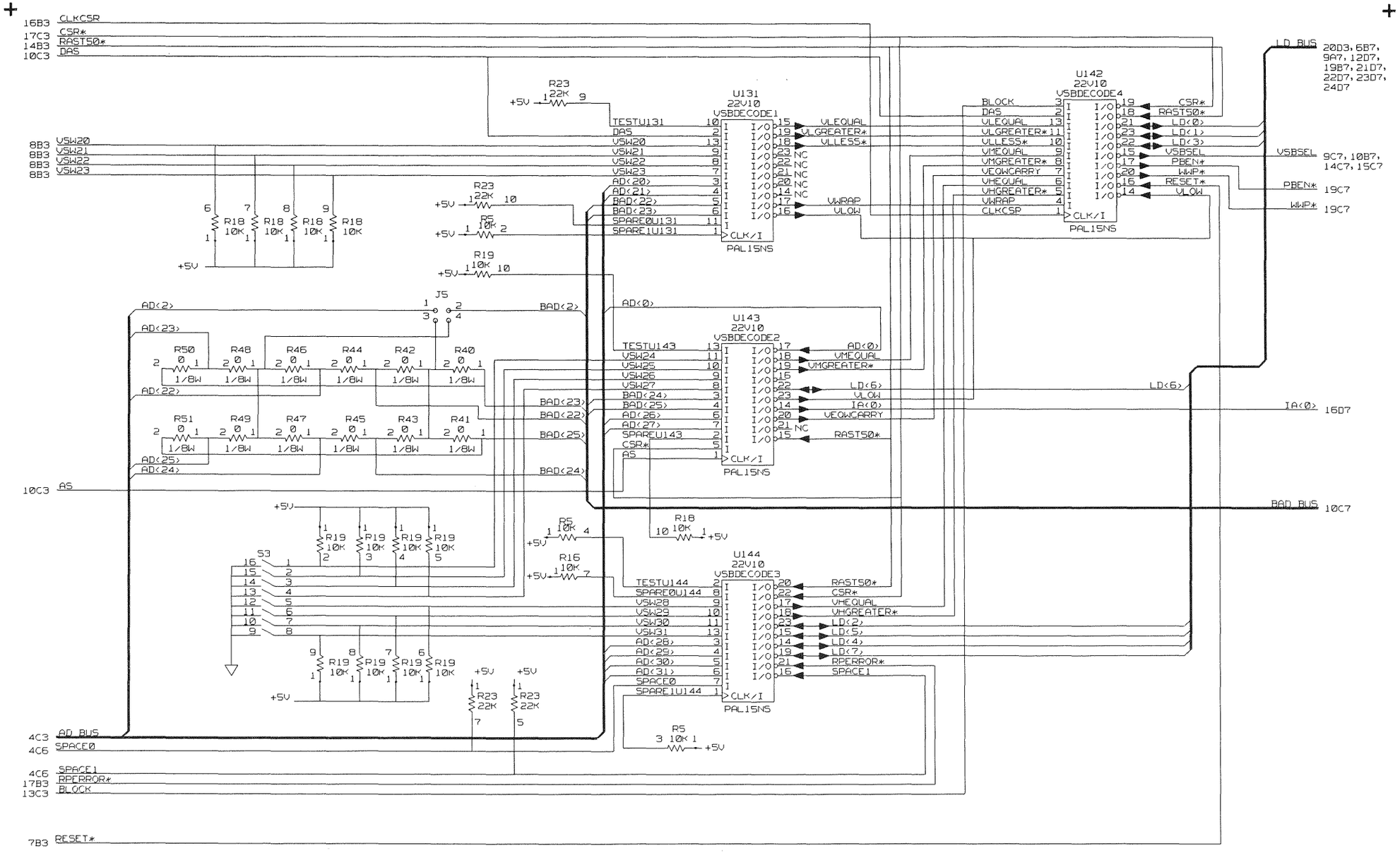


FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 9 OF 25)



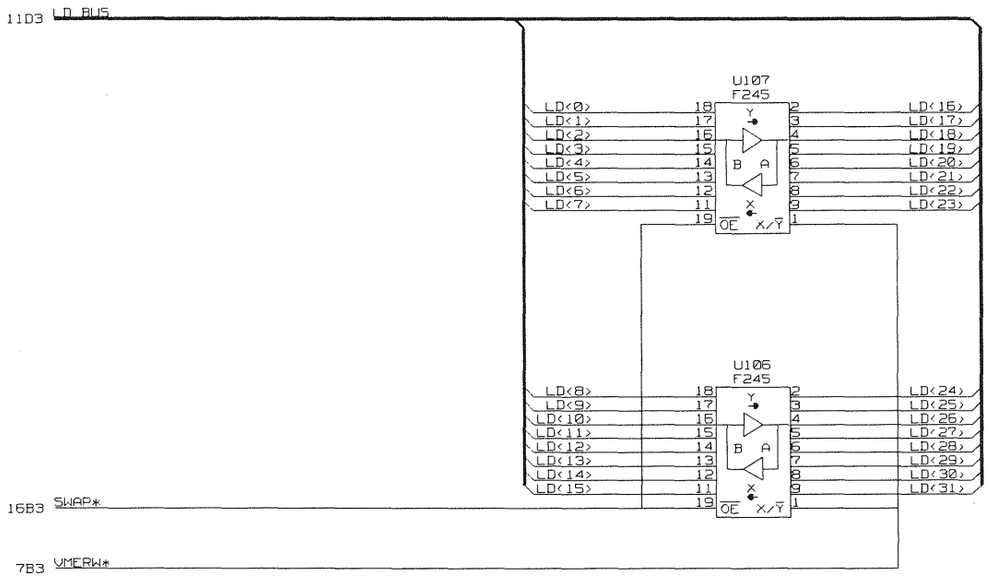
VSB ADDRESS BUFFERS
63DW3588B0C REV A SH 10 OF 25

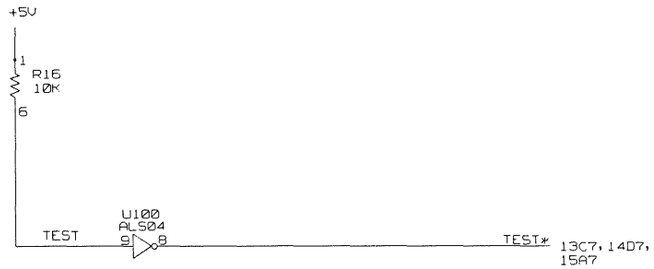
FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 10 OF 25)



VSB ADDRESS DECODE
63DW3588B0C REV A SH 11 OF 25

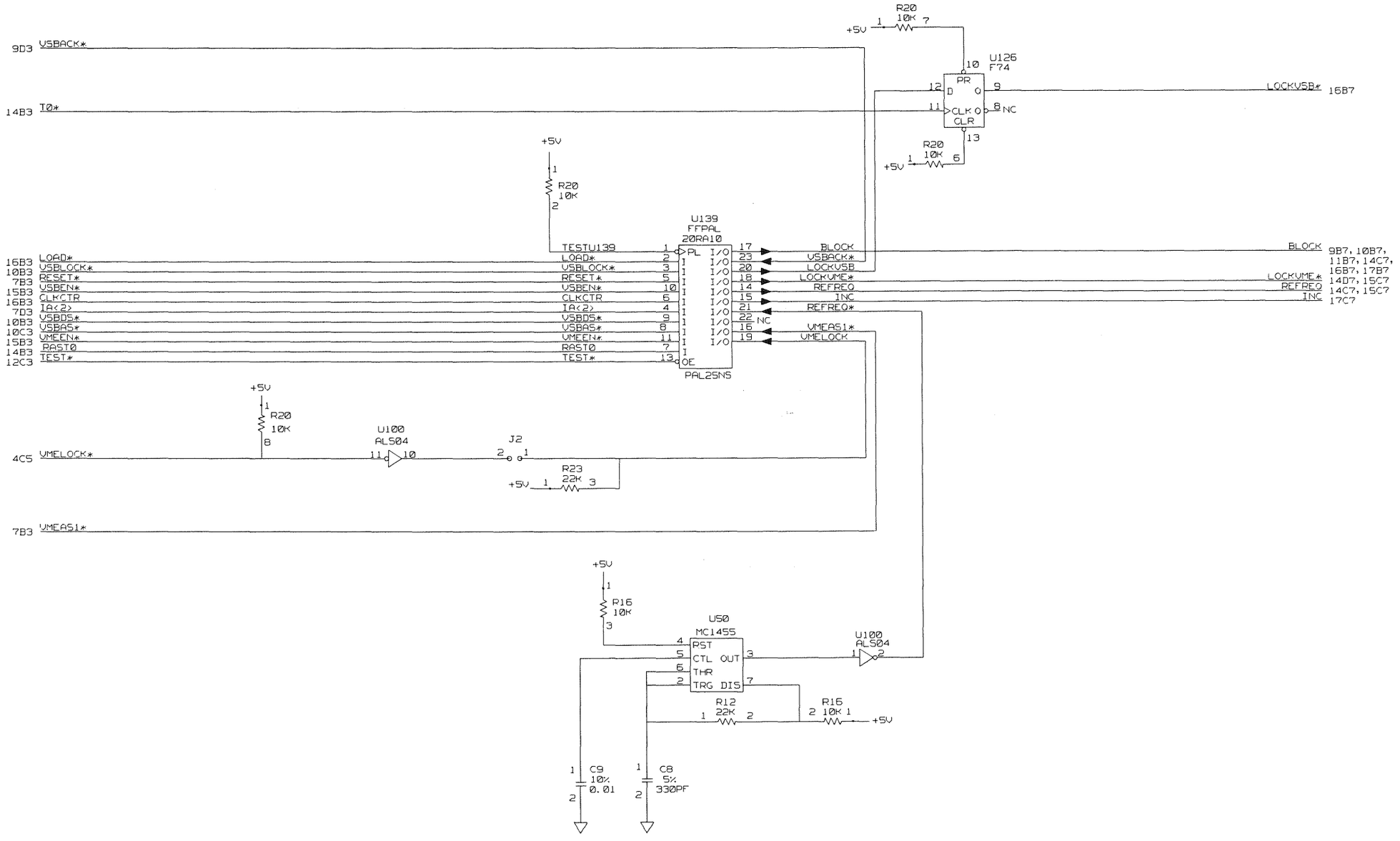
FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 11 OF 25)





SWAP BUFFERS
63DW3588B0C REV A SH 12 OF 25

FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 12 OF 25)



REFRESH
63DW3588B0C REV A SH 13 OF 25

FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 13 OF 25)

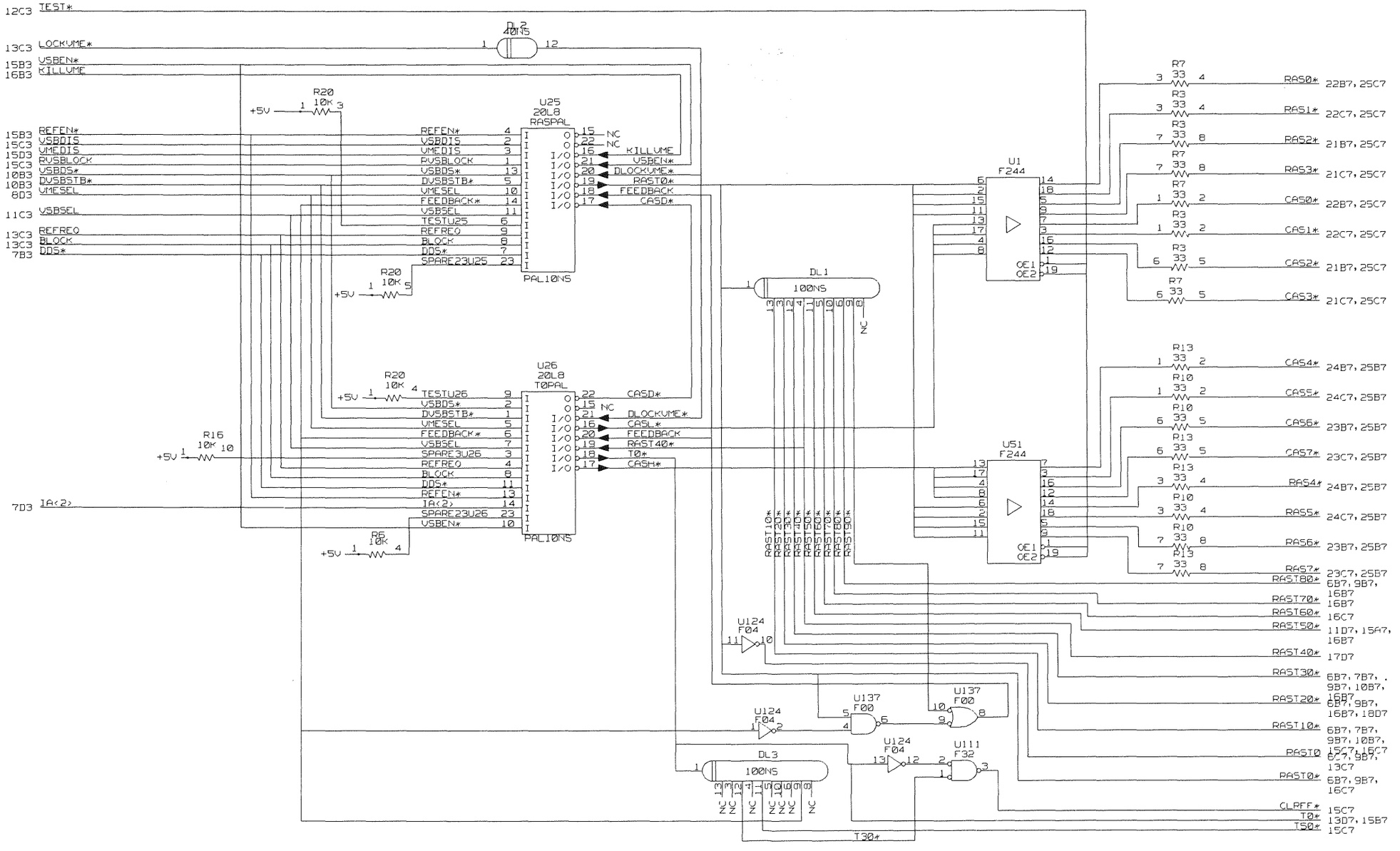


FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 14 OF 25)

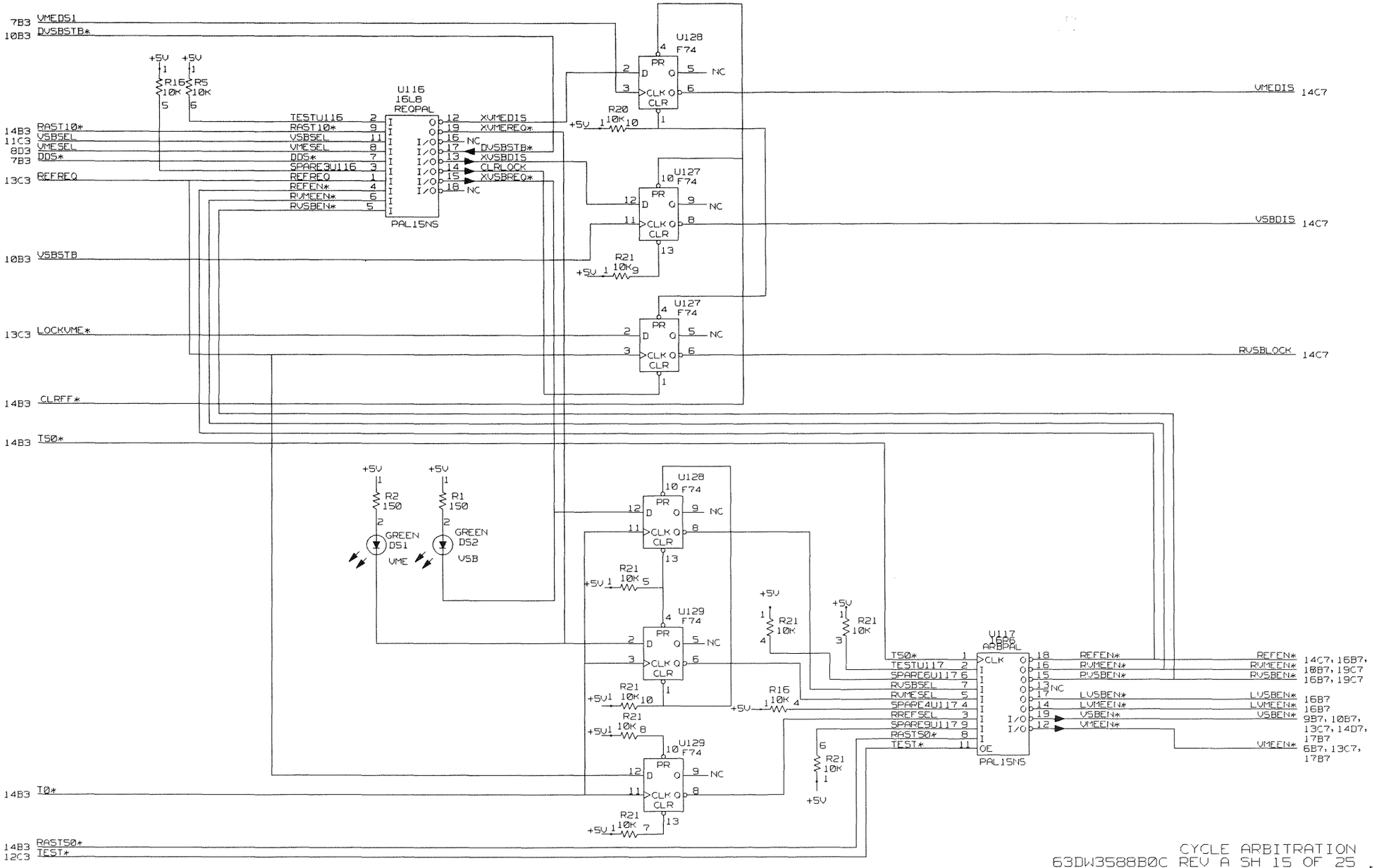
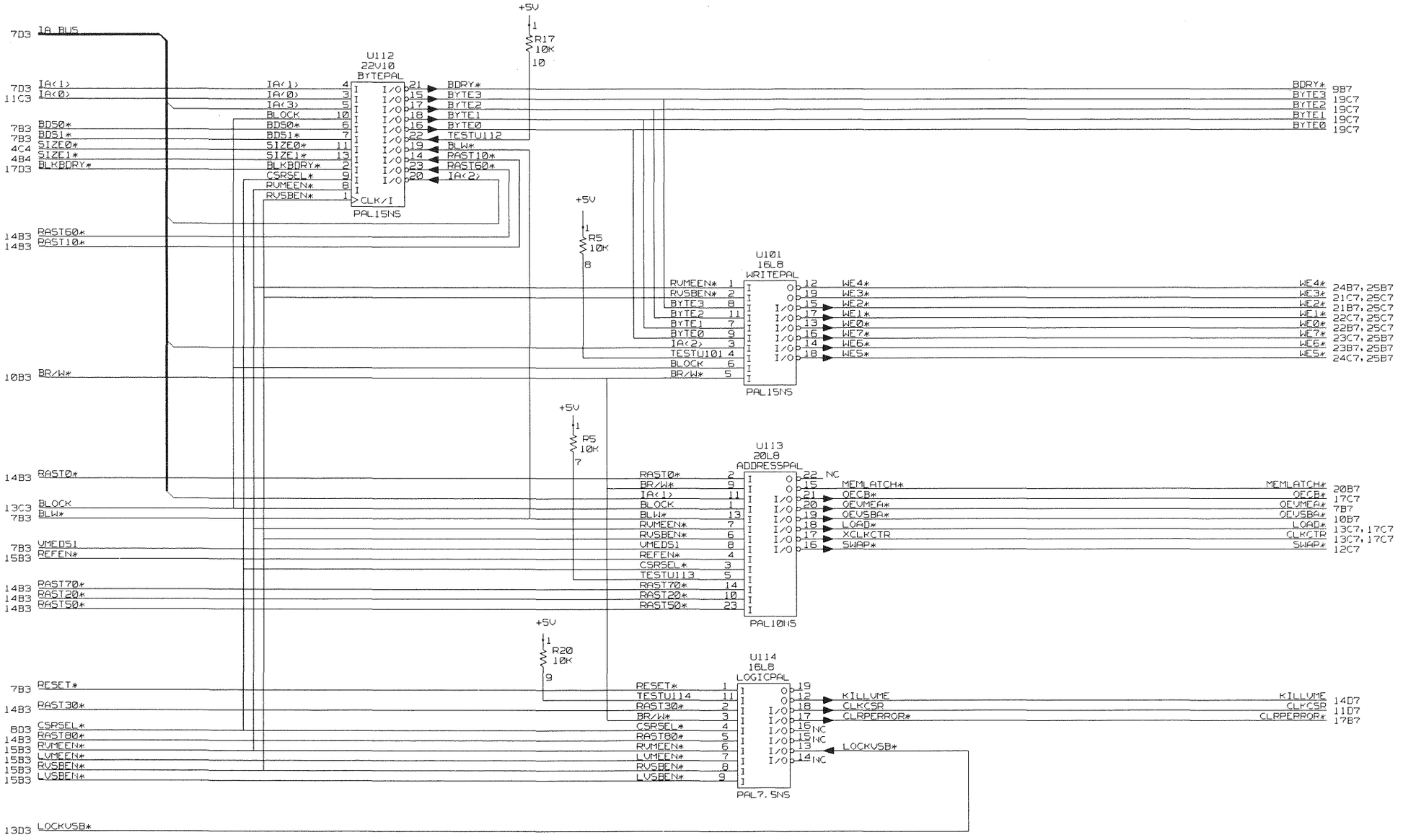


FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 15 OF 25)



WRITE DECODE
63DW3588B0C REV A SH 16 OF 25

FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 16 OF 25)

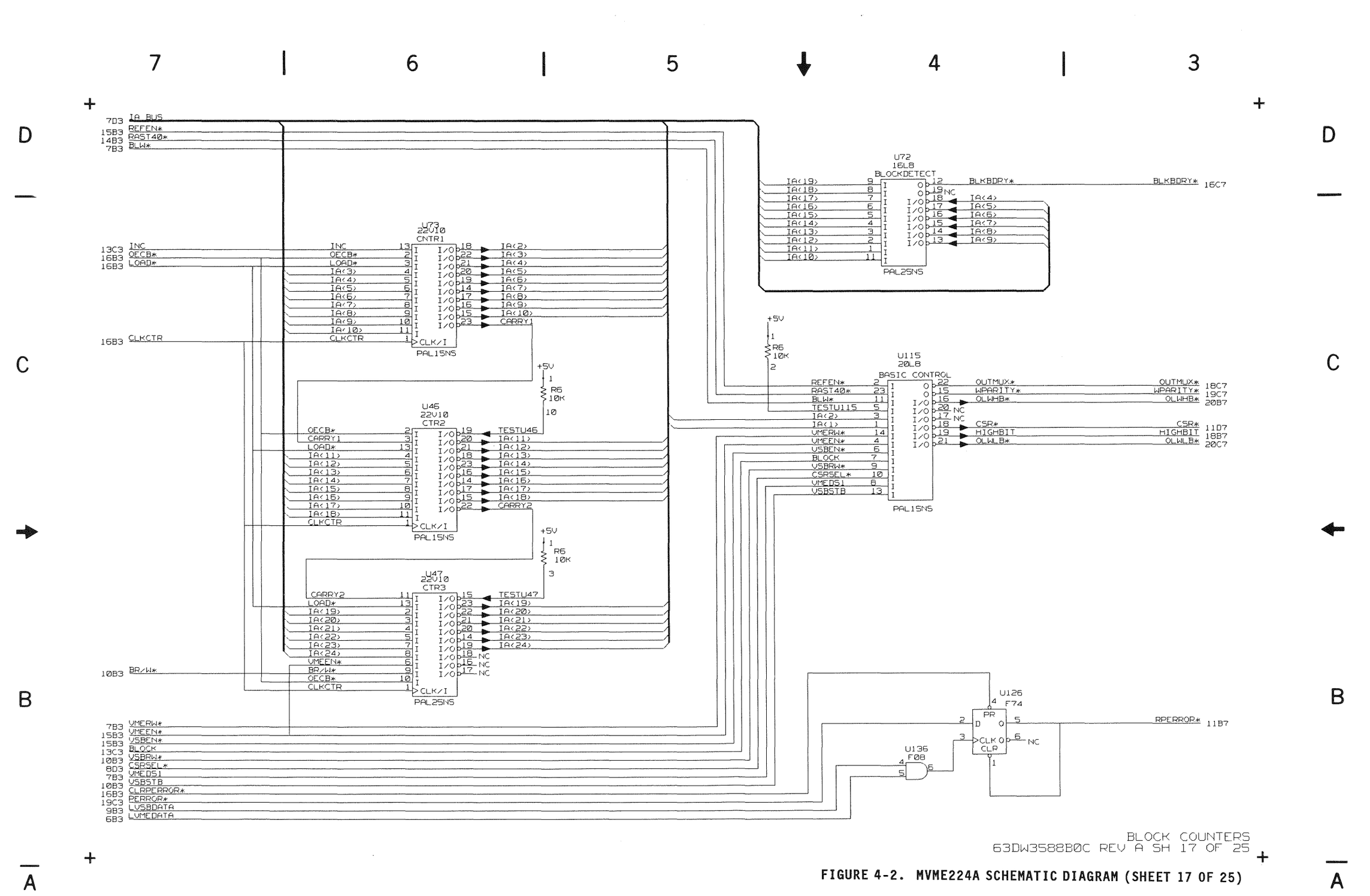
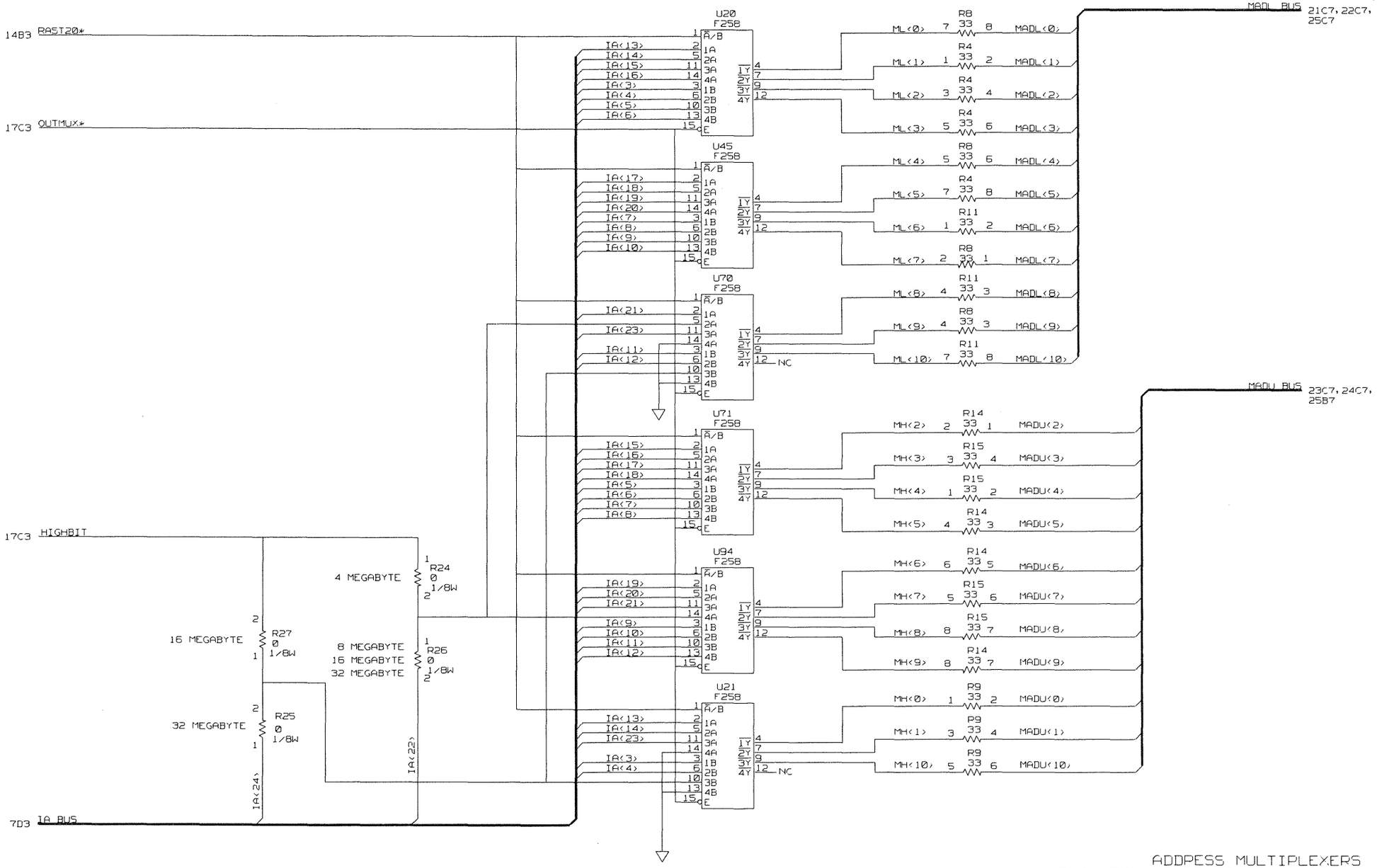
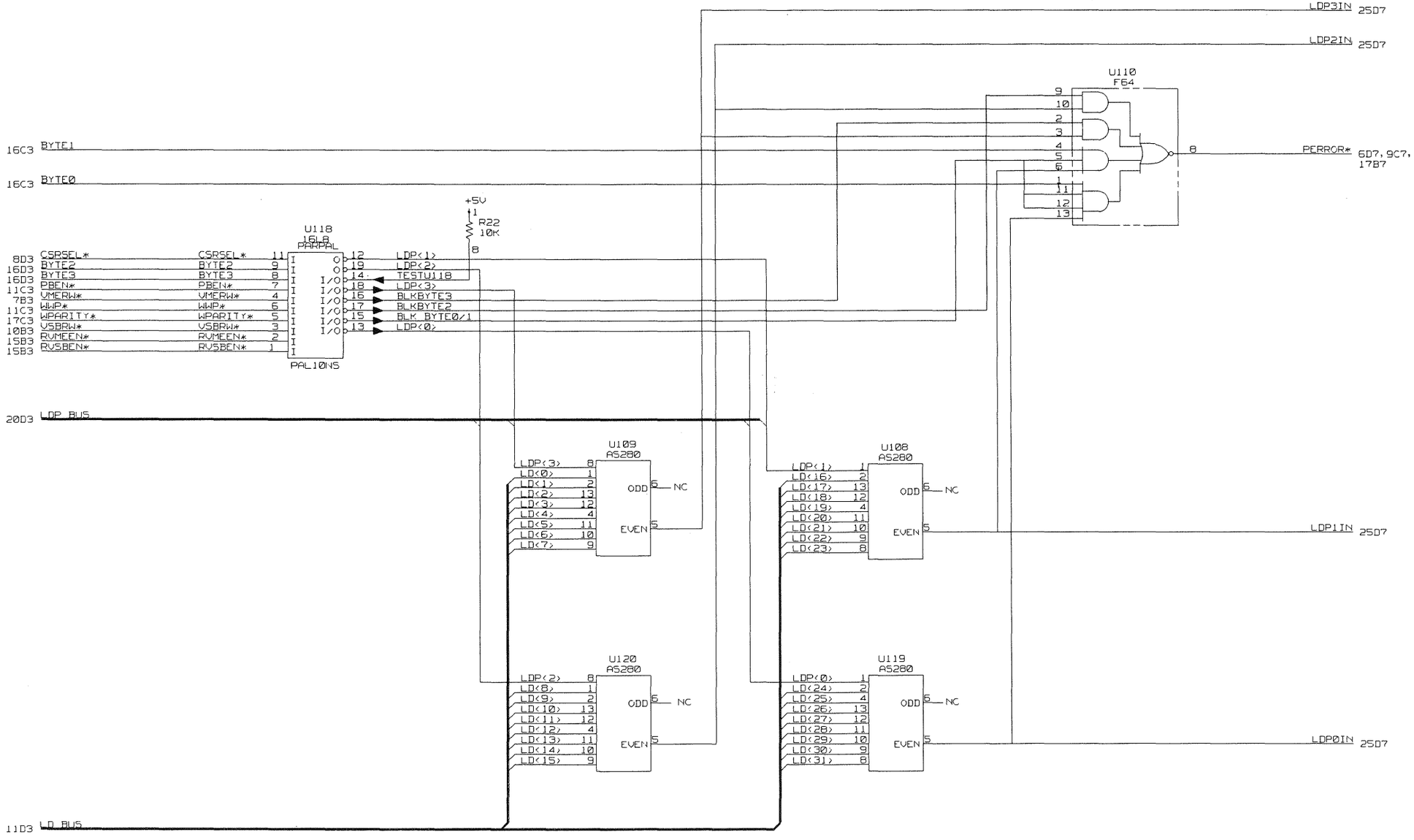


FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 17 OF 25)



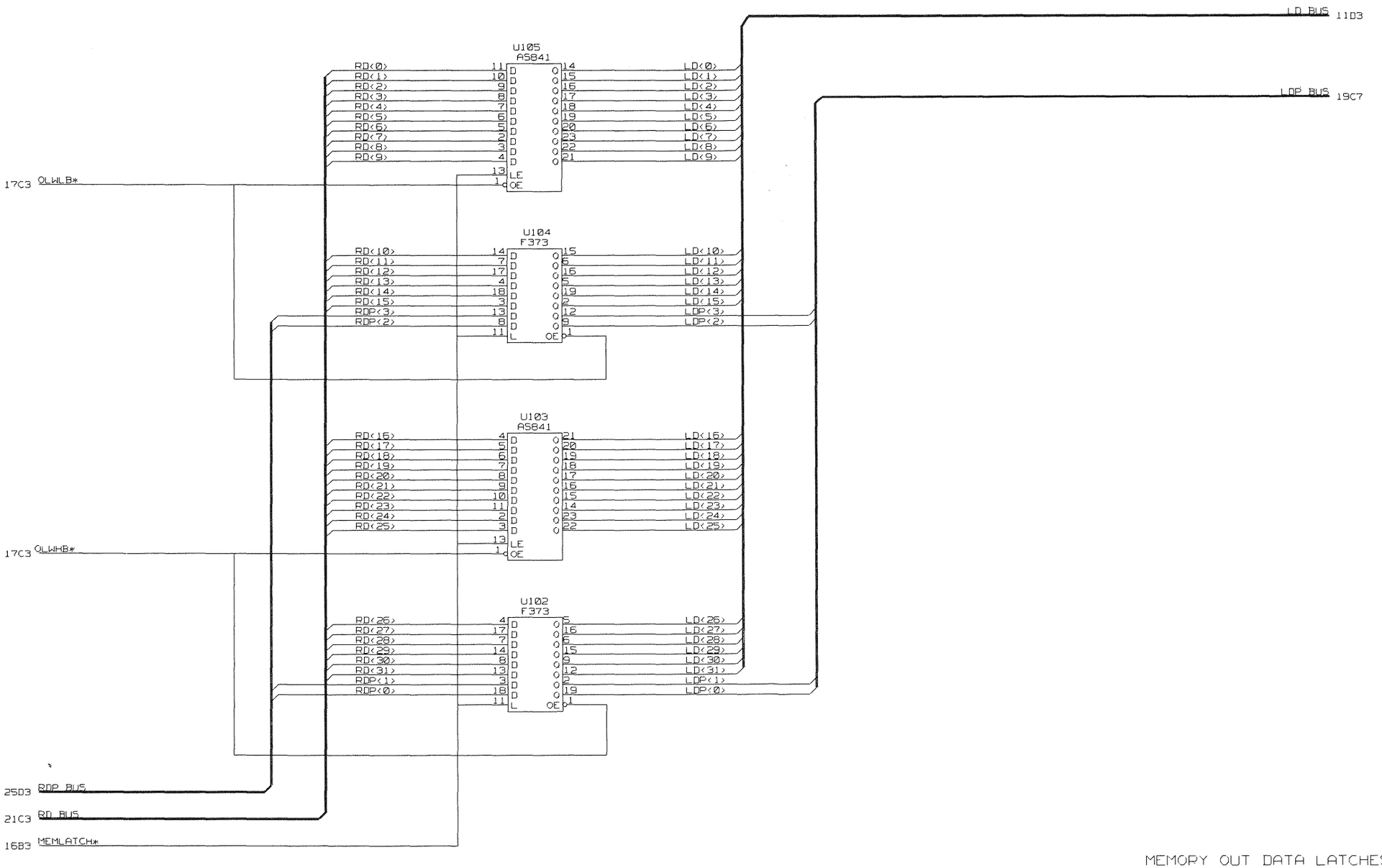
ADDRESS MULTIPLEXERS
63DW3588B0C REV A SH 18 OF 25

FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 18 OF 25)



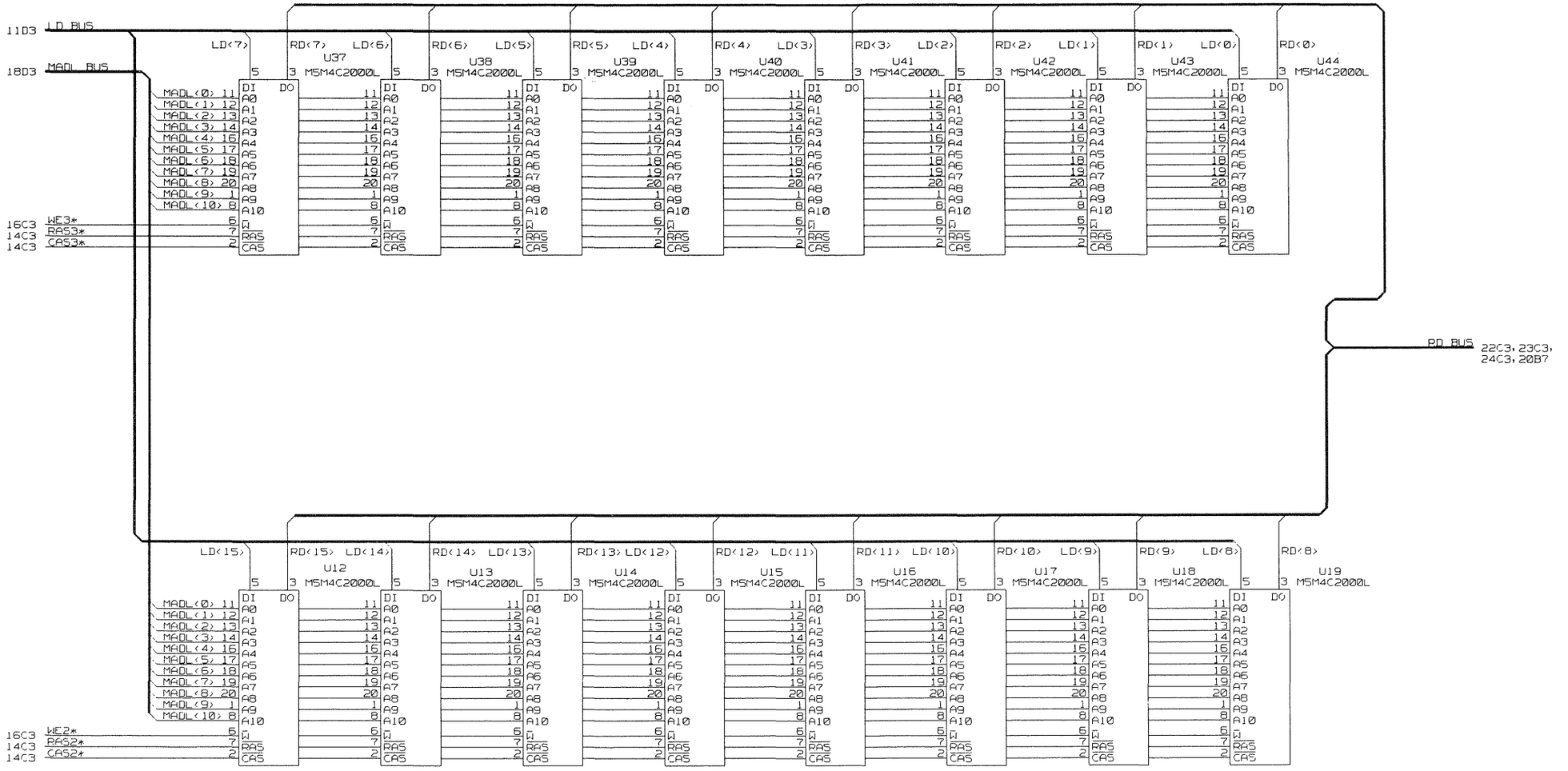
PARITY GENERATION
63DW3588B0C REV A SH 19 OF 25

FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 19 OF 25)



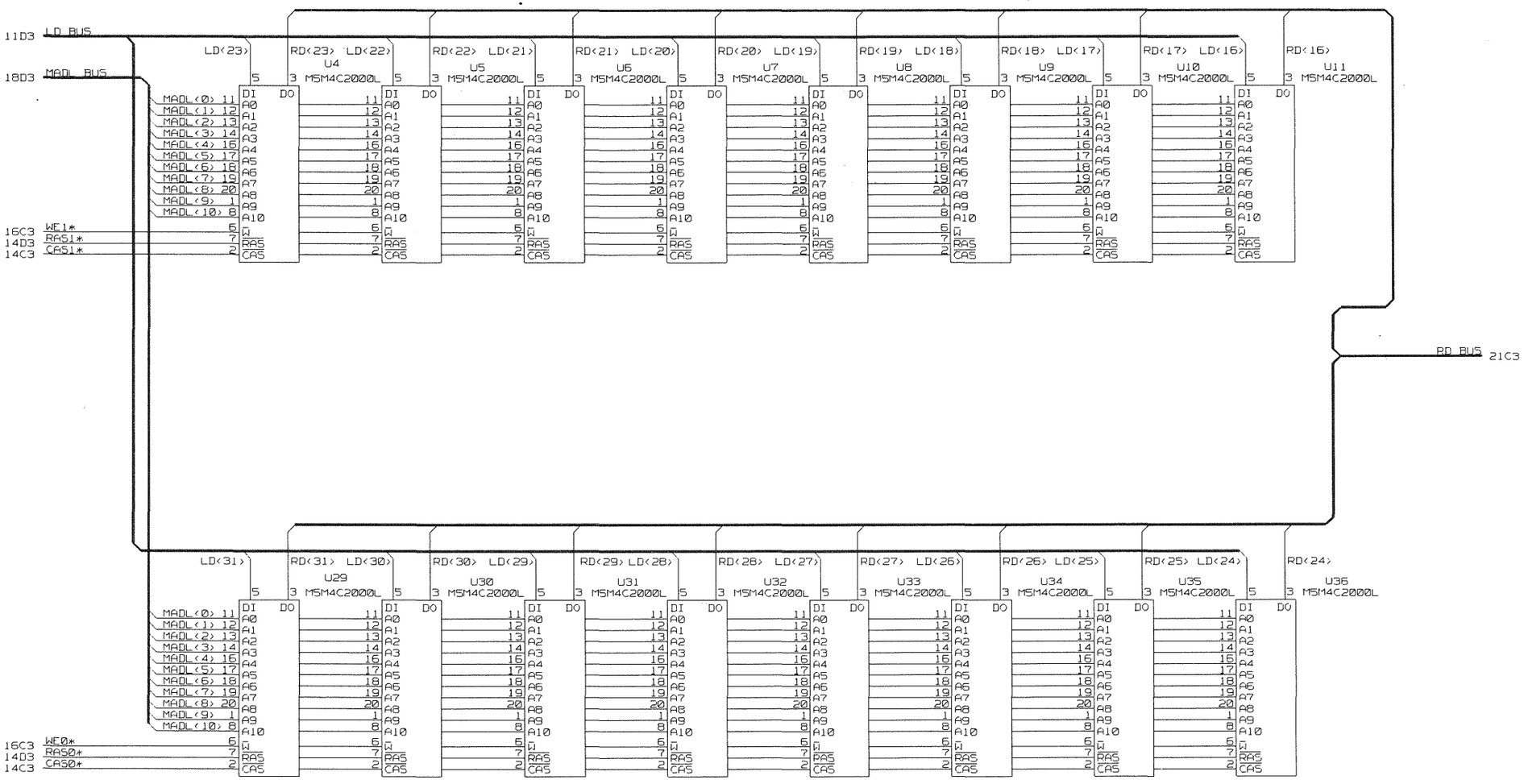
MEMORY OUT DATA LATCHES
63DW3588B0C REV A SH 20 OF 25

FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 20 OF 25)



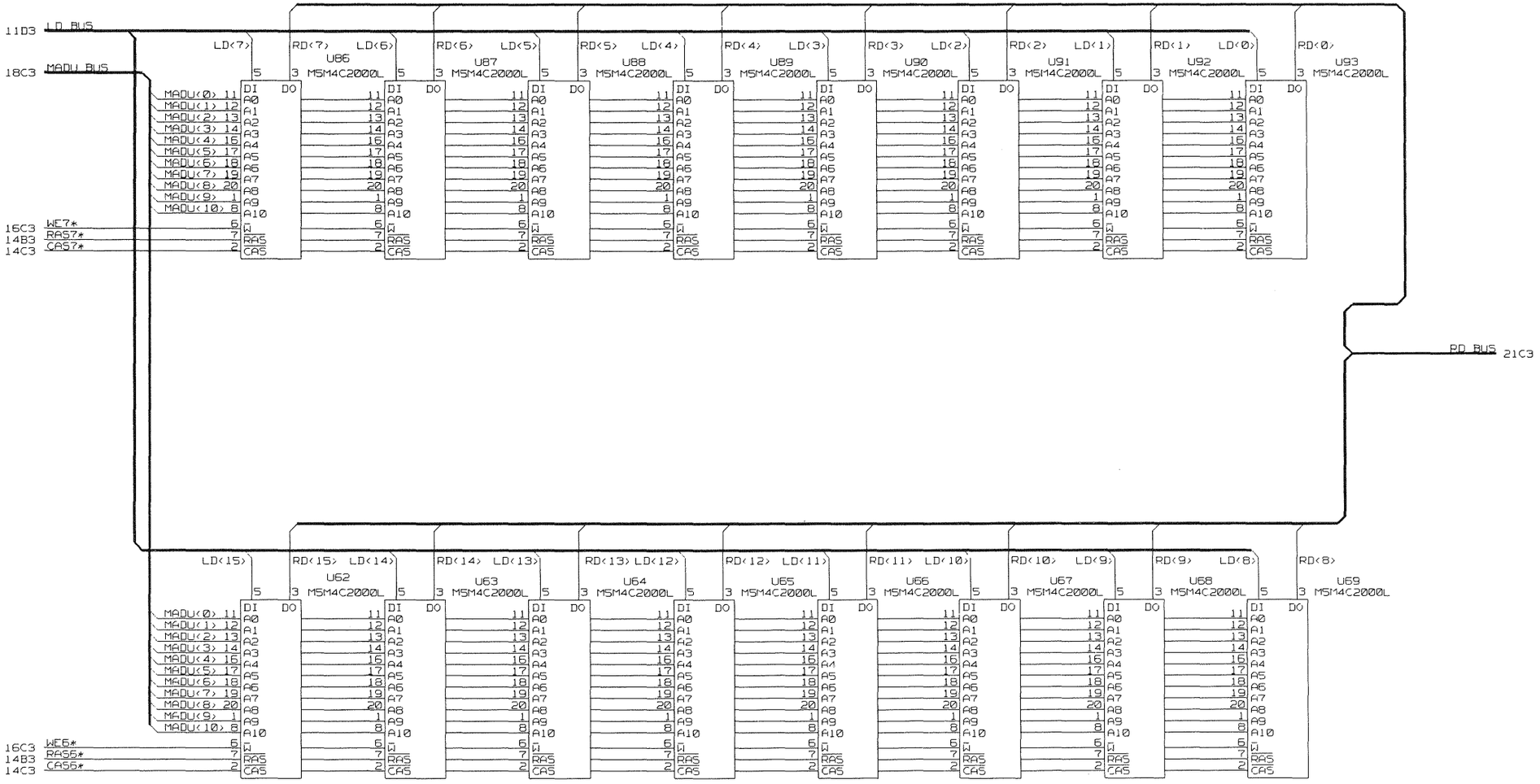
DRAM LOWER BYTES 2 AND 3
63DW3588B0C REV A SH 21 OF 25

FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 21 OF 25)



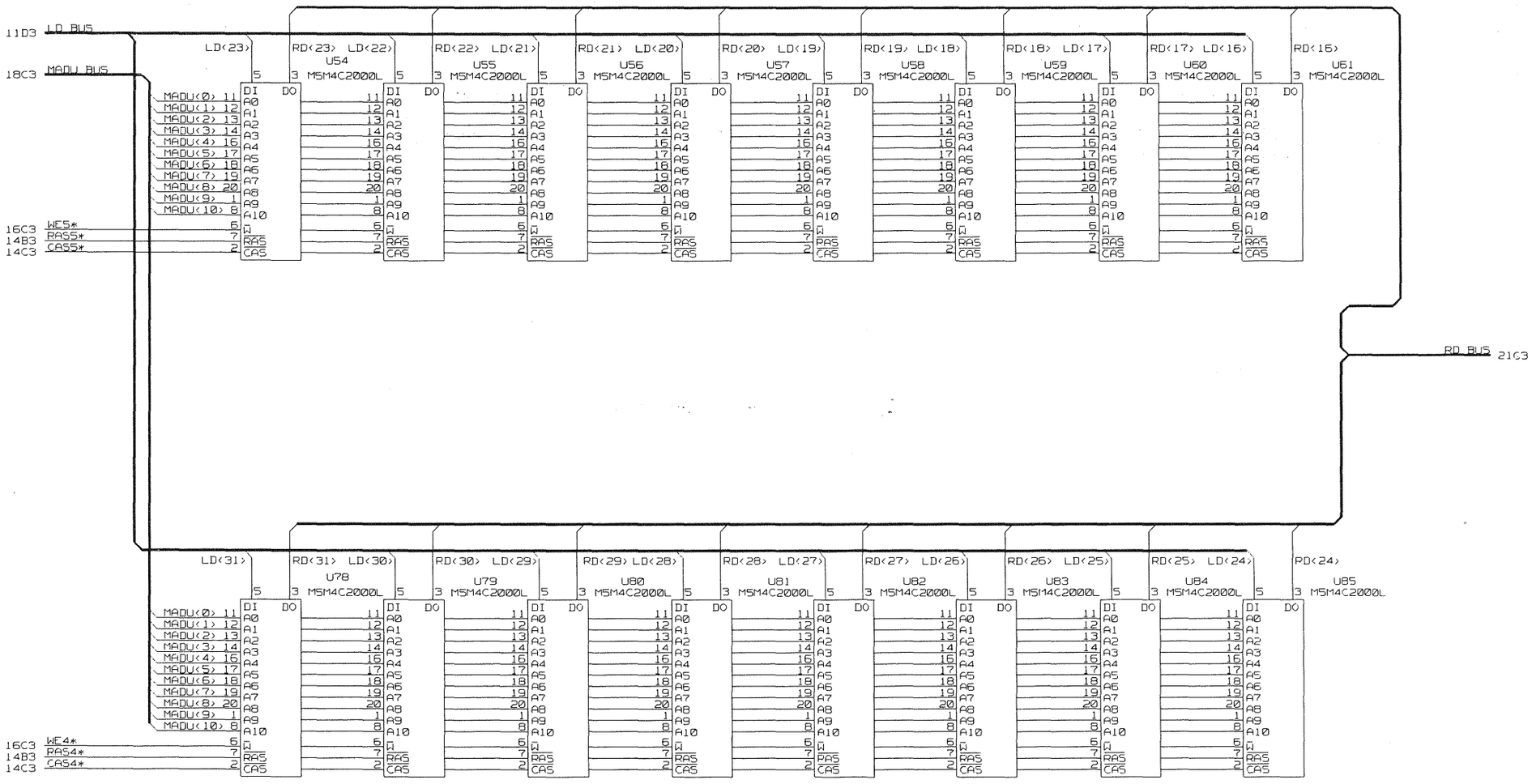
DRAM LOWER BYTES 0 AND 1
63DW3588B0C REV A SH 22 OF 25

FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 22 OF 25)



DPAM UPPER BYTES 2 AND 3
63DW3588B0C REV A SH 23 OF 25

FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 23 OF 25)



DRAM UPPER BYTES 0 AND 1
63DW3588B0C REV A SH 24 OF 25

FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 24 OF 25)

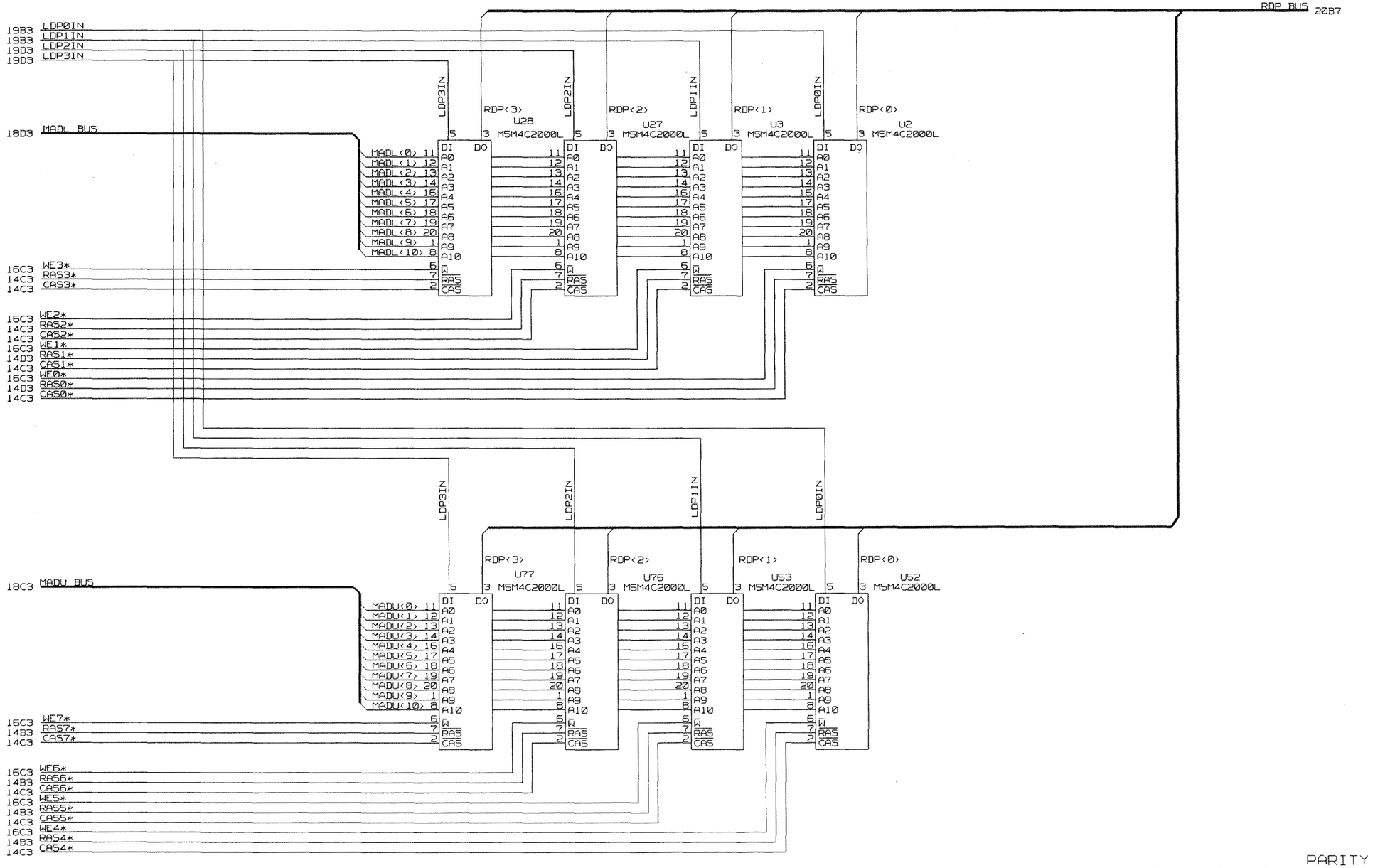


FIGURE 4-2. MVME224A SCHEMATIC DIAGRAM (SHEET 25 OF 25)

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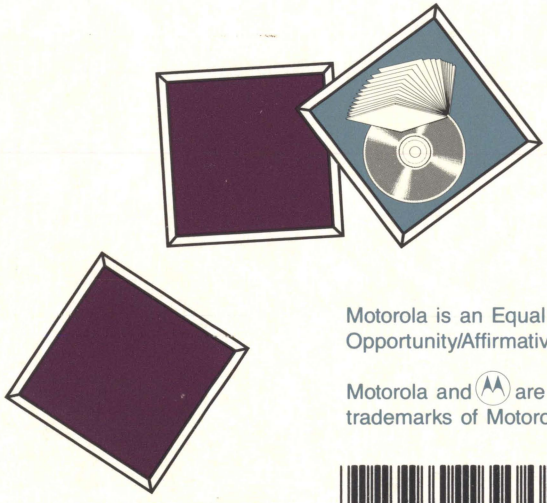

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