PAMS Technical Documentation

NSC/W–1/3 Series Transceivers

Disassembly & Troubleshooting Instructions

Original 09/98

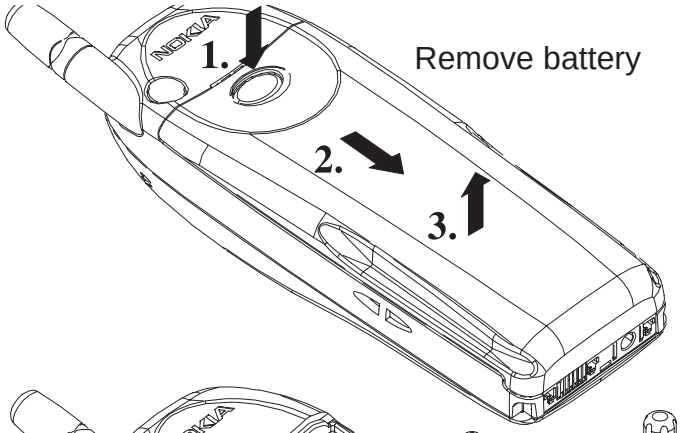
AMENDMENT RECORD SHEET

Amendment Number	Date	Inserted By	Comments
	05/98		Original
Issue2	**09/98**	O Juntunen	P.4 5. screw added p.5 IR removed Troubleshooting revised IC data added

CONTENTS

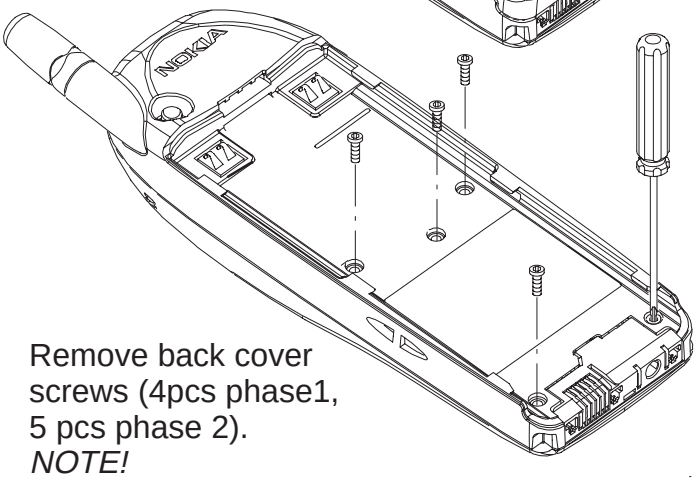
Disassembly

NOTE: Do not attempt antenna removal white the covers are on. The antenna can be removed only when the phone covers are off



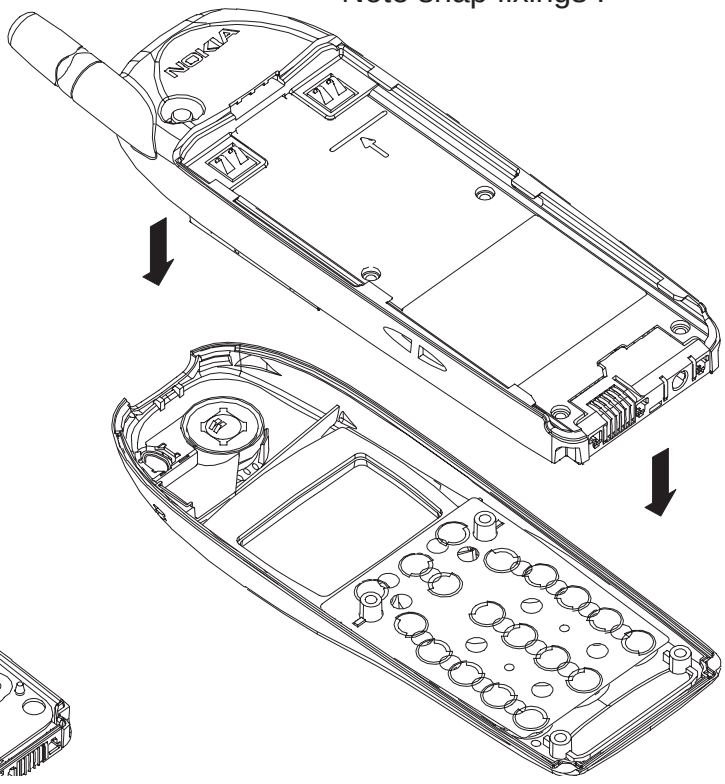
Remove battery

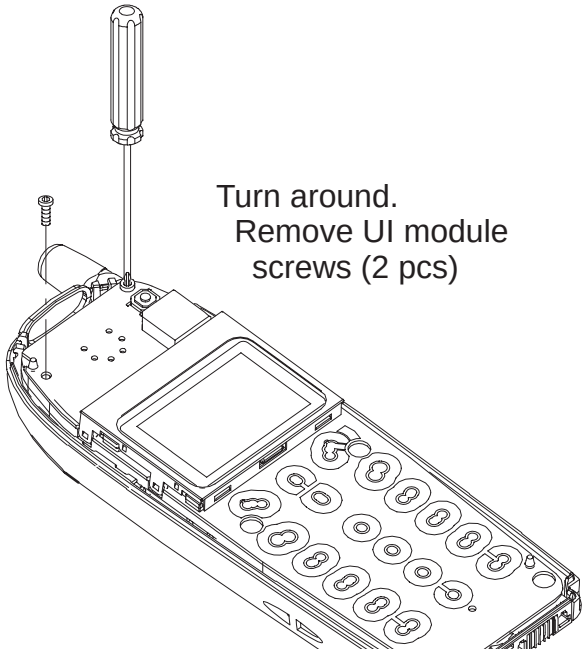
Remove dust cap by finger nail



Remove back cover screws (4pcs phase1, 5 pcs phase 2).
NOTE!
When assembling the B cover screws, use 17 Ncm torque.

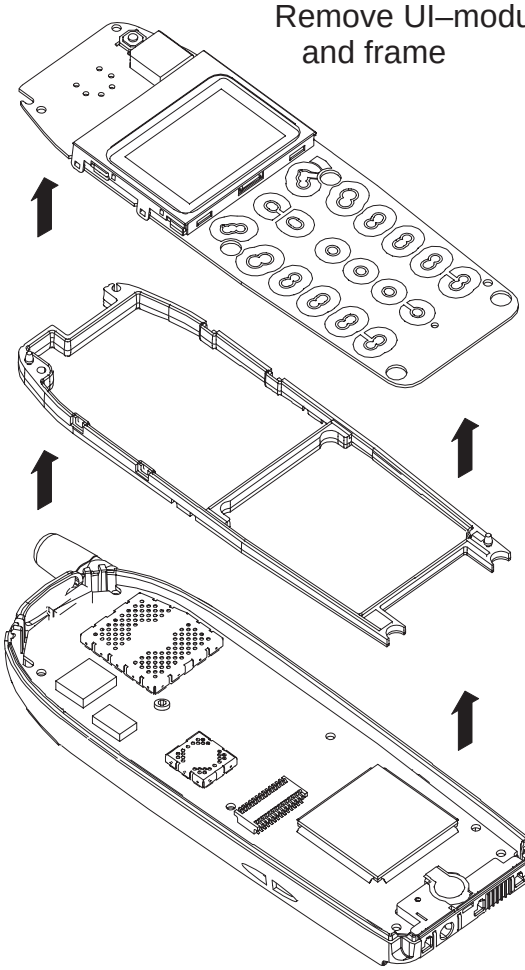
Carefully remove A–cover, keymat, powerkeymat and speaker will follow. Note snap fixings !



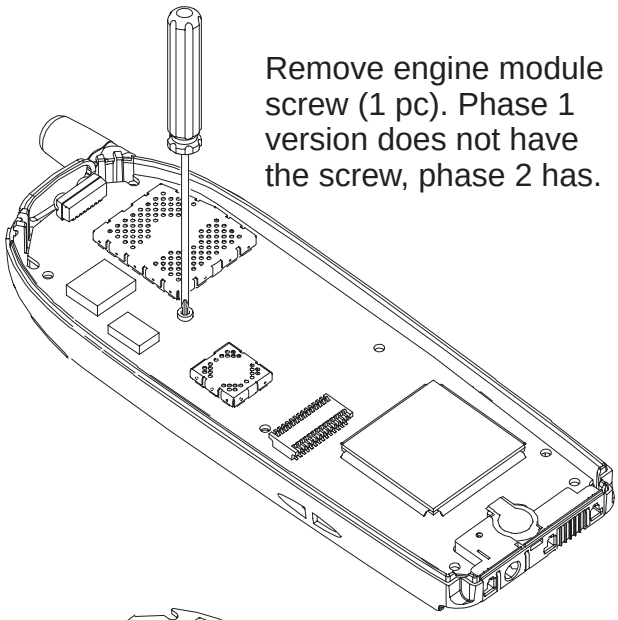


Turn around.
Remove UI module screws (2 pcs)

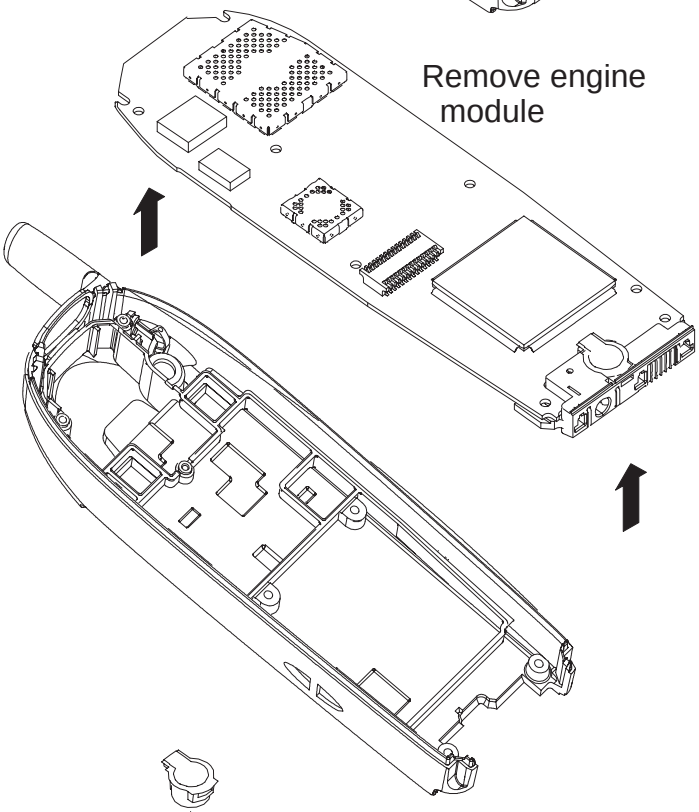
Remove UI–module and frame



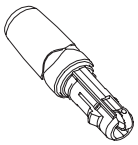
Remove engine module screw (1 pc). Phase 1 version does not have the screw, phase 2 has.

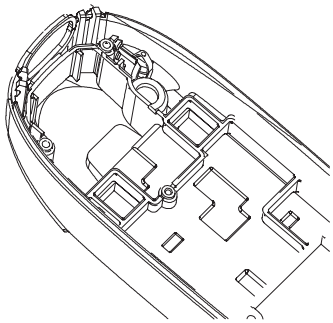


Remove engine module

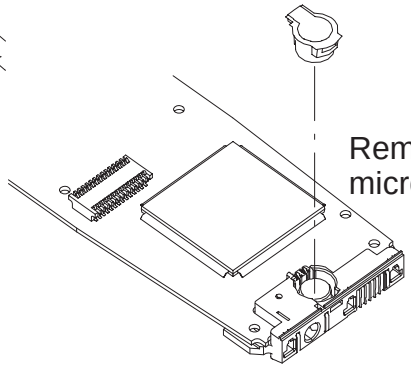


To remove antenna : push in snap at antenna base with screwdriver tip while pushing antenna out of B cover.





Remove microphone



Introduction

RF–measurements must be done using a spectrum analyzer and an high–frequency probe. (Local and reference frequencies and RF power levels in the intermediate stages of the chain) Oscilloscope is used to measure DC–voltages and low frequency signals. Multimeter is also a useful measurement equipment in fault finding.

The external RF connector must be used when reasonable to improve the reliability of the measurement results.

The RF–section is mainly built around the PLUSSA IC (N750). The RF block has separate external filters, UHF synthesizer, Power Amplifier , TX Driver, frontend and upconverter circuit for both frequency bands. In the TDMA1900 mode the external regulator is used to provide supply voltage for RF parts.

Before changing single ASICs or components, please check the following :

1. The soldering and connections of pins of the ASICS are OK
2. Supply voltages and control signals are OK
3.Signals of the synthesizers are coming to ASICS. This to prevent the unnecessary changing of the ASICS.

NOTE! Grounding of the PA–IC is directly underneath so it is hard to check. ***The PA–module is static discharge sensitive!*** *So ESD protection must be used when dealing with PA–IC (ground straps and ESD soldering tools). The PA is also a moisture sensitive components and it is important to follow additional information about handling the component.*

There are still lots of discrete components (resistors, inductors and capacitors) troubleshooting of which comprises just checking that the component is soldered or it is not missing from PCB.

Abbreviations in RF–fault finding charts

TP	Test Point
BB	Baseband
f:	Frequency of signal (measured with spectrum analyzer)
LO	Local Oscillator
P:	Power of signal in desibels (dB) (measured with spectrum analyzer)
PA	Power Amplifier
PCB	Printed Circuit Board
PLL	Phase Locked Loop
RF	Radio Frequency
RX	Receiver
T:	Time between pulses
TX	Transmitter
UHF	Ultra High Frequency
V:	Voltage of signal (measured with oscilloscope)
VCO	Voltage controlled oscillator
VHF	Very High Frequency
AF:	Audio Frequency

Interface signals between RF and BB/DSP

Signal name	From	To	Parameter	Mini-mum	Typi-cal	Maxi-mum	Unit	Function
VBAT NOTE! Not char-ger	Battery	RF	Voltage	3.1	3.6	5.3 5.0	V	Supply volt-age for RF
VREF	CCONT	PLUSSA	Voltage	1.478	1.500	1.523	V	Reference voltage for PLUSSA
RFTEMP	RF	CCONT	Voltage	0 HOT	1.4 ROO M TEMP	2.7 COLD	V	RF tempera-ture sensor 47k NTC to GND
AFC	COB-BA_D	VCTCXO c	Voltage	0.05	1.1	2.25	V	Automatic frequency control
AGC1	Cobba_D	PLUSSA	Voltage	0.5		1.4	V	
AGC2	MAD	RX LNA	Voltage	0		2.85	V	LNA Gain switch “1” min 2.0 V “0” max 0.7 V
BAND	COB-BA_D	VHF VCO	Voltage	0		2.85	V	“0” 2 Ghz “1” 1 GHz
MODE	MAD	1Ghz PA	Voltage	0		2.85	V	“0” AMPS “1” TDMA
IF2AP/ IF2AN	PLUSSA	COB-BA_D	Voltage/Frequency		0.6 / 450		Vpp / kHz	Differential limiter output to DEMO de-tector
IF2DP / IF2DN	PLUSSA	COB-BA_D	Voltage/Frequency		170 / 450	1400	mVpp / kHz	Differential IF2–signal to RX A/D–con-verter
SENA1	MAD	PLUSSA	Logic high ”1”	2.0			V	1 Ghz PLL enable
			Logic low ”0”	0		0.8	V	
SDATA	MAD2	PLUSSA	Logic high ”1”	2.0			V	Synthesizer data
			Logic low ”0”	0		0.8	V	
SCLK	MAD2	PLUSSA	Logic high ”1”	2.0			V	Synthesizer clock
			Logic low ”0”	0		0.8	V	
RFC	VCTCXO	COB-BA_D	Voltage/Frequency	0.2	0.4 / 19.44	1.0	Vpp / MHz	Clock signal for the logic circuits

RFCEN	MAD	CCONT / PENTA regulator	Voltage	0		2.85	V	“1” min 2.0 V “0” max 0.4 V
RSSI	PLUSSA	CCONT	Output level	0.1		1.5	V	Analog mode field sternght indicator
TXIP/ TXIN	COBBA	PLUSSA	Differential voltage swing (static)	1.022	1.1	1.18	Vpp	Differential in–phase TX baseband signal for the RF modulator
			Output level on each output	0.760	0.8	0.84	V	
TXQP/ TXQN	COBBA	PLUSSA	Same as TXIP/ TXIN					Differential quadrature phase TX baseband signal for the RF modulator
TXP1	MAD	CCont	Logic high ”1”	2.0			V	1 Ghz Transmitter power control enable
			Logic low ”0”			0.5	V	VR7 ON/ OFF
TXC	COBBA	PLUSSA	Number of bits	10			bits	Transmitter power control (ramps & power levels)
			Output voltage swing	2.09	2.15	2.21	V	
			Minimum code output level	0.12	0.15	0.18	V	
			Maximum code output level	2.27	2.3	2.33	V	
TXF	PLUSSA	MAD	Voltage	0		2.85	V	False transmission indicator, function controlled via PLUSSA register
TXP2	MAD	PENTA regulator	Logic high ”1”	2.0			V	2 Ghz Transmitter power control enable
			Logic low ”0”			0.5	V	VR11 ON/ OFF
TXA	MAD	PLUSSA	Logic high ”1”	2.5			V	PWR control loop during TX burst

			Logic low ”0”			0.2	V	PWR control loop during ramp up/ down
TXLX1	MAD	RF TDMA 800	Logic high ”1”	2.1			V	Low power level mode for power detector
			Logic low ”0”			0.6	V	High power level mode for power detector
TXLX2	MAD	RF TDMA 1900	Logic high ”1”	2.1			V	Low power level mode for power detector
			Logic low ”0”			0.6	V	High power detector mode power detector
SENA2	MAD	2 Ghz UHF PLL	Logic high ”1”	2.0			V	2 Ghz PLL enable
			Logic low ”0”	0		0.8	V	
RXPWR1	MAD	CCONT	Logic high ”1”	2.0			V	VR4 ON
			Logic low ”0”	0		0.8	V	VR4 OFF
RXPWR2	MAD	PENTA	Logic high ”1”	2.0			V	VR8 ON, 1Ghz fron-tend
			Logic low ”0”	0		0.8	V	VR8 OFF
RXPWR3	MAD	PENTA	Logic high ”1”	2.0			V	VR9 ON 2Ghz fron-tend
			Logic low ”0”	0		0.8	V	VR9 OFF
SPWR1	COB-BA_D	CCONT	Logic high ”1”	2.0			V	VR2 ON , 1Ghz UHF
			Logic low ”0”	0		0.5	V	VR2 OFF
SPWR2	COB-BA_D	CCONT	Logic high ”1”	2.0			V	VR3 ON, VHF ON/ OFF
			Logic low ”0”	0		0.5	V	VR3 OFF
SPWR3	COB-BA_D	PENTA	Logic high ”1”	2.0			V	VR10 ON , 2Ghz UHF
			Logic low ”0”	0		0.5	V	VR10 OFF
TXPWR1	MAD	CCont	Logic high ”1”	2.0			V	VR5 ON , TX pwr control enable
			Logic low ”0”	0		0.5	V	VR5 OFF

TXWR2	MAD	PENTA	Logic high ”1”	2.0			V	VR12 ON , TDMA1900 TX–mixer enable
			Logic low ”0”	0		0.5	V	VR12 OFF
TXWR3	MAD	TDMA800 TX–mixer	Logic high ”1”	2.0			V	AMPS & TDMA800 TX–mixer enable
			Logic low ”0”	0		0.5	V	TX–mixer disable
VR1	CCont	RF	Voltage	2.7	2.8	2.85	V	Supply for VCTCXO, Plussa VHF prescaler and bias, 2 Ghz PLL and 3x
VR2	CCont	RF	Voltage	2.7	2.8	2.85	V	Supply voltage for 1GHZ UHF VCO and prescaler
VR3	CCont	RF	Voltage	2.7	2.8	2.85	V	Supply voltage for VHF VCO, LO buffer, 1 Ghz TX–mixer and TXF
VR4	CCont	RF	Voltage	2.7	2.8	2.85	V	Supply voltage for PLUSSA IF–parts and IF–amplifier
VR5	CCont	RF	Voltage	3.1	3.6	5.3	V	Supply voltage for modulator, TX pwr control
VR6	CCont	RF	Voltage	2.7	2.8	2.85	V	Supply voltage for PLUSSA digital parts and Cobba_D analog supply
VR7	CCont	RF	Voltage	2.7	2.8	2.85	V	TX PA bias and driver supply
V5V	CCont	PLUSSA	Voltage	4.8	5.0	5.2	V	Plussa and 2 Ghz PLL chargepump

Trouble Shooting

The following hints should facility finding the cause of the problem when the circuitry seems to be faulty. This trouble shooting instruction is divided in following section.

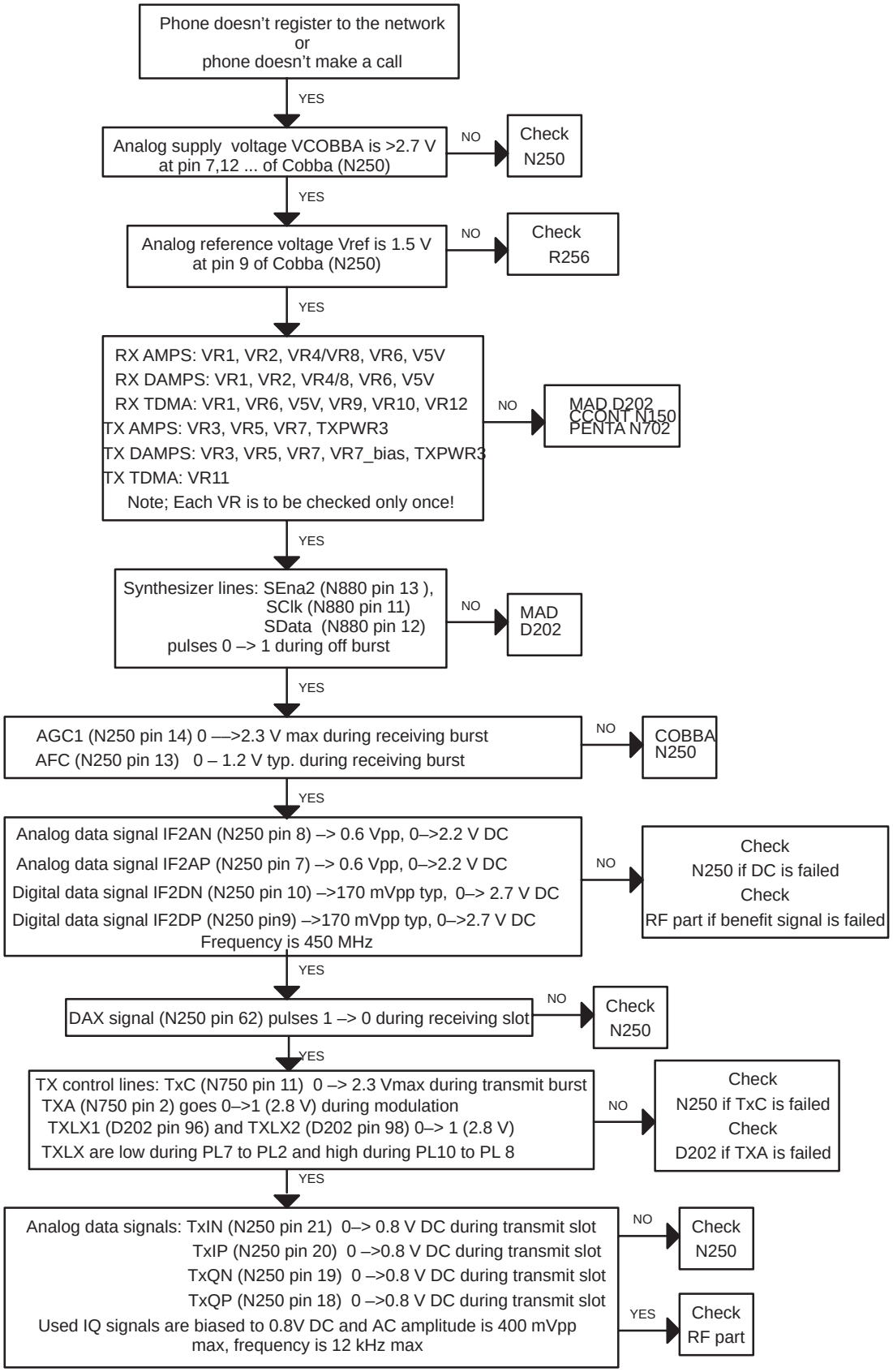
1. Phone is totally dead
2. Flash programming doesn‘t work
3. Power doesn‘t stay on or the phone is jammed
4. Display information: Contact Service
5. Phone doesn‘t register to the network or phone doesn‘t make a call.
6. Audio fault.
7. Charging fault

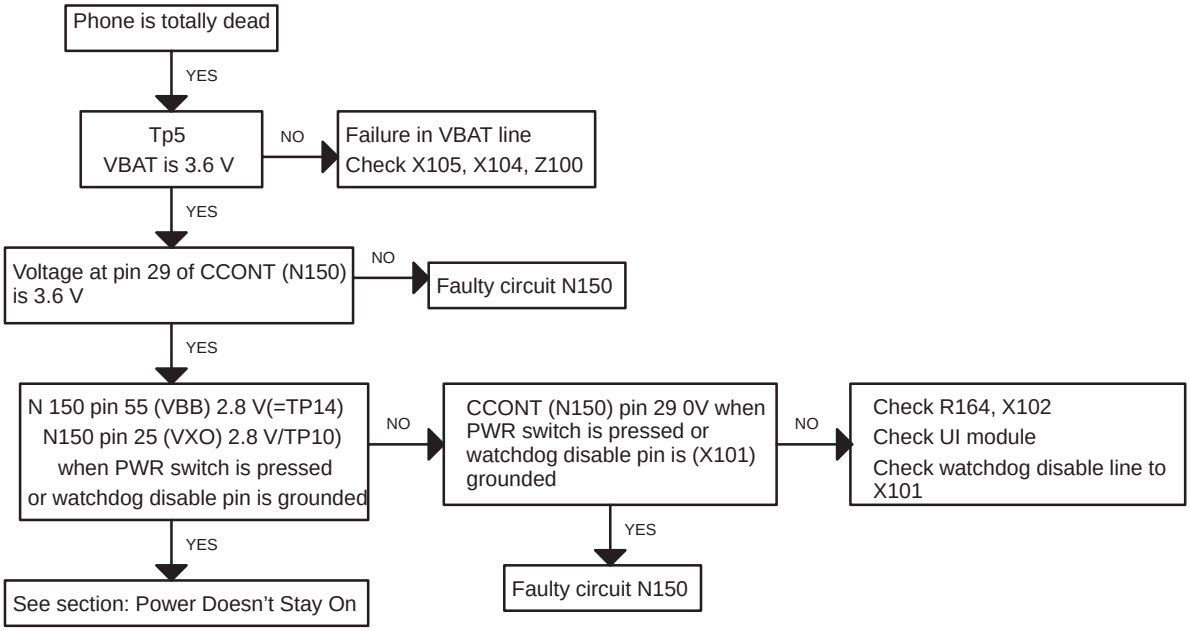
The first thing to do is carry out a through visual check of the module. Ensure in particular that:
a) there are not any mechanical damages
b) soldered joints are OK

Phone is totally dead

This means that phone doesn’t take current at all when the power switch is pressed or when the watchdog disable pin (X101 pin 11) is grounded. Used battery voltage must be higher than 3.0 V. Otherwise the hardware of CCONT (N150) prevents totally from switching.

The phone doesn't register to the network or phone doesn't make a call



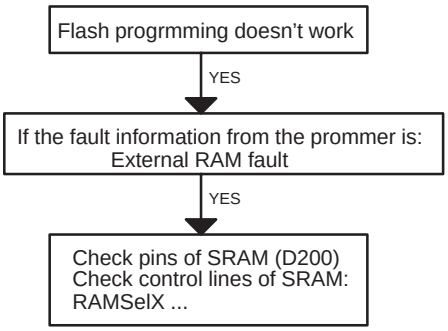


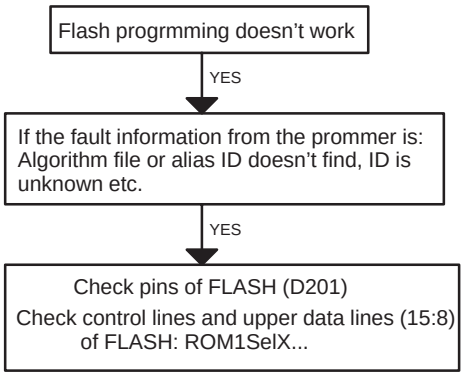
Flash programming doesn't work

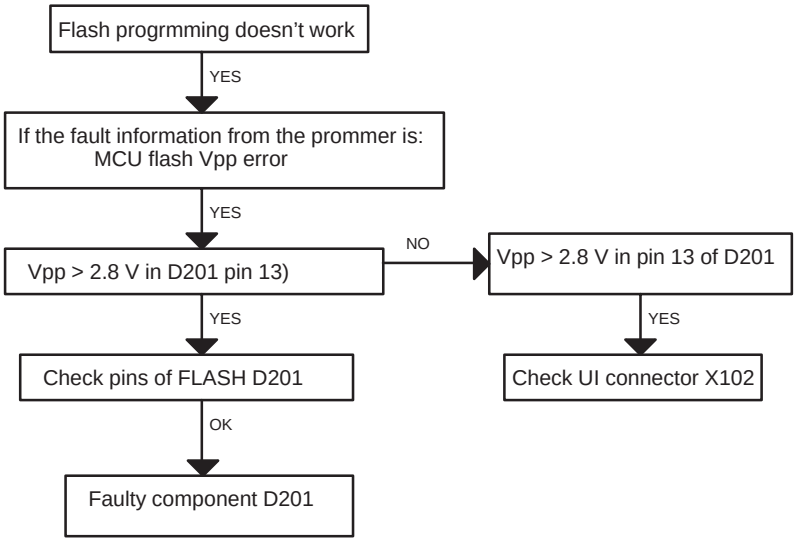
The flash programming can be done via panel connector X101 or via system connector X100.
The main differences between these are:
a) FLASH programming voltage is produced different way.
b) Signal routings are different.

In flash programming error cases the flash prommer can give some information about a fault.
The fault information messages could be:
– MCU doesn't boot
– Serial clock line failure
– Serial data line failure
– External RAM fault
– Algorithm file or alias ID doesn't find
– MCU flash Vpp error

In cases that the flash programming doesn't succeed there is a possibility to check short circuits between the memories and the MCU (MAD1).
This test is useful to do, when the fault information is: MCU doesn't boot, Serial clock line failure or Serial data line failure.


Flash progrmming doesn't work
YES
If the fault information from the prommer is:
External RAM fault
YES
Check pins of SRAM (D200)
Check control lines of SRAM:
RAMSelX ...


Flash progrmming doesn't work
YES
If the fault information from the prommer is:
Algorithm file or alias ID doesn't find, ID is
unknown etc.
YES
Check pins of FLASH (D201)
Check control lines and upper data lines (15:8)
of FLASH: ROM1SelX...


Flash progrmming doesn't work
YES
If the fault information from the prommer is:
MCU flash Vpp error
YES
Vpp > 2.8 V in D201 pin 13)
NO
Vpp > 2.8 V in pin 13 of D201
YES
YES
Check pins of FLASH D201
Check UI connector X102
OK
Faulty component D201

Power doesn’t stay on, or phone is jammed

If this kind of fault has come after flash programming, there are most probably open pins in ICs.

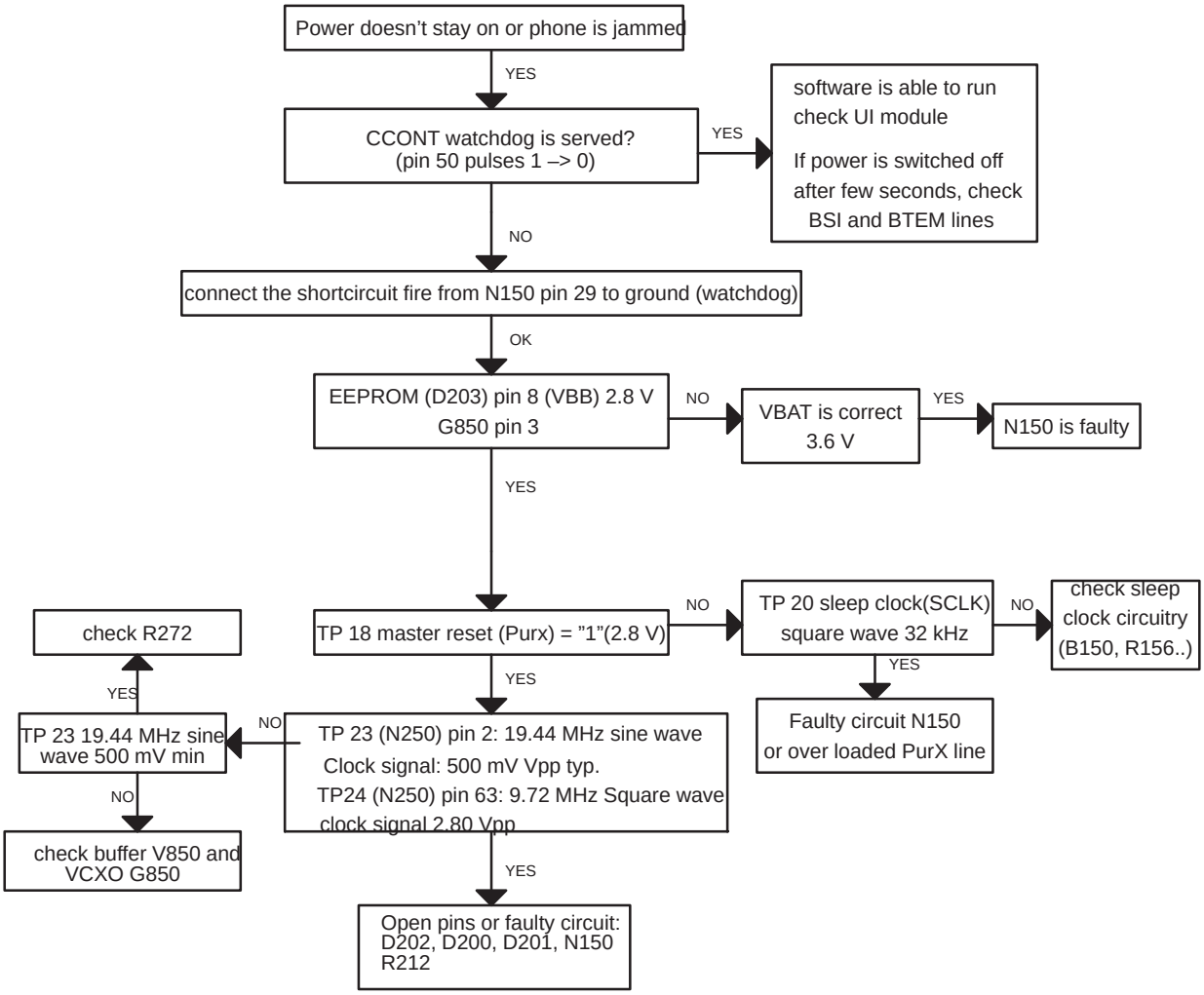
The soldered joints of ICs: D202 (MAD1), D201 (FLASH), N150 (CCONT), D200 (SRAM) are useful to check first.

Normally the power will be switched of by CCONT (N150) after 30 seconds, if the watchdog of the CCONT can not be served by software.

The watchdog updating can be seen by oscilloscope at pin 50 (DataselX) of CCONT.

In a normal case there is a short pulse from ”1” –> 0 every 8 seconds.

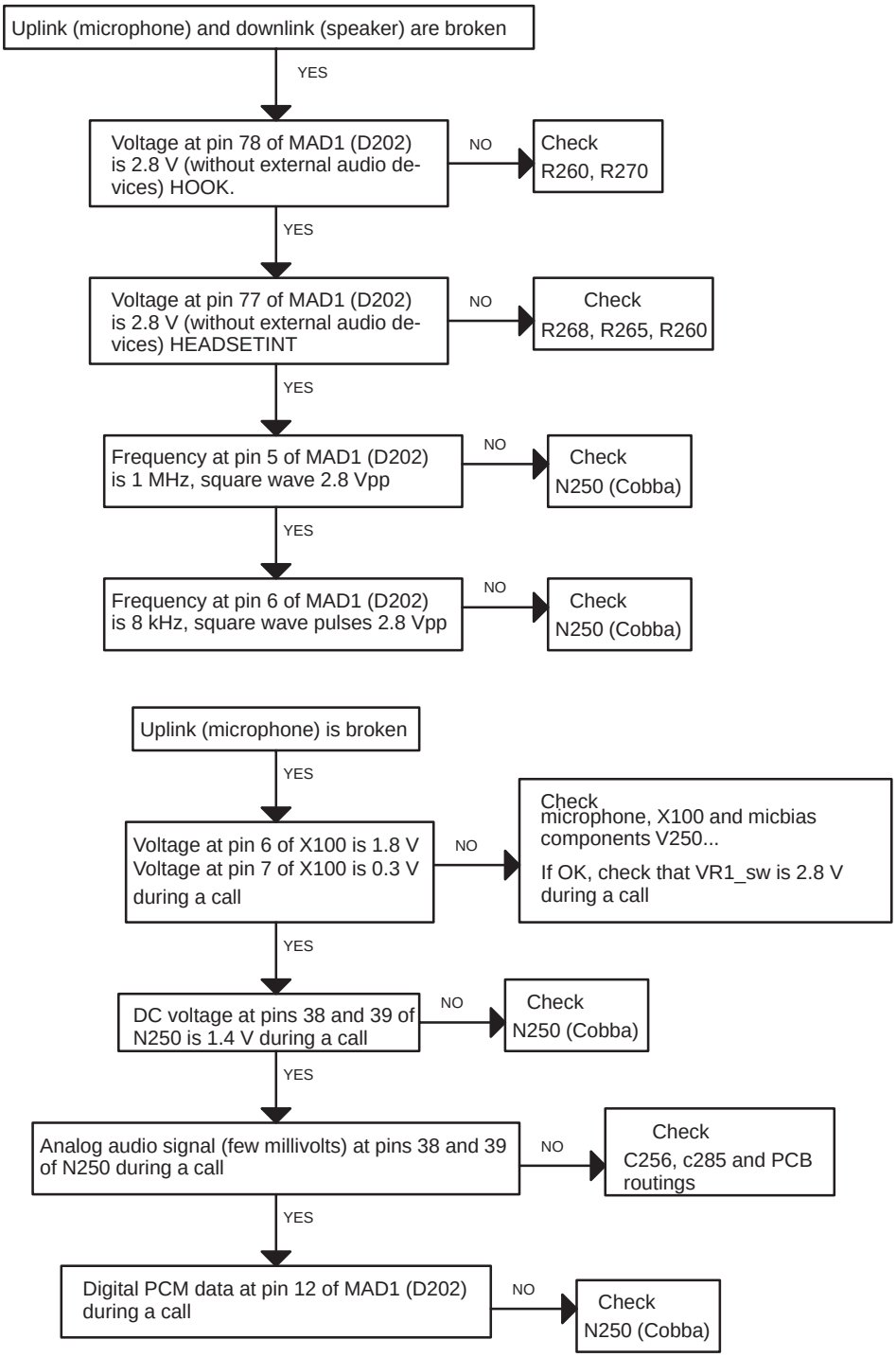
The power off function of CCONT can be prevented by connecting a short circuit wire from CCONT pin 29 to ground.

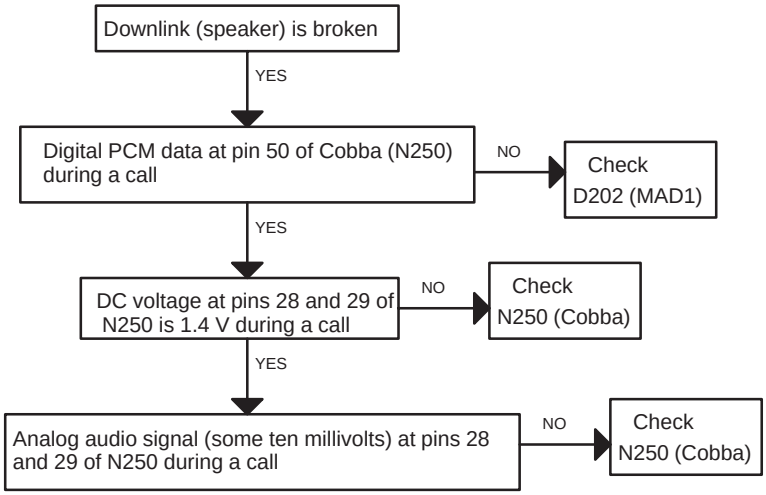

Power doesn't stay on or phone is jammed
YES
CCONT watchdog is served?
(pin 50 pulses 1 –> 0)
YES
software is able to run
check UI module
If power is switched off
after few seconds, check
BSI and BTEM lines
NO
connect the shortcircuit fire from N150 pin 29 to ground (watchdog)
OK
EEPROM (D203) pin 8 (VBB) 2.8 V
G850 pin 3
NO
VBAT is correct
3.6 V
YES
N150 is faulty
YES
TP 18 master reset (Purx) = "1"(2.8 V)
NO
TP 20 sleep clock(SCLK)
square wave 32 kHz
NO
check sleep
clock circuitry
(B150, R156..)
YES
Faulty circuit N150
or over loaded PurX line
YES
check R272
YES
TP 23 19.44 MHz sine
wave 500 mV min
NO
TP 23 (N250) pin 2: 19.44 MHz sine wave
Clock signal: 500 mV Vpp typ.
TP24 (N250) pin 63: 9.72 MHz Square wave
clock signal 2.80 Vpp
NO
check buffer V850 and
VCXO G850
YES
Open pins or faulty circuit:
D202, D200, D201, N150
R212

Display Information: Contact Service

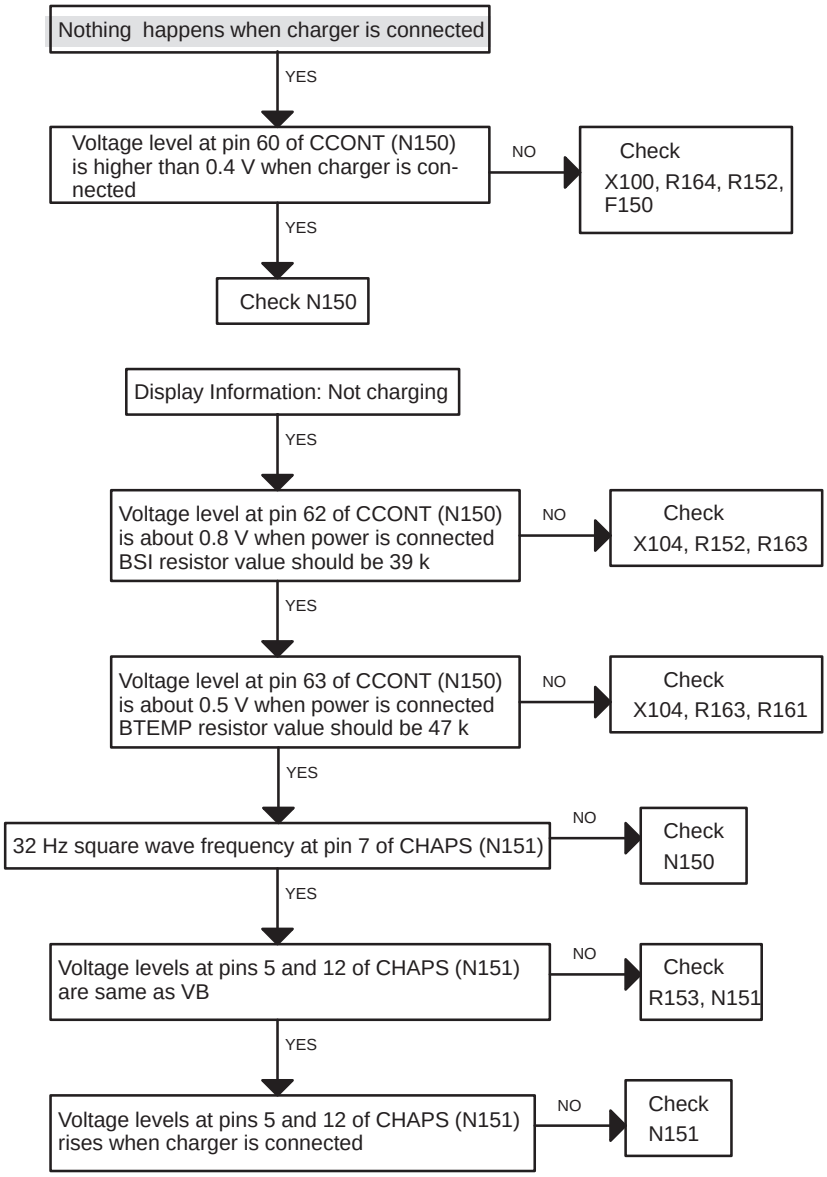
This fault means that software is able to run and thus the watchog of CCONT (N150) can be served.
Selftest functions are run when power is switched on and software is started to excute from flash.
If any of selftests is failed, contact service information will be shown on display.

Audio failure




Downlink (speaker) is broken
YES
Digital PCM data at pin 50 of Cobba (N250) during a call
NO
Check D202 (MAD1)
YES
DC voltage at pins 28 and 29 of N250 is 1.4 V during a call
NO
Check N250 (Cobba)
YES
Analog audio signal (some ten millivolts) at pins 28 and 29 of N250 during a call
NO
Check N250 (Cobba)

Charging failure



Receiver Fault AMPS

General Instructions

Start the WINTESLa software and use it to start the needed RX mode of the phone. The troubleshooting flow chart is divided into three steps:

– general checking,
– local checking
– RX-chain checking.

Make sure to check all solderings and the presence of all components before changing an ASIC or filter.

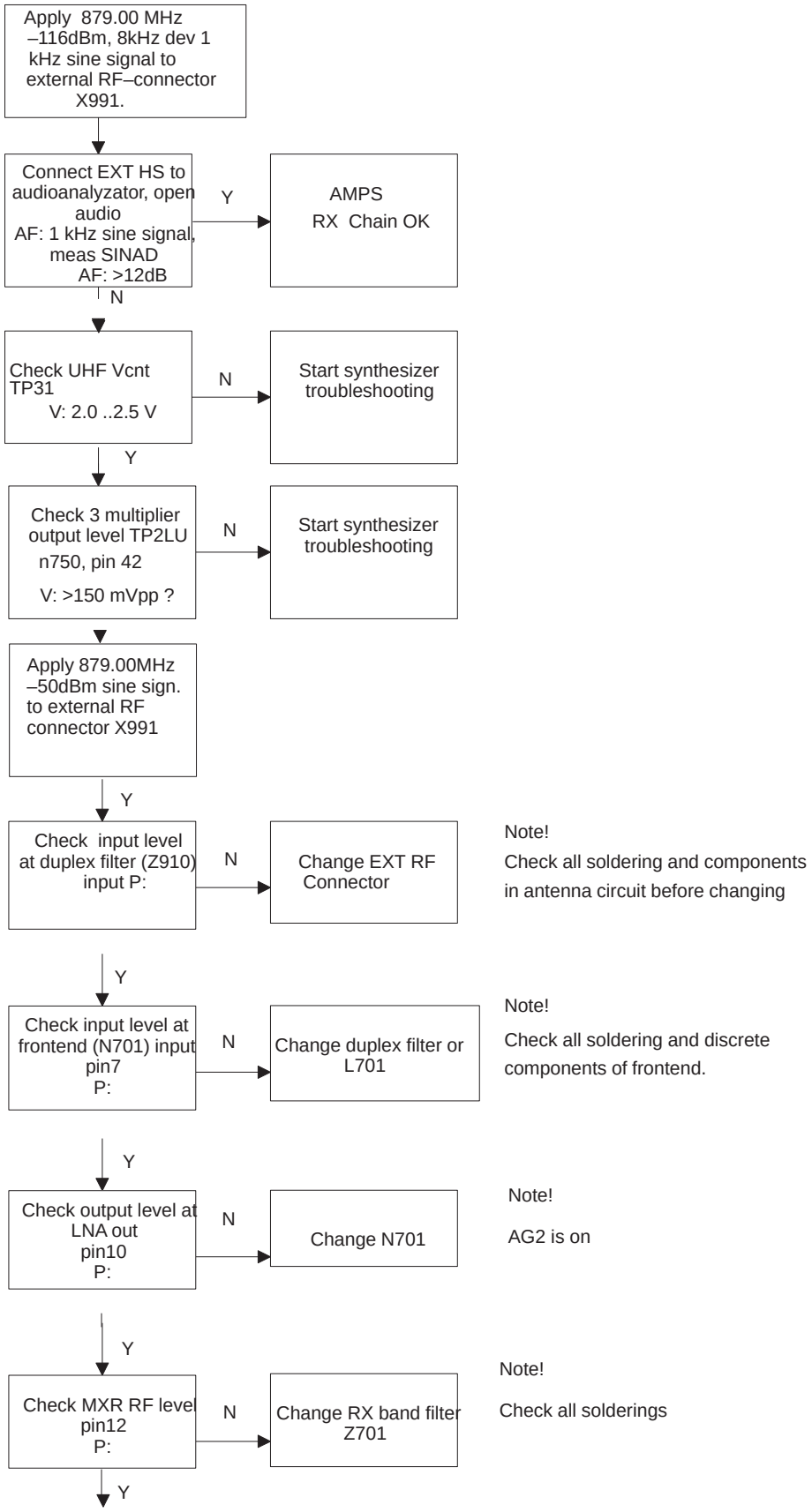
Path of the received signal

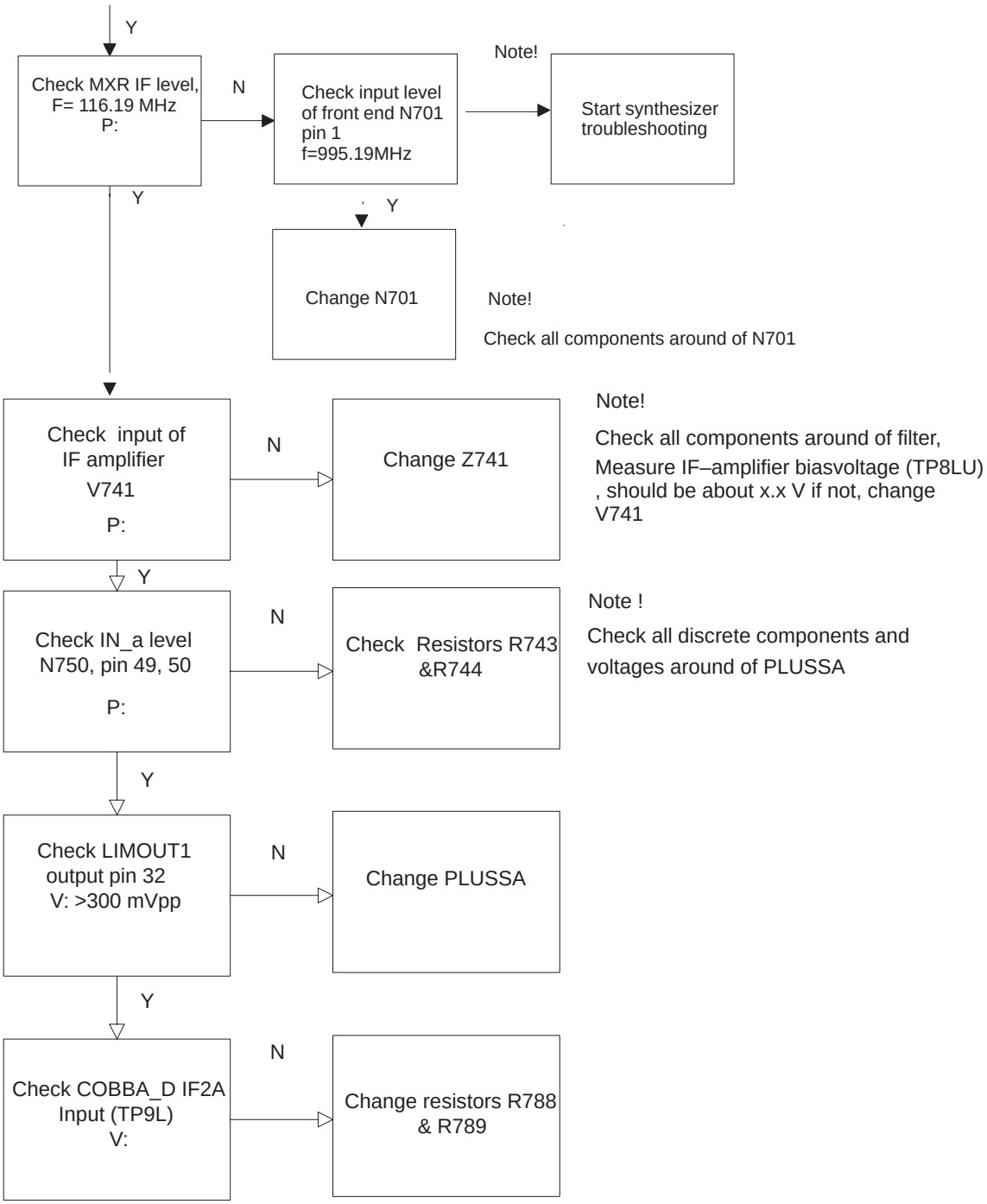
Block level listing:

Path of the received signal
Antenna EXT RF
Duplexer
Low Noise Amplifier (LNA)
RX Filter
First Mixer
116.19 MJz filter
IF amplifer
ACG/Buffer
Second mixer
450 kHz fillter
Buffer/limiter
Baseband (FM detector)

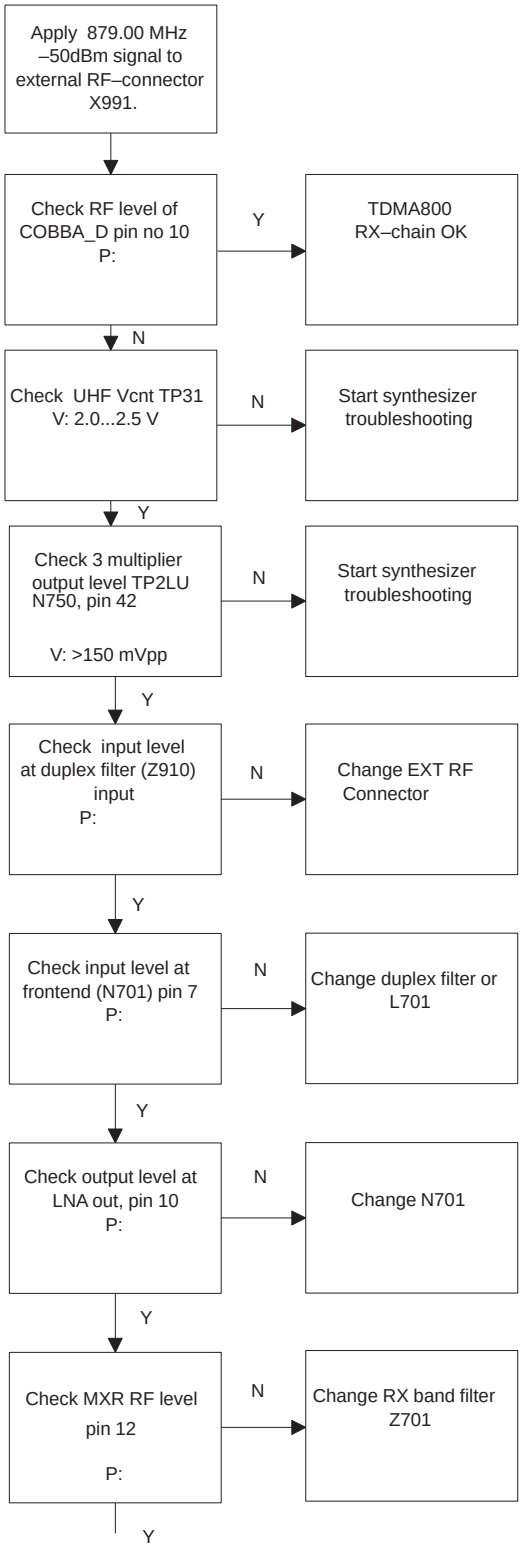
The following fault finding charts are for the receiver chain.

Receiver Fault AMPS




Y
Check MXR IF level,
F= 116.19 MHz
P:
N
Check input level
of front end N701
pin 1
f=995.19MHz
Note!
Start synthesizer
troubleshooting
Y
Y
Change N701
Note!
Check all components around of N701
Check input of
IF amplifier
V741
P:
N
Change Z741
Note!
Check all components around of filter,
Measure IF–amplifier biasvoltage (TP8LU)
, should be about x.x V if not, change
V741
Y
Check IN_a level
N750, pin 49, 50
P:
N
Check Resistors R743
&R744
Note !
Check all discrete components and
voltages around of PLUSSA
Y
Check LIMOUT1
output pin 32
V: >300 mVpp
N
Change PLUSSA
Y
Check COBBA_D IF2A
Input (TP9L)
V:
N
Change resistors R788
& R789

Receiver Fault TDMA800



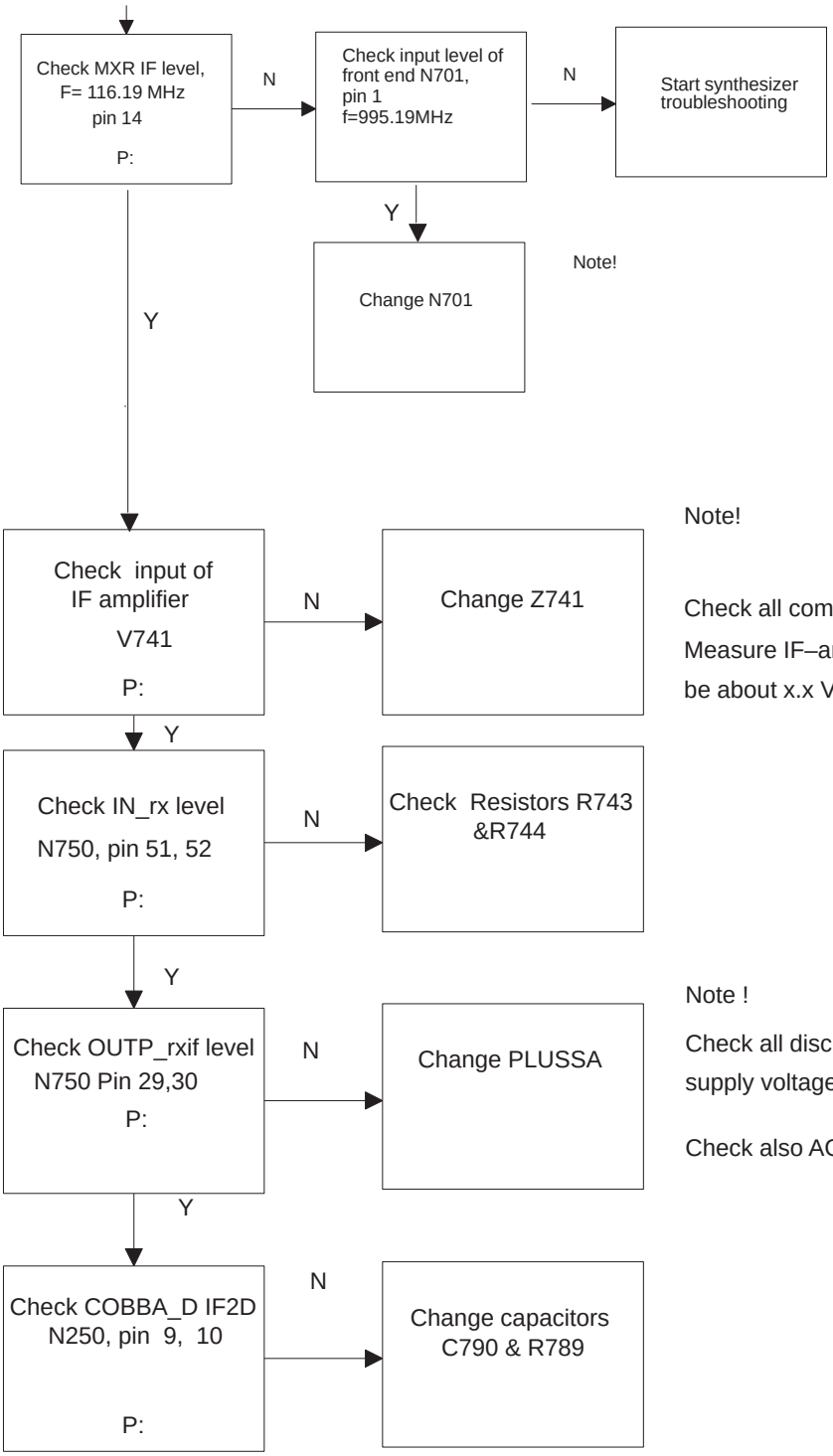
Note!
Check all soldering and components in antenna circuit before changing

Note!
Check all soldering and discrete components of frontend.

Note!
AG2 is on , TP11LU

Note!
Check all soldering

Check all components around of N701



Note!

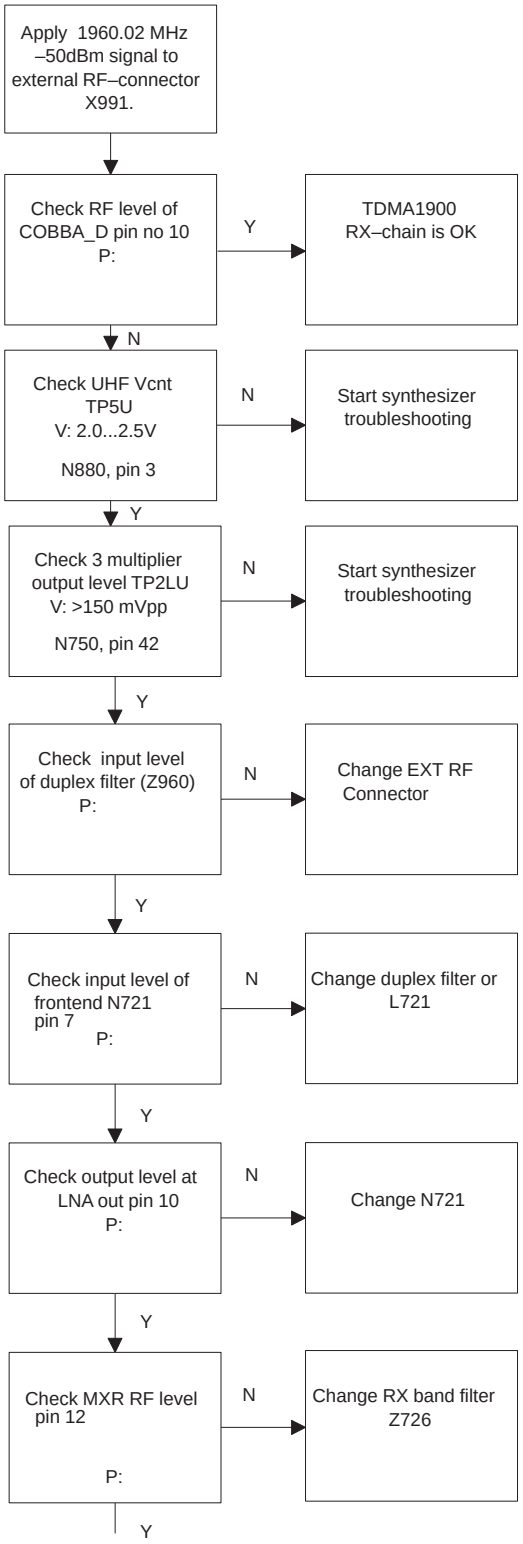
Check all components around of filter, Measure IF–amplifier biasvoltage, should be about x.x V if not change V741 (TP8LU)

Note !

Check all discrete components and supply voltages of PLUSSA..

Check also AGC1 line. (TP10LU)

Receiver Fault TDMA1900 (only for dualbander)



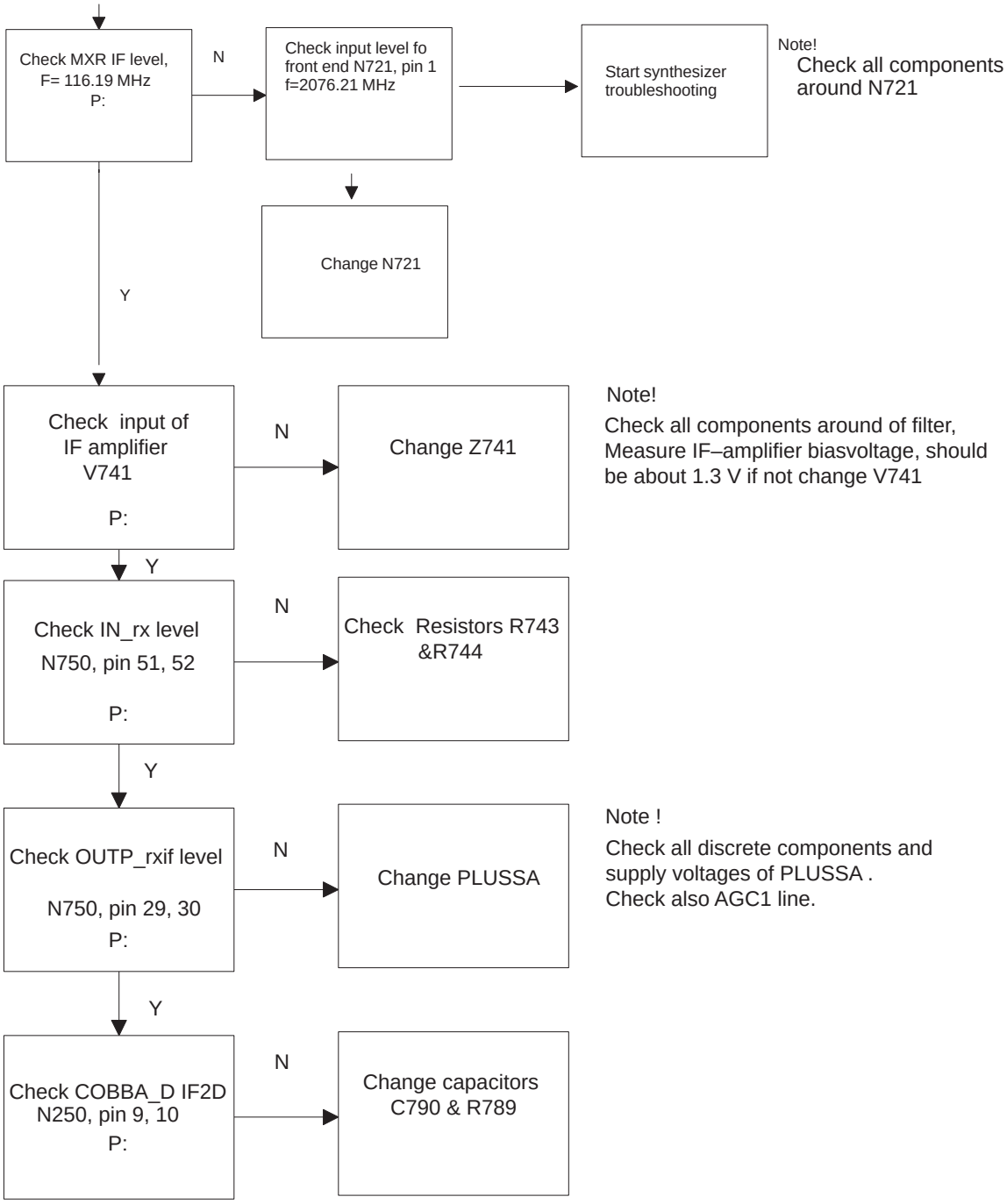
Note!
Check all soldering and components in antenna circuit before changing

Note!
Check all soldering and discrete components of frontend.

Note!
AG2 is on

Note!
Check all soldering

Check all components around of N721


Check MXR IF level,
F= 116.19 MHz
P:
N
Check input level fo
front end N721, pin 1
f=2076.21 MHz
Start synthesizer
troubleshooting
Note!
Check all components
around N721
Change N721
Y
Check input of
IF amplifier
V741
P:
N
Change Z741
Note!
Check all components around of filter,
Measure IF–amplifier biasvoltage, should
be about 1.3 V if not change V741
Y
Check IN_rx level
N750, pin 51, 52
P:
N
Check Resistors R743
&R744
Y
Check OUTP_rxif level
N750, pin 29, 30
P:
N
Change PLUSSA
Note !
Check all discrete components and
supply voltages of PLUSSA .
Check also AGC1 line.
Y
Check COBBA_D IF2D
N250, pin 9, 10
P:
N
Change capacitors
C790 & R789

Transmitter Fault – General

Always use a RF–cable connected from an external RF connector to the analyzer via RF–power attenuator. This is important to protect the analyzer against excessive RF power and to not let unwanted RF power leak in the cellular frequencies.

Start the WINTESLA software and select the TX mode for testing (AMPS, DAMPS, or TDMA 1900). Select mid channel (383 for AMPS, DAMPS or 1000 for TDMA 1900) Select random data for digital mode of operation.

One of the basic test is to monitor current when transmitter is on. If the current consumption does not change when transmitter is turned on, the fault is in the PA. Also if pressing the PA chip more tightly to PCB does have an effect on current consumption, the fault is in PA.

In case of a faulty PA the IC can be changed only under correct (ESD) grounding and using only a hot air blower set to 10m/s and 300 degree centigrade. The new chip must be taken from its vacuum package and the heating process must be done in less than 30 second. Note that the bottom plate of the chip must be properly soldered and excessive solder material, if any, has to be remove.

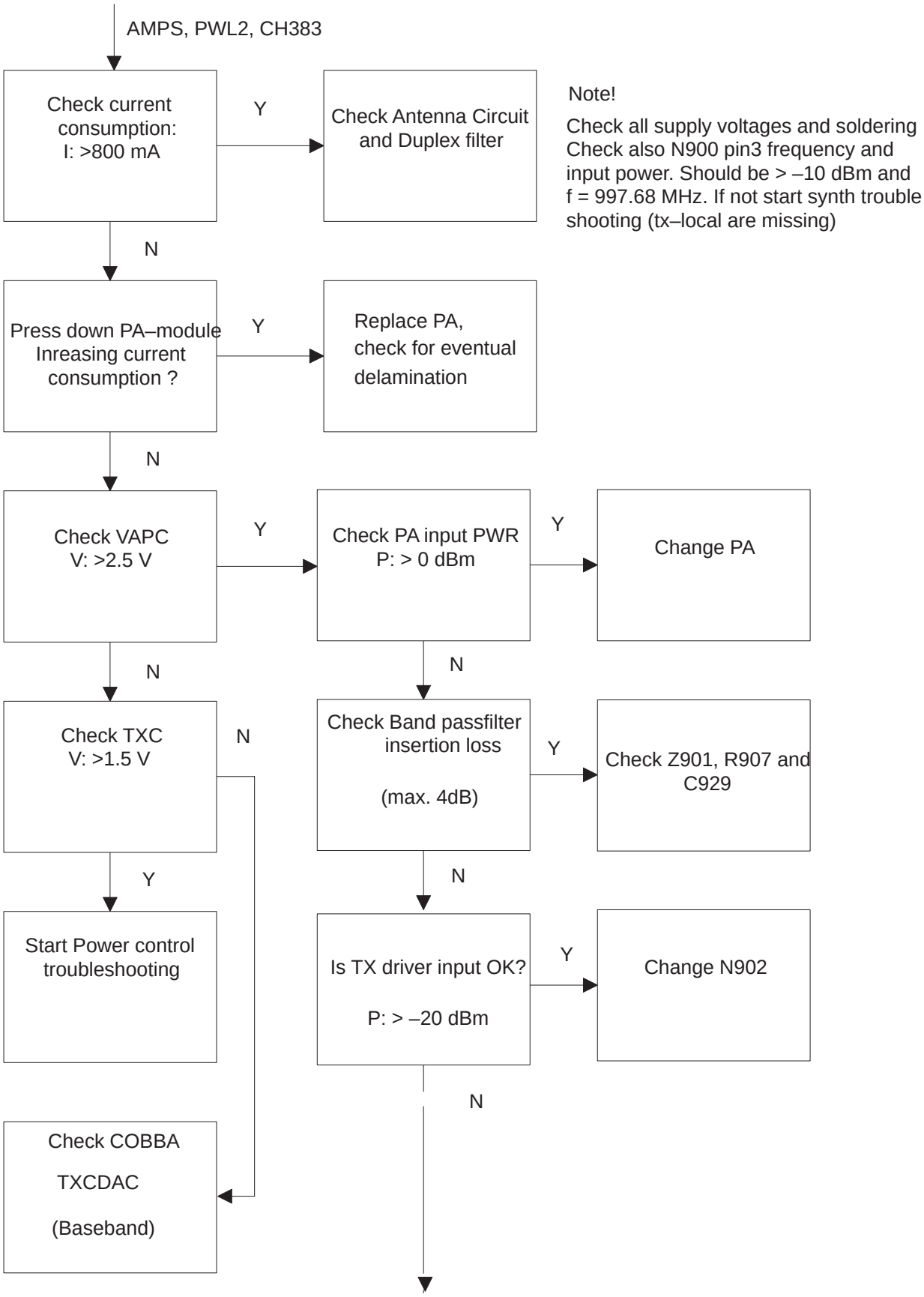
Path of the transmitted signal

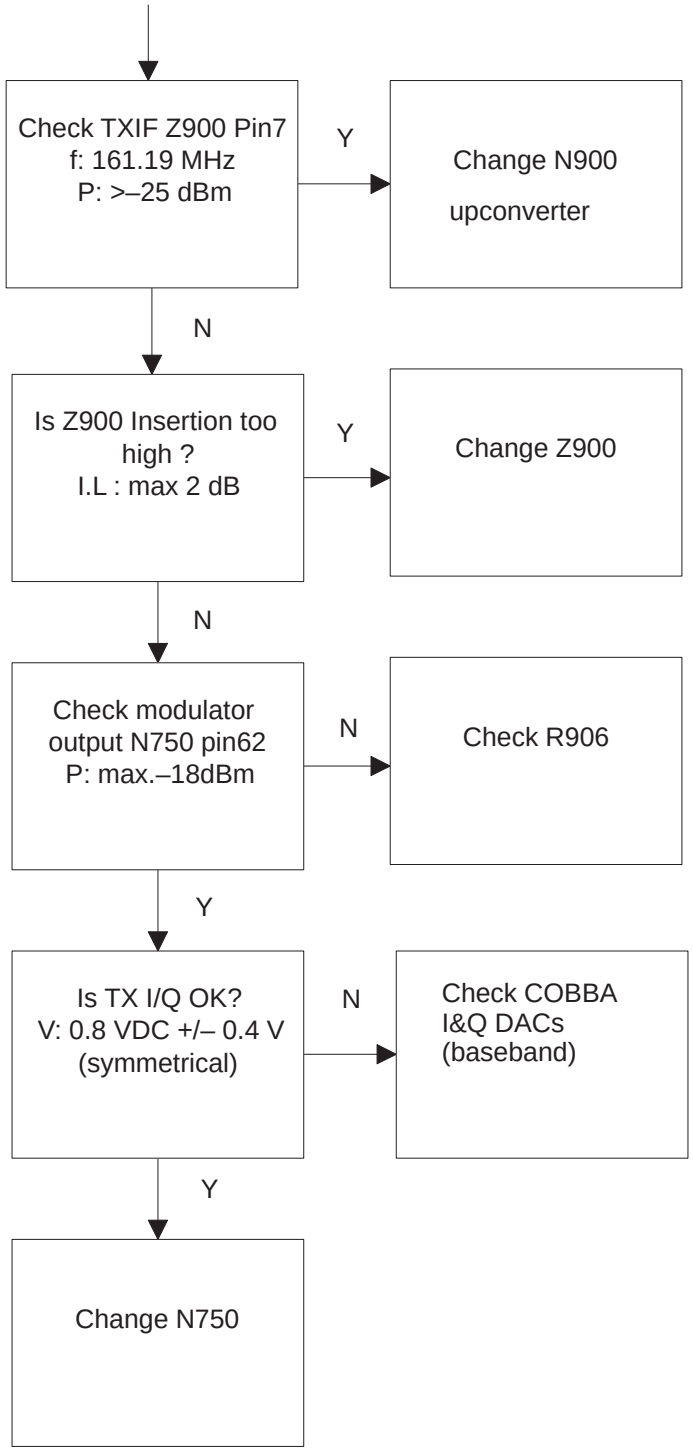
Block level listing AMPS, DAMPS	Block level listing TDMA 1900
COBBA TX I/Q DA–converters	COBBA TX I/Q DA–converters
I/Q modulator and Digital gain step amplifier	I/Q modulator and Digital gain step amplifier
IF–BPF	IF–BPF
Upconverter	Upconverter
TX Driver	BPF
BPF	TX Driver
PA	BPF
Coupler	PA
Duplex filter	Coupler
Antenna matching circuit	Duplex filter
EXT RF connector	Antenna matching circuit
Antenna	EXT RF Connector
	Antenna

Power detection and power control circuit are included in the power control part of this guide.

Start the WINTESLA software and set the phone in Analog mode. Set Channel 383 and Power level 2. Apply the RF cable to Ext RF onnector and connect the cable to the spectrum analyzer input, measure the RF level. Notice the insertion loss of the cable and the attenuators. Use external attenuator to avoid overloading the spectrum analyzer.

Transmitter Fault AMPS

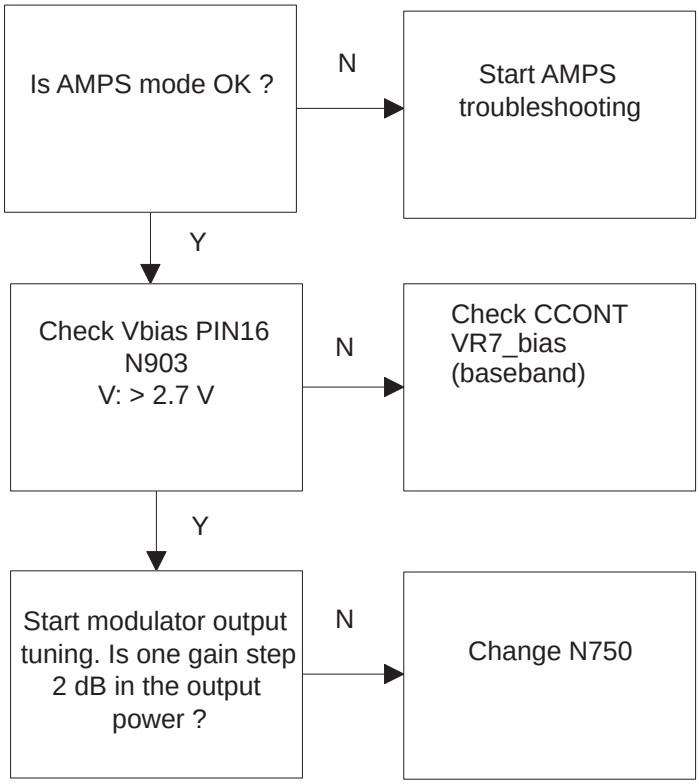




Note!
check also I/Q–resistors

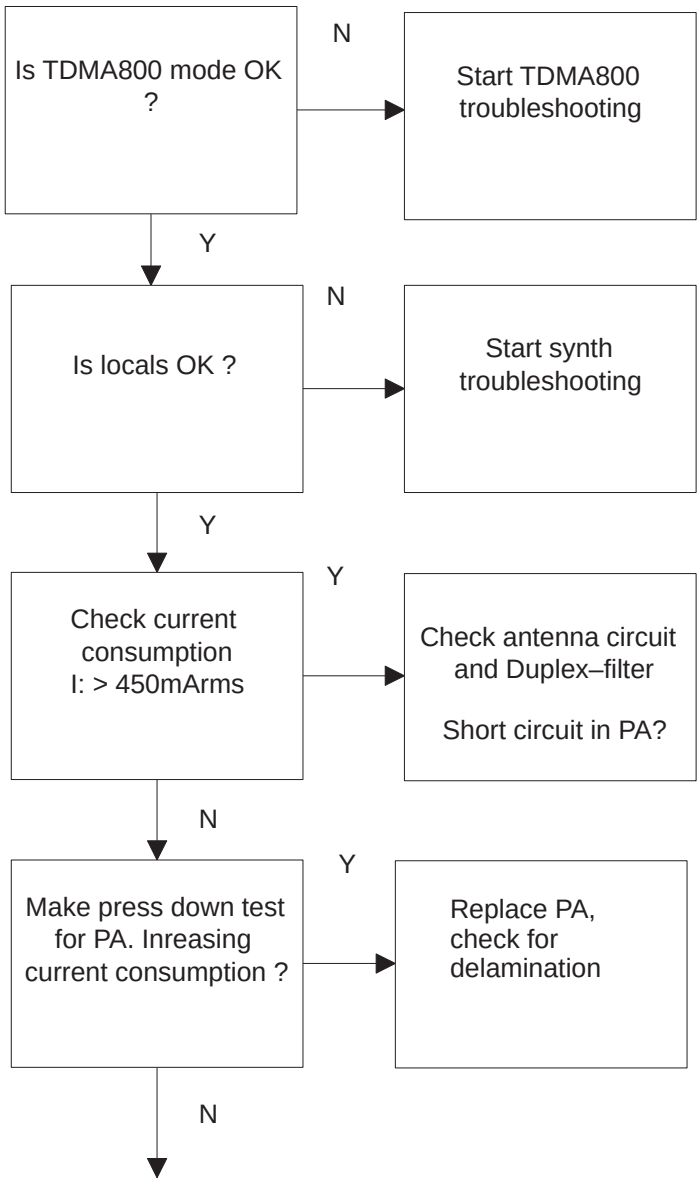
Transmitter Fault TDMA800

The transmitter is the same as in AMPS mode, but the power amplifier is biased to more linear. Consequently it is essential that the AMPS is free of any faults.



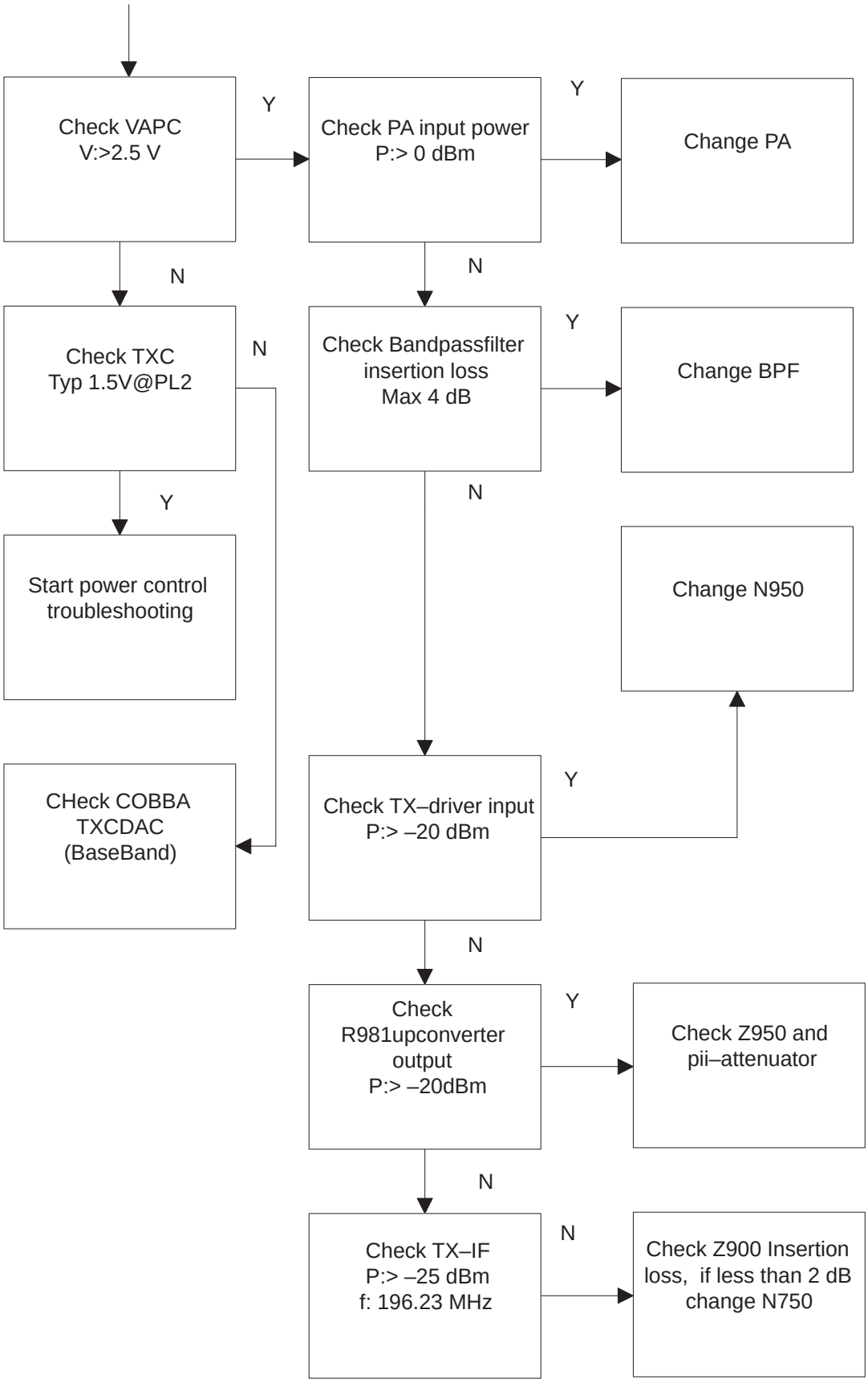
Transmitter Fault TDMA1900

TDMA1900 and DAMPS modes share a common IF section and antenna circuit. Consequently it is essential that the DAMPS mode is free of any faults.



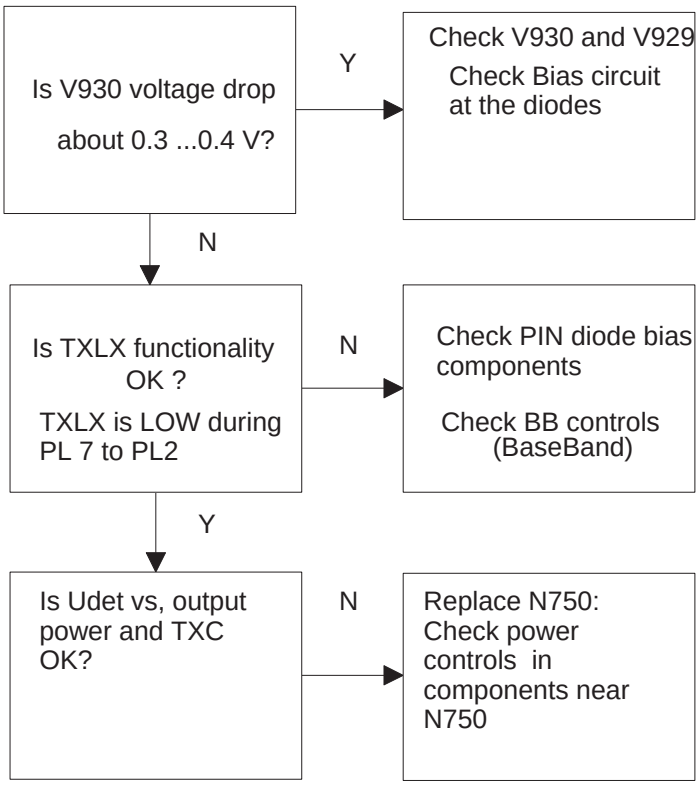
Note!

Check VHF and UHF locals including Lo–buffer, measuring point for UHF is N980 pin5.


Check VAPC
V:>2.5 V
Y
Check PA input power
P:> 0 dBm
Y
Change PA
N
N
Check TXC
Typ 1.5V@PL2
N
Check Bandpassfilter
insertion loss
Max 4 dB
Y
Change BPF
Y
N
Start power control
troubleshooting
Change N950
CHeck COBBA
TXCDAC
(BaseBand)
Check TX–driver input
P:> –20 dBm
Y
N
Check
R981upconverter
output
P:> –20dBm
Y
Check Z950 and
pii–attenuator
N
Check TX–IF
P:> –25 dBm
f: 196.23 MHz
N
Check Z900 Insertion
loss, if less than 2 dB
change N750

Power Control Loop

Power control section is basically similar for both band except both bands include a coupler and detector. The power control is actually effected in the PLUSSA IC.



Note !

See Udet vs. Output power curve

Note !

1. Gain control voltage of driver is directly proportional to output power and TXC voltage in AMPS MODE.
2. Gain coltrol voltage of driver will remain same (+/– 2dB typ.) regardless of power level and TXC voltage in DIGITAL MODE.
3. Udet and TXC will be about same in each mode.
4. TXA is high during modulation (any).
5. TXLX signals will carry about 4mA in HIGH state.

Typical detected voltage level at different power levels, +32 C:
HD961/HD963

LB:

		TXC	
PL	10	–348	0.36736
	9	–319	0.43232
	8	–283	0.51296
	7	–324	0.42112
	6	–291	0.49504
	5	–243	0.60256
	4	–170	0.76608
	3	–61	1.01024
	2	106	1.38432

UB:

		TXC	
PL	10	–352	0.3584
	9	–313	0.44576
	8	–259	0.56672
	7	–291	0.49504
	6	–262	0.56
	5	–225	0.64288
	4	–163	0.78176
	3	–46	1.04384
	2	74	1.31264

NOTE: DAC VALUES MAY VARY +/– 150 DAC UNITS

Synthesizers

There are four oscillators generating the needed frequencies for RF–section. They are

19.44 MHz reference oscillator,	
1GHz UHF VCO,frequency range	985.23 ... 1010.2 MHz
2Ghz UHF VCO frequency range	2046.2 ... 2107.2 Mhz
VHF VCO.has two fixed frequencies,	322.38 Mhz for lowband
	392.46 for upper band

VHF VCO operating frequency is controlled by the BAND–signal and the PLL–circuit of the PLUSSA. All locals are locked to a stable reference oscillator.

A practical way to check the synthesizer status is measuring the control voltage of the VCO from the Integrator capacitor. If the voltage is stable and reasonable, the local oscillators are running correctly.

19.44 MHz reference oscillator

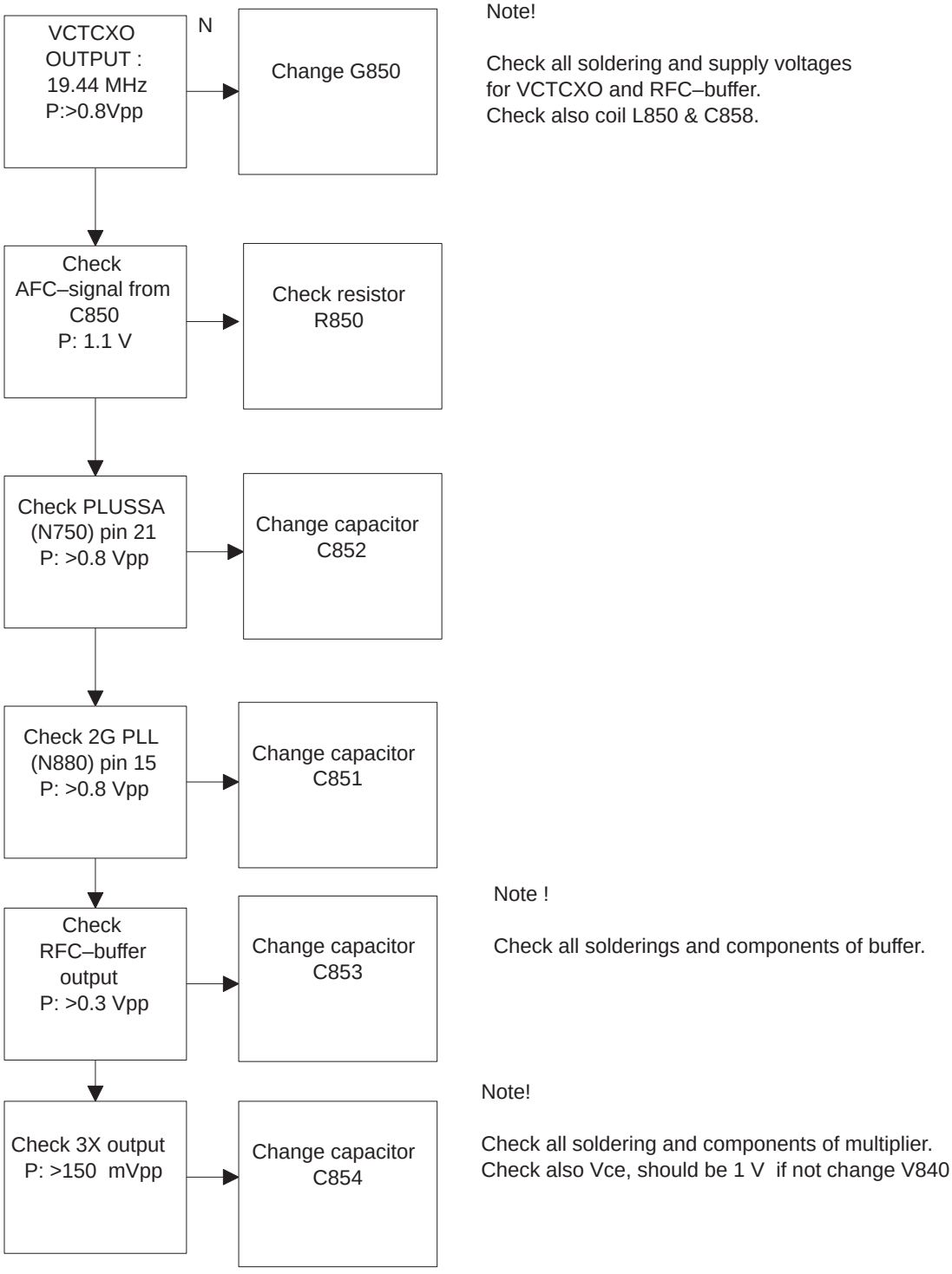
The 19.44 MHz oscillator frequency (G850)is controlled by the COBBA_D. This signal is fed to the PLUSSA and TDMA1900 PLL circuit. All synthesizers use the divided signal as reference signal for the phase locked loop to provide a correct LO frequency. The VCTCXO output signal is also used to generate the 2LO frequency by multipliers.

The baseband clock signals are generated from this signal. The VCTCXO output signal is buffered and connected to MAD2.

58.32 MHz 3–multiplier

The 3–multiplier is a discrete circuit which is used to generate the second local frequency for the receiver. The multiplier output signal is connected to the PLUSSA IN_X2 pin. In the PLUSSA the signal is multiplied by 2 and then fed to the 2nd mixer.

19.44 MHz oscillator and 3–multiplier troubleshooting



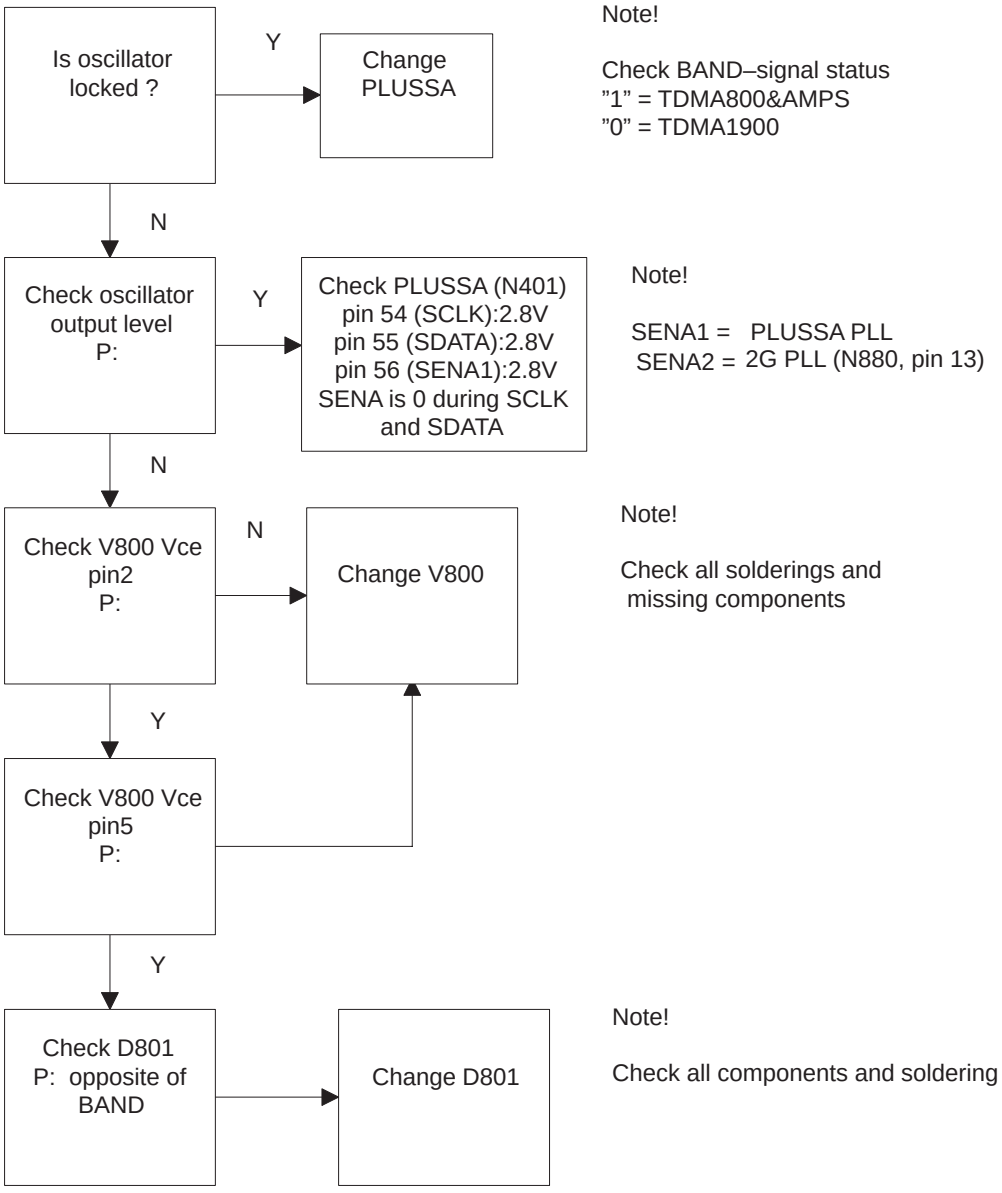
VHF VCO

The VHF VCO signal is used to generate the transmitter intermediate frequencies. The VHF VCO has two fixed frequencies. The operating frequency is locked in phase locked loop which is controlled by the baseband

Because the oscillator employs two frequencies it also has two diferent switching modes. These modes are controlled by the BAND signal. In AMPS and TDMA800 modes the frequency is 322.38 MHz and the logical level of the BAND signal is ”HIGH”. In TDMA1900 mode a higher if is needed and the operating frequency is increased to 392.46 MHz. The BAND signal is also set to logical level ”zero”

The VHF VCOoutput signal is fed to the PLUSSA LO pin no.8. In the PLUSSA the signal is divided for the phase detector and TX elements. Before being fed to the I/Q–modulator the frequency is divided by 2.

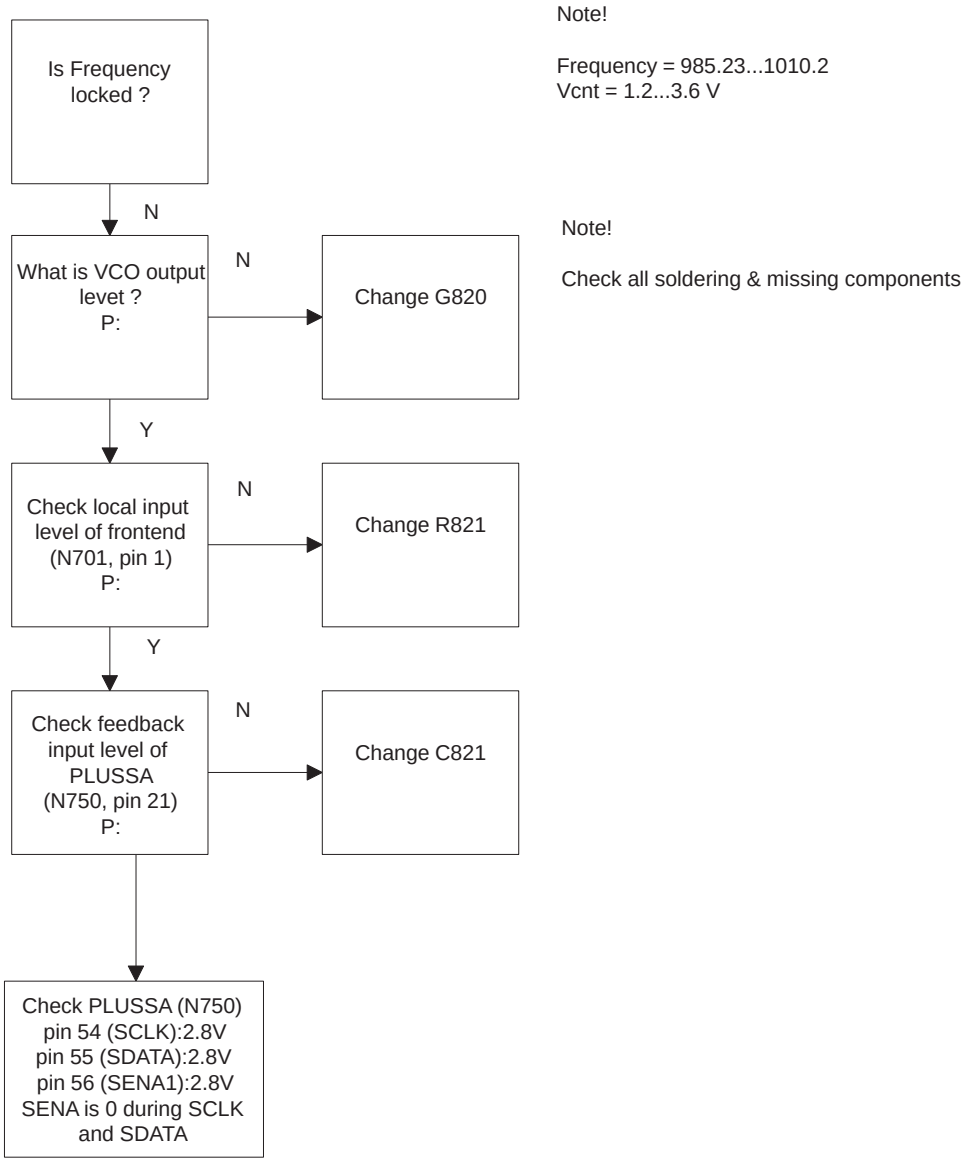
VHF VCO troubleshooting



AMPS & TDMA UHF SYNTHESIZER

The 1GHz UHF VCO (G820) generates the first injection for RX (869...897MHz) and the final injection for TX (824...849 MHz) . The output frequency of the module depends on thje DC control voltage supplied by the PLUSSA.

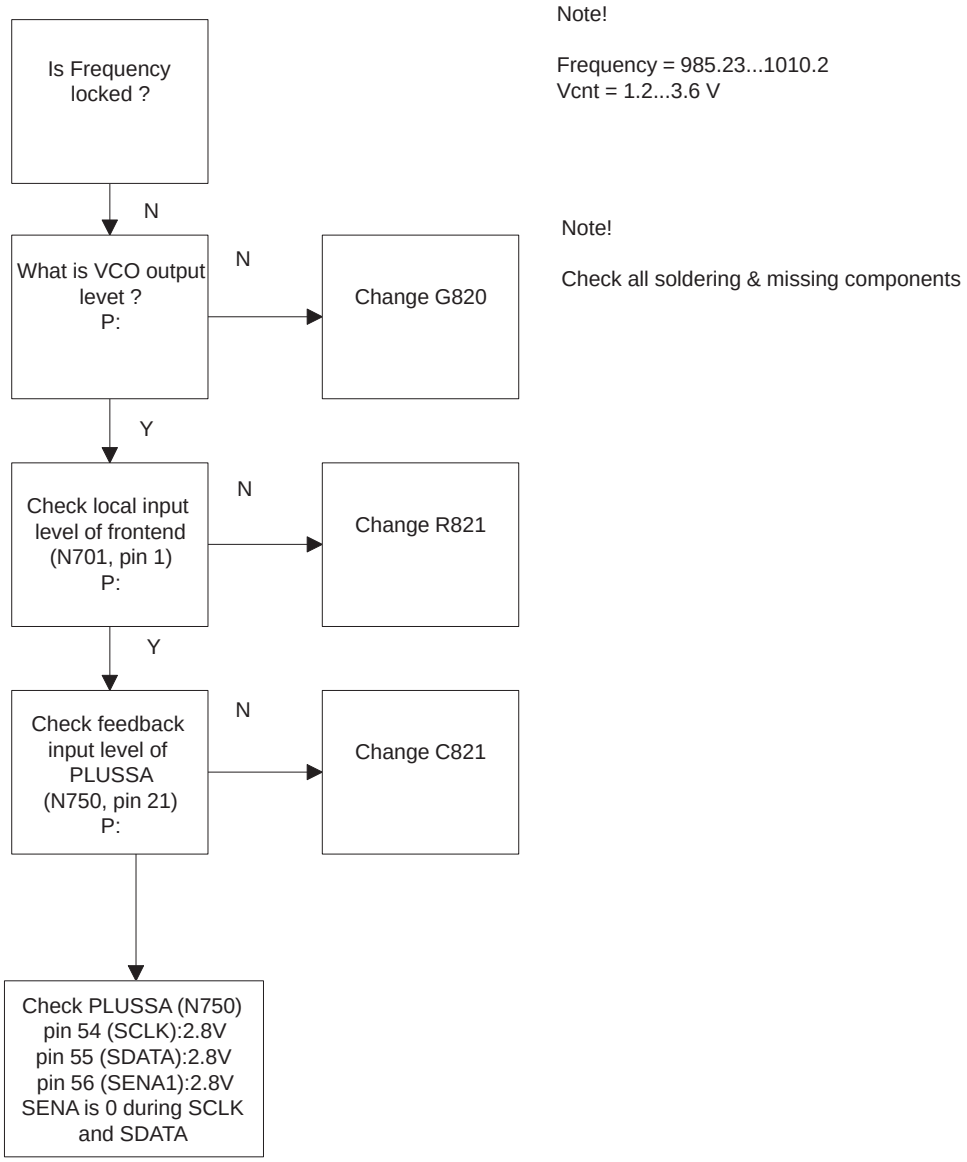
1GHz UHFsynthesizer troubleshooting



TDMA1900 UHF Synthesizer 2 GHz (ONLY DUALBANDER)

The 2GHz UHF synthesizer generates the needed injection frequencies for TX and RX chain. The output frequency of the VCO depends on the control voltage supplied by the PLL circuit.

2 GHz UHF synthesizer troubleshooting



About RF ASICs and MMIC PA

General information

The PLUSSA (N750) provides two main functions:

1. RX/TX blocks
2. PLL

The receiver block consists of IF buffers, active mixers, 2–multiplier, AGC amplifier and limiter.

The transmitter section includes a digital gain step amplifier, a divider , an I/Q Modulator and control part for the Transmitter Power Control loop.

The PLL section is controled via the serial bus and contains both UHF and VHF PLL and predividers.

PLUSSA ASIC

Pin #	Pin name	Nominal level	Description
1	TXP_pwc	2.8V	TX power control enable
2	TXA_pwc	2.8V	TX power loop control mode
3	INPi_tx	0.8V	Positive I–channel input of the TX
4	INMi_tx	0.8V	Negative I–channel input of the TX
5	INMq_tx	0.8V	Positive Q–channel input of the TX
6	INPq_tx	0.8V	Negative Q–channel input of the TX
7	GND_P1	0	Ground
8	LO	?	VHF VCO signal
9	VP1	2.8V	VHF prediv supply voltage from CCONT
10	VOP	2.8V	Positive supply voltage for the 1st opamp in pwrcnrl
11	TXC_pwc	0.5–2V	Power level control of the TX
12	DET_pwc	?	Feedback from the peak detector diode
13	TXI_pwc	–	False transmission indicator
14	opain_pwc	–	Input for the 2nd opamp in the pwr cntrl loop
15	opaout_pwc		Opamp output for external feedback
16	OUT_pwc	–	Output voltage for TX–driver
17	VCE1	~5V	VHF charge pump V5V–signal from BB
18	PD	?	VHF charge pump output
19	VSE1	0	Ground for VHF charge pump
20	DGND	0	Digital ground
21	OSC	?	19.44 MHz–signal from G850
22	VDD	2.8V	Positive supply for digital parts
23	GND_P2	0	Ground for UHF predivider
24	U_in	0dBm	UHF VCO signal from G820
25	VP2	2.8V	Positive supply for UHF predivider
26	VSE2	0	Negative supply for UHF charge pump
27	PD2	–	UHF charge pump output

28	VCE2	~5V	V5V–signal for UHF charge pump from BB
29	OUTP_rxif	?	Positive output of the receiver output gain stage
30	OUTM_rxif	?	Negative output of the receiver output gain stage
31	LIMOUT2	–	Negative output of the limiter amplifier
32	LIMOUT1	–	Positive output of the limiter amplifier
33	RSSI	–	Received signal strenght indicator voltage
34	INM_rxif	?	Negative input of the receiver output gain stage
35	INP_rxif	?	Positive input of the receiver output gain stage
36	LIMIN2		AC ground of limiter offset comp feedback
37	LIMIN1		Limiter amplifier input
38	LIMD1		AC ground of limiter offset comp feedback
39	UB_a2		Filtering cap for bias of lim amplifier
40	VRX_limi	–	Positive supply of lim amplifier and RSSI
41	GND_if2	0	Ground
42	IN_X2	–	Input to x2–frequency multiplier
43	Vcc_x2	–	Positive supply of x2 block
44	OUTP_rx	?	Positive mixer output of the receiver
45	OUT_rx_a		Positive output of analog mode RX mixer
46	UB_a1	–	Filtering cap for bias of analog mode RX
47	VRX	2.8V	Power supply of the receiver
48	GND_if1	0	Ground
49	INP_a	–	Positive input of analog mode rx amplifier
50	INN_a	–	Negative input of analog mode rx amplifier
51	INM_rx	–	Negative input of the receiver
52	INP_rx	–	Positive input of the receiver
53	GC_rx	?	RX gain control signal
54	SCLK	0.8–2V	Clock for PLL serial programming and digital gain step amplifier adjusting
55	SDAT	0.8–2V	Data for PLL serial programming and digital gain step adjusting
56	SLE	0.8–2V	Latch enable for PLL serial programming and digital gain step adjusting
57	VB2_rx	0	Connection for filtering capacitor of Bias voltage of RX&TX
58	VB_ext	1.5V	VREF–signal from BB
59	IB	0	Internal Bias voltage
60	GND	0	Ground
61	OUTN_tx	?	Negative output of the transmitter
62	OUTP_tx	?	Positive output of the transmitter
63	VTX	2.8V	Positive power supply of the transmitter
64	LO_out		Not connected

Receiver front ends

Pin #	Pin name	Nominal level	Description
1	LO IN	?	Mixer lo input
2	Vdd buf	2.8V	Lo–buffer Vdd
3	LO out		Lo–buffer output
4	GND	0	ground
5	Vdd LNA	2.8V	LNA Vdd
6	GND	0	ground
7	LNA in	?	LNA RF input port
8	GND	0	LNA ground
9	Gain sel		LNA gain select
10	LNA out		LNA output port
11	GND	0	ground
12	Mxr RF	?	Mixer RF input port
13	GND	0	ground
14	MXR IF	?	Mixer IF input port
15	GND	0	ground
16	Vdd MXR	?	Mixer lo–buffer Vdd and lo–buffer tuning

MMIC Power Amplifiers

Pin #	Pin name	Nominal level	**Description N960**
1	Vcc	VBAT	Power supply for bias circuit
2	N/C	–	Not connected
3	LTune	?	Tuning pin for interstage matching network
4	Vcc1	VBAT	Power supply for the 1st stage collector
5	GND1	–	Ground
6	RF IN		RF input
7	N/C	–	Not connected
8	Vreg	2.8V	Regulated power supply for bias circuit. PA shut down
9	N/C		Not connected
10	N/C		Not connected
11	N/C		Not connected
12	RF OUT	?	RF output and bias for output stage
13	RF OUT	?	RF output and bias for output stage
14	2*fo	?	Second harmonic trap
15	N/C		Not connected
16	Vbias	–	Bias control 2.8V
Package Base	Ground	–	Ground connection. The backside of the package must be connected to the ground plane throught a short path

Pin #	Pin name	Nominal level	**Description N960**
1	N/C		Not connected
2	N/C		Not connected
3	Vcc/Q2C	VBAT	Power supply for the 2nd stage
4	Vcc/Q1C	VBAT	Power supply for the 1st stage.
5	GND	–	Ground
6	RF IN	?	RF input
7	GND	–	Ground
8	Vreg	2.8V	Regulated voltage supply for the bias circuit
9	N/C		Not connected
10	Bias		Bias ground
11	RF OUT	?	RF output matching
12	RF OUT	?	RF output and bias for output stage
13	RF OUT	?	RF output and bias for output stage
14	RF OUT	?	Second harmonic trap
15	N/C		Not connected
16	N/C		Not connected
Package Base	Ground	–	Ground connection. The backside of the package must be connected to the ground plane throught a short path

PENTA regulator

Pin #	Pin name	Nominal level	Description
1	Bypass	–	Pin for external bypass capacitor
2	Common enable	?	Enable for whole circuit
3	VR1cntrl		Regulator 1 ON/OFF
4	VR2cntrl		Regulator 2 ON/OFF
5	VR3cntrl		Regulator 3 ON/OFF
6	VR4cntrl		Regulator 4 ON/OFF
7	VR5cntrl		Regulator 5 ON/OFF
8	GND		Ground
9	VR5	2.8V	Regulator 5 output
10	Vcc2	VBAT	VR4 and VR5 common input voltage
11	VR4	2.8V	Regulator 4 output
12	VR3	2.8V	Regulator 3 output
13	VR2	2.8V	Regulator 2 output
14	VR1	2.8V	Regulator 1 output
15	Vcc1	VBAT	VR1, VR2 and VR3 common input voltage
16	N/C		Not connected

TDMA1900 UPCONVERTER

Pin #	Pin name	Nominal level	Description
1	VDD1	2.8V	Supply voltage
2	N/C		Not connected
3	N/C		Not connected
4	GND	0	Ground
5	LO IN	?	TX local input
6	GND	0	Ground
7	RF OUT	?	RF output
8	VDD2	2.8V	Supply voltage
9	N/C		Not connected
10	N/C	–	Not connected
11	GND	–	Ground
12	VDD3	2.8V	Supply voltage
13	GND	0	Ground
14	IF IN	–	Intermediate frequency input
15	N/C	–	Not connected
16	TX ENA		TX enable

TDMA1900 PLL

Pin #	Pin name	Nominal level	Description
1	FAST	2.8V	Enable input for fast chargepump
2	CPF		Fast charge pump output
3	CP		Normal charge pump output
4	VDD2	2.8V	Power supply voltage
5	Vss3	0	Ground
6	RFI	?	Main divider input
7	Vss2	0	Ground
8	POL	2.8V	polarity select
9	PON	2.8V	Power on input
10	Vss1	0	Ground
11	CLK	?	Programming bus clock input
12	DATA	?	Programming bus data input
13	E	?	Programming bus enable input
14	Vdd1	–	Power supply voltage
15	XTALB	–	Complementary crystal frequency input
16	XTALA	–	Complementary crystal frequency input
17	GND(CP)	0	Ground for charge pump
18	Vcc	4.8V	Supply voltage for charge pump
19	Iset	–	charge pump currents setting
20	LOCK	–	Out of lock detector